NCV891330

3 A, 2 MHz Low-I_Q Dual-Mode Step-Down Regulator for Automotive

The NCV891330 is a Dual Mode regulator intended for Automotive, battery−connected applications that must operate with up to a 45 V input supply. Depending on the output load, it operates either as a PWM Buck Converter or as a Low Drop−Out Linear Regulator, and is suitable for systems with low noise and Low Quiescent Current requirements often encountered in automotive driver information systems. A reset pin (with fixed delay) simplifies interfacing with a microcontroller.

The NCV891330 also provides several protection features expected in automotive power supply systems such as current limit, short circuit protection, and thermal shutdown. In addition, the high switching frequency produces low output voltage ripple even when using small inductor values and an all−ceramic output filter capacitor – forming a space−efficient switching regulator solution.

Features

- 30 μA Iq in Light Load Condition
- 3.0 A Maximum Output Current in PWM Mode
- Internal N−channel Power Switch
- V_{IN} Operating Range 3.7 V to 36 V
- Withstands Load Dump to 45 V
- Logic Level Enable Pin can be Tied to Battery
- Fixed Output Voltage of 5.0 V, 4.0 V or 3.3 V
- 2 MHz Free−running Switching Frequency
- ±2 % Output Voltage Accuracy
- NCV Prefix for Automotive Requiring Site and Control Changes
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Audio
- Infotainment
- Instrumentation
- Safety−Vision Systems

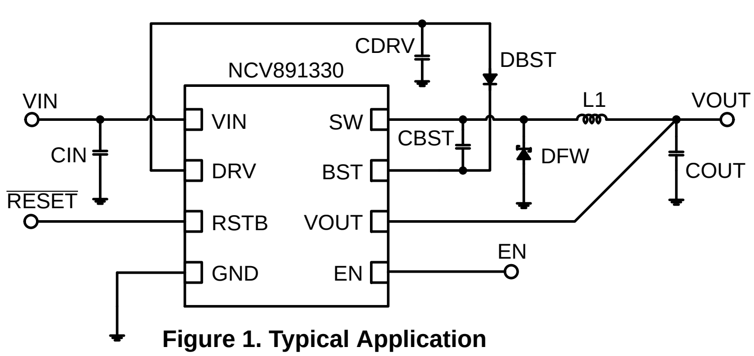

Figure 1. Typical Application

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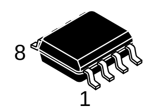
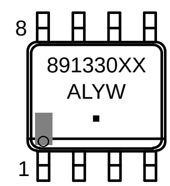


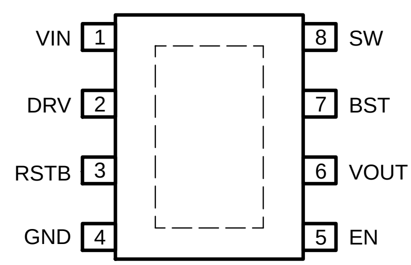
SOIC−8
EXPOSED PAD
CASE 751AC

MARKING DIAGRAM



With XX	=	33 for 3.3 V Output
		40 for 4.0 V Output
		50 for 5.0 V Output
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Device

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

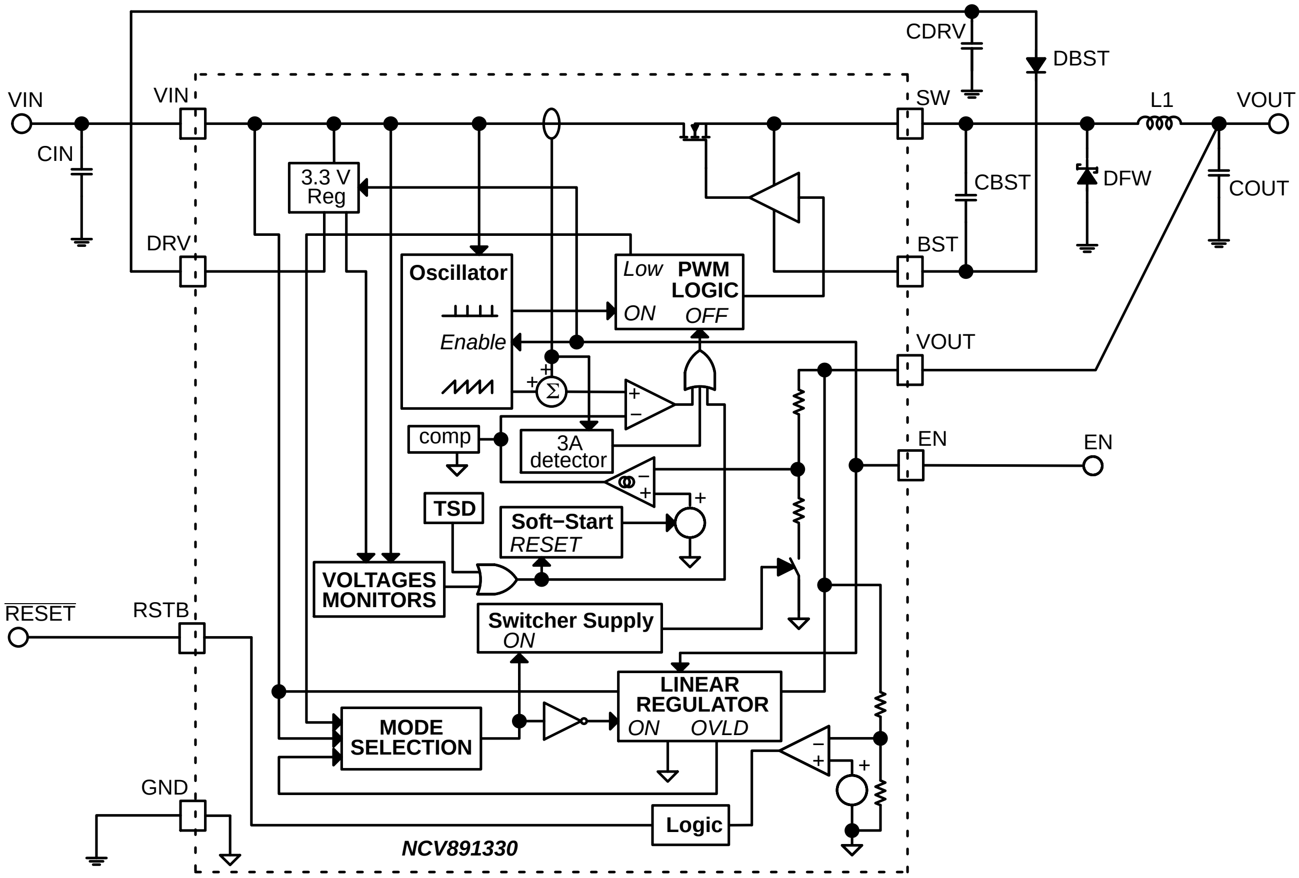


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	VIN	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	DRV	Output voltage to provide a regulated voltage to the Power Switch gate driver.
3	RSTB	Reset function. Open drain output, pulling down to ground when the output voltage is out of regulation.
4	GND	Battery return, and output voltage ground reference.
5	EN	This TTL compatible Enable input allows the direct connection of Battery as the enable signal. Grounding this input stops switching and reduces quiescent current draw to a minimum.
6	VOUT	Output voltage feedback and LDO output. Feedback of output voltage used for regulation, as well as LDO output in LDO mode.
7	BST	Bootstrap input provides drive voltage higher than VIN to the N−channel Power Switch for minimum switch Rdson and highest efficiency.
8	SW	Switching node of the Regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
EPAD		Connect to Pin 4 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Min/Max Voltage VIN			−0.3 to 45	V
Max Voltage VIN to SW			45	V
Min/Max Voltage SW			−0.7 to 40	V
Min Voltage SW − 20 ns			−3.0	V
Min/Max Voltage EN			−0.3 to 40	V
Min/Max Voltage VIN to EN			−1.5 to 45	V
Min/Max Voltage BST			−0.3 to 43	V
Min/Max Voltage BST to SW			−0.3 to 3.6	V
Min/Max Voltage on RSTB			−0.3 to 6	V
Min/Max Voltage VOUT			−0.3 to 18	V
Min/Max Voltage DRV			−0.3 to 3.6	V
Thermal Resistance, SOIC8−EP Junction–to–Ambient (Note 1)		$R_{\theta JA}$	30	°C/W
Storage Temperature range			−55 to +150	°C
Operating Junction Temperature Range		T_J	−40 to +150	°C
ESD withstand Voltage (Note 2)	Human Body Model	VESD	2.0	kV
Moisture Sensitivity		MSL	Level 2	
Peak Reflow Soldering Temperature (Note 3)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Value based on 4 layers of 645 mm^2 (or 1 in^2) of 1 oz copper thickness on FR4 PCB substrate.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. ELECTRICAL CHARACTERISTICS
V_{IN} = 4.5 to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3 V, C_{DRV} = 0.1 μF, for typical values T_J = 25°C, Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Quiescent Current, enabled	V_{IN} = 13.2 V, I_{OUT} = 100 μA, 25°C	I_q		30	39	μA
Quiescent Current, shutdown	V_{IN} = 13.2 V, V_{EN} = 0 V, 25°C	I_{qSD}		9	12	μA
UNDERVOLTAGE LOCKOUT – VIN (UVLO)						
UVLO Start Threshold	V_{IN} rising	V_{UVLSTT}	4.1		4.5	V
UVLO Stop Threshold	V_{IN} falling	V_{UVLSTP}	3.1		3.7	V
UVLO Hysteresis		V_{UVLOHY}	0.4		1.4	V
SOFT−START (SS)						
Soft−Start Completion Time		t_{SS}	0.8	1.4	2.0	ms
OUTPUT VOLTAGE						
Output Voltage during regulation	100 μA < I_{OUT} < 2.5 A 5.0 V option 4.0 V option 3.3 V option	V_{OUTreg}	 4.9 3.92 3.234	 5.0 4.0 3.3	 5.1 4.08 3.366	V

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Table 3. ELECTRICAL CHARACTERISTICS
V_{IN} = 4.5 to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3 V, C_{DRV} = 0.1 μF, for typical values T_J = 25°C, Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency	4.5 < V_{IN} < 18 V 20 V < V_{IN} < 28V	F_{SW} $F_{SW(HV)}$	1.8 0.9	2.0 1.0	2.2 1.1	MHz
VIN FREQUENCY FOLDBACK MONITOR						
Frequency Foldback Threshold V_{IN} rising V_{IN} falling		V_{FLDUP} V_{FLDDN}	18.4 18		20 19.8	V
Frequency Foldback Hysteresis		V_{FLDHY}	0.2	0.3	0.4	V
MODE TRANSITION						
Normal to Low−Iq mode Current Threshold	8 V < V_{IN} < 28 V	I_{NtoL}	3		40	mA
Mode Transition Duration Switcher to Linear Linear to Switcher		$t_{SWtoLIN}$ $t_{LINtoSW}$		300 1	 2	μs
Minimum time in Normal Mode before starting to monitor output current		$t_{SWblank}$		500		μs
Linear to switcher transition at high Vin at low Vin	V_{OUT} = 3.3 V	$V_{LINtoSW(HV)}$ $V_{LINtoSW(LV)}$	19 3.6		28 4.5	V
PEAK CURRENT LIMIT						
Current Limit Threshold		I_{LIM}	3.9	4.4	4.9	A
POWER SWITCH						
ON Resistance	V_{BST} = V_{SW} + 3.0 V	R_{DSON}		180	360	mΩ
Leakage current VIN to SW	V_{SW} = 0, −40°C ≤ T_J ≤ 85°C	I_{LKSW}			10	μA
Minimum ON Time	Measured at SW pin	t_{ONMIN}	45		70	ns
Minimum OFF Time	Measured at SW pin At F_{SW} = 2 MHz (normal) At F_{SW} = 500 kHz (max duty cycle)	t_{OFFMIN}	 30	 30 50	 70	ns
SLOPE COMPENSATION						
Ramp Slope (With respect to switch current)	4.5 < V_{IN} < 18 V 20 V < V_{IN} < 28V	S_{ramp} $S_{ramp(HV)}$	1.45 0.65	2.0 1.0	2.8 1.3	A/μs
LOW POWER LINEAR REGULATOR						
Line Regulation	I_{OUT} = 5 mA, 6 V < V_{IN} < 18 V	$V_{REG(line)}$		5	25	mV
Load Regulation	V_{IN} = 13.2 V, 0.1 mA < I_{OUT} < 50 mA	$V_{REG(load)}$		5	35	mV
Power Supply Rejection	$V_{OUT(ripple)}$ = 0.5 Vp−p, F = 100 Hz	PSRR		65		dB
Current Limit		$I_{LIN(lim)}$	50		80	mA
Output clamp current	V_{OUT} = $V_{OUTreg(typ)}$ + 10%	$I_{CL(OUT)}$	0.5	1.0	1.5	mA
SHORT CIRCUIT DETECTOR						
Switching frequency in short−circuit condition Analog Foldback Analog foldback – high V_{IN} Hiccup Mode	V_{OUT} = 0 V, 4.5 V < V_{IN} < 18 V V_{OUT} = 0 V, 20 V < V_{IN} < 28 V	F_{SWAF} F_{SWAFHV} F_{SWHIC}	450 225 24	550 275 32	650 325 40	kHz
RESET						
Leakage current into RSTB pin		I_{RSTBlk}			1	uA

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Table 3. ELECTRICAL CHARACTERISTICS
V_{IN} = 4.5 to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3 V, C_{DRV} = 0.1 μF, for typical values T_J = 25°C, Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET						
Output voltage threshold at which the RSTB signal goes low	V_{OUT} decreasing 5.0 V option 4.0 V option 3.3 V option	V_{RESET}	 4.50 3.6 2.97	 4.625 3.7 3.05	 4.75 3.8 3.14	V
Hysteresis on RSTB threshold	V_{OUT} increasing 5.0 V option 4.0 V option 3.3 V option	V_{REShys}	 25 20 17	 60 50 40	 100 80 66	mV
Noise−filtering delay	From V_{OUT}<V_{RESET} to RSTB pin going low	t_{filter}	10		25	μs
Restart Delay time	From V_{OUT}>V_{RESET}+V_{REShys} to high RSTB	t_{delay}	14	16	18	ms
Low RSTB voltage	$R_{RSTBpullup}$ = V_{OUTreg}/1 mA, V_{OUT} > 1 V	$V_{RSTBlow}$			0.4	V
GATE VOLTAGE SUPPLY (DRV pin)						
Output Voltage		V_{DRV}	3.1	3.3	3.5	V
DRV UVLO START Threshold		V_{DRVSTT}	2.7	2.9	3.05	V
DRV UVLO STOP Threshold		V_{DRVSTP}	2.5	2.8	3.0	V
DRV UVLO Hysteresis		V_{DRVHYS}	50		200	mV
DRV Current Limit	V_{DRV} = 0 V	I_{DRVLIM}	21		50	mA
VIN OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage Stop Threshold	V_{IN} increasing	V_{OVSTP}	36.5	37.7	39.0	V
Overvoltage Start Threshold	V_{IN} decreasing	V_{OVSTT}	36.0	37.3	38.8	V
Overvoltage Hysteresis		V_{OVHY}	0.25	0.40	0.50	V
ENABLE (EN)						
Logic low threshold voltage		V_{ENlow}	0.8			V
Logic high threshold voltage		V_{ENhigh}			2	V
EN pin input current		I_{ENbias}	0.2		1	μA
THERMAL SHUTDOWN						
Activation Temperature		TSD	155		190	°C
Reset temperature		$TSD_{restart}$	135		185	°C
Hysteresis		T_{HYS}	5		20	°C

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

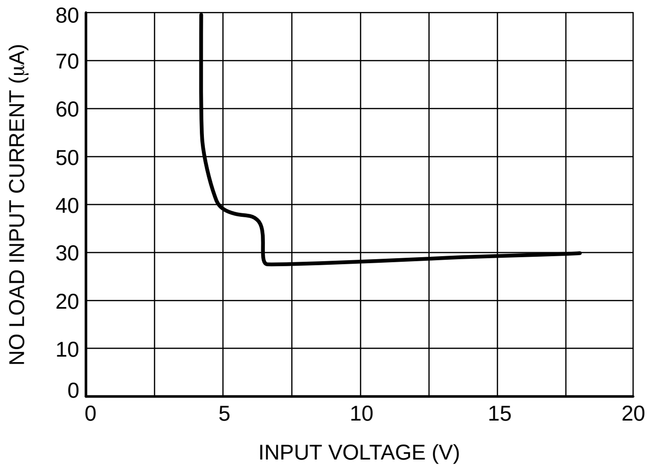


Figure 3. No−load Input Current at T_J = 25°C vs. Input Voltage

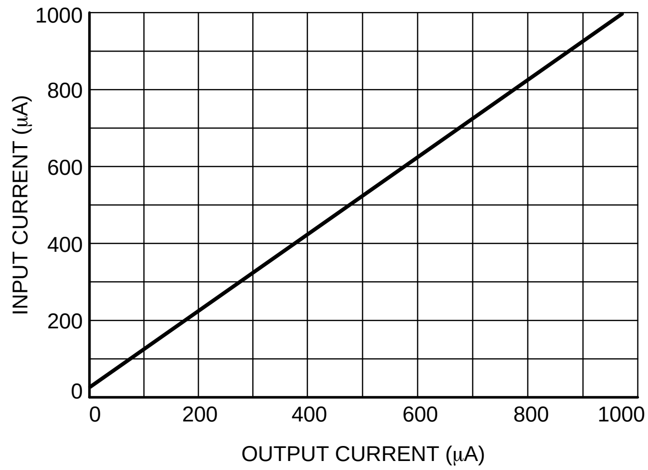


Figure 4. Input Current at T_J = 25°C vs. Output Current

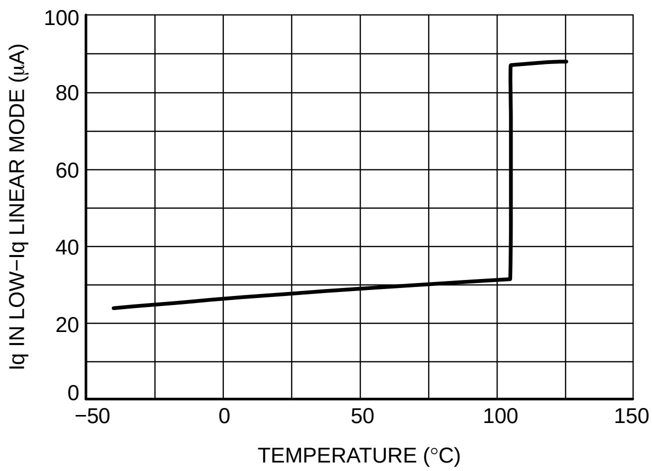


Figure 5. Low−Iq Mode Quiescent Current vs. Junction Temperature

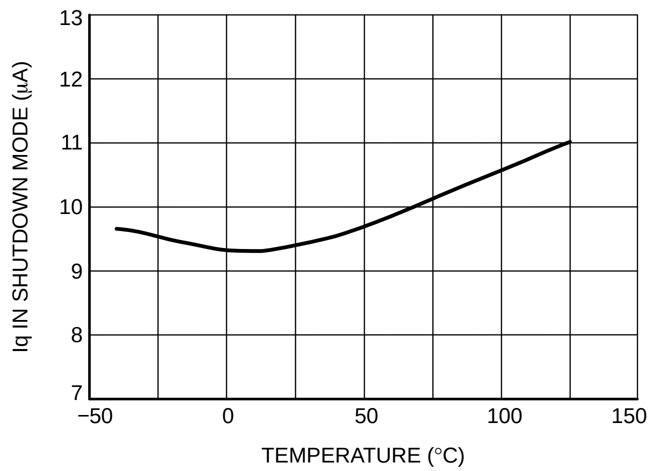


Figure 6. Shutdown Mode Quiescent Current vs. Junction Temperature

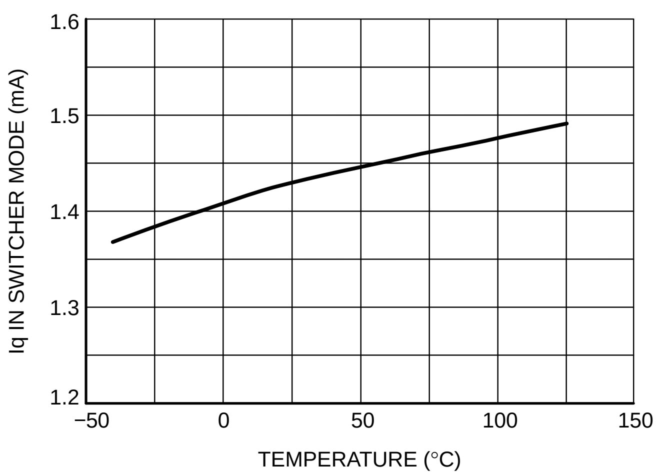


Figure 7. Switching Mode Quiescent Current vs. Junction Temperature

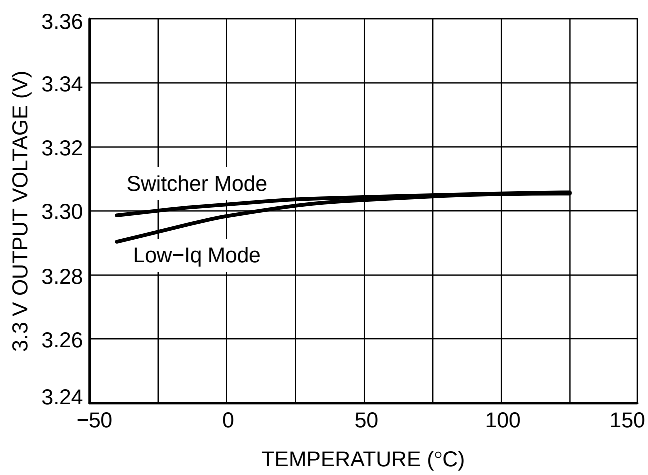


Figure 8. 3.3 V Output Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

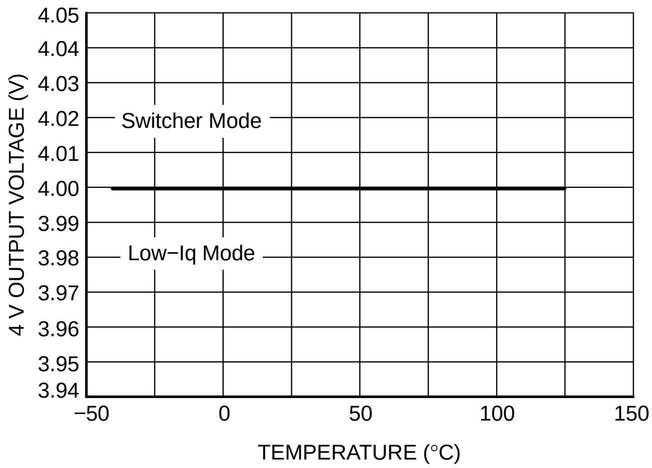


Figure 9. 4.0 V Output Voltage vs. Junction Temperature

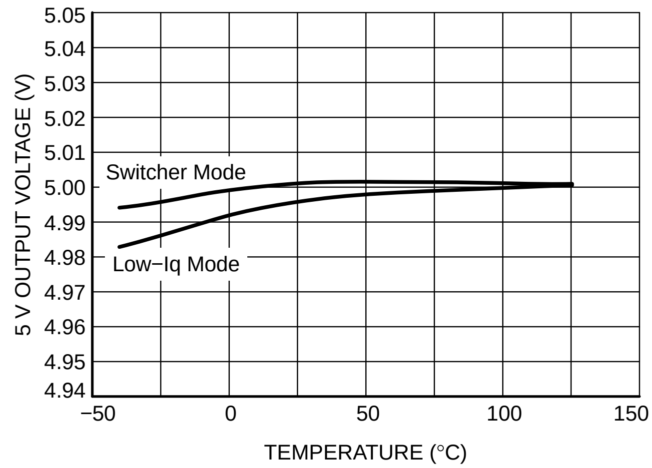


Figure 10. 5.0 V Output Voltage vs. Junction Temperature

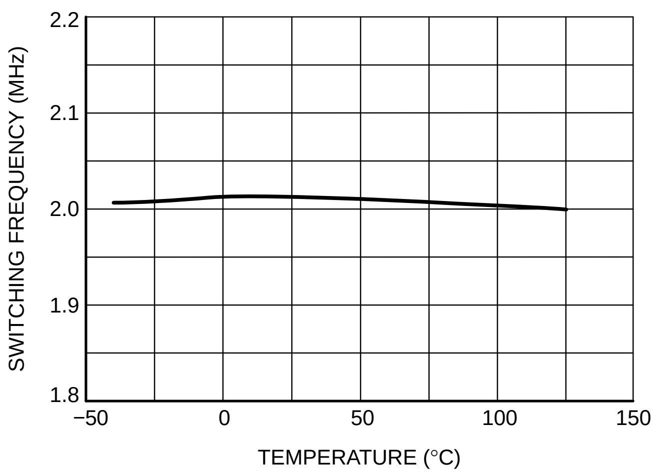


Figure 11. Switching Frequency vs. Junction Temperature

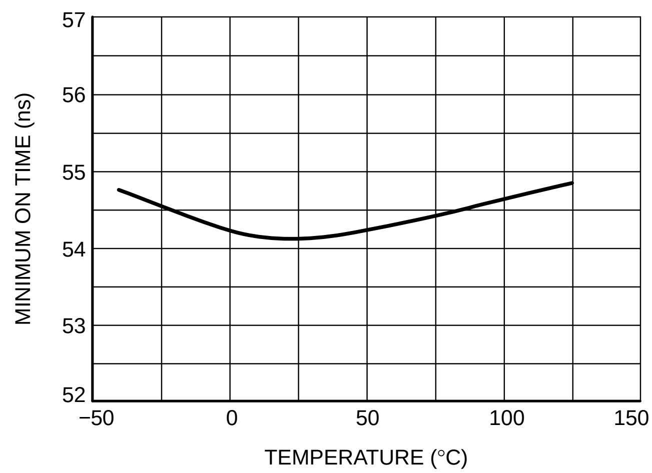


Figure 12. Minimum On Time vs. Junction Temperature

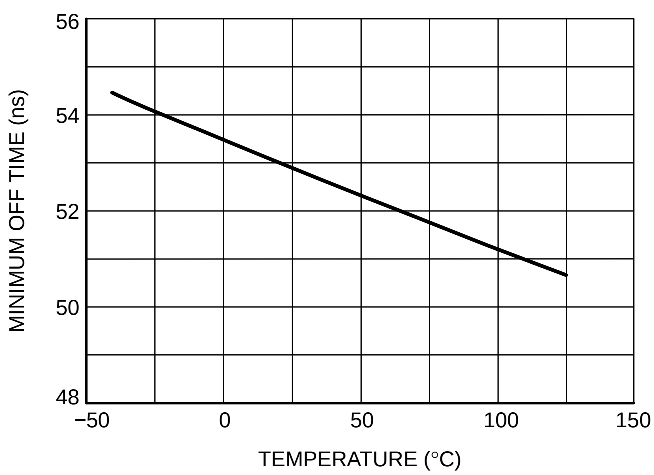


Figure 13. Minimum Off Time vs. Junction Temperature

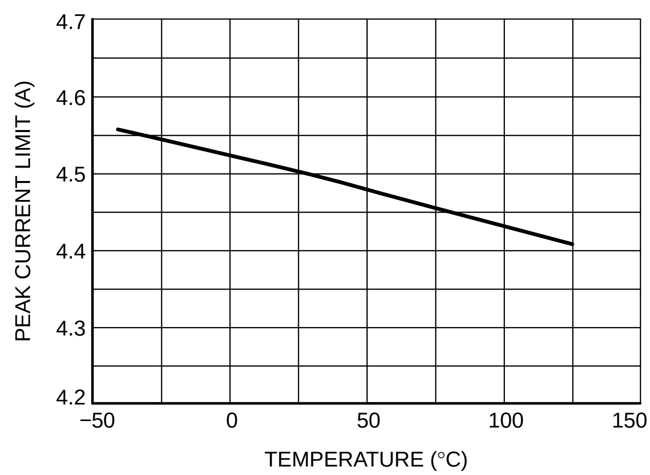


Figure 14. Peak Current Limit vs. Junction Temperature

TYPICAL CHARACTERISTICS

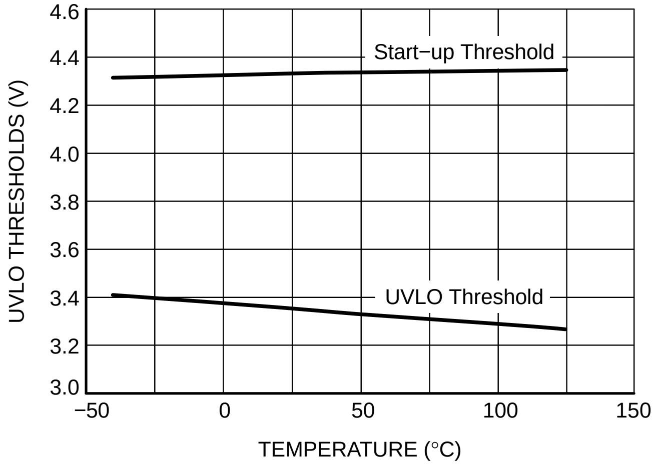


Figure 15. UVLO Thresholds vs. Junction Temperature

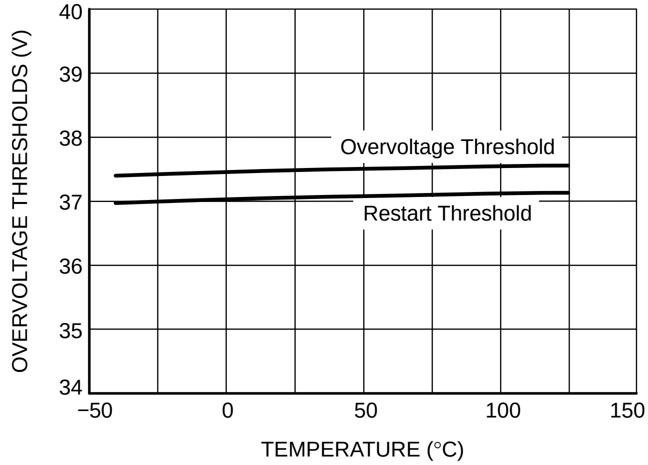


Figure 16. Input Overvoltage Thresholds vs. Junction Temperature

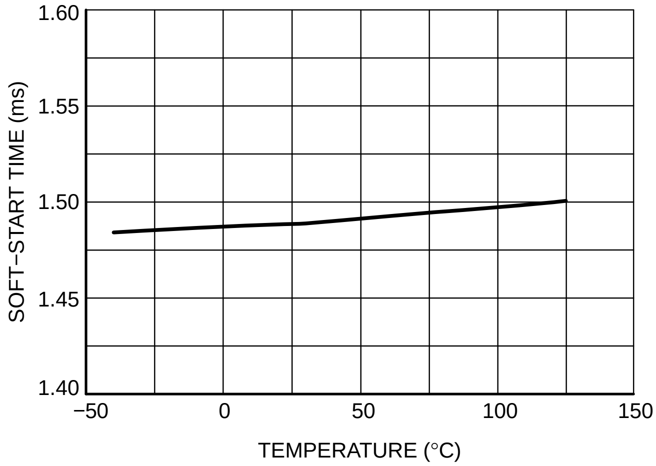


Figure 17. Soft−start Duration vs. Junction Temperature

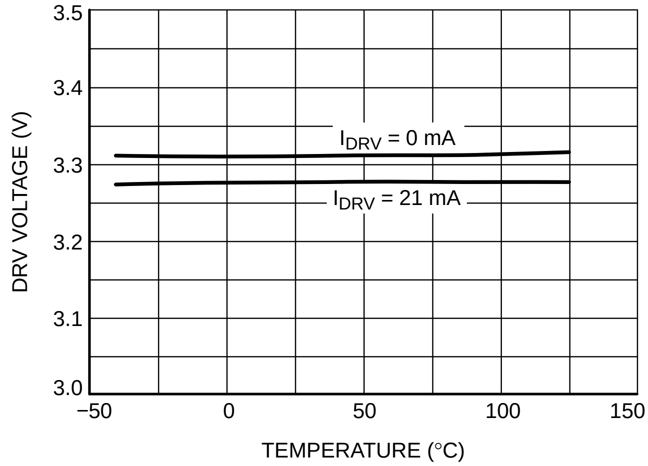


Figure 18. DRV Voltage vs. Junction Temperature

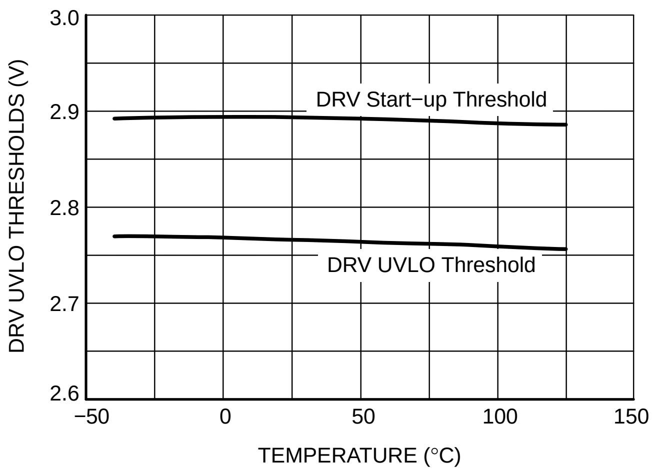


Figure 19. DRV Voltage UVLO Tresholds vs. Junction Temperature

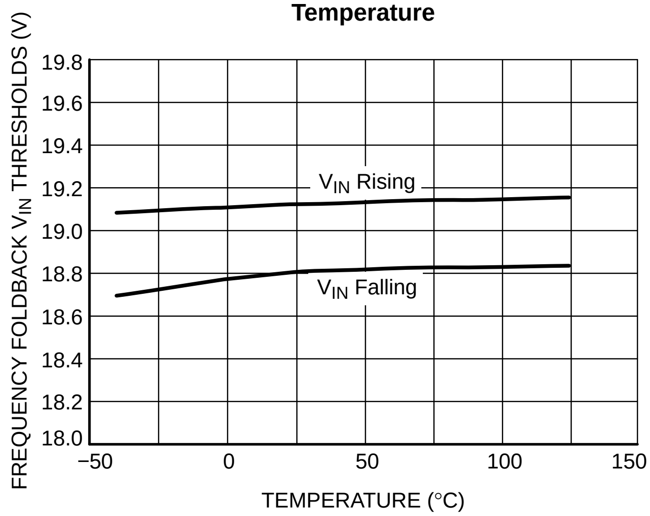


Figure 20. Frequency Foldback Voltage Tresholds vs. Junction Temperature

TYPICAL CHARACTERISTICS

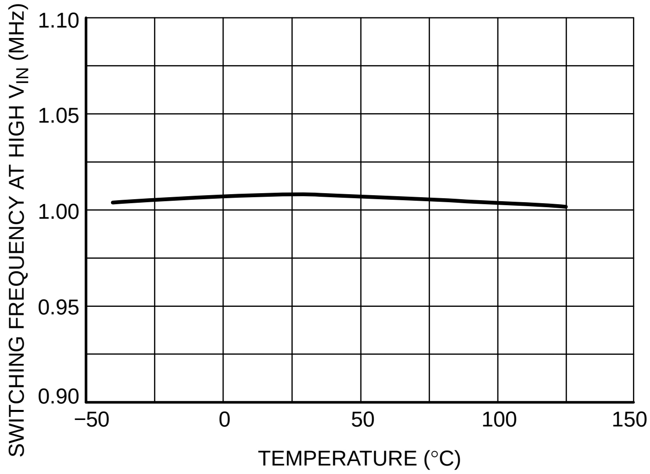


Figure 21. Foldback Frequency vs. Junction Temperature

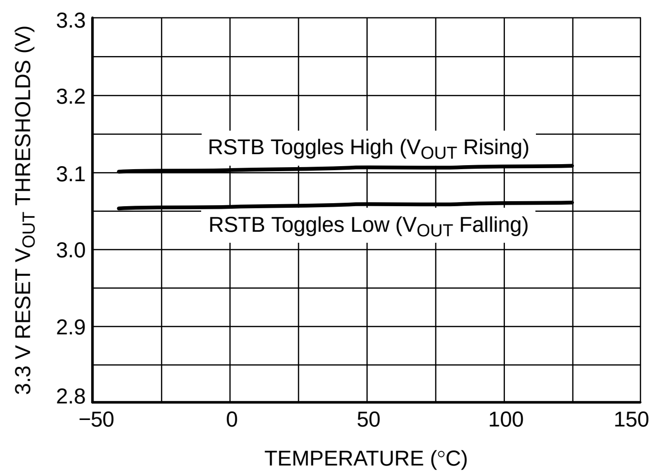


Figure 22. 3.3 V Version RESET Thresholds vs. Junction Temperature

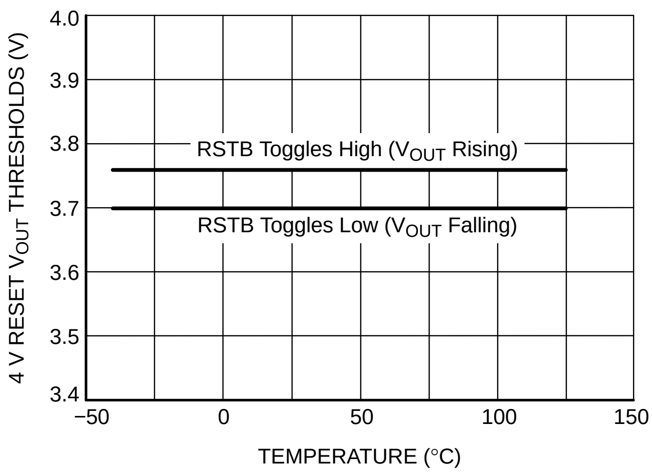


Figure 23. 4.0 V Version RESET Thresholds vs. Junction Temperature

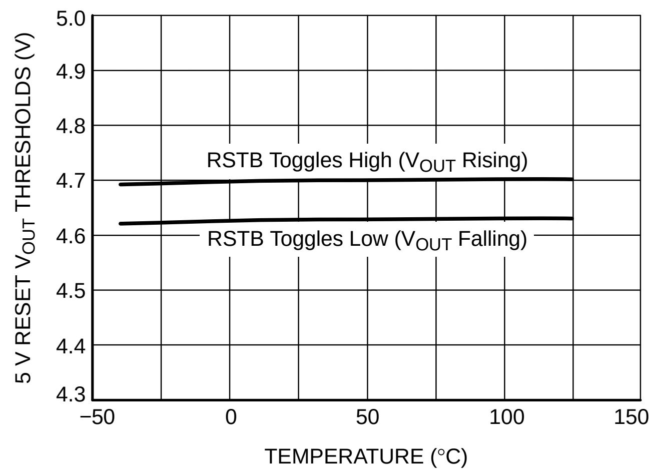


Figure 24. 5.0 V Version RESET Thresholds vs. Junction Temperature

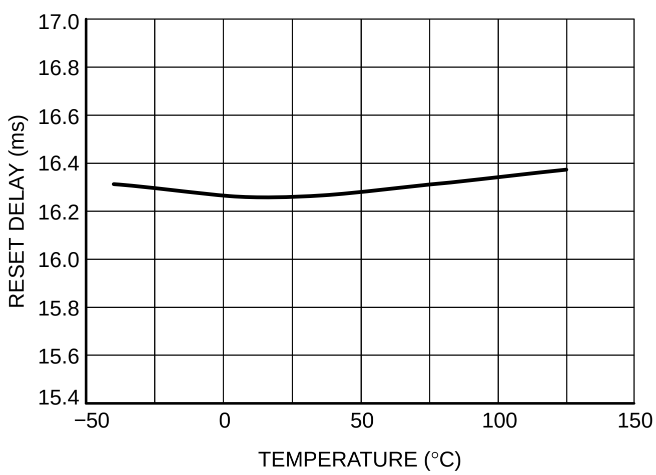


Figure 25. RESET Delay vs. Junction Temperature

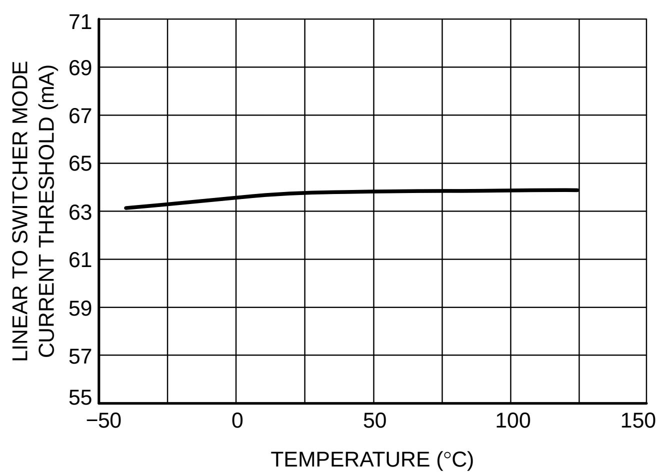


Figure 26. Low−Iq to Switcher Mode Transition vs. Junction Temperature

TYPICAL CHARACTERISTICS

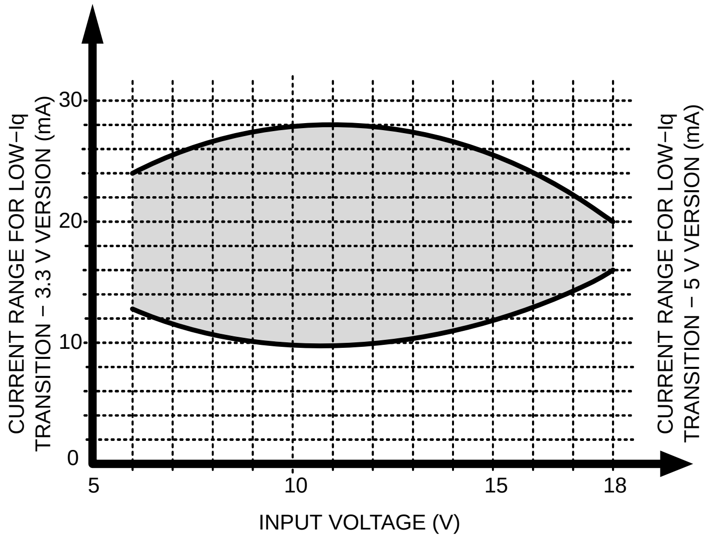


Figure 27. Switcher to Low−Iq Mode Transition (3.3 V Version, 2.2 μH) vs. Input Voltage

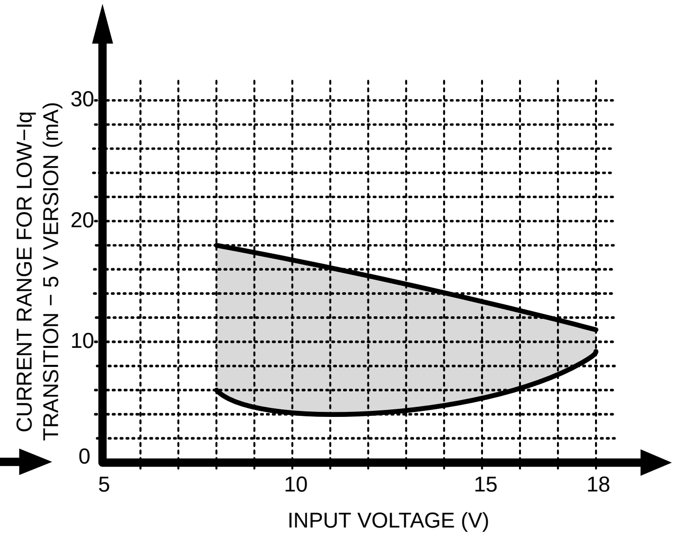


Figure 28. Switcher to Low−Iq Mode Transition (5.0 V Version, 2.2 μH) vs. Input Voltage

APPLICATION INFORMATION

Hybrid Low−Power Mode

A high−frequency switch−mode regulator is not very efficient in light load conditions, making it difficult to achieve low Iq requirements for sleep−mode operation. To remedy this, the NCV891330 includes a low−Iq linear regulator that turns on at light load, while the PWM regulator turns off, ensuring a high−efficiency low−power operation. Another advantage of linear mode is the tight regulation free of voltage ripple usually associated with low−Iq switchers in light load conditions.

At initial start−up the NCV891330 always runs in PWM converter mode, regardless of the output current, and goes through a soft start. It then stays in PWM mode if the output current is high enough. If the output current is low, the NCV891330 transitions to Linear Regulator mode, after a 300 μs period during which it assesses the level of ouput current. Note that the Reset signal needs to be high before the IC starts to look at the output current level.

It stays in this low−power mode until the output current exceeds the $I_{LINtoSW}$ limit: it then transitions to PWM converter mode. This transition happens in less than 2 μs, so that the transient response is not affected by the mode change.

Once the NCV891330 has transitioned to switcher mode, it cannot go back to low−Iq mode before a 500 μs blanking period has elapsed, after which it starts looking at the output current level.

If the NCV891330 is in Low−Iq Linear Regulator mode in normal battery range, it will transition to switcher mode when V_{IN} increases above $V_{LINtoSW(HV)}$, regardless of the output current. Similarly, if the NCV891330 is in PWM mode and V_{IN} is higher than V_{FLDUP}, it will not transition to Low−Iq Linear mode even if the output current becomes lower than I_{NtoL}.

At low input voltage, the NCV891330 stays in low−Iq mode down to $V_{LINtoSW(LV)}$ if it entered this mode while in normal battery range. However it may not enter low−Iq mode below 8 V depending on the charge of the bootstrap capacitor (see Bootstrap section and typical characteristics curves for details).

Figures 29 and 30 show a mode transition for a large load transient, while Figures 5 and 6 show a transition on a small load transient.

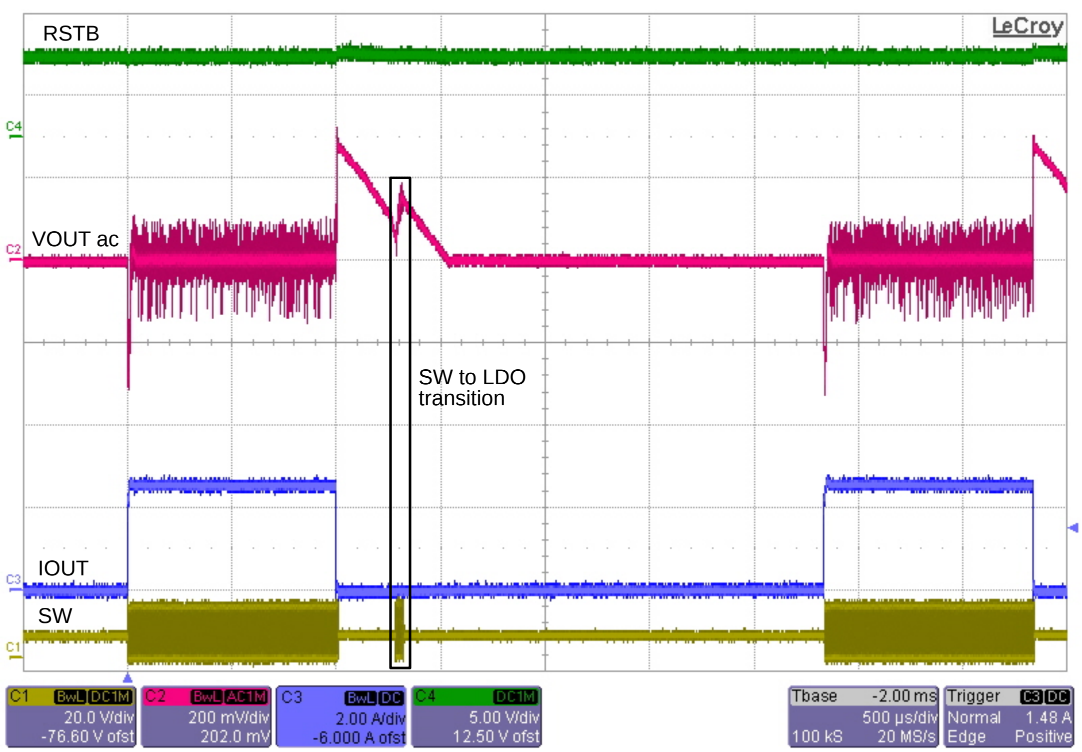


Figure 29. V_{IN} = 13 V, V_{OUT} = 5 V, 20 mA to 2.5 A at 1 A/μs – with Mode Transition

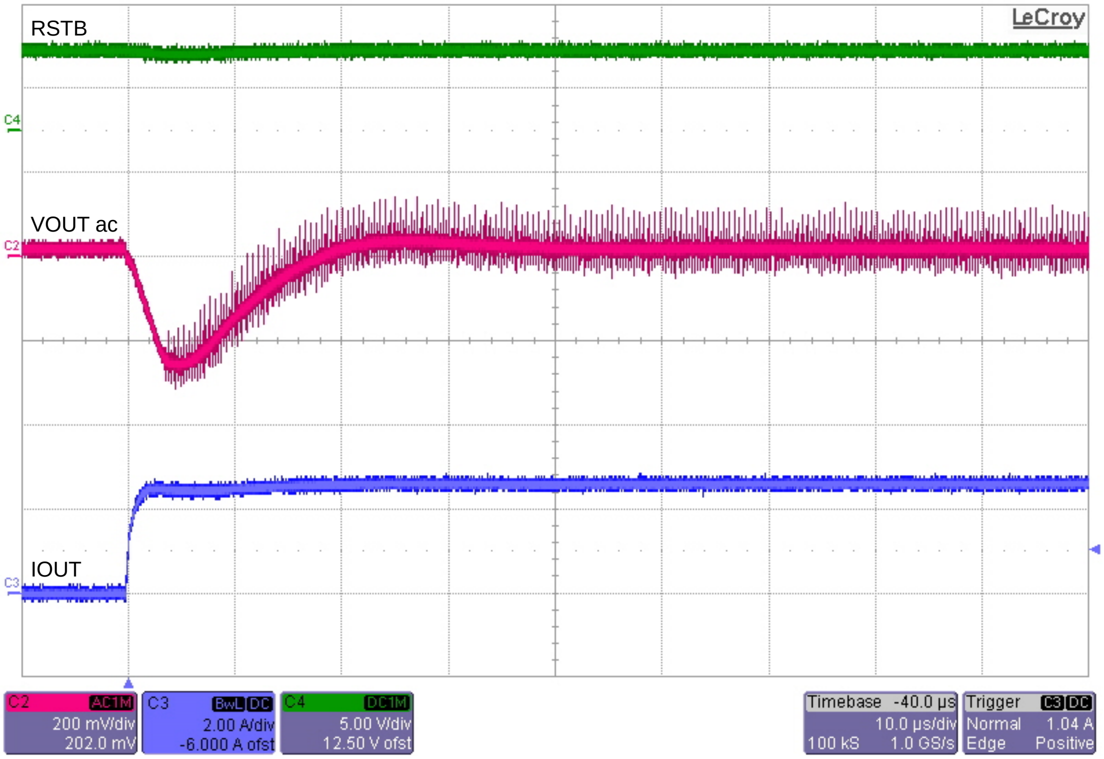


Figure 30. Detail of the 20 mA to 2.5 A Transition at V_{IN} = 13 V and V_{OUT} = 5 V

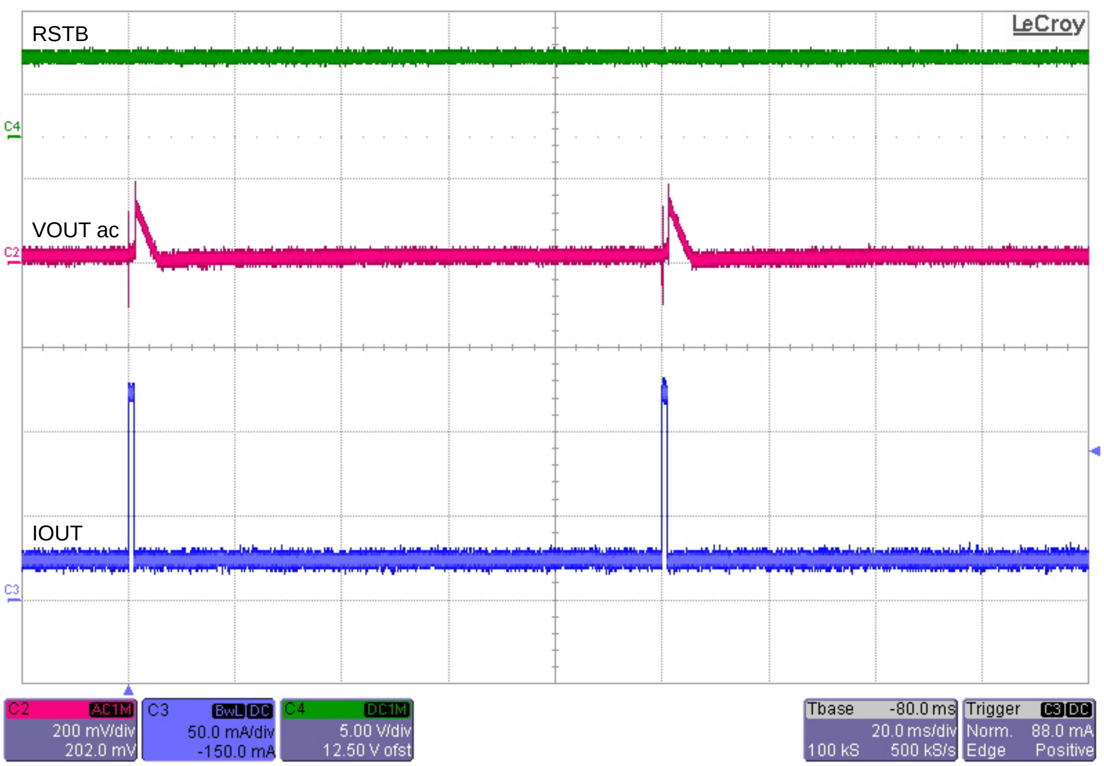


Figure 31. V_{IN} = 13 V, V_{OUT} = 5 V, 20 mA to 120 mA Load Transient – with Mode Transition

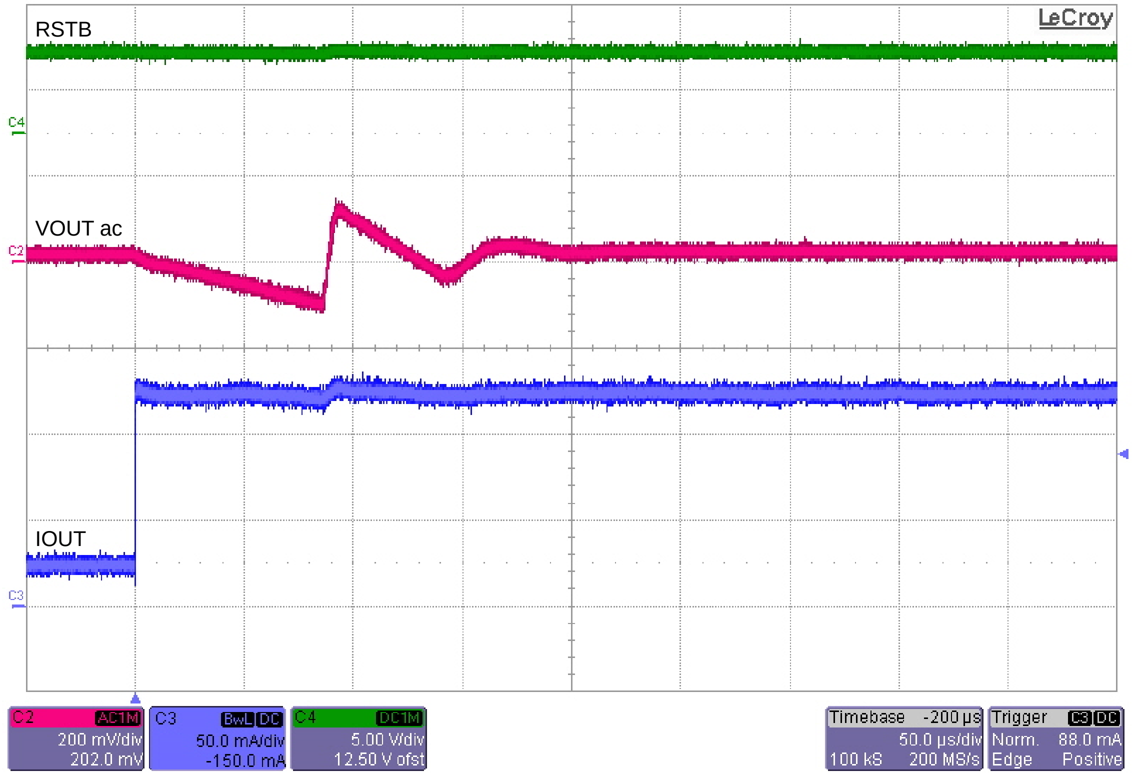


Figure 32. Detail of the 20 mA to 120 mA Transition at V_{IN} = 13 V and V_{OUT} = 5 V

Figure 33 shows a load transient for which no mode transition occurred.

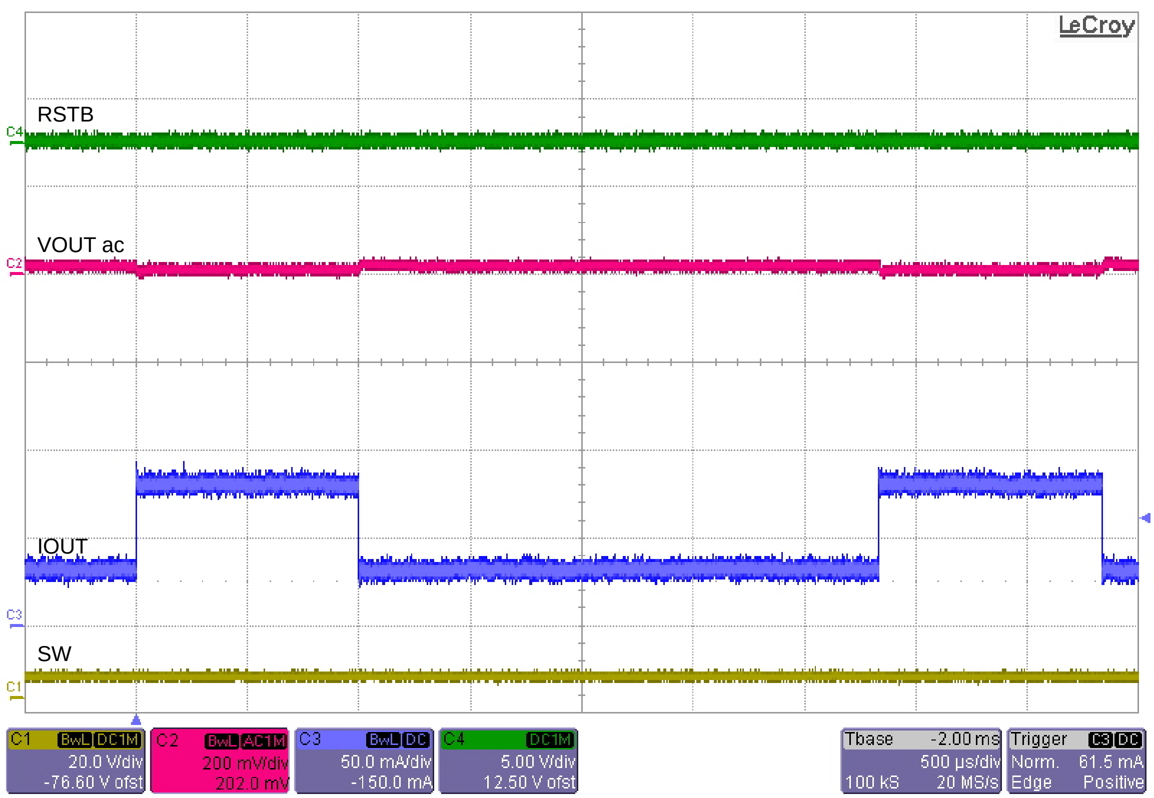


Figure 33. V_{IN} = 13 V, V_{OUT} = 5 V, 20 mA to 70 mA Load Transient – LDO Mode Only (no transition)

Input Voltage

An Undervoltage Lockout (UVLO) circuit monitors the input, and can inhibit switching and reset the Soft−start circuit if there is insufficient voltage for proper regulation. Depending on the output conditions (voltage option and loading), the NCV891330 may lose regulation and run in drop−out mode before reaching the UVLO threshold: refer to the Minimum Vin calculation tool for details. When the input voltage drops low enough that the part cannot regulate because it reaches its maximum duty cycle, the switching frequency is divided down by up to 4 (down to 500 kHz). This helps lowering the minimum voltage at which the regulator loses regulation.

An overvoltage monitoring circuit automatically terminates switching if the input voltage exceeds V_{OVSTP} (see Figure 34), but the NCV891330 can withstand input voltages up to 45 V.

To avoid skipping switching pulses and entering an uncontrolled mode of operation, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{IN} Frequency Foldback threshold (see Figure 34). Frequency reduction is automatically terminated when the input voltage drops back below the V_{IN} Frequency Foldback threshold. This also helps to limit the power lost in switching and generating the drive voltage for the Power Switch.

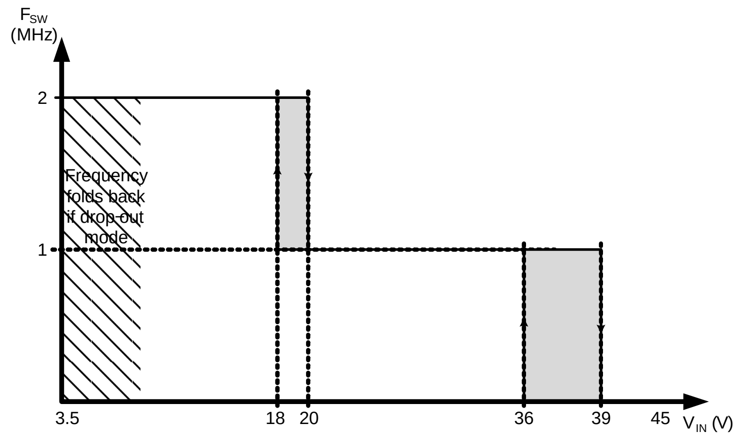


Figure 34. NCV891330 Switching Frequency Profile vs. Input Voltage

Soft−Start

Upon being enabled or released from a fault condition, and after the DRV voltage is established, a soft−start circuit ramps the switching regulator error amplifier reference voltage to the final value. During soft−start, the average switching frequency is lower until the output voltage approaches regulation.

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub−harmonic oscillations. The recommended inductor values are 2.2 or 3.3 μH, although higher values are possible.

Current Limiting

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 35 shows – for a 2.2 μH inductor – how the variation of inductor peak current with input voltage affects the maximum DC current the NCV891330 can deliver to a load.

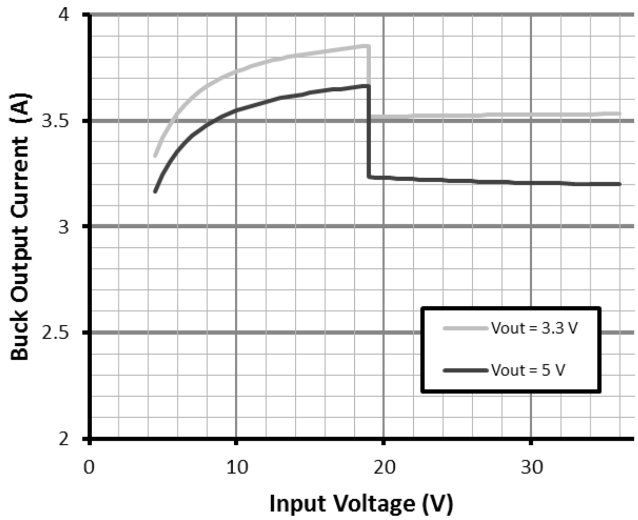


Figure 35. NCV891330 Load Current Capability with a 2.2 μH Inductor

Short Circuit Protection

During severe output overloads or short circuits, the NCV891330 automatically reduces its switching frequency. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed.

In more severe short−circuit conditions where the inductor current is still too high after the switching frequency has fully folded back, the regulator enters a hiccup mode that further reduces the power dissipation and protects the system.

RESET Function

The RSTB pin is pulled low when the output voltage falls below 7.5% of the nominal regulation level, and floats when the output is properly regulated. A pull−up resistor tied to the output is needed to generate a logic high signal on this open drain pin. The pin can be left unconnected when not used.

When the output voltage drops out of regulation, the pin goes low after a short noise−filtering delay (t_{filter}). It stays low for a 16 ms delay time after the output goes back to regulation, simplifying the connection to a micro−controller.

The RSTB pin is also pulled low immediately in case of VIN overvoltage, Thermal shutdown, VIN UVLO or DRV UVLO.

Feedback Loop

All components of the feedback loop (output voltage sensing, error amplifier and compensation) are integrated inside the NCV891330, and are optimized to ensure regulation and sufficient phase and gain margin for the recommended conditions of operation.

Recommended conditions and components:

- Input: car battery
- Output: 3.3 V, 4 V or 5 V, with output current up to 3 A
- Output capacitor: one to three parallel ceramic 10 μF capacitors
- Inductor: 2.2 μH to 3.3 μH

With these operating conditions and components, the open loop transfer function has a phase margin greater than 50°, as can be seen in Figure 36.

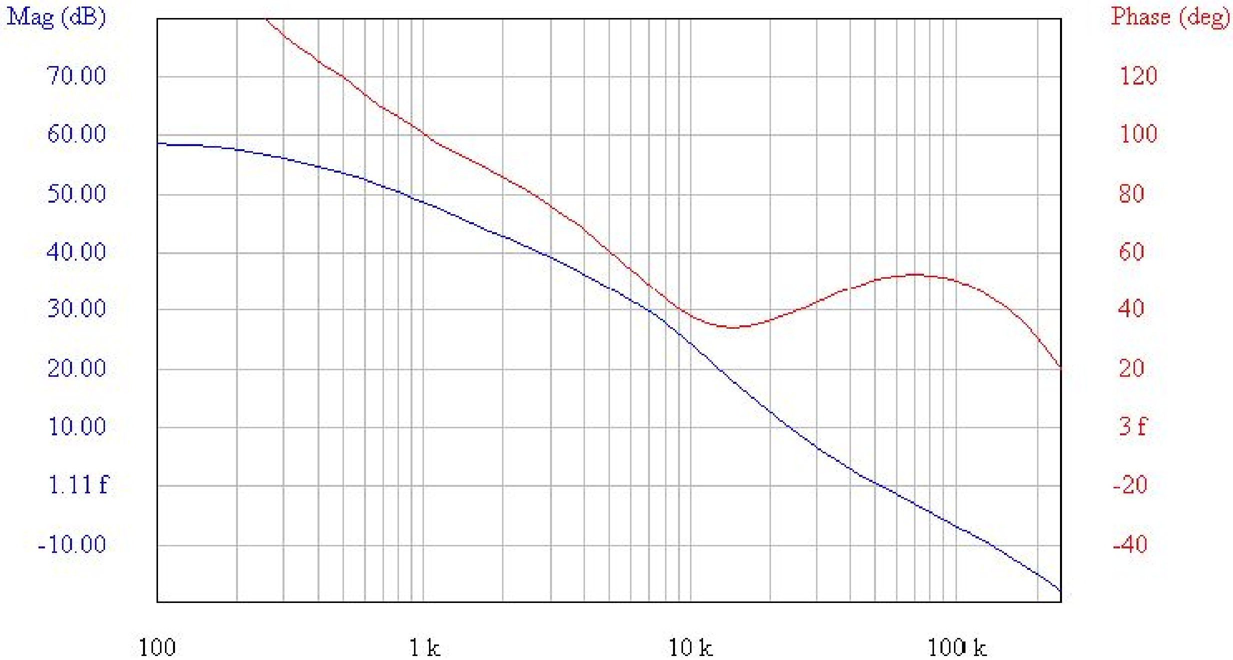


Figure 36. Bode Plot of the Open Loop Transfer Function of a Buck Converter using the NCV891330 for Vin = 13 V, Vout = 3.3 V, Iout = 2 A, Cout=3x10 μF and L=2.2 μH

For more details and for effect of component values other than the recommended ones, please refer to the design spreadsheet provided on the www.onsemi.com NCV891330 page.

The total open loop transfer function (from output voltage sensing at the NCV891330 VOUT pin to output voltage) can be modeled using the following equation:

$$G_{Loop}(s) = G_{L0} \cdot \frac{1 + \frac{s}{1.48 \times 10^5}}{\left(1 + \frac{s}{1.26 \times 10^3}\right) \cdot \left(1 + \frac{s}{1.85 \times 10^6}\right)} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \cdot \frac{1}{1 + \frac{s}{\omega_n \cdot Q_p} + \frac{s^2}{\omega_n{}^2}}$$

With:

$$G_{L0} = \frac{1.54 \times 10^4 \cdot V_{OUT}}{I_{OUT} \cdot \left(1 + \frac{V_{OUT}}{L \cdot F_{sw} \cdot I_{OUT}}\right) \cdot \left[\left(1 + \frac{2.0 \times 10^6 \cdot L}{V_{IN} - V_{OUT}}\right) \cdot (1 - D) - 0.5\right]}$$

$$\omega_z = \frac{1}{R_{ESR(C_{OUT})} \cdot C_{OUT}}$$

$$\omega_p = \frac{I_{OUT}}{V_{OUT} \cdot C_{OUT}} + \frac{\left(1 + \frac{2.0 \times 10^6 \cdot L}{V_{IN} - V_{OUT}}\right) \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot F_{sw}}$$

$$\omega_n = \pi \cdot F_{sw}$$

$$Q_p = \frac{1}{\pi \cdot \left[\left(1 + \frac{2.0 \times 10^6 \cdot L}{V_{IN} - V_{OUT}}\right) \cdot (1 - D) - 0.5\right]}$$

This equation is used in the design spreadsheet provided on the www.onsemi.com NCV891330 page.

Bootstrap

At the DRV pin an internal regulator provides a ground−referenced voltage to an external capacitor (C_{DRV}), to allow fast recharge of the external bootstrap capacitor (C_{BST}) used to supply power to the power switch gate driver. If the voltage at the DRV pin goes below the DRV UVLO Threshold V_{DRVSTP}, switching is inhibited and the Soft−start circuit is reset, until the DRV pin voltage goes back up above V_{DRVSTT}.

The NCV891330 permanently monitors the bootstrap capacitor, and always ensures it stays charged no matter what the operating conditions are. As a result, the additional charging current for the bootstrap capacitor may prevent the regulator from entering Low−Iq mode at low input voltage. Practically, the 5 V output version does not enter Low−Iq mode for input voltages below 8 V, and the 4 V version for input voltages below 6.5 V (see typical characteristics curves for details).

Enable

The NCV891330 is designed to accept either a logic level signal or battery voltage as an Enable signal. However if voltages above 40 V are expected, EN should be tied to VIN through a 10 kΩ resistor in order to limit the current flowing into the overvoltage protection of the pin.

EN low induces a shutdown mode which shuts off the regulator and minimizes its supply current to 9 μA typical by disabling all functions.

Upon enabling, voltage is established at the DRV pin, followed by a soft−start of the switching regulator output.

Thermal Shutdown

A thermal shutdown circuit inhibits switching, resets the Soft−start circuit, and removes DRV voltage if internal temperature exceeds a safe level. Switching is automatically restored when temperature returns to a safe level.

Exposed Pad

The exposed pad (EPAD) on the back of the package must be electrically connected to the electrical ground (GND pin) for proper, noise−free operation.

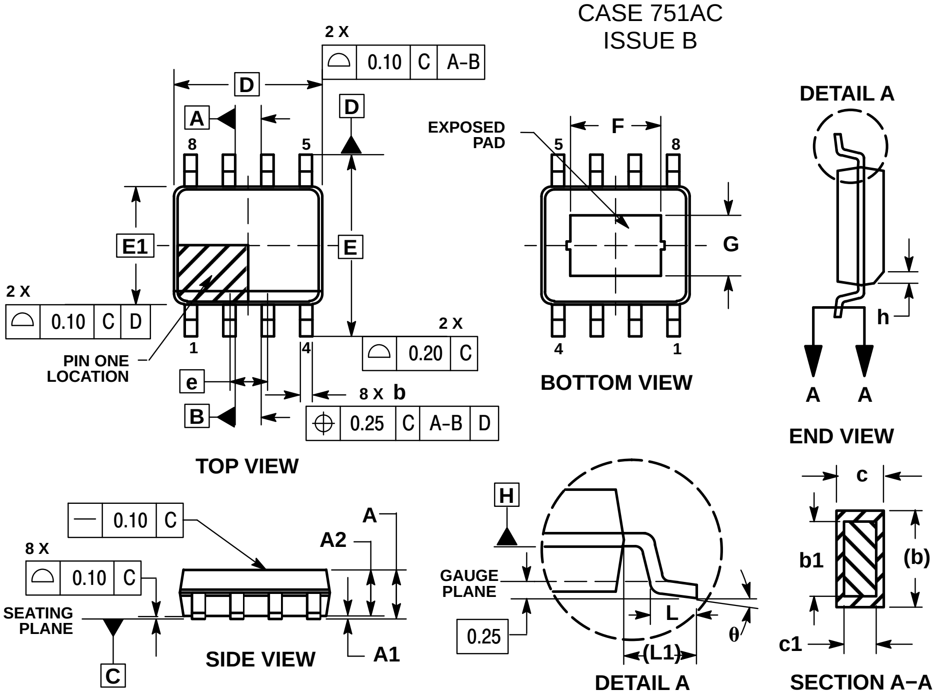
ORDERING INFORMATION

Device	Output	Package	Shipping
NCV891330PD50R2G	5.0 V	SOIC−8 EP	2500 / Tape & Reel
NCV891330PD40R2G	4.0 V		
NCV891330PD33R2G	3.3 V		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

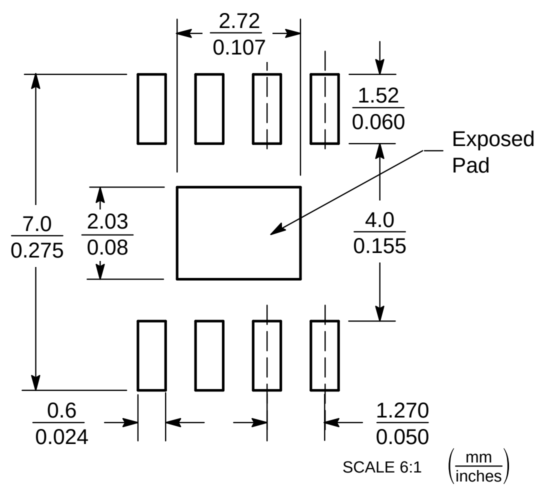
SOIC−8 EP
CASE 751AC
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

SOLDERING FOOTPRINT



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