CSE 433 Embedded Systems Project 0

Due Date April 2, 2021

Combinational Circuits
Design & Simulation with Intel Quartus

You will design a circuit and simulate using Quartus II and ModelSim software. For that purpose,

1. First download and install free Quartus II Web Edition (including ModelSim) from:
https://fpgasoftware.intel.com/13.1/?edition=web&platform=windows

2. You will design the circuit in Verilog, using either structural Verilog or dataflow model (assign statement). Behavioral Verilog is not allowed.

3. You will write a Verilog benchmark file so that you can fully test your circuit. This benchmark will prove the functionality of your designed circuit by writing the outputs for each different input. Then compare the results with the actual results you find using a C implementation. If they are same your design is OK. You will test all possible inputs.

The circuit will take two unsigned 8-bit numbers x and y as inputs and implement the following C code:

```
if(x + y < 400)
      z = x % 64 + 3 * y;
else
      z = x % 16 + 13 * y
```

Do not use any sequential component like registers and flip flops in your circuit.

Do not use any multiplier or '*' sign in your design.

Do not use any divisor or '/' sign in your design.

Submit your Verilog files and the simulation results with your report to Teams.

In your PDF report;

- explain your design
- draw a schematic for your design
- explain your Verilog testbench file
- show and explain the simulation results.

Design 40%, Simulation 40%, Report 20%. You can ask your questions to your TA, Fatma Nur.