# CSE 433 Assignment 2
# FSM in Verilog
# Due Date: May 19 Wednesday

In this assignment you will design a FSM in Verilog.

The inputs will be:

```
n: number of integers
num: 32-bit number
go_i: start signal
CLK: input clock for the FSM
```

The output will be:

```
x: the largest prime number in the array
ready: output ready signal.
```

You will first take n numbers and put them into a memory. You must take the numbers serially in a predefined clock speed or by a way of handshaking. It depends on you. Take them correctly and store them in the memory. For memory use IP catalog of Quartus.

Then you will find the largest prime number in the array. You are not allowed to use division or mod.

Try to be as fast as possible.

You will also write a testbench that takes numbers from a text file and inputs to your module one by one. Read the output when ready and display the output in Modelsim. You will verify your circuit using this testbench on Modelsim.