CSE 433 Embedded Systems Project 1

Due Date April 16, 2021

FSM Controller Design in Verilog

In this assignment, you will design a FSM controller in Verilog but without using all capabilities of Verilog. Actually, you will first draw the state diagram and derive the stat table and derive the Boolean expressions. Only after then you will implement the Boolean expressions through Verilog.

You will design and submit as a zip file, your report including:

1. State diagram
2. State table
3. Boolean expressions
4. Verilog implementation
5. Simulation results

In this assignment, you will design a vending machine that can take 1TL and 0.5TL and it can supply either water (2.5TL) or sandwich (5TL).

The machine can give 0.5TL cash back to the customer. Assume the customer does not necessarily give any cash. For instance, if he wants water and has given 3TL, he will not give any more 0.5 or 1 TL.

- There are two sensors S1 and S2:

  S1 detects if a cash is given to the machine:

  0: No entry

  1: Cache entered

  S2 detects the cache type:

  0: 0.5TL

  1: 1TL

- There are three motor controllers M1, M2 and M3:

  M1 gives the water if it is made 1 for one cycle.

  M2 gives sandwich if it is made 1 for one cycle.

  M3 gives the 0.5TL back to the user if it is made 1 for one cycle.

You cannot use behavioral Verilog. You will use always@ only for state register definition.