TERM PROJECT

DİGİTAL DESİGN 2

INF606

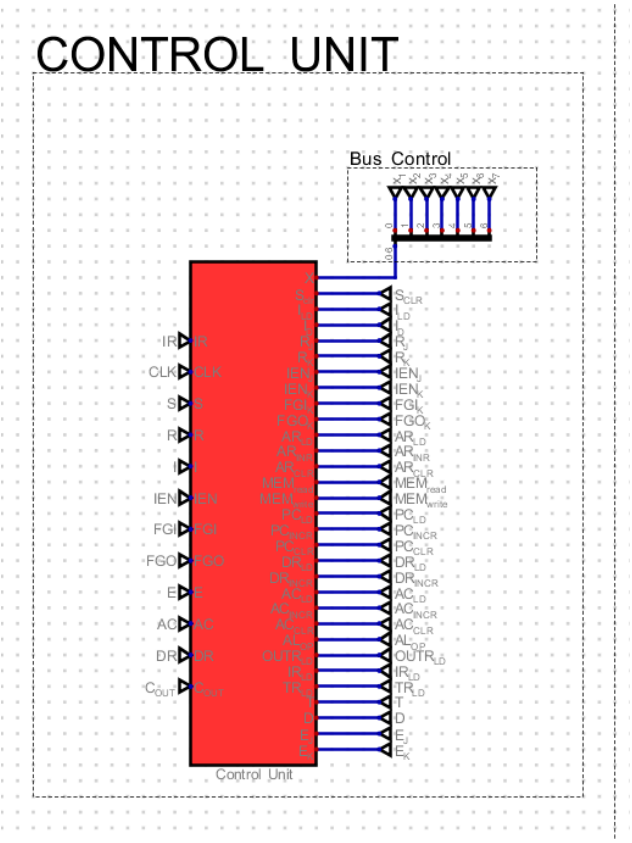
Oğuzhan Topal - 190503001

Summary:

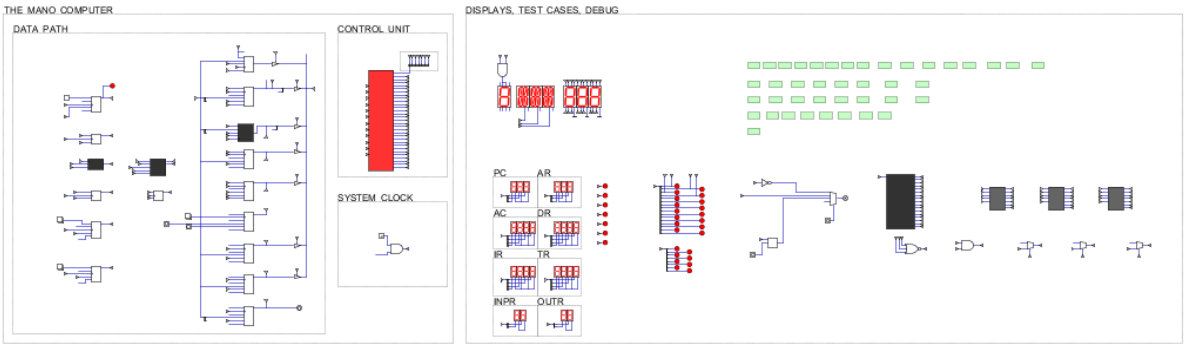
In this project I made the simulation Control Unit of Mano Computer in Digital simulation tool. While making the Control Unit, I followed descriptions in the Computer System Architecture book written by M. Morris Mano (especially chapter 5).

Design Assumptions:

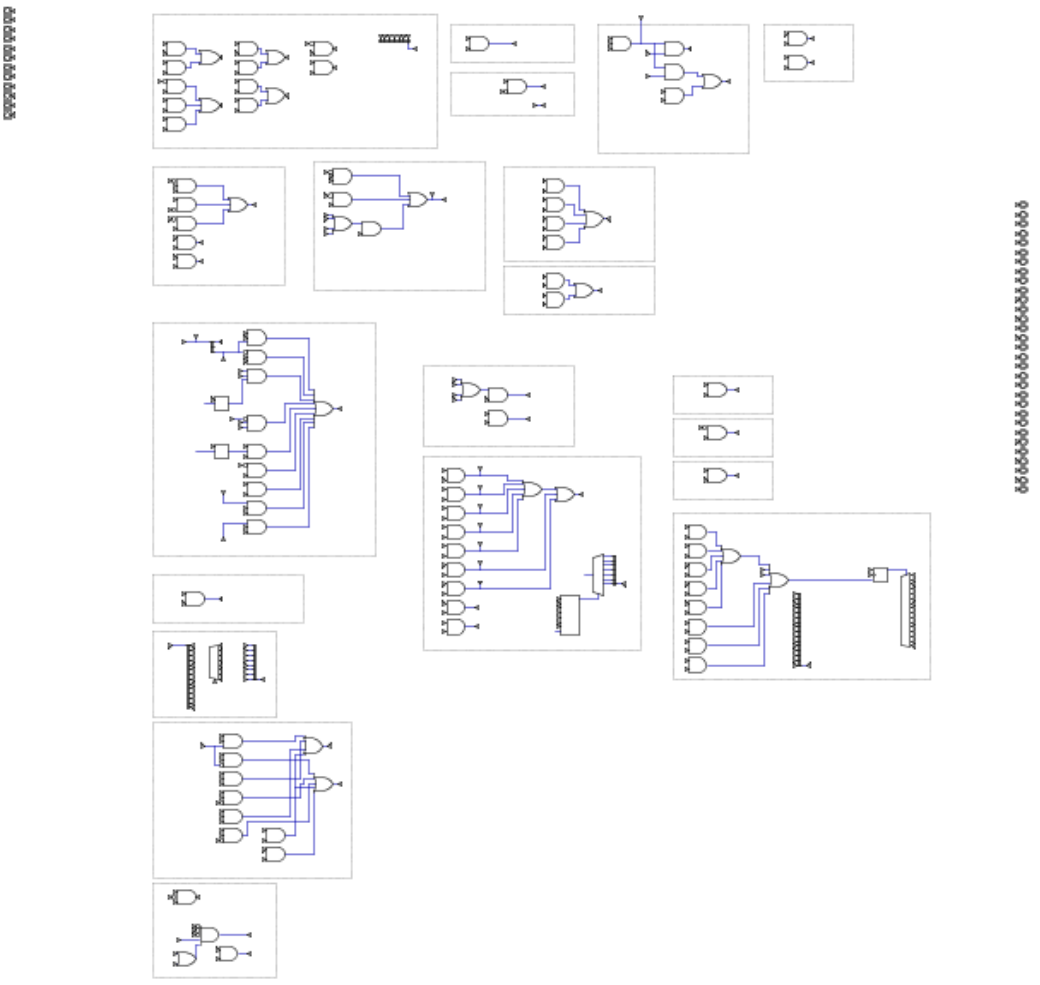
Control Unıt takes 19 inputs from datapath and gives 31 control signals to datapath and display-test area. The sequence clocks is inside of Control Unit, It choose Arithmetic-Logic Units operations, it controls bus system and all the registers.It also needs to fulfill tests given by lecturer.



Control Unit



Full Picture



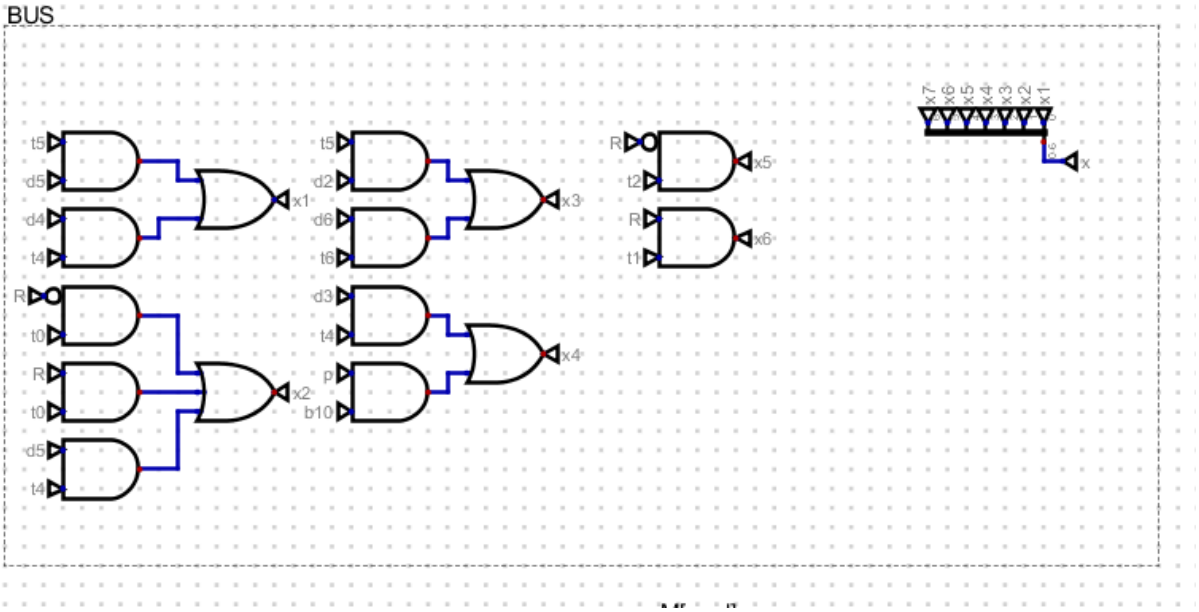
İnside Control Unit

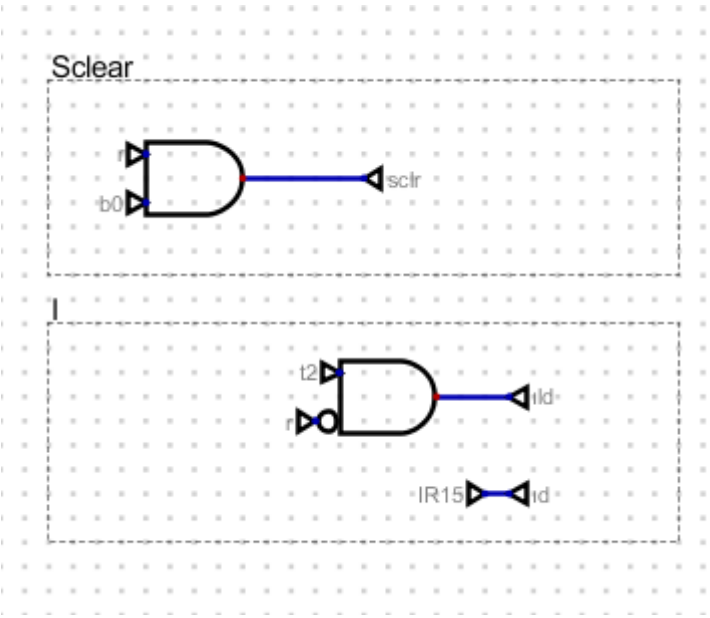
Design Approach:

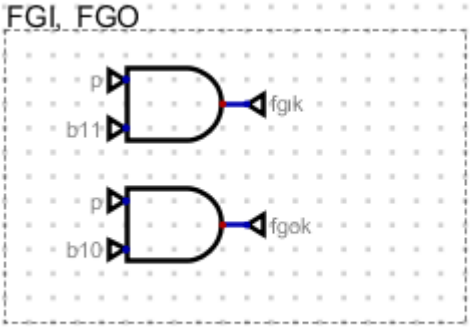
I mainly used table 5.6 in the Computer Systems Architecture book. Based on the functions given in the table I created the Circuits and connected them related İnputs and Outputs. The following pictures are Table 5.6 in the book and circuits inside the Control Unit.

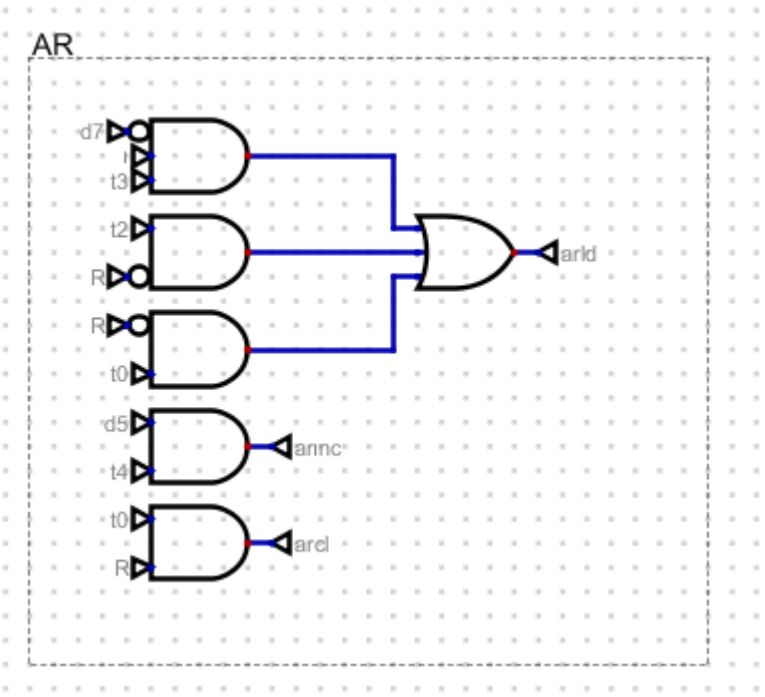
TABLE 5-6 Control Functions and Microoperations for the Basic Computer

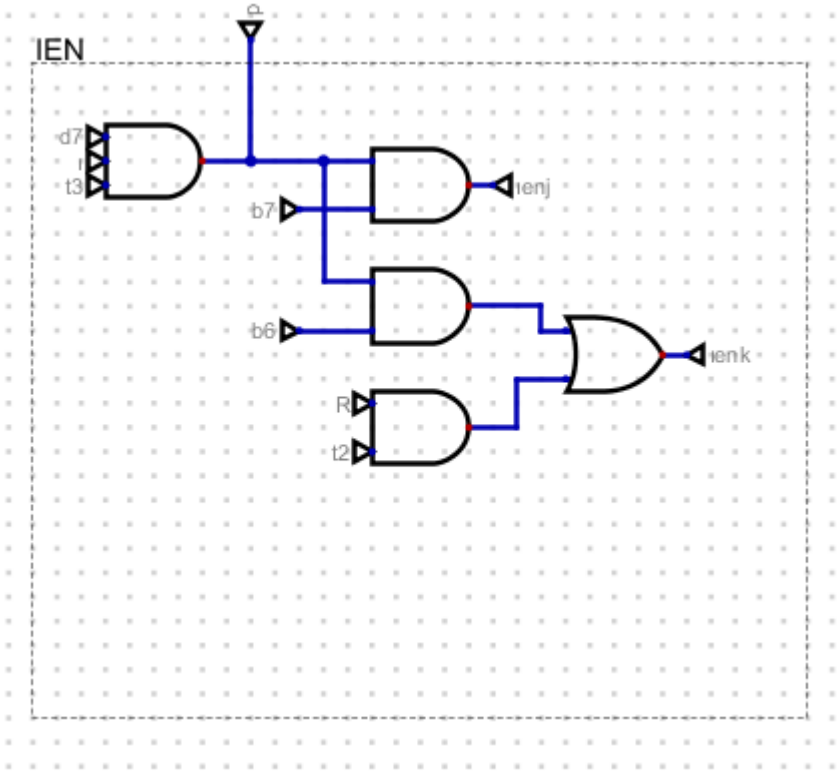
Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	$D_7'IT_3$:	$AR \leftarrow M[AR]$
Interrupt:		
	$T_0'T_1'T_2'(IEN)(FGI + FGO)$:	$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
		$D_7I'T_3 = r$ (common to all register-reference instructions)
		$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1)$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
		$D_7IT_3 = p$ (common to all input–output instructions)
		$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$

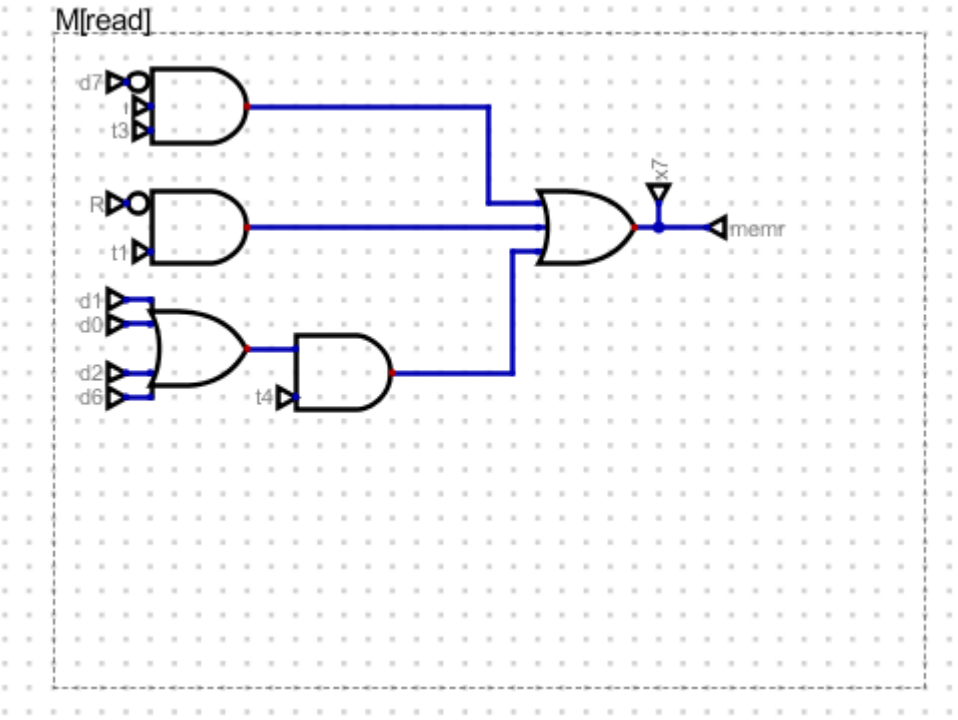

BUS
t5
d5
d4
t4
x1
t5
d2
d6
t6
x3
R
t2
R
t1
x5
x6
x7
x6
x5
x4
x3
x2
x1
x
R
t0
R
t0
d5
t4
x2
d3
t4
p
b10
x4

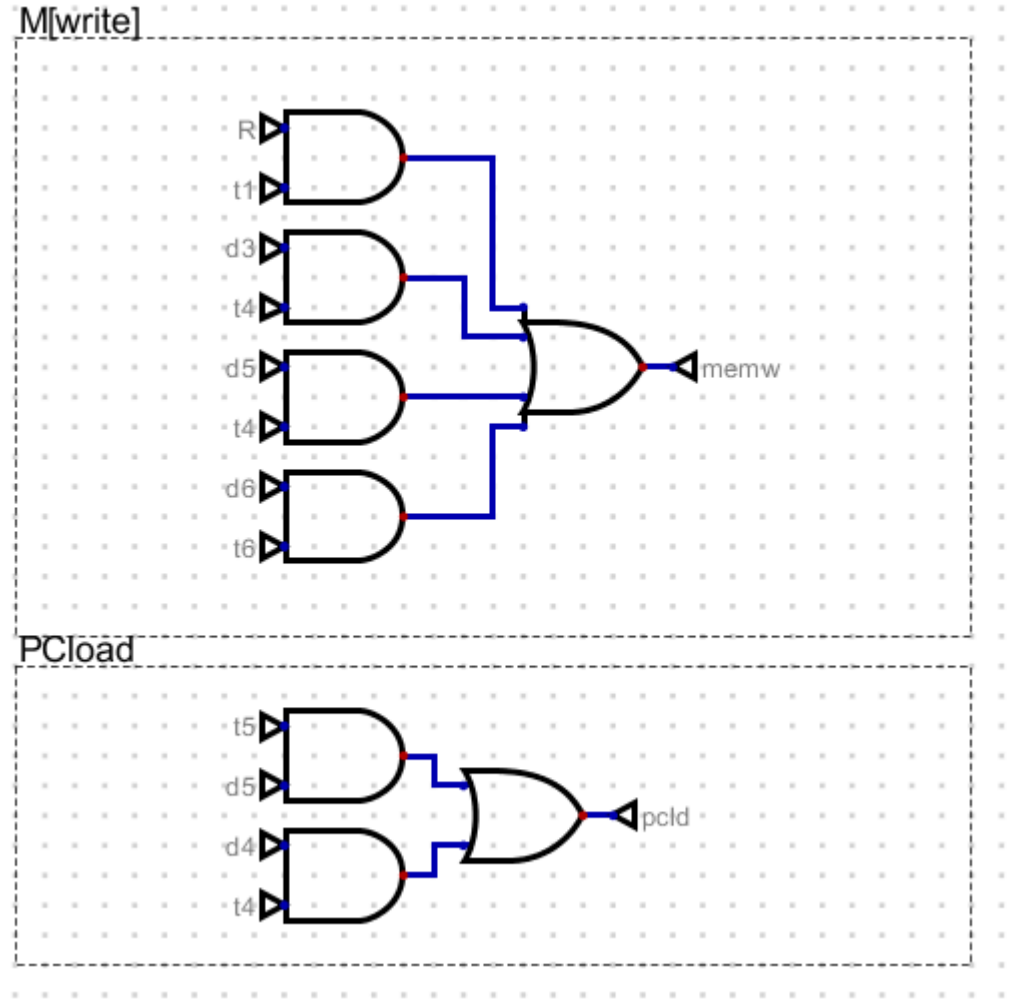

Sclear
r
b0
sclr
I
t2
r
ild
IR15
id

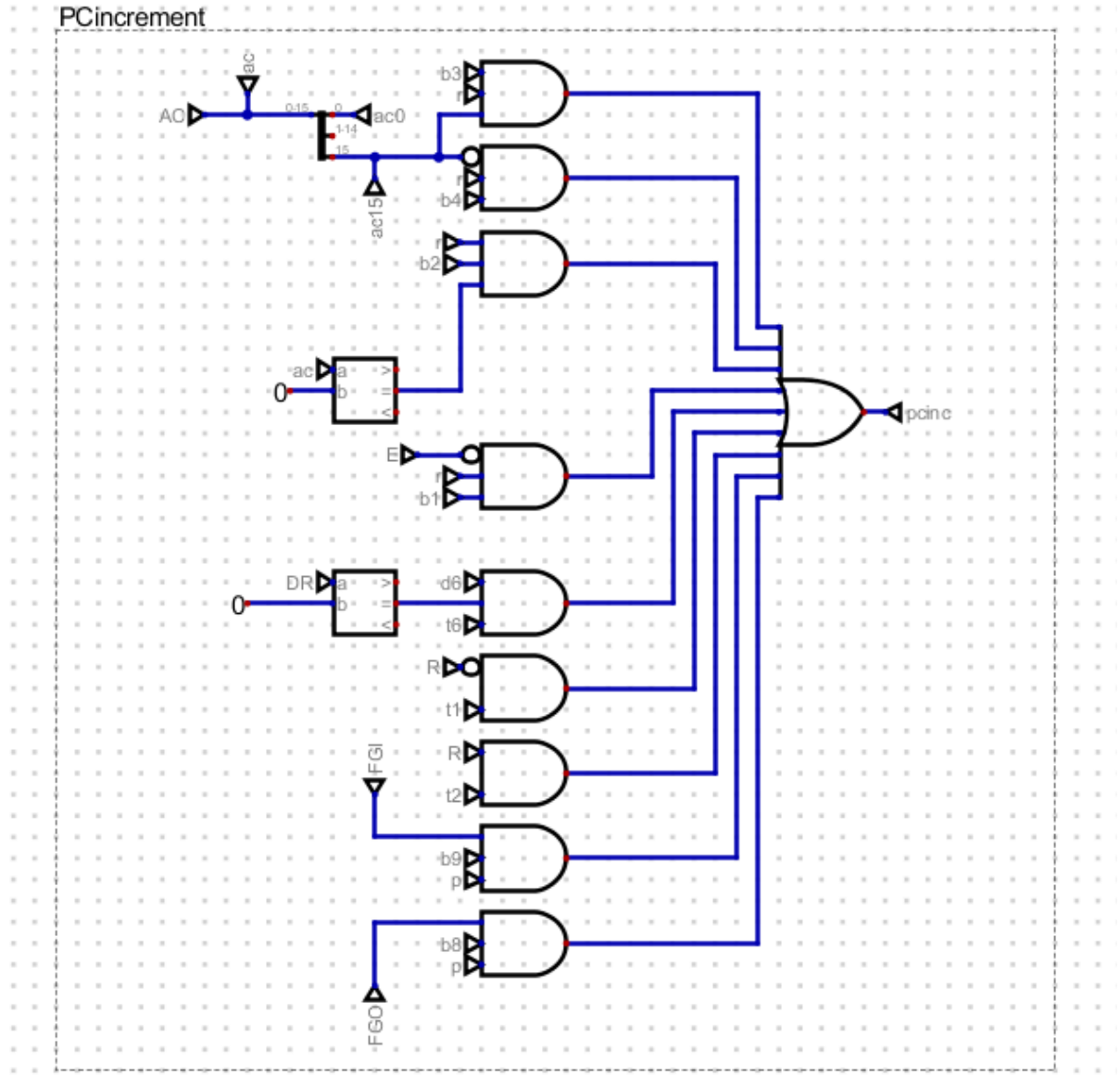

FGI, FGO
p
b11
fgik
p
b10
fgok

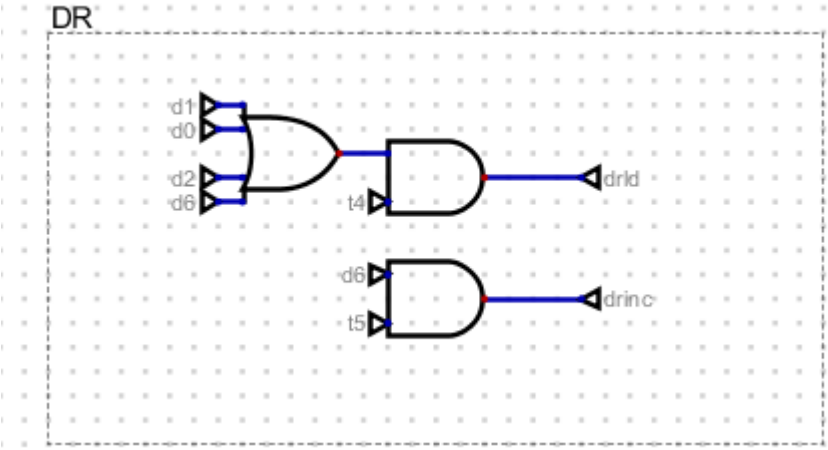

AR
d7
I
t3
t2
R
R
t0
d5
t4
t0
R
arld
annc
arcl

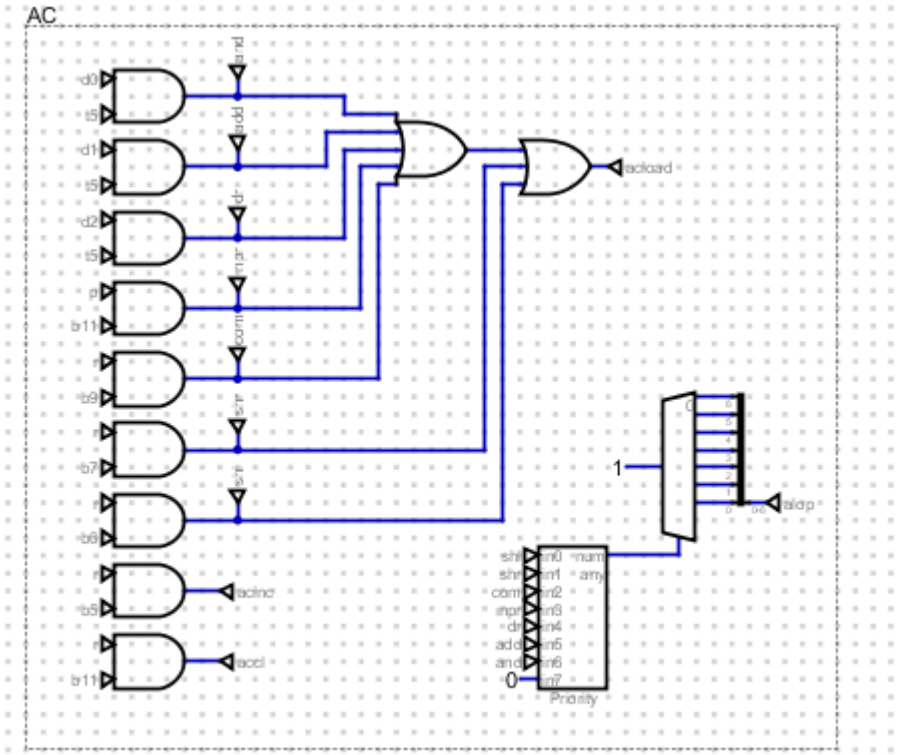

IEN
p
d7
I
t3
b7
b6
R
t2
ienj
ienk

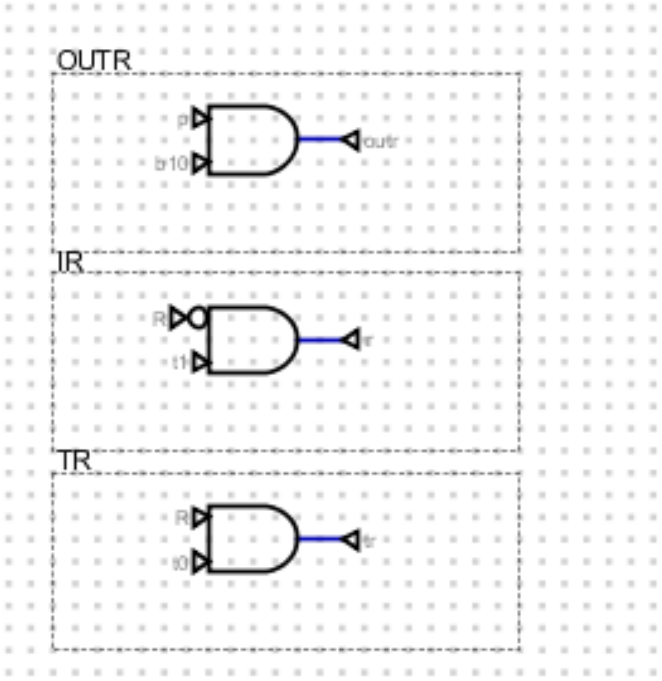

M[read]
d7
t3
R
t1
d1
d0
d2
d6
t4
x7
memr

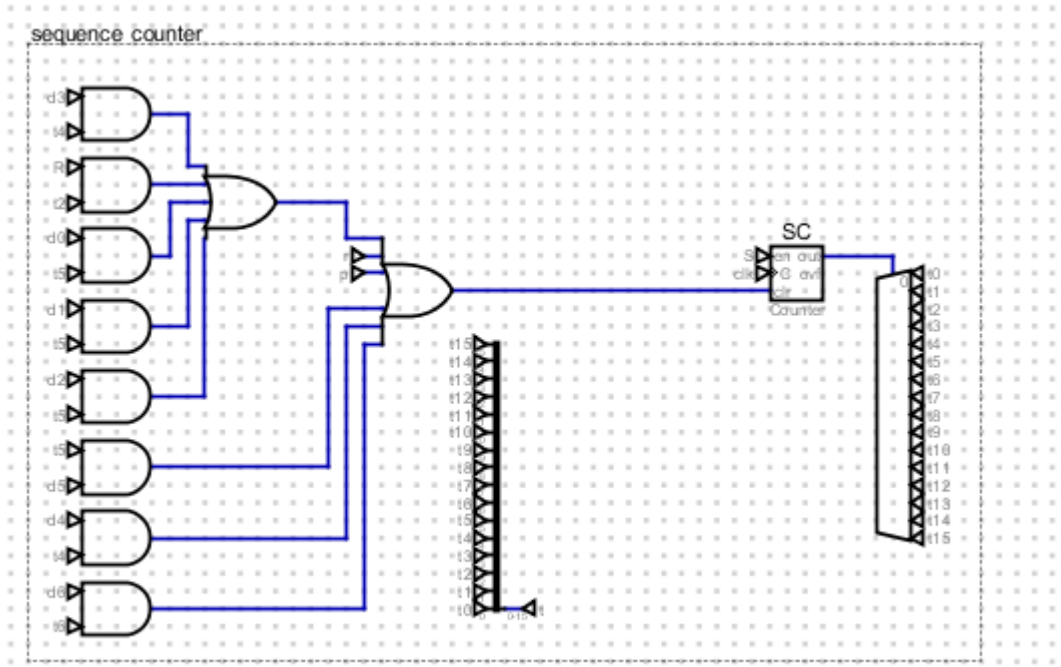

M[write]
R
t1
d3
t4
d5
t4
d6
t6
memw
PCload
t5
d5
d4
t4
pcld

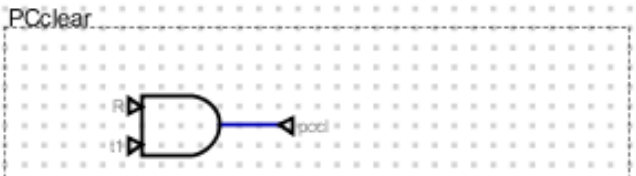

PCincrement
ac
AC
0-15
0
ac0
1-14
15
ac15
b3
r
r
b4
r
b2
ac
a
0
b
>
=
<
pcinc
E
r
b1
DR
a
0
b
d6
t6
R
t1
R
t2
FGI
b9
p
b8
p
FGO

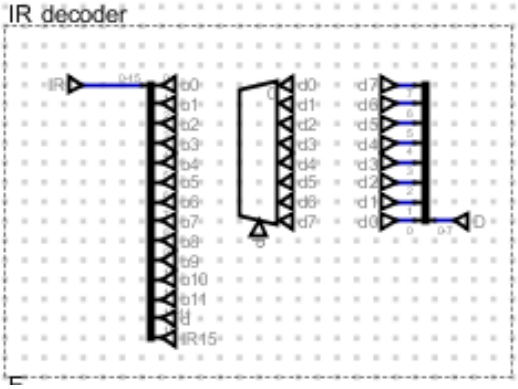

DR
d1
d0
d2
d6
t4
drld
d6
t5
drinc

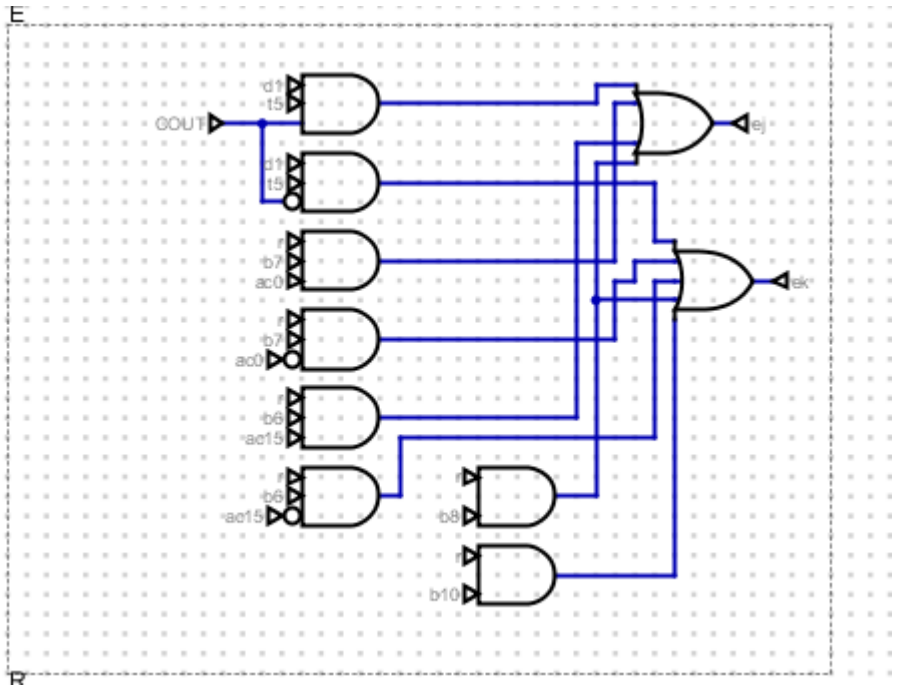

AC
d0
t5
d1
t5
d2
t5
p
b11
r
b9
r
b7
r
b6
r
b5
r
b11
and
add
dr
inpr
com
shr
shl
acload
aczero
accl
1
0
n0
n1
n2
n3
n4
n5
n6
n7
num
any
Priority

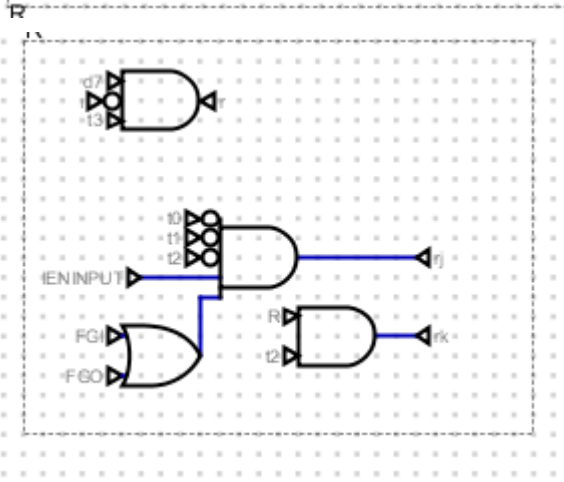

OUTR
p
b10
outr
IR
R
t1
ir
TR
R
t0
tr

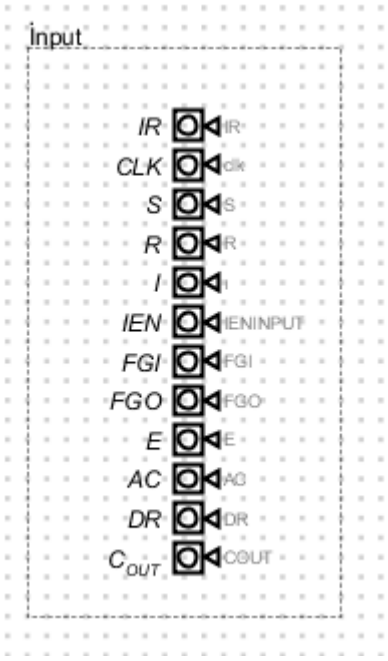

sequence counter
SC
Counter

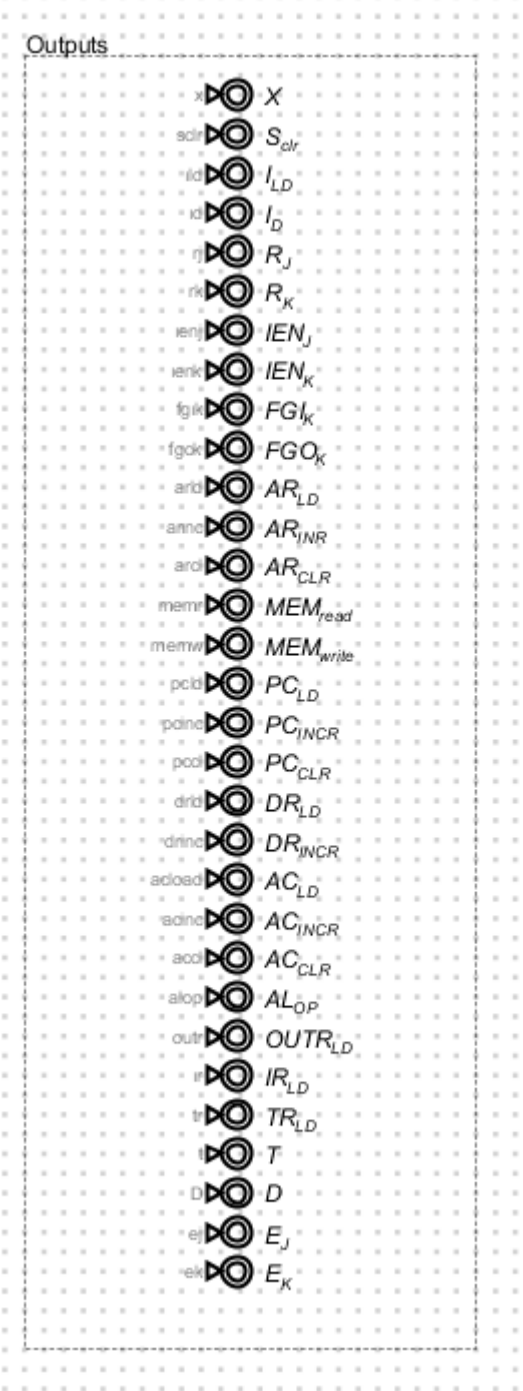

PCclear
R
t1
pccl


IR decoder
IR15


E
d1
t5
COUT
ej
d1
t5
r
b7
ac0
ek
r
b7
ac0
r
b6
ac15
r
b6
ac15
r
b8
r
b10

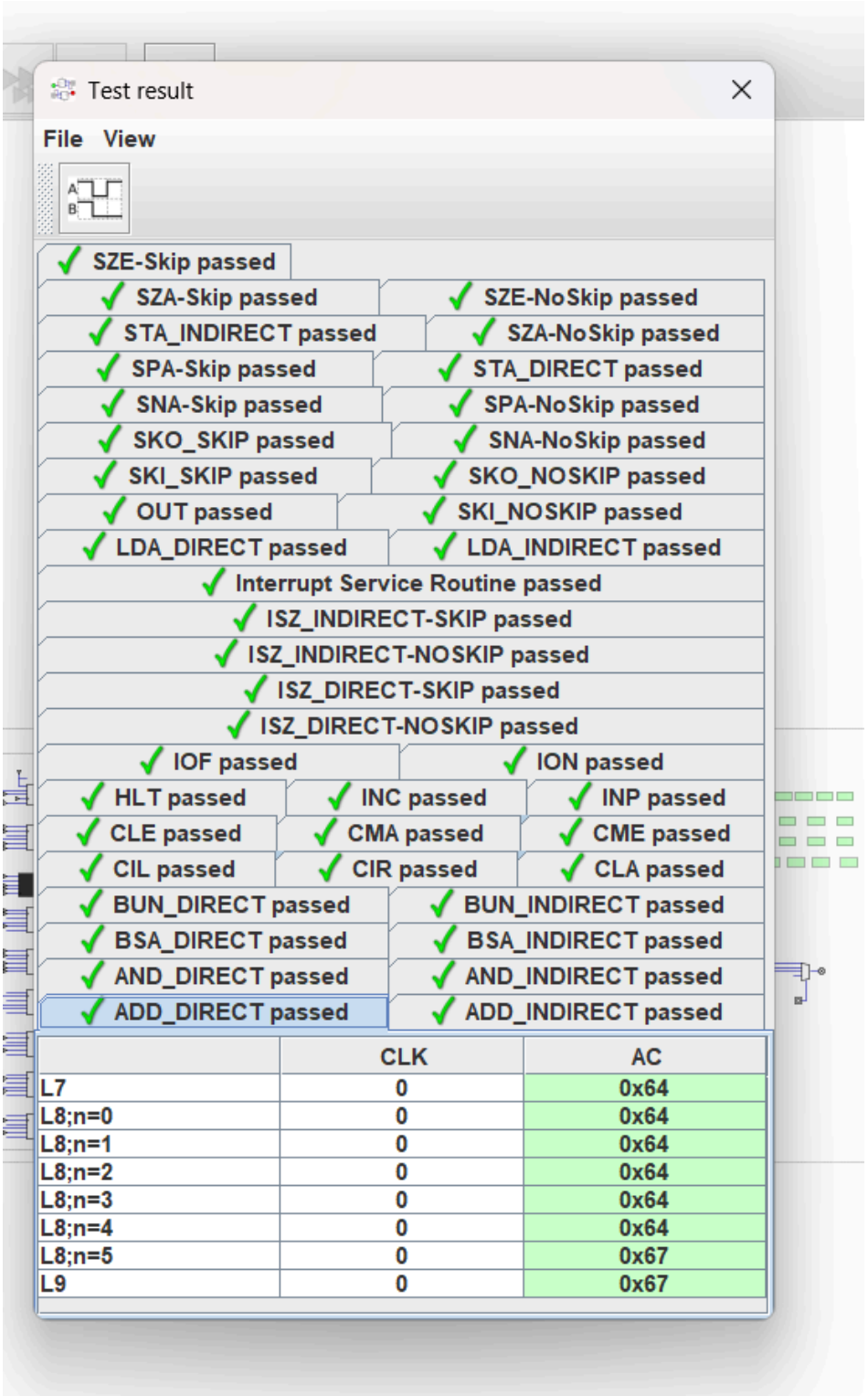

R
d7
r
t3
ri
t0
t1
t2
IENINPUT
rj
FGI
FGO
R
t2
rk


İnput
IR
CLK
S
R
I
IEN
FGI
FGO
E
AC
DR
C_{OUT}
IR
clk
S
R
I
IENINPUT
FGI
FGO
E
AC
DR
COUT


Outputs
x
X
sclr
S_{clr}
ild
I_{LD}
id
I_D
rj
R_J
rk
R_K
ienj
IEN_J
ienk
IEN_K
fgik
FGI_K
fgok
FGO_K
arld
AR_{LD}
arinc
AR_{INR}
arcl
AR_{CLR}
memr
MEM_{read}
memw
MEM_{write}
pcld
PC_{LD}
pcinc
PC_{INCR}
pccl
PC_{CLR}
drld
DR_{LD}
drinc
DR_{INCR}
acload
AC_{LD}
acinc
AC_{INCR}
accl
AC_{CLR}
alop
AL_{OP}
outr
$OUTR_{LD}$
irl
IR_{LD}
trl
TR_{LD}
t
T
D
D
ej
E_J
ek
E_K

Test Cases:

The Control Unit passed all the tests given by lecturer.



	CLK	AC
L7	0	0x64
L8;n=0	0	0x64
L8;n=1	0	0x64
L8;n=2	0	0x64
L8;n=3	0	0x64
L8;n=4	0	0x64
L8;n=5	0	0x67
L9	0	0x67