BOX PLACING DEVICE USING ZYBO

by

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Engineering Project Report

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BOX PLACING DEVICE

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ABSTRACT

BOX PLACING DEVICE USING ZYBO

Autonomous systems are developed to decrease human work. Engineers aim at increasing capabilities of people with disabilities by using robotic technology. In this field, one of the issues considered is to create cheap and useful system for people who need a wheelchair. For This reason, I decided to produce autonomous robot arm to show that it is effective and portable for companies.

The aim of the project is to create Zynq All Programmable System on Chip system to object placing which was based on colour detection and image thresholding. For this reason, green colour was detected to find position of the object by using the real time images obtained by the camera. After detecting location of the object, object grapped by robot arm and it release the point which was defined.

ÖZET

Günümüzde hızla gelişen ve adını endüstri 4.0 olarak alan teknolojik gelişmeler elektronik mühendisliği alanında büyük bir ivme kazandırıyor. Endüstriyel tarım, depolama ve kargolama sistemleri hızlı bir şekilde otomasyona dönüşüm geçiriyor. Bu alanda yapılan önemli çalışmalardan biri de otomatik olarak çalışan stabil akıllı cihazlar üretmek. Bu doğrultuda; günümüz teknolojik gelişimiyle adapte, otomatik çalışan istenilen, objeyi konumundan farklı bir noktaya taşıyan bir sistem tasarlamak istedim.

Projede görüntü üzerinden istenilen objenin konumunu belirleyen sonrasında robot kol ile objeyi yerinden istenilen noktaya bırakan bir sistem kurdum. Bunun için Zybo'nun bir kamera yardımıyla görüntü almasını sağladım. Görüntüyü işleyerek objenin konumunu belirleyen Zybo, Bluetooth haberleşmesi ile robot kol işlemcisine gitmesi gereken konuma yönlendirmesini ve robotun objeyi almasını ve istenilen konuma bırakmasını sağladı.

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LIST OF SYMBOLS / ABBREVIATIONS

AP	All Programmable
SoC	System on Chip
FPGA	Field Programmable Gate Array
AXI	Advanced eXtensible Interface
DDR	Double Data Rate
RGB	Red Green Blue
VGA	Video Graphics Array
A	Ampere
VCC	+3.3V
GND	0V
S2MM	Stream to Memory Mapping
MM2S	Memory Mapping to Stream
VDMA	Video Direct Memory Access
SDK	Software Development Kit

1. INTRODUCTION

Many kinds of developments in technology have been changing the comfort and convenience of our life. Developments in technology led to have faster and reliable chips and more featured tools that increase the productivity. We use all of these advancements to create intelligent systems that help people in daily life. These advancements are used for not only daily life of people but also making manufacturing processes faster and reliable. Universities, companies and entrepreneurs agree on these solutions. Therefore, they search for solutions that will make life easier and increase productivity. For instance, hearing and visually impaired people take advantage of applications and robots that were produced by giant companies in the field of information technology and robotics. In order to develop new manufacturing platforms companies, create new hardware solutions that can be configured according to needs.

In my project, my goal is to remote control a robotic arm via using video processing algorithms on a SoC system. By sorting the colour of the objects on SoC, robotic arm is commanded to change the position of the object. This kind of system can be used to sort packages in a large warehouse. Xilinx Zynq is a powerful SoC platform that enables designers to implement video processing algorithms on Arm hard processor and FPGA. Power of parallel processing of FPGA and power of software on Arm are combined on this system. Moreover, Xilinx Zynq platform has a large community that can be communicated to request help. These advantages led me to choose this platform. I picked up Zybo board which is the product of Digilent.

Firstly, the hardware that I used to implement this project will be explained. Secondly, system design will be explained. Finally, conclusion will be stated.

2.Equipments and Environments

2.1 OV7670 Cmos Camera

Ov7670 is cheap, useful a camera sensor. It uses many test, hobby projects. It has YUS/YCbCr 4:2:2, BGR4:2:2, RGB5:5:5, RGB4:4:4 and RGB5:6:6 out colour formats and It work 50MHz clock frequency. It has 14 pins which are Vcc, GND, siod, sioc, xclk, pclk, reset, vsync, href,8 data pin, pwdn. It can produce VGA 640x480 resolution in 30 frame per second. Using i2c communication, it can be reduced. It uses Serial Control Camera Bus (SCCB) protocol (similar i2c communication).

Figure 1. OV7670

Active Array Size		640 x 480
Power Supply	Digital Core	1.8VDC ±10%
	Analog	2.45V to 3.0V
	I/O	1.7V to 3.0V[a]
Power Requirements	Active	60 mW typical (15fps VGA YUV format)
	Standby	< 20 µA
Temperature Range	Operation	-30°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB565/555/444 • GRB 4:2:2 • Raw RGB Data
Lens Size		1/6"
Chief Ray Angle		25°
Maximum Image Transfer Rate		30 fps for VGA
Sensitivity		1.3 V/(Lux • sec)
S/N Ratio		46 dB
Dynamic Range		52 dB
Scan Mode		Progressive
Electronics Exposure		Up to 510:1 (for selected fps)
Pixel Size		3.6 µm x 3.6 µm
Dark Current		12 mV/s at 60°C
Well Capacity		17 K e
Image Area		2.36 mm x 1.76 mm
Package Dimensions		3785 µm x 4235 µm

a. I/O power should be 2.45V or higher when using the internal regulator for Core (1.8V); otherwise, it is necessary to provide an external 1.8V for the Core power supply.

Figure 2. Properties of OV7670

Figure 3. Pins of OV7670

2.2 VGA out and Monitor

VGA is an analogue image standard. VGA can only send image data. It cannot send audio data. HDMI can both. VGA has 3 data pin which are red, green, blue and 2 synchronization pin

which are horizontal sync and vertical sync. Synchronization pins scale the image on frame and data pins create the frame.

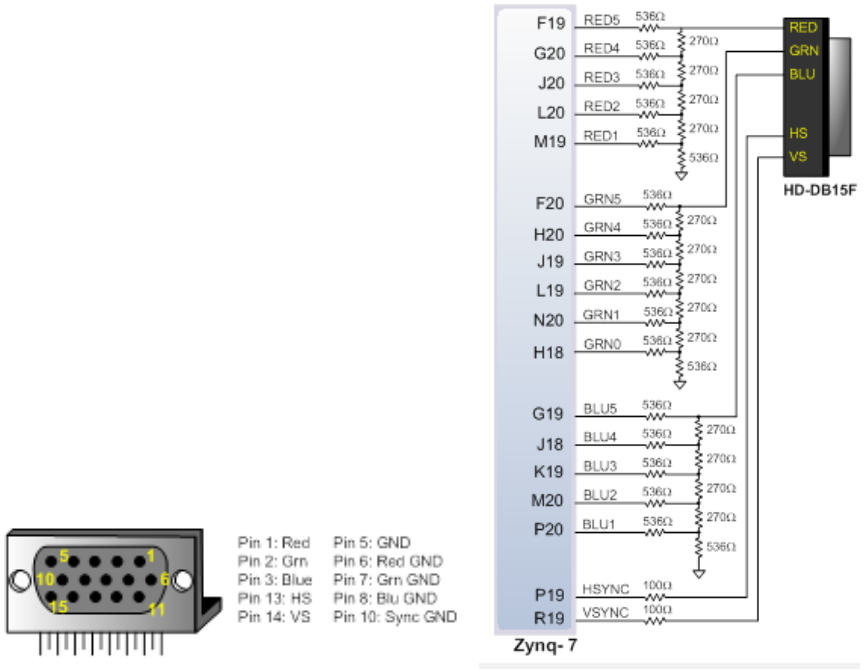

Figure 4. Connector pins and SoC Bank connection of OV7670

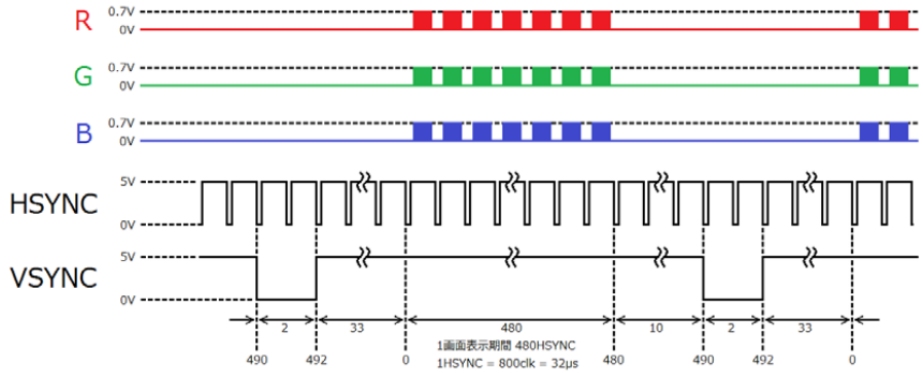

Figure 5. Video Timing of OV7670

2.3 HC06 Bluetooth Module

HC06 Bluetooth serial module convert serial port to Bluetooth communication. The module supports Bluetooth 2.0 and use 2.4 GHz ISM band. Range of module is 10 meters, if there is no engel. It can transmit data point to point (PTP) network technology using low energy. It works 3.3V-6V and voltage level is 3.3V. It has four basic pins which are Vcc, Ground (GND), transmit data (TxD) and receive data (RxD). It can use UART communication protocol. To configurate the module, it has AT commands. Using AT commands, baud rate, device id, device password, pairing another device can configure.

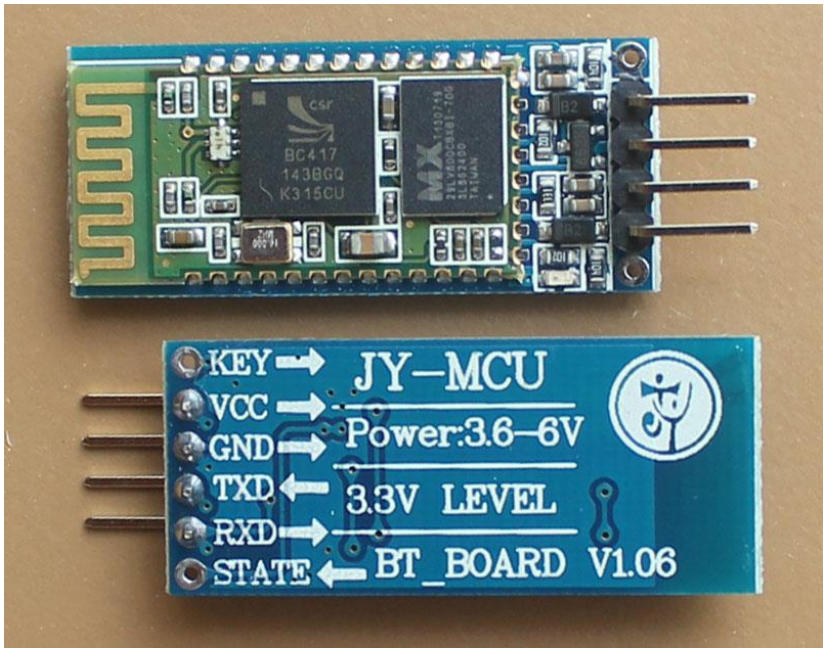

Figure 6. HC06 Bluetooth Module

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2.4 ZYBO FPGA Board

The Zybo (Zynq™ Board) is a feature-rich, ready-to-use, entry-level embedded software and digital circuit development platform built around the smallest member of the Xilinx Zynq-7000 family. The board produced by DIGILENT. It has ARM Cortex A9 dual core processor and Xilinx Artix 7 Field Programmable Gate Array (FPGA). When coupled with the rich multimedia and connectivity peripherals available in Zybo. Zynq-7010 can host whole system design. Zybo has on-board memories, video and audio I/O, dual role USB, Ethernet, SD slot and 6 Pmod ports etc.

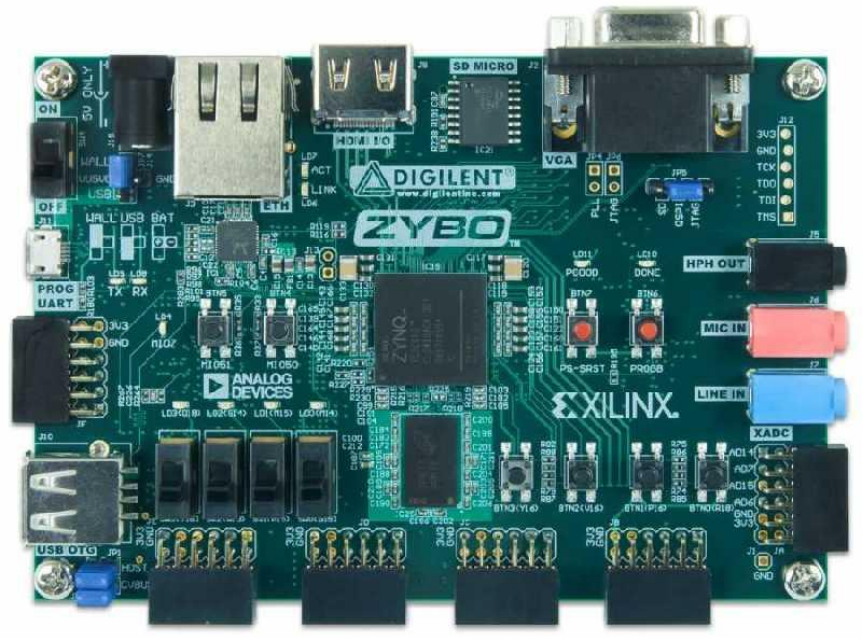

Figure 7. Zybo Demo Board

2.4.2 Zynq-7000 All Programable SoC Architecture

Zynq products integrate an ARM® Cortex™-A9 based processing system (PS) and Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 CPUs are the centre of the PS and include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. Zynq family provide flexibility on FPGA. Zynq devices has PS and PL. Use processor and FPGA features both. Zynq has wide range of applications.

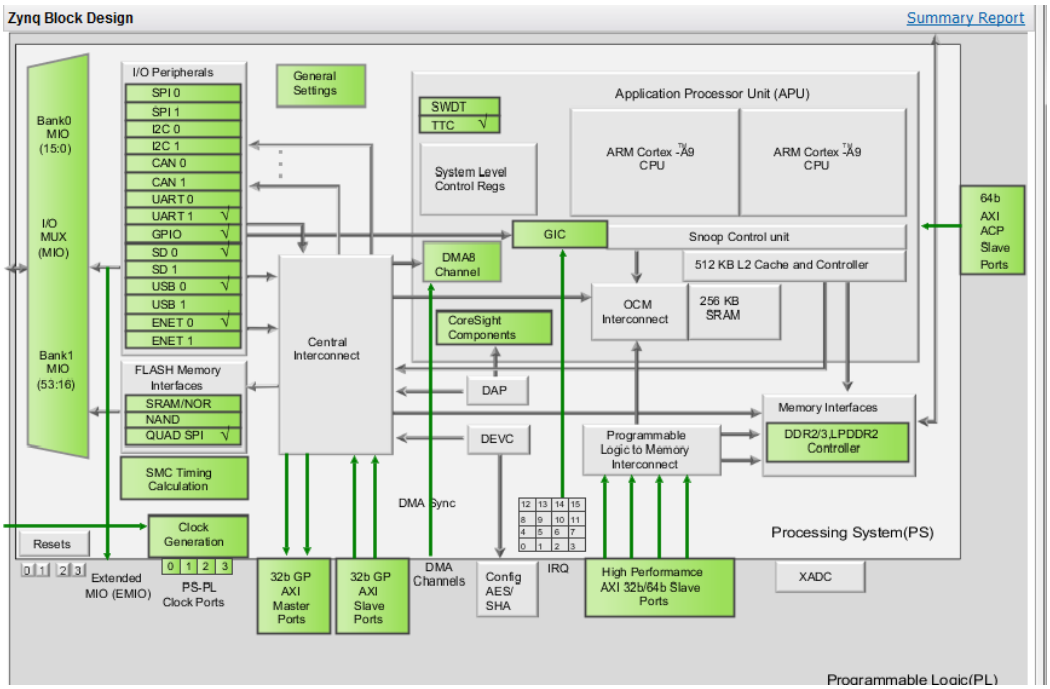

Figure 8. Zynq Block Design

2.5 Robot Arm

Robot Arm produced by Nurettin Can Özbakır for his engineering project. It works like a human arm. Robot Arm can move on 3 dimensions and it has a gripper to grip objects. 5 dc motor rotate 5 joints which are base, shoulder, elbow, wrist, gripper. Robot Arm has MSP430G2553 microcontroller. The microcontroller receives 5 different data using HC05 Bluetooth module and every input data rotates its different joints.

2.6 Vivado Design Suite

Vivado Design Suite is an environment to design Xilinx FPGAs. It can simulate designs, run synthesis, run implement and generate bitstream. Verilog or VHDL hardware description languages use to design FPGAs on Vivado. Vivado 2016.4 used in the project. If one uses older or newer version, he or she should check versions of Vivado IPs.

2.6.1 AXI Protocol

AXI protocol produced by ARM specification. It provides design whole system around the PS. It provides flexibility, productivity, availability. It provides a standard for developers to understand designs.

There are three types of AXI4 interfaces:

- AXI4-for high performance memory-mapped requirements.
- AXI4-Lite-for simple, low-throughput memory-mapped communication
- AXI4-Stream- for high speed streaming data.

There are five different channels is both AXI4 and AXI4-Lite protocols:

- Read Address Channel
- Write Address Channel
- Read Data Channel
- Write Data Channel
- Write Response Channel

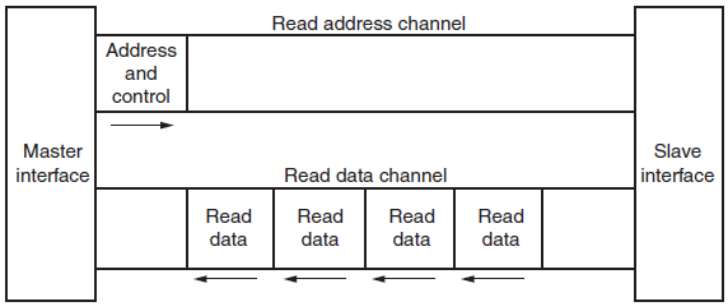

Figure 9. Read Data Transaction

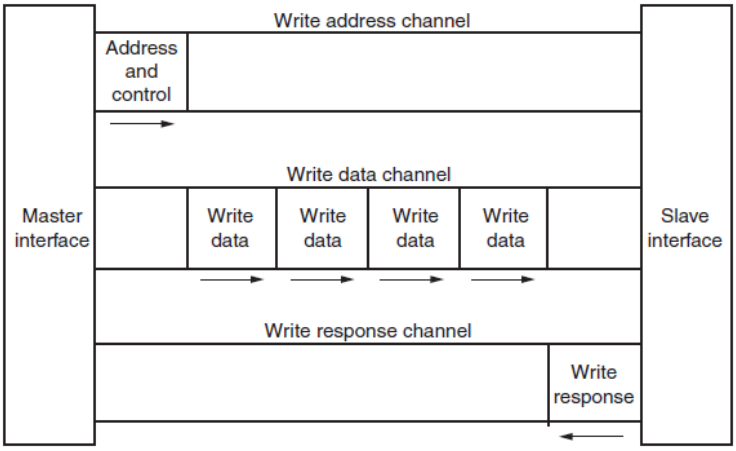

Figure 10.Write Data Transaction

The AXI4-Stream protocol is used for the applications that typically focus on a data-centric and data-flow paradigm where the concept of an address is not present or not required. Each AXI4-Stream acts as a single unidirectional channel for a handshake data flow.

2.7 Vivado Software Development Kit

Vivado SDK provides embed and run C or C++ codes. When PL design completed and launched SDK, it initializes PL design and ready to develop ARM Cortex A9. Vivado SDK provide run on debug mode and can read RAM data's real time. It can access registers. Compile codes.

3. SYSTEM DESIGN

There are one input which is ov7670 camera and two different outputs which are Robot Arm and VGA monitor in the system design. Real-time image of the camera is written to DDR3 memory. Firstly, Image written to DDR3 is read to feed VGA module to view the input on display. Secondly, the date processed on PS is sent to HC06 Bluetooth module via UART protocol. HC06 transmits UART bytes to robot Arm. For robot arm part, robot arm system prepared by Nurettin Can ÖZBAKIR is used. Nothing modified or edited on the robot arm.

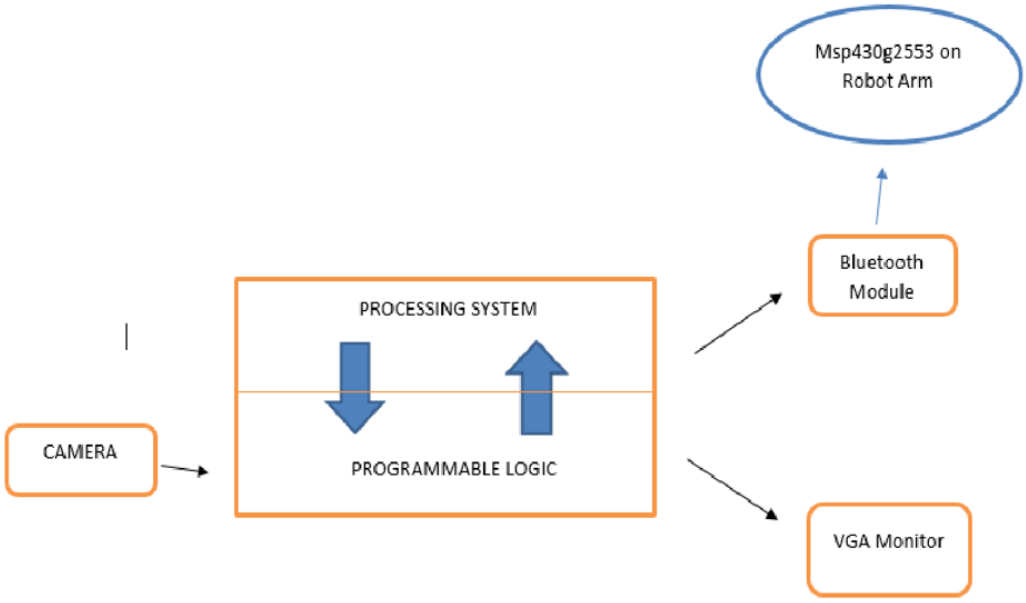

Figure 11.System Overview

3.2 PL Design

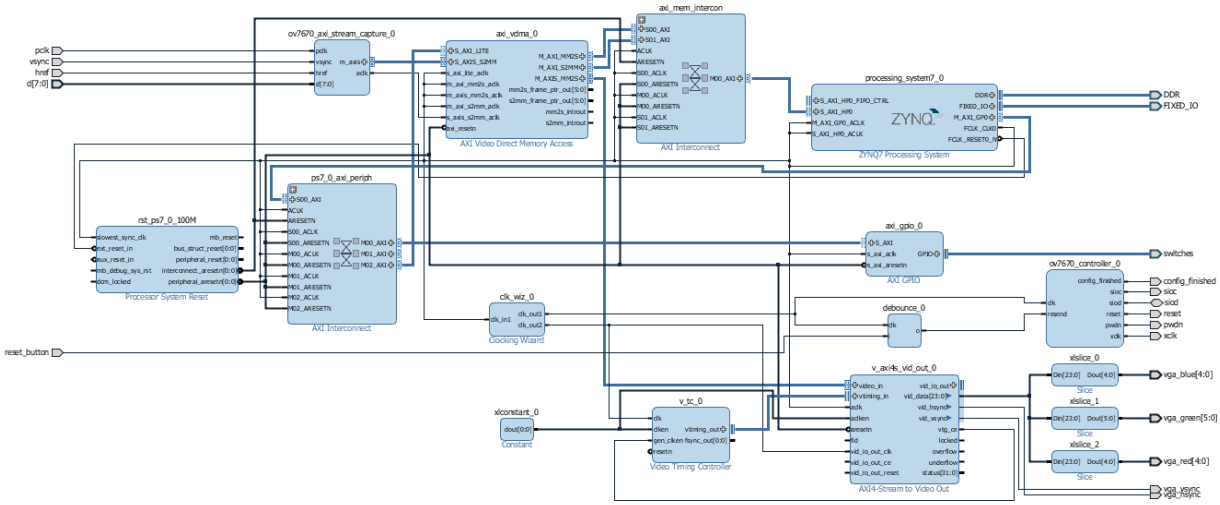

Figure 12. RTL Schematic

3.2.1 OV7670 CAMERA design

The camera configured to generate 640x480 resolution at 50MHz RGB565 colour format. ov7670_controller and ov7670_axi_stream_capture blocks provide this configuration. Ov7670_controller provides I2C protocol and it works on 50 MHz, so controller block is connected clk_out1 pin of clock wizard. Camera capture block created on AXI protocol. The Capture block writes (S2MM) rgb565 data on DDR3 memory at 30 frame per second. The camera works 3.3V provided by Zybo PMOD. Also, debounce block is used for camera stabilization. Camera is affected by change of voltage and to regulate this change a button is added to reset camera initialization. VHDL codes of blocks are in Appendix.

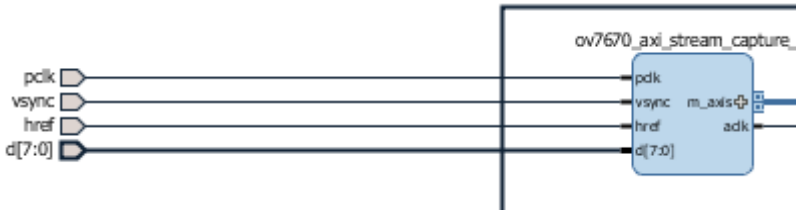

Figure 13. OV7670 AXI Interface

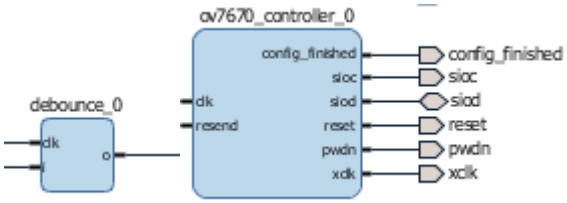

Figure 14.OV7670 Debounce Filter and Register Setting Block

3.2.3 DDR3 Memory

DDR3 Memory has the data address span from 0x1000_0000 to 0x0004_B000. It can has 512MB data, but 614400 bytes (640x480x16 bit) enough for this system. Every frame overwrites the addresses. AXI Video Direct Memory Access IP is used to access DDR3 to read and write video frames.

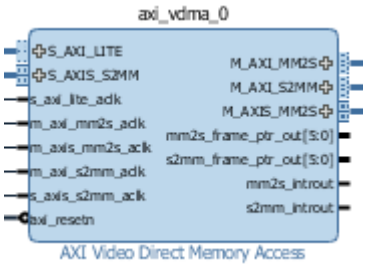

Figure 15. VDMA IP

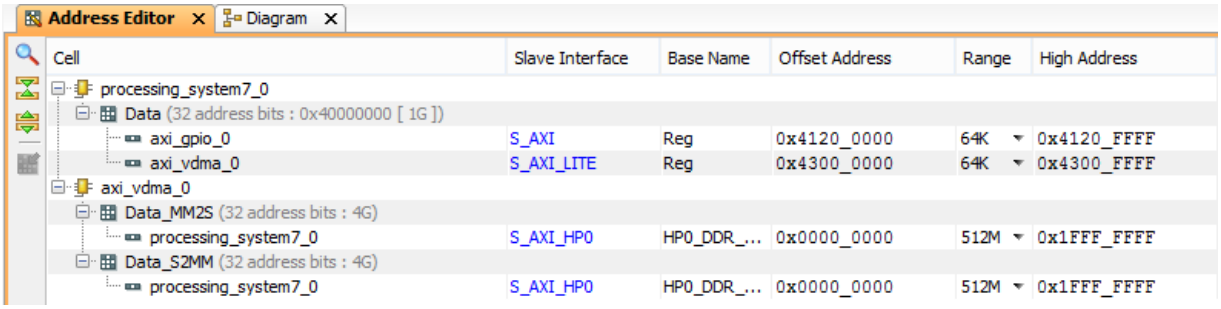

Figure 16. Configuration of VDMA

3.2.3 VGA design

To show frame on monitor, Video Timing Controller and AXI4-to Stream to Video out IP cores are used. Video Timing Controller block provides 640x480 resolution. Configuration of block showed on diagram. Video Out block reads (MM2S) 24 bits data from DDR3 addresses. RGB data stores less significant 16 bits, therefore slice blocks cut pieces of RGB and data transmits VGA port. VGA block operates at 25MHz, therefore clk_out2 pin of clock wizard module is connected to Video Timing Controller and Video Out block. Customization of blocks showed on the figure.

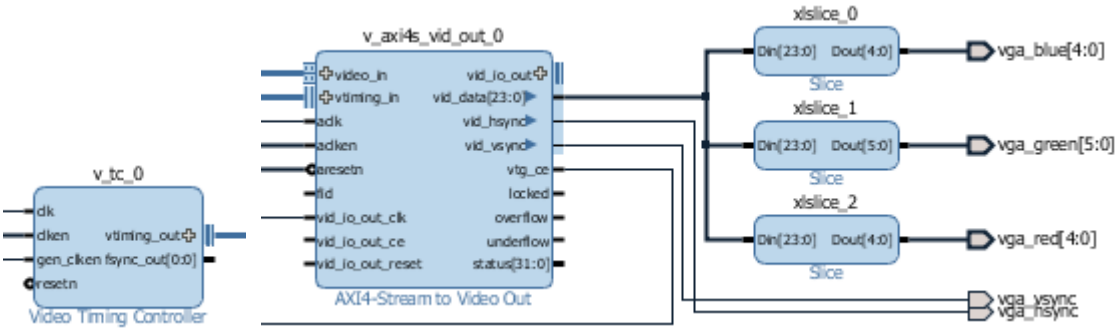

Figure 17. Video Timing Controller and AXI-Stream to Video OUT

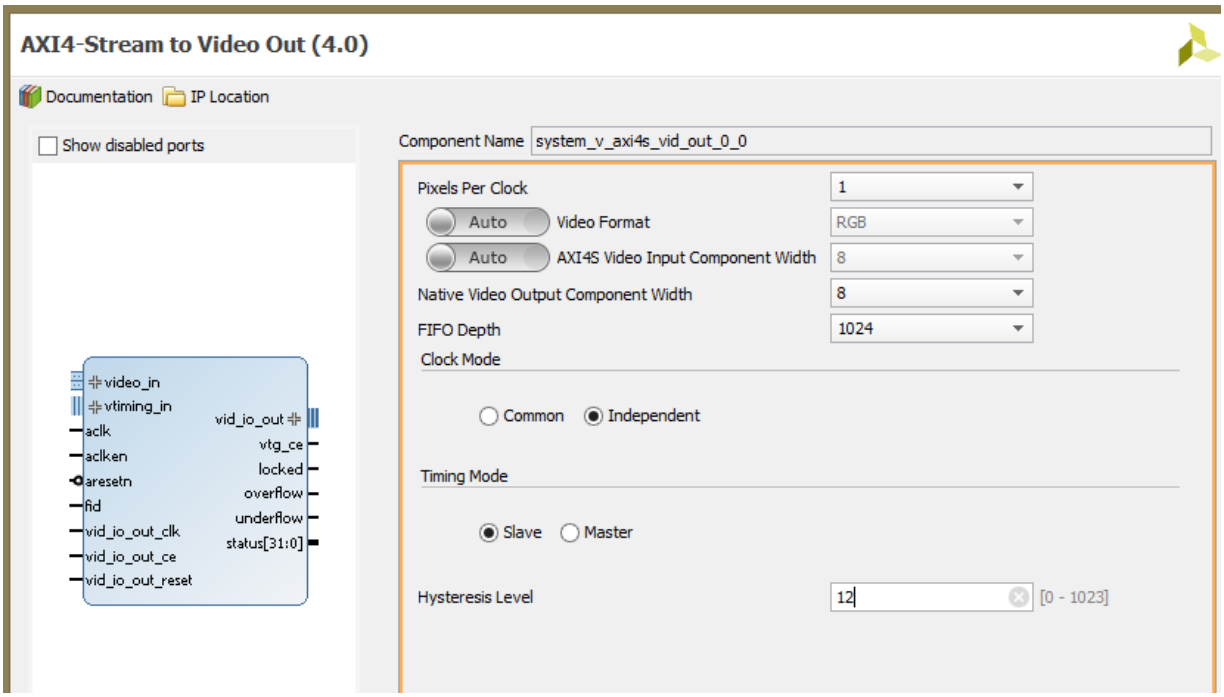

Figure 18. AXI-Stream to Video OUT Configuration

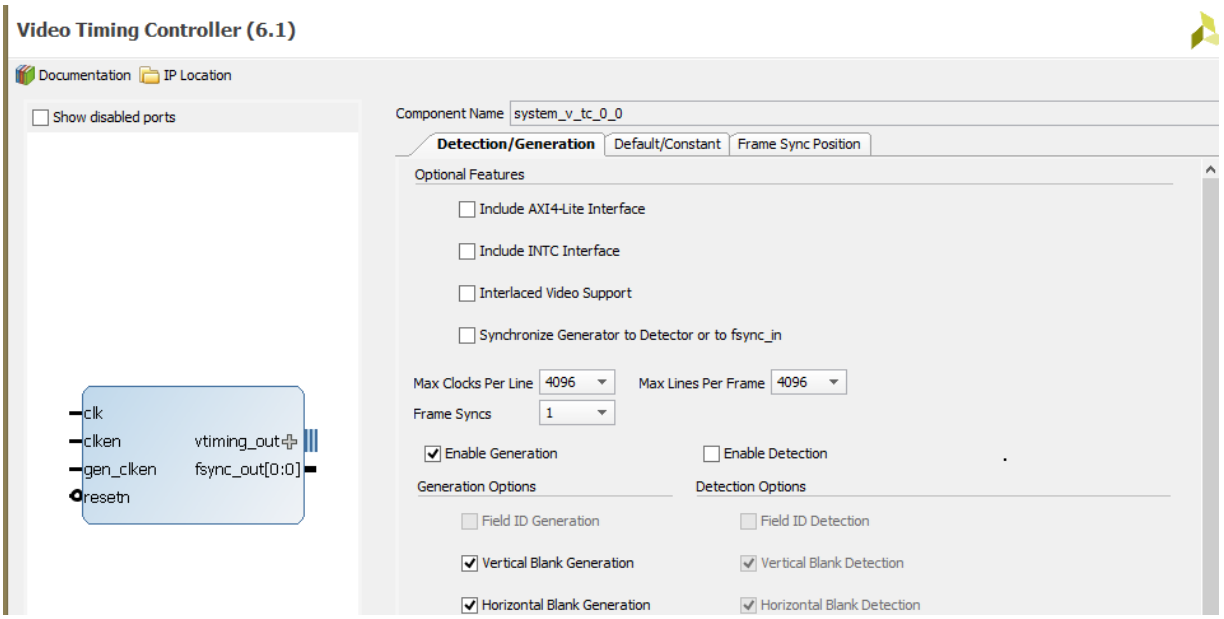

Figure 19. Video Timing Controller Configuration (1)

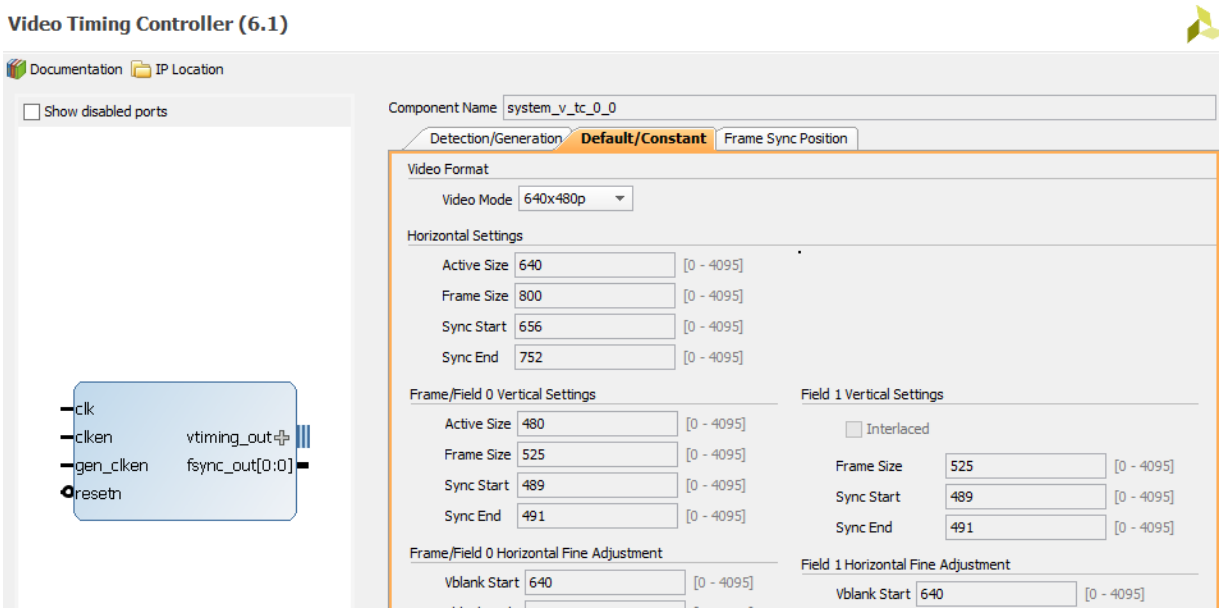

Figure 20. Video Timing Controller Configuration (2)

3.2.4 Clock Divider

PS generates 100 MHz clock frequency, but ov7670 camera operates at 50 MHz and VGA operates at 25 MHz. Clock Wizard block divides PS clock and generates 50 MHz and 25 MHz clock frequency. Customization of clock wizard block showed in the figure.

Figure 21. Clocking Wizard

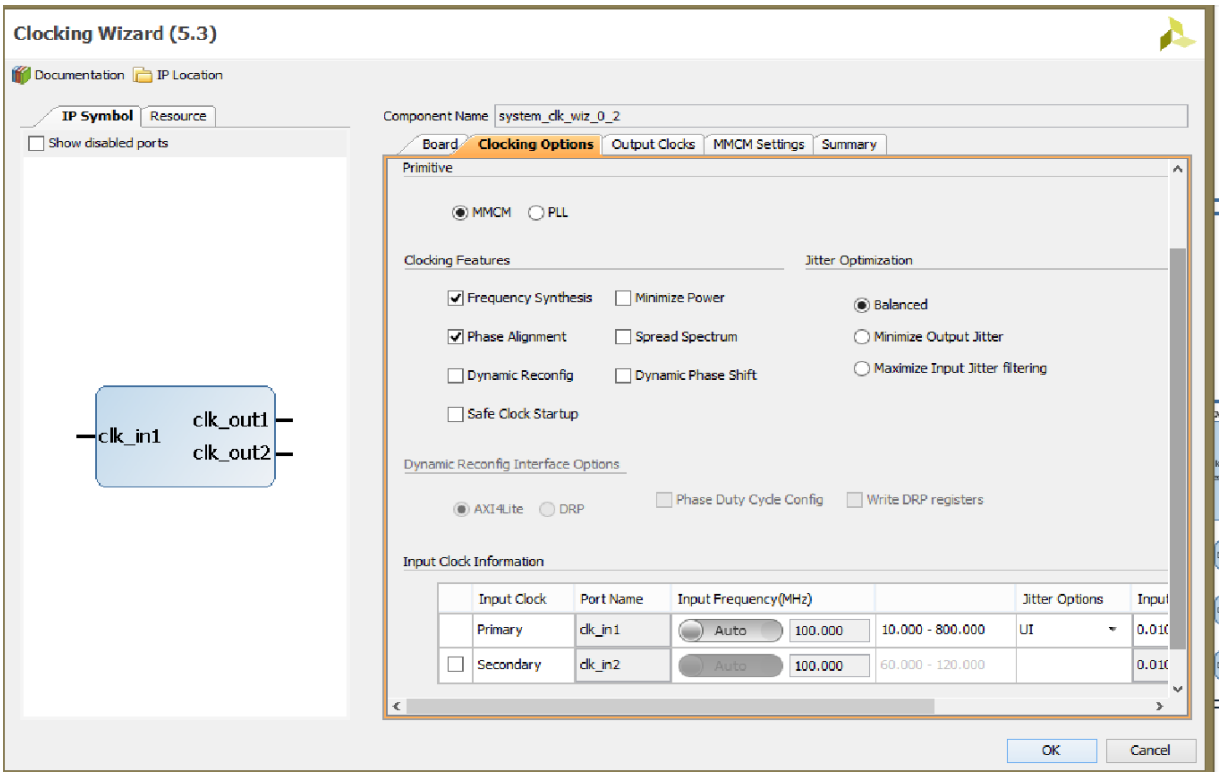

Figure 22.Clock Wizard Configuration (1)

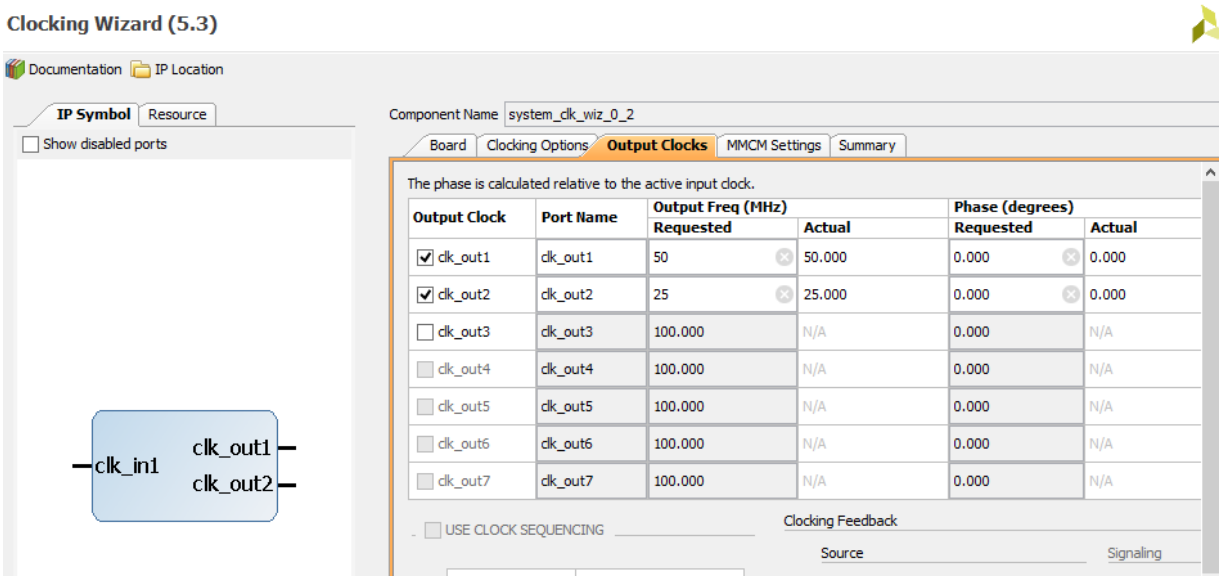

Figure 23. Clock Wizard Configuration (2)

3.2.4 Zynq Processing System

To control whole system by processor, two AXI interconnect blocks and Zynq7 Processing System block Vivado IPs are added. Customization of Zynq7 block showed the in figure. In the block, GP and HP ports should be activated.

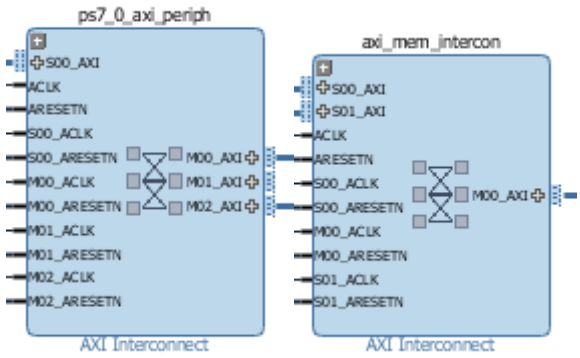

Figure 24. AXI Interconnect

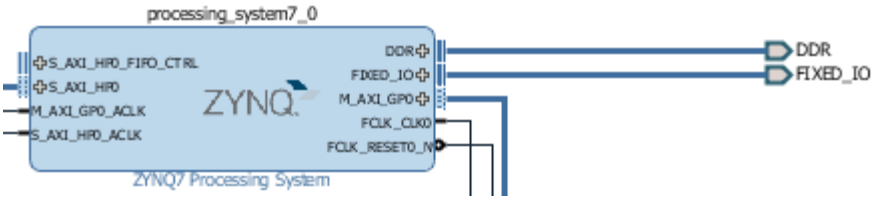

Figure 25.ZYNQ PS

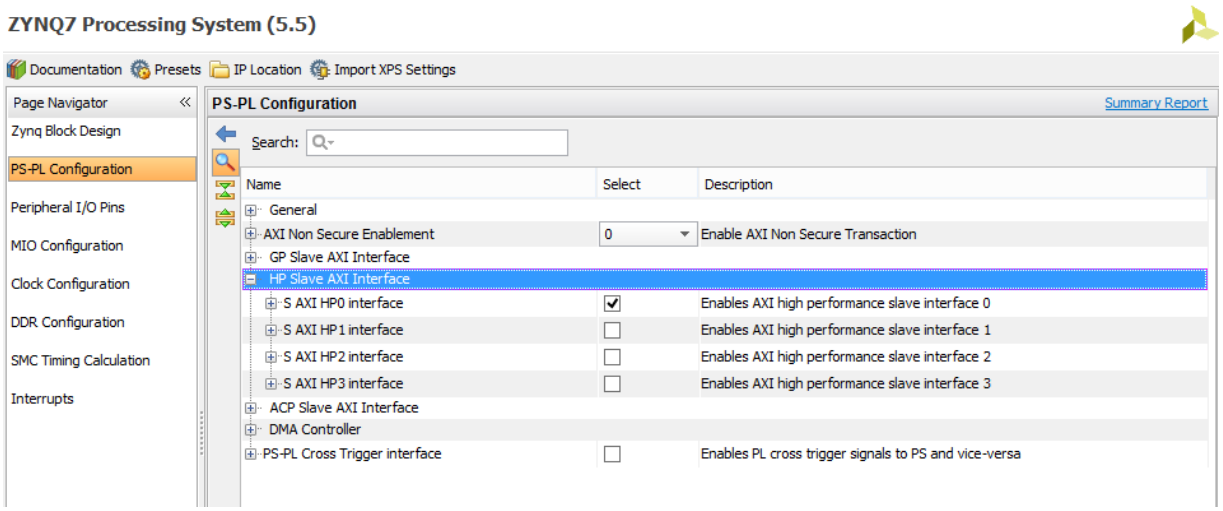

Figure 26. PS Configuration

3.3 PS Design

In the PS design, a feedback algorithm is created. PS compare centre of green and red objects. Every frame, it takes distance between two colours. When the centres are matched, it stops on that location. For this, I putted a red paper on gripper and it selected green tennis ball. After matching, using switch 1, robot arm moved to the blue point and gripped object which is determined. Same feedback algorithm works for this. Finally, using switch 2 arm left the object to the blue point.

3.3.1 vdma_main file

To run VDMA run_tripple_buffer function is used. It is driver of the VDMA. To read pixel data from DDR, Xil_In32 function is used. To scan every pixel value, two nested loop is used. First loop counts 640 horizontal sync of frame and second loop counts 480 vertical sync of frame. Then, the data (pixel) is stored unsigned integer variable. Then, red, blue, green pixels are counted. When first loop (i) and second loop (j) counters are divided to blue, red, green

counter values, location of the objects is found. To move robot arm joints, characters decimal 0 to 7 ASCII values are transmitted.

3.3.2 vdma_api file

This c file is provided from Vivado SDK example project in the Xilinx setup folder. To use it, the design should have VDMA with both MM2S and S2MM paths enabled

5.CONCLUSION

The goal of this project is to create a smart object placing device which is controlled by colour of the object. Big cargo companies need to place objects from one location to another. Autonomous systems work cheaper and effective. In the project, Xilinx ZYNQ7 SoC platform is used. Its ease of use and flexibility made my work easier. If change of colour, size, or location etc. is needed, one can modify FPGA block and C algorithm. Vivado Design Suite 2016.4 was used for VHDL and Vivado SDK was used for C code. All steps that must be followed and equipment's and software environment were explained.

In system design section, Firstly, equipment's and components listed and explained principles of work. Secondly, PL design explained. VDMA, Debounce, AXI interconnect, OV7670 Camera, Zynq7 Processor System, VGA, clock wizard blocks were explained in detail. Thirdly, PS design explained, and VDMA driver initialization, C codes detailed. Finally, I clarified whole system design.

The total cost of the whole project is as follows:

- Zybo 190 USD (Academic)
- Ov7670 camera 12 USD
- VGA Monitor 80 USD
- HC06 Bluetooth Module 4 USD
- Robot Arm 80 USD

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[13] ug761_axi_reference_guide

6. APPENDIX

https://github.com/oguzsimsek/Engineering_Project_2017