CSE 331 HOMEWORK-4

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MAIN CONTROL TESTBENCH

```
add wave -position end  sim:/testbench_control/MemWrite
add wave -position end  sim:/testbench_control/MemtoReg
add wave -position end  sim:/testbench_control/RegDst
add wave -position end  sim:/testbench_control/RegWrite
add wave -position end  sim:/testbench_control/opcode
VSIM 13> run
# RType => op=0000,RegDst=1,ALUSrc=0,MemtoReg=0,RegWrite=1,MemRead=0,MemWrite=0,Branch=0,ALUop=000
# Addi => op=0001,RegDst=0,ALUSrc=1,MemtoReg=0,RegWrite=1,MemRead=0,MemWrite=0,Branch=0,ALUop=100
# Andi => op=0010,RegDst=0,ALUSrc=1,MemtoReg=0,RegWrite=1,MemRead=0,MemWrite=0,Branch=0,ALUop=101
# Ori => op=0011,RegDst=0,ALUSrc=1,MemtoReg=0,RegWrite=1,MemRead=0,MemWrite=0,Branch=0,ALUop=110
# Nori => op=0100,RegDst=0,ALUSrc=1,MemtoReg=0,RegWrite=1,MemRead=0,MemWrite=0,Branch=0,ALUop=011
VSIM 14> run
# beq => op=0101,RegDst=0,ALUSrc=0,MemtoReg=0,RegWrite=0,MemRead=0,MemWrite=0,Branch=1,ALUop=011
# bne => op=0110,RegDst=0,ALUSrc=0,MemtoReg=0,RegWrite=0,MemRead=0,MemWrite=0,Branch=1,ALUop=001
# slti => op=0111,RegDst=1,ALUSrc=1,MemtoReg=0,RegWrite=1,MemRead=0,MemWrite=0,Branch=0,ALUop=010
# lw => op=1000,RegDst=0,ALUSrc=1,MemtoReg=1,RegWrite=1,MemRead=1,MemWrite=0,Branch=0,ALUop=001
# sw => op=1001,RegDst=0,ALUSrc=1,MemtoReg=0,RegWrite=0,MemRead=0,MemWrite=1,Branch=0,ALUop=001
```

ALU CONTROL TESTBENCH

```
add wave -position end  sim:/testbench_ALUcontrol/Result
VSIM 7> run
# ALUop=000,Func=000,Result2=000
# ALUop=000,Func=001,Result2=001
# ALUop=000,Func=010,Result2=110
# ALUop=000,Func=011,Result2=010
# ALUop=000,Func=100,Result2=001
run
# ALUop=000,Func=101,Result2=000
# ALUop=101,Func=000,Result2=101
# ALUop=101,Func=111,Result2=100
# ALUop=100,Func=000,Result2=100
# ALUop=100,Func=011,Result2=010
run
# ALUop=101,Func=000,Result2=101
# ALUop=101,Func=010,Result2=110
# ALUop=110,Func=000,Result2=000
# ALUop=101,Func=111,Result2=100
# ALUop=111,Func=000,Result2=000
run
# ALUop=111,Func=110,Result2=101
# ALUop=011,Func=111,Result2=100
# ALUop=101,Func=000,Result2=101
VSIM 8> run
```

ALU32 TESTBENCH

```
add wave -position end  sim:/testbench_ALU/A
add wave -position end  sim:/testbench_ALU/ALUop
add wave -position end  sim:/testbench_ALU/B
add wave -position end  sim:/testbench_ALU/Result
VSIM 9> run
# time =  0, A =00000011010111110001000001001011, B=00000001110011010011111101000001, A+B=00000101001011000100111101001100,S=001
# time = 20, A =01010011011111000101000001111010, B=00000001110011010011111101000001, A+B=01010101010010011000111101111011,S=001
# time = 40, A =00000000000000000000000100000001, B=11111111111111111000011111000001, A AND B=00000000000000000000000100000001,S=000
# time = 60, A =11111111000011001000010101100111, B=11111111111111111000011111000111, A AND B=11111111000011000000010101000111,S=000
# time = 80, A =00000111010111101100001100000010, B=00100011111111110000000000010011, A - B=00101011010111001100001100010110,S=010
run
# time = 100, A =01010000000000001111111111110111, B=00000011001111100000000101110000, A - B=01010011001111111000000100101000,S=010
# time = 120, A =00000000000000000000000100000001, B=11111111111111111000011111000001, A XOR B=11111111111111111000011101000000,S=011
# time = 140, A =00100000000001110011001101000000, B=01110011011101010011001100000000, A XOR B=01010011011100100000000001000000,S=011
# time = 160, A =00000000010100010000001111111111, B=00110101010110101111001100001100, A NOR B=11001010101001000000110000000000,S=100
# time = 180, A =00000000000000111011111110110000, B=11111111111111111000011111000111, A NOR B=00000000000000001000000000001000,S=100
run
# time = 200, A =00000000000000000000000100000001, B=00000000000000110000111100001101, A OR B=00000000000000110000111100001101,S=101
# time = 220, A =00000000000000000000000000001111, B=00000000000000000000000000000101, A OR B=00000000000000000000000000001111,S=101
VSIM 10> run

VSIM 10>
```

REGISTER TESTBENCH

```
add wave -position end  sim:/testbench_Registers/read_data_1
add wave -position end  sim:/testbench_Registers/read_data_2
add wave -position end  sim:/testbench_Registers/read_reg_1
add wave -position end  sim:/testbench_Registers/read_reg_2
add wave -position end  sim:/testbench_Registers/write_data
add wave -position end  sim:/testbench_Registers/write_reg
VSIM 12> run
# read_data_1=xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx,read_data_2=xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, write_data=xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
yet),
#  read_reg_1=xxx, read_reg_2=xxx, write_reg=xxx, RegWrite=x, clk=x
# read_data_1=00000000000000000000000000000001,read_data_2=00000000000000000000000000000011, write_data=11110000100000010000000000010000
yet),
#  read_reg_1=001, read_reg_2=011, write_reg=001, RegWrite=0, clk=1
# read_data_1=00000000000000000000000000000100,read_data_2=00000000000000000000000000000001, write_data=11110000100000010000000000010000
yet),
#  read_reg_1=100, read_reg_2=001, write_reg=011, RegWrite=1, clk=1
# read_data_1=00000000000000000000000000000010,read_data_2=00000000000000000000000000000001, write_data=11110000100000010000000000010000
yet),
#  read_reg_1=010, read_reg_2=001, write_reg=011, RegWrite=0, clk=1
# read_data_1=00000000000000000000000000000000,read_data_2=00000000000000000000000000000001, write_data=11110000100000010000000000010000
yet),
#  read_reg_1=000, read_reg_2=001, write_reg=010, RegWrite=1, clk=1

VSIM 13>
```

Challenging Parts

I didn't do program counter part and because of this part I couldn't complete the connections with program counter otherwise it works correctly.