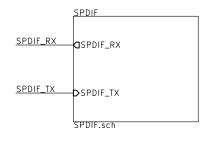
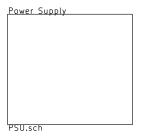
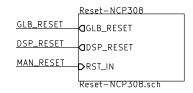
Open Hardware DSP Platform - www.ohdsp.org uDSP 1.1

A 5cm x 5cm DSP board using Analog Device SigmaDSP devices Supports ADAU1466, ADAU1462, ADAU1452, ADAU1451, ADAU1450 Selfboot and external control supported All I/O routed out

	DSP	
IN_LRCLK0	-DADCIN_LRCLKO	DACOUT_LRCLKOD OUT_LRCLKO
IN_BCLK0	-DADCIN_BCLKO	DACULT BCLKUD OUT BCTKO
IN_SDATA0	-DADCIN_SDATA0	DACOUT_SDATAOD OUT_SDATAO
IN_LRCLK1	ADCIN_LRCLK1	DACOUT_LRCLK1
IN_BCLK1	DADCIN_BCLK1	DACOUT_BCLK1
IN_SDATA1	-DADCIN_SDATA1	DACOUT_SDATA1
IN_LRCLK2		OUT LDCLKS
IN_BCLK2	-DADCIN_LRCLK2 -DADCIN BCLK2	DACOUT_LRCLK2D OUT_BCLK2 DACOUT_BCLK2D OUT_BCLK2
IN_SDATA2	DADCIN_BCER2 DADCIN_SDATA2	DACOUT_BCER2D OUT_SDATA2
IN_LRCLK3		OUT I DCI KZ
IN_BCLK3	ADCIN_LRCLK3	DACOUI_LKCLKJ
IN_SDATA3	—DADCIN_BCLK3 —DADCIN_SDATA3	DACOUT_BCLK3D OUT_BCLK3 DACOUT_SDATA3
SPDIF_RX	_	CDDIE TV
	→ADAU_SPDIF_RX	ADAU_SPDIF_TXD SPDIF_IX
AUXADC1	-DAUXADC_IN1	
AUXADC2	-DAUXADC_IN2	
AUXADC3 AUXADC4	— D AUXADC_IN3	SPI_MISOD SPI_MISO
AUXADC4 AUXADC5	– ⊳ AUXADC_IN4	SPI SCIKAL SPI_SCLK
AUXADC5	-PAUXADC_IN5	SPI_MOSIASPI_MOSI
HONADCO	-DAUXADC_IN6	SPI_SS SPI_SS
DSP_RESET	DDSP_RESET	MCLKD MCLK
	DDSF_KESET	MCLKD
SPI_M_MUTE	SPI_M_MUTE	SPI M CIKE SPI_M_CLK
SPI_M_CS1	SPI_M_CS1	STI_M_CLND CDLM MOCI
SPI_M_CS2	SPI_M_CS2	3FI_M_MOSID CDLM MICO
		SPI_M_MISO
	ADAU1452.sch	
IN_LRCLK0	Connectors	DAC LECIKO OUT_LRCLKO
IN_BCLK0	Connectors ADC_LRCLKO	DAC BCLKO OUT_BCLKO
	Connectors ADC_LRCLKO ADC_BCLKO	DAC_BCLKO OUT_BCLKO
IN_BCLK0	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATA0	DAC_BCLKO OUT_BCLKO DAC_SDATAO
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1	Connectors QADC_LRCLKO QADC_BCLKO QADC_SDATA0 QADC_LRCLK1	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_LRCLK1 DAC_BCLK1 OUT_BCLK1
IN_BCLK0 IN_SDATA0 IN_LRCLK1	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATA0 GADC_LRCLK1 GADC_BCLK1	DAC_BCLKO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_BCLK1 DAC_BCLK1 DAC_BCLK1
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1	Connectors QADC_LRCLKO QADC_SDATA0 QADC_LRCLK1 QADC_BCLK1 QADC_SDATA1	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_LRCLK1 DAC_BCLK1 OUT_BCLK1 DAC_SDATA1 OUT_SDATA1
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1	Connectors DADC_LRCLKO DADC_BCLKO DADC_SDATA0 DADC_LRCLK1 DADC_BCLK1 DADC_BCLK1 DADC_BCLK1 DADC_BCLK2	DAC_BCLKO DAC_BCLKO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_BCLK1 DAC_SDATA1 DAC_SDATA1 DAC_LRCLK2 DAT_BCLK2 DAT_BCLK2
IN_BCLKO IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATAO GADC_LRCLK1 GADC_BCLK1 GADC_SDATA1 GADC_SDATA1 GADC_SDATA1 GADC_LRCLK2 GADC_BCLK2	DAC_BCLKO DAC_SDATAO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_SDATA1 DAC_SDATA1 DAC_SDATA1 DAC_SDATA1 DAC_LRCLK2 DAC_BCLK2 DAC_BCLK2 DAC_BCLK2
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_BCLK2 IN_SDATA2	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATAO GADC_LRCLK1 GADC_SDATA1 GADC_SDATA1 GADC_SDATA1 GADC_LRCLK2 GADC_BCLK2 GADC_SDATA2	DAC_BCLKO DAC_SDATAO DAC_SDATAO DAC_LRCLK1 OUT_SDATAO DAC_LRCLK1 OUT_SDATA1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_SDATA1 DAC_LRCLK2 OUT_SDATA2 DAC_SDATA2 OUT_SCLK2 DAC_SDATA2 OUT_SCLK2
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2	Connectors QADC_LRCLKO QADC_BCLKO QADC_SDATAO QADC_LRCLK1 QADC_SDATA1 QADC_SDATA1 QADC_LRCLK2 QADC_BCLK2 QADC_BCLK2 QADC_BCLK2 QADC_BCLK2	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_BCLK1 DAC_BCLK1 OUT_SDATAI DAC_SDATA1 OUT_SDATAI DAC_LRCLK2 OUT_SDATAI DAC_LRCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_LRCLK3
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3	Connectors QADC_LRCLKO QADC_SDATAO QADC_SDATAO QADC_BCLK1 QADC_BCLK1 QADC_SDATA1 QADC_LRCLK2 QADC_BCLK2 QADC_SDATA2 QADC_BCLK3 QADC_BCLK3	DAC_BCLKO DAC_SDATAO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_BCLK1 DAC_SDATA1 DAC_SDATA1 DAC_SCLK1 DAC_BCLK2 DAC_LRCLK2 DAC_BCLK2 DAC_BCLK2 DAC_SDATA2 DAC_SDATA2 DAC_LRCLK3 DAC_LRCLK3 DAC_BCLK3 DAC_BCLK3
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_LRCLK3	Connectors QADC_LRCLKO QADC_BCLKO QADC_SDATAO QADC_LRCLK1 QADC_SDATA1 QADC_SDATA1 QADC_LRCLK2 QADC_BCLK2 QADC_BCLK2 QADC_BCLK2 QADC_BCLK2	DAC_BCLKO DAC_BCLKO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_BCLK1 DAC_SDATA1 DAC_SDATA1 DAC_LRCLK2 DAC_BCLK2 DAC_BCLK2 DAC_SDATA2 DAC_LRCLK3 DAC_LRCLK3 DAC_LRCLK3 DAC_LRCLK3 DAC_LRCLK3 DAC_BCLK3 DAC_BCLK3
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_LRCLK3	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATAO GADC_SDATAO GADC_SDATAI GADC_SDATA1 GADC_LRCLK1 GADC_SDATA1 GADC_LRCLK2 GADC_BCLK2 GADC_SDATA2 GADC_LRCLK3 GADC_SDATA3	DAC_BCLKO DAC_SDATAO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_BCLK1 DAC_SDATA1 DAC_SDATA1 DAC_SCLK1 DAC_BCLK2 DAC_LRCLK2 DAC_BCLK2 DAC_BCLK2 DAC_SDATA2 DAC_SDATA2 DAC_LRCLK3 DAC_LRCLK3 DAC_BCLK3 DAC_BCLK3
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_BCLK2 IN_BCLK3 IN_LRCLK3 IN_SDATA3	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATAO GADC_SDATAO GADC_SDATA1 GADC_SDATA1 GADC_SCLK2 GADC_BCLK2 GADC_BCLK2 GADC_BCLK2 GADC_SDATA2 GADC_SDATA2 GADC_LRCLK3 GADC_SDATA3 GAUXADCIN_1	DAC_BCLKOO DAC_SDATAOO DAC_SDATAOO DAC_LRCLK1 OUT_SDATAO DAC_LRCLK1 OUT_BCLK1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_LRCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_SDATA2 DAC_LRCLK3 OUT_LRCLK3 DAC_BCLK3 OUT_LRCLK3 DAC_SDATA3 OUT_SDATA3
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_BCLK3 IN_SDATA3 AUXADC1	Connectors QADC_LRCLKO QADC_BCLKO QADC_SDATAO QADC_LRCLK1 QADC_SDATA1 QADC_SDATA1 QADC_LRCLK2 QADC_BCLK2 QADC_BCLK2 QADC_SDATA2 QADC_LRCLK3 QADC_SDATA2 QADC_SDATA3 QADC_SDATA3	DAC_BCLKO DAC_BCLKO DAC_SDATAO OUT_BCLKO OUT_SDATAO OUT_BCLK1 OUT_BCLK1 OUT_BCLK1 OUT_SDATA1 OUT_SDATA1 OUT_SDATA1 OUT_SDATA1 DAC_LRCLK2C OUT_LRCLK2 OUT_BCLK2 OUT_BCLK2 OUT_SDATA2 OUT_SDATA2 OUT_SDATA2 OUT_SDATA2 OUT_SDATA3 DAC_BCLK3C OUT_BCLK3 OUT_BCLK3 OUT_SDATA3 DAC_SDATA3C OUT_SDATA3
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_BCLK2 IN_BCLK2 IN_BCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC2 AUXADC3 AUXADC4	Connectors CADC_LRCLKO CADC_BCLKO CADC_BCLK1 CADC_BCLK1 CADC_SDATA1 CADC_SDATA1 CADC_LRCLK2 CADC_SDATA2 CADC_BCLK2 CADC_SDATA2 CADC_SDATA2 CADC_SDATA3 CADC_BCLK3 CADC_SDATA3 CAUXADCIN_1 CAUXADCIN_1 CAUXADCIN_2 CAUXADCIN_2 CAUXADCIN_3	DAC_BCLKO DAC_SDATAO DAC_BCLKO DAC_SDATAO DAC_LRCLK1 DAC_BCLK1 DAC_SDATA1 DAC_SDATA1 DAC_LRCLK2 DAC_BCLK2 DAC_BCLK2 DAC_SDATA2 DAC_LRCLK3 DAC_LRCLK3 DAC_BCLK3 DAC_BCLK3 DAC_BCLK3 DAC_BCLK3 DAC_BCLK3 DAC_BCLK3 DAC_BCLK3 DAC_SDATA3 DAC_SDATA3 SPI_MISO SPI_SCLK SPI_SCLK
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_SDATA2 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC2 AUXADC3 AUXADC4 AUXADC5	Connectors QADC_LRCLKO QADC_BCLKO QADC_SDATAO QADC_LRCLK1 QADC_SDATA1 QADC_SDATA1 QADC_LRCLK2 QADC_BCLK2 QADC_BCLK2 QADC_SDATA2 QADC_LRCLK3 QADC_SDATA2 QADC_SDATA3 QADC_SDATA3	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_LRCLK1 DAC_BCLK1 OUT_SDATA1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_SDATA2 DAC_LRCLK3 OUT_BCLK3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_SCLK SPI_SCLK SPI_SCLK SPI_SSD SPI_SSD
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_BCLK2 IN_BCLK2 IN_BCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC2 AUXADC3 AUXADC4	Connectors	DAC_BCLKO DAC_BCLKO DAC_SDATAO OUT_BCLKO DAC_LRCLK1 OUT_BCLK1 OUT_BCLK1 OUT_BCLK1 OUT_BCLK1 OUT_BCLK1 OUT_BCLK1 OUT_BCLK2 OUT_BCLK2 OUT_BCLK2 OUT_BCLK2 OUT_BCLK2 OUT_BCLK2 OUT_BCLK2 OUT_BCLK3 OUT_BCLK1
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_BCLK2 IN_SDATA1 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC1 AUXADC2 AUXADC3 AUXADC4 AUXADC5 AUXADC6	Connectors GADC_LRCLKO GADC_BCLKO GADC_BCLKO GADC_SDATAO GADC_LRCLK1 GADC_SDATA1 GADC_SDATA1 GADC_LRCLK2 GADC_BCLK2 GADC_BCLK3 GADC_BCLK3 GADC_BCLK3 GADC_SDATA3 GAUXADCIN_1 GAUXADCIN_2 GAUXADCIN_2 GAUXADCIN_4 GAUXADCIN_5 GAUXADCIN_6	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_LRCLK1 DAC_BCLK1 OUT_SDATA1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_SDATA2 DAC_LRCLK3 OUT_BCLK3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_SCLK SPI_SCLK SPI_SCLK SPI_SSD SPI_SSD
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_BCLK1 IN_BCLK1 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC1 AUXADC3 AUXADC4 AUXADC5 AUXADC6 MAN_RESET	Connectors QADC_LRCLKO QADC_BCLKO QADC_BCLKO QADC_SDATAO QADC_LRCLK1 QADC_SDATA1 QADC_LRCLK2 QADC_BCLK2 QADC_BCLK2 QADC_BCLK3 QADC_BCLK3 QADC_SDATA2 QADC_SDATA3 QAUXADCIN_1 QAUXADCIN_2 QAUXADCIN_3 QAUXADCIN_5	DAC_BCLKO DAC_SDATAO DAC_BCLKO OUT_BCLKO DAC_SDATAO DAC_LRCLK1 OUT_BCLK1 DAC_BCLK1 OUT_BCLK1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_SDATA3 SPI_MISO SPI_SCLK SPI_SCLK SPI_SCLK SPI_SCLK SPI_SCLK SPI_SCLK SPI_SCLK SPI_MOSID SPI_MOSI MCLK_INC MCLK
IN BCLKO IN SDATAO IN LRCLK1 IN BCLK1 IN BCLK1 IN BCLK2 IN BCLK2 IN BCLK2 IN SDATA2 IN LRCLK3 IN SDATA3 AUXADC1 AUXADC1 AUXADC2 AUXADC3 AUXADC4 AUXADC5 AUXADC6 MAN_RESET SPI_M_MUTE	Connectors GADC_LRCLKO GADC_BCLKO GADC_BCLKO GADC_SDATAO GADC_LRCLK1 GADC_SDATA1 GADC_SDATA1 GADC_LRCLK2 GADC_BCLK2 GADC_BCLK3 GADC_BCLK3 GADC_BCLK3 GADC_SDATA3 GAUXADCIN_1 GAUXADCIN_2 GAUXADCIN_2 GAUXADCIN_4 GAUXADCIN_5 GAUXADCIN_6	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_BCLK1 DAC_BCLK1 OUT_SDATA1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_LRCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_MISO SPI_SCLK SPI_SCLKD SPI_SCLK SPI_SSD SPI_MOSI SPI_MOSID MCLK_INC MCLK M_SPI_CS2C SPI_M_CS2 M_SPI_CS2C SPI_M_CLK
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_SDATA1 IN_LRCLK2 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC1 AUXADC2 AUXADC3 AUXADC4 AUXADC5 AUXADC6 MAN_RESET SPI_M_MUTE GLB_RESET	Connectors GADC_LRCLKO GADC_BCLKO GADC_SDATAO GADC_SDATAO GADC_SDATAI GADC_SDATA1 GADC_SDATA1 GADC_LRCLK2 GADC_BCLK2 GADC_BCLK2 GADC_SDATA2 GADC_LRCLK3 GADC_BCLK3 GADC_SDATA3 GAUXADCIN_1 GAUXADCIN_1 GAUXADCIN_2 GAUXADCIN_2 GAUXADCIN_4 GAUXADCIN_6 GAUXADCIN_6 GUSB_RST	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_BCLK1 DAC_BCLK1 OUT_BCLK1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_SCLK SPI_SCLKD SPI_SCLK SPI_SSD SPI_SSS SPI_MOSID SPI_MOSI MCLK_INC MCLK M_SPI_CS2 SPI_M_CS2 M_SPI_MOSIC SPI_M_MOSI M_SPI_MOSIC SPI_M_MOSI
IN BCLKO IN SDATAO IN LRCLK1 IN BCLK1 IN BCLK1 IN BCLK2 IN BCLK2 IN BCLK2 IN SDATA2 IN LRCLK3 IN SDATA3 AUXADC1 AUXADC1 AUXADC2 AUXADC3 AUXADC4 AUXADC5 AUXADC6 MAN_RESET SPI_M_MUTE	Connectors QADC_LRCLKO QADC_BCLKO QADC_BCLKO QADC_SDATAO QADC_LRCLK1 QADC_SDATA1 QADC_SDATA1 QADC_BCLK2 QADC_BCLK2 QADC_BCLK3 QADC_BCLK3 QADC_SDATA2 QADC_SDATA3 QAUXADCIN_1 QAUXADCIN_1 QAUXADCIN_2 QAUXADCIN_3 QAUXADCIN_5 QAUXADCIN_5 QAUXADCIN_6 QUSB_RST DM_MUTE	DAC_BCLKO DAC_SDATAO DAC_SDATAO DAC_LRCLK1 OUT_SDATAO DAC_LRCLK1 OUT_SCLK1 DAC_BCLK1 OUT_SDATA1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_LRCLK2 DAC_BCLK2 OUT_SDATA2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_SDATA3 DAC_SDATA3 OUT_SDATA3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_SDATA3 SPI_MISO SPI_SCLK SPI_SCLK SPI_SCL SPI_SCLK SPI_SS SPI_MOSI SPI_MOSI MCLK M_SPI_CS2 SPI_M_CS2 M_SPI_SCLK CULM MOSI
IN_BCLK0 IN_SDATA0 IN_LRCLK1 IN_SDATA1 IN_LRCLK2 IN_SDATA1 IN_LRCLK2 IN_BCLK2 IN_SDATA2 IN_LRCLK3 IN_SDATA3 AUXADC1 AUXADC1 AUXADC2 AUXADC3 AUXADC4 AUXADC5 AUXADC6 MAN_RESET SPI_M_MUTE GLB_RESET	Connectors QADC_LRCLKO QADC_BCLKO QADC_BCLK1 QADC_BCLK1 QADC_SDATA1 QADC_SDATA1 QADC_BCLK2 QADC_BCLK2 QADC_BCLK3 QADC_BCLK3 QADC_SDATA2 QADC_SDATA3 QAUXADCIN_1 QAUXADCIN_1 QAUXADCIN_2 QAUXADCIN_3 QAUXADCIN_5 QAUXADCIN_6 QUISB_RST DM_MUTE DM_RST	DAC_BCLKO OUT_BCLKO DAC_SDATAO OUT_SDATAO DAC_LRCLK1 OUT_BCLK1 DAC_BCLK1 OUT_BCLK1 DAC_SDATA1 OUT_SDATA1 DAC_LRCLK2 OUT_BCLK2 DAC_BCLK2 OUT_BCLK2 DAC_SDATA2 OUT_SDATA2 DAC_LRCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_BCLK3 OUT_BCLK3 DAC_SDATA3 OUT_SDATA3 SPI_MISO SPI_SCLK SPI_SCLKD SPI_SCLK SPI_SSD SPI_SSS SPI_MOSID SPI_MOSI MCLK_INC MCLK M_SPI_CS2 SPI_M_CS2 M_SPI_MOSIC SPI_M_MOSI M_SPI_MOSIC SPI_M_MOSI







Changelog: Revision 1.1:

Add both chip select lines to master SPI headers — removed 3V3 power Add 3V3 monitor option to reset circuit

Notes:

All digital I/O is 3V3. Use outside this voltage can cause damage. See bill of materials for detailed parts information.

KiCad E.D.A. kicad (5.1.0)-1

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Title: uDSP				
Size: A4	Date: 2019-04-02	Rev: 1.1		

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