

to change something post floorplan, pre placement:

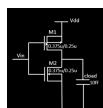
Set :  
:env(var\_name) value

Run\_floorplan

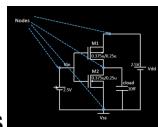
Check in magic that there was a change

Spice simulations:

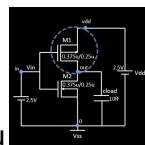
- Create space desk (netlist)
  - Connectivity info
  - Inputs
  - Tap points (output)
  - (pmos = middle arrow out, nmos = middle arrow in)



- Define component values
  - Channel width/channel length
  - Pmos should be 2 or 3x width nmos

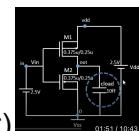


- identify nodes
  - Things separated by a component
  - Can describe any component via nodes
- Name nodes
  - Node lies between x and y node
  - M1(name for mosfet) out(drain node) in(gate) vdd(source) vdd(substrait) pmos

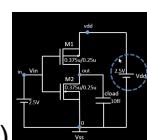


$W=0.375\mu$   $L=0.25\mu$

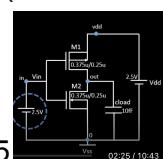
- Defines connectivity



- Cloud(name) out 0 (connected between these nodes) 10f(output)



- Vdd vdd 0 (connected between) 2.5(val)



- Vin in 0.25

- Simulation commands

- .op
- .dc Vin 0 2.5 0.05 (sweep from 0 to 2.5 at steps of 0.05) to measure output)

```
.LIB "tsmc_025um_model.mod" CMOS_MODELS
.end
```

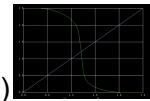
- file of

output, describe all Pmos Nmos

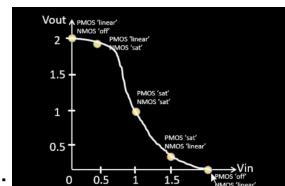
- In SPICE consul, cd into netlist
- Source netlist(circuit file)
- Run
- Setplot (shows which plot is currently in Spice sim)
- Type in name of plot
- Display
- Plot out (want waveform) vs in (sweeping)



- nmos: bigger: (left slant v middle, though 1.5 v 3.75 (pmos bigger) width/length ratio)
- Still same shape
- Vin low, Vout high, and vice versa, reliable on both
- Cmos very robust
- Cmos features proving robustness:

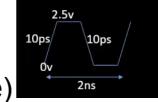


- Switching threshold,  $V_m$  (when  $V_{in}=V_{out}$ ) (draw  $x=y$ , intersection = switching threshold) (when both in saturation region, high leakage current, high probability current flows from + to ground)
- For nmos, low x region pmos on, nmos off, later nmos on, pmos off, so no direct line from power to ground
- $V_m$  lower (0.98 v 1.2) nmos

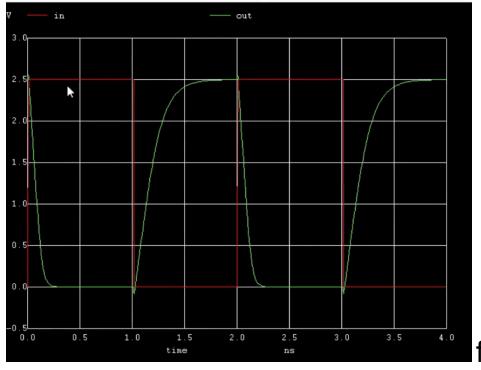


- Labeled wave diagram:
- Gate voltage = drain voltage
- $V_{gs}=V_{ds}$  (current diff direction, but voltage same)
- $I_{ds}=I_{dsn}$
- Transient analysis:

- $V_{in}$  in 0 0 pulse 0 2.5 0(shift 0, start exactly at 0) 10p(rise time)



10p(fall time) 1n(pulse width) 2n(complete cycle)



- or rise delay, go to mid point of rising green + according red, subtract x value (time)
- click on point to get exact position
- same for fall

Wp/Lp	x.Wn/Ln
Wp/Lp	Wn/Ln
Wp/Lp	2Wn/Ln
Wp/Lp	3Wn/Ln
Wp/Lp	4Wn/Ln
Wp/Lp	5Wn/Ln
Rise delay	Fall delay
hh	148ps
	71ps

- Nmos+pmos .lib files:
- How to git clone:



- Copy link under code:

```
% git clone https://github.com/nickson-jose/vsdstdcelldesign.git
```

(creates folder vsdstandard design in openlane directory) ls -ltr in openlane dir:

```
drwxr-xr-x 6 root          root 4096 Jul 21 09:27 vsdstdcelldesign
```

- Inside, same as on github:

```
openLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane
$ cd vsdstdcelldesign
openLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane
/vsdstdcelldesign$ ls -ltr
total 44
drwxr-xr-x 2 root root 4096 Jul 21 09:27 Images
-rw-r--r-- 1 root root 13525 Jul 21 09:27 README.md
-rw-r--r-- 1 root root 11357 Jul 21 09:27 LICENSE
drwxr-xr-x 2 root root 4096 Jul 21 09:27 extras
drwxr-xr-x 2 root root 4096 Jul 21 09:27 libs
-rw-r--r-- 1 root root 2716 Jul 21 09:27 sky130_inv.mag
```

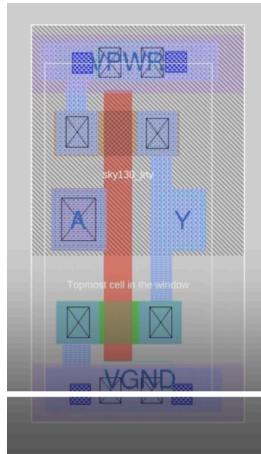
- To get to tec file:

- Cd file.tec dirWeCloned (to move) -

```
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -lfr
total 136
-rw-r--r-- 1 nickson nickson 12529 Sep 15 00:31 README.md
-rw-r--r-- 1 nickson nickson 11357 Sep 15 00:31 LICENSE
drwxr-xr-x 2 nickson nickson 4096 Sep 15 00:31 extras
drwxr-xr-x 2 nickson nickson 4096 Sep 15 00:31 libs
-rw-r--r-- 1 nickson nickson 2716 Sep 15 00:31 sky130_inv.mag
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

- To open in magic: (& moves so not stuck on this command line)

```
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 11016
```



- Inverter:

- 16-mask CMOS process

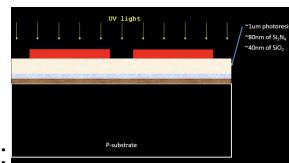
- Select substrate
  - Usually p-type silicon



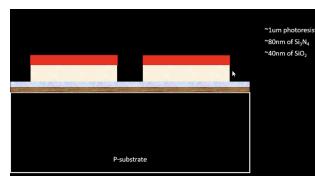
- Properties of p-type silicon:
  - P-type, high resistivity ( $\rho=10 \text{ ohm cm}$ ), doping level ( $10^{17} \text{ cm}^{-3}$ ), orientation (100)
  - Must be doped less than well

- Create active region for transistors (where nmos + pmos go)

- Isolation so don't interfere w/ each other
- 40 nm silicon oxide insulator
- 80 nm silicon nitrate
- 1um photoresist



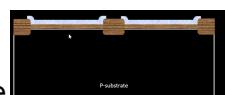
- mask1: (red = protection layer from UV)->



- Now we can etch off silicon nitrate from unprotected areas, and

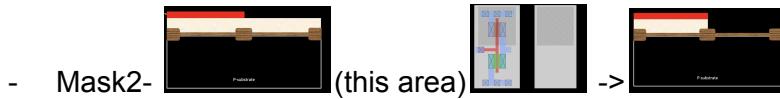


chemically remove photoresist

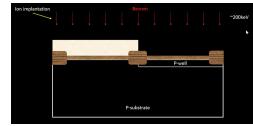


- Put in oxidation furnace ( silicon nitrate protect ~90-95 % underneath from growing)
- Non-grown areas will be transistors

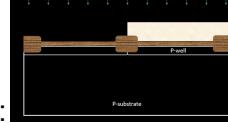
- LOCOS process
- Birds beak area = oxidized region under silicon nitrate
- N-well + p-well fabrication



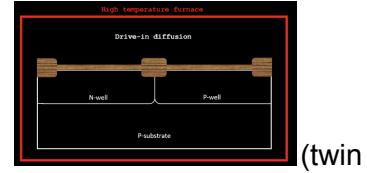
w/ ion implantation



(200keV energy to get through oxidized layer)



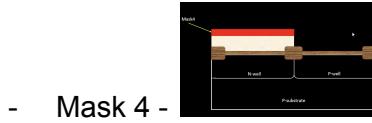
- Do same for n-well:
- Now must diffuse areas so enough room for transistors



- Put in high temp furnace for drive-in diffusion: (twin tub process)

#### - Formation of gate

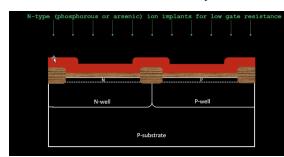
- Control doping concentration + oxide capacitance to control threshold voltage

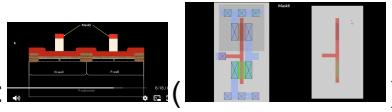
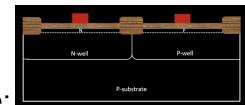
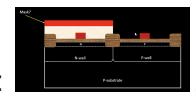
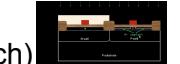
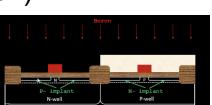
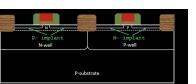
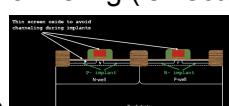
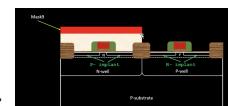
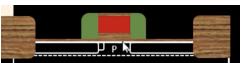
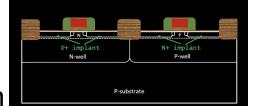
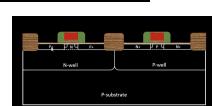


-> (boron low energy to required doping

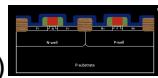


- Do Same for p-mos, w/ arsenic
- To fix silicon oxide (damaged):
  - Use HF to strip old silicon oxide
  - Now regrow again about 10nm (thickness controls capacitance)
- Add 0.4nm polysilicon layer
- Bc gate is low resistance, take n-type (phosphorous or arsenic) as ion implants:

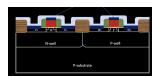


- Mask 6: 
- Etch away extra, left w/ polysilicon gate: 
- Lightly Doped drain (LDD) formation
  - Ideal p+ (pmos), p-(nmos) N(already below), N+N-, P(already below)
  - Reasons for this:
    - Hot electron effect
      - Electric field increases w/ device size
      - Creates breaks in high-energy Si-Si bonds
      - Breaks conduction band (SiO<sub>2</sub>)
    - Short channel effect
      - For short channels, drain field penetrates into channel (had to control current)
- Mask 7: 
- then use phosphorus for implantation (energy chosen so doesn't penetrate too much) 
- Mask 8 (same thing, but with boron) 
- 0.1 um SiO<sub>2</sub> layer, then plasmic anisotropic etching (leaves at side vaults -side wall spacers, integral to transistor, keep separation): 
- Avoids channeling (is vector velocity matched p-substrate, no block, just interacts) 
- Source + drain formation
  - Mask 9: 
  - arsenic exposure, 75 keV (N+implant) 
  - Mask 10 - same but w/ Boron 
  - Goes in high temp furnace (push in): 
  - Steps to form contents and interconnects

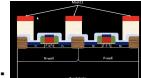
- Rake away thin screen oxide (prevented channeling) with HF
- Deposit titanium (low resistance), via sputtering (hit Ti metal w/ argon gas, bumps Ti metal to substrate)



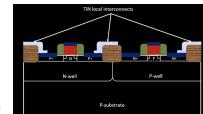
- Heat wafer very hot in N<sub>2</sub> (600-700 C) -> low resistance TiSi<sub>2</sub>:



= TiN (local communication)



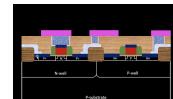
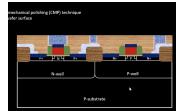
- mask 11: (put where want local contact)
- TiN etched w/ RCA cleaning (de-ionized H<sub>2</sub>O, ammonium hydroxide, hydrogen peroxide)->



- Higher level metal formation:
- 1um SiO<sub>2</sub> doped w/ Phosphorous(protection from wandering electrons) or boron (reduce temp) + polish (chemical mechanical polishing - CMP)



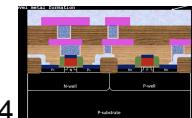
- Mask 12: (in photo TiN (10 um) added too - good barrier between interconnects at top + bottom, and good addition layer)
- Blanket tungsten for good connectivity bottom to top, then CMP again



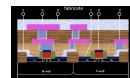
- Aluminum deposit+ mask 13:
- SiO<sub>2</sub> deposited again, CMP, mask 14
- Deposit thin TiN, tungsten, CMP, aluminum w/ mask 15 (level 3 interconnects)



(thickness metal layers increases as goes up)



- Add top dielectric to protect Si<sub>3</sub>N<sub>4</sub>



- Mask 16 to bring last contact out of chip:

- Skywater colors + meanings:

- Hover w/ mouse, says at top what color means

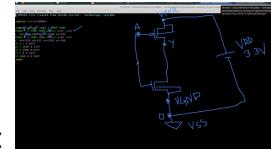
- level1 = local interconnect (light blue)
- Metal 1 = light purple
- Metal 2 = pink
- N-well = solid slanting dark lines (aqua)
- hover on region, click s, type what in consul, says what it is
- Pres s 2x shows what highlighted area is connected to
- Elaborated on github:
  - (LEF) - has all metal layers, not much logic info (gives pins, vdd, gnd, needed to place cell) (protects product ideologically too)
  - how to make standard cells in magic



- (lower left x, y) (upper right x, y)
- Can make layers + contact (dark blue) - connection local interconnectivity + metal
- Crossed line = n substrate (well) + local interconnectivity
- DRC=error (to check, DRC, DRC find next error, zooms on issue, and writes exact issue in consul) - makes sure in line with manufacturer needs
- Do spice sim for logic check:
  - Extract all (in vsdstdcelldesign dir)
  - Says where it put it (vsdstdcelldesign)(.ext file)
  - Ex2spice cthresh 0 rthresh 0 (extracts + gets rid parasitic capacitors)
  - Ex2spice

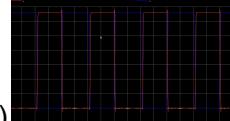


- Now spice file has been created (in spice file: )
- M1000 Y A VPWR VPWR pshort w=37 l=23 pmos - drain gate source substrate



- We can use info to draw out the circuit: (doesn't define all connections (like Vdd ones))
- Set .option scale =0.01u(smallest we can in diagram)
- Add .include ./libs/pshort.lib
- Add .include ./libs/nshort.lib
- Comment out .end (// first)
- Add VDD VPWR VPWR 0 3.3V
- Add VSS VGND 0 0V
- Va (input voltage) A VGND PULSE(0V (low) 3.3V(high) 0(n/s, start pulse) 0.1ns (pulse rise time) 0.1ns (pulse fall time) 2ns (pulse time) 4ns (time))

- .tran (run analysis) 1n(from) 20n(to)
- Switch name of pmos+nmox to pshort\_model.0 + nshort\_model.0 (as seen in SPICE file, so we can assign to simulation and run)
- Less pshort.lib in terminal to see info
- Ngspice sky130 inv.spice (source tool)



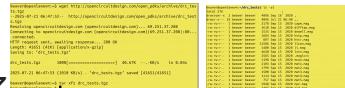
- To see — plot y vs time a (input)
- Spikes at end - cload is too low
- Change from 0.24 fF to 2fF
- Plot again [redacted] -- a little better
- Calc rise transition (20-80) fall (80-20), fall cell delay, rise cell delay, PROPAGATION DELAY - time diff 50 out to 50 in (fall), 50 in to 50 out (rise)

- Magic DRC:

- Open opencircuitdesign.com/magic/
- Clock on using magic, magic tutorials
- Magic command line tool
- .cif = caltech intermediate format (human readable, often
- Google/skywaterpdk on github
- Run magic -dxr met3

- Lab exercise:

- Used this command in terminal to download lab files: `wget http://opencircuitdesign.com/open_pkgs/archive/drc_tests.tgz`
- `cd drc_tests`



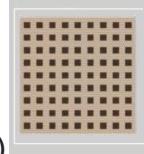
- To extract files, `tar xfz drc_tests.tgz`
- To run magic, `magic -d XR`



- File -> open ->met3.mag
- (use : in consul to redirect all keystrokes to consul, finishing w/ return)
- Create box around an element, for error type in console `drc`

```
% drc why
Metal3 spacing < 0.3um (met3.2)
Loading DRC CIF style.
why%
```

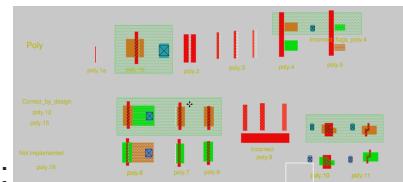
- To visualize via2, create area w/ paint tool, in consul type cif



see VIA2 (feed clear to end) (black squares = contact cuts, show mask layer that there will be in output gds)

- Run command snap in to adjust on microscale
- Click b to show width
  - Errors contained:
    - M3.1: width of metal has to be 0.3 um
    - M3.2 spacing of metal 3 to metal 3 has to be 0.3 um
    - M3.5: Via2(area filled w/ contact cuts) must be enclosed by Met3 on one of two adjacent sides by at least 0.065 um
    - M3.6: min area of metal3 is 0.24 um^2
    - M3.3c: Min. spacing of features attached to or extending from huge\_met3 for a distance of up to 0.400 μm to metal3
    - M3.3d: Min. spacing of huge\_met3 to metal3 excluding features checked by m3.3a is 0.4 um

Poly 9 fix:



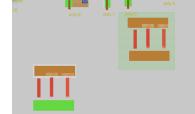
- Loaded poly.mag to see: (flags errors)
- Run vi sky130A.tech in drc\_tests directory
- Change 1: add rule to poly, touching based on space illegal(allpolynonres, poly and all things touching)
 

```
spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
  "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
```
- Change 2: add
 

```
spacing npres allpolynonres 480 touching_illegal \
```
- :wq to save
- Now restart magic to see change: 'tech load sky130A.tech' and 'drc check'



- Poly now correctly sized, but other layers not:



- Drew two structures : , errors because of spacing
- change \*nsd to alldiff

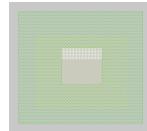
We want to add rule so that any gates not used after sequence are definitionally errors

- In sky130A.tech:

- Temp layers don't get output as part of design
- Building blocks for other layers
- since DRC doesn't make GDS output, only temp layers
- Shrinks nwell to go legal amount over deep nwell:
 

```
# Ensure nwell overlaps dowell at least 0.4um outside and 1.03um inside
templayer dowell_shrink dowell
shrink 1030
```
- Grows nwell so at least 400 over deep nwell, least possible area to satisfy overlap and overflow rules. If any area doesn't contain nwell, one of two rules is being violated, last nwell line means left over if any rule violated. This passes back to maxwidth, so anything left over flagged as error

```
templayer nwell_missing dowell
grow 400
and-not dowell_shrink
and-not nwell
```



- So to fix nwell.6:
- Select component
- In consul: cif ostyle drc
- To see area of shrink: cif see dowell\_shrink

```
% cif ostyle drc
CIF output style is now "drc"
.layout1.pane.top.magic
There's no material visible underneath the cursor.
Switching to NETLIST tool.
Switching to PICK tool.
Switching to BOX tool.
% cif see nwell_shrink
CIF name "nwell_shrink" doesn't exist in style "drc".
The valid CIF layer names are: dowell_shrink, nwell_missing, dnwell_missing, mim_bottom, mim2_bottom, ptap_reach, ptap_missing, ntap_reach, ntap_missing, dptap_reach, dptap_missing, mi_small_hole, mi_hole_empty, m2_small_hole, m2_hole_empty.
% cif see dowell_shrink
```

- Feed clear
- Cif see nwell\_missing
- Drc fast - don't have to load everything, and slow (loads all) switch via drc style fast/slow
- For second error on nwell.4:
  - All wells will contain metal-contacted tap (no space specified between, so no easy edge rule, but good for cit output rule—take all ntap contacts and expand to fill area of nwell underneath)

- Use operator bloat-all –takes set of all nwell, removes all w/ taps, rest are errors
- To accomplish this, add

```
templayer nwell_tapped
```

```
bloat-all nsc nwell
```

```
on "drc"
```

```
templayer nwell_untapped nwell
```

```
and-not nwell_tapped
```

```
variants (full)
```

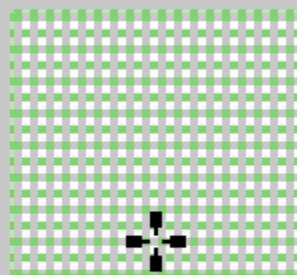
```
  cifmaxwidth nwell_untapped 0 bend_illegal \
    "nwell missing tap (nwell.4)"
```

```
variants *
```

```
"
```

- Variants = not always checked in drc, only when full
- Then load tech file, drc check, drc style drc(full): (error over full, bc not tapped)

ERROR: Incorrect Implementation



nwell.4

- When we add tap, error goes away:

