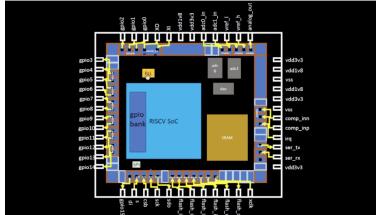


Processor layout:



Package (pinouts labeled and shown in connection to chip):

Pad (outer ring of blue) - send signal through chip (info can be transferred in and out chip through this)

Core (black) - all digital logic

Foundry IP's (yellow + grey) - need intelligence to build blocks

Macros (inner blue + small white)

### RISC-V Instruction Set Architecture (ISA):

Compile computer language program to convert (ultimately) to machine language (ex. binary)

Hardware description language to implement RISC-V architecture specifications (ex. picorv 32 cpu core), which then goes to machine language

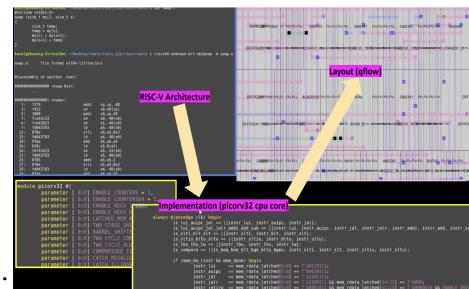


figure showing flow from user view to hardware:

app-> system software (OS, compiler, assembler) -> hardware

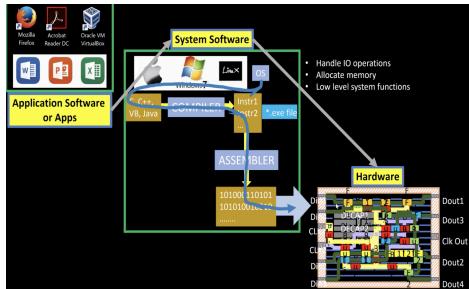
### Role of OS:

- IO operations
- Memory control and assignment
- Low level system processes
- Translate to machine language via compiler + assembler

Compiler - code -> instructions(varies in syntax by hardware)\*.exe file (abstract interface/instruction set architecture - language human connects to hardware)

Assembler - instructions -> binary (machine language) (RTL snipped gates netlist)

Diagram showing flow from app to hardware through system software:



To design ASIC's:

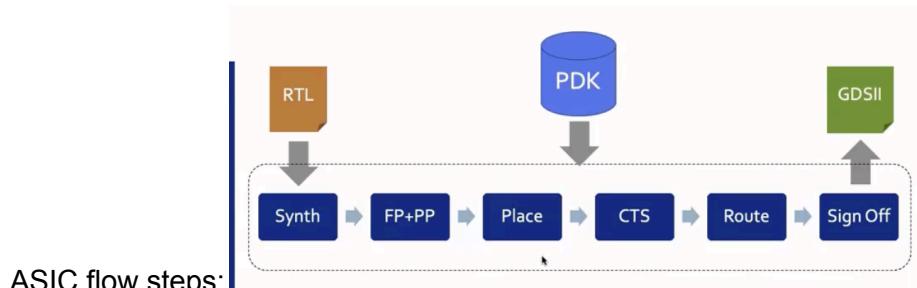
- RTL IP's
- EDA tools
- PDK data

Many open source options of these for first two, now google x Skywater PDK (130 nm process, v current capacity 5 nm - still 60% market (bc not all need to be 5nm high tech, still cheaper) stil fase, ex. Intel: P4EE)

Separation of design only and fabrication only companies very recent

PDK = interface between two

- Device model
- Tech info
- Design rule
- Standard cell libraries



ASIC flow steps:

1. Synthesis:
  - design to HDL described component from standard cell library (diff. Models based on EDA tool)(gate level netlist, functionally like RTL)
2. FP + PP
  - Macro v full chip diffs
  - Design silicon, how power circuit
  - Die between components
  - Define macro dimensions + pin places, routing tracks
  - Power pens defined - parallel for less resistance
3. Placement
  - on macros, gate level netlist plans placed
  - Connected close
  - global (optimal for all, but not necessarily legal) + detailed (min. alter from global for legality)

4. Clock routing
  - Deliver clock to all clock cells
  - Best shape
  - Min skew (diff time clock arrival)
5. Signal Route
  - Find valid placement horizontal + vertical wires given placement + metal layers (defined by pdk)
  - Routing grid out of metal layer tracks (mostly)
  - global, then fine grade
6. Sign Off
  - Make sure final layout matches netlist
  - Static timing analysis

Open source issues:

- Tool qualification
- Tool calibration
- Missing tools

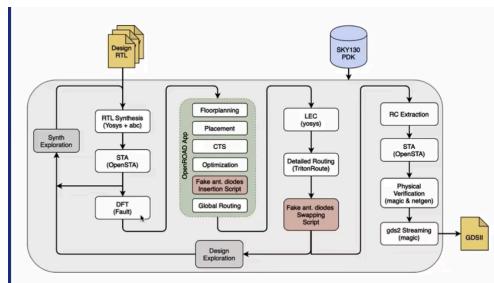
Openlane - open source flow for open source tapeout

Clean GDSII, no human intervention

Clean:

- No LVS violations
- No DRC violations
- No timing violations

World w/ macros + chips



Openlane ASIC flow:

Needs PDK

1. RTL synthesis
  - RTL fed to yosys w/ constraints
  - Yosys translates RTL to logic circuit
  - Optimized + mapped w/ abc (design explorer, report on bunch of configurations)
2. DFT (testing)
  - Auto simulation + test
3. Physical Implementation
  - FP + PP
  - End decoupling capacitors + tap cell insertion
  - Global+detailed placement + optimization pst
  - Clock tree synthesis
  - Routing, global + detailed

- Fake antenna diodes insertion - charge collects on too long wire, charge accumulates, transistor damaged during fabrication (fixes bridging or antenna diodes (to take away charges)) preventive, fake antenna diode to every cell input after placement, if reports violation, replace w/ real diode
4. LEC (logic equivalence testing)
    - Compare netlist from optimization w/ original
  5. analysis
    - RC extraction
    - STA
    - To sign off, Design rules checking

In work/tools/openlane\_woring\_dir/pdk there are two items:

- Libs.ref - specific to process

```
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ cd libs.ref/
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ ls -ltr
total 44
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_hd
drwxr-xr-x 6 nickson nickson 4096 Jul 28 09:44 sky130_fd_pr_rf
drwxr-xr-x 7 nickson nickson 4096 Jul 28 09:44 sky130_fd_pr_base
drwxr-xr-x 11 nickson nickson 4096 Jul 28 09:44 sky130_fd_io
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_ls
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_hs
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_hdll
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_hd
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_ms
drwxr-xr-x 5 nickson nickson 4096 Jul 28 09:44 sky130_fd_pr_rf2
drwxr-xr-x 12 nickson nickson 4096 Jul 28 09:44 sky130_fd_sc_lp
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ ls
```

- Libs.tech - specific to tool

```
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ cd libs.tech/
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ ls -ltr
total 24
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 klayout
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 ngspice
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 netgen
drwxr-xr-x 3 nickson nickson 4096 Jul 28 09:44 magic
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 qflow
drwxr-xr-x 7 nickson nickson 4096 Jul 28 09:44 openlane
```

We are interested in sky130\_fd\_sc\_hd:

```
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ cd sky130_fd_sc_hd
nickson@nickson-VirtualBox:~/Desktop/work/tools/openlane_working_dir/pdk$ ls -ltr
total 104
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 verilog
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 spice
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 techlef
drwxr-xr-x 2 nickson nickson 36864 Jul 28 09:44 maglef
drwxr-xr-x 2 nickson nickson 36864 Jul 28 09:44 mag_I
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 gds
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 doc
drwxr-xr-x 2 nickson nickson 4096 Jul 28 09:44 cdl
drwxr-xr-x 2 nickson nickson 4096 Aug 12 14:27 lib
drwxr-xr-x 2 nickson nickson 4096 Aug 12 14:29 lef
```

Techlef - layering info

Lib - time files (speed (process corners), temp, voltage)