Design Issues for Dynamic Voltage Scaling

Thomas D. Burd
Berkeley Wireless Research Center
University of California, Berkeley
2108 Allston Way, Berkeley, CA 94704
+1-510-666-3151
burd@eecs.berkeley.edu

Robert W. Brodersen
Berkeley Wireless Research Center
University of California, Berkeley
2108 Allston Way, Berkeley, CA 94704
+1-510-666-3110
rb@eecs.berkeley.edu

ABSTRACT
Processors in portable electronic devices generally have a computational load which has time-varying performance requirements. Dynamic Voltage Scaling is a method to vary the processor's supply voltage so that it consumes the minimal amount of energy by operating at the minimum performance level required by the active software processes. A dynamically varying supply voltage has implications on the processor circuit design and design flow, but with some minimal constraints it is straightforward to design a processor with this capability.

Keywords
Energy efficient, variable voltage, processor, circuit design.

1. INTRODUCTION
Processors used in portable electronic devices have the conflicting requirements to provide both ever-increasing performance and ever-decreasing energy consumption. A technique called Dynamic Voltage Scaling (DVS) addresses these requirements by exploiting the computational burstiness in these devices where typically only a fraction of the computation utilizes the full processor performance. By varying the supply voltage and clock frequency on demand, DVS provides the highest possible performance when required while minimizing the energy consumption during the remaining low performance periods.

DVS has been demonstrated on a complete embedded processor system [1]. This prototype system contains 4 custom chips in 0.6µm 3-metal CMOS: a battery-powered DC-DC voltage converter, a microprocessor (ARM8 core with 16kB cache), SRAM memory chips, and an interface chip for connecting to commercial I/O devices. The entire system can operate from 1.2-3.8V and 5-80MHz while the energy consumption varies from 0.54-5.6 mW/MIP.

This paper describes the fundamental trade-off of DVS, as well as DVS' impact on design flow and circuit design. By following a simple set of rules and design constraints, the design of DVS circuits moderately increases design validation and reduces energy-efficiency at a fixed voltage. However, these constraints are heavily outweighed by the potential 10x increase in energy efficiency when the voltage can dynamically vary.

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1.1 DVS Processor
The prototype processor, pictured in Figure 1, is a fully functional microprocessor for portable systems. The design contains a multitude of different circuits, including static logic, dynamic logic, CMOS pass-gate logic, memory cells, sense-amps, bus drivers, and I/O drivers. All these circuits have been demonstrated to continuously operate over voltage transients in excess of 1V/µs.

While the prototype system demonstrates DVS in a 3.3V, 0.6µm process technology, DVS is a viable technique for improving processor system energy efficiency well into deep-sub-micron process technologies. Maximum V_{DD} decreases with advancing process technology, seeming to reduce the potential of DVS, but this decrease is alleviated by decreases in V_T. While the maximum V_{DD} may be only 1.2V in a 0.10µm process technology, the V_T will be ~0.35V yielding an achievable energy efficiency improvement, V_{DD}^2/V_T^2, still in excess of 10x.

2. DVS FUNDAMENTALS
Processors generally operate at a fixed voltage, and require a regulator to tightly control voltage supply variation. The processor pro-

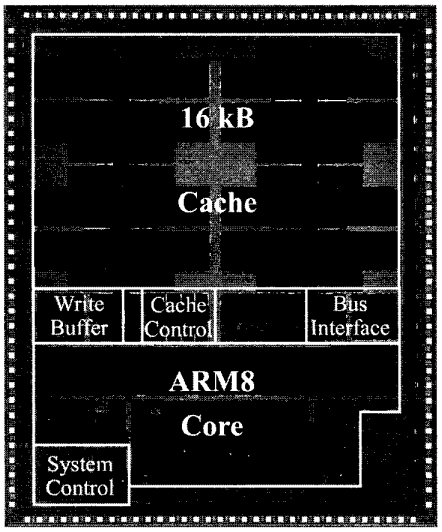

Figure 1. CPU Die Photo (7.5x9.0mm).

duces large current spikes for which the regulator's output capacitor supplies the charge. Hence, a large output capacitor is desirable to minimize ripple on the voltage supply.

The voltage converter required for DVS is fundamentally different from a standard voltage regulator because in addition to regulating voltage for a given clock frequency, it must also change the operating voltage, V_{DD}, when a new clock frequency is requested. Since the hardware, by itself, has no knowledge of the importance of the current instruction it is executing, the operating system software controls the clock frequency by writing to a register in the system control state [2].

2.1 Feedback Loop

The feedback loop for converting a desired operating frequency, F_{DES}, into V_{DD} is shown in Figure 2. The ring oscillator converts V_{DD} to a clock signal, f_{CLK}. A counter converts f_{CLK} to a digital measured frequency value, F_{MEAS}. This value is subtracted from F_{DES} to find the frequency error, F_{ERR}. The loop filter implements a hybrid pulse-width/pulse-frequency modulation algorithm which generates an M_P or M_N enable signal. The inductor, L, transfers charge to the capacitor, C, to generate a V_{DD} which is fed back to the ring oscillator to close the loop.

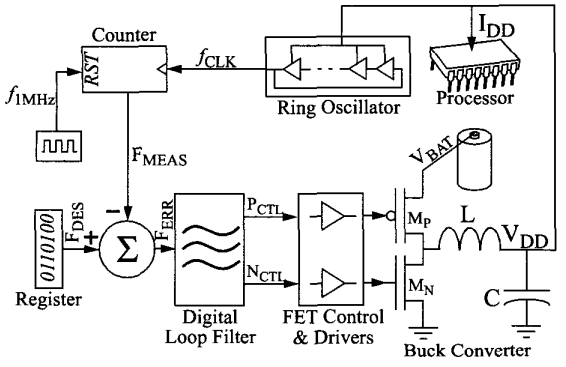

Figure 2. DVS Feedback Loop Architecture.

In addition to the supply ripple and conversion efficiency performance metrics of a standard voltage regulator, the DVS converter introduces two new performance metrics: transition time and transition energy. For a large voltage change (from V_{DD1} to V_{DD2}), the transition time is:

$$t_{TRAN} \approx \frac{2 \cdot C}{I_{MAX}} \cdot |V_{DD2} - V_{DD1}| \qquad \text{(EQ 1)}$$

where I_{MAX} is the maximum output current of the converter, and the factor of 2 exists because the current is pulsed in a triangular waveform. The energy consumed during this transition is:

$$E_{TRAN} = (1-\eta) \cdot C \cdot \left| V_{DD2}^2 - V_{DD1}^2 \right| \qquad \text{(EQ 2)}$$

where η is the efficiency of the DC-DC converter.

A typical capacitance of 100µF yields $t_{TRAN} \approx 520\mu s$ and $E_{TRAN}=130\mu J$ for a 1.2-3.8V transition (for the prototype system: $I_{MAX}=1A$, $\eta=90\%$). This long t_{TRAN} precludes any real-time control or fast interrupt response time, and only allows very coarse speed control. The power dissipated transitioning, is a sizable $130\mu J \bullet f_{VDD}$, where f_{VDD} is the frequency of voltage transitions.

Increasing C reduces supply ripple and increases low-voltage conversion efficiency, making the loop a better voltage regulator, while decreasing C reduces transition time and energy, making the loop a better voltage tracking system. Hence, the fundamental trade-off in DVS system design is to make the processor more tolerant of supply ripple so that C can be reduced in order to minimize transition time and energy. The hybrid modulation algorithm of the loop filter maintains good low-voltage conversion efficiency to counter the effect of a smaller C [3].

2.2 Limitations to Reducing Capacitance

Decreasing capacitance reduces transition time, and by doing so increases dV_{DD}/dt. CMOS circuits can operate with a varying supply voltage, but only up to a point, which is process dependent. This is discussed further in Section 4.

Decreased capacitance increases supply ripple, which in turn increases processor energy consumption as shown in Figure 3. The increase is moderate at high V_{DD}, but begins to increase as V_{DD} approaches V_T because the negative ripple slows down the processor so much that most of the computation is performed during the positive ripple, which decreases energy efficiency.

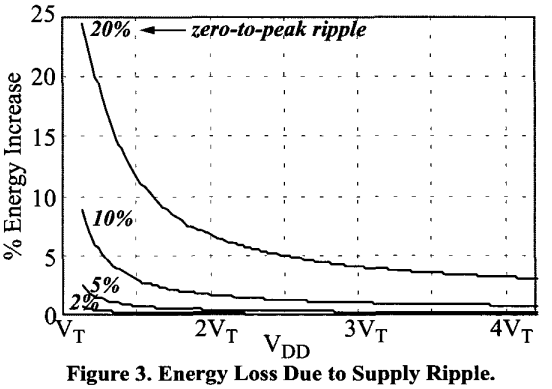

Figure 3. Energy Loss Due to Supply Ripple.

Loop stability is another limitation on reducing capacitance. The dominant pole in the system is set by C and the load resistance (V_{DD}/I_{DD}). The inductor does not contribute a pole because the buck converter operates in discontinuous mode; inductor current is pulsed to deliver discrete quantities of charge to C.

As C is reduced the pole frequency increases, particularly at high I_{DD}. As the pole approaches the sampling frequency, a 1MHz pole due to a sample delay becomes significant, and will induce ringing. Interaction with higher-order poles will eventually make the system unstable.

Increasing the converter sampling frequency will reduce supply ripple and increase the pole frequency due to the sample delay. Thus, these two limits are not fixed, but can be varied. However, increasing the sampling frequency has two negative side-effects. First, low-load converter efficiency will decrease, and f_{CLK} quantization error will increase. These side-effects may be mitigated with a variable sampling frequency that adapts to the system power requirements (e.g. V_{DD} and I_{DD}).

The maximum dV_{DD}/dt at which the circuits will still operate properly is a hard constraint, but occurs for a much smaller C than the supply ripple and stability constraints.

2.3 Transition Power Dissipation

The importance of minimizing the converter output capacitor is demonstrated in Figure 4 which plots transition power for three different transition frequencies. Also plotted is the system power which includes all power dissipated except transition power. This value is highly application dependent, and the value used is the minimum power dissipation of the prototype system.

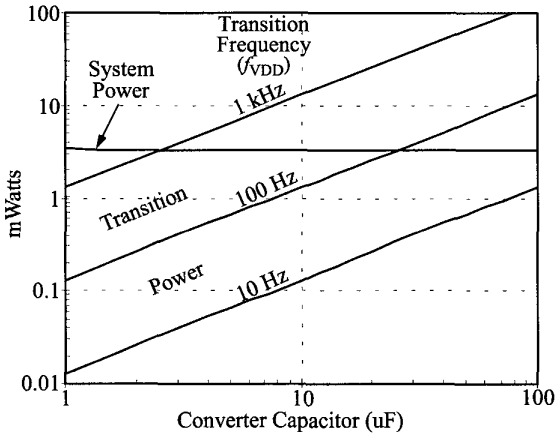

Figure 4. Processor System Power Dissipation.

The transition power, which is also highly application dependent, assumes full-scale voltage changes. For infrequent changes, a large output capacitor is tolerable. For changes on the order of a context switch (30-100Hz), a 100µF capacitor, which is a typical value found in low-power systems, will cause the transition power to dominate the system power (55-80% of the total power).

2.4 Prototype System Design

In the prototype design the converter capacitor was set to 5µF in order to maintain an 84% low-voltage conversion efficiency. This value yields a maximum transition time of 26µs, a full-scale transition power of $6.5\mu J \bullet f_{VDD}$, and a 2% supply ripple. The maximum dV_{DD}/dt is 0.2V/µs and the loop pole is 7kHz at its maximum frequency.

To further improve transition time and energy the capacitance can be reduced as the loop was originally designed for a converter capacitor as low as 0.5µF. This is the lower bound as determined by the stability constraint given the selected 1MHz sampling frequency and processor I_{DD}.

3. DESIGN OVER VOLTAGE

A typical processor targets a fixed supply voltage, and is designed for +/-10% maximum voltage variation. In contrast, a DVS processor must be designed to operate over a much wider range of supply voltages, which impacts both design implementation and verification time.

3.1 Circuit Design Constraints

To realize the full range of DVS energy efficiency, only circuits that can operate all the way down to V_T should be used.

NMOS pass gates are often used in low-power design due to their small area and input capacitance. However, they are limited by not being able to pass a voltage greater than V_{DD}-V_{Tn}, such that a minimum V_{DD} of $2 \bullet V_T$ is required for proper operation. Since throughput and energy consumption vary 4x over the voltage range V_T to $2 \bullet V_T$, using NMOS pass gates restricts the range of operation by a significant amount, and are not worth the moderate improvement in energy efficiency. Instead, CMOS pass gates, or an alternate logic style, should be utilized to realize the full voltage range of DVS.

The delay of CMOS circuits track over voltage such that functional verification is only required at one operating voltage. The one possible exception is any self-timed circuit, which is a common technique to reduce energy consumption in memory arrays. If the self-timed path layout exactly mimics that of the circuit delay path as was done in the prototype design, then the paths will scale similarly with voltage and eliminate the need to functionally verify over the entire range of operating voltages.

3.2 Circuit Delay Variation

While circuit delay tracks well over voltage, subtle delay variations exist and do impact circuit timing. To demonstrate this, three chains of inverters were simulated whose loads were dominated by gate, interconnect, and diffusion capacitance respectively. To model paths dominated by stacked devices, a fourth chain was simulated consisting of 4 PMOS and 4 NMOS transistors in series. The relative delay variation of these circuits is shown in Figure 5 for which the baseline reference is an inverter chain with a balanced load capacitance similar to the ring oscillator.

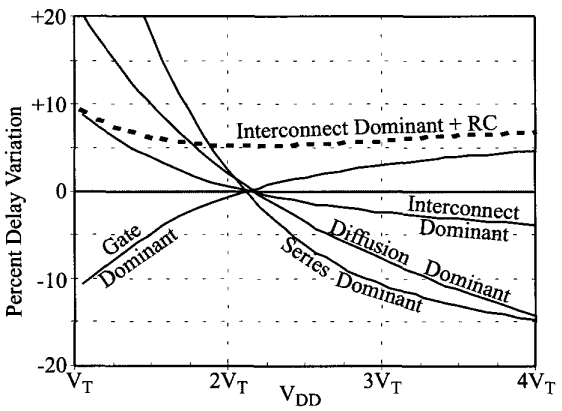

Figure 5. Relative CMOS Circuit Delay Variation.

The relative delay of all four circuits is a maximum at only the lowest or highest operating voltages. This is true even including the effect of the interconnect's RC delay. Since the gate dominant curve is convex, combining it with one or more of the other effects' curves may lead to a relative delay maxima somewhere between the two voltage extremes. However, all the other curves are concave and roughly mirror the gate dominant curve such that this maxima will be less than a few percent higher than at either the lowest or highest voltage, and therefore insignificant. Thus, timing analysis is only required at the two voltage extremes, and not at all the intermediate voltage values.

As demonstrated by the series dominant curve, the relative delay of four stacked devices rapidly increases at low voltage. Additional devices in series will lead to an even greater increase in relative

delay. As supply voltage increases, the drain-to-source voltage increases for the stacked devices during an output transition. For the stacked devices whose sources are not connected to V_{DD} or ground, their body-effect increases with supply voltage, such that it would be expected that the relative delay would be a maximum at high voltage. However, the sensitivity of device current and circuit delay to gate-to-source voltage exponentially increases as supply voltage goes down. So even though the magnitude change in gate-to-source voltage during an output transition scales with supply voltage, the exponential increase in sensitivity dominates such that stacked devices have maximum relative delay at the lowest voltage.

Thus, to improve the tracking of circuit delay over voltage, a general design guideline is to limit the number of stacked devices, which was four in the case of the prototype design. One exception to the rule is for circuits in non-critical paths, which can tolerate a widely varying relative delay. Another exception is for circuits whose alternative design would be significantly more expensive in area and/or power (e.g. memory address decoder), but the circuits must still be designed to meet timing constraints at low voltage.

3.3 Noise Margin Variation

Switching current reduces the circuits' noise margin, which must be evaluated to ensure proper processor operation. Reduction occurs through resistive (IR) and inductive (dI/dt) voltage drop on the power distribution network both on chip and through the package pins.

Figure 6 plots the relative IR and dI/dt voltage drop as a function of V_{DD}. It is interesting to note that the worst case condition occurs at high voltage, and not at low voltage, since the decrease in current and dI/dt more than offsets the reduced voltage swing. Thus, the design of the power grid (to evaluate R) and the package (to evaluate L) only needs to consider one operating voltage, which is maximum V_{DD}.

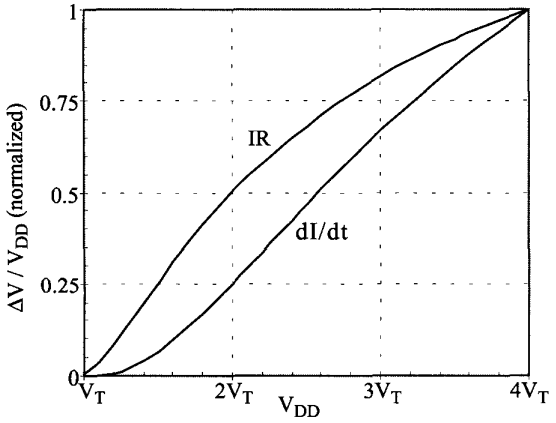

Figure 6. Normalized Noise Margin Variation.

4. DESIGN FOR VARYING VOLTAGE

One approach for designing a processor system that switches voltage dynamically is to halt processor operation during the switching transient. The drawback to this approach is that interrupt latency is increased and potentially useful processor cycles are discarded. However, static CMOS gates are quite tolerable to supply voltage slew, so there is no fundamental need to halt operation during the transient.

For the simple inverter in Figure 7, when V_{in} is high the output remains low irrespective of V_{DD}. However, when V_{in} is low, the output will track V_{DD} via the PMOS device, and can be modeled as a simple RC network. In a 0.6μm process, the RC time constant is a maximum of 5ns, at low voltage where it is largest. Thus, the inverter tracks quite well for a dV_{DD}/dt in excess of 200V/μs.

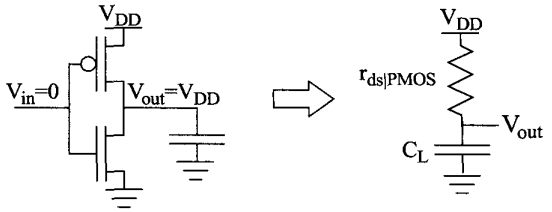

Figure 7. Static CMOS Inverter Equivalent RC.

Because all the logic high nodes will track V_{DD} very closely, the circuit delay will instantaneously adapt to the varying supply voltage. Since the processor clock is derived from a ring oscillator also powered by V_{DD}, its output frequency will dynamically adapt as well, as demonstrated in Figure 8.

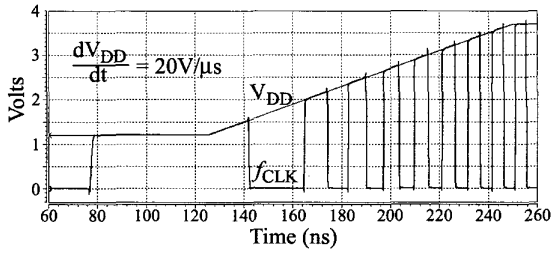

Figure 8. Ring Oscillator Adapting to Varying V_{DD}.

Thus, static CMOS is well-suited to continue operating during voltage transients. However, there are design constraints when using a design style other than static CMOS.

4.1 Dynamic Logic

Dynamic logic styles are often preferable over static CMOS as they are more efficient for implementing complex logic functions. They can be used with a varying supply voltage, as long as their failure modes are avoided by design. These two failure modes for a simple dynamic circuit are shown in Figure 9, and occur while the

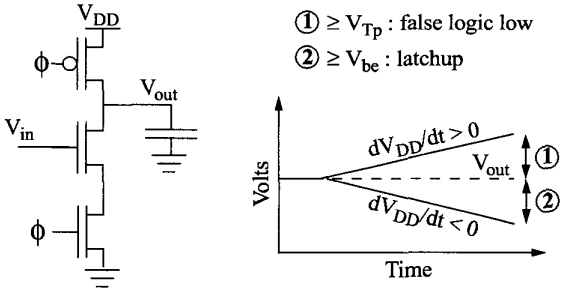

Figure 9. Failure Modes for Dynamic Logic.

circuit is in the evaluation state (ϕ=1) and Vin is low. In this state, V_{out} has been precharged high, and is undriven during the evaluation state.

If V_{DD} ramps down by more than a diode drop, V_{be}, by the end of the evaluation state, the drain-well diode will become forward biased. This current may be injected into the parasitic PNP of the PMOS device and induce latchup, which leads to catastrophic failure by short-circuiting V_{DD} to ground [4]. This condition occurs:

$$\frac{dV_{DD}}{dt} \leq \frac{-V_{BE}}{\tau_{CLK|AVE}/2} \quad \text{(EQ 3)}$$

where $\tau_{CLK|AVE}$ is the average clock period as V_{DD} varies from V_{out} to V_{out}-V_{be}. Since the clock period is longest at lowest voltage, this is evaluated as V_{DD} ranges from V_{MIN}+V_{be} to V_{MIN}, where V_{MIN}=V_T+100mV. For a 0.6µm process, the limit is 20V/µs, and will increase with improved process technology.

If V_{DD} ramps up by more than V_{Tp} by the end of the evaluation state, and V_{out} drives a PMOS device, a false logic low may be registered, giving a functional error. This condition occurs:

$$\frac{dV_{DD}}{dt} \geq \frac{V_{Tp}}{\tau_{CLK|AVE}/2} \quad \text{(EQ 4)}$$

evaluated for $\tau_{CLK|AVE}$ as V_{DD} varies from V_{MIN} to V_{MIN}+V_{Tp}. For a 0.6µm process, the limit is 24V/µs, and will increase with improved process technology because clock frequency improvement generally outpaces threshold voltage reduction.

These limits assume that the circuit is in the evaluation state for no longer than half the clock period. If the clock is gated, leaving the circuit in the evaluation state, these limits drop significantly. Hence, the clock should only be gated when the circuit is in the precharge state.

These limits may be increased to that of static CMOS logic using a small bleeder PMOS device, as shown in Figure 10. The left circuit can be used in logic styles without an output buffer (e.g. NP Domino), but has the penalty of static power dissipation. The right circuit is more preferable, as it eliminates static power dissipation, and only requires a single additional device in logic styles with an output buffer (e.g. Domino, CVSL). Since the bleeder device can be made quite small, there is insignificant degradation of performance due to the PMOS bleeder fighting the NMOS pull-down devices.

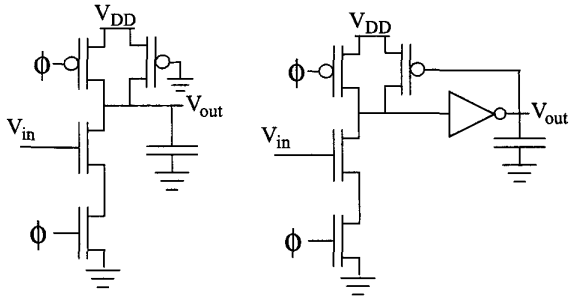

Figure 10. Bleeder Devices Improve Robustness.

4.2 Tri-State Busses

Tri-state busses that are not constantly driven for any given cycle suffer from the same two failure modes as seen in dynamic logic circuits due to their floating capacitance. The resulting dV_{DD}/dt can be much lower if the number of consecutive undriven cycles is unbounded. Tri-state busses can only be used if one of two design methods are followed.

The first method is to ensure by design that the bus will always be driven. This is done easily on a tri-state bus with only two drivers as the enable signal of one driver is simply inverted to create the enable signal for the other driver. This may become expensive to ensure by design for a large number of drivers, N, which requires routing N enable signals.

The second method is to use cross-coupled inverters. This is more preferable to just a bleeder PMOS as it will also maintain a low voltage on the floating bus. Otherwise, leakage current may drive the bus high while it is floating for an indefinite number of cycles. The size of this inverter can be quite small, even for large busses. For a 0.6µm process, an inverter can readily tolerate a dV_{DD}/dt in excess of 75V/µs with minimal impact on performance, and only a 10% increase in energy consumption.

4.3 Sense Amp Design

SRAM memory is an essential component of a processor. It is found in the processor's cache, translation look-aside buffer (TLB), and possibly in the register file(s), prefetch buffer, branch-target buffer, and write buffer. Since these memories all operate at the processor's clock speed, fast response time is critical, which demands the use of a sense-amp. The static and dynamic CMOS logic portions (e.g. address decoder, word-line driver, etc.) of the memory respond to a changing supply voltage similar to the ring oscillator, as desired. The sense-amp, however, must be carefully designed to scale in a similar fashion.

The basic SRAM cell is shown in Figure 11. Bit and $\overline{Bit}$ are precharged to the V_{DD} value at the end of the precharge cycle. Once the Word signal has been activated to sense the cell, Bit and $\overline{Bit}$ do not respond to a changing V_{DD}. If V_{DD} drops, m will drop, but since Word will also drop, there is no effect on Bit since the pass device is in the off state. When V_{DD} increases, m will increase, as will word, but will have no effect until V_{DD} increases by V_{Tn}, which is required to turn on the pass device.

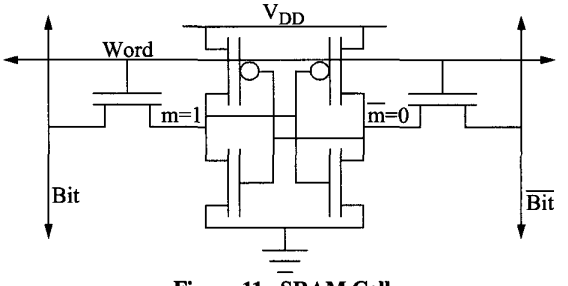

Figure 11. SRAM Cell.

This is most critical at low-voltage where the sensing time can be on the order of 20-40ns (for a 0.6µm process). During this time, a dV_{DD}/dt of 5V/µs translates to a voltage shift of 100-200mV, which can vary the clock period by up to +/-2x.

The basic sense-amp topology, shown in Figure 12, responds to the varying V_{DD} in a desirable manner. When V_{DD} increases, the cell current drive pulling down V_{bit} increases because the cell's internal voltage increases, and the trip point of the sense-amp shifts up. Likewise, when V_{DD} decreases, the cell current drive decreases, and the trip-point shifts down. The net effect is that the decrease/increase in response time of the sense-amp with dV_{DD}/dt is relatively similar to the decrease/increase in clock period. Thus, the basic sense-amp is very suitable for DVS.

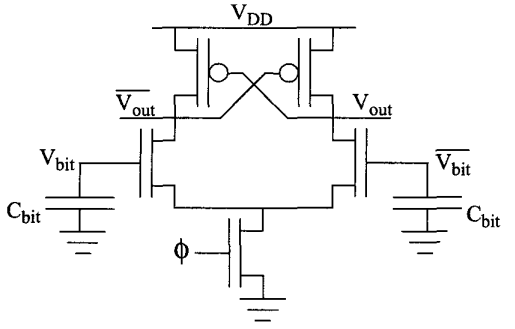

Figure 12. Basic Sense Amp Topology.

What must be avoided are more complex sense-amps whose aim is to improve response time and/or lower energy consumption for a fixed V_{DD}, but fail for varying V_{DD}. One example is a charge-transfer sense-amp [5].

4.4 Circuit Design Summary

As was demonstrated for the sense-amp, simpler circuit design ensures greater DVS compatibility. Many circuit design techniques developed for low power, such as the charge-transfer sense-amp and NMOS pass-gate logic, are not amenable to DVS.

In addition, a methodical design approach must ensure that no signal is ever floating for more than a half-cycle to prevent functional errors. But even with this approach, there are limits to dV_{DD}/dt, on the order of 20V/µs for a 0.6µm process. Higher dV_{DD}/dt can be tolerated for dynamic circuits with the use of bleeder and feedback devices, but is not recommended since the sense-amp is the limiting factor. While the basic sense-amp does scale relatively well with dV_{DD}/dt, there is some variation with dV_{DD}/dt above and beyond static CMOS logic, so a more practical limit is on the order of 5V/µs.

5. CONCLUSIONS

The DVS prototype processor system has successfully demonstrated significant improvement in energy efficiency. In addition DVS will continue to be a viable and valuable technique for future CMOS process technologies.

To achieve the full benefit of DVS, however, digital circuits must be designed to accommodate larger supply ripple in order to minimize the new contribution of transition power.

By restricting certain types of circuit design, the processor can robustly operate from maximum V_{DD} down to V_T. This dynamic range of operating voltages has minimal impact on design verification. Design verification is only required at maximum V_{DD} with the exception of timing verification, which is also required at minimum V_{DD}.

Simple static CMOS is very tolerant of slew on the voltage supply. Through careful circuit design, an entire processor system can be designed to operate robustly and continuously over dV_{DD}/dt in excess of 1V/µs. By sacrificing a small amount of energy efficiency in circuit design, much larger gains can be had at the system level.

6. ACKNOWLEDGMENTS

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