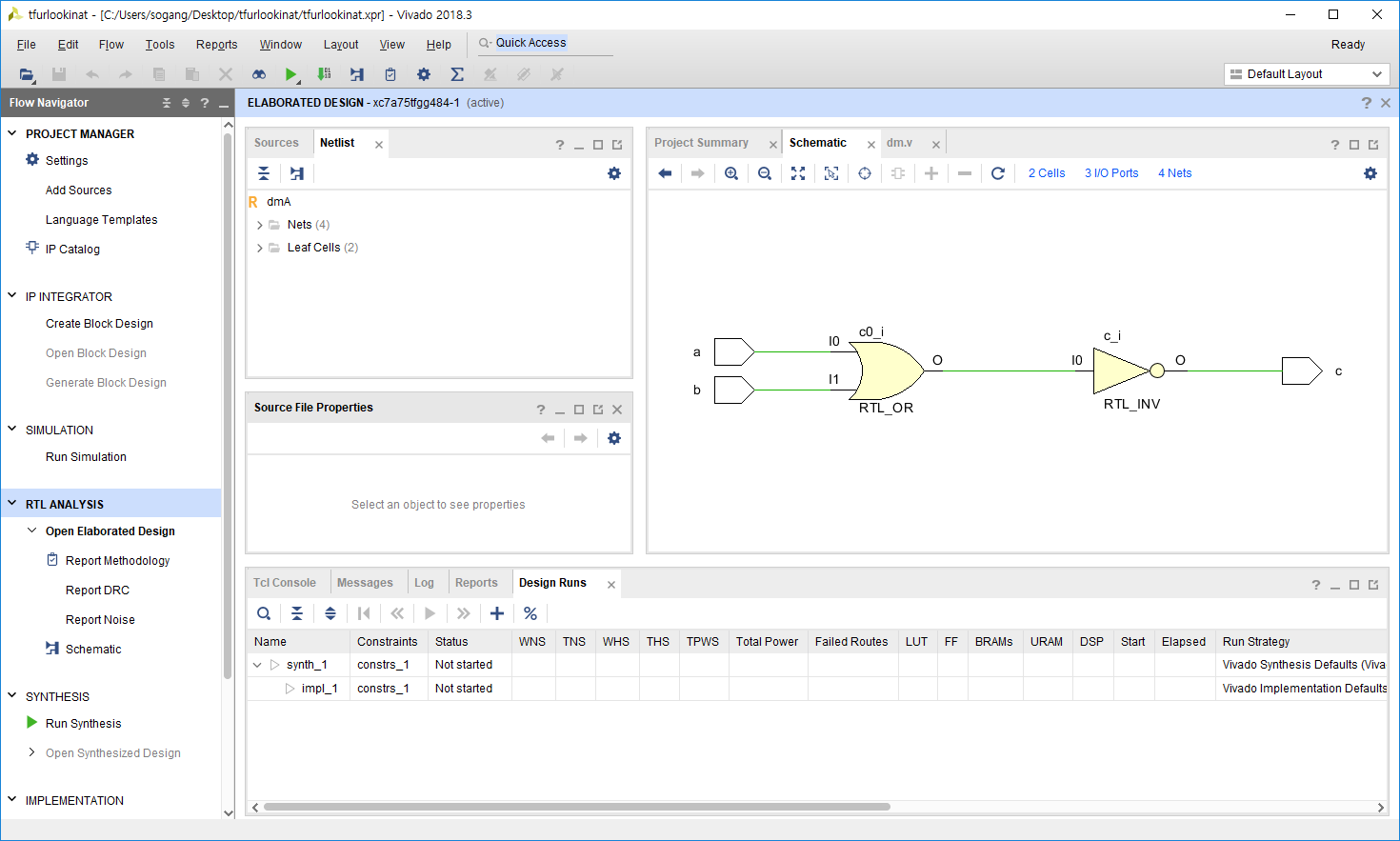
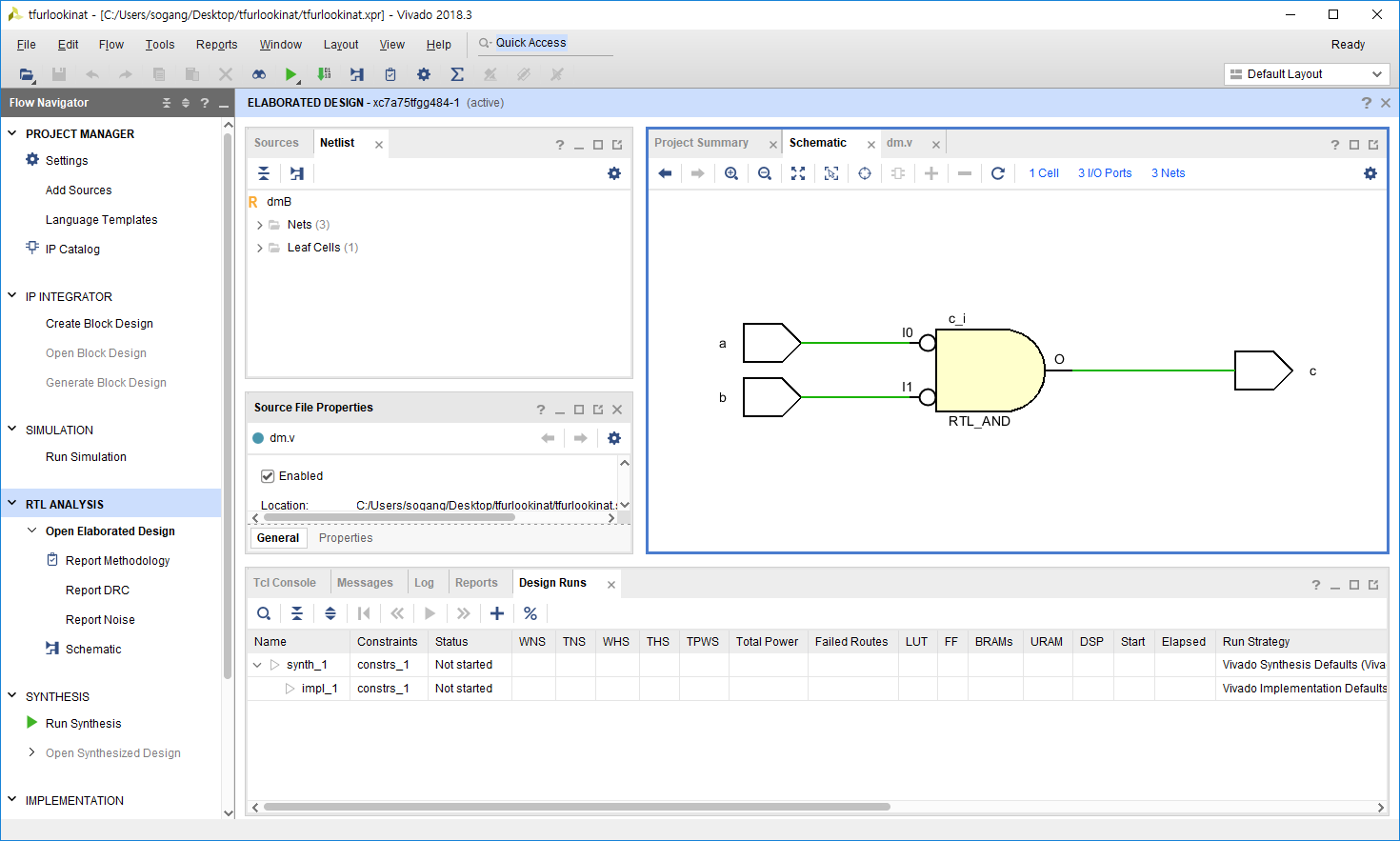
DM

A



B



`timescale 1ns / 1ps

module dmA(

input a, b,

output c

);

assign c = ~(a|b);

endmodule

module dmB(

input a, b,

output c

);

assign c = (~a)&(~b);

endmodule

`timescale 1ns / 1ps

module sim;

reg [1:0] in;

wire outA, outB;

dmA testA(in[0], in[1], outA);

dmB testB(in[0], in[1], outB);

initial in = 2'b00;

always in = #200 in + 1;

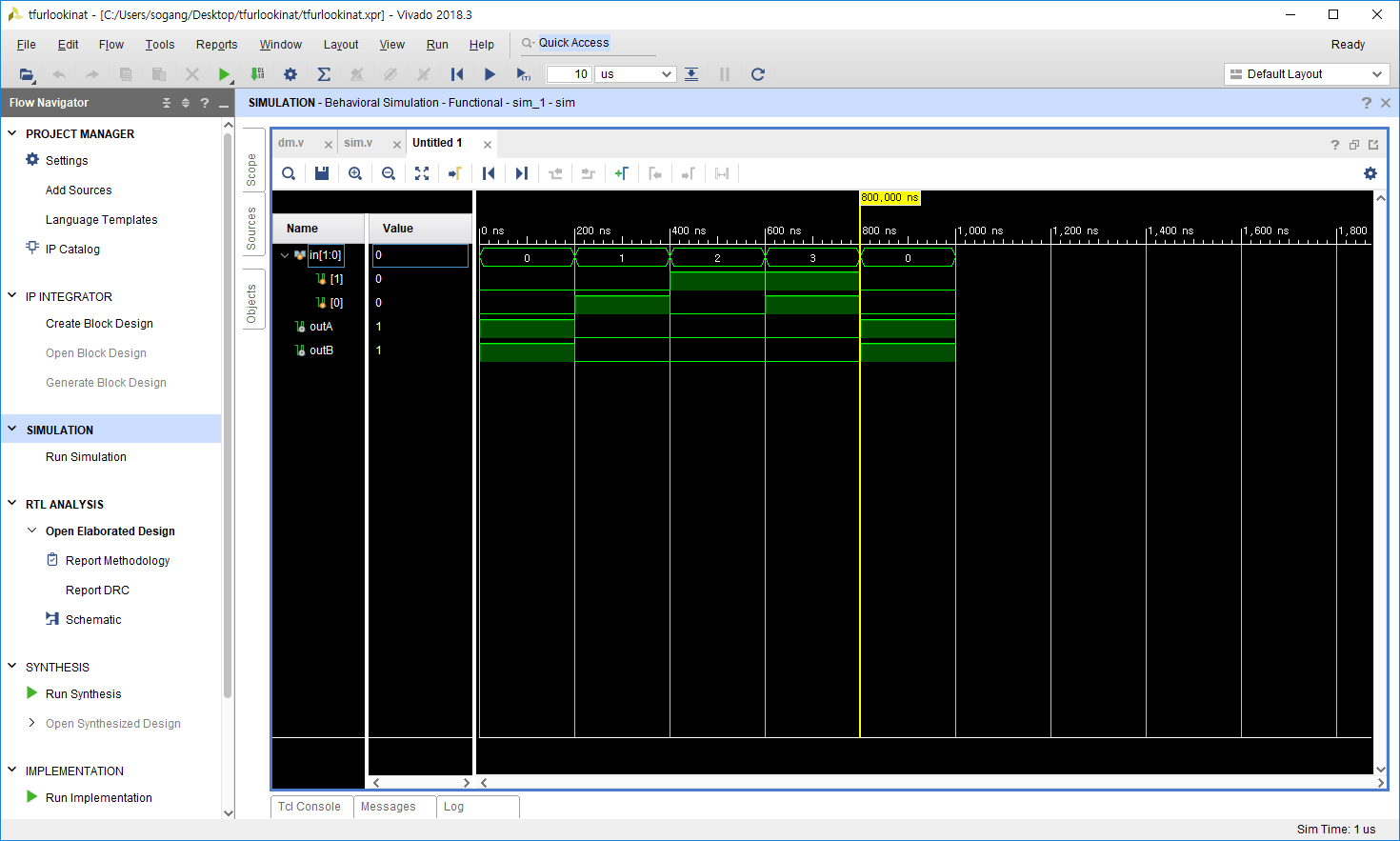
initial begin

#20000

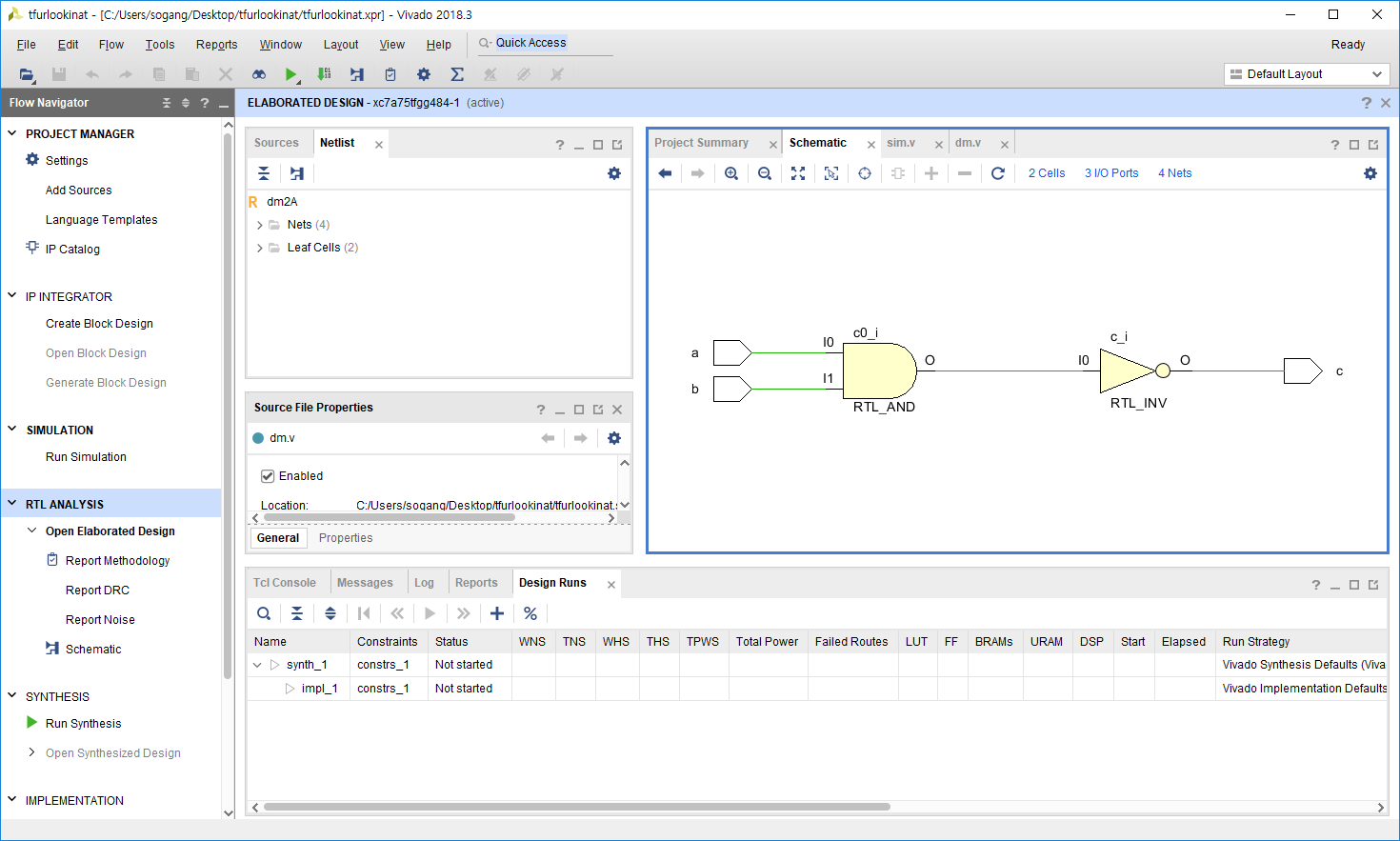
$finish;

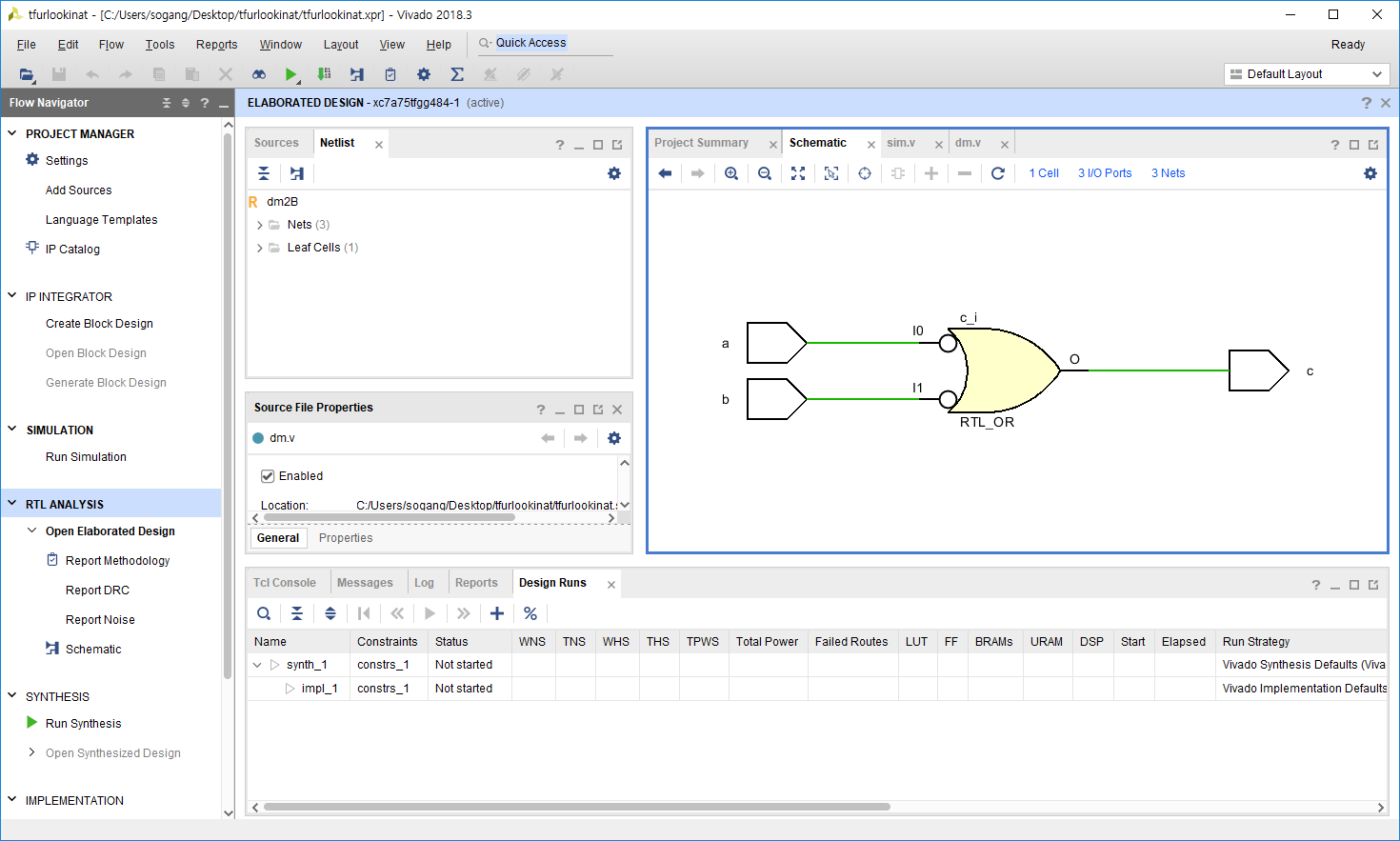
end

endmodule



DM2





module dm2A(

input a, b,

output c

);

assign c = ~(a&b);

endmodule

module dm2B(

input a, b,

output c

);

assign c = (~a)|(~b);

endmodule

`timescale 1ns / 1ps

module sim;

reg [1:0] in;

wire outA, outB;

//dm1A testA(in[0], in[1], outA);

//dm1B testB(in[0], in[1], outB);

dm2A testA(in[0], in[1], outA);

dm2B testB(in[0], in[1], outB);

initial in = 2'b00;

always in = #200 in + 1;

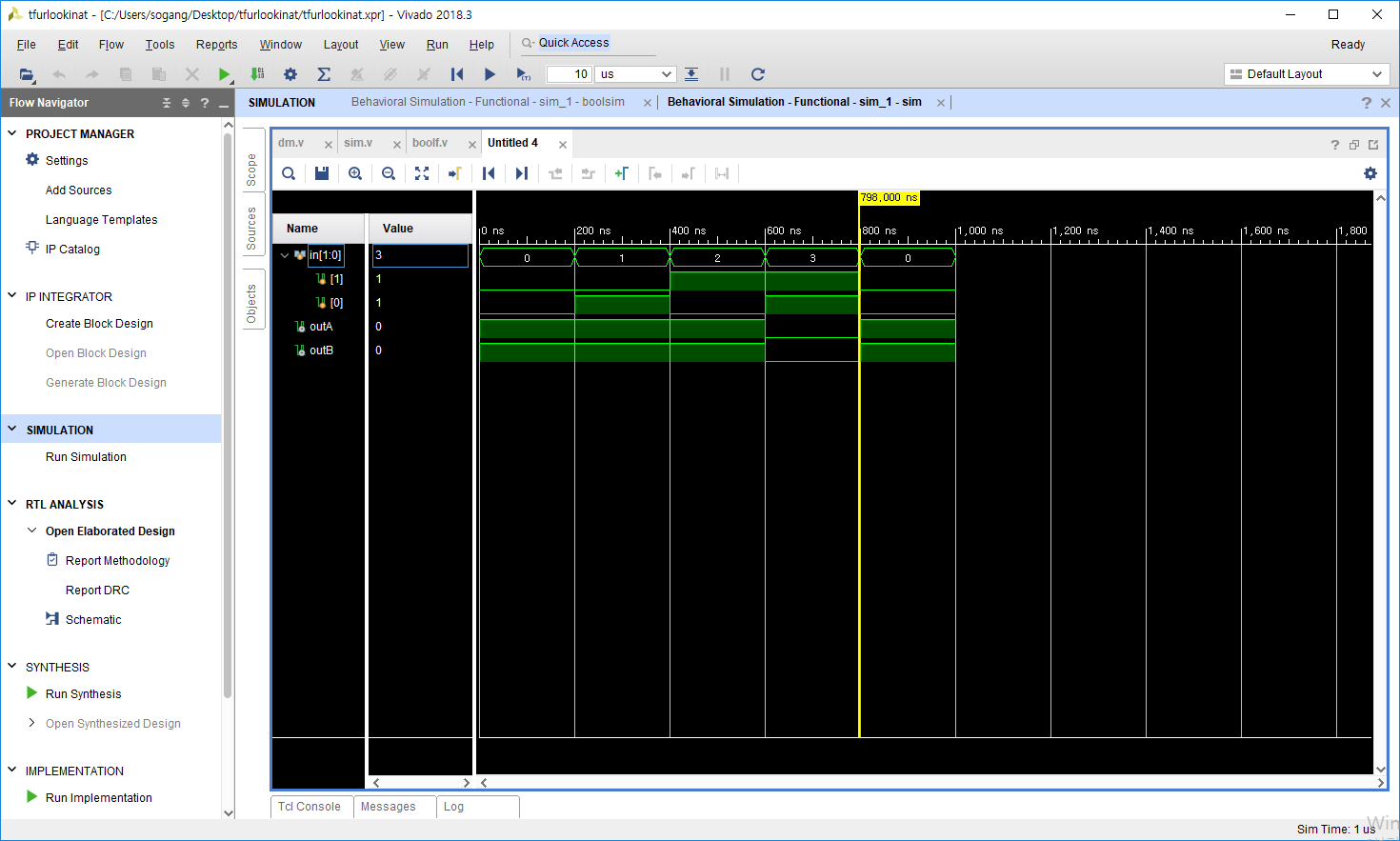
initial begin

#20000

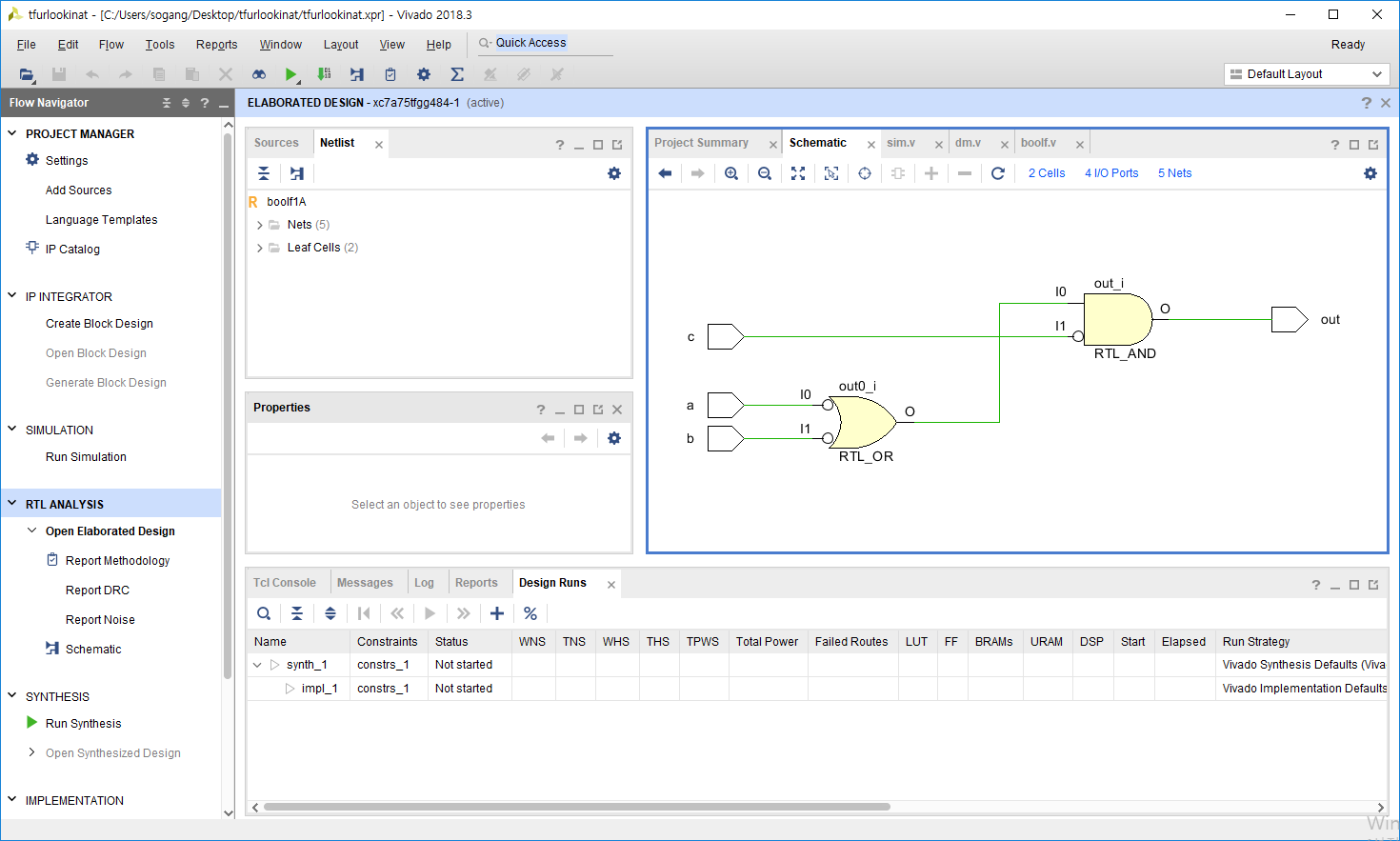
$finish;

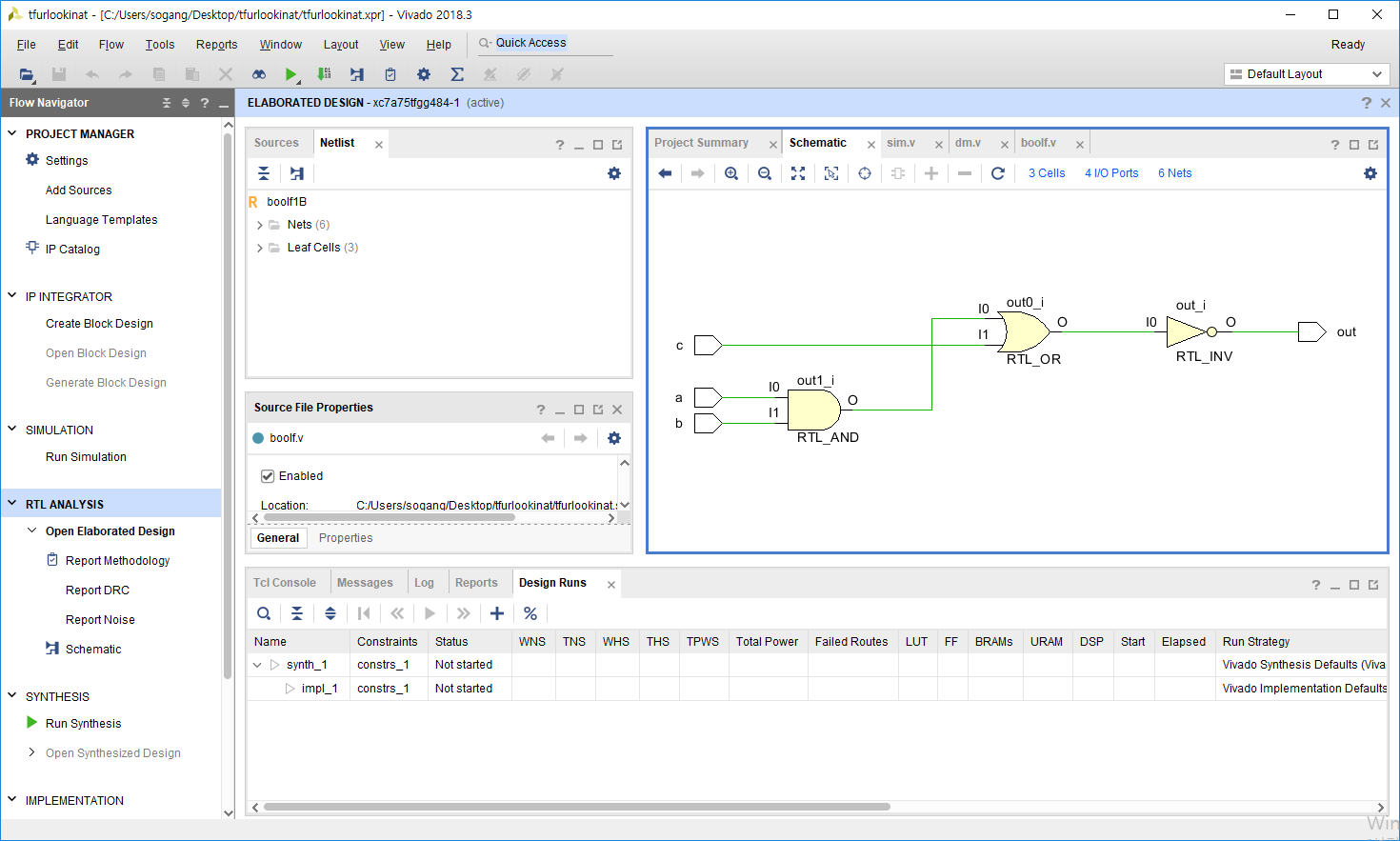
end

endmodule



Bool function





`timescale 1ns / 1ps

module boolf1A(

input a, b, c,

output out

);

assign out = (~a|~b)&~c;

endmodule

module boolf1B(

input a, b, c,

output out

);

assign out = ~((a&b)|c);

endmodule

module boolsim;

reg [2:0] in;

wire outA, outB;

boolf1A testA(in[0], in[1], in[2], outA);

boolf1B testB(in[0], in[1], in[2], outB);

initial in = 3'b000;

always in = #200 in + 1;

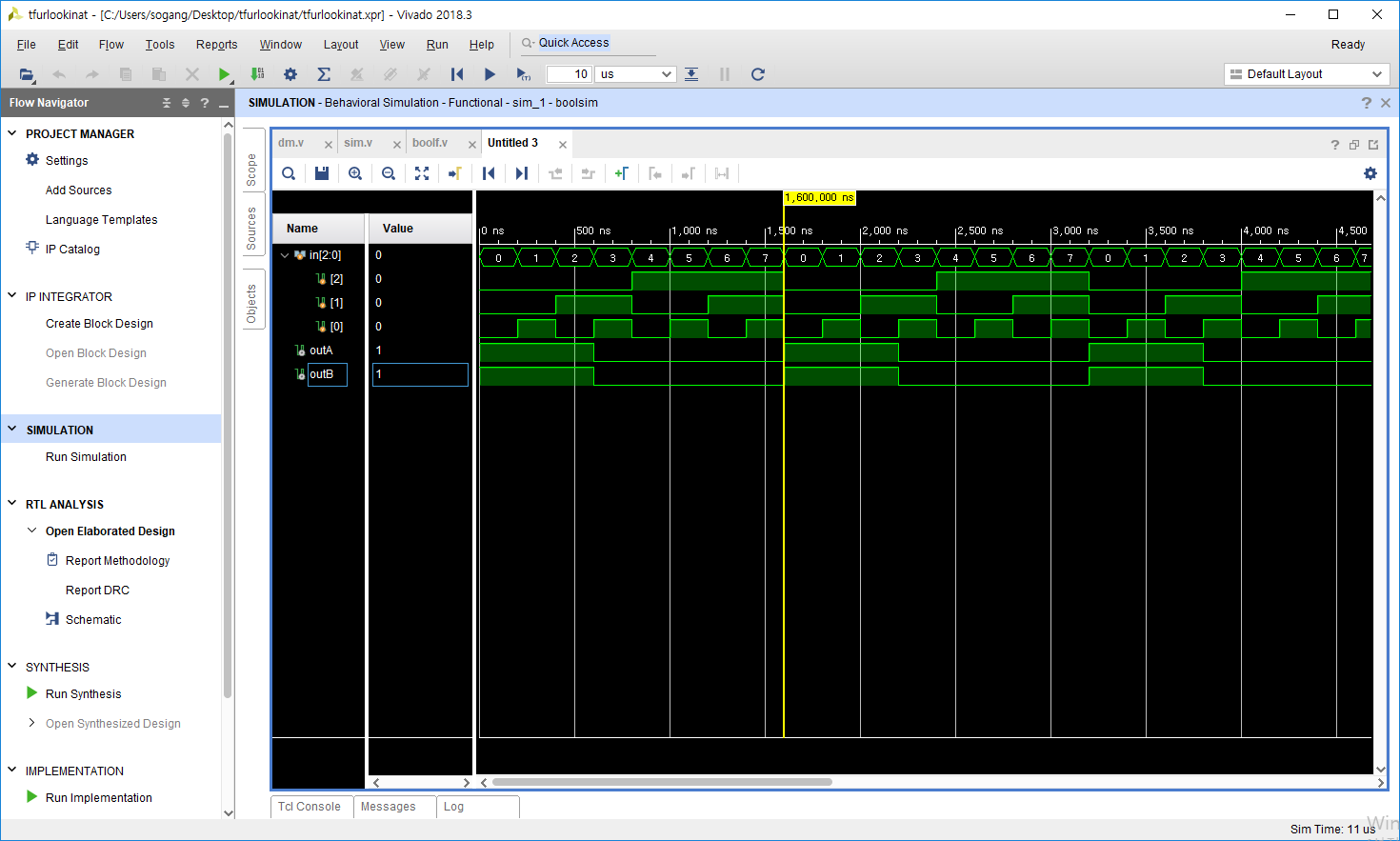
initial begin

#20000

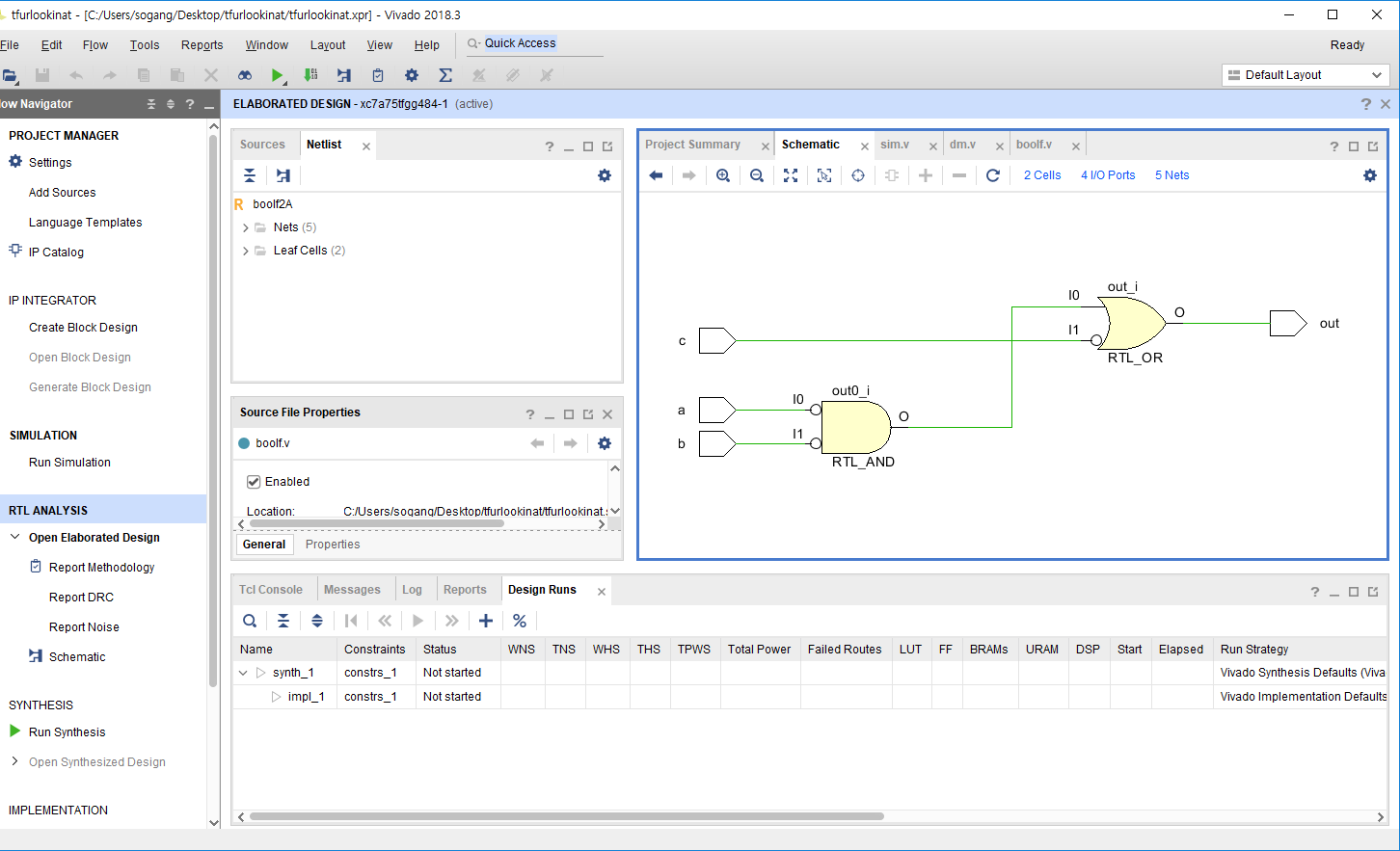
$finish;

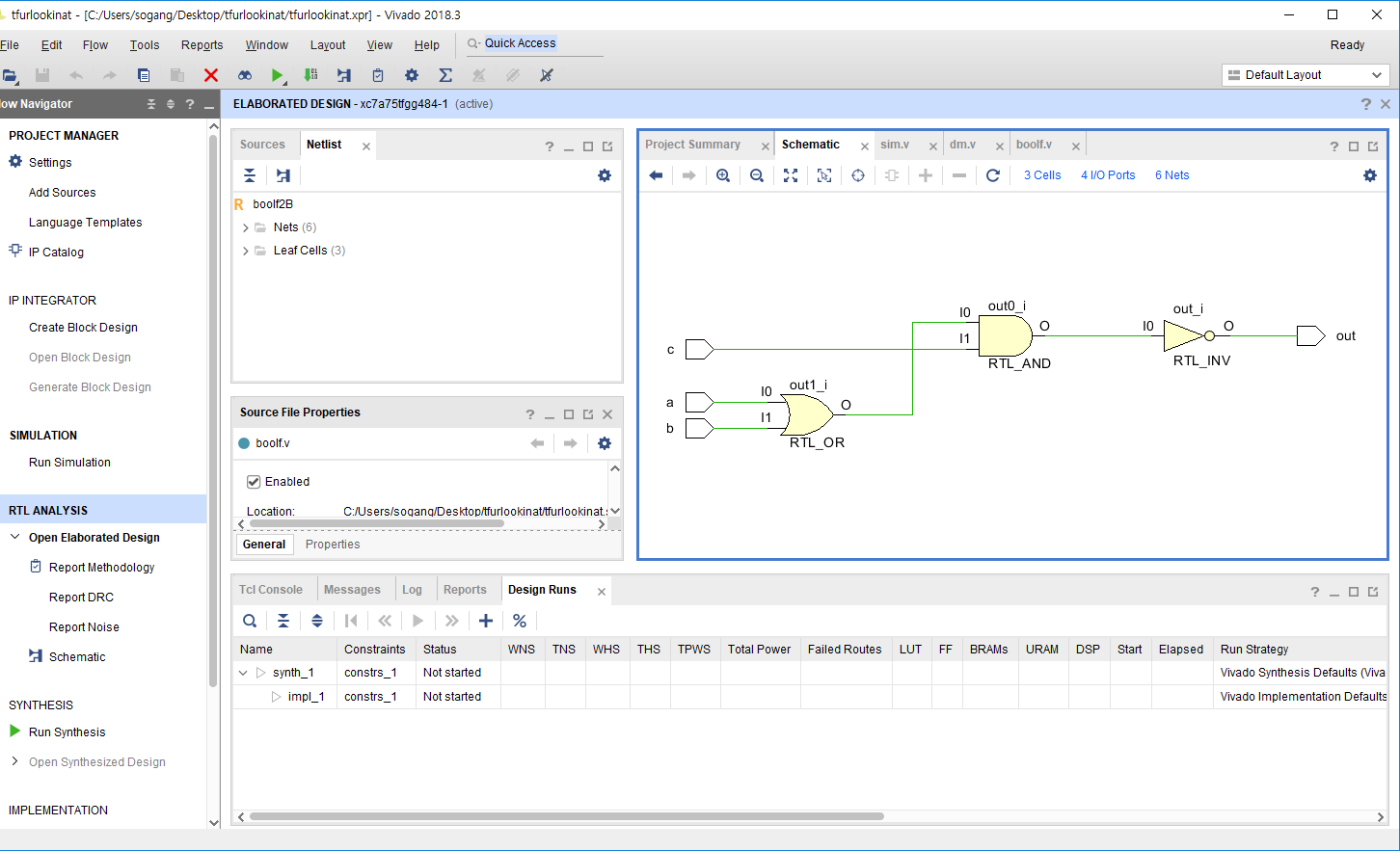
end

endmodule



Bf2





module boolf2A(

input a, b, c,

output out

);

assign out = (~a&~b)|~c;

endmodule

module boolf2B(

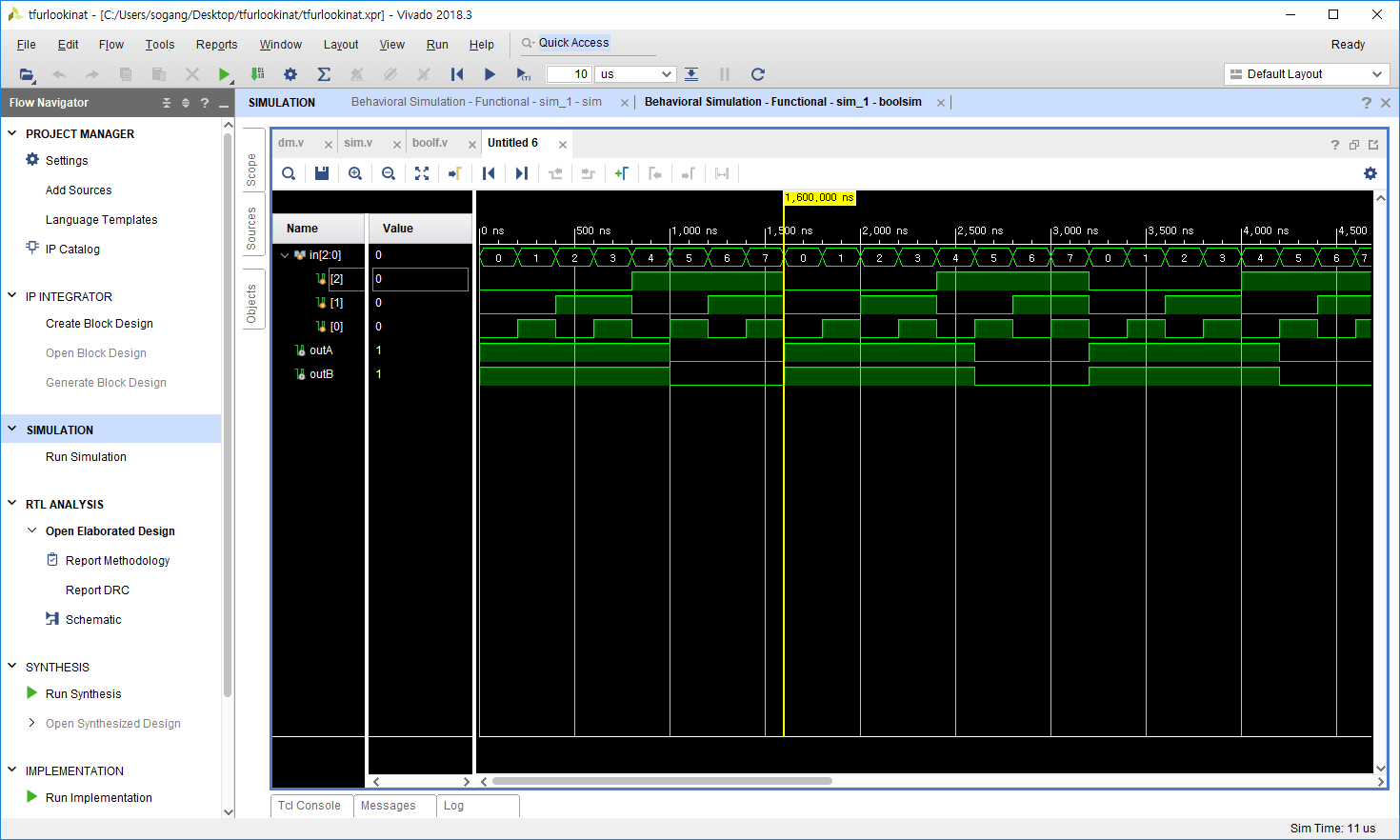
input a, b, c,

output out

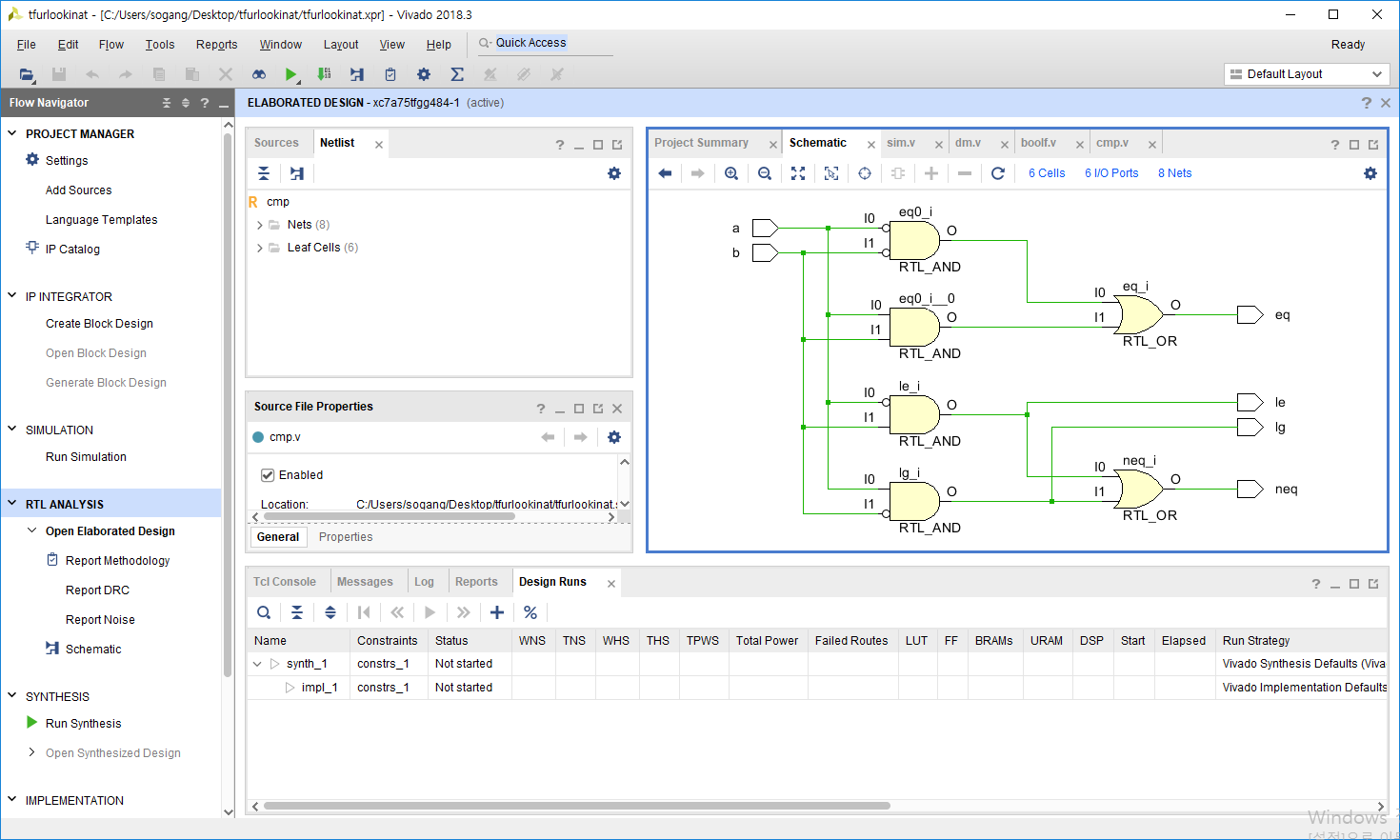
);

assign out = ~((a|b)&c);

endmodule



1bit comparator



`timescale 1ns / 1ps

module cmp(

input a, b,

output eq, neq, lg, le

);

assign eq = (~a&~b)|(a&b);

assign neq = (~a&b)|(a&~b);

assign lg = a&~b;

assign le = ~a&b;

endmodule

module cmpsim;

reg [1:0] in;

wire eq, neq, lg, le;

cmp testA(in[0], in[1], eq, neq, lg, le);

initial in = 2'b00;

always in = #200 in + 1;

initial begin

#20000

$finish;

end

endmodule

