NC State University
Department of Electrical and Computer Engineering

ECE 310 – Fall 2025

Lab 2

Summary

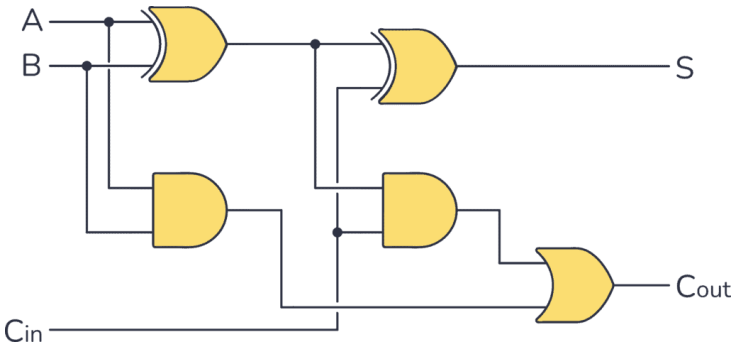
In this lab, you will create a **gate-level/structural** model for a 4-bit Ripple-Carry Adder (RCA).

Deliverables

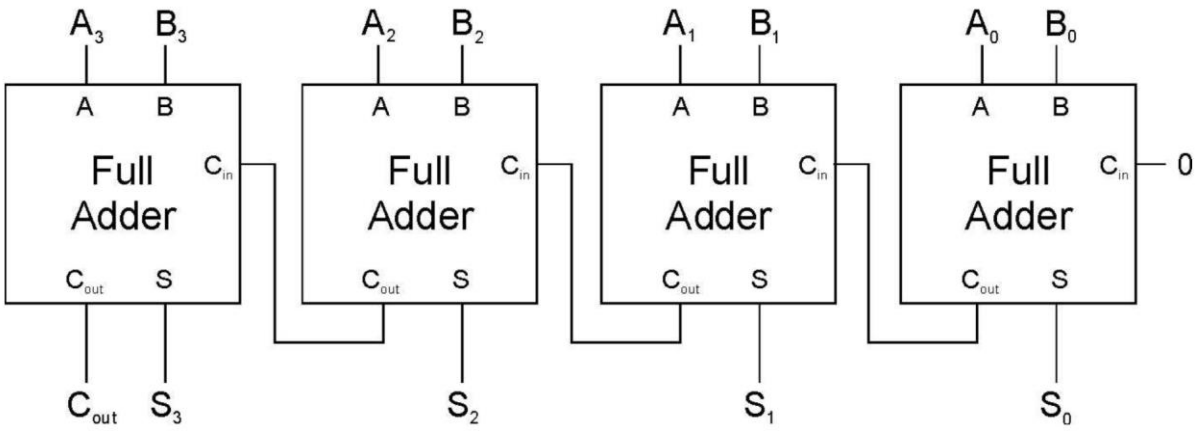
1. Code for model and testbench (.v file(s)).
2. Clear screenshot of simulation waveform(s) of the 4-bit adder with at least 4 test vectors with some representative values (not trivial values). Justify why you used these values.
3. Short report describing the theory of operation, design/diagrams, snippets of code as needed, results, and a discussion.

Instructions

1. Create a new project in Vivado named **full_adder_struct**.
2. Implement a full adder at the gate-level using the following diagram. A full adder has 3 inputs (A, B, and Cin) and 2 outputs (Cout and S). The implementation below may be different than usual, so pay attention to the gates and connections.



3. Once a full-adder is implemented, use it to create a 4-bit Ripple Carry Adder (declare a new module named **rca_4bit** to implement this). Declare 2 4-bit inputs names A and B and a 4-bit output named S, as well as a 1-bit output named Cout for this module.



4. Create a testbench named **rca_4bit_tb** and test your model with some representative values as inputs. Justify why you used these values in your submission.
5. Submit your code for the model for the full adder and 4-bit ripple carry adder and testbench (as .v file(s)), a clear screenshot of your simulation results showing all test values, and a justification for why you used those test values.

Grading Breakdown:

- Design and implementation of full adder at the gate level – 20 pts
- Design and implementation of RCA at the gate level – 30 pts
- Testbench for RCA – 15 pts
- Justification for at least 4 input test vectors used – 10 pts
- Lab report with as much information present as possible – 20 pts
- Upload of .v model file with testbench (could also be 2 separate files) to Moodle and .pdf report to Gradescope – 5 pts