NC State University
Department of Electrical and Computer Engineering

ECE 310 – Fall 2025

Project 1

Due: Wednesday September 17 by EOD

Summary

In this project, you will be designing and implementing an 8×8 Wallace unsigned multiplier. No other implementation will be accepted.

Deliverables

1. Code for model and testbench.
2. Screenshot of simulation waveforms with at least 4 pairs of non-trivial input vectors and discussion comparing to expected results.
3. A detailed formal report. If written using LaTeX, up to 10 additional points will be added to the score.

Instructions

1. A Wallace tree multiplier (Wallace multiplier) is a type of fast multiplier that reduces the number of evaluation layers compared to a regular shift-and-add multiplier at a cost of higher gate count and number of wires. For more information: https://en.wikipedia.org/wiki/Wallace_tree . Do not implement a shift-and-add, Booth, etc binary multiplier.

2. Create a new project in Vivado named **Project1**.

3. Design a Wallace multiplier that multiplies an 8-bit unsigned number (**input a**) with another 8-bit unsigned number (**input b**) to produce a 16-bit number (**output prod**) using gate-level modeling. The design will use Full-Adders and Half-Adders (as needed) that are described at the gate-level. The rest of the design must also be at gate-level/structural (such as partial products made with AND gates, etc). If an addition operation requires only 2 bits to be added, use a Half-Adder instead of a Full-Adder. All gates/units have no propagation delay that have to be accounted for in this project.

4. Show the entire design (hand-drawn is acceptable) with labels for each partial product and adders for each stage of the multiplier (this will take an entire page at least, leave plenty of space between the partial products/units as additional labels/rework may be needed). Perform a count of the number of AND gates, Full-Adders, and Half-Adders used (and any other units) and include this in your final report. Submit this as your design work for the design submission by Wednesday September 3 in Gradescope.

5. Implement the design using Verilog and show clear simulation results using at least 4 pairs of non-trivial input vectors. Discuss the results of your simulation with expected results.

Points Breakdown:

15 pts: Clear diagram of design with all units labeled and any necessary discussion are present. Blackbox drawings for sub-units are acceptable as long as they are labeled and individually detailed at the gate-level in another part of the design diagram.

15 pts: Instantiation and connections of partial products (AND's)

40 pts: Instantiation and connections of Full- and Half-Adders

10 pts: Instantiation and connections of product outputs

15 pts: A .pdf report detailing the design structure and approach, test vectors (minimum 4) and reasoning for choices made, any specific description of code as necessary, expected results vs timing diagram and discussion, anything else relevant to this project. The more formal the report, the more points will be awarded. If the report is written using LaTeX, up to 10 additional points will be awarded, depending on the use of LaTeX elements.

5 pts: Correct upload of .v files to Moodle and .pdf to Gradescope.