NC State University
Department of Electrical and Computer Engineering

ECE 310 – Fall 2025

Lab 4

Summary

In this lab, you will create an 8-bit shift register with various shifting capabilities mostly designed using dataflow modeling (significant number of points will be lost for not designing according to instructions).

Deliverables

1. Code for model and testbench as separate .v files uploaded to Moodle.
2. Report describing the theory of operation, design/diagrams, snippets of code as needed, results, and a discussion. Include a screenshot of simulation waveforms for the design with some representative values (not trivial values) that exhaustively tests all possible output operations. Justify why you used these values as inputs. Upload the report to Gradescope.
3. Extra Credit – up to 10 additional points will be added for typesetting your report in LaTeX, depending on usage of LaTeX elements (e.g. figures, tables, sections, etc).

Instructions

1. Create a new project in Vivado named **shifter_8bit** with a module of the same name.

2. Design a shifter using dataflow modeling with various capabilities to shift an 8-bit input value (left and right, by 1 and 2 bits), rotate (left and right, by 1 bit), and hold the value. If any hardware used requires the use of more input lines/options, load 0's (this translates to unused inputs on a mux loading 0's). The rotation operation is equivalent to a circular shift, where the rotate left/right operation shifts all bits left/right and the MSB/LSB is shifted into the LSB/MSB location, respectively. See https://en.wikipedia.org/wiki/Circular_shift for more information.

3. The 8-bit result of the operation will be stored in an 8-bit register designed using 8 instances of the DFF model provided in class slides (using behavioral modeling) with some modifications as outlined in step 4. This DFF model is the only part of the lab allowed to be coded at the behavioral level. Use an appropriately-sized multiplexer to select between the operations above to pass data to the register, with the following control values and operations:
   0 – shift left by 1 bit
   1 – shift left by 2 bits
   2 – logical shift right by 1 bit
   3 – logical shift right by 2 bits
   4 – rotate left by 1 bit
   5 – rotate right by 1 bit
   6 – hold old value (no change in output)
   Other values – load 0's.

4. An additional control signal (named **capture**) will be used to store the result in the 8-bit register, as follows: **capture** = 0, the new value will be loaded, and **capture** = 1, the old value is not changed (**capture** is active-low). You may need to use additional units/gates to implement this capability in another module based on the DFF model.
5. Summary of port connections:

Signal	Direction	Description
clock	input	Free-running clock (useful in testbench)
d_in	input	8-bit unsigned input to register
d_out	output	8-bit unsigned output of register
op	input	***n***-bit operation selector based on table in step 3 (justify value of *n* in report)
capture	input	1-bit capture indicator

6. Submit a report, similar to previous labs, containing the information in the Deliverables section above. A design diagram with descriptions is required to be submitted with the lab report.

Grading Breakdown:

- Design and implementation of the shifter module including any additional required modules to achieve desired operation – 50 pts
- Testbench implementation – 10 pts
- Use of separate files for model and testbench – 5 pts
- Justification for input test vectors used and output waveform correctness – 10 pts
- Lab report with as much information present as possible, see Deliverables section. A diagram and descriptions for the diagram is required, as well as justification for size(s) of mux(es). – 20 pts
- Upload of .v model file and testbench (2 separate files) to Moodle and a .pdf report to Gradescope – 5 pts