

ECE 310 – Fall 2025

Lab 1

Summary


In this lab, you will run a “Hello World!”-type program to show your Vivado installation works correctly. If you do not install Vivado on your own machine, you should be able to accomplish this lab using a remote connection to the Linux servers (see instructions in Moodle on connection information.)

Deliverables

1. Screenshot of message containing your name (.jpg or .png file format only).

Instructions

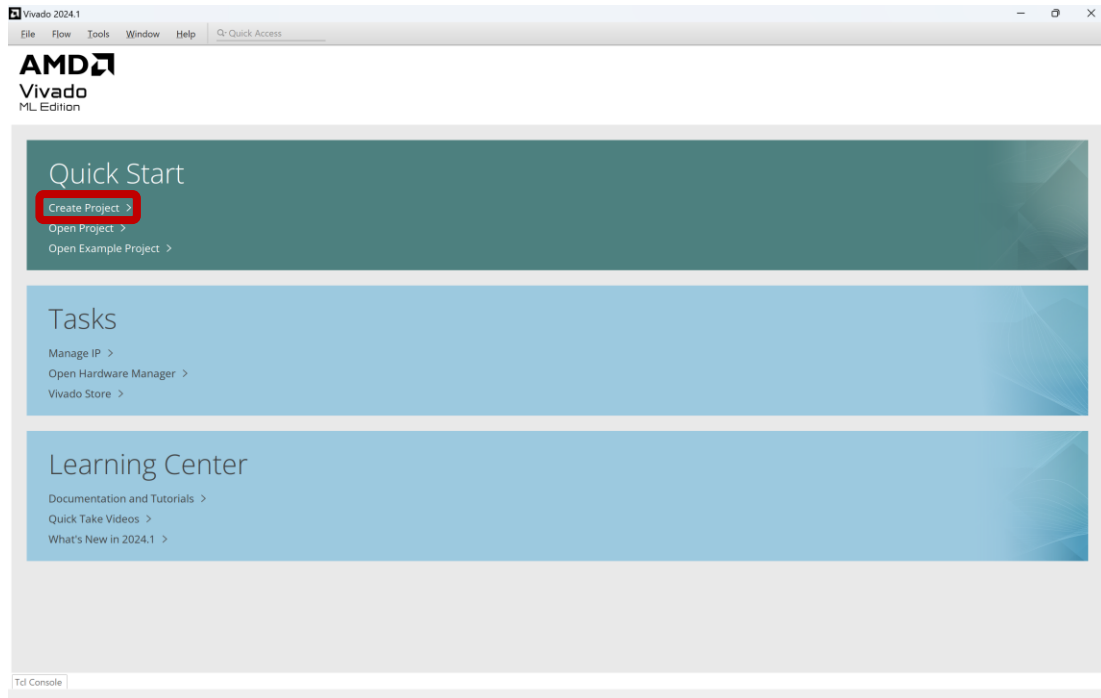
0. Create a projects folder where all code and other related files for the labs will be stored. Vivado does not work well with deep directory structures or spaces in file names, so create a folder on the C:\ drive and do not include spaces in the name (I used *ECE310Fall2025-Projects*)

 ECE310Fall2025-Projects

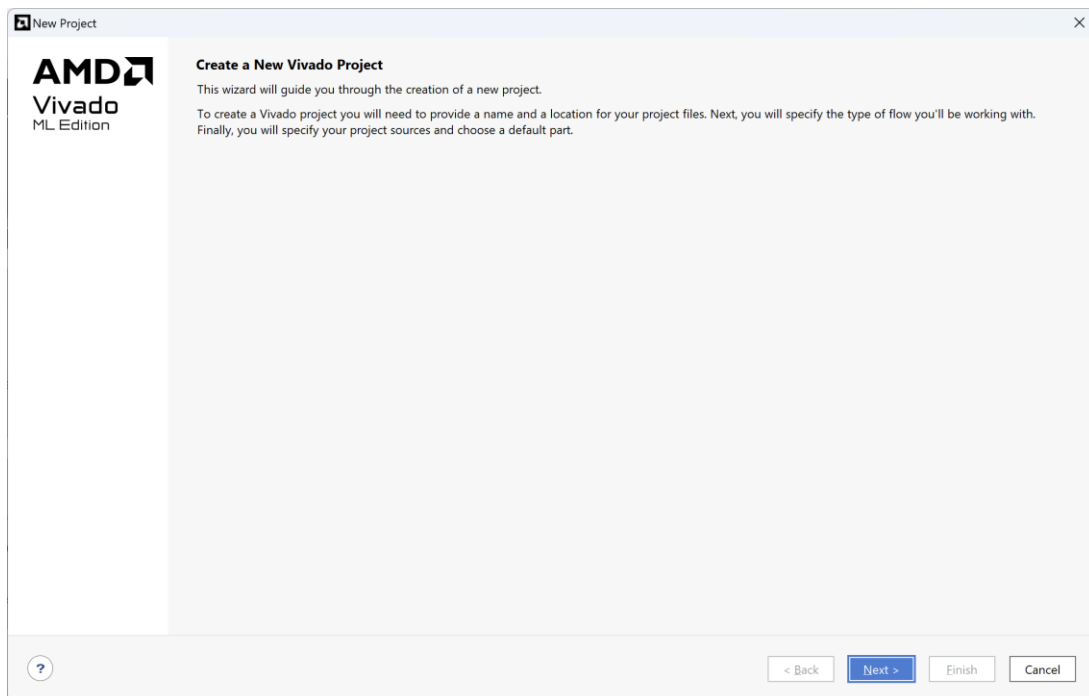
1. Double-click on the Vivado 2024.1 (or any version of Vivado you installed) shortcut that should have been added to your Desktop as part of installation. There should be another 3 shortcuts that were added during installation – you can delete them as we will not be using them (DocNav, Vitis HLS, and Vitis Model Composer). **Vivado is slow to open – wait at least 30 seconds** so that you do not have 2 instances start up and delaying everything even further.



2. A window similar to the one below should open. This is the starting point for any project in Vivado. Click on “Create Project”.



3. You should see a window with a description of next steps. Click “Next”.



4. Enter project information:
Name: *Lab1* (no spaces)
Location: your project directory from step 0.
There should be a check mark already on “*Create project subdirectory*”, but double-check that this is the case.

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at: C:/ECE310Fall2024-Projects/Lab1

5. Project type is *RTL Project*. Click “Next”.

New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

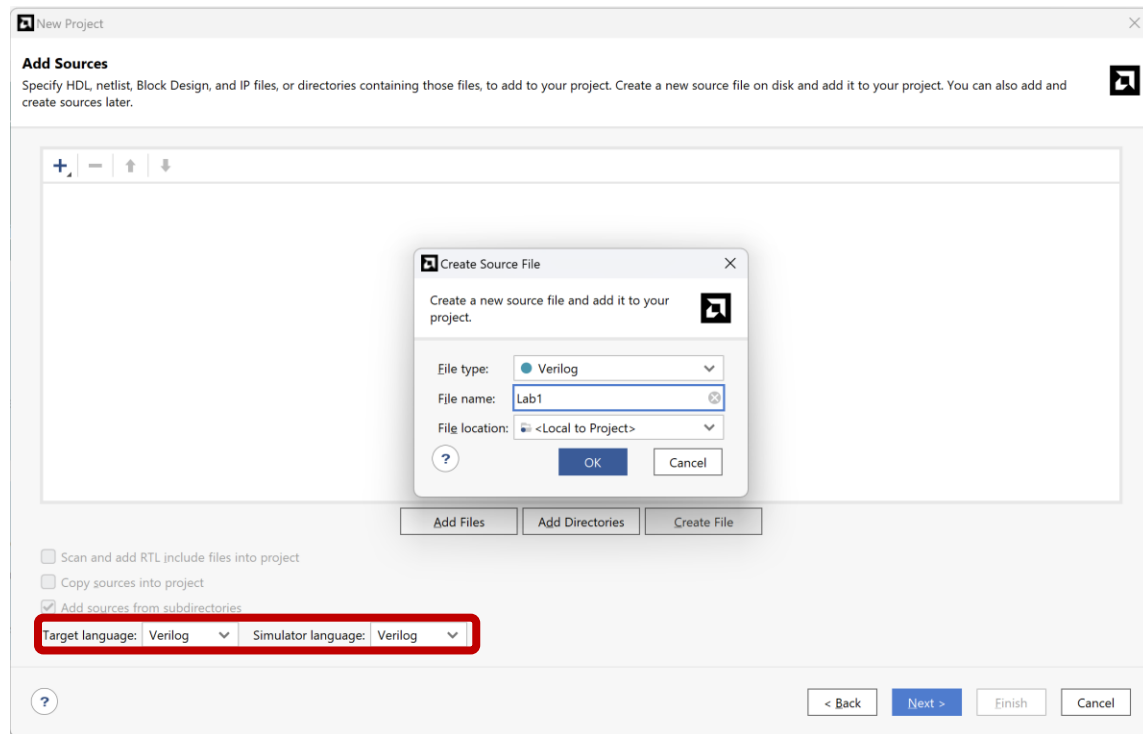
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

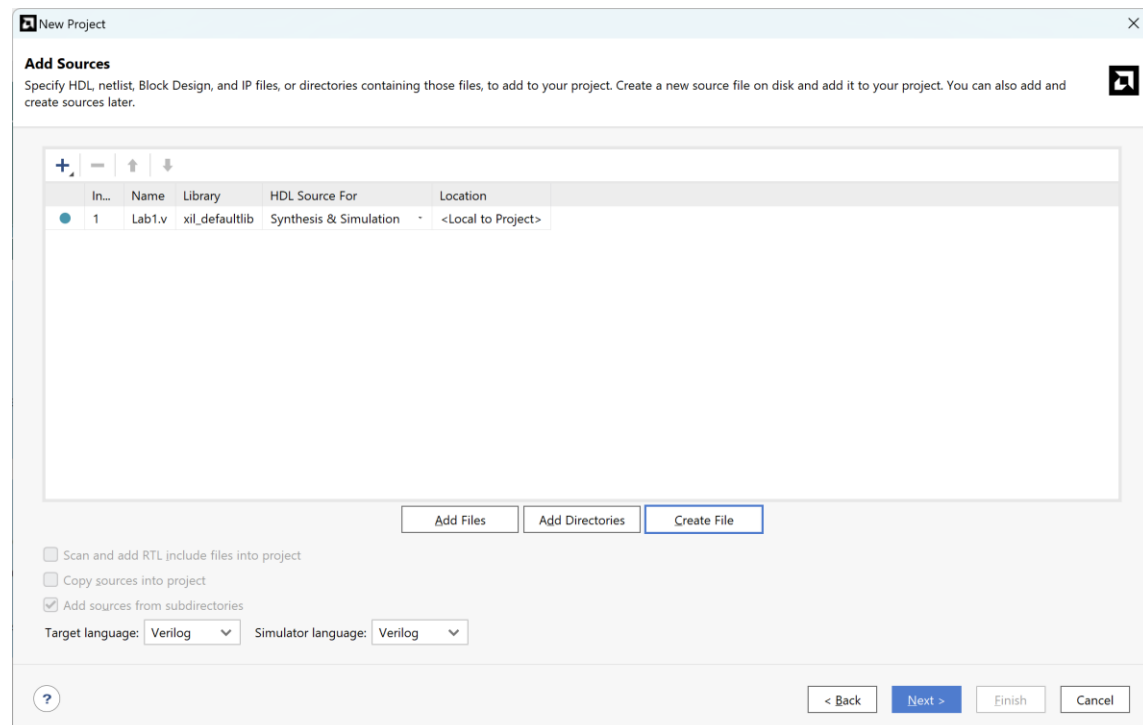
☐ **Imported Project**
Create a Vivado project from a Synplify Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

6. Make sure the “Target language” and “Simulator language” are both set to *Verilog*. Add source files – click on “*Create File*” and in the new window enter *Lab1* for the file name and click “*OK*”. The file type should be already set to Verilog, but double check before closing the window.



7. You should see a new file named “*Lab1.v*” added to your project. Click “*Next*”.



8. Add any constraints files. This only happens for projects where you need to go through Synthesis, but for this project, there is no constraints file. Click “*Next*”.

New Project

Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

☐ Copy constraints files into project

9. You will not use a FPGA for this class, but Vivado still requires you to enter board information. We will choose the Basys3 board and select the following values from the drop-down menus, then select the middle option and click “Next”.

New Project

Default Part
Choose a default AMD part or board for your project.

Parts | Boards

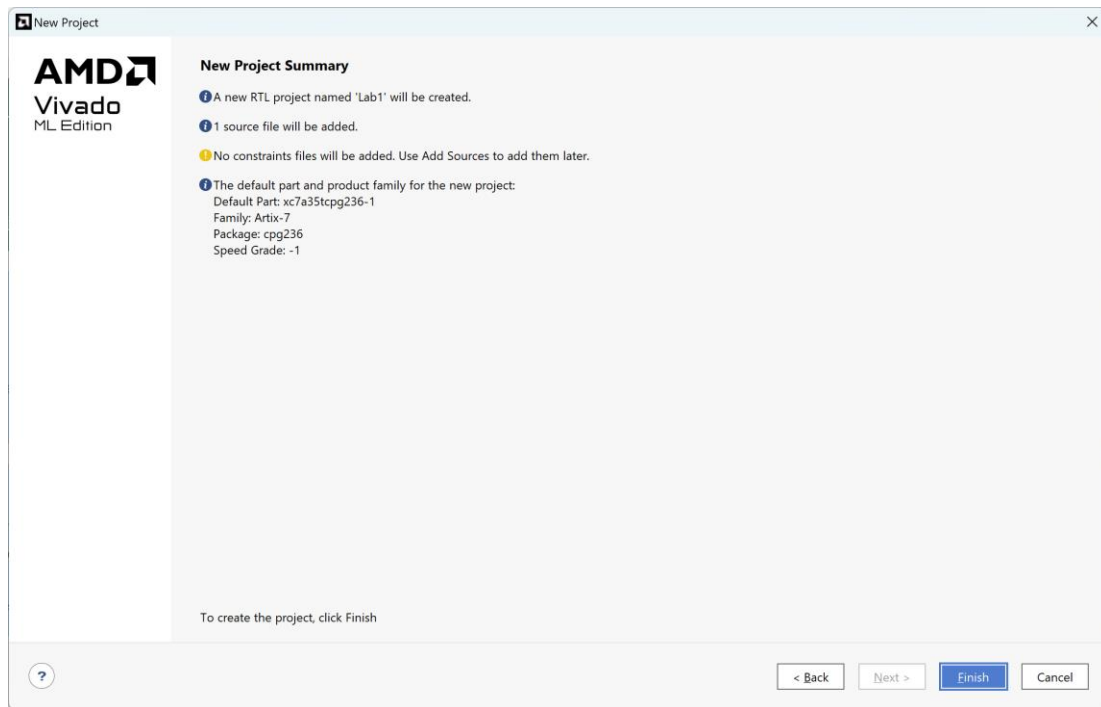
[Reset All Filters](#)

Category: All Package: cpg236 Temperature: All Remaining
Family: Artix-7 Speed: -1 Static power: All Remaining

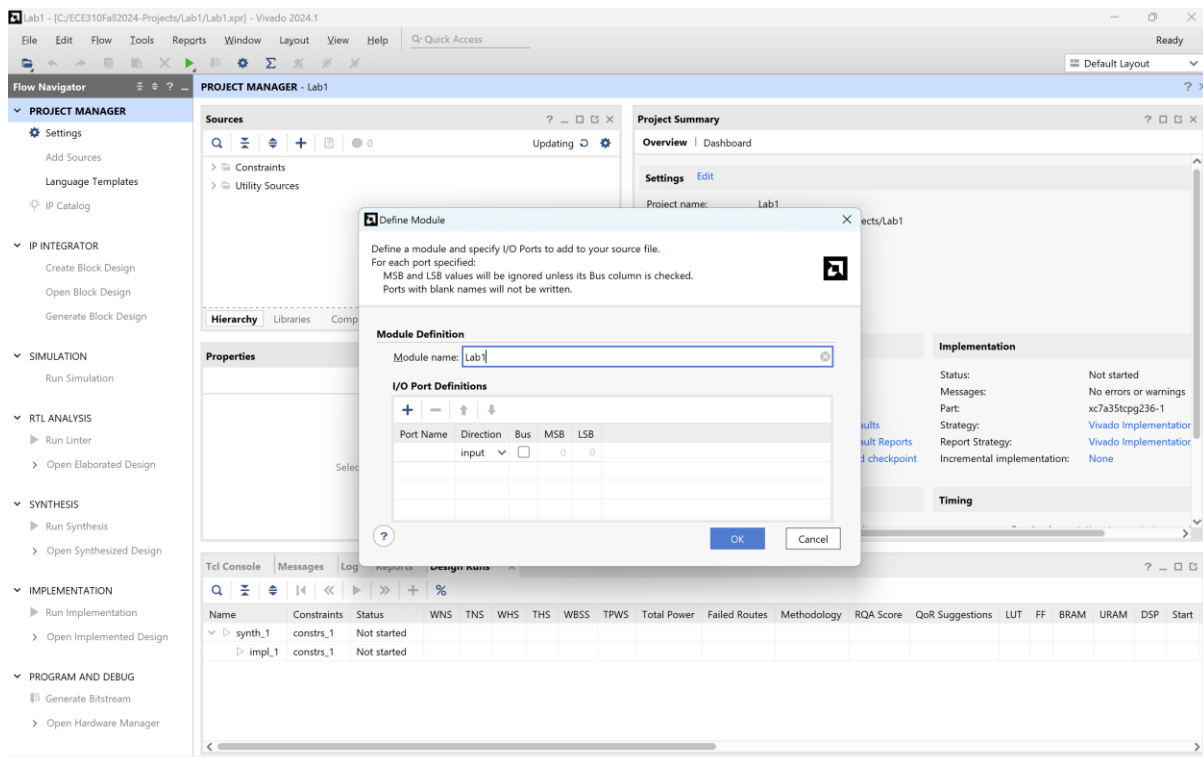
Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	BUFGs	Gb Transceivers	GTPE2 Transceivers
xc7a15tcbg236-1	236	106	10400	20800	25	0	45	32	2	2
xc7a35tcbg236-1	236	106	20800	41600	50	0	90	32	2	2
xc7a50tcbg236-1	236	106	32600	65200	75	0	120	32	2	2

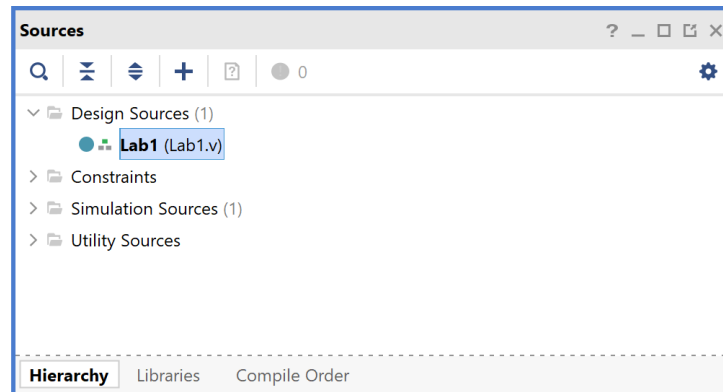
10. You will see a summary of the options selected. If all is correct, click “Finish”.



11. After a few seconds, you should see a project window open, along with a new window to define a new module. This is a wizard that will help you generate the inputs/outputs of a module, but we will not use it in this lab, so click “OK”. You may get a warning that the module is empty, ignore it and approve.



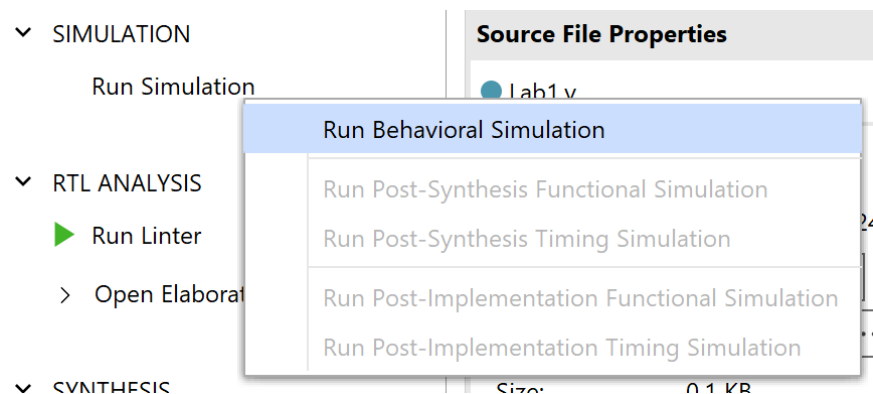
12. Under the *Sources* sub-window, you should now see a new Design Sources file (this could also be under a Non-Module heading). Open it by double-clicking on the file name.



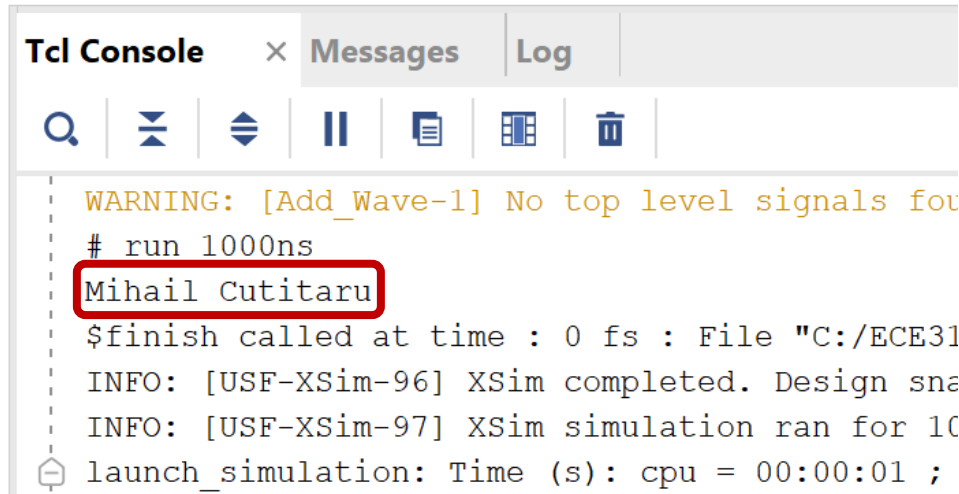
13. Type the following code. Replace my name with your own name and save the file.

```
Project Summary x Lab1.v * x
C:/ECE310Fall2024-Projects/Lab1/Lab1.srscs/sources_1/new/Lab1.v
1 `timescale 1ns / 1ps
2
3 module Lab1();
4     initial begin
5         $display("Mihail Cutitaru");
6         $finish;
7     end
8 endmodule
9
```

14. On the left side, click on “Run Simulation” and choose “Run Behavioral Simulation”.

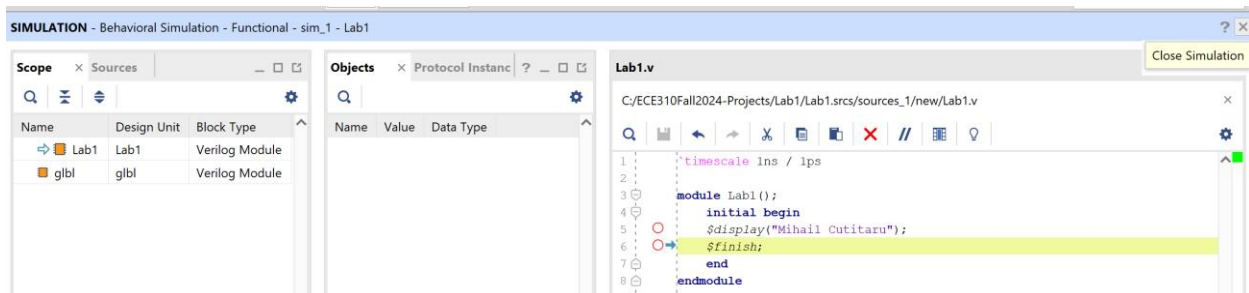


15. You will enter Simulation mode and Vivado will simulate your code. Under the Tcl Console sub-window at the bottom of the screen you will see your name be displayed along with a significant other of other lines. **Take a screenshot of this and upload to Moodle as the deliverable for Lab 1. It must show your name in order to get credit.**



```
WARNING: [Add_Wave-1] No top level signals for
# run 1000ns
Mihail Cutitaru
$finish called at time : 0 fs : File "C:/ECE31
INFO: [USF-XSim-96] XSim completed. Design sn
INFO: [USF-XSim-97] XSim simulation ran for 10
launch_simulation: Time (s): cpu = 00:00:01 ;
```

16. Exit simulation mode by clicking on the close button in the upper right corner. You will get a warning that you are about to exit, check “Don’t show this dialog again” and click “OK”.



17. Close Vivado. You will get a warning that you are about to exit, check “Don’t show this dialog again” and click “OK”.