NC State University
Department of Electrical and Computer Engineering

ECE 310 – Fall 2025

Lab 6

Summary

In this lab, you will implement a Parallel-Input-Serial-Output (PISO) and a Serial-Input-Parallel-Output (SIPO) 8-bit registers.

Deliverables

1. Pen-and-paper/digital design of PISO and SIPO modules (2 designs).
2. Code for models (testbench submissions are optional).
3. Screenshots of simulation waveforms with at least 2 non-trivial input vectors for each model (4 vectors total).
4. Screenshots of synthesis results (*RTL Analysis* section in Vivado), comparison to expected results in Step 1, and discussion on any differences.
5. Extra Credit – up to 10 additional points will be added for typesetting your report in LaTeX, depending on usage of LaTeX elements (e.g. figures, tables, sections, etc).

Instructions

1. A PISO is a hardware structure that loads parallel data (multiple bits) on the input side and serializes it (one bit at a time) on the output side. A SIPO is a hardware structure that is the opposite of a PISO. Both structures are modifications of a basic shift register with additional hardware to account for these functionalities. Use any level of modeling for this lab.

2. Create a new project in Vivado named **PISO_8bit**.

3. Design an 8-bit PISO register with 8-bit input **parallel_in** and 1-bit output **serial_out** that will serialize the input in 8 clock cycles. The output is serialized LSB-first – first output bit is **parallel_in[0]** (LSB) and then 1 bit per cycle until **parallel_in[7]** (MSB). The core of the shift register will be composed of the basic DFF described in class (input **d**, output **q**, input **clk**) and modified as needed to add the capability for an active-high synchronous reset (input **rst**). Additional gates/units/logic may be needed in order to add the ability for the PISO module to load parallel data (input **load**) and shift data (input **shift**), both active-high inputs that are mutually exclusive (i.e. (load = 1 and shift = 1) or (load = 0 and shift = 0) will cause no change in the output). Hint: this may require the equivalent of a mux control structure. Shift in **0**'s for the emptied locations in the shift register.
   Show the pen-and-paper/digital diagram for your PISO unit and submit it with your work. Create a testbench for your own testing purposes and show clear timing diagram screenshots with at least TWO 8-bit inputs passing through your PISO module one after the other, with and without a delay between the inputs as well as loading and shifting data. Synthesize your design and show a screenshot of the synthesis results in your report (use the *RTL Analysis* section in Vivado).

Compare the synthesized design with your pen-and-paper design and note any differences. Submission of your .v testbench file is optional.

4. Create a new project in Vivado named **SIPO_8bit**.

5. Design an 8-bit SIPO register with 1-bit input **serial_in** and 8-bit output **parallel_out** that will parallelize the input in 8 clock cycles. The first output bit is **parallel_out[0]** (LSB-first) and then 1 bit per cycle until **parallel_out[7]** (MSB). The core of the shift register will be composed of the basic DFF described in class (input **d**, output **q**, input **clk**) and modified as needed to add the capability for an active-high synchronous reset (input **rst**). Additional gates may be needed in order to add the ability for the SIPO module to shift data (active-high input **shift**) into the appropriate location in the output register. When not shifting, the SIPO module maintains the old value and ignores the input value.
   Show the pen-and-paper/digital diagram for your SIPO unit and submit it with your work. Create a testbench for your own testing purposes and show clear timing diagram screenshots with TWO 8-bit sequences as inputs being parallelized through your SIPO module, with and without a delay between the 8-bit sets and shifting or not shifting. Synthesize your design (use the *RTL Analysis* section in Vivado) and show a screenshot of the synthesis results in your report. Compare the synthesized design with your pen-and-paper design and note any differences. Submission of your .v testbench file is optional.

Grading breakdown:

- Pen-and-paper/digital designs – 20 pts (10 pts each)
- SIPO/PISO model/implementation in Verilog – 40 pts (20 pts each)
- Passing tests (at least 2 for each design) – 20 pts (5 pts each test)
- Lab report with as much information present as possible, including test vectors and reasoning, resulting waveforms and discussion, synthesis vs. paper design results and discussion of any differences – 20 pts
- Extra Credit – up to 10 additional points will be added for typesetting your report in LaTeX, depending on usage of LaTeX elements (e.g. figures, tables, sections, etc).