Abstract

The objective of this report is to examine the realization of a room occupancy tracking project using VHDL code. The code is simulated and synthesized using the Modelsim software and the Vivado software respectively. A conceptual diagram was created to establish the system. Since the code has not faithfully followed that diagram and there was poor management of time, the code has been poorly designed. This poor design has impacted the quality of the design and the speed of the system. Furthermore, it has perhaps been the one to cause warnings during the synthesis process. Despite this, the project has been fully realized and is fully functional.

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2. Introduction

This report aims to discuss the design, modelling, simulation, and synthesization processes of a digital design project. The project's objective was to design, simulate, and synthesize a digital system that tracks the occupancy of a room.

In the room, there is an exit door and an entrance door, where each are equipped with sensors. When people enter or exit the room, the signals X and Y are respectively triggered. The room has a max occupancy of 63 people. When it is reached, the signal Z is triggered. In addition, a reset signal exists to return the system to its initial state if wanted.

To create such a system, a conceptual diagram was made. With the diagram, the VHDL code was written to model the system. A testbench was created to verify the outputs using the Modelsim simulation software. Finally, the code was synthesized for a Xilinx Nexys A7 FPGA development board using the Vivado software.

3. Conceptual diagram

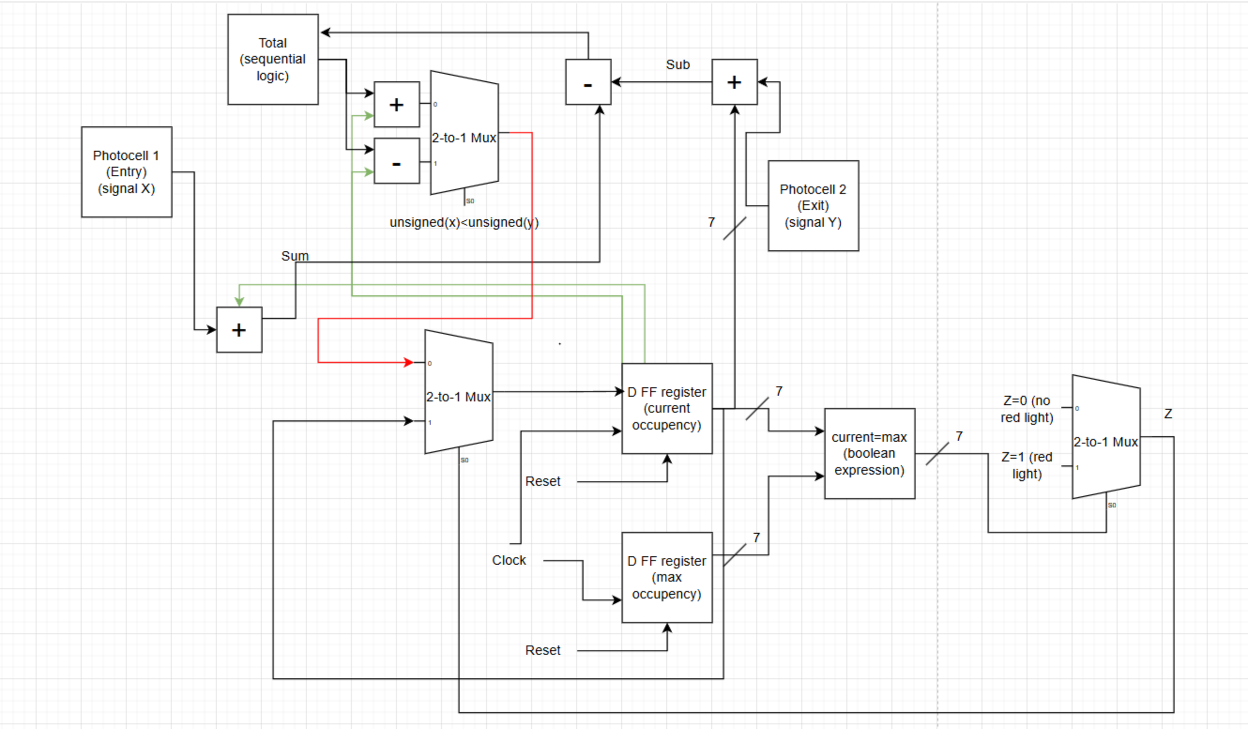

Total (sequential logic)
+
-
2-to-1 Mux
0
1
S0
-
Sub
+
Photocell 1 (Entry) (signal X)
Photocell 2 (Exit) (signal Y)
unsigned(x)<unsigned(y)
7
Sum
+
2-to-1 Mux
0
1
S0
D FF register (current occupency)
7
current=max (boolean expression)
7
Z=0 (no red light)
Z=1 (red light)
2-to-1 Mux
0
1
S0
Z
Reset
Clock
D FF register (max occupency)
7
Reset

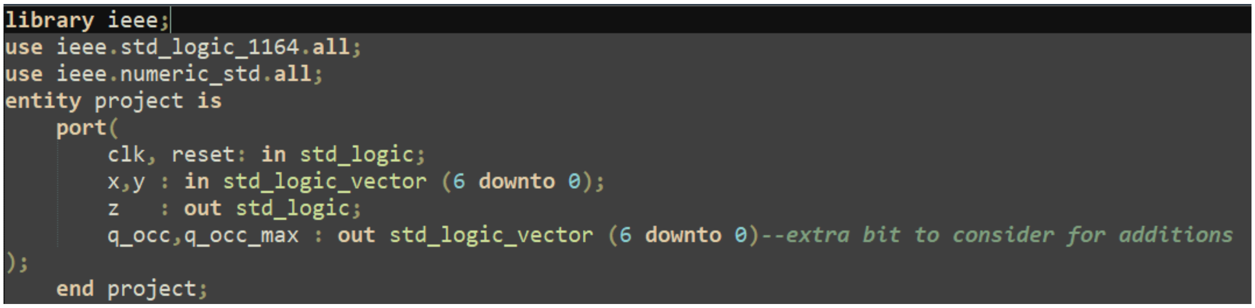
Figure 1: Conceptual diagram of the system (for the sake of clarity, some lines are colored)

Figure 1 represents the conceptual diagram of the system. Starting from the right with the Z signal, the current occupancy and max occupancy, which are held in two different registers, are used for a Boolean expression which acts as a selector for the mux. If they are equal, it means that max occupancy is reached, and Z is then 1. Otherwise, Z is 0. Both registers have a clock and reset signal.

The Z signal is used as a selector for another mux. Since the Z signal is an indicator whether the max occupancy of the room is reached, if Z=1, then no change is made to the current occupancy value inside the register (current occupancy value is fed back into the register). Otherwise, the total is fed into the register.

The sum of the binary signal X (ex: 0000100) is added with the current occupancy and stored in a variable called sum. Another variable, sub, is calculated by adding the binary signal Y and the current occupancy. The sum and sub are then used in a subtraction operation and the result is stored in total, where total represents the net amount of people that enter and leave the room. Depending on whether the signal Y is bigger than the signal X, the addition or subtraction with the current occupancy and the total is done, where the result represents the final value of the current occupancy after people have entered or left the room.

4. VHDL model and Testbench

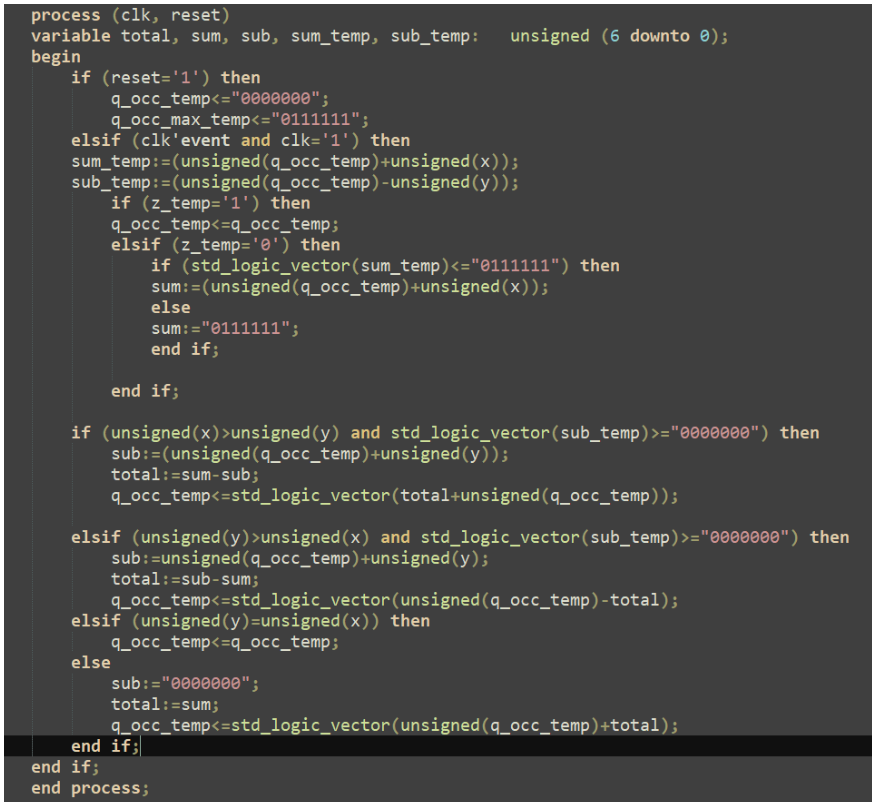


```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity project is
    port(
        clk, reset: in std_logic;
        x,y : in std_logic_vector (6 downto 0);
        z   : out std_logic;
        q_occ,q_occ_max : out std_logic_vector (6 downto 0)--extra bit to consider for additions
);
    end project;
```

Figure 2: Entity code of the project

Figure 2 shows the entity code of the project. There are 4 input ports: clk, reset, x, and y. X and Y are binary signals where their values are represented as vectors in VHDL (for ex: 0010000). There are 3 output ports: z, q_occ, and q_occ_max. The latter two signals respectively represent the current occupancy and max occupancy.

During the modeling of the project, some challenges were met, namely the addition of two vectors. The max occupancy (q_occ_max) is 63, or 111111 in unsigned binary, which is 6 bits. To add two vectors in VHDL, the vectors are converted to unsigned, which are then added together and converted back to a vector. However, when adding two vectors of 6 bits where their numbers are rather large (ex: 111111 and 111111), the overflow bit is discarded, which would mean that the sum is not correct. To resolve this problem, the vectors are extended from 6 bits to 7 bits.



```
process (clk, reset)
variable total, sum, sub, sum_temp, sub_temp:   unsigned (6 downto 0);
begin
    if (reset='1') then
        q_occ_temp<="0000000";
        q_occ_max_temp<="0111111";
    elsif (clk'event and clk='1') then
    sum_temp:=(unsigned(q_occ_temp)+unsigned(x));
    sub_temp:=(unsigned(q_occ_temp)-unsigned(y));
        if (z_temp='1') then
        q_occ_temp<=q_occ_temp;
        elsif (z_temp='0') then
            if (std_logic_vector(sum_temp)<="0111111") then
            sum:=(unsigned(q_occ_temp)+unsigned(x));
            else
            sum:="0111111";
            end if;

        end if;

    if (unsigned(x)>unsigned(y) and std_logic_vector(sub_temp)>="0000000") then
        sub:=(unsigned(q_occ_temp)+unsigned(y));
        total:=sum-sub;
        q_occ_temp<=std_logic_vector(total+unsigned(q_occ_temp));

    elsif (unsigned(y)>unsigned(x) and std_logic_vector(sub_temp)>="0000000") then
        sub:=unsigned(q_occ_temp)+unsigned(y);
        total:=sub-sum;
        q_occ_temp<=std_logic_vector(unsigned(q_occ_temp)-total);
    elsif (unsigned(y)=unsigned(x)) then
        q_occ_temp<=q_occ_temp;
    else
        sub:="0000000";
        total:=sum;
        q_occ_temp<=std_logic_vector(unsigned(q_occ_temp)+total);
    end if;
end if;
end process;
```

Figure 3: Process to determine what is fed into the current occupancy register

Variables, such as sum or sub, are used in the process to do sequential logic. From Figure 3, one can notice that the code does not accurately represent the conceptual diagram. When Z is equal to 0, the sum is calculated instead of the total being fed into the register. As such, the total is calculated after with the sub. While the objective of this code is accomplished, the code is rather not well designed after much consideration. The code could be shortened and be more comprehensible if the conceptual diagram was faithfully followed. This lack of proper design is due to mismanagement of time.

Another problem that was encountered when designing the model was the number of possible cases that can be encountered with the system. There were a relatively large number of cases, such as the number of people that enter that are lower than the number of people that leave the room. As such, there are many if-else statements in the code, which creates multiple multiplexers in the design. Furthermore, the last else statement has a needless statement, where sub is assigned a value of 0.

With the way the process works, people enter first and then people leave. For example, if the current occupancy is 43, the number of people that want to enter is 63, and the number of people that want to leave is 15. The system adds first and the maximum is reached. Therefore, the sum is 63, and sub is 15. The final occupancy becomes 63-15 = 48. The arguably preferrable way for the system to work is that people leave first, and then people enter. As such, more people enter the room.

As for the testbench, a number of scenarios were covered, such as what if all people leave or what if Z is 1 and people are trying to enter the room. If one wanted the system to be activated every time someone enters or leaves the room (i.e. changing X and Y to std_logic and increment/decrement by one), then one can create an intermediate signal vector and use the concatenation operator to attach the value of X or Y to the vector and use for loops in the testbench to test the code.

If further explanation about the codes is needed, the VHDL model and testbench codes can be viewed with .txt files in the ZIP file attached with this report.

5. Simulation and Synthesis results

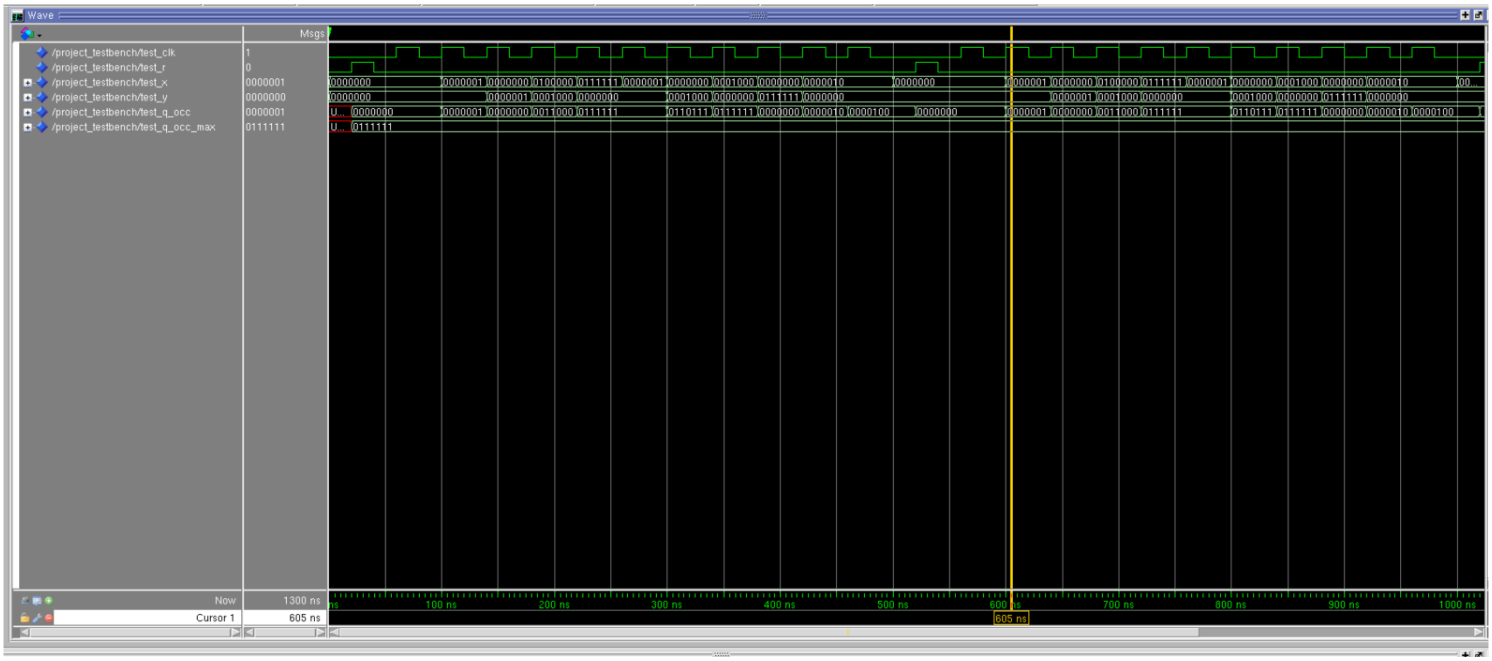

Wave
Msgs
/project_testbench/test_clk 1
/project_testbench/test_r 0
/project_testbench/test_x 0000001
/project_testbench/test_y 0000000
/project_testbench/test_q_occ 0000001
/project_testbench/test_q_occ_max 0111111
0000000 0000001 0000000 0100000 0111111 0000001 0000000 0001000 0000000 0000010 0000000 0000001 0000000 0100000 0111111 0000001 0000000 0001000 0000000 0000010 00...
0000000 0000001 0001000 0000000 0001000 0000000 0111111 0000000 0000001 0001000 0000000 0001000 0000000 0111111 0000000
U... 0000000 0000001 0000000 0011000 0111111 0110111 0111111 0000000 0000010 0000100 0000000 0000001 0000000 0011000 0111111 0110111 0111111 0000000 0000010 0000100
U... 0111111
Now 1300 ns
Cursor 1 605 ns
ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1000 ns
605 ns

Figure 4: Simulation results (for more clarity, the picture and simulation results are attached in the Zip file)

As seen from Figure 4, the simulation results show that the VHDL code works as intended. While the Z wave is missing, when trying to add more to the room which has reached max occupancy, the current occupancy is still 63. Furthermore, the waves are reset to their intended values when the reset signal is one. As expected, when Y is 0111111, the current occupancy becomes 0.

The synthesis process proved to be successful, and its log file can be seen Figure 7. The RTL schematic and the synthesis schematic can be seen in Figure 5 and Figure 6. However, there were some warnings that were encountered during the synthesis. The first four warnings were about unused sequential elements such as sum_temp_reg or total_reg. The software then proceeded to remove them. Another warning was that parallel synthesis criteria was not met. Another was that a sequential element (sum_reg[6]) was unused, which was then promptly removed.

Overall, the simulation and synthesis results showed that the realization of the project has been a success.

6. Discussion of results

From the log file at the end section, one can see that the peak memory reached is 1773 MB. Free physical memory is 10247 MB and free virtual memory is 22170 MB. One can infer from the number of free memory that the design is more or less efficient. The log file does not contain any explicit information about the speed of the project.

However, while the Big-O function of this project is not known, one can see from the log file and from Figure 7 that it has 13 inputs and a large number of gates. Therefore, the speed of the system should still be adequately fast. The poor design of the code is reflected in Figure 7, and therefore affects the speed of the system. Overall, the design of the system is acceptable. It can easily be improved with better code design.

7. Conclusion

In conclusion, the project has been a success. It has been fully realized despite the warnings and problems that were met in the design, modelling, simulation, and synthesis processes. The speed and quality of the system is more or less adequate. Overall, this project has shown that there is a need for better time management for such a project, and has taught the skills required to design, model, and test such a project in VHDL.

Appendix

Figure 5: RTL schematic presented by Vivado

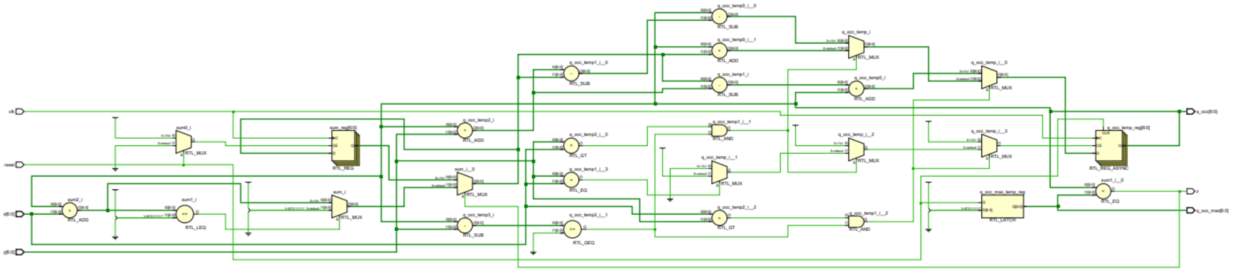


Figure 6: Synthesis schematic presented by Vivado

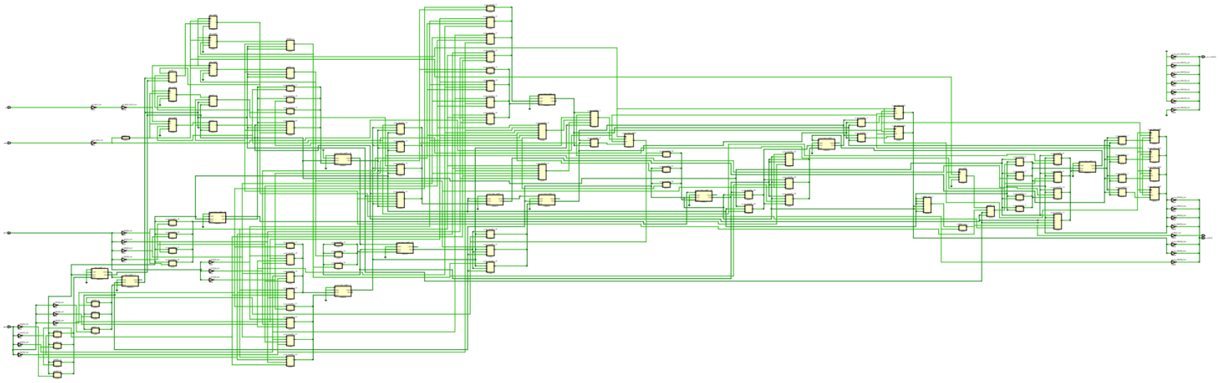


Figure 7: Log of the synsthesis

runme.log

```
*** Running vivado
    with args -log project.vds -m64 -product Vivado -mode batch -messageDb
vivado.pb -notrace -source project.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source project.tcl -notrace
Command: synth_design -top project -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 28800
-----------------------------------------------------------------------------
----
Starting Synthesize : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory
(MB): peak = 1401.578 ; gain = 85.801 ; free physical = 10440 ; free virtual
= 22361
-----------------------------------------------------------------------------
----
INFO: [Synth 8-638] synthesizing module 'project'
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:13]
WARNING: [Synth 8-6014] Unused sequential element sum_temp_reg was removed.
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:34]
WARNING: [Synth 8-6014] Unused sequential element sub_temp_reg was removed.
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:35]
WARNING: [Synth 8-6014] Unused sequential element sub_reg was removed.
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:48]
WARNING: [Synth 8-6014] Unused sequential element total_reg was removed.
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:49]
INFO: [Synth 8-256] done synthesizing module 'project' (1#1)
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:13]
-----------------------------------------------------------------------------
----
Finished Synthesize : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory
(MB): peak = 1446.219 ; gain = 130.441 ; free physical = 10452 ; free virtual
= 22373
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Finished Constraint Validation : Time (s): cpu = 00:00:02 ; elapsed =
00:00:03 . Memory (MB): peak = 1446.219 ; gain = 130.441 ; free physical =
10452 ; free virtual = 22373
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Start Loading Part and Timing Information
-----------------------------------------------------------------------------
----
Loading part: xc7a100tcsg324-1
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
-----------------------------------------------------------------------------
----
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:02 ;
elapsed = 00:00:03 . Memory (MB): peak = 1454.215 ; gain = 138.438 ; free
physical = 10451 ; free virtual = 22372
```

```
------------------------------------------------------------------------------
----
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared.
To prevent sharing consider applying a KEEP on the output of the operator
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:47]
WARNING: [Synth 8-327] inferring latch for variable 'q_occ_max_temp_reg'
[/nfs/home/b/br_duong/COEN313/Modelsim/Code/project.vhd:20]
------------------------------------------------------------------------------
----
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:02 ; elapsed =
00:00:03 . Memory (MB): peak = 1462.219 ; gain = 146.441 ; free physical =
10443 ; free virtual = 22364
------------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
No constraint files found.
------------------------------------------------------------------------------
----
Start RTL Component Statistics
------------------------------------------------------------------------------
----
Detailed RTL Component Info :
+---Adders :
           3 Input      7 Bit       Adders := 3
           2 Input      7 Bit       Adders := 2
           4 Input      7 Bit       Adders := 1
+---Registers :
                        7 Bit    Registers := 2
+---Muxes :
           2 Input      7 Bit        Muxes := 10
           2 Input      1 Bit        Muxes := 2
------------------------------------------------------------------------------
----
Finished RTL Component Statistics
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start RTL Hierarchical Component Statistics
------------------------------------------------------------------------------
----
Hierarchical RTL Component report
Module project
Detailed RTL Component Info :
+---Adders :
           3 Input      7 Bit       Adders := 3
           2 Input      7 Bit       Adders := 2
           4 Input      7 Bit       Adders := 1
+---Registers :
                        7 Bit    Registers := 2
+---Muxes :
           2 Input      7 Bit        Muxes := 10
```

```
          2 Input      1 Bit        Muxes := 2
-----------------------------------------------------------------------------
----
Finished RTL Hierarchical Component Statistics
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Start Part Resource Summary
-----------------------------------------------------------------------------
----
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
-----------------------------------------------------------------------------
----
Finished Part Resource Summary
-----------------------------------------------------------------------------
----
No constraint files found.
-----------------------------------------------------------------------------
----
Start Cross Boundary and Area Optimization
-----------------------------------------------------------------------------
----
Warning: Parallel synthesis criteria is not met
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\q_occ_max_temp_reg[6] )
INFO: [Synth 8-3886] merging instance 'q_occ_max_temp_reg[0]' (LD) to
'q_occ_max_temp_reg[5]'
INFO: [Synth 8-3886] merging instance 'q_occ_max_temp_reg[1]' (LD) to
'q_occ_max_temp_reg[5]'
INFO: [Synth 8-3886] merging instance 'q_occ_max_temp_reg[2]' (LD) to
'q_occ_max_temp_reg[5]'
INFO: [Synth 8-3886] merging instance 'q_occ_max_temp_reg[3]' (LD) to
'q_occ_max_temp_reg[5]'
INFO: [Synth 8-3886] merging instance 'q_occ_max_temp_reg[4]' (LD) to
'q_occ_max_temp_reg[5]'
INFO: [Synth 8-3333] propagating constant 1 across sequential element
(\q_occ_max_temp_reg[5] )
WARNING: [Synth 8-3332] Sequential element (q_occ_max_temp_reg[6]) is unused
and will be removed from module project.
WARNING: [Synth 8-3332] Sequential element (q_occ_max_temp_reg[5]) is unused
and will be removed from module project.
-----------------------------------------------------------------------------
----
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:06 ;
elapsed = 00:00:16 . Memory (MB): peak = 1596.051 ; gain = 280.273 ; free
physical = 10249 ; free virtual = 22171
-----------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
No constraint files found.
-----------------------------------------------------------------------------
----
Start Timing Optimization
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Finished Timing Optimization : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16
. Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical = 10249 ;
free virtual = 22171
-----------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-----------------------------------------------------------------------------
----
Start Technology Mapping
-----------------------------------------------------------------------------
----
WARNING: [Synth 8-3332] Sequential element (sum_reg[6]) is unused and will be
removed from module project.
-----------------------------------------------------------------------------
----
Finished Technology Mapping : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 .
Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical = 10249 ; free
virtual = 22171
-----------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-----------------------------------------------------------------------------
----
Start IO Insertion
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Start Flattening Before IO Insertion
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Finished Flattening Before IO Insertion
-----------------------------------------------------------------------------
----
-----------------------------------------------------------------------------
----
Start Final Netlist Cleanup
```

```
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Finished Final Netlist Cleanup
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Finished IO Insertion : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 .
Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical = 10273 ; free
virtual = 22195
------------------------------------------------------------------------------
----

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
------------------------------------------------------------------------------
----
Start Renaming Generated Instances
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Finished Renaming Generated Instances : Time (s): cpu = 00:00:06 ; elapsed =
00:00:16 . Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical =
10273 ; free virtual = 22195
------------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
------------------------------------------------------------------------------
----
Start Rebuilding User Hierarchy
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:06 ; elapsed =
00:00:16 . Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical =
10273 ; free virtual = 22195
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Renaming Generated Ports
------------------------------------------------------------------------------
----
```

```
------------------------------------------------------------------------------
----
Finished Renaming Generated Ports : Time (s): cpu = 00:00:06 ; elapsed =
00:00:16 . Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical =
10273 ; free virtual = 22195
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Handling Custom Attributes
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed =
00:00:16 . Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical =
10273 ; free virtual = 22195
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Renaming Generated Nets
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Finished Renaming Generated Nets : Time (s): cpu = 00:00:06 ; elapsed =
00:00:16 . Memory (MB): peak = 1596.051 ; gain = 280.273 ; free physical =
10273 ; free virtual = 22195
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Writing Synthesis Report
------------------------------------------------------------------------------
----

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    12|
|3     |LUT1   |     2|
|4     |LUT2   |    26|
|5     |LUT3   |    12|
|6     |LUT4   |    28|
|7     |LUT5   |     2|
|8     |LUT6   |     6|
|9     |FDCE   |     7|
|10    |FDRE   |     6|
```