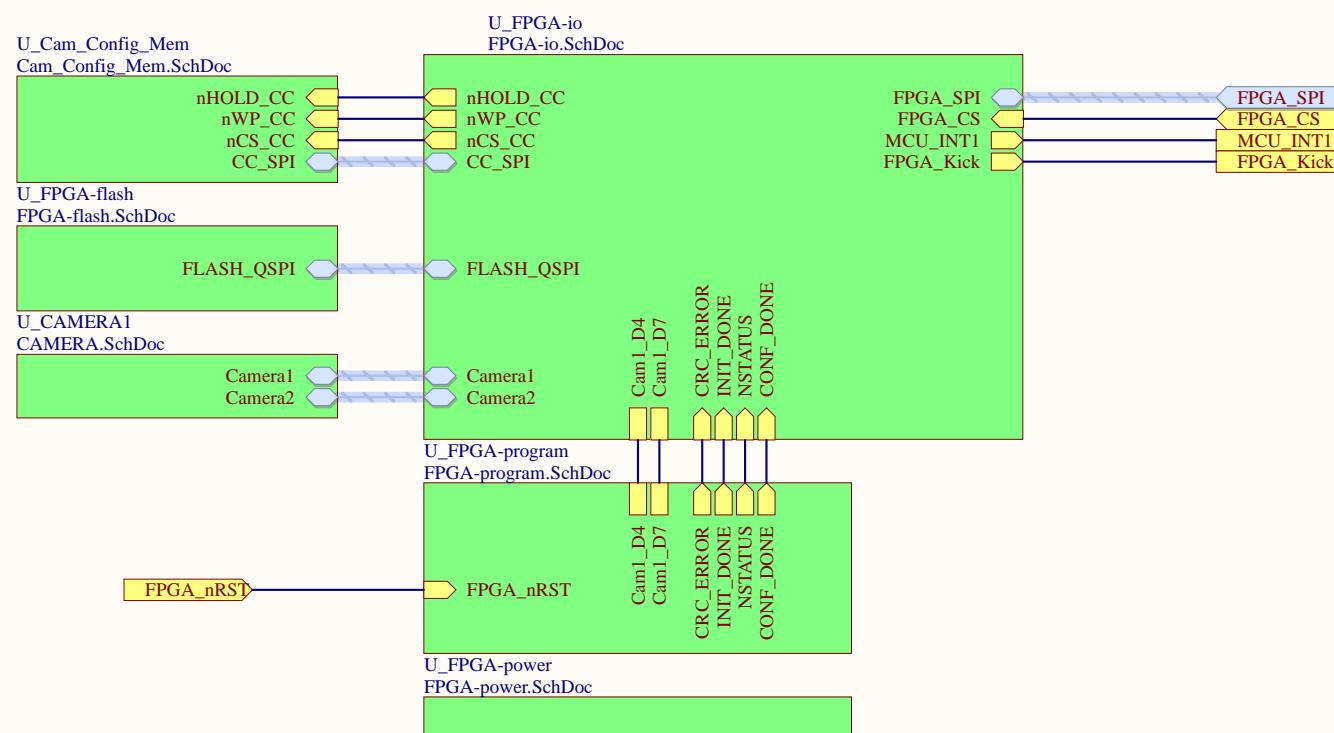


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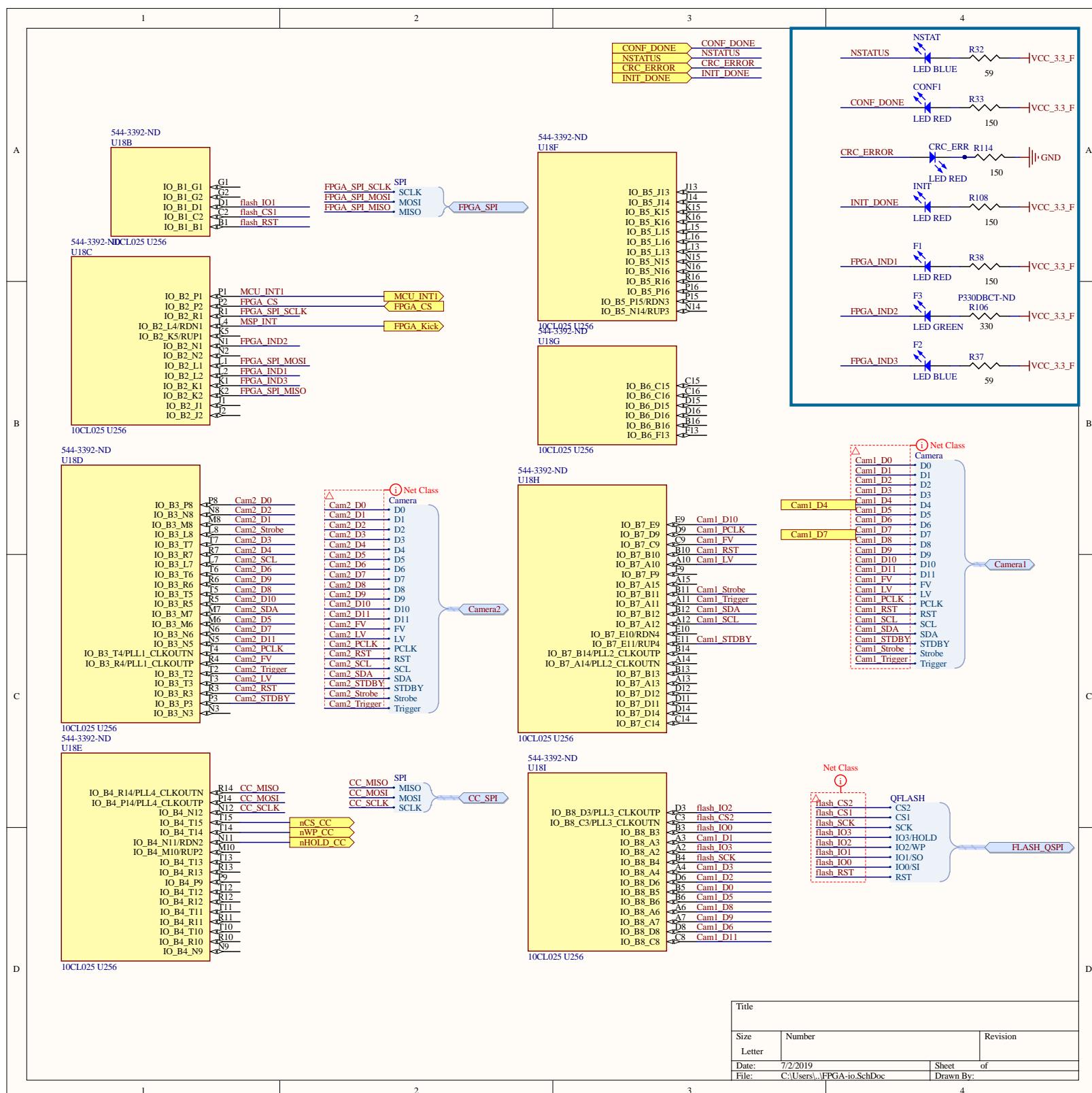
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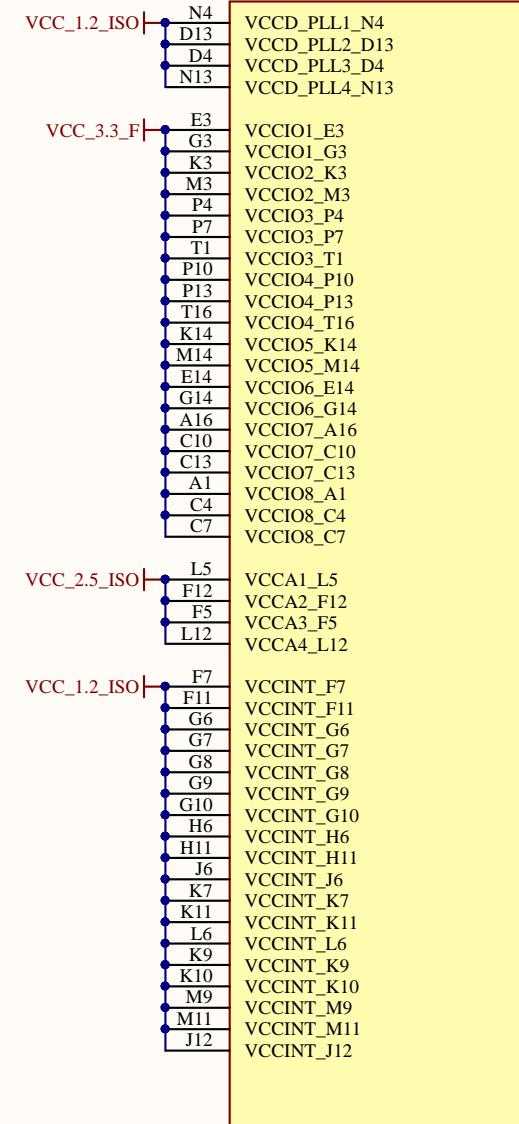
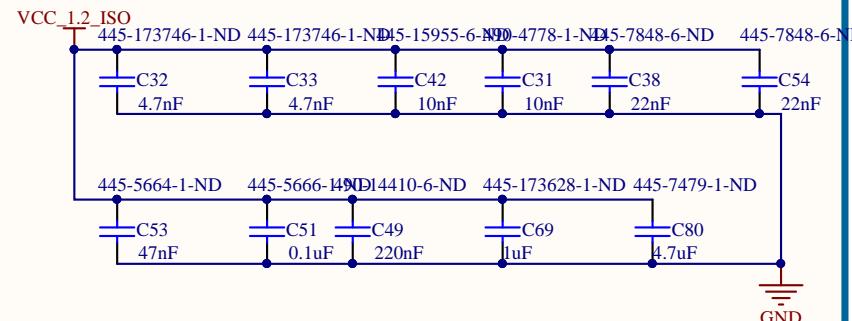
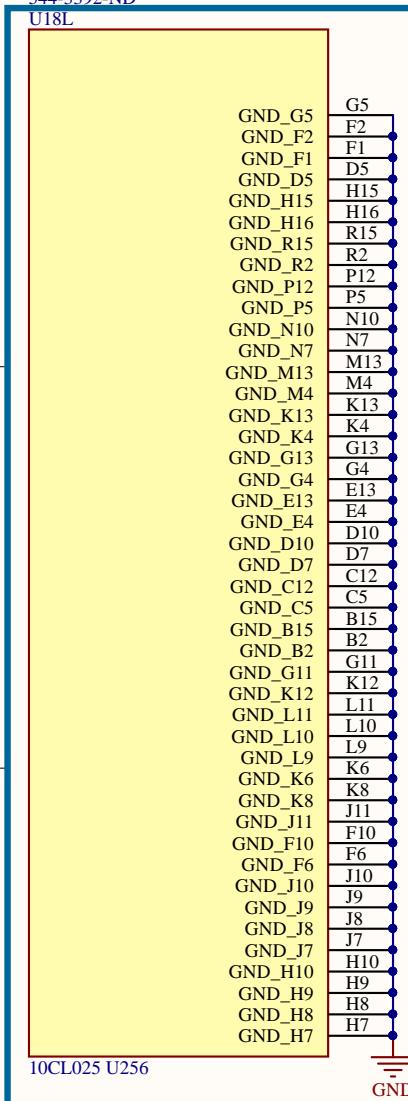
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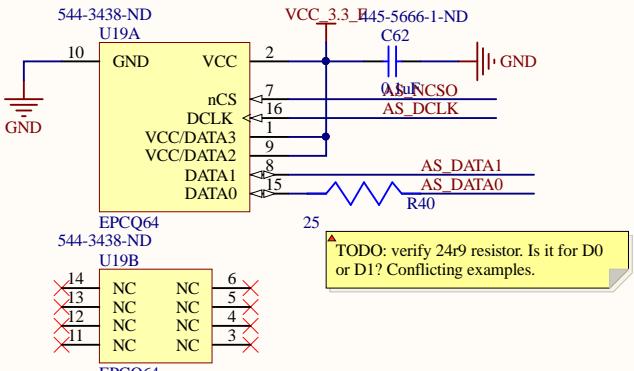
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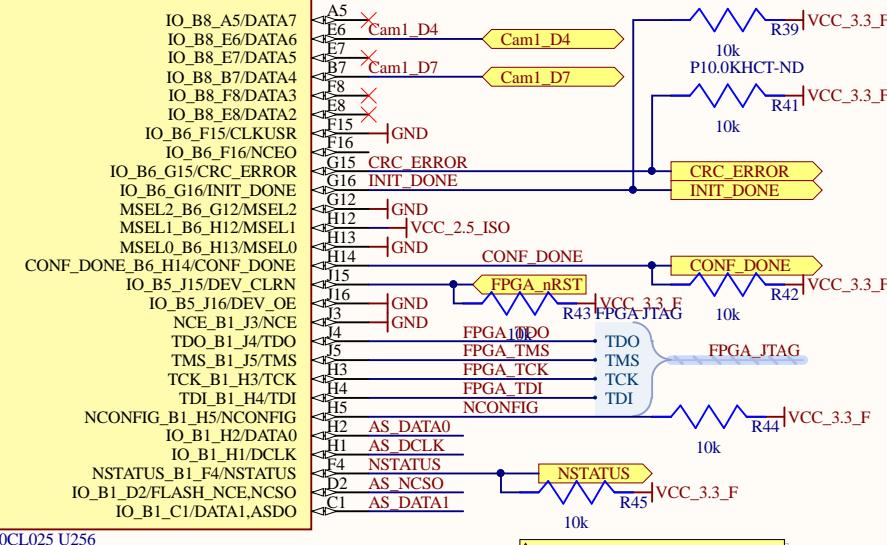
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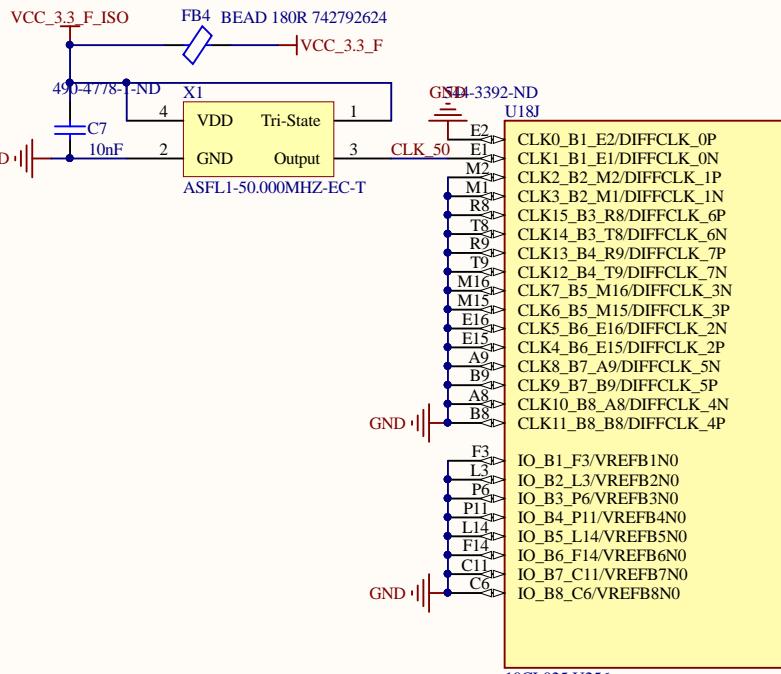
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VERSION : 2017.05.19  
PAGE : 11 of 13  
DATE : JUL 2017

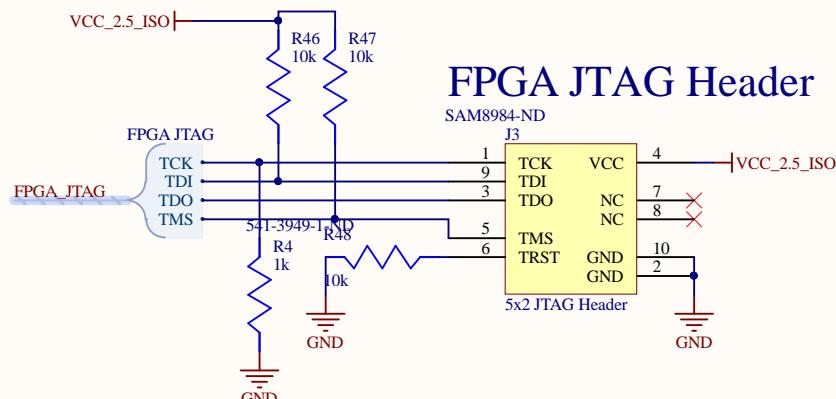
## FPGA Configuration Pins



# FPGA Clock/VREF



## FPGA JTAG Header



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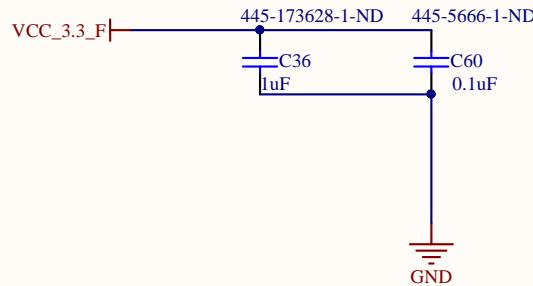
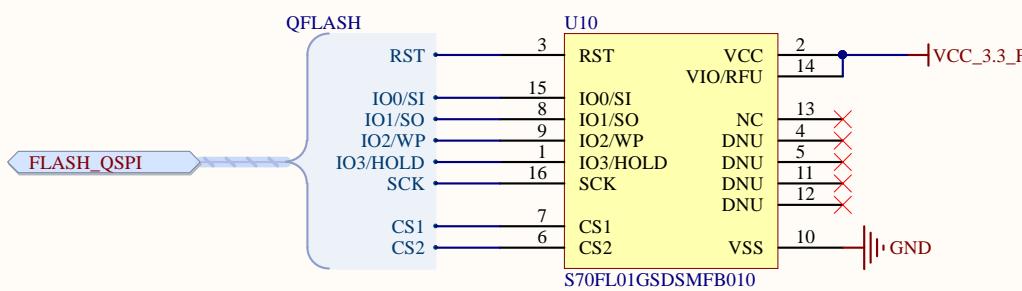
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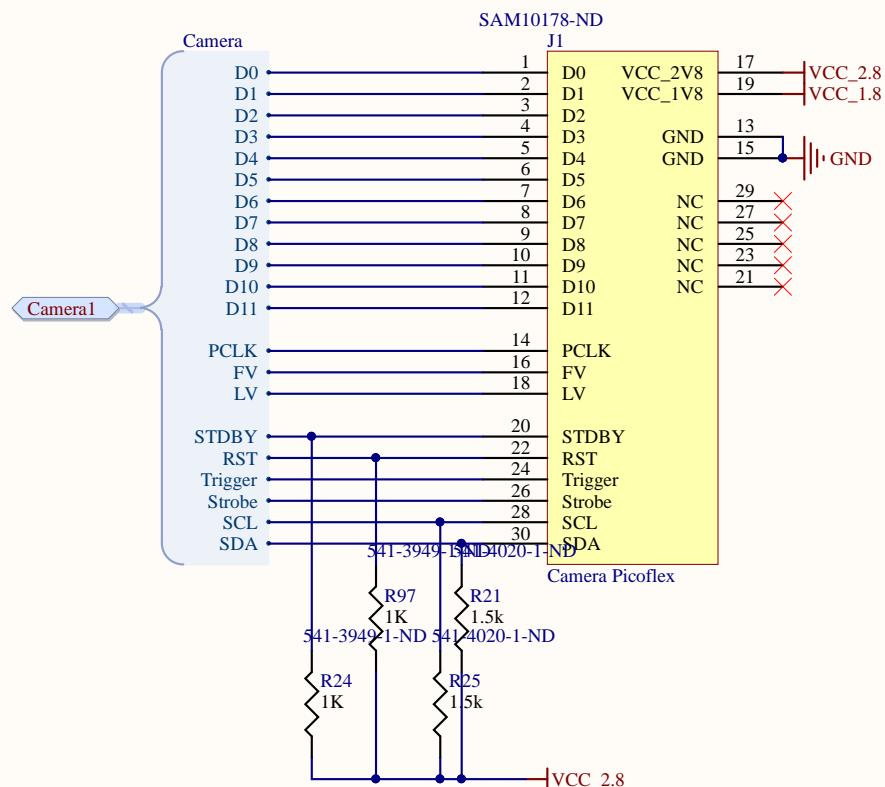
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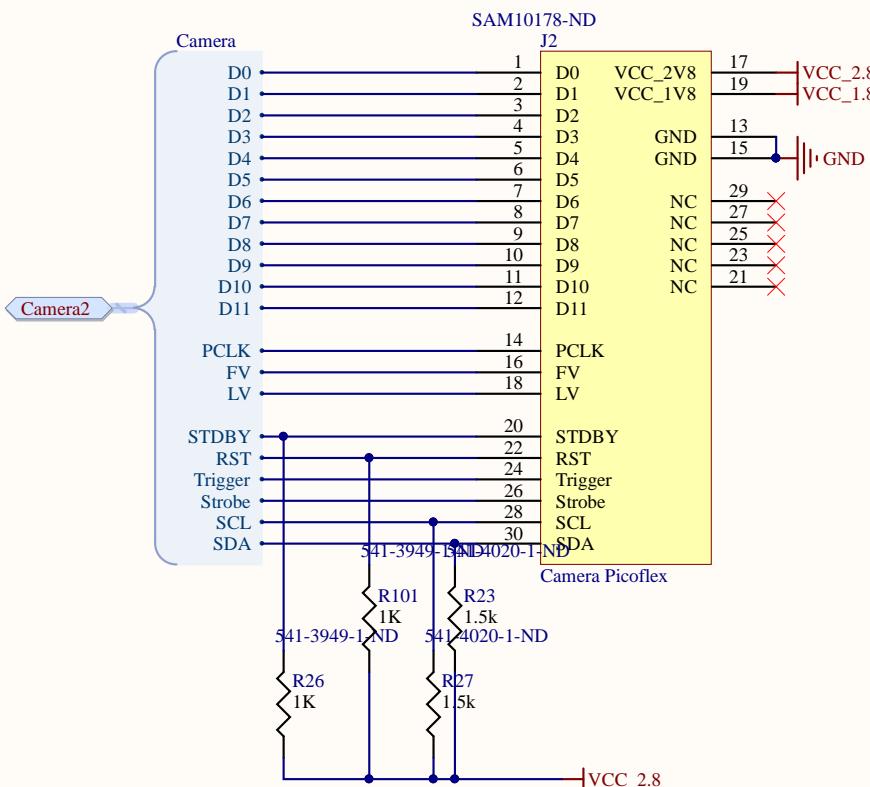
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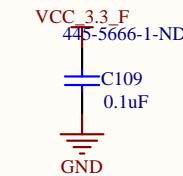
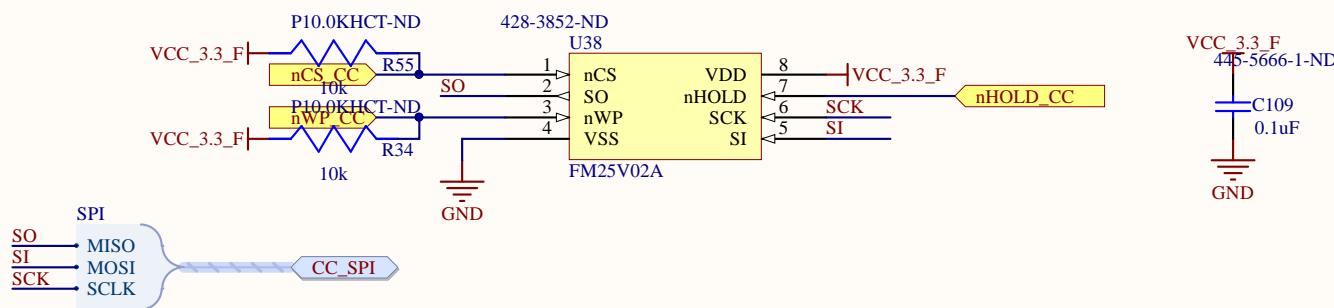
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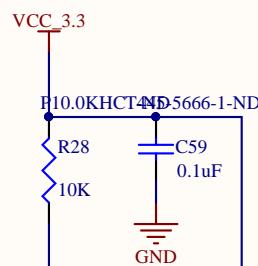
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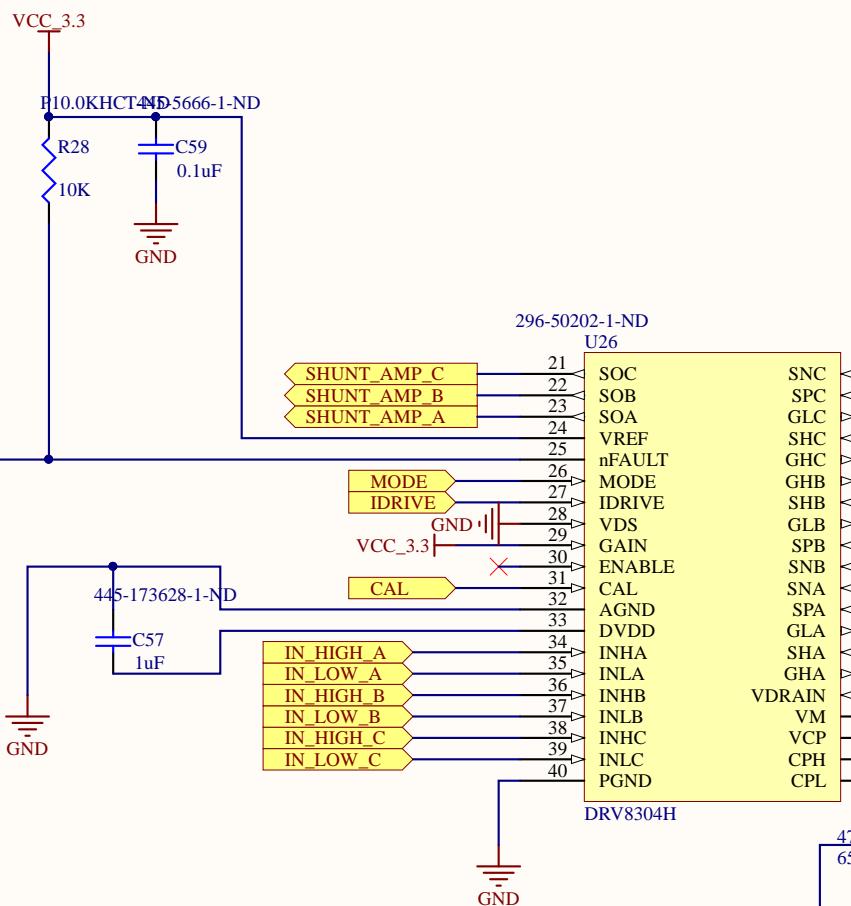
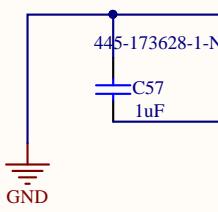
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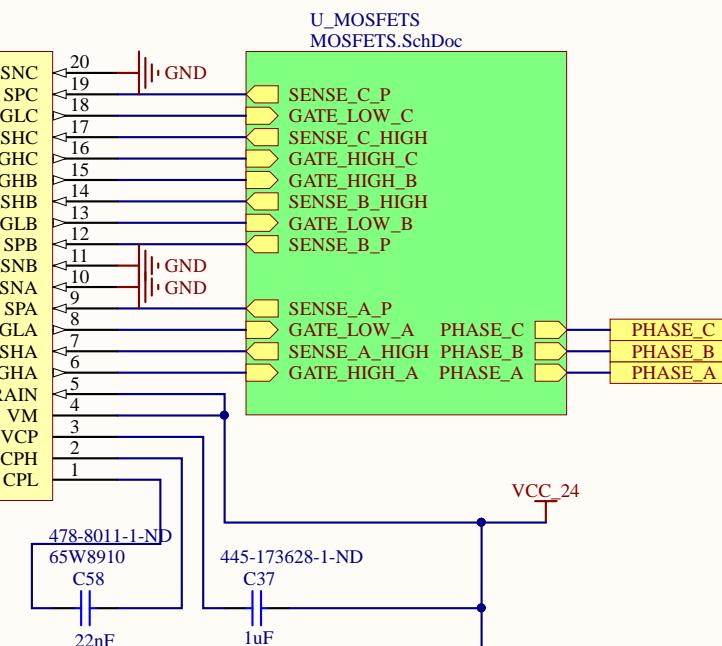
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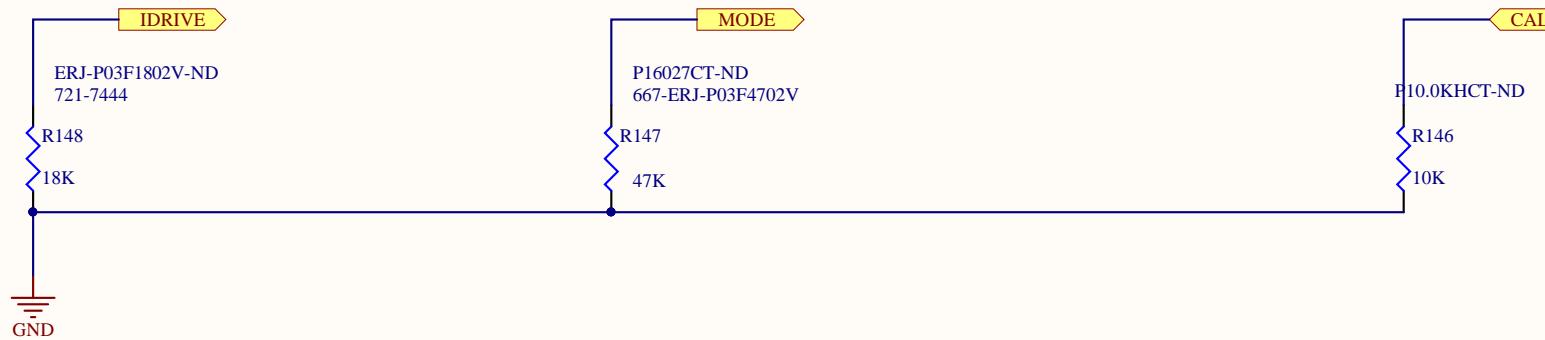
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IN\_LOW\_A

INLB\_CTRL

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INLC\_CTRL

IN\_LOW\_C

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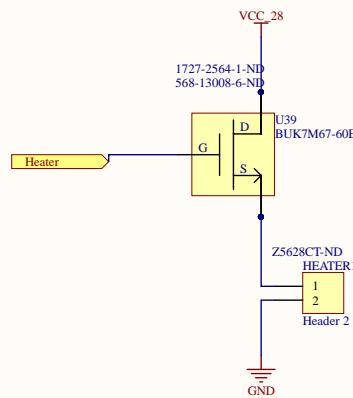
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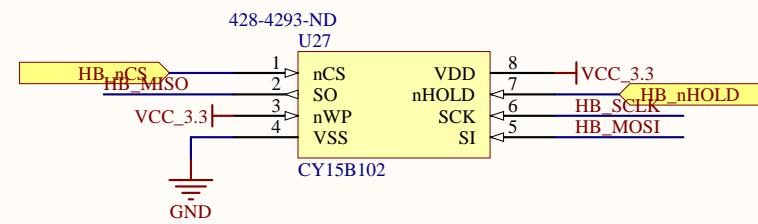
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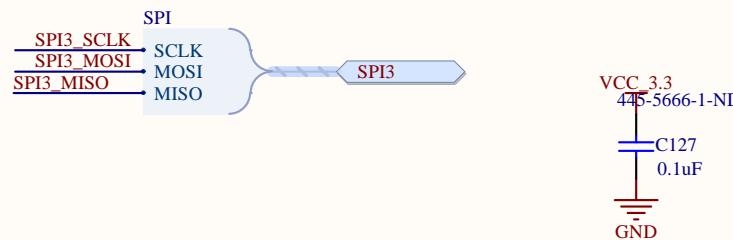
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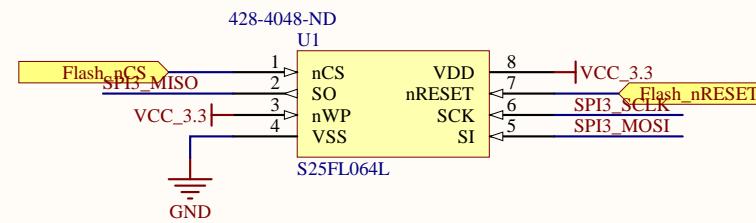
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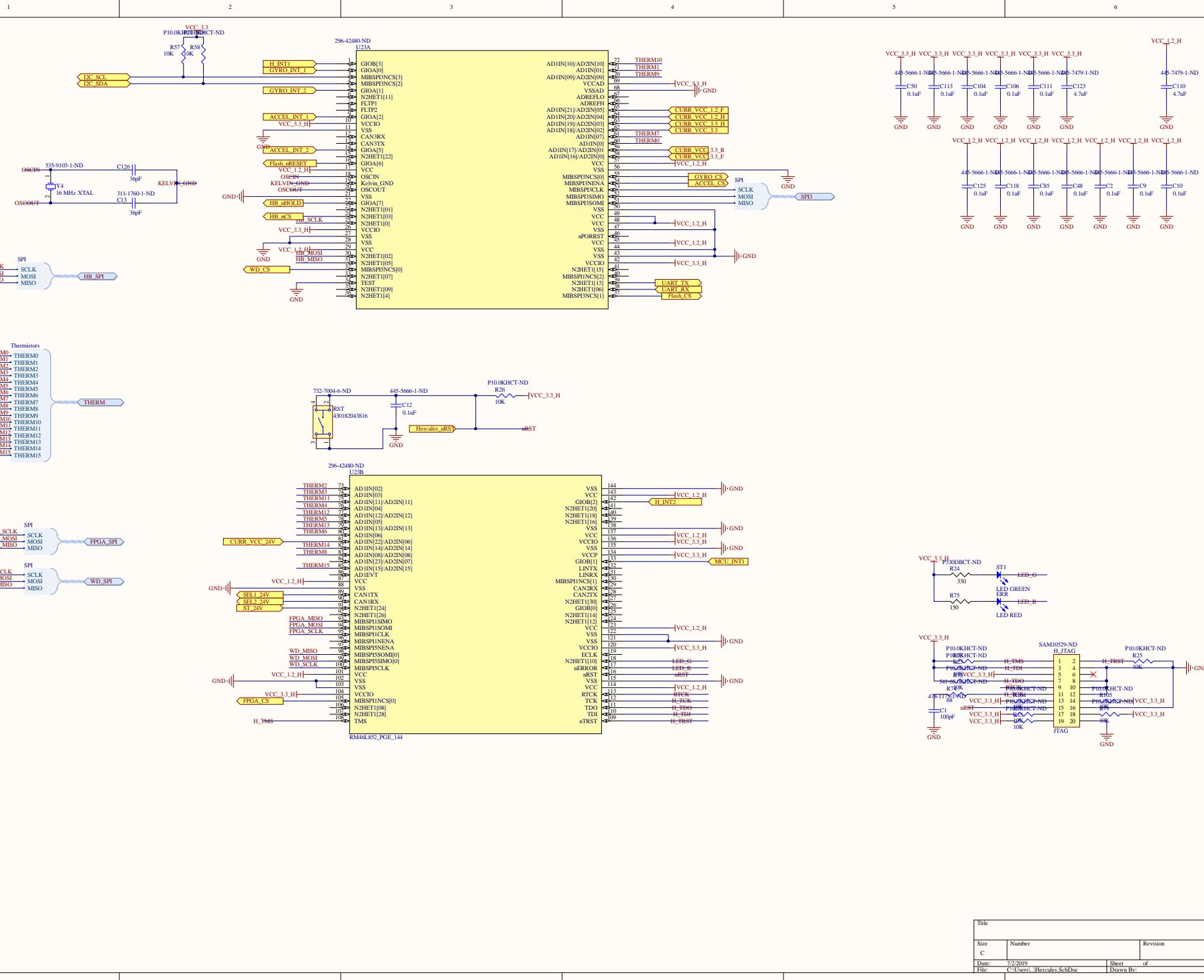
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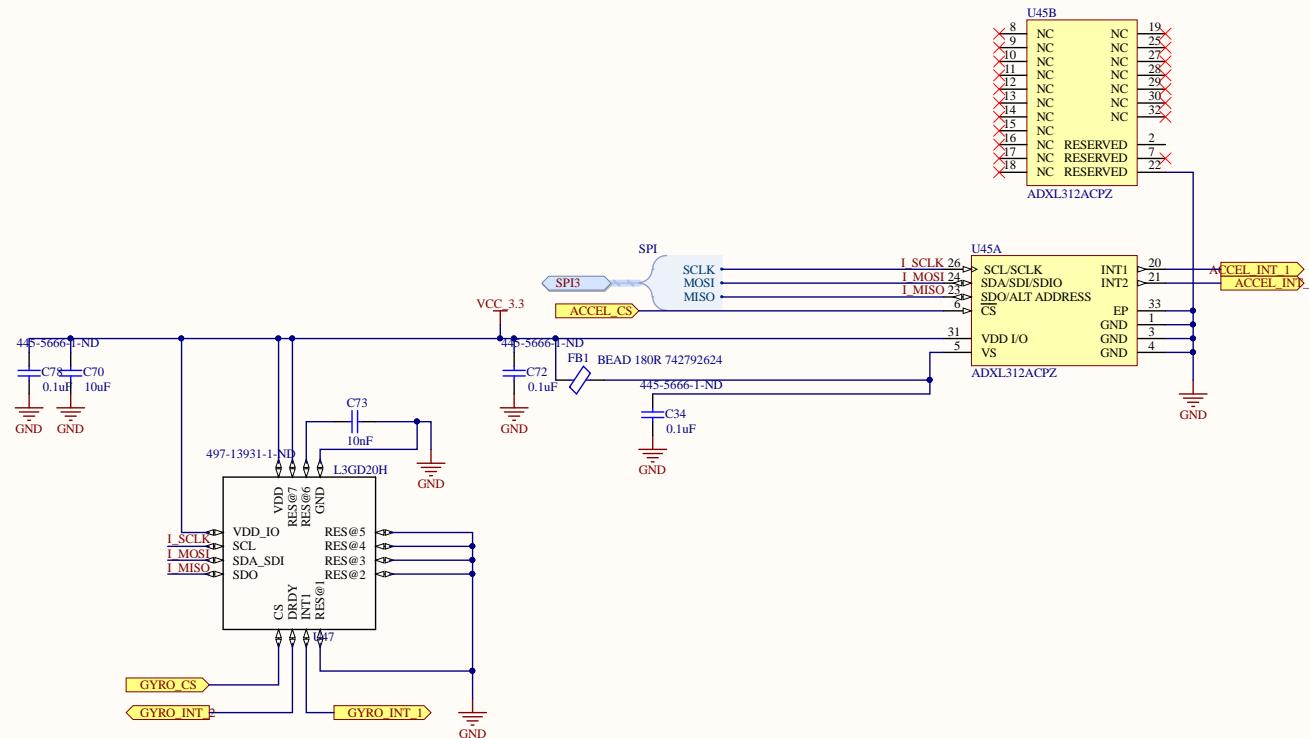


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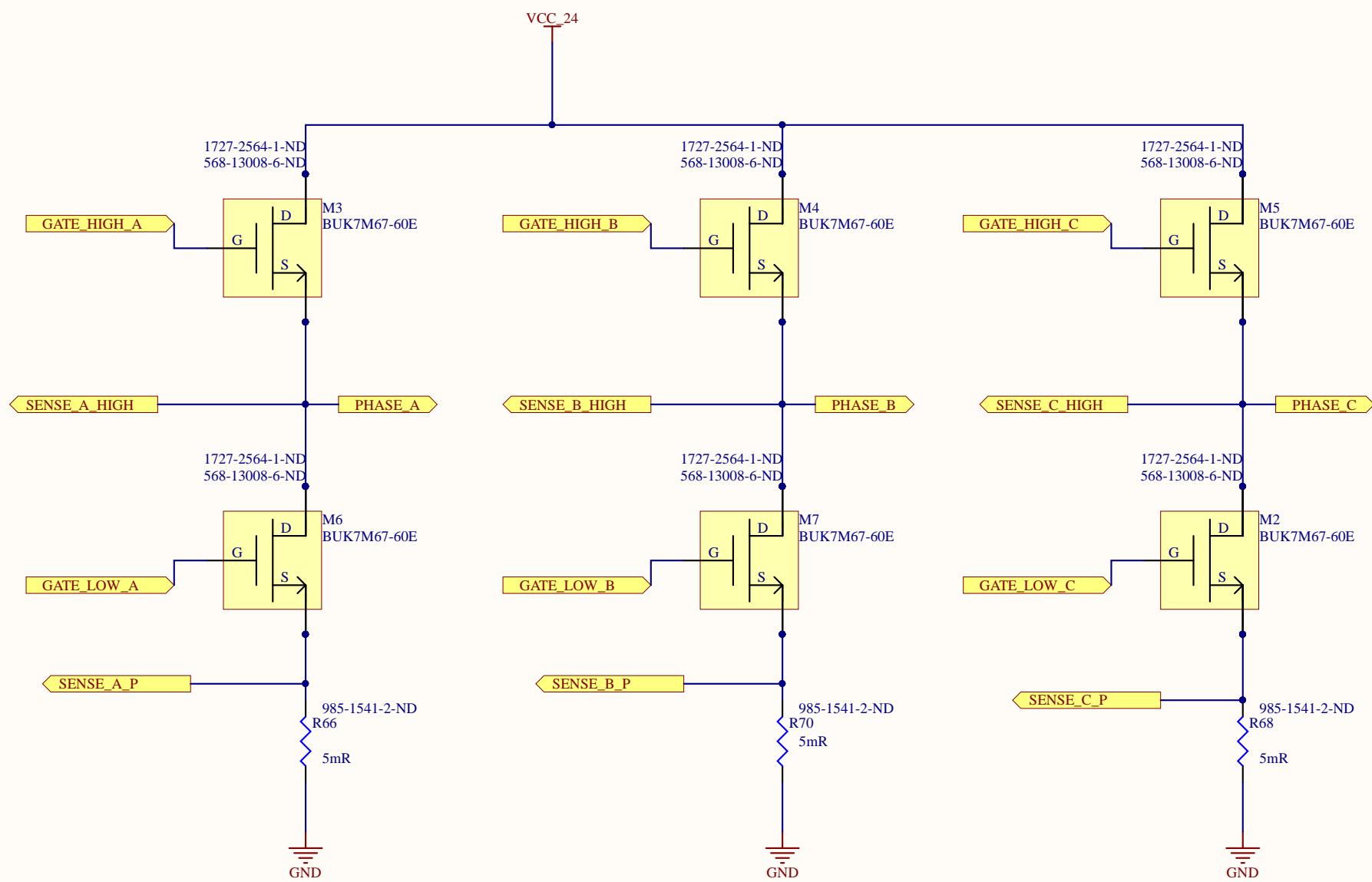




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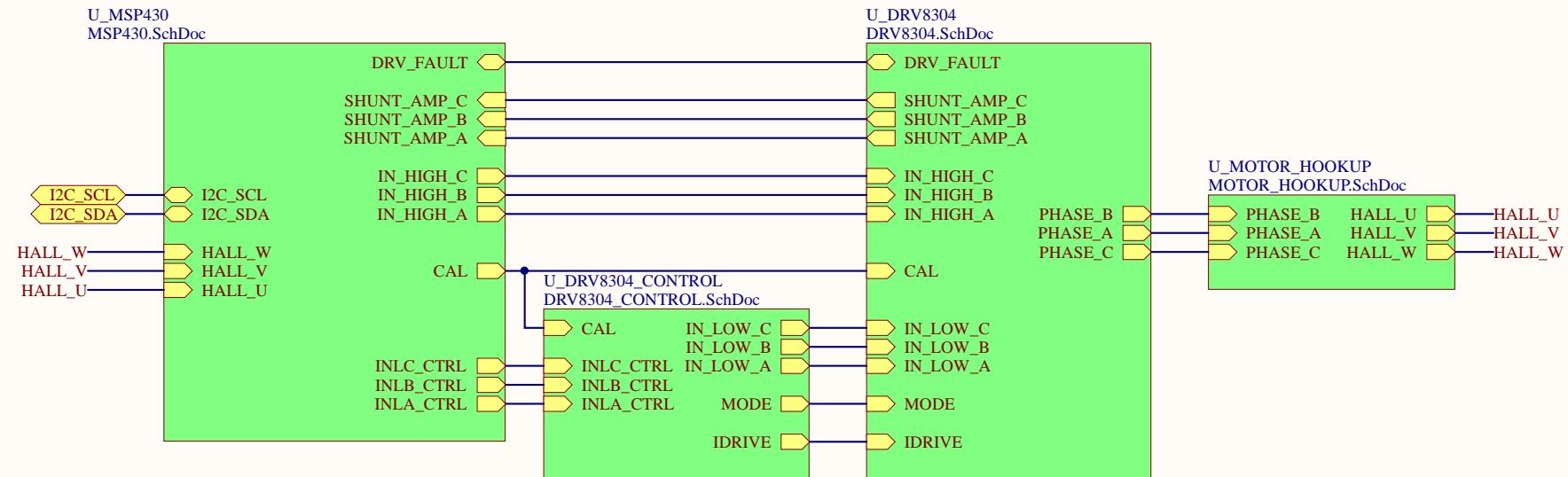
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File: C:\Users\...\Motor\_Driver.SchDoc

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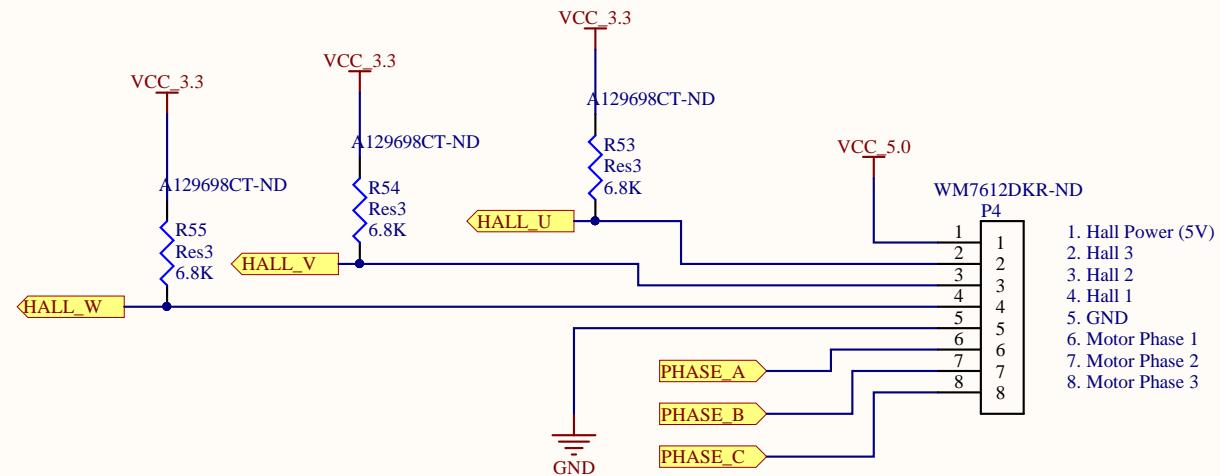
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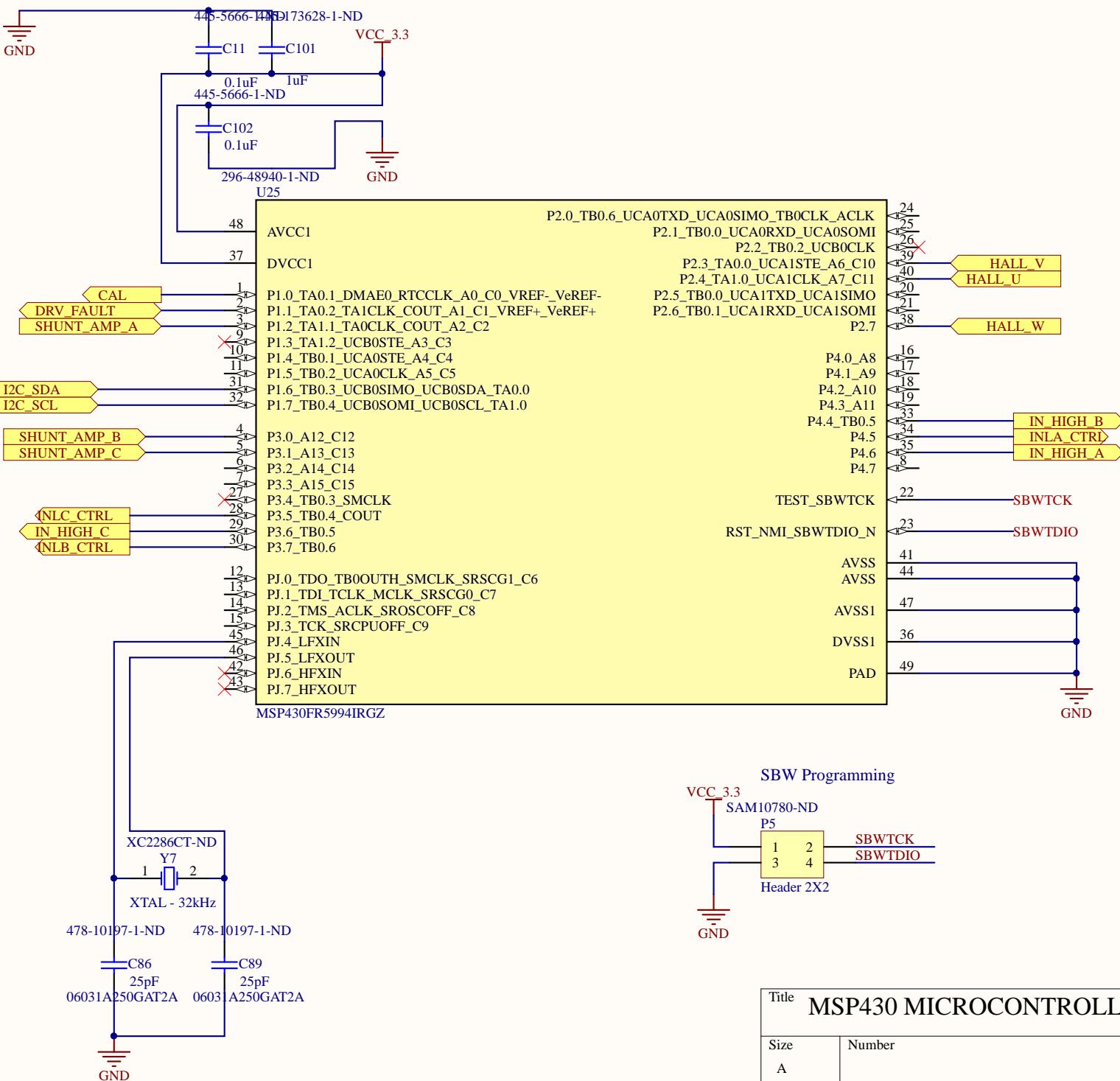
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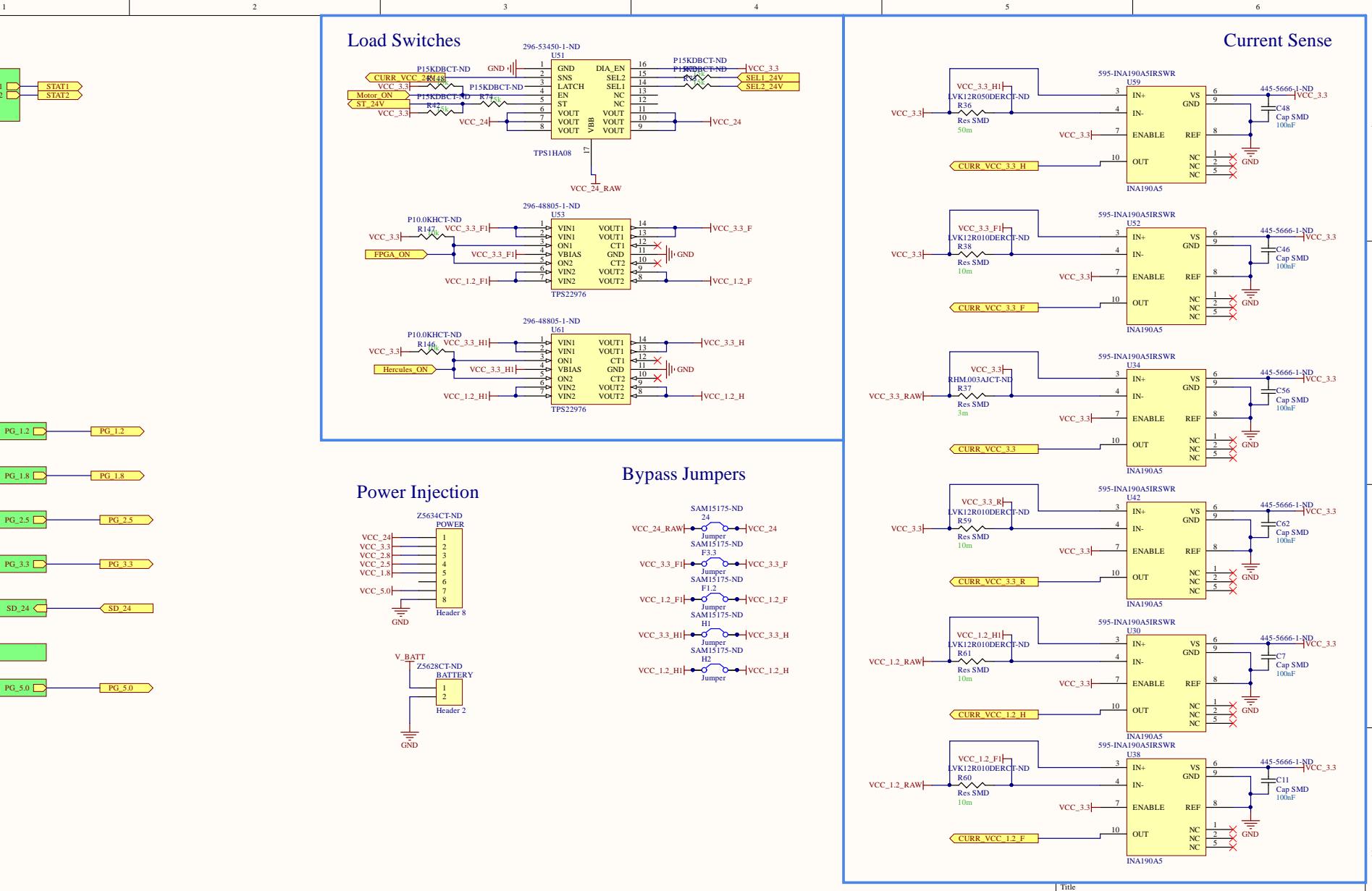
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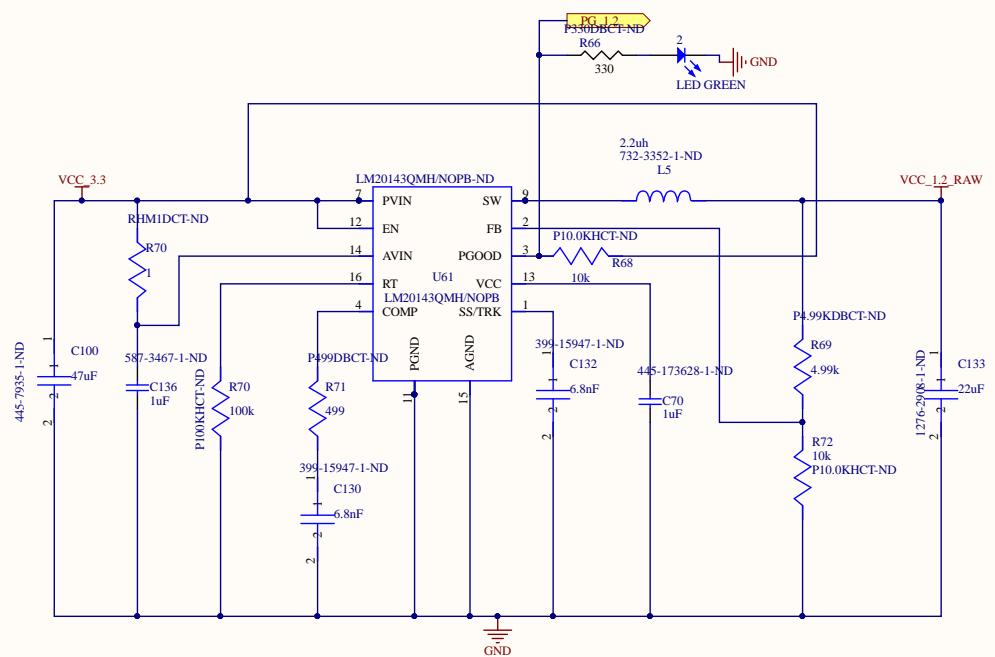
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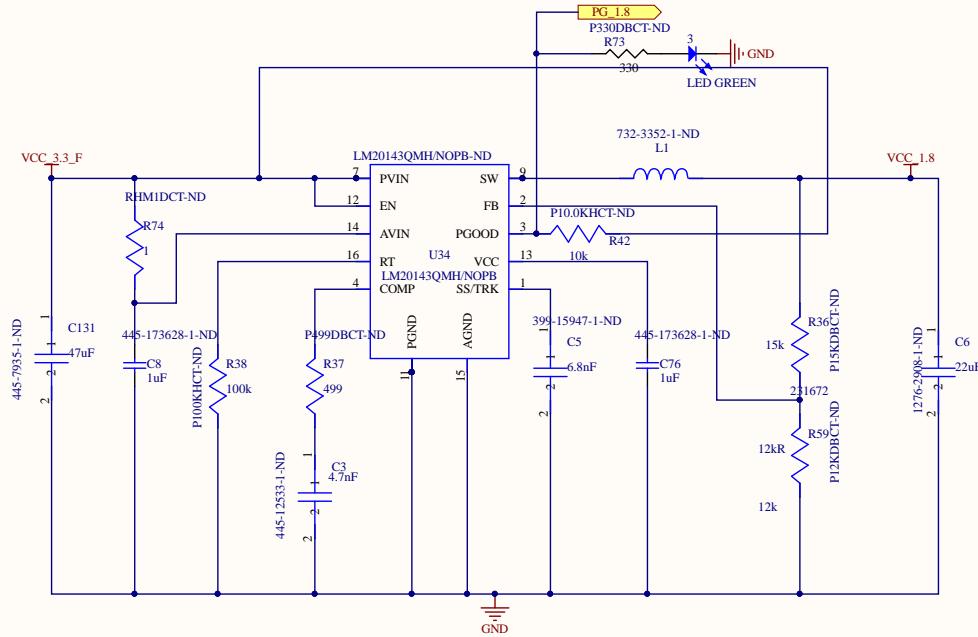
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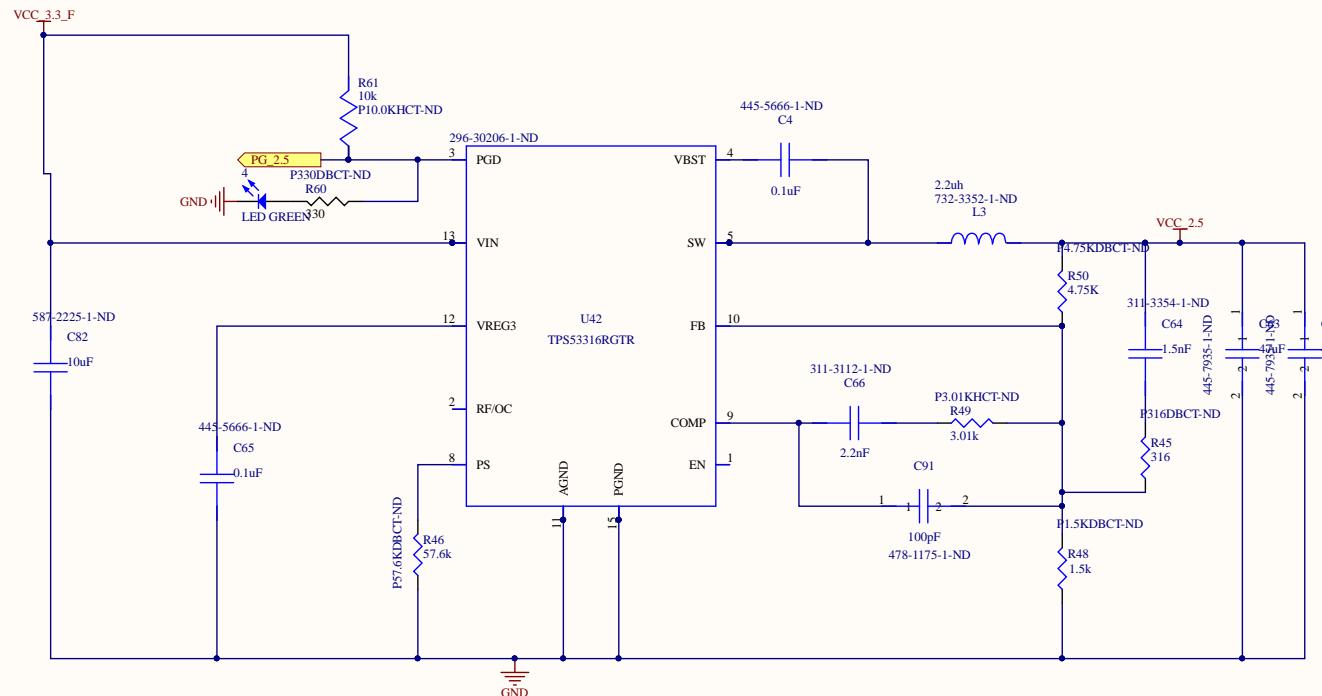
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Date: 7/2/2019	Sheet of	
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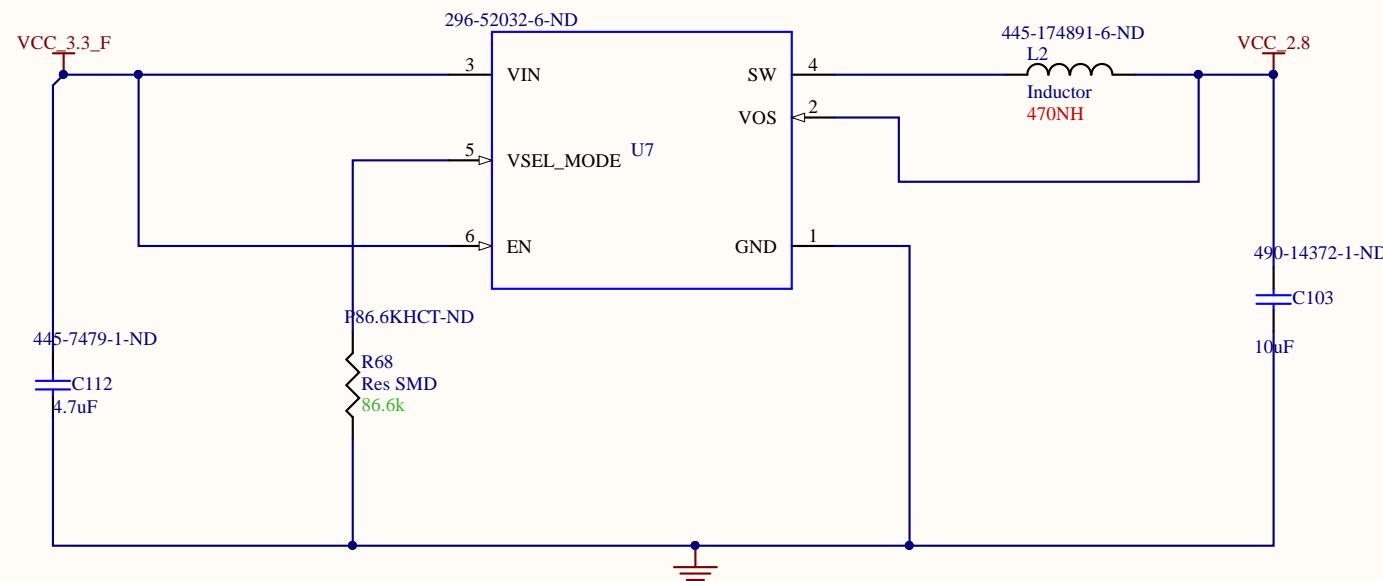
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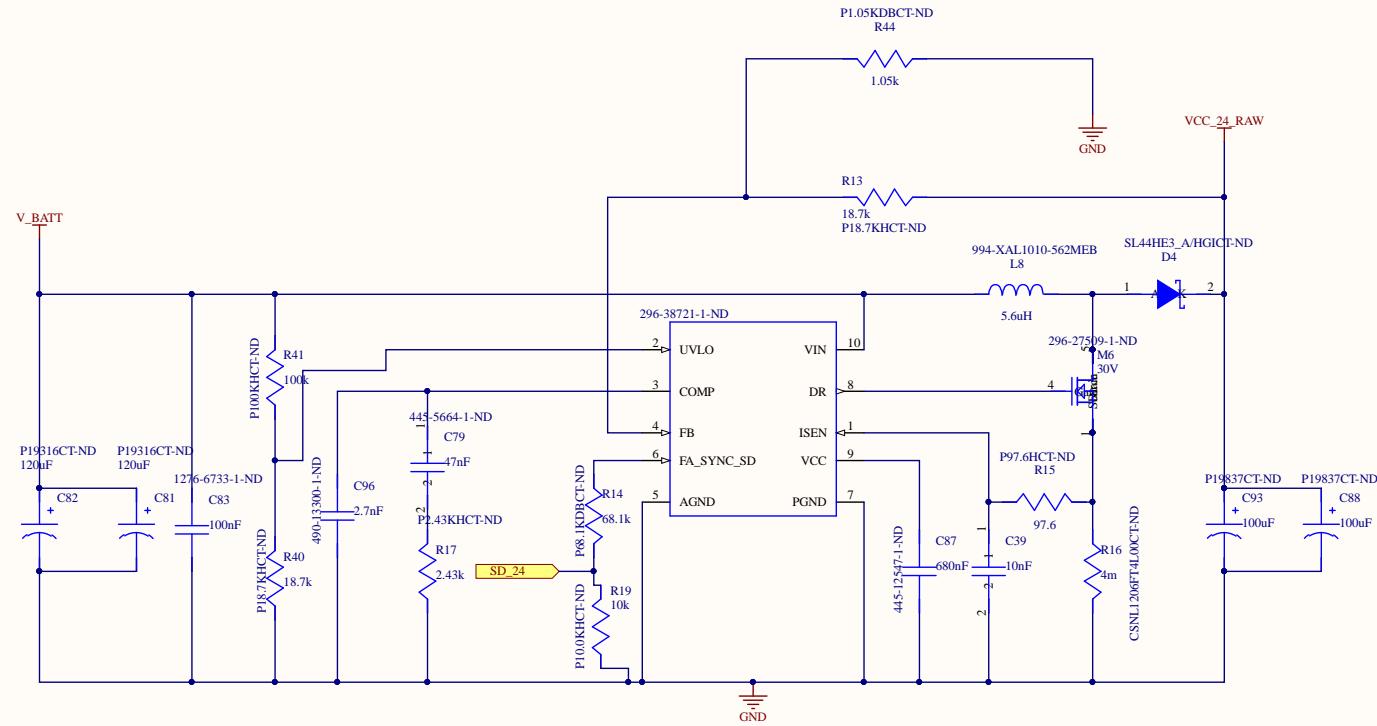
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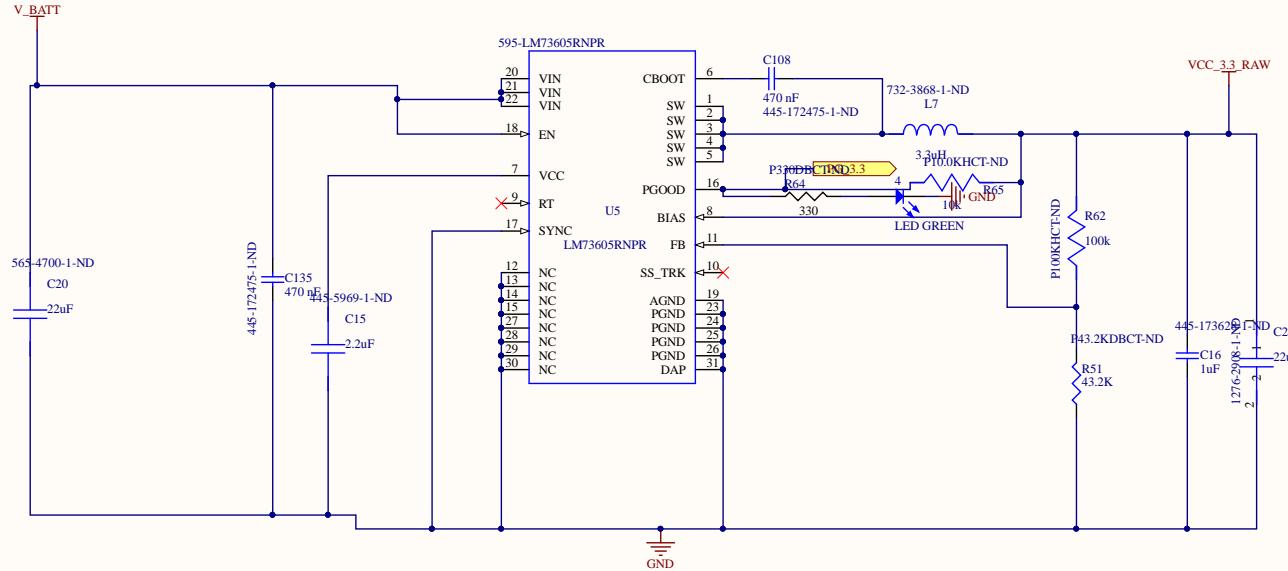
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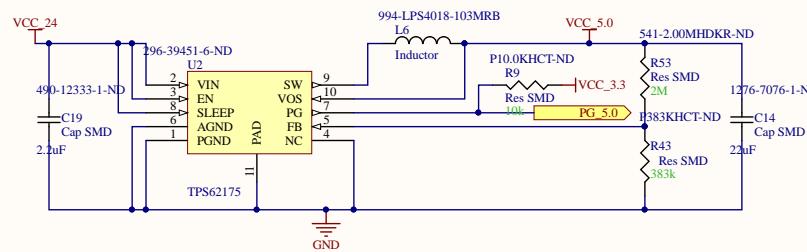
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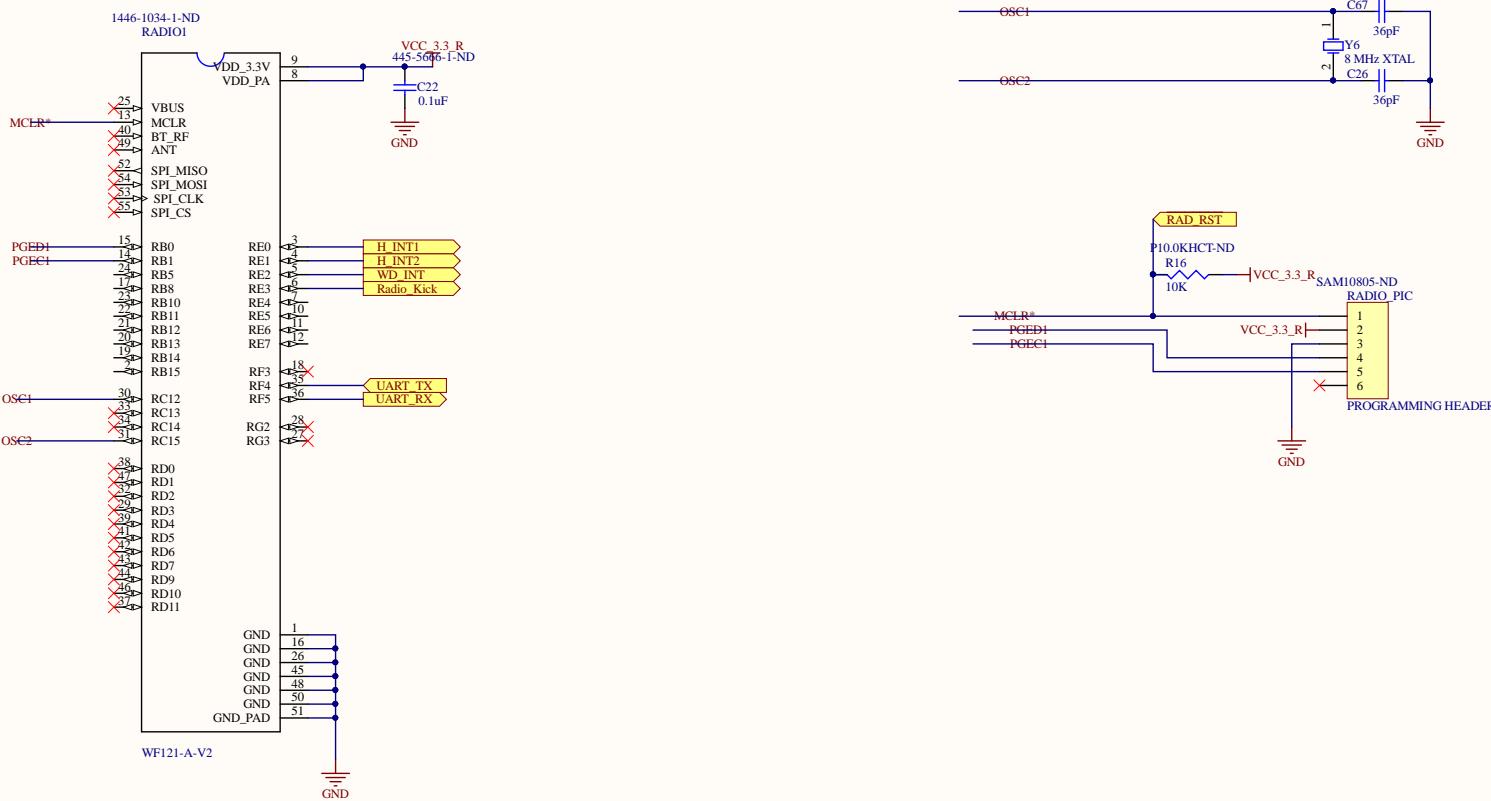
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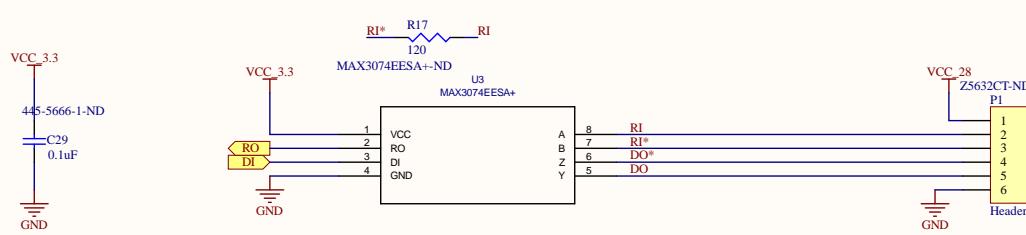
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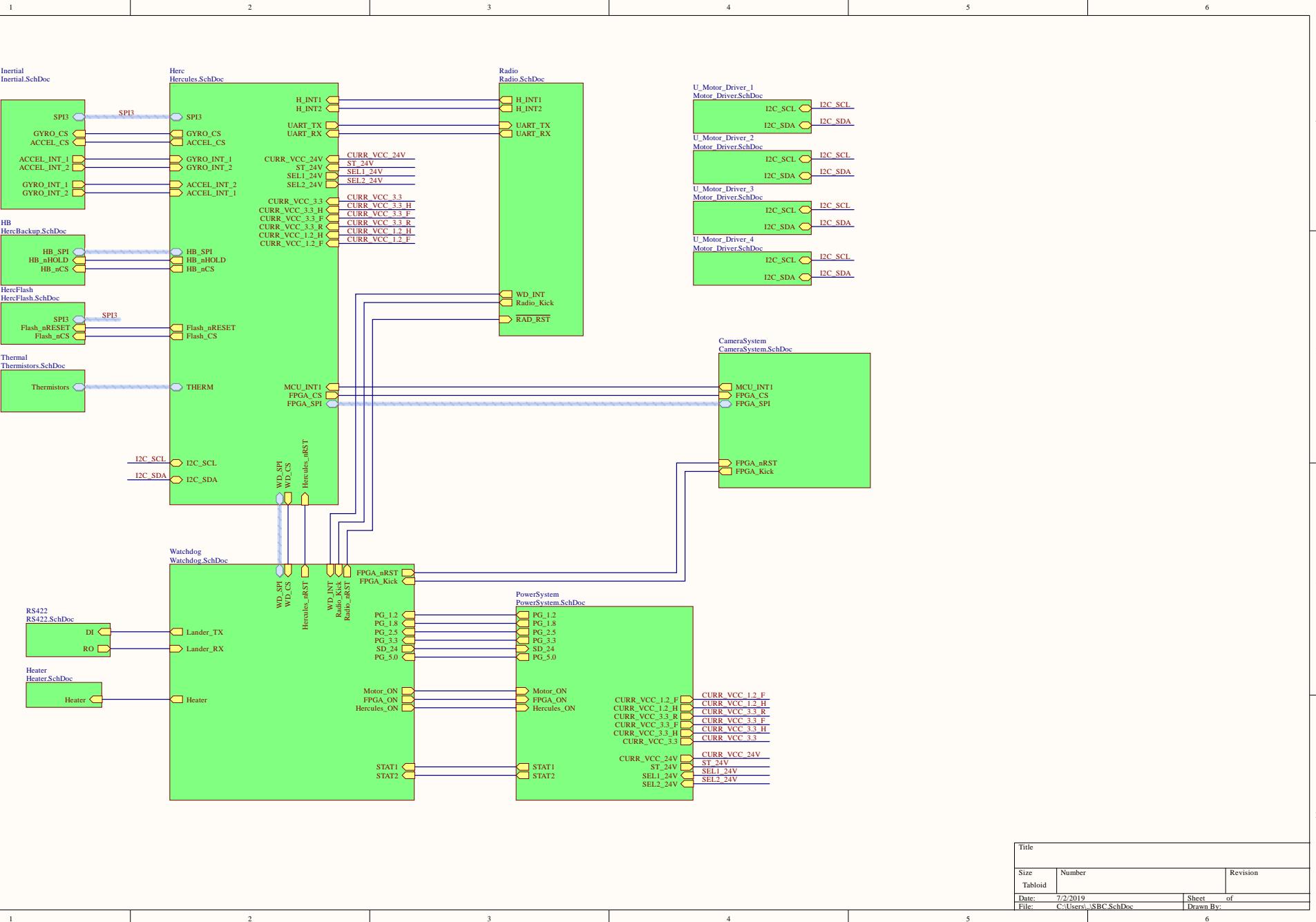
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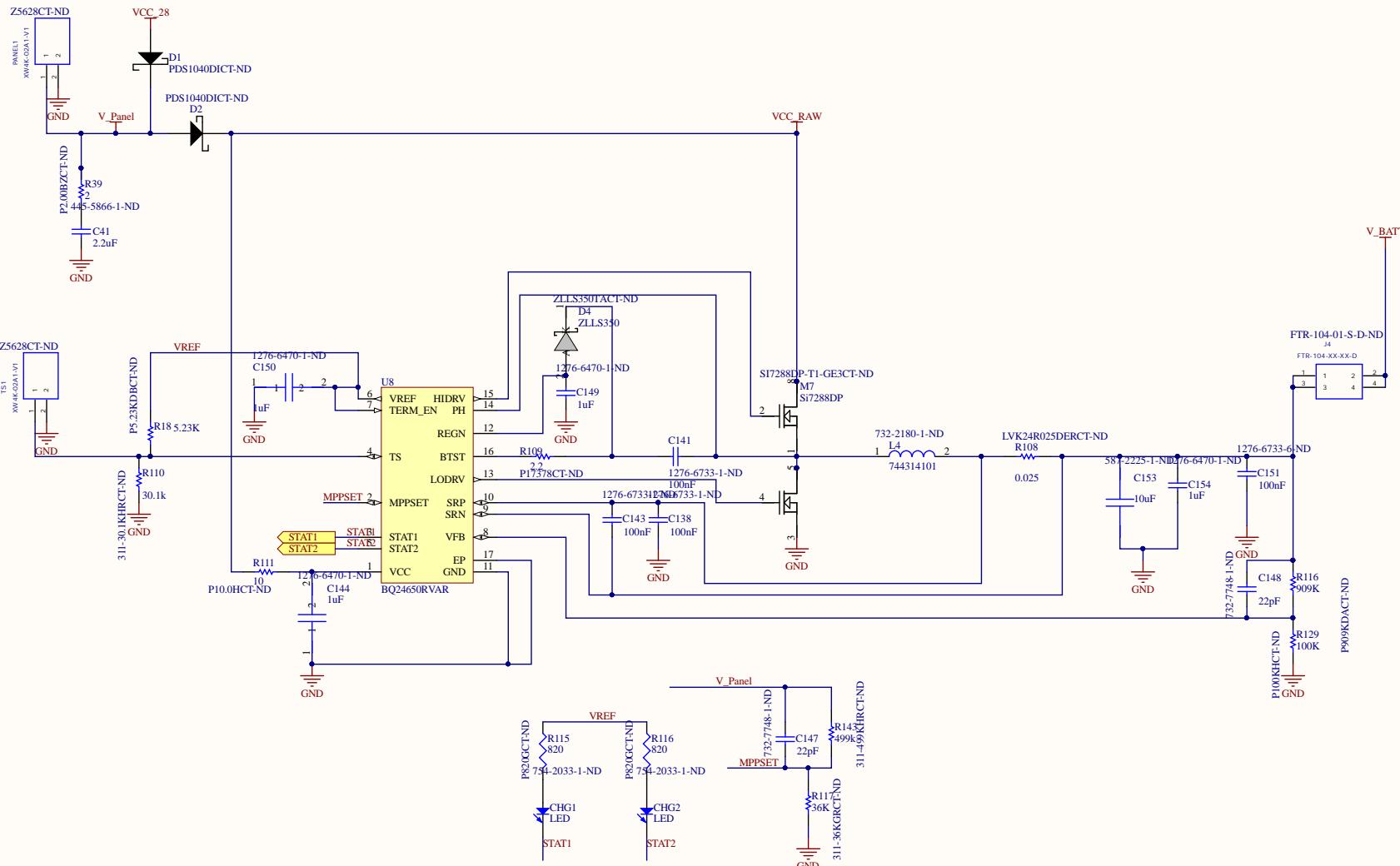
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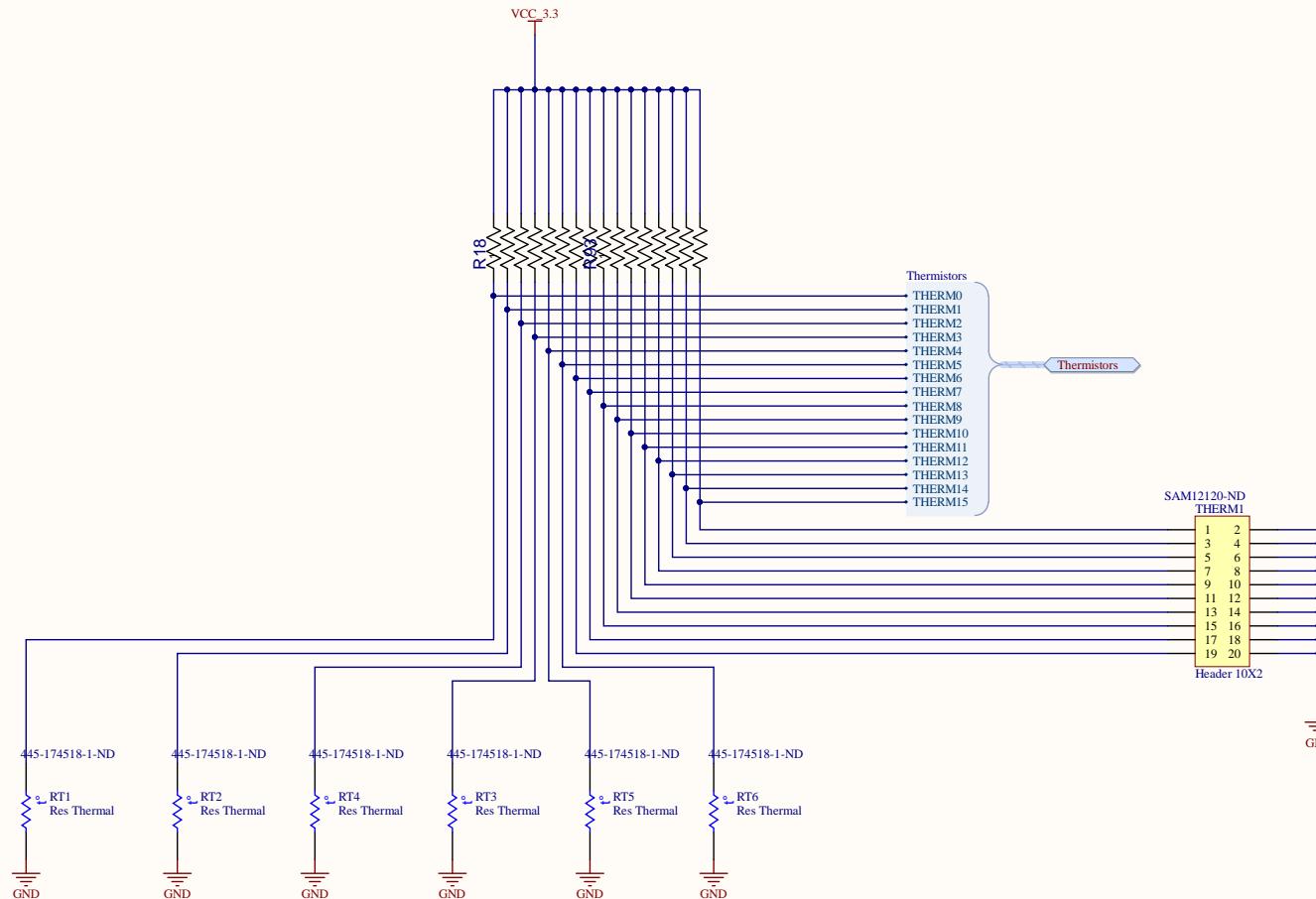
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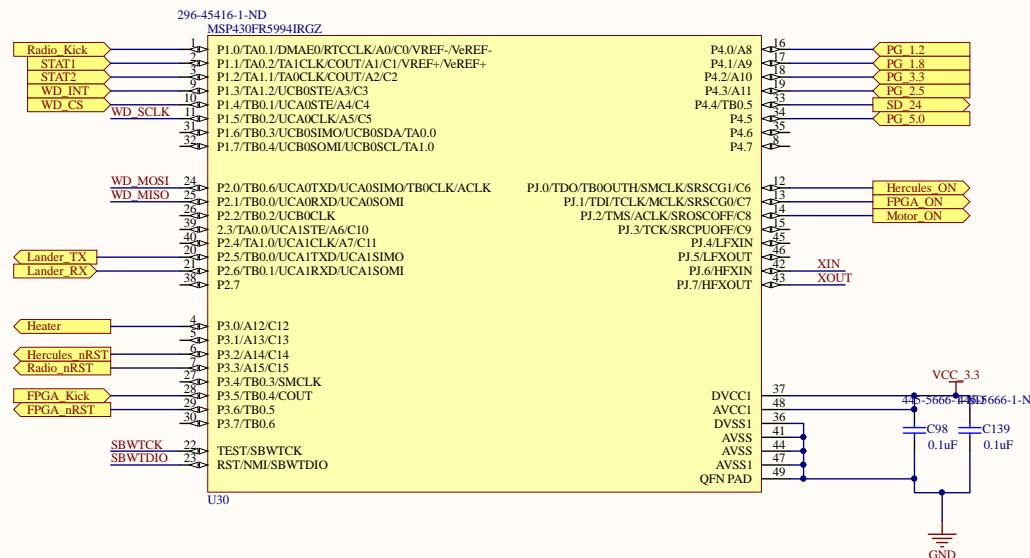
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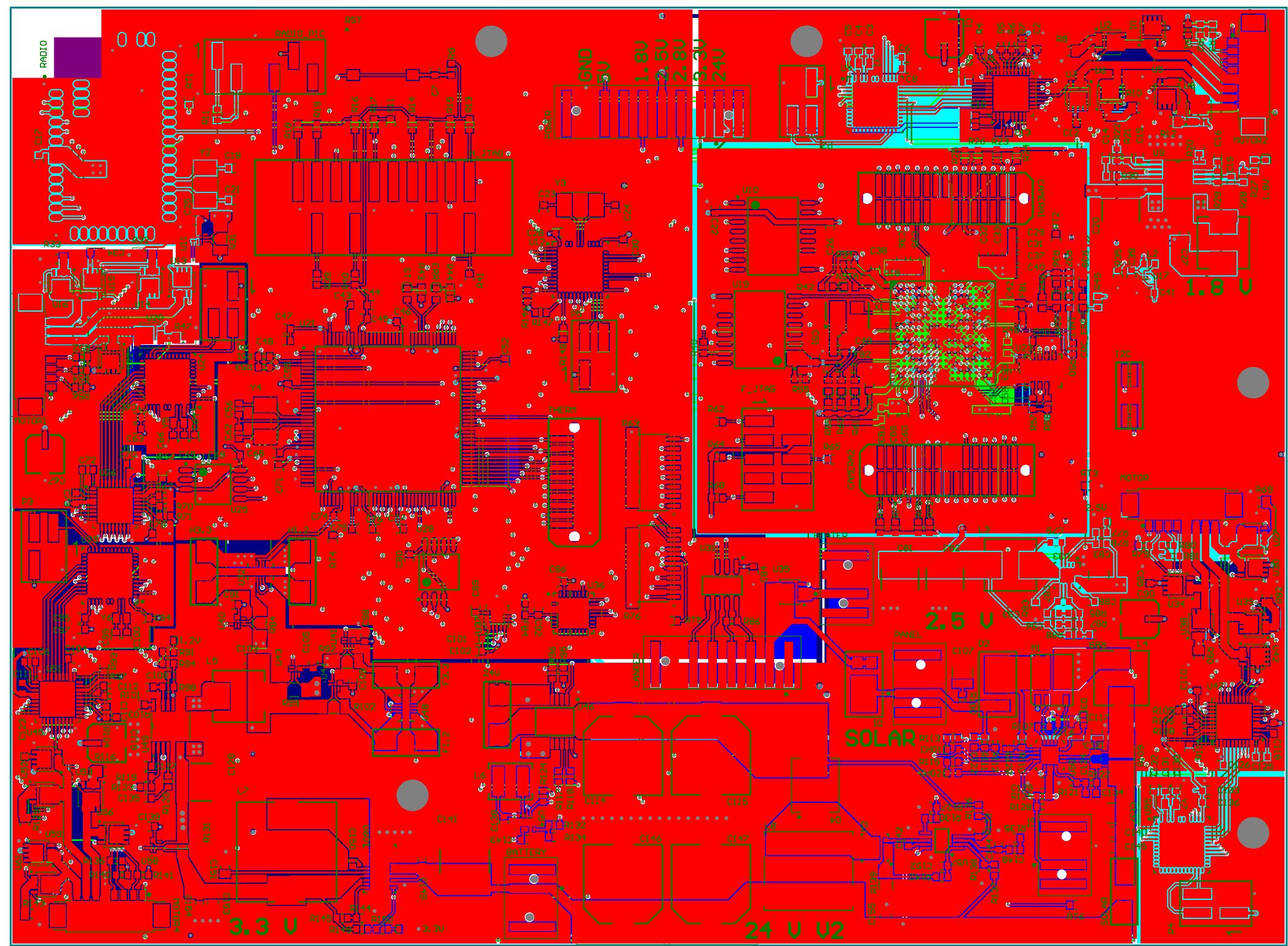
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# Boards