PC Hardware and x86

Dr. Jun Zheng
CSE325 Principles of Operating
Systems
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A PC



☐ How to make it do something userful?

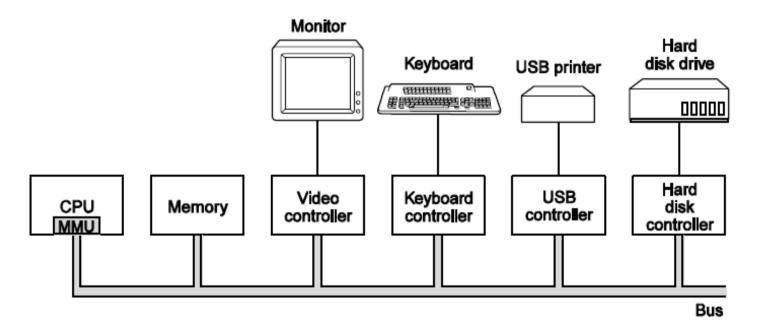
Outline

- □PC architecture
- □x86 Instruction set
- □gcc calling conventions



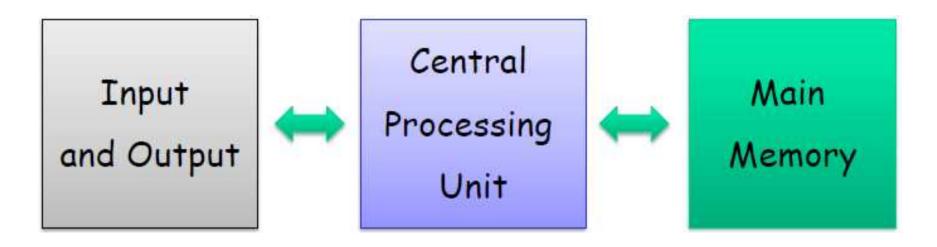
PC Organization

☐ One or more CPUs, memory, and device controllers connect through system bus

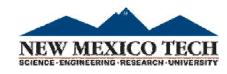




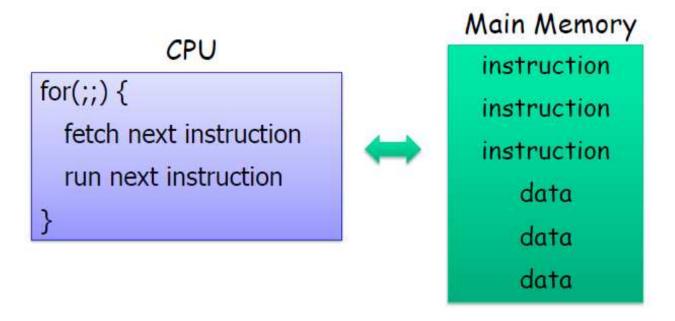
Abstract Model



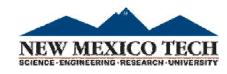
- □I/O: communicating data to and from devices
- □CPU: digital logic for doing computation
- \square Memory: *N* words of *B* bits



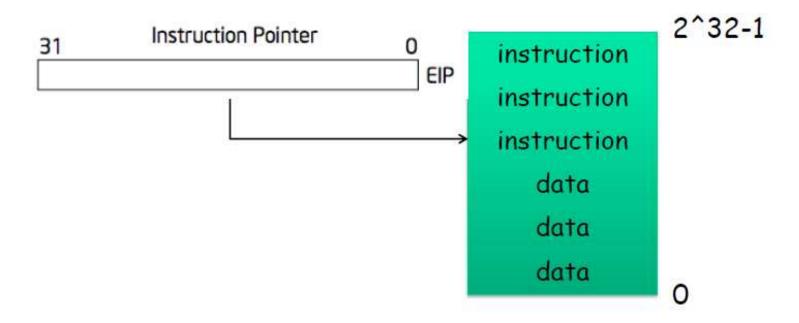
The Stored Prgram Computer



- ☐ Memory holds both instructions and data
- □CPU interprets instructions
- □Instructions read/write data



x86 Implementation



- **DEIP** incremented after each instruction
- □Variable length instructions
- □EIP modified by CALL, RET, JMP, conditional JMP



Registers: Work Space

General-Purpose Registers

31	1615	8 7	0	16-bit	32-bit	
	AH	AL		AX	EAX	
	BH	BL		BX	EBX	ESP: stack pointer
	CH	CL		CX DX	ECX	1945
	DH	DL			EDX	EBP: frame base pointer
	36	BP			EBP	ESI: source index
		SI			ESI	EDI: destination index
	30	DI			EDI	EDI. GOSTINGTION INGOX
	3,6	SP			ESP	

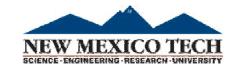
- □8, 16, and 32 bit versions
- □Example: ADD EAX, 10
 - ☐More: SUB, AND, etc.
- □ By convention some for special purposes.

EFLAGS Register

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	D	VIP	V F	AC	V M	R	0	N	I O P L	O F	DF	F	F	SF	Z	0	A	0	D.H.	1	CF
X ID Flag (ID X Virtual Inter X Virtual Inter X Alignment C X Virtual-8086 X Resume Fla X Nested Tas X I/O Privilege S Overflow Fl C Direction Fl X Interrupt En X Trap Flag (T S Sign Flag (S S Zero Flag (Z S Auxiliary Ca S Parity Flag (S Carry Flag (S Carry Flag (S Carry Flag (S S Virtual Interrupt En X Trap Flag (S S Zero Flag (S S Carry Flag (S Car	rruprup ruprup i Mag k (lag lag lag lag (PF) irry (PF	pt Feck loc (RNT ev) (C [le - F])	Per la	end g (Ac (V) (IC)— ag	din (VI ce M))PI (IF	E)-	C	oni	tro	1 (/	AC	:)																	24.		

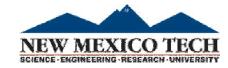
- S Indicates a Status Flag
- C Indicates a Control Flag
- X Indicates a System Flag





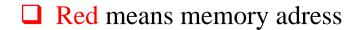
x86 Instructon Set

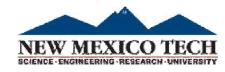
```
☐ Instruction syntax
   □Intel manual Volumne 2: op dst, src
   \squareAT&T (gcc/gas): op src, dst
      □op uses suffix b, w, l for 8, 16, 32-bit operands
      \squarexv6, JOS
□Instruction classes
   □ Data movement: MOV, PUSH, POP, ...
   □Arithmetic: TEST, SHL, ADD, AND, ...
   \squareI/O: IN, OUT, ...
   □Control: JMP, JZ, JNZ, CALL, RET
   □String: MOVSB, REP, ...
   □System: INT, IRET
```



Memory: Addessing Examples

Address	Value	Operand	Value	Comment
0x100	0xFF	%eax	0×100	Value in the register
0x104	0xAB	0x104	0xAB	Vaue is at the address
0×108	0x13	\$0x108	0x108	Value is the value (\$ means immediate, i.e. constant, value)
0x10C	0x11	(%eax)	0xFF	value is at the address stored in the register -> GTV@(reg)
		4(%eax)	oxAB	GTV@(4 + reg)
Register	Value	9(%eax, %edx)	OX11	GTV@(9 + reg + reg)
%eax	0x100	<pre>0xFC(,%ecx, 4)</pre>	0xFF	GTV@(oxFC + o + reg*4)
%ecx	0x1	(%eax, %edx, 4)	0x11	GTV@(reg + reg*4)
%edx	0x3			





Memory: Addressing Modes

```
movl \%eax, \%edx = eax;
                                        register mode
mov1 $0x123, %edx edx = 0x123;
                                        immediate
movl 0x123, %edx edx = *(int32_t*)0x123; direct
movl (%ebx), %edx = *(int32_t*)ebx;
                                       indirect
movl 4(\%ebx), \%edx edx = *(int32_t*)(ebx+4); displaced
☐ Memory instructions: MOV, PUSH, POP,
  etc.
☐ More instructions can take a memory
  address
```

Stack Memory + Operations

Example instruction What it does

pushl %eax subl \$4, %esp

movl %eax, (%esp)

popl %eax movl (%esp), %eax

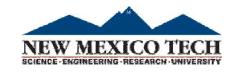
addl \$4, %esp

call 0x12345 pushl %eip (*)

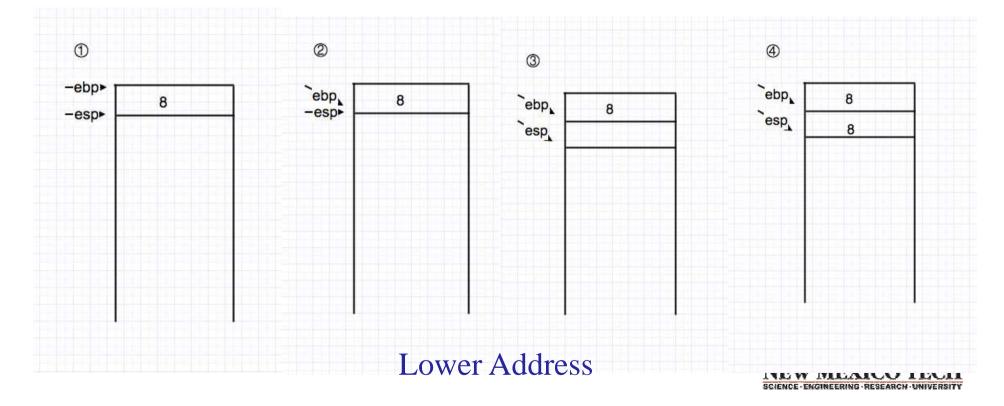
movl \$0x12345, %eip (*)

ret popl %eip (*)

- □ For implementing function calls
- □Stack grows "down" on x86



Stack Operation Example



More Memory

- □8086 16-bit register and 20-bit bus addresses
- ☐ These extra 4 bits come from segment register
 - □CS: code segment, for EIP
 - □Instruction address: CS * 16 + EIP
 - □SS: stack segment, for ESP and EBP
 - DS: data segment for load/store via other registers
 - □ES: another data segment, destination for string ops
- ☐ Make life more complicated
 - □ Cannot directly use 16-bit stack address as pointer
 - ☐ For a far pointer programmer must specify segment reg
 - ☐ Pointer arithmetic and array indexing across seg bound

And More Memory

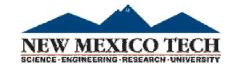
- □80386: 32 bit register and addresses (1985)
- □AMD k8: 64 bit (2003)
 - □ RAX instead of EAX
 - \square x86-64, x64, amd64, intel64: all same thing
- ☐ Backward compatibility
 - ☐ Boots in 16-bit mode; bootasm. S switches to 32
 - ☐ Prefix 0x66 gets 32-bit mode instructions
 - \square MOVW in 32-bit mode = 0x66 + MOVW in 16-bit mode
 - \square .code32 in bootasm. S tells assembler to insert 0x66
- □80386 also added virtual memory addresses



I/O Space and Instructions

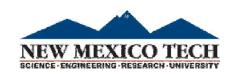
```
#define DATA PORT
                     0x378
#define STATUS PORT
                     0 \times 379
#define BUSY 0x80
#define CONTROL PORT 0x37A
#define STROBE 0x01
void
lpt putc(int c)
  /* wait for printer to consume previous byte */
  while((inb(STATUS PORT) & BUSY) == 0)
  /* put the byte on the parallel lines */
  outb(DATA PORT, c);
  /* tell the printer to look at the data */
  outb(CONTROL PORT, STROBE);
  outb(CONTROL PORT, 0);
```

□8086: only 1024 I/O addresses

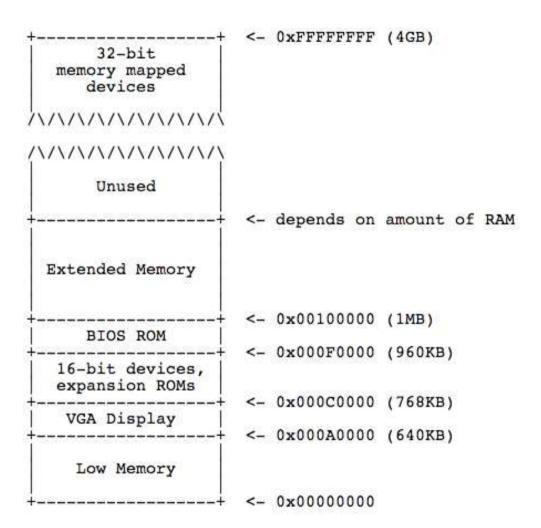


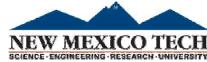
Memory-mapped I/O

- ☐ Use normal addresses for I/O
 - □No special instructions
 - □No 1024 limit
 - ☐ Hardware routes to appropriate device
- ☐Works like "magic" memory
 - □I/O device addressed and accessed like memory
 - ☐ However, reads and writes have "side effects"
 - □Read result can change due to external events



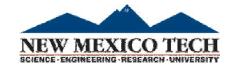
Memory Layout





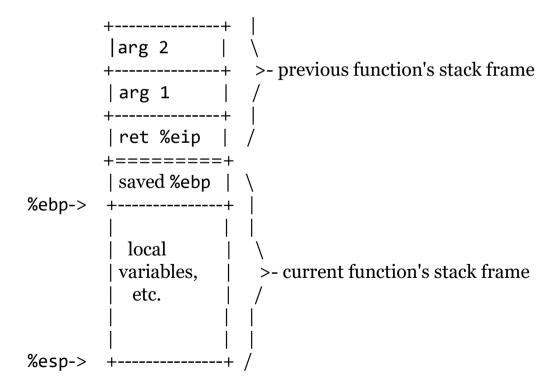
gcc Inline Assembly

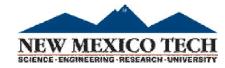
```
☐ Can embed assembly code in C code
   ☐ Many examples in xv6
☐ Basic syntax: asm ("assembly code")
   ☐ e.g., asm ("movl %eax, %ebx")
☐ Advanced syntax:
   asm (assembler template
       : output operands /* optional */
       : input operands /* optional */
       : list of clobbered registers /* optional */ );
   e.g., int val;
        asm ("movl %%ebp,%0" : "=r" (val));
```



gcc Calling Conventions

- ☐ Functions can do anything that doesn't violate contract. By convention, GCC does more:
 - □ each function has a stack frame marked by %ebp, %esp
 - □ %esp can move to make stack frame bigger, smaller
 - □ %ebp points at saved %ebp from previous function, chain to walk stack





gcc Calling Conventions (cont.)

- □%eax contains return value, %ecx, %edx may be trashed
- □64 bit return value: %eax + %edx
- □%ebp, %ebx, %esi, %edi must be as before call
- □Caller saved: %eax, %ecx, %edx
- □Callee saved: %ebp, %ebx, %esi, %edi

