Exercise 1

b) Suppose AMD wants to support virtual address spaces of 512 PB. What changes would need to be made to Figure 5.18? How many different "Page-Map Level-5" tables could then exist for a single process? Read sections 1.1.3 and 5.3.1 and indicate the ranges of canonical addresses for the proposed extension.

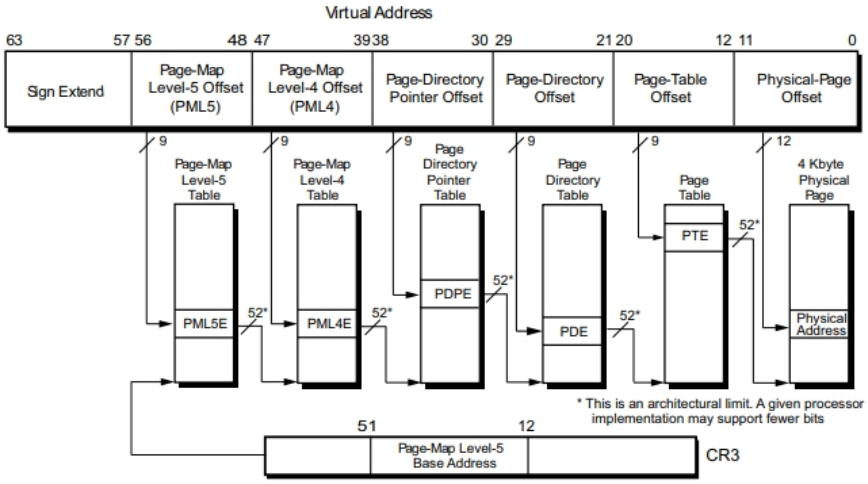


Figure 5-18. 4-Kbyte Page Translation—Long Mode 5-Level Paging

Figure 1: Figure 5.18

1.1.3 Canonical Address Form

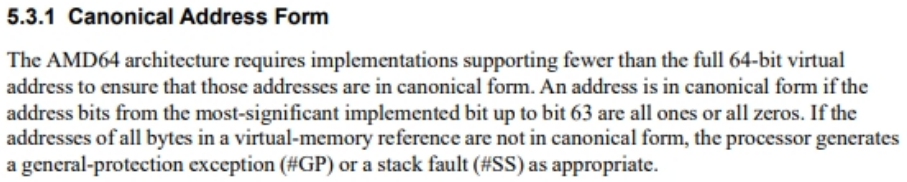
Long mode defines 64 bits of virtual-address space, but processor implementations can support less. Although some processor implementations do not use all 64 bits of the virtual address, they all check bits 63 through the most-significant implemented bit to see if those bits are all zeros or all ones. An address that complies with this property is in *canonical address form*. In most cases, a virtual-memory reference that is not in canonical form (in either the linear or effective form of the address) causes a general-protection exception (#GP) to occur. However, implied stack references where the stack address is not in canonical form causes a stack exception (#SS) to occur. Implied stack references include all push and pop instructions, and any instruction using RSP or RBP as a base register.

By checking canonical-address form, the AMD64 architecture prevents software from exploiting unused high bits of pointers for other purposes. Software complying with canonical-address form on a specific processor implementation can run unchanged on long-mode implementations supporting larger virtual-address spaces.

Figure 2: section 1.1.3

Se quisessemos estender o suporte a 512PB, teriamos de usar 59 bits. 2^{59} = 512PB

Uma das formas de seria cria um *Page-Map Level-6* (PML6) com apenas 2 bits,



5.3.1 Canonical Address Form

The AMD64 architecture requires implementations supporting fewer than the full 64-bit virtual address to ensure that those addresses are in canonical form. An address is in canonical form if the address bits from the most-significant implemented bit up to bit 63 are all ones or all zeros. If the addresses of all bytes in a virtual-memory reference are not in canonical form, the processor generates a general-protection exception (#GP) or a stack fault (#SS) as appropriate.

Figure 3: section 5.3.1

que poderia apontar para 4 *Page-Map Level-5* (PML5) distintas, o que quer dizer que cada processo poderia ter 4 PML5.

Ficariamos assim com:

- 12 bits de offset
- 9 bits de Page-Table Index
- 9 bits de Page-Directory Index
- 9 bits de Page-Directory pointer Index
- 9 bits de Page-Map Level-4
- 9 bits de Page-Map Level-5
- 2 bits de Page-Map Level-6
- 5 bits de extensão do sinal do bit 58:
  - bit 58 a **1 - endereços para kernel mode**
    - do 0xF800 0000 0000 0000 ao 0xFFFF FFFF FFFF FFFF
  - bit 58 a **0 - endereços para user mode**
    - do 0x0000 0000 0000 0000 ao 0x07FF FFFF FFFF FFFF