Industrial Inductive Load Driver

NUD3160, SZNUD3160

This micro−integrated part provides a single component solution to switch inductive loads such as relays, solenoids, and small DC motors without the need of a free−wheeling diode. It accepts logic level inputs, thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

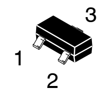
- Provides Robust Interface between D.C. Relay Coils and Sensitive Logic
- Capable of Driving Relay Coils Rated up to 150 mA at 12 V, 24 V or 48 V
- Replaces 3 or 4 Discrete Components for Lower Cost
- Internal Zener Eliminates Need for Free−Wheeling Diode
- Meets Load Dump and other Automotive Specs
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

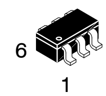
- Automotive and Industrial Environment
- Drives Window, Latch, Door, and Antenna Relays

Benefits

- Reduced PCB Space
- Standardized Driver for Wide Range of Relays
- Simplifies Circuit Design and PCB Layout
- Compliance with Automotive Specifications

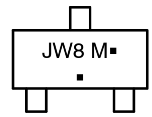


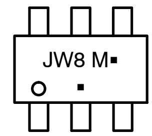
SOT−23
CASE 318
STYLE 21



SC−74
CASE 318F
STYLE 7

MARKING DIAGRAMS





JW8 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

JW8 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

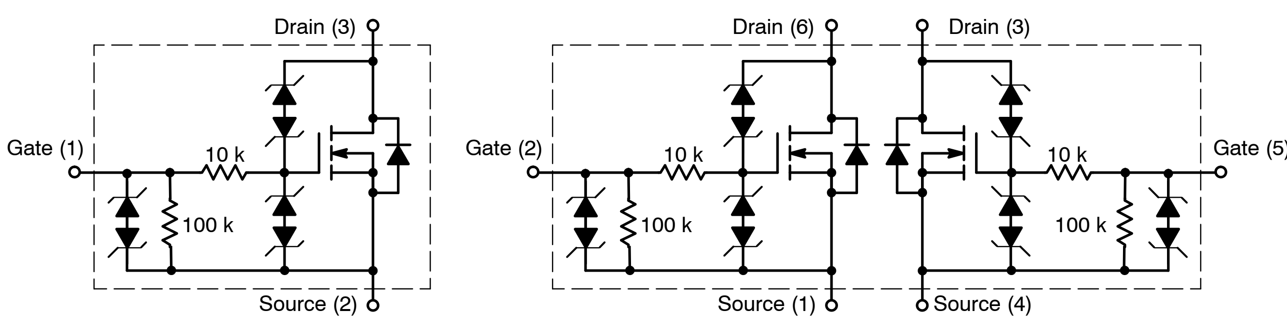
Device	Package	Shipping†
SZNUD3160LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
SZNUD3160DMT1G	SC−74 (Pb−Free)	3000 / Tape & Reel

DISCONTINUED (Note 1)

NU31D60LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
NUD3160DMT1G	SC−74 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



CASE 318 CASE 318F

Figure 1. Internal Circuit Diagrams

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Rating	Value	Unit
V_{DSS}	Drain−to−Source Voltage – Continuous (T_J = 125°C)	60	V
V_{GSS}	Gate−to−Source Voltage – Continuous (T_J = 125°C)	12	V
I_D	Drain Current – Continuous (T_J = 125°C) Minimum copper, double sided board, T_A = 80°C SOT−23 SC74 Single device driven SC74 Both devices driven 1 in^2 copper, double sided board, T_A = 25°C SOT−23 SC74 Single device driven SC74 Both devices driven	 158 157 132 ea 272 263 230 ea	mA
E_Z	Single Pulse Drain−to−Source Avalanche Energy (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	200	mJ
P_{PK}	Peak Power Dissipation, Drain−to−Source (Notes 2 and 3) (T_J Initial = 85°C)	20	W
E_{LD1}	Load Dump Pulse, Drain−to−Source (Note 4) R_{SOURCE} = 0.5 Ω, T = 300 ms) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	60	V
E_{LD2}	Inductive Switching Transient 1, Drain−to−Source (Waveform: R_{SOURCE} = 10 Ω, T = 2.0 ms) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	100	V
E_{LD3}	Inductive Switching Transient 2, Drain−to−Source (Waveform: R_{SOURCE} = 4.0 Ω, T = 50 μs) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	300	V
Rev−Bat	Reverse Battery, 10 Minutes (Drain−to−Source) (For Relay's Coils/Inductive Loads of 80 Ω or more)	−14	V
Dual−Volt	Dual Voltage Jump Start, 10 Minutes (Drain−to−Source)	28	V
ESD	Human Body Model (HBM) According to EIA/JESD22/A114 Specification	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Rating		Value	Unit
T_A	Operating Ambient Temperature		−40 to 125	°C
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		−65 to 150	°C
P_D	Total Power Dissipation (Note 5) Derating above 25°C	SOT−23	225 1.8	mW mW/°C
P_D	Total Power Dissipation (Note 5) Derating above 25°C	SC−74	380 3.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient Minimum Copper 300 mm^2 Copper	 SOT−23 SC−74 One Device Powered SC−74 Both Devices Equally Powered SOT−23 SC−74 One Device Powered SC−74 Both Devices Equally Powered	 556 556 398 395 420 270	°C/W

2. Nonrepetitive current square pulse 1.0 ms duration.
3. For different square pulse durations, see Figure 12.
4. Nonrepetitive load dump pulse per Figure 3.
5. Mounted onto minimum pad board.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain to Source Sustaining Voltage (I_D = 10 mA)	V_{BRDSS}	61	66	70	V
Drain to Source Leakage Current (V_{DS} = 12 V, V_{GS} = 0 V) (V_{DS} = 12 V, V_{GS} = 0 V, T_J = 125°C) (V_{DS} = 60 V, V_{GS} = 0 V) (V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125°C)	I_{DSS}	 – – – –	 – – – –	 0.5 1.0 50 80	μA
Gate Body Leakage Current (V_{GS} = 3.0 V, V_{DS} = 0 V) (V_{GS} = 3.0 V, V_{DS} = 0 V, T_J = 125°C) (V_{GS} = 5.0 V, V_{DS} = 0 V) (V_{GS} = 5.0 V, V_{DS} = 0 V, T_J = 125°C)	I_{GSS}	 – – – –	 – – – –	 60 80 90 110	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1.0 mA) (V_{GS} = V_{DS}, I_D = 1.0 mA, T_J = 125°C)	$V_{GS(th)}$	 1.3 1.3	 1.8 –	 2.0 2.0	V
Drain to Source On−Resistance (I_D = 150 mA, V_{GS} = 3.0 V) (I_D = 150 mA, V_{GS} = 3.0 V, T_J = 125°C) (I_D = 150 mA, V_{GS} = 5.0 V) (I_D = 150 mA, V_{GS} = 5.0 V, T_J = 125°C)	$R_{DS(on)}$	 – – – –	 – – – –	 2.4 3.7 1.8 2.9	Ω
Output Continuous Current (V_{DS} = 0.3 V, V_{GS} = 5.0 V) (V_{DS} = 0.3 V, V_{GS} = 5.0 V, T_J = 125°C)	$I_{DS(on)}$	 150 100	 200 –	 – –	mA
Forward Transconductance (V_{DS} = 12 V, I_D = 150 mA)	g_{FS}	–	400	–	mmho
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	C_{iss}	–	30	–	pf
Output Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	C_{oss}	–	14	–	pf
Transfer Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	C_{rss}	–	6.0	–	pf
SWITCHING CHARACTERISTICS					
Propagation Delay Times: High to Low Propagation Delay; Figure 2, (V_{DS} = 12 V, V_{GS} = 3.0 V) Low to High Propagation Delay; Figure 2, (V_{DS} = 12 V, V_{GS} = 3.0 V) High to Low Propagation Delay; Figure 2, (V_{DS} = 12 V, V_{GS} = 5.0 V) Low to High Propagation Delay; Figure 2, (V_{DS} = 12 V, V_{GS} = 5.0 V)	 t_{PHL} t_{PLH} t_{PHL} t_{PLH}	 – – – –	 918 798 331 1160	 – – – –	ns
Transition Times: Fall Time; Figure 2, (V_{DS} = 12 V, V_{GS} = 3.0 V) Rise Time; Figure 2, (V_{DS} = 12 V, V_{GS} = 3.0 V) Fall Time; Figure 2, (V_{DS} = 12 V, V_{GS} = 5.0 V) Rise Time; Figure 2, (V_{DS} = 12 V, V_{GS} = 5.0 V)	 t_f t_r t_f t_r	 – – – –	 2290 618 622 600	 – – – –	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL WAVEFORMS

(T_J = 25°C unless otherwise specified)

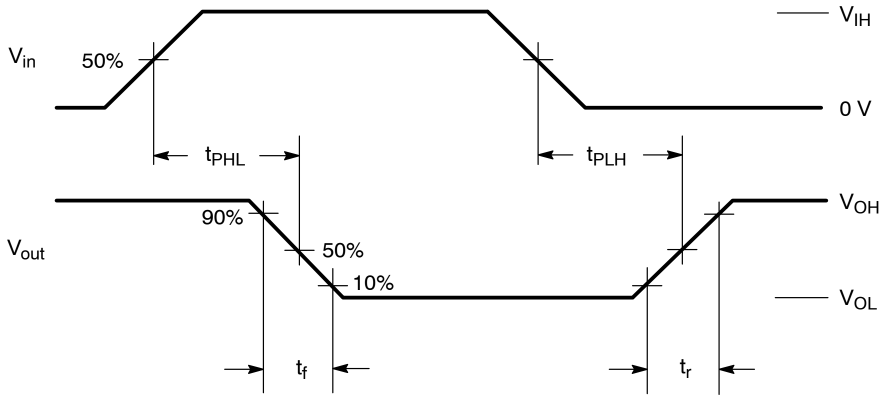


Figure 2. Switching Waveforms

Load Dump Pulse Not Suppressed:

V_r = 13.5 V Nominal ±10%
V_S = 60 V Nominal ±10%
T = 300 ms Nominal ±10%
t_r = 1 − 10 ms ±10%

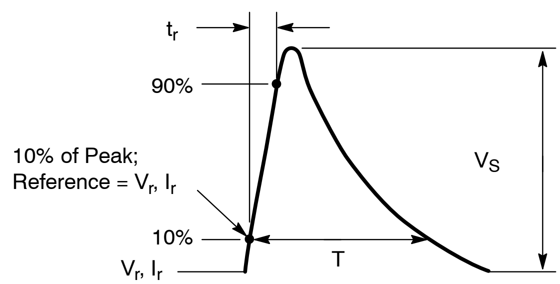


Figure 3. Load Dump Waveform Definition

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise specified)

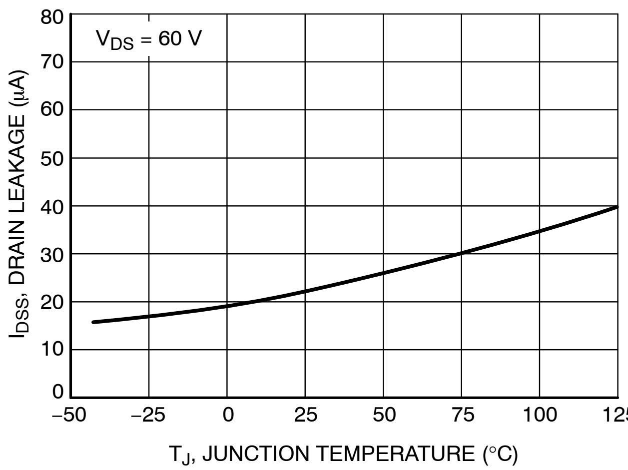


Figure 4. Drain−to−Source Leakage vs. Junction Temperature

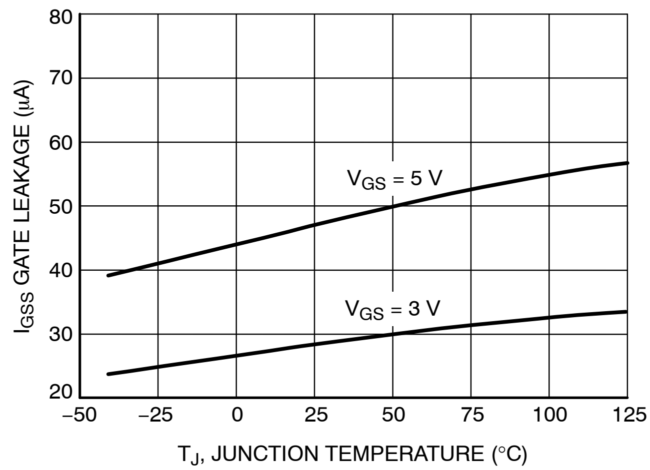


Figure 5. Gate−to−Source Leakage vs. Junction Temperature

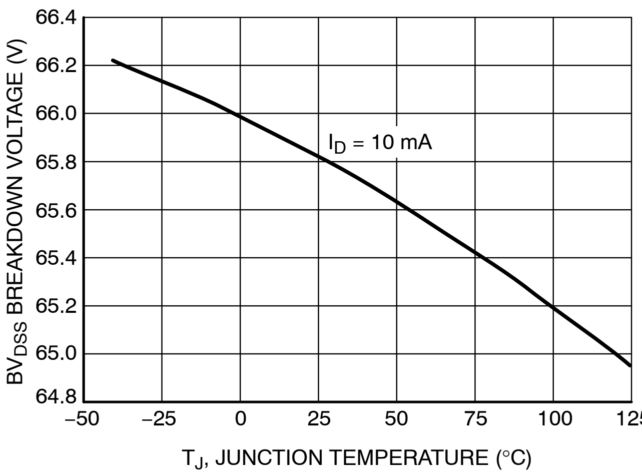


Figure 6. Breakdown Voltage vs. Junction Temperature

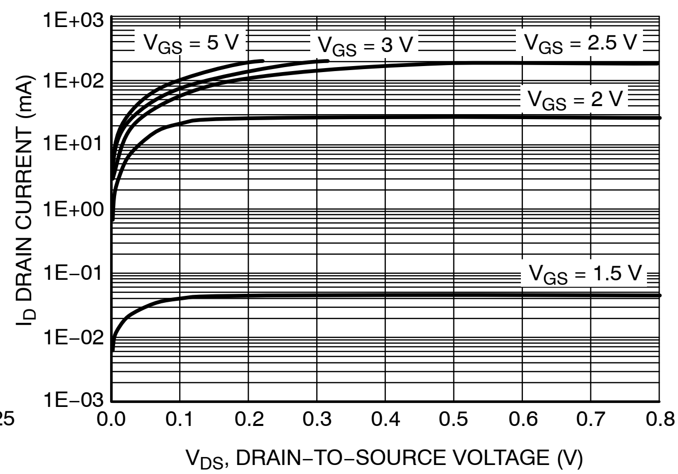


Figure 7. Output Characteristics

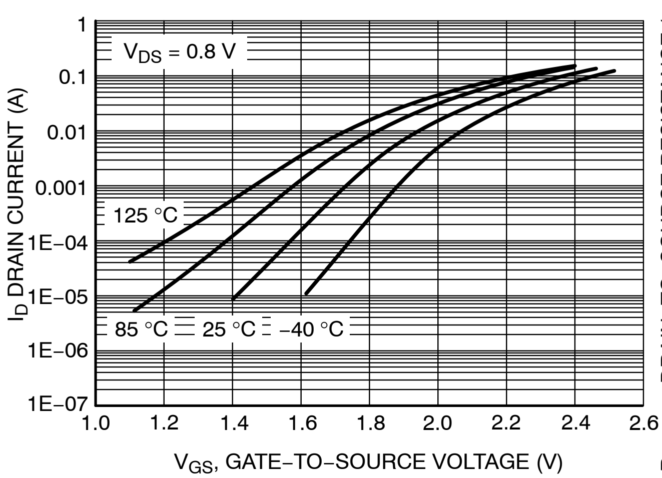


Figure 8. Transfer Function

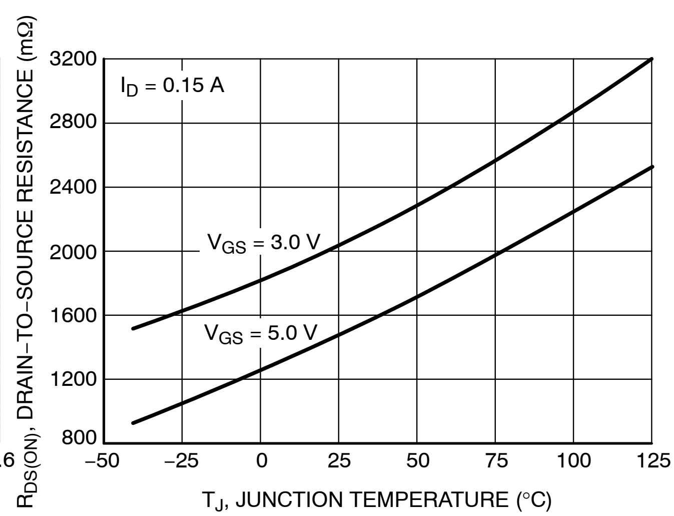


Figure 9. On Resistance Variation vs Junction Temperature

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise specified)

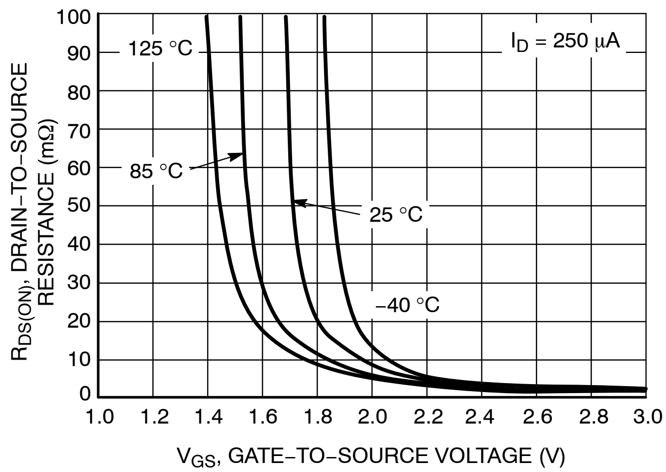


Figure 10. On Resistance Variation vs. Gate−to−Source Voltage

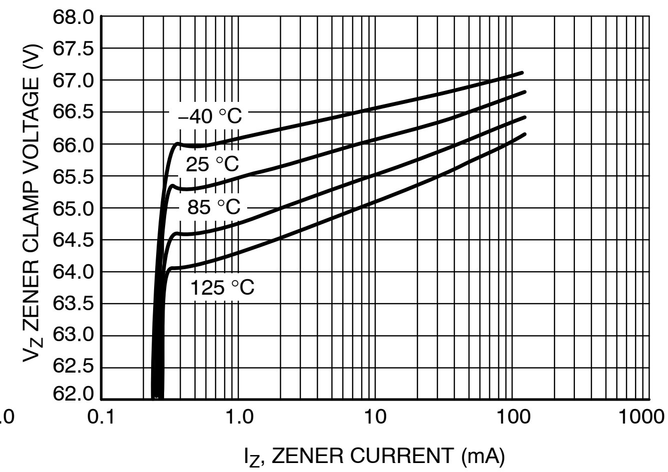


Figure 11. Zener Clamp Voltage vs. Zener Current

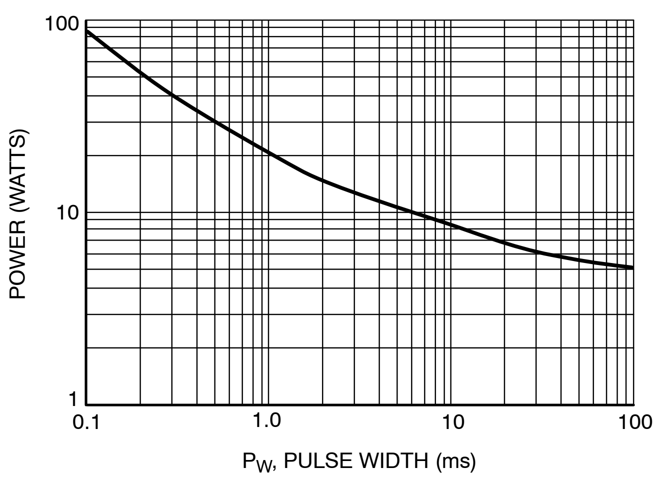


Figure 12. Maximum Non−repetitive Surge Power vs. Pulse Width

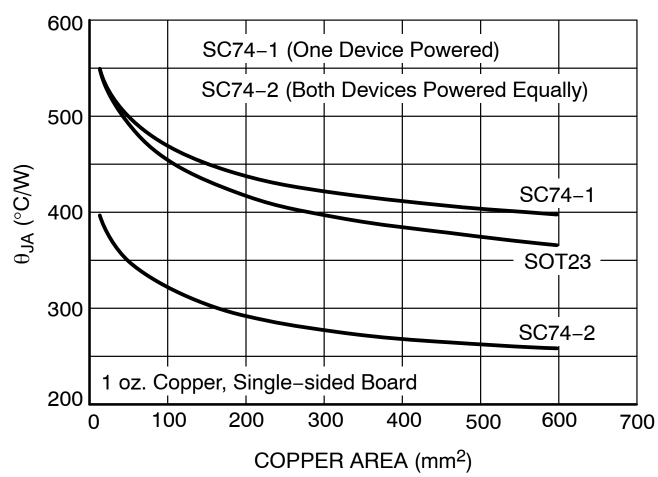


Figure 13. Thermal Performance vs. Board Copper Area

APPLICATIONS INFORMATION

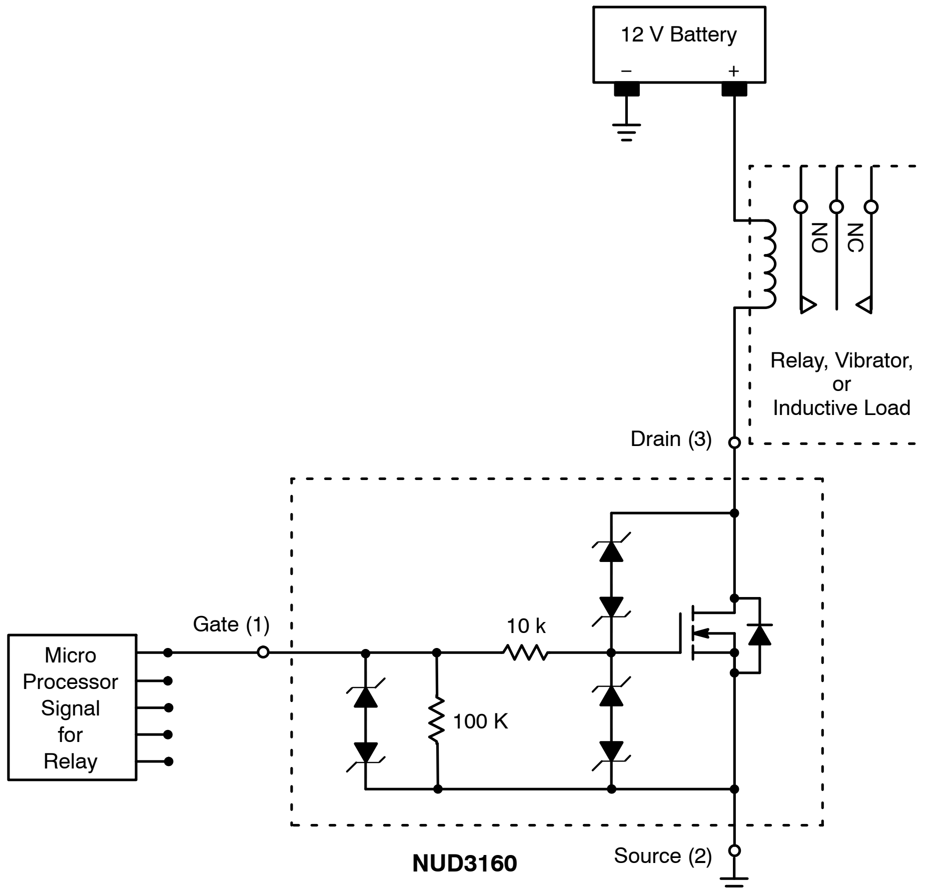
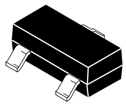


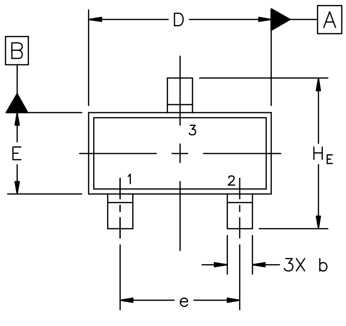
Figure 14. Applications Diagram



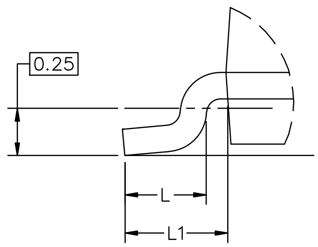
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

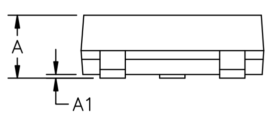
DATE 14 AUG 2024



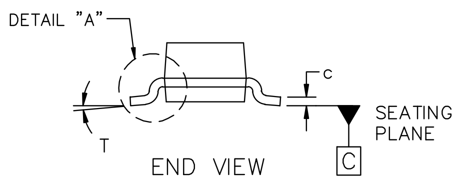
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

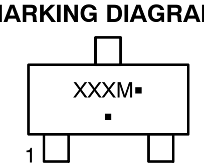


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

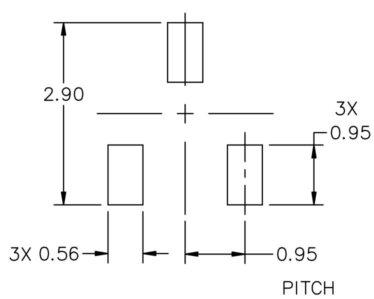
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**	**PAGE 1 OF 2**

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

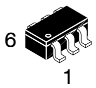
STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

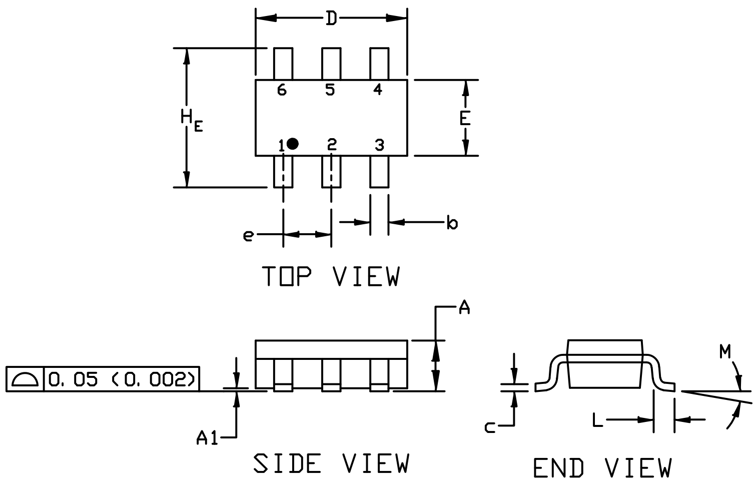
DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**	**PAGE 2 OF 2**



SCALE 2:1

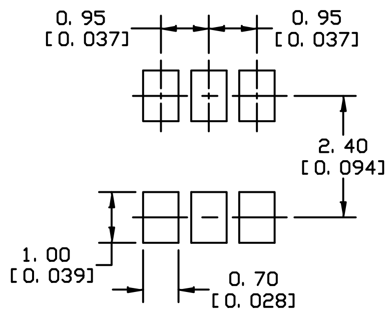
SC−74
CASE 318F
ISSUE P

DATE 07 OCT 2021



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

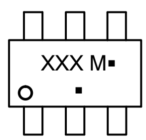
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
H_E	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0°	---	10°	0°	---	10°



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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