# TC5020BP

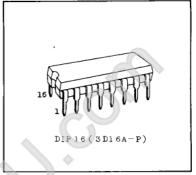
TC5020BP HEX LOW-TO-HIGH VOLTAGE TRANSLATOR (INVERTING)

TC5020BP contains six circuits of level converters which convert the signals from low power supply voltage logical systems to the logical signals for high power supply voltage C2MOS systems.

This is most suitable for interfacing between TTL, MDTL systems and C2MOS systems, and between two power supply voltage C2MOS systems.

Normally, VCC is connected to low voltage power supply and VDD is connected to high voltage power supply, however this can also operate having VCC and VDD common.

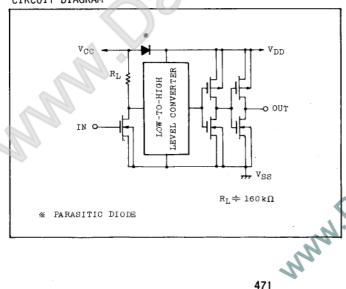
When the input is "H", some amount of ICC flows because of circuit structure.



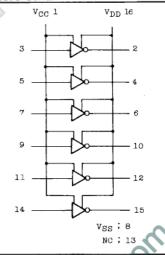
#### ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$v_{DD}$	$V_{SS}-0.5 \sim V_{SS}+20$	V
bo suppry vortage	V <sub>CC</sub>	$V_{SS}-0.5 \sim V_{DD}+0.5$	v
Input Voltage	VIN	V <sub>SS</sub> -0.5~V <sub>CC</sub> +0.5	v
Output Voltage	VOUT	Vss-0.5 ~ VDD+0.5	V
DC Input Current	IIN	±10	mA
Power Dissipation	PD	300	mW
Storage Temperature Range	Tstg	−65 ~ 150	°c
Lead Temp./Time	Tso1	260°C · 10sec	•

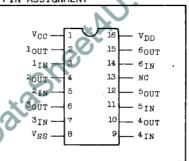
#### CIRCUIT DIAGRAM



#### LOGIC DIAGRAM



### PIN ASSIGNMENT



## RECOMMENDED OPERATING CONDITIONS (VSS=0V)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage (1)	V <sub>CC</sub>	$v_{CC} = v_{DD}$	3	-	18	V
Supply Voltage (2)	VCC	$v_{CC} < v_{DD}$	5	-	$v_{ m DD}$	v
Supply Voltage (2)	$v_{ m DD}$	\cc < \np	5	_	18	· ·
Input Voltage	VIN		0	-	VCC	v
Operataing Temp.	Topr		-40	-	85	°C

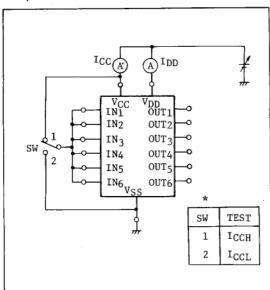
# ELECTRICAL CHARACTERISTICS (VSS=0V, VCC=VDD)

CHARACTERISTIC	SYMBOL	TEST	V <sub>DD</sub>			25°C			85°C		UNIT
011111111111111111111111111111111111111		CONDITIONS	(V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	v <sub>OH</sub>	I <sub>OUT</sub>   < 1µA   V <sub>IN</sub> = V <sub>SS</sub>	5 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.00 10.00 15.00	- - -	4.95 9.95 14.95	- - -	V
Low Level Output Voltage	VOL	ابرا >ا I <sub>OUT</sub> V <sub>IN</sub> = V <sub>DD</sub>	5 10 15	1 1 1	0.05 0.05 0.05	- - -	0.00 0.00 0.00	i .	- - -	0.05 0.05 0.05	
High Level Output Current	IOH	V <sub>OH</sub> = 4.6V V <sub>OH</sub> = 9.5V V <sub>OH</sub> = 13.5V V <sub>IN</sub> = V <sub>SS</sub>	5 10 15	-0.2 -0.5 -1.4		-0.16 -0.4 -1.2		- - -	-0.12 -0.3 -1.0	- - -	mA
Low Level Output Current	$I_{ m OL}$	V <sub>OL</sub> = 0.4V V <sub>OL</sub> = 0.5V V <sub>OL</sub> = 1.5V V <sub>IN</sub> = V <sub>DD</sub>	5 10 15	0.52 1.3 3.6	- - -	0.44 1.1 3.0		- - -	0.36 0.9 2.4	- - -	
High Level Input Voltage	v <sub>IH</sub>	V <sub>OUT</sub> = 0.5V V <sub>OUT</sub> = 1.0V V <sub>OUT</sub> = 1.5V   I <sub>OUT</sub>   < 1µA	5 10 15	4.0 7.0 10.0	- - -	4.0 7.0 10.0		- - -	4.0 7.0 10.0	- - -	v
Low Level Input Voltage	VIL	V <sub>OUT</sub> = 4.5V V <sub>OUT</sub> = 9.0V V <sub>OUT</sub> = 13.5V   I <sub>OUT</sub>   < 1µA	5 10 15		1.0 1.2 1.5	- -		1.0 1.2 1.5	- - -	1.0 1.2 1.5	
Input H Level	IIH	V <sub>IH</sub> = 18V	18	-	0.3	-	10-5	0.3	-	1.0	Aιι
Current L Level	IIL	$V_{IL} = 0V$	18	-	-0.3	-	-10-5	-0.3	-	-1.0	
Quiescent Current Consumption	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>SS</sub> ,V <sub>DD</sub>	5 10 15	- - -	1.0 2.0 4.0	-	0.001 0.001 0.002	1.0 2.0 4.0	1	7.5 15.0 30.0	Αις
Quiescent Current Consumption	тссн	VIN = VDD	5 10 15	-	0.9 1.6 2.1	-	0.2 0.4 0.6	0.48 0.96 1.5	1 1 1,	0.9 1.6 2.1	mA
Quiescent Current Consumption	ICCL	VIN = VSS	5 10 15	- - -	1.0 2.0 4.0	- - -	0.001 0.001 0.002	1.0 2.0 4.0		7.5 15.0 30.0	ДLA

<sup>\*</sup> All valid input combinations

CHARACTERISTIC	SYMBOL	CONDITIONS	VCC(V)	VDD(V)	MIN.	TYP.	MAX.	UNIT	
Output Rise Time	tTLH		- -	5 10 15	1 1	130 65 50	400 200 160	ns	
Output Fall Time	t <sub>THL</sub>		- - -	5 10 15	- - -	100 50 40	200 100 80		
(LOW-HIGH) Propagation Delay Time	t <sub>p</sub> LH		5 10 15	5 10 15	- - -	780 330 230	1600 800 600		
		5 5 10	10 15 15	- - -	750 850 330	1600 1800 800	ns		
(HICH-LOW) Propagation Delay Time	tpHL		5 10 15	5 10 15	- - -	220 75 50	600 300 200		
		5 5 10	10 15 15	-	130 150 60	300 400 200			
Input Capacity	CIN				-	5	7.5	pF	

IDD, ICC TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT AND WAVEFORM

