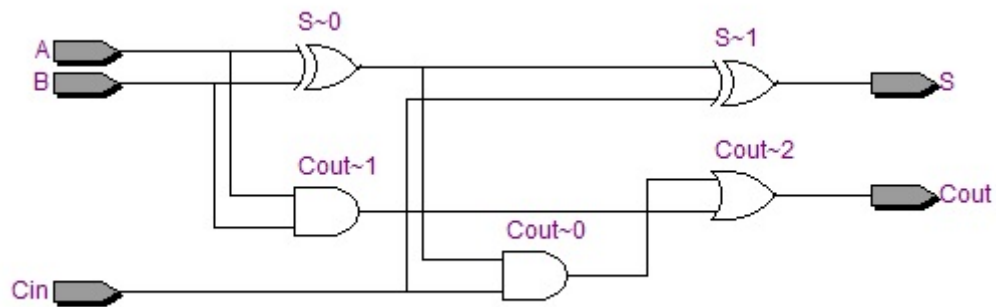
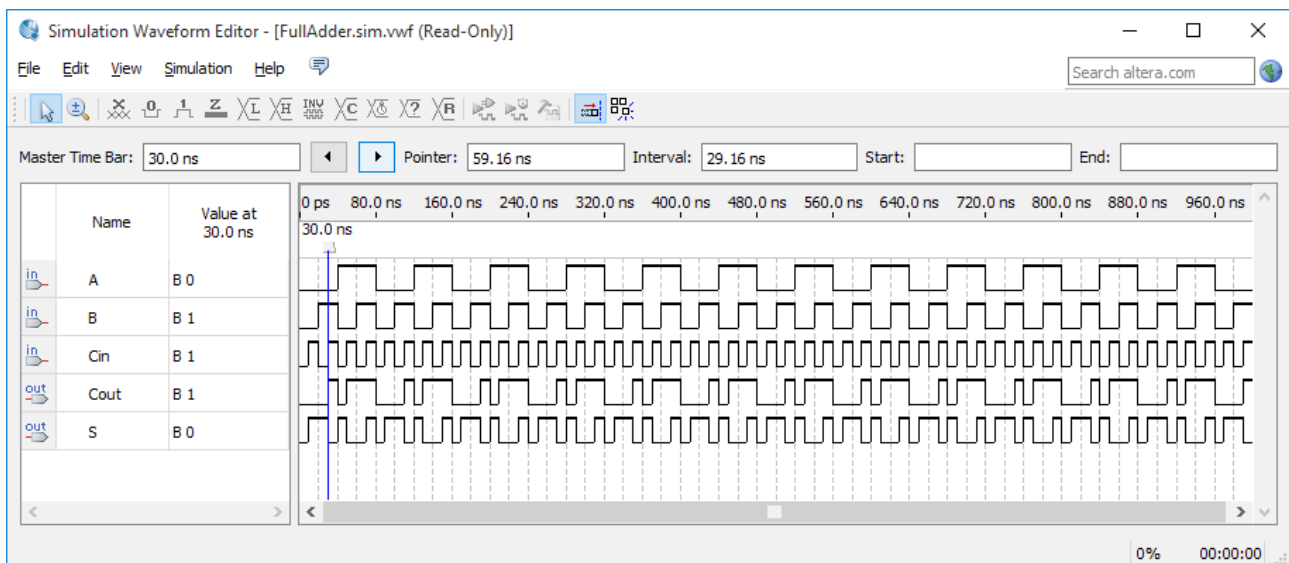


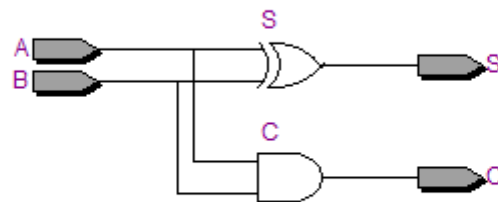
## Register Transfer Logic Diagram of Full Adder:



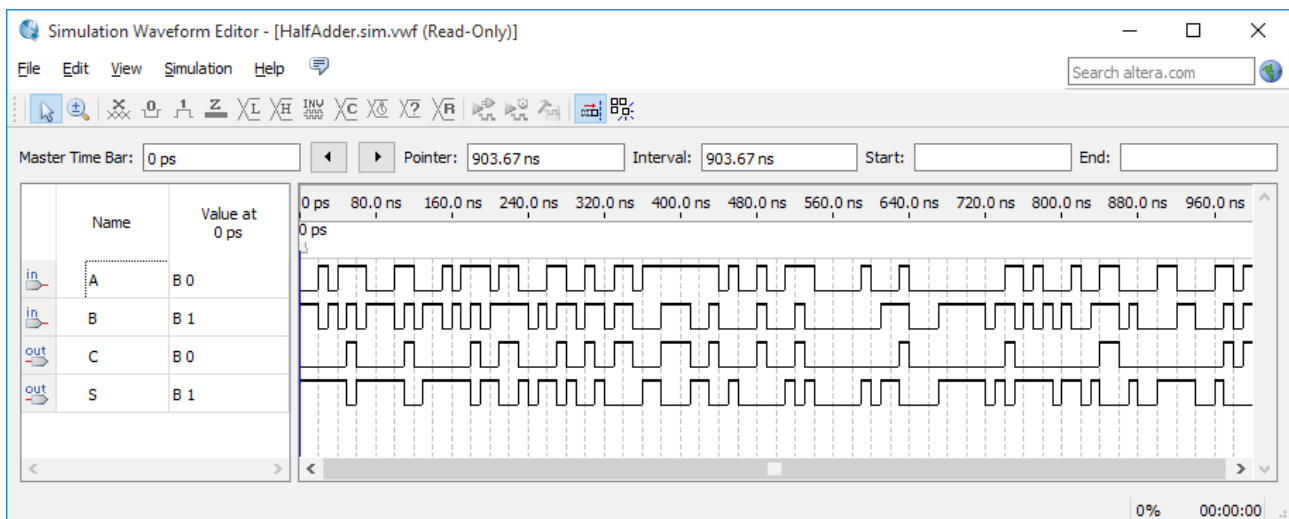
## Output Waveform of Full Adder:



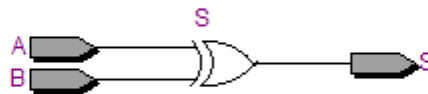
## Register Transfer Logic Diagram of Half Adder:



## Output Waveform of Half Adder:



## Register Transfer Logic Diagram of XOR Gate:



## Output Waveform of XOR Gate:

