COMPUTER ARCHITECTURE LAB EXPERIMENTS AND ASSIGNMENTS (CS 493)		
HARDWARE USED: Desktop PC, Altera DE 1and Spartan-6. **SOFTWARE USED** : Quartus II (Version 13.0)		
Weeks	**Experiment No.**	**Name of the Experiment**
Week 1	*Introduction about VHDL Coding and its syntax and Design using Dataflow Modeling.*	
	Lab Work	
	Experiment 1.1	Procedure for designing and simulating an AND/XOR gate.
	Experiment 1.2	Design Half adder.
	Home Work	
	Assignment 1.1	Design Full Adder
Week 2	*Design Circuits using Behavioral Modeling using "signal".*	
	Lab Work	
	Experiment 2.1	Design Half Subtractor.
	Experiment 2.2	Design a Magnitude comparator of two bit data
	Home Work	
	Assignment 2.1	Design Full Subtractor.
Week 3	*Introduction of condition Statement "If Else" to design architecture using Behavioral Modeling in VHDL and Verify the waveform.*	
	Lab Work	
	Experiment 3.1	Design Multiplexer (8:1).
	Home Work	
	Assignment 3.1	Design Encoder (8 to 3).
Week 4	*Introduction of condition Statement "When Else" to design architecture using Behavioural Modeling in VHDL and Verify the waveform.*	
	Lab Work	
	Experiment 4.1	Design Decoder (3 to 8).
	Home Work	
	Assignment 4.1	Design (1: 8) Demultiplexer.
Week 5	*Introduction to sequential circuits using "variable" in Behavioural modeling in VHDL and verify the waveform.*	
	Lab Work	
	Experiment 5.1	Design J-K flip flop in VHDL.
	Experiment 5.2	Design S-R flip flop in VHDL .
	Home Work	
	Assignment 5.1	D flip flop in VHDL.
	Assignment 5.2	Design J-K based Master-slave flip flop in VHDL.
Week 6	*Introduction to FPGA hardware and implement the VHDL code within the Development FPGA Board.*	
	Lab Work	
	Experiment 6.1	Design and implement the code in FPGA for BCD to 7-segment display converter.
	Home Work	
	Assignment 6.1	Design and implement the code in FPGA for a binary to gray code converter.

Week 7	*Design registers using sequential building blocks and implement it on FPGA development board.*	
	Lab Work	
	Experiment 7.1	Design Serial Input Parallel output shift register and implement it on Altera DE1.
	Home Work	
	Assignment 7.1	Design Parallel Input Serial output shift register.
Week 8	*Design registers using sequential building blocks and implement it on FPGA development board.*	
	Lab Work	
	Experiment 8.1	Design Parallel Input Parallel output shift register and implement it on Altera DE1.
	Home Work	
	Assignment 8.1	Design Serial Input Serial output shift register.
Week 9	*Design 4-bit Arithmetic Logic Unit using VHDL and implement it on FPGA development board.*	
	Lab Work	
	Experiment 9.1	Design 4-bit ALU for 8 operations with mode line.
	Home Work	
	Assignment 9.1	Design 8-bit Arithmetic Logic Unit with 16/32 operations with mode line.
Week 10	*Design 4/8-bit Central Processing Unit (CPU) using VHDL and implement it on FPGA development board.*	
	Lab Work	
	Experiment 10.1	Design a SRAM memory unit in VHDL to perform read/write operations.
	Home Work	
	Assignment 10.1	Code for 4/8-bit simple CPU.
	Assignment 10.2	Code to interface the memory with the CPU.
LIST OF ADDITIONAL EXPERIMENTS TO MEET POs AND PEOs		
Week 1-10	**Micro Project Topics**	Project works using VHDL on FPGA platform.