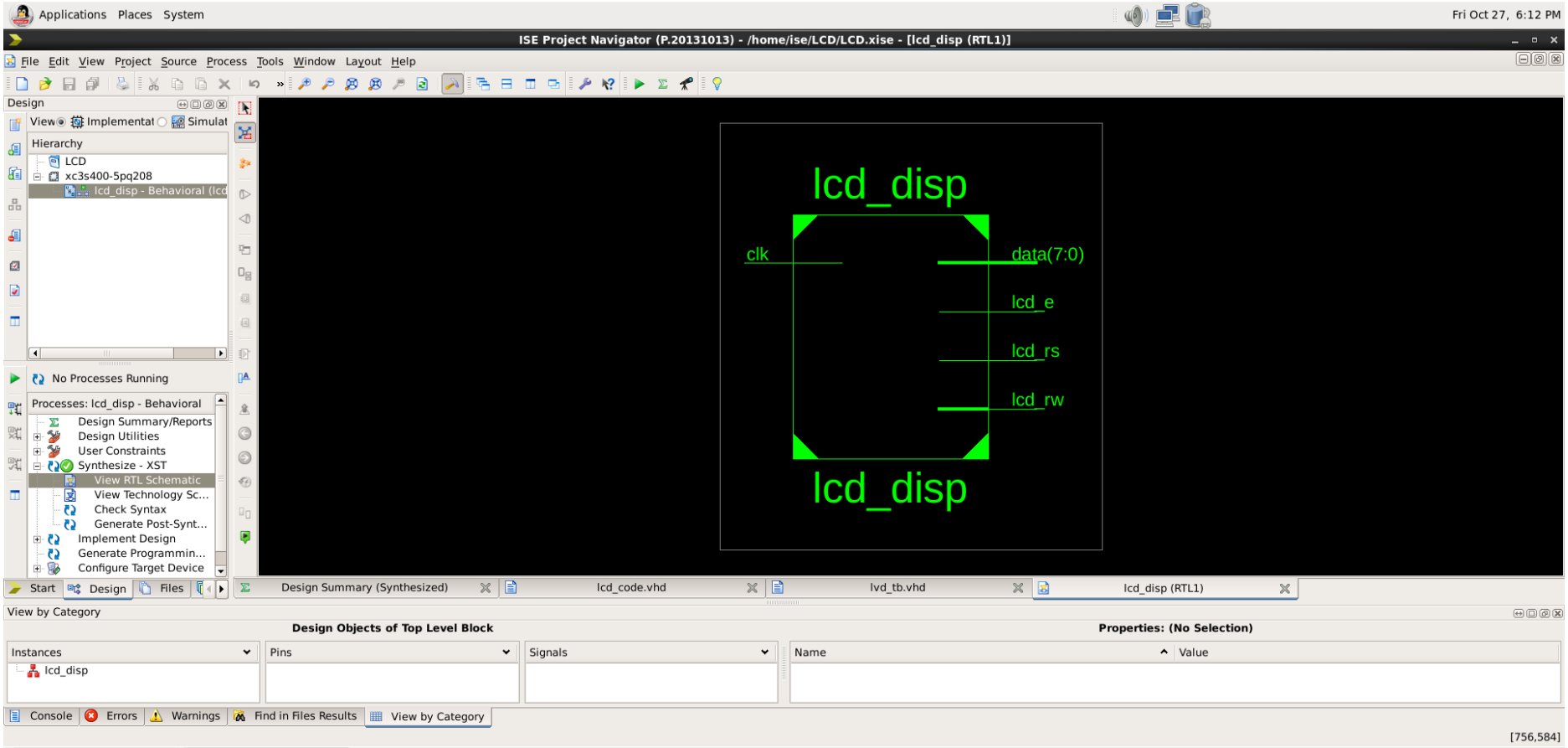
CODE

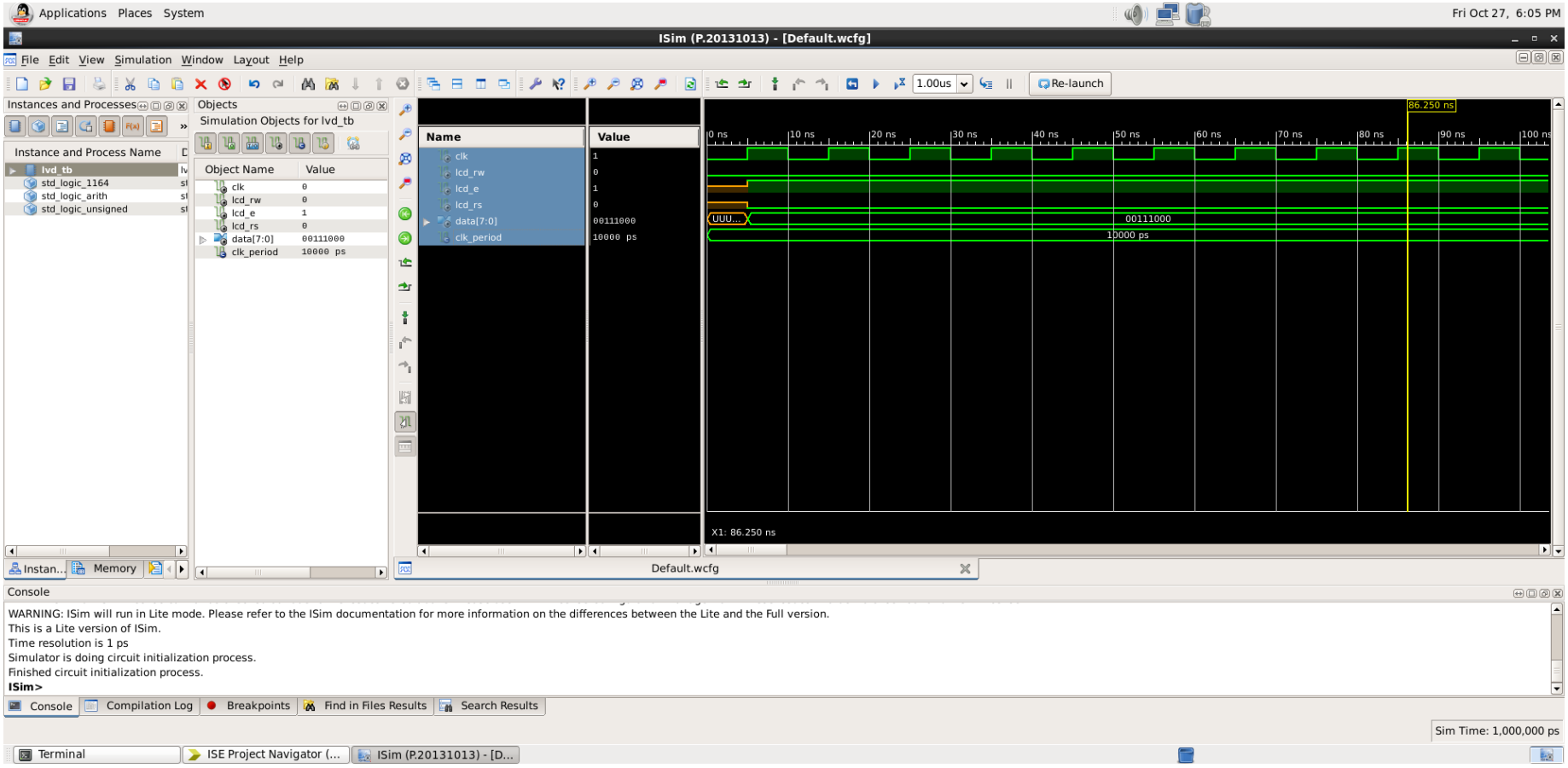
```
----------------------------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY lcd_disp IS
	PORT (
		clk : IN std_logic; ----clock i/p
		lcd_rw : OUT std_logic; ---read&write control
		lcd_e : OUT std_logic; ----enable control
		lcd_rs : OUT std_logic; ----data or command control
	data : OUT std_logic_vector(7 DOWNTO 0)); ---data line
END lcd_disp;

ARCHITECTURE Behavioral OF lcd_disp IS
	CONSTANT N : INTEGER := 12;
	TYPE arr IS ARRAY (1 TO N) OF std_logic_vector(7 DOWNTO 0);
	CONSTANT datas : arr :=(X"38", X"0c", X"06", X"01", X"C0", X"50", x"41", x"42", x"43", x"44",
x"45", x"53"); --command AND data TO display
BEGIN
	lcd_rw <= '0'; ----lcd write
	PROCESS (clk)
	VARIABLE i : INTEGER := 0;
	VARIABLE j : INTEGER := 1;
	BEGIN
		IF clk'EVENT AND clk = '1' THEN
			IF i <= 1000000 THEN
				i := i + 1;
				lcd_e <= '1';
				data <= datas(j)(7 DOWNTO 0);
			ELSIF i > 1000000 AND i < 2000000 THEN
				i := i + 1;
				lcd_e <= '0';
			ELSIF i = 2000000 THEN
				j := j + 1;
				i := 0;
			END IF;
			IF j <= 5 THEN
				lcd_rs <= '0'; ---command signal
			ELSIF j > 5 THEN
				lcd_rs <= '1'; ----data signal
			END IF;
			IF j = 12 THEN ---repeated display of data
				j := 5;
			END IF;
		END IF;
	END PROCESS;
END Behavioral;
```

TESTBENCH

```
--------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY lvd_tb IS
END lvd_tb;

ARCHITECTURE behavior OF lvd_tb IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT lcd_disp
   PORT(
        clk : IN  std_logic;
        lcd_rw : OUT  std_logic;
        lcd_e : OUT  std_logic;
        lcd_rs : OUT  std_logic;
        data : OUT  std_logic_vector(7 downto 0)
       );
   END COMPONENT;


  --Inputs
  signal clk : std_logic := '0';

            --Outputs
  signal lcd_rw : std_logic;
  signal lcd_e : std_logic;
  signal lcd_rs : std_logic;
  signal data : std_logic_vector(7 downto 0);

  -- Clock period definitions
  constant clk_period : time := 10 ns;

BEGIN

            -- Instantiate the Unit Under Test (UUT)
  uut: lcd_disp PORT MAP (
         clk => clk,
         lcd_rw => lcd_rw,
         lcd_e => lcd_e,
         lcd_rs => lcd_rs,
         data => data
        );
```

```
  -- Clock process definitions
  clk_process :process
  begin
                    clk <= '0';
                    wait for clk_period/2;
                    clk <= '1';
                    wait for clk_period/2;
  end process;


  -- Stimulus process
  stim_proc: process
  begin
          WAIT FOR 10ms;
  end process;

END;
```


Applications Places System
Fri Oct 27, 6:12 PM
ISE Project Navigator (P.20131013) - /home/ise/LCD/LCD.xise - [lcd_disp (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View Implementat Simulat
Hierarchy
LCD
xc3s400-5pq208
lcd_disp - Behavioral (lcd
No Processes Running
Processes: lcd_disp - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sc...
Check Syntax
Generate Post-Synt...
Implement Design
Generate Programmin...
Configure Target Device
lcd_disp
clk
data(7:0)
lcd_e
lcd_rs
lcd_rw
lcd_disp
Start Design Files
Design Summary (Synthesized)
lcd_code.vhd
lvd_tb.vhd
lcd_disp (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
lcd_disp
Console Errors Warnings Find in Files Results View by Category
[756,584]


Applications Places System
Fri Oct 27, 6:05 PM
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
Instances and Processes
Instance and Process Name
lvd_tb
std_logic_1164
std_logic_arith
std_logic_unsigned
Objects
Simulation Objects for lvd_tb
Object Name
Value
clk 0
lcd_rw 0
lcd_e 1
lcd_rs 0
data[7:0] 00111000
clk_period 10000 ps
Name
Value
clk
lcd_rw
lcd_e
lcd_rs
data[7:0]
clk_period
1
0
1
0
00111000
10000 ps
86.250 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
100 ns
UUU...
00111000
10000 ps
X1: 86.250 ns
Instan...
Memory
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
Terminal
ISE Project Navigator (...
ISim (P.20131013) - [D...