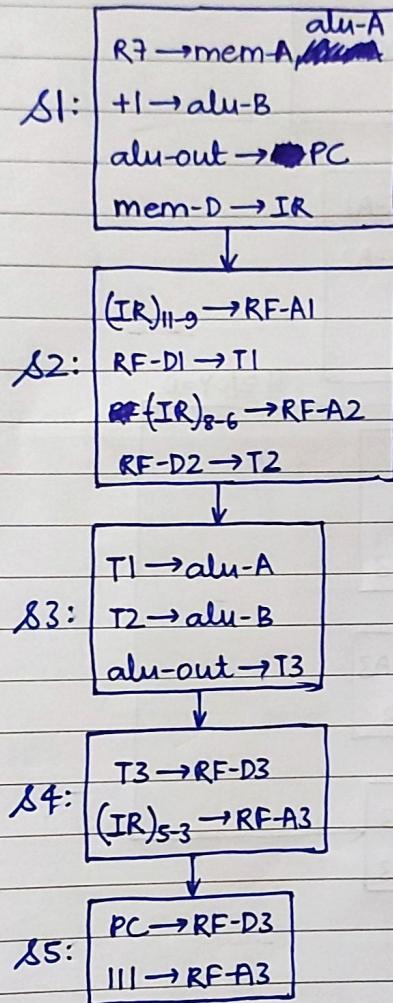


Group members: Shashwat Gupta (200070075), Atishay Jain (20007011)
Ojasvi Kathuria (200070058), Bhagyashree (20007013) S S
Page No. _____
Date. _____

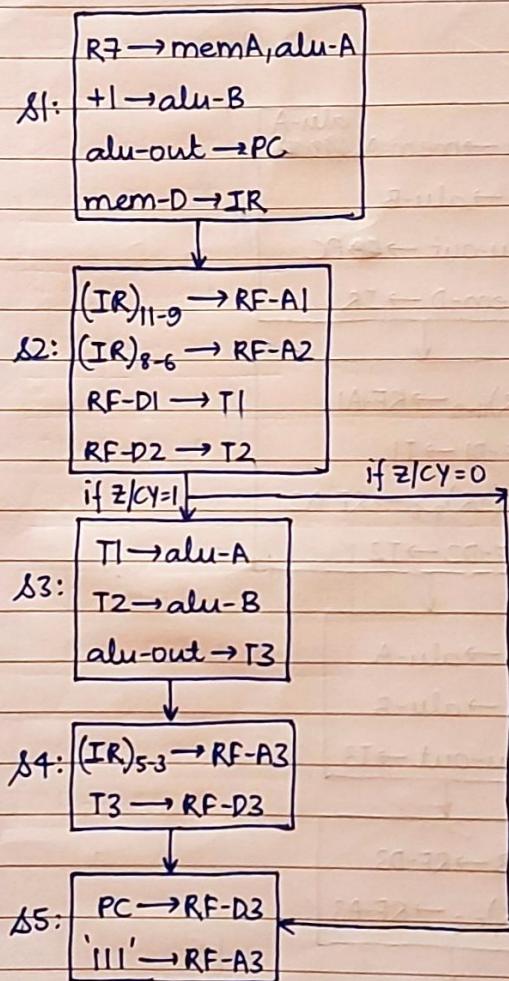
Hardware Flowcharts:

① ADD/NDU

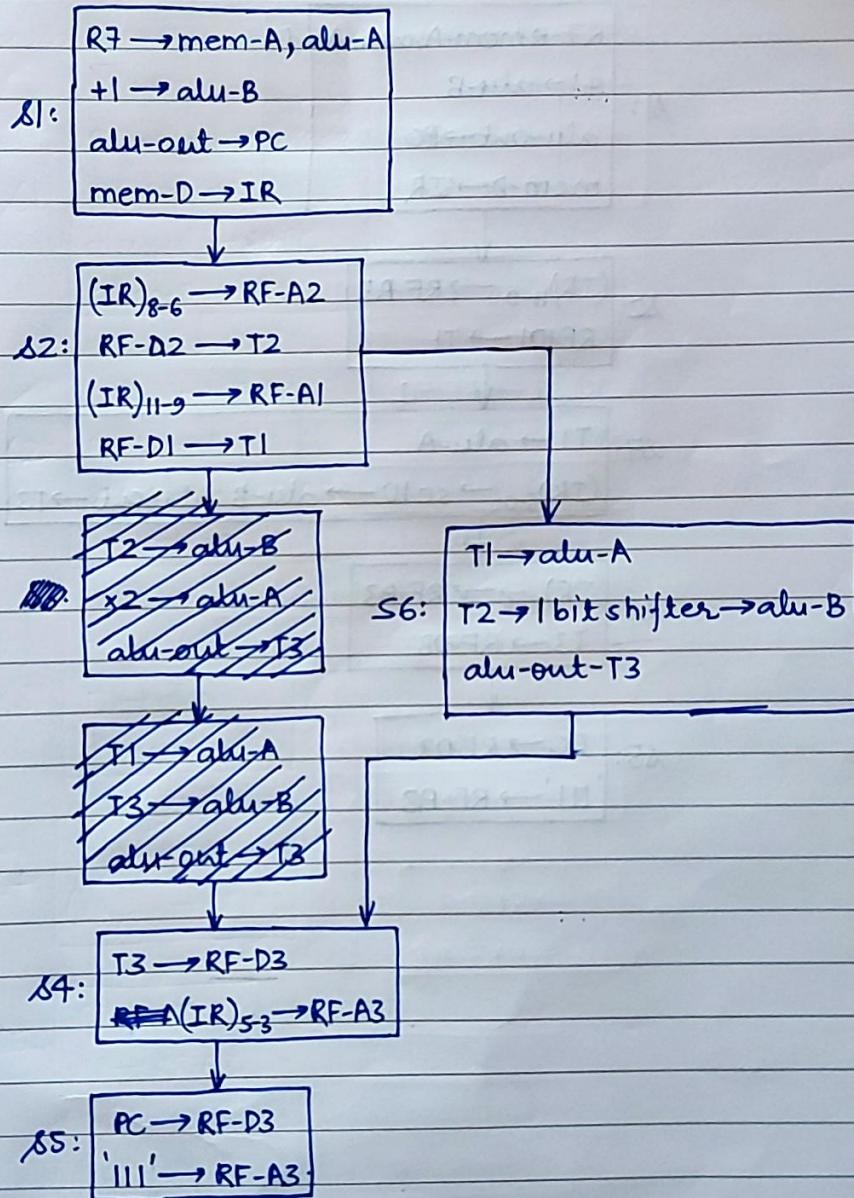
add rc, ra, rb



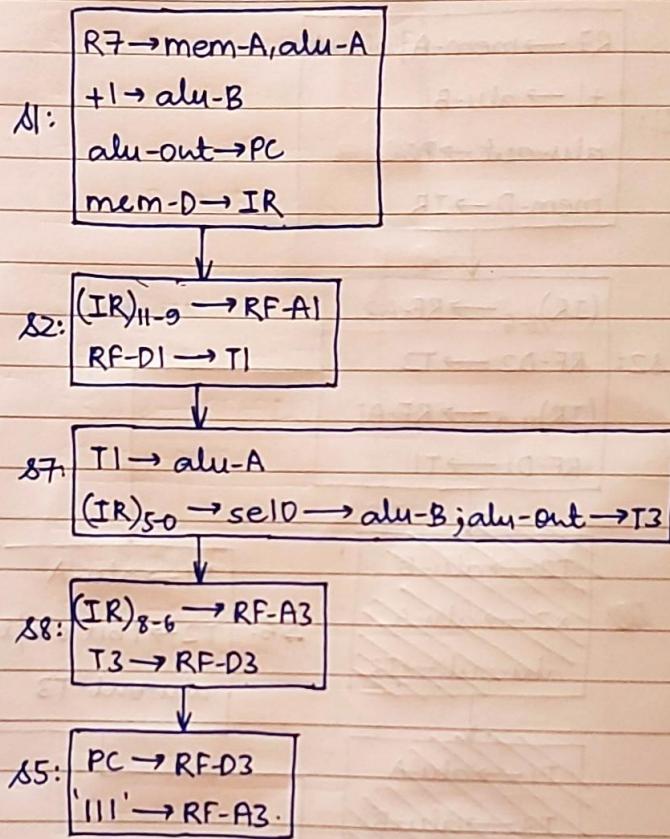
② ADC/NDC/ADZ/NDZ



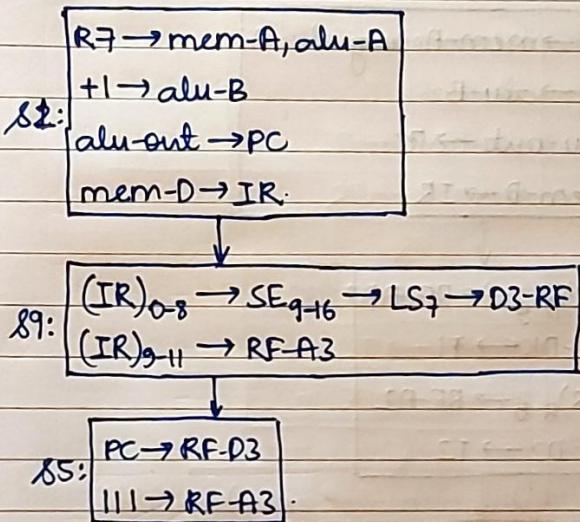
③ ADL: (add with left shift)



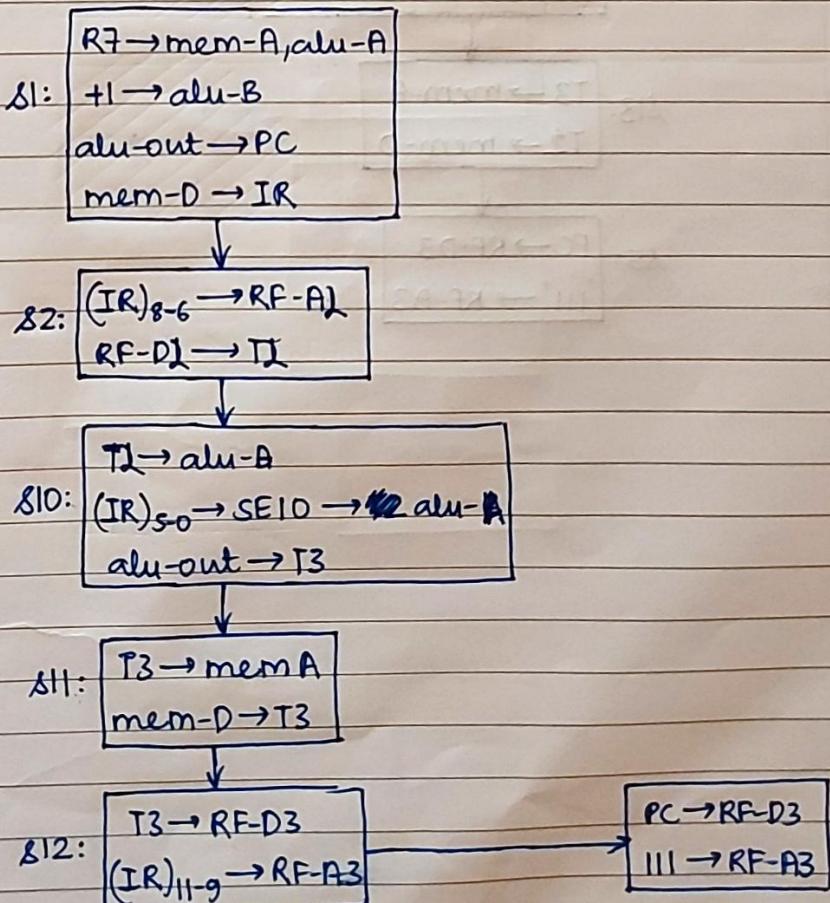
④ ADI:



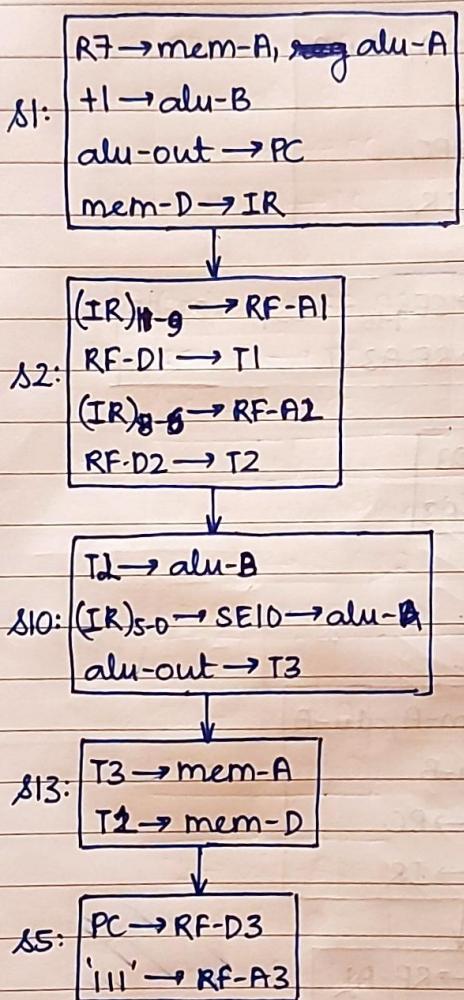
⑤ LHI:



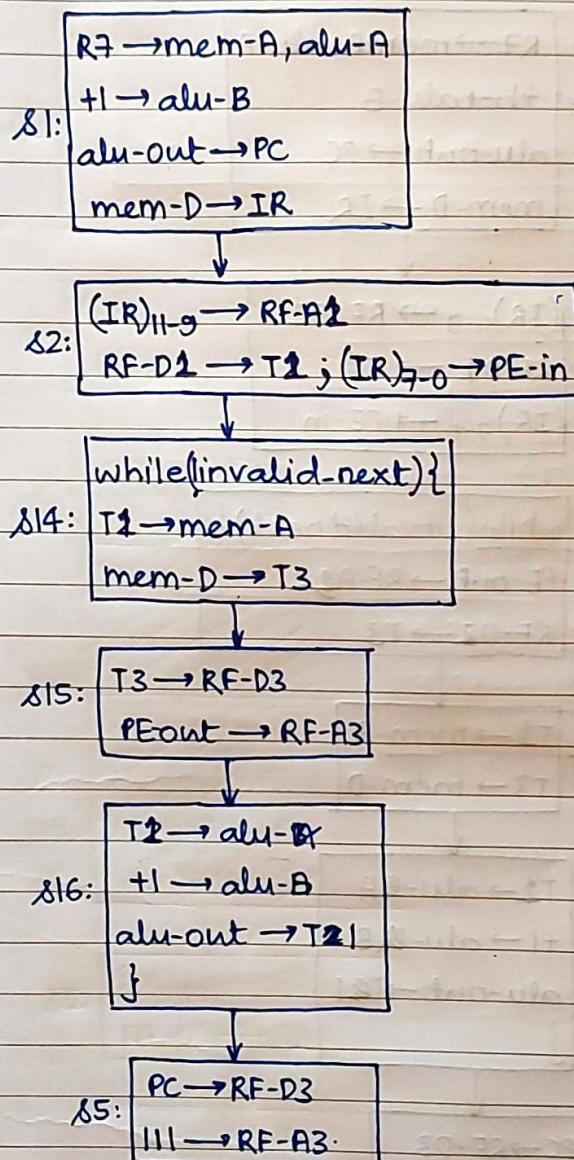
⑥ LW:



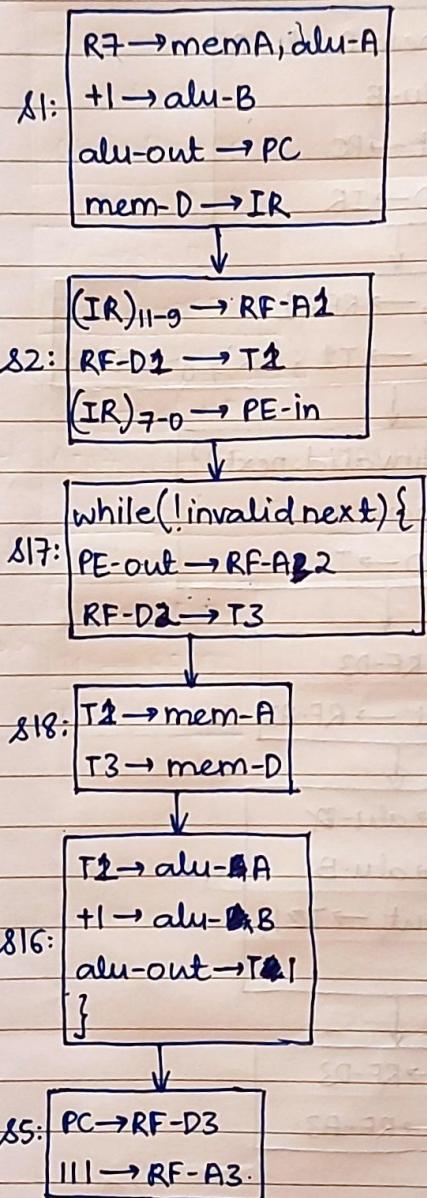
⑦ SW:



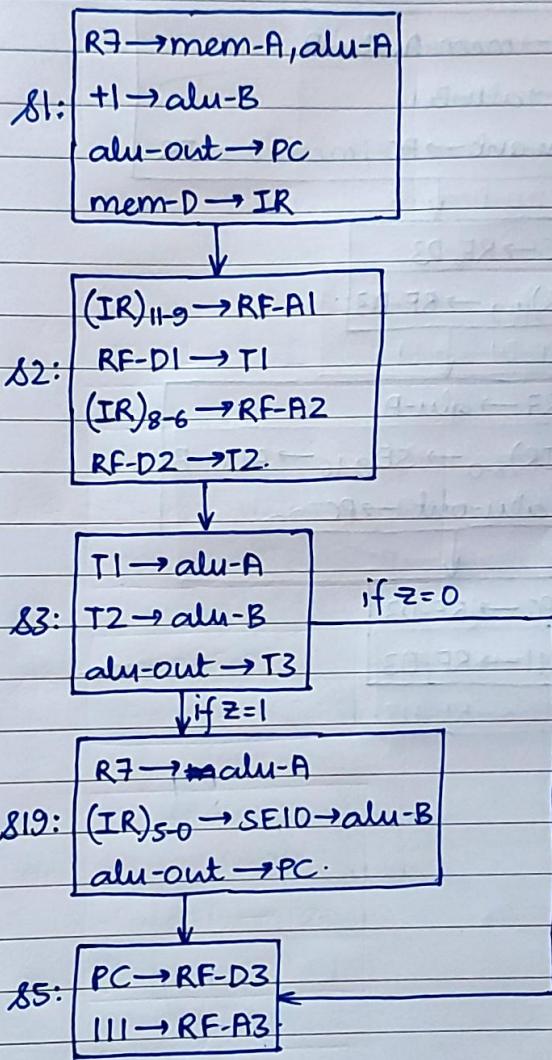
⑧ LM:



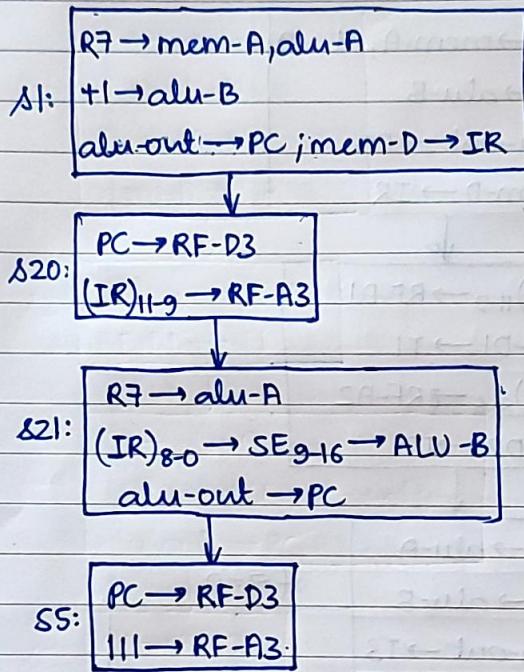
⑤ SM:



10) BEQ:

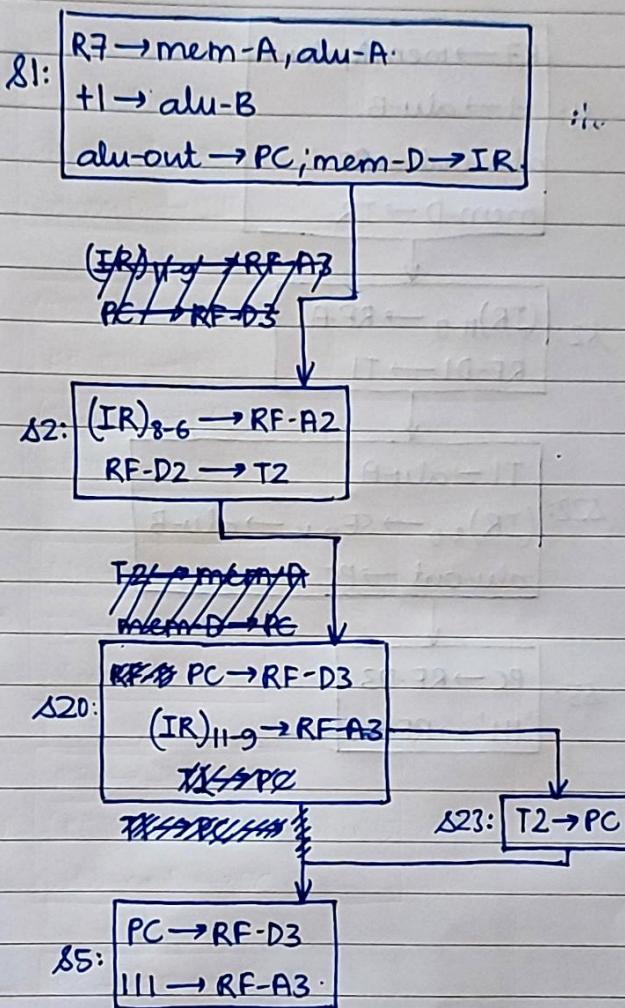


(11) JAL:

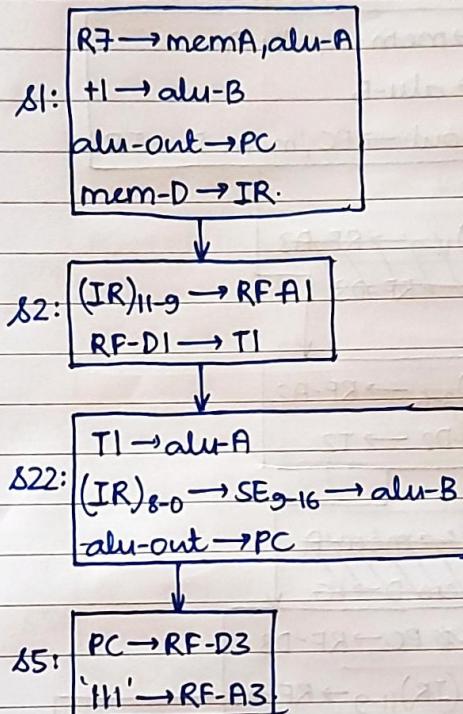


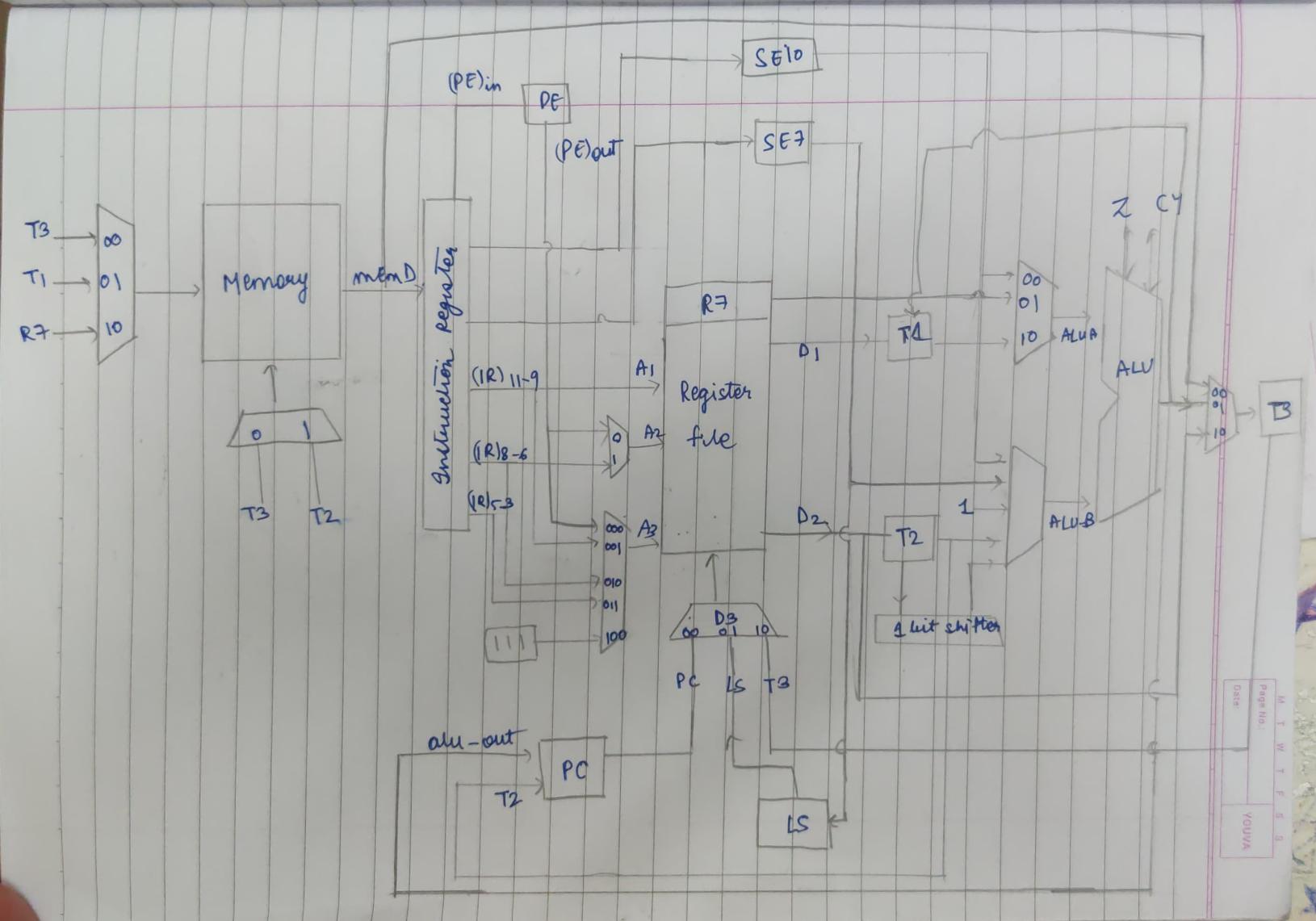
12 JLR:

13.11

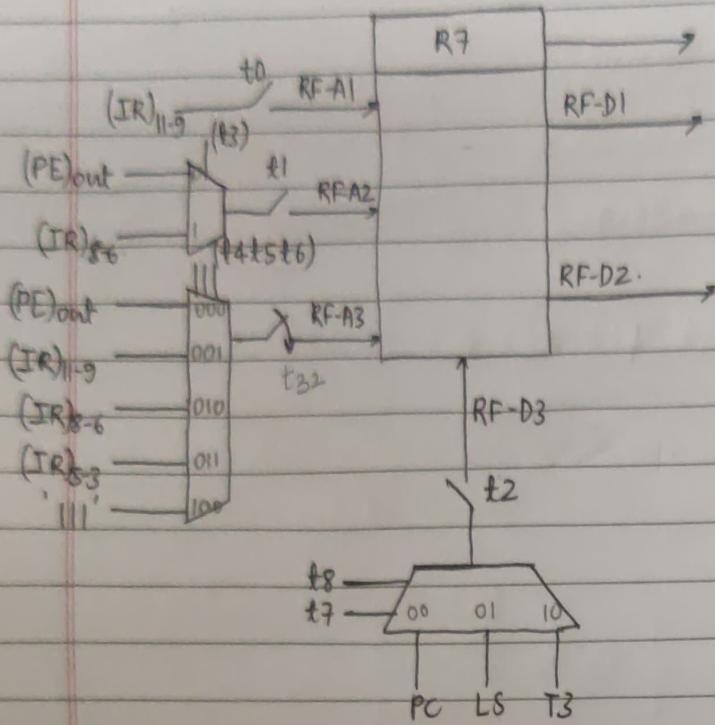


⑬ JRI:



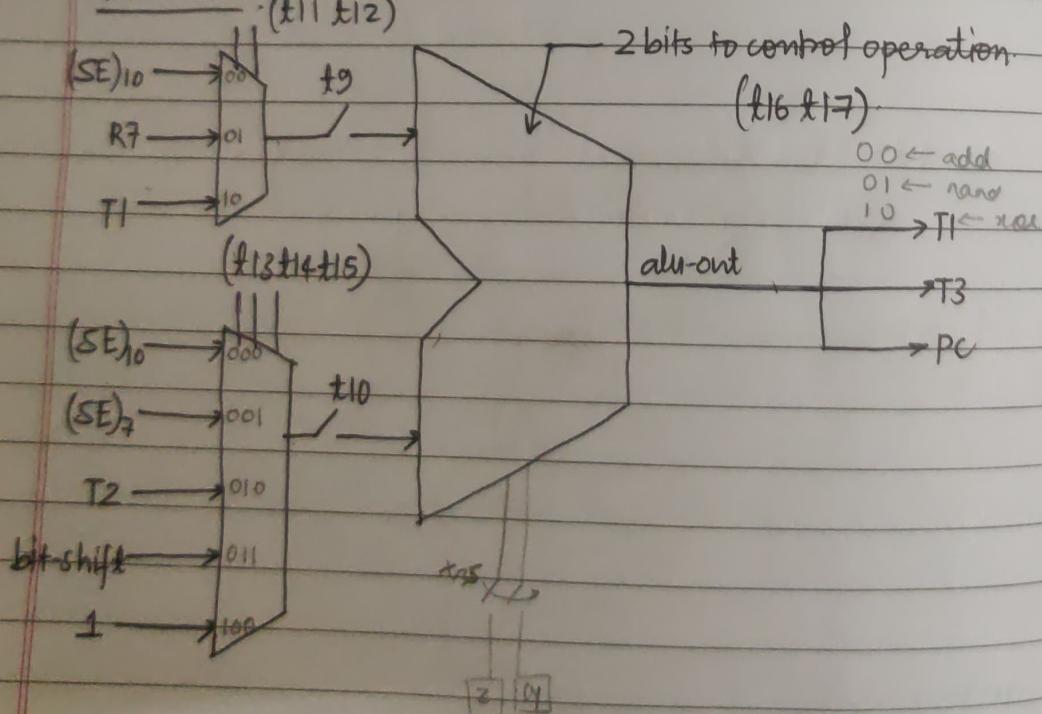


register file control

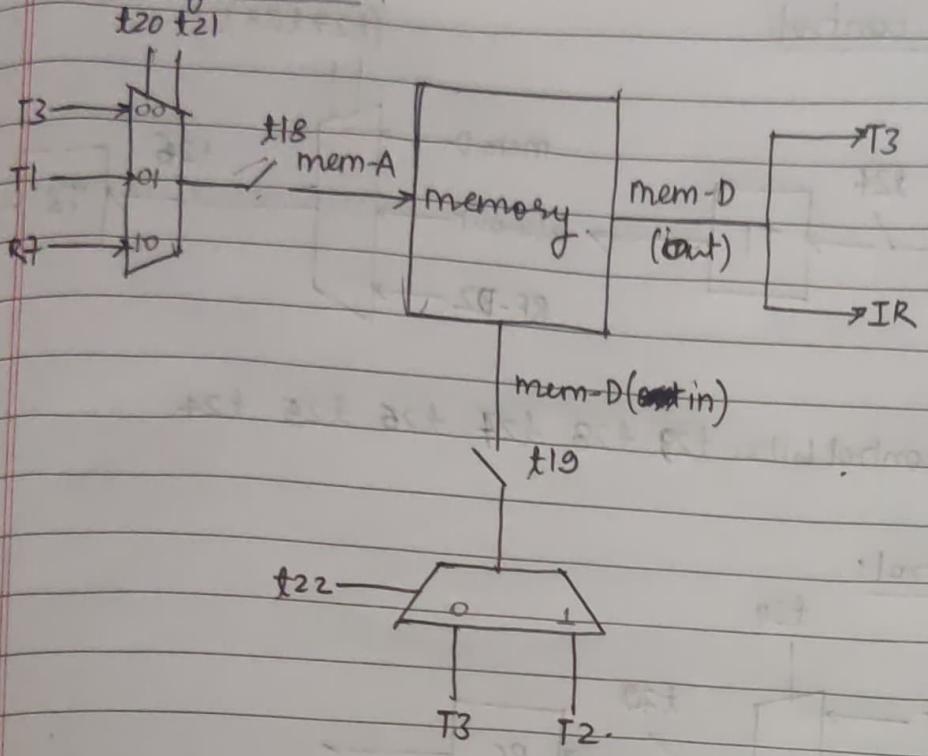


10.8 control bits: t₈ t₇ t₆ t₅ t₄ t₃ t₂ t₁ t₀

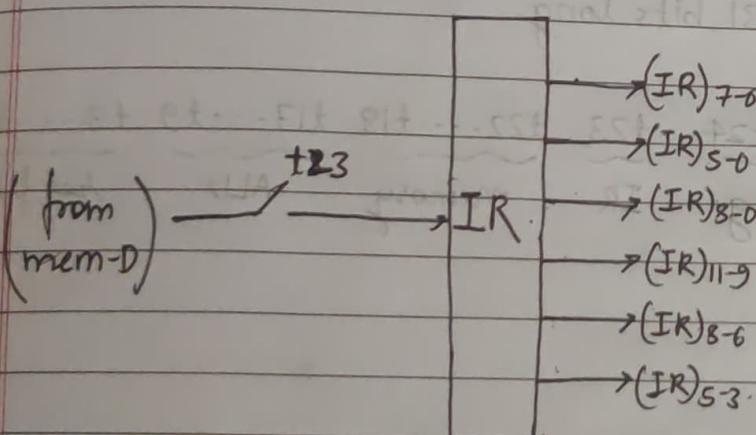
ALU control:



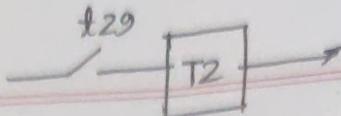
9 control bits: t17 t16 t15 t14 t13 t12 t11 t10 t9

memory control:

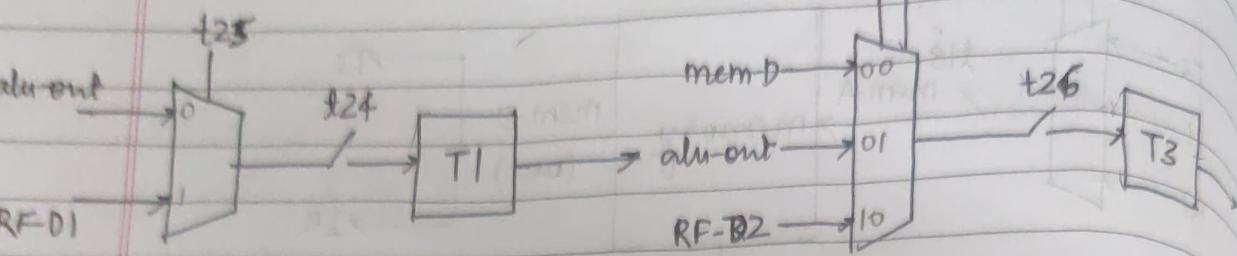
5 control bits: $t_{22} t_{21} t_{20} t_{19} t_{18}$

instruction register control:

1 control bit: t_{23} .

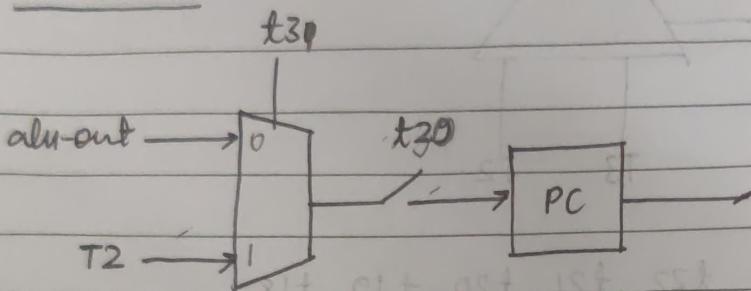


T1/T2/T3 control:



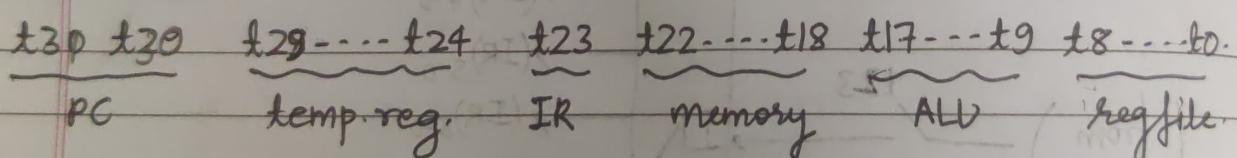
5 control bits: t29 t28 t27 t26 t25 t24

PC control:



2 control bits: t30 t29

CONTROL WORD: 31 bits long.



T32 → RF write enable

T33 → LS multiple write enable

T34 → LS multiple set zero

T35 → flag set

T36 → op. code forwarding

1 forwarded

0 from IR

