

VBUS to 5V - SWITCH

JVS Power Source Only for Digital parts

1V8 Power Source

JVS Power Source Only for Analog parts

Figure 1 illustrates four power supply decoupling circuit diagrams for the AD9288 ADC. The first diagram, 'VBUS to 5V - SWITCH', shows a P-channel MOSFET (P1M01) switching between a 5V source and a 1.8V source. The second diagram, 'JVS Power Source Only for Digital parts', shows a 3.3V digital power source using a TPS7A03 regulator. The third diagram, '1V8 Power Source', shows a 1.8V power source using a TPS7A03 regulator. The fourth diagram, 'JVS Power Source Only for Analog parts', shows a 3.3V analog power source using a TPS7A03 regulator. All diagrams include a 10k resistor and a 100nF capacitor for decoupling.

[illegible][illegible][illegible]

The schematic diagram shows a common-emitter amplifier circuit. A 10V DC supply is connected to the collector resistor (100kV) and the emitter resistor (100V). The base resistor (10kV) is connected to the base of the NPN transistor. The input signal, a 10V sine wave, is applied to the base. The output is taken from the collector. The circuit is labeled with 'base', 'collector', and 'emitter' nodes.

The schematic illustrates a USB-to-serial converter circuit. Key components include:

- USB Connector:** VBUS, D+, D-, and GND pins.
- Hub Controller:** UH1 (USB Hub Controller).
- Serial Converter:** FT232RL (FT232RL).
- Power Regulation:** 3.3V regulator (U1), decoupling capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100).
- Signal Traces:** TXD, RXD, and RTS signals are shown on the right side.

[illegible][illegible][illegible][illegible][illegible]

The schematic diagram illustrates the input stage of the AD7950. It features four differential input pairs, each consisting of an NMOS transistor (labeled NM1A_ETS1, NM1A_ETS2, NM1B_ETS1, NM1B_ETS2) and a PMOS transistor (labeled PM1A_ETD1, PM1A_ETD2, PM1B_ETD1, PM1B_ETD2). The NMOS transistors have their sources connected to ground and their gates driven by a +5.5V signal through inverters. Their drains are connected to the gates of the PMOS transistors. The PMOS transistors have their sources connected to a +5.5V supply and their gates also connected to +5.5V. The drains of the PMOS transistors converge at a central common node, which is then connected to a resistor network.

Use the jumpers to choose the HALL source signal!

Diagram showing the wiring for the HALL sensor. The sensor is connected to the HALL source signal via jumpers. The jumpers are labeled: HALL, HALL, HALL, HALL, HALL. The sensor is connected to the HALL source signal via jumpers. The jumpers are labeled: HALL, HALL, HALL, HALL, HALL.

2.1in_TFT_Screen

Pin connections for the 2.1in TFT_Screen module:

- GND → VSS
- VCC → +3.3V
- SCL → AR10A_S2P1_SCL
- SDA → AR10A_S2P1_SDA
- RESET → AR10A_RST
- D/C → AR10A_D_C
- CS → AR10A_CS_A0_VSS
- BLU → AR10A_BLU

Additional connections for the 2.1in_TFT_Screen module:

- T1 → VSS
- T2 → VSS

MCPWM PWM Output Ports

The diagram illustrates the MCPWM PWM output ports for pins 151 through 160. Each pin is connected to a specific MCPWM module output (e.g., MCPWM_CH1, MCPWM_CH2, MCPWM_CH3, MCPWM_CH4, MCPWM_CH5, MCPWM_CH6, MCPWM_CH7, MCPWM_CH8, MCPWM_CH9, MCPWM_CH10) and a corresponding VDD pin. The diagram shows the connection between the MCPWM module and the VDD pin for each output port.

Pin	MCPWM Module	VDD Pin
151	MCPWM_CH1	VDD151
152	MCPWM_CH2	VDD152
153	MCPWM_CH3	VDD153
154	MCPWM_CH4	VDD154
155	MCPWM_CH5	VDD155
156	MCPWM_CH6	VDD156
157	MCPWM_CH7	VDD157
158	MCPWM_CH8	VDD158
159	MCPWM_CH9	VDD159
160	MCPWM_CH10	VDD160

CMP Signal Inputs

The diagram illustrates the OPAMP signal input and output. It shows two input channels, each with a 10kΩ resistor (R120, R122) and a 10V/1V scale indicator. The inputs are labeled 'MCMC_OPAMP_IN_1' and 'MCMC_OPAMP_IN_2'. The outputs are labeled 'OPAMP_OUT_1' and 'OPAMP_OUT_2'. The diagram also shows the internal structure of the OPAMP, including the RC Filter, the OPAMP core, and the output buffer. The output buffer is labeled 'OPAMP_OUT_1' and 'OPAMP_OUT_2'.

Figure 10 shows two RC filter circuit diagrams. The top circuit is for ACINA_OPAMP0_IN, featuring a 10k resistor (R120) in series with a 100pF capacitor (C92) connected to a 1.8V supply, and a 100pF capacitor (C93) connected to ground. The bottom circuit is for ACINA_OPAMP0_ID, featuring a 10k resistor (R120) in series with a 100pF capacitor (C94) connected to a 1.8V supply, and a 100pF capacitor (C95) connected to ground. Both circuits are labeled 'RC Filter'.

AKINA Single Ended OPAMP Output

[illegible]

$\text{P}(\text{M}_0, \text{Z} \times \text{S})$

Sheet: /		Rev:
File: PSVB_EvalBoard.kicad_sch		
Title:		
Size: A0	Date:	
KiCad 3.0.4	KiCad 7.0.1	Id: 1/1