TP 1 ISL

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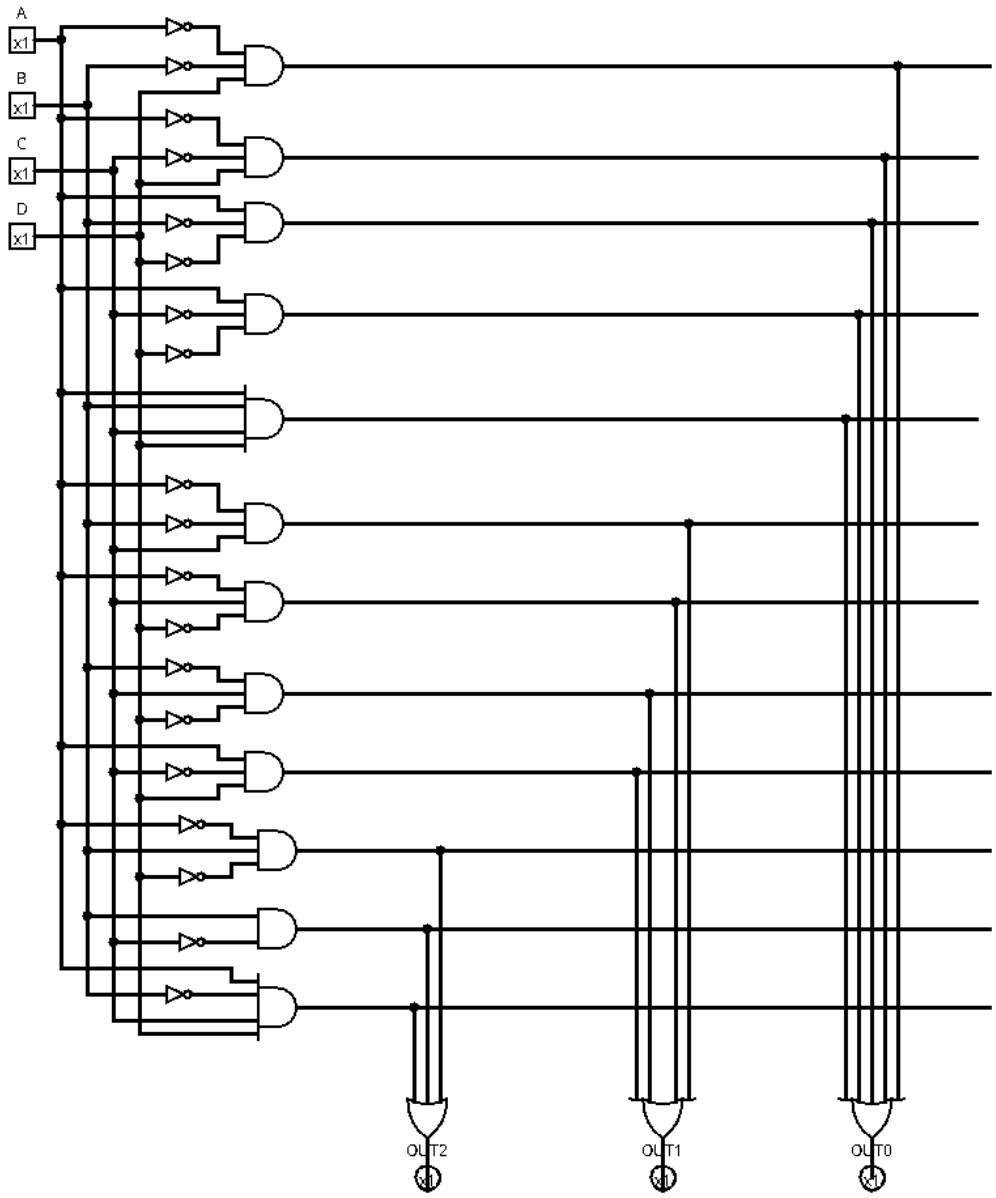
Matrícula: 2023002138

a)

ENTRADAS (A,B, C, D)

SAÍDAS (OUT 2, OUT 1, OUT 0)

O circuito foi implementado usando a tecnologia PAL, pela questão de sua robustez e eficiência, além disso o fato de nenhum dos produtos ter sido compartilhado pelas portas OR foi significativa na decisão de usar a tecnologia PAL.



b)

Saída OUT 2 (N3, N2, N1, D) = Σm(4, 5, 6, 11, 12, 13)

Saída OUT 1 (A, B, C, D) = Σm(2, 3, 6, 9, 10, 13)

Saída OUT 0 (A, B, C, D) = Σm(1, 3, 5, 8, 10, 12, 15)

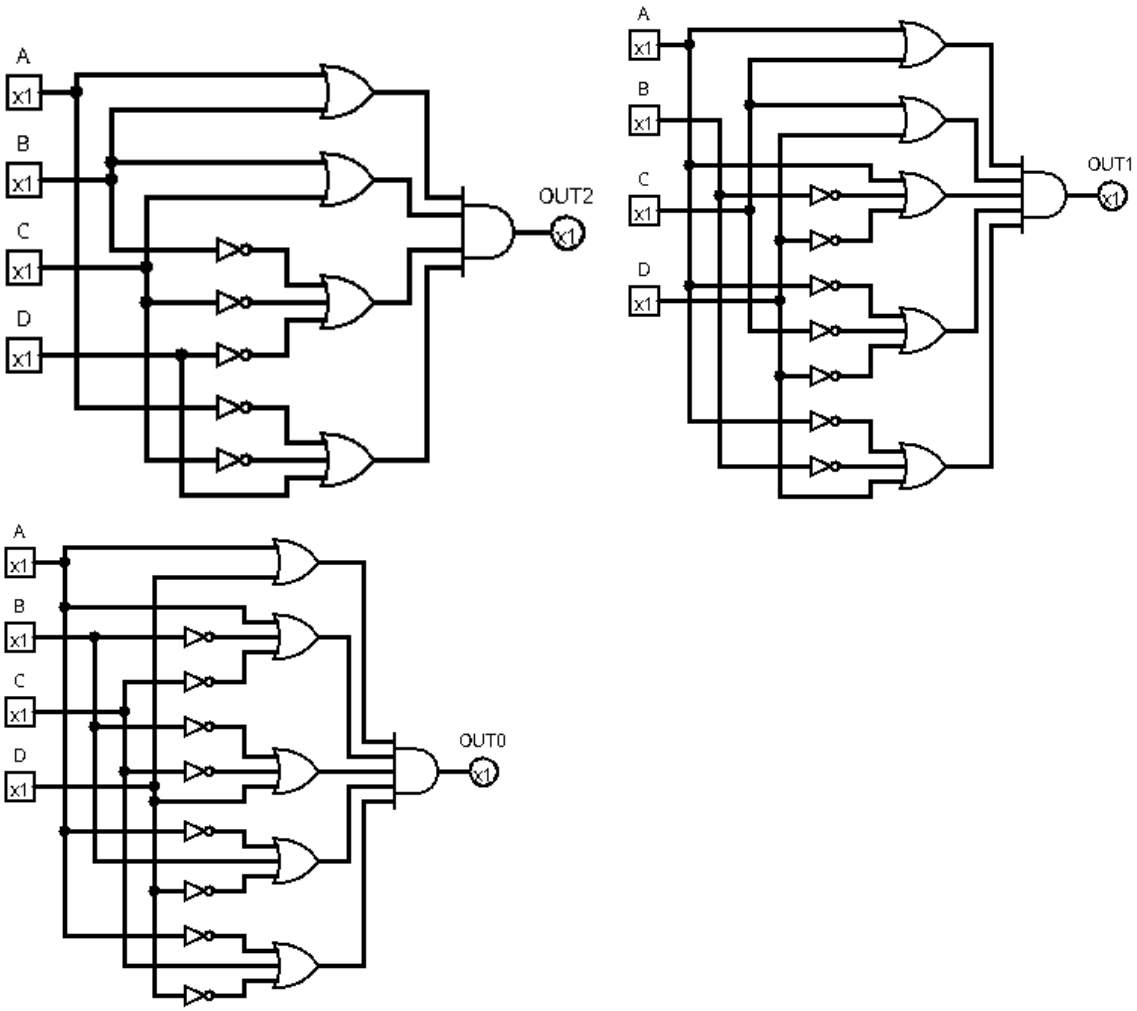
c)

Saída OUT 2(A, B, C, D) = (A + B) (B + C) (B' + C' + D') (A' + C' + D)

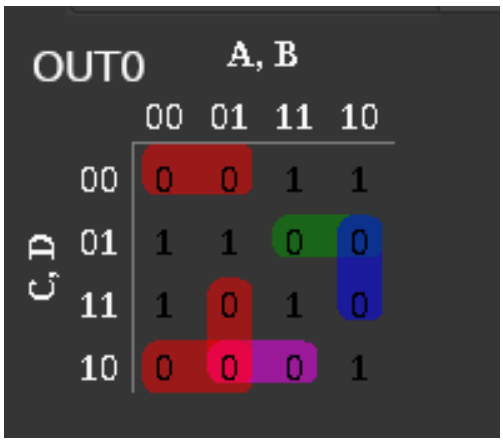
Saída OUT 1(A, B, C, D) = (A + C) (C + D) (A + B' + D') (A' + C' + D') (A' + B' + D)

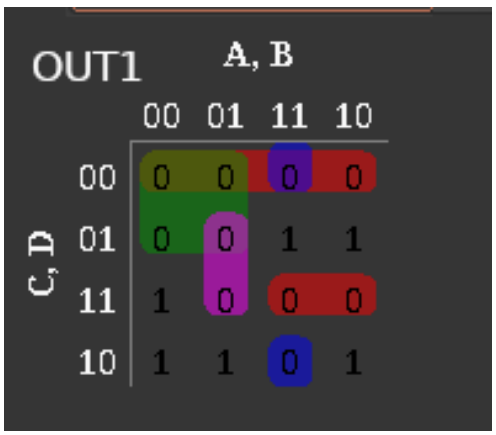
Saída OUT 0(A, B, C, D) = (A + D) (A + B' + C') (B' + C' + D) (A' + B + D') (A' + C + D')

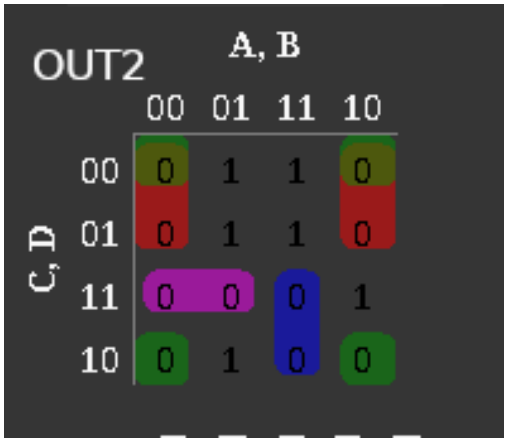
d)



e)







f)

A	B	C	D	OUT2
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

A	B	C	D	OUT1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

A	B	C	D	OUT0
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

g)