**Design Requirements of a Test-Board for DM3730/AM3703 TorpedoSOM**

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1. **Introduction**
   1. Objective

Objective of this document is to understand the requirements for the design of a Test Board for the DM3730/AM3703(equipped with a Up to 1-GHz Sitara™ ARM® Cortex™-A8 Core processor) Torpedo System on Module(SOM) in order to facilitate the use of the microcontroller DM3730/AM3703 for further development of end-user applications and hence, provide a functional description of the design.

* 1. Background

The DM3730/AM3703 Torpedo System on Module(SOM)(Table 1) has an onboard Power Management IC which takes care of all the voltage conversions required to power up the microcontroller and all its IOs buses. It also has a clock distribution circuitry which again takes care of all the clocks required by the microcontroller. Other than that it also provides some special interfaces like AudioIO, keypad, HS OTG etc. All these interface lines have been made accessible to the user through two 100 pin connectors. Other than these another 40-pin connector has been provided for debug purpose through JTAG and ETM interfaces.

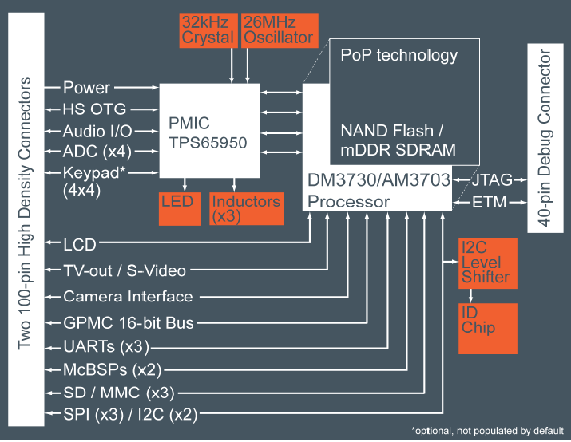


Table 1 : *DM3730/AM3703 TorpedoSOM Block Diagram.*

1. **Requirements**

The test board should be able to test the Torpedo SOM board and hence, provide a platform for further development of specific applications. The following system requirements have been noted after discussion:

* 1. SOM Power Supply
  2. Two UART access ports through USB
  3. SD Card slot
  4. Boot Configuration Switches
  5. Reset Button
  6. GPIOs
  7. User LEDs

1. **Test Board Design**
   1. Review of the requirements & strategies for design
      1. SOM Power Supply

The SOM has all the power distribution circuitry required for the different processor voltages. But, the user has to provide a single power source to the SOM having a voltage range of 2.7V to 4.5V at the 100 pin connector. So, a separate connector will be provided specifically for the power supply which can be provided by a single cell Li ion Battery.

* + 1. Two UART access port through USB

UART provides access to the processor registers which is required to establish a communication channel for configuring the SOM. UART to USB convertor ICs is required to facilitate UART access through external PC USB port.

* + 1. SD card slot

SD card slot is requirement to provide boot facilities through an SD card in which the operating system can be stored.

* + 1. Boot Configuration Switches

The Boot Configuration switches are required for choosing Boot options like Multi Media Card(MMC), NAND flash memory, USB, UART etc. Dual In-line Package(DIP) switches are simple and cost-effective solutions for such a requirement

* + 1. Reset Button

The processor Reset Button shall be provided through a push-button switch which when pressed for a finite time interval triggers the processor to reset all its internal registers as well as generate a reset out signal which can be used to reset all peripheral devices.

* + 1. GPIOs

The 100 pin connectors on the SOM board facilitates many IO interfaces like I2C, multi-channel SPI(MCSPI), HS USB OTG etc. 20 IO lines will be made available for the user on two separate connectors. One connector will have two sets of SPI lines and the other will have two sets of I2C lines and five GPIO’s.

* + 1. LEDs

LED’s will be mounted on 5 IO lines.

* 1. Design Review

After understanding the requirements of the system and analyzing the design strategies, all the building blocks have been put together to provide a functional description of the test board shown in Table 2.

2 X (USB TO UART)

DM3730/AM3703 Torpedo SOM

USER PC

**POWER SUPPLY (2.7V-4.5V)**

BOOT CONFIG

GPIOs(I2C,MCSPI, Other GPIOs)

LED’s

SD CARD

SYSTEM RESET

Test Board Block Diagram

Table 2 : *Test Board Block Diagram.*

1. Conclusion

Requirements for the design of the test board have been discussed and a functional description of the design has been laid down after analyzing the components required for the design. Further, documentation of the actual board design and test strategies will be done next.