

ZYNQ\_TOP\_LEVEL  
ZYNQ\_TOP\_LEVEL.SchDoc

PS\_POR\_B  
PWR\_SHDN\_TRIG

LM\_SPI  
ZYNQ\_LMS\_DIG\_IO

GigEthernet\_1  
GigEthernet\_2

L1\_OK

PS\_SPI

GPS\_D

UART\_0

UART\_1

JTAG

I2C

PS\_SRST\_B

I2C\_EN

DDR3

Power\_Distribution\_TopLevel  
Power\_Distribution\_TopLevel.SchDoc

PS\_POR\_B  
PWR\_SHDN\_TRIG

RF\_TOP\_LEVEL  
RF\_TOP\_LEVEL.SchDoc

LM\_SPI  
ZYNQ\_LMS\_DIG\_IO

ETHERNET\_TOP\_LEVEL  
ETHERNET\_TOP\_LEVEL.SchDoc

Gig\_Ethernet\_1  
Gig\_Ethernet\_2

PS\_POR\_B  
L1\_OK

PERIPHERALS  
PERIPHERALS.SchDoc

PS\_SPI

GPS\_D

UART\_0

UART\_1

JTAG

I2C

PS\_SRST\_B

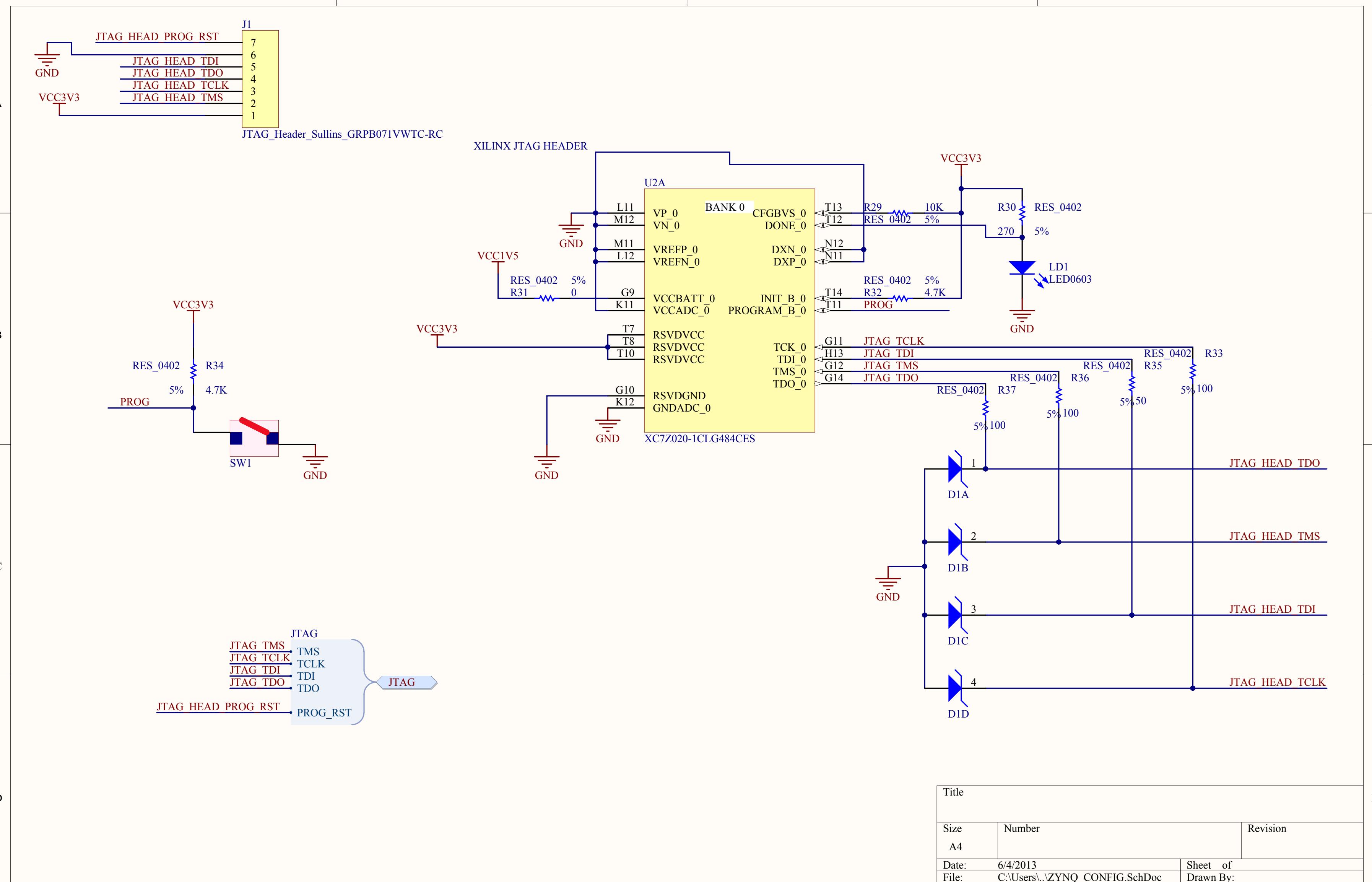
I2C\_EN

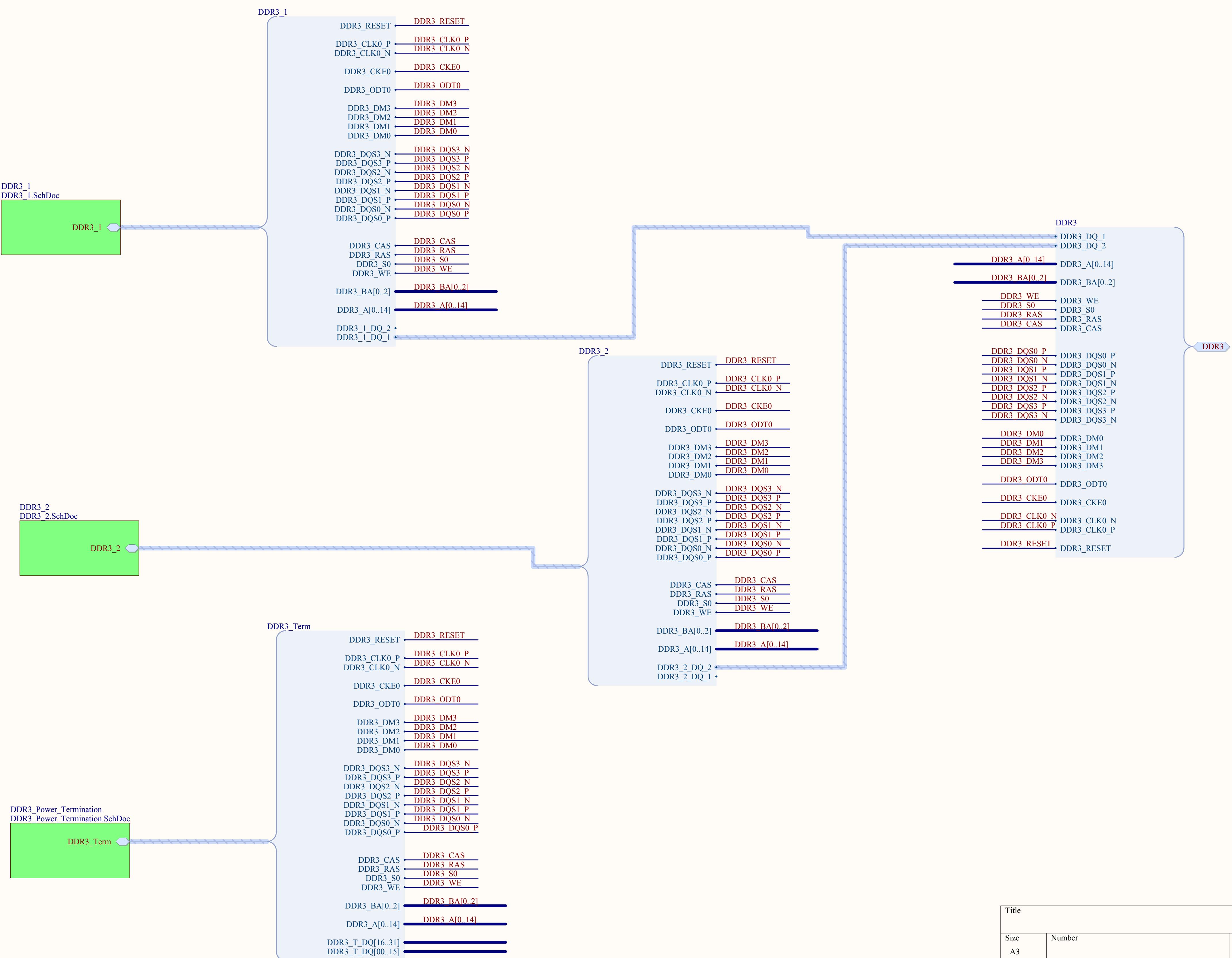
DDR3\_TOP\_LEVEL  
DDR3\_TOP\_LEVEL.SchDoc

DDR3

Mounting\_Holes  
Mounting\_Holes.SchDoc

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\COMRAD_TOP_LEVEL.SchDoc	Drawn By:

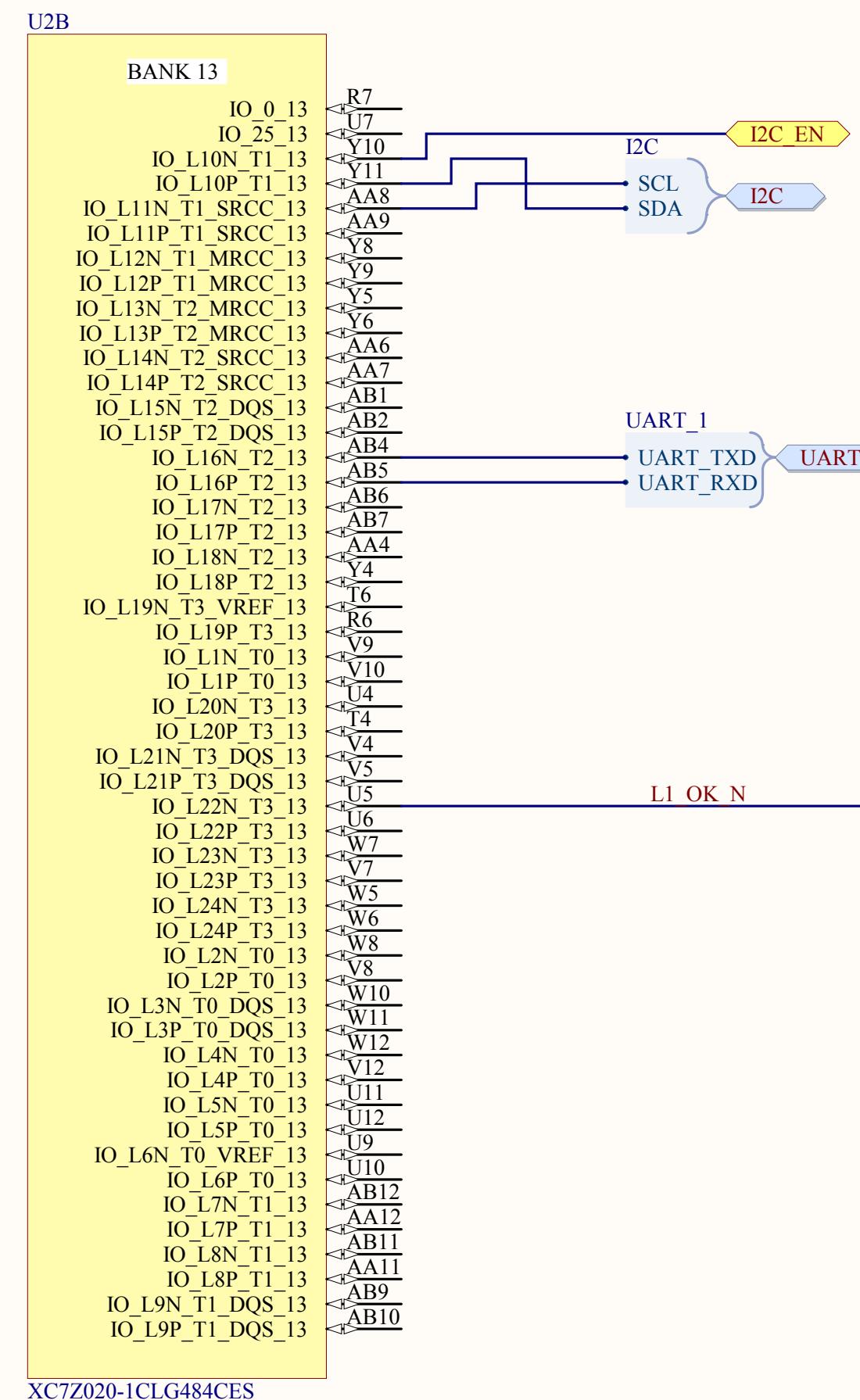




Title		
Size	Number	Revision
A3		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\DDR3_TOP_LEVEL.SchDoc	Drawn By:

A

A



B

B

C

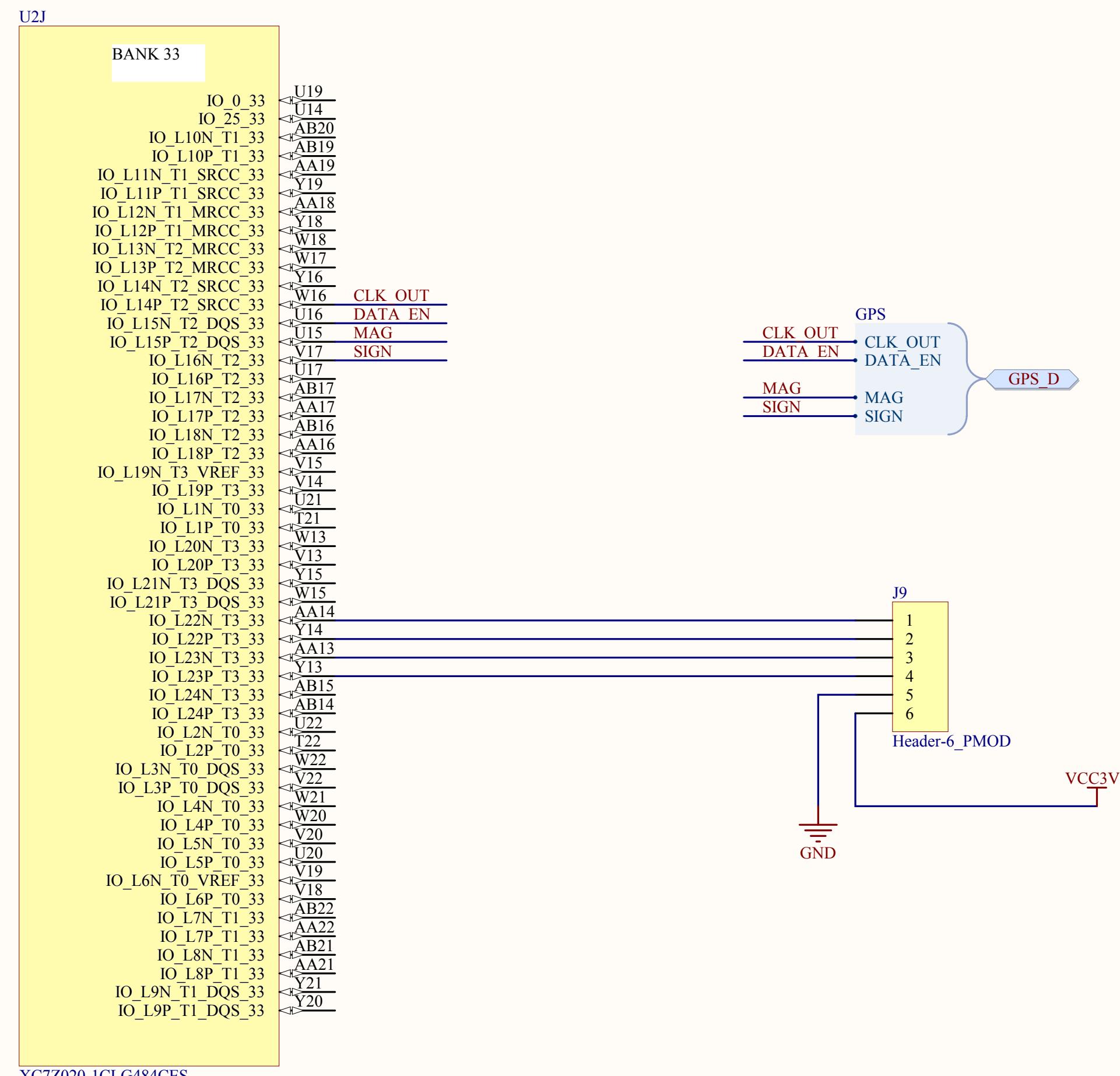
C

D

D

Title		
Size	Number	Revision
A4		
Date: 6/4/2013	Sheet of	
File: C:\Users\..\ZYNQ_PL_Bank_13.SchDoc	Drawn By:	

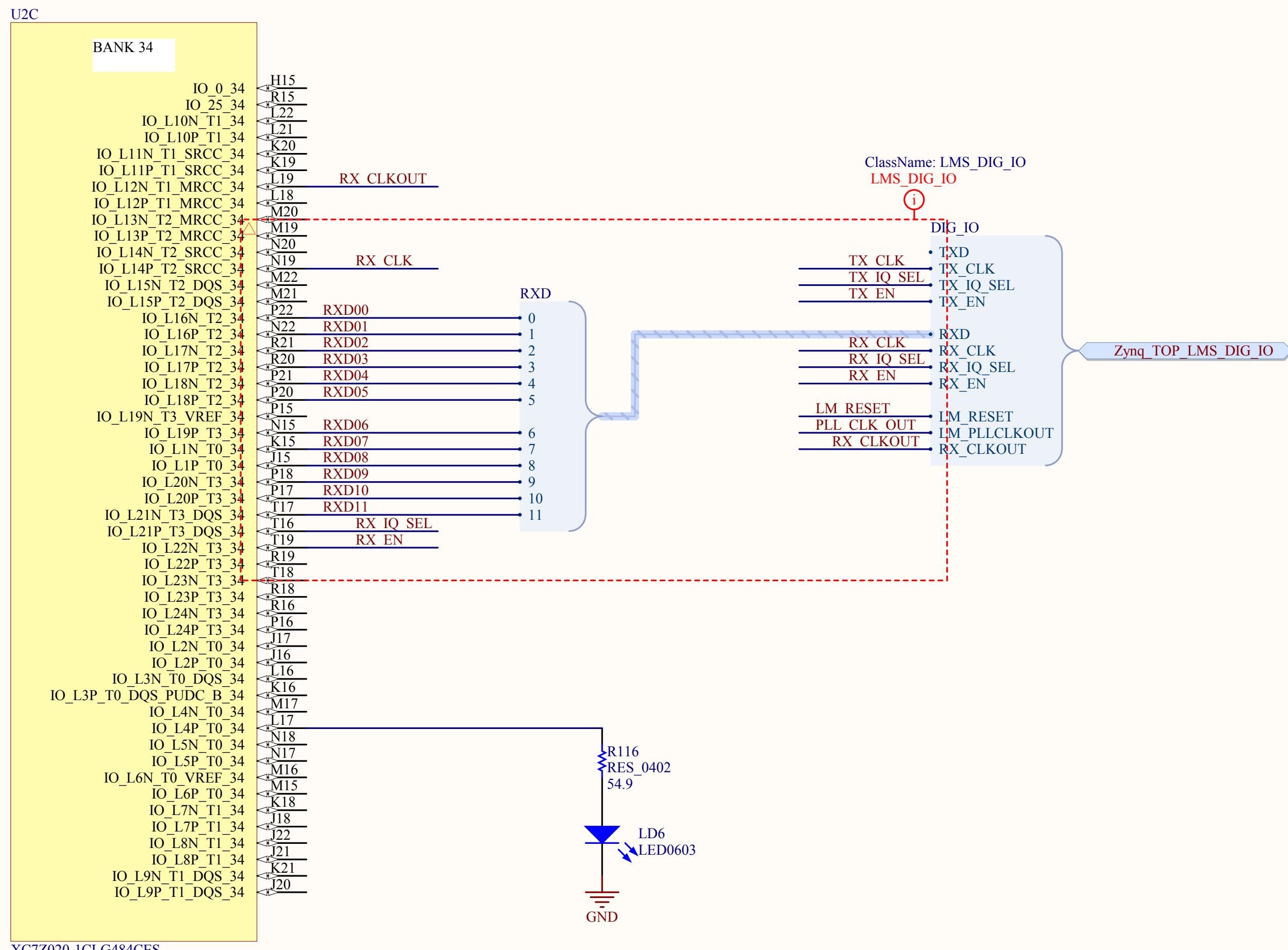
A



Title

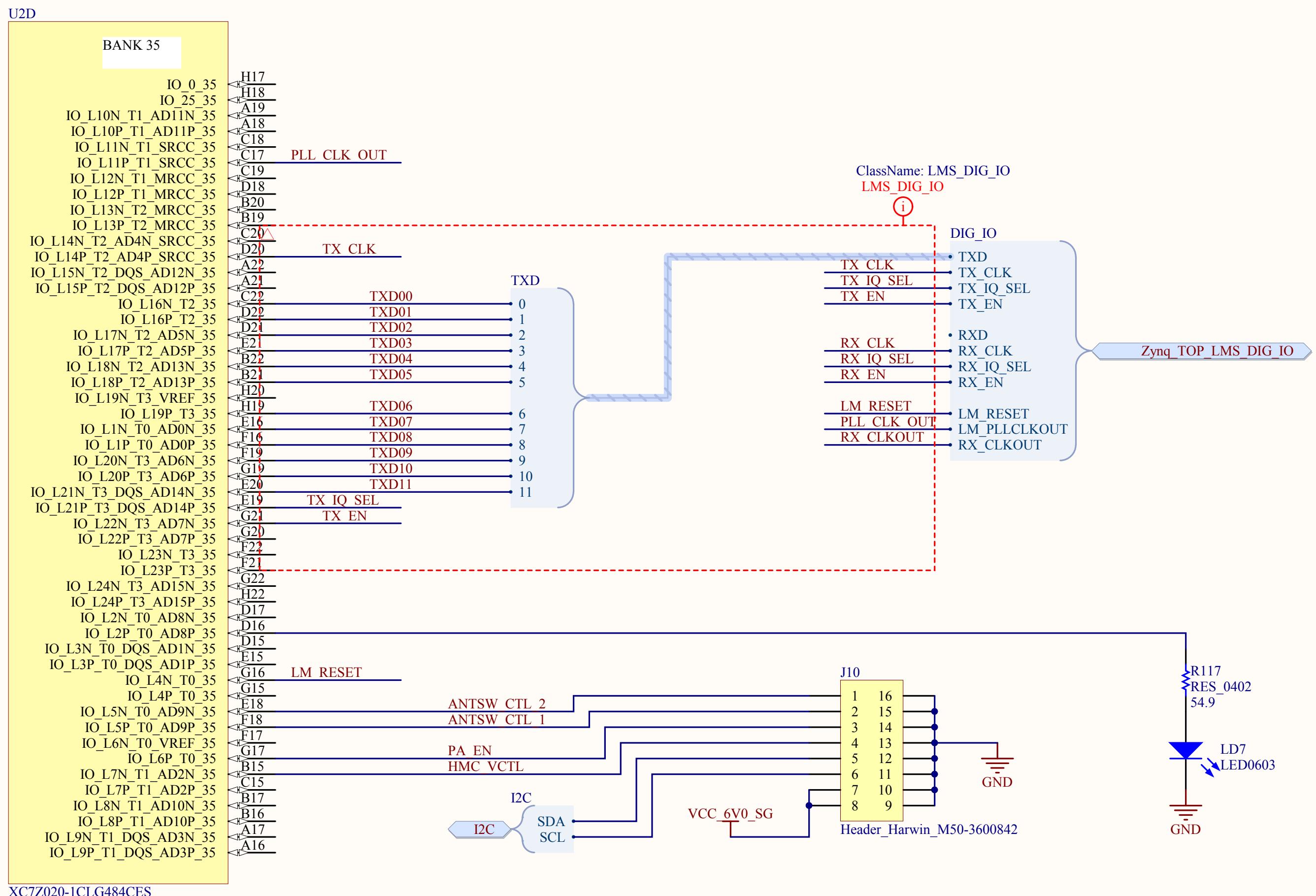
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\ZYNQ_PL_Bank_33.SchDoc	Drawn By:

A

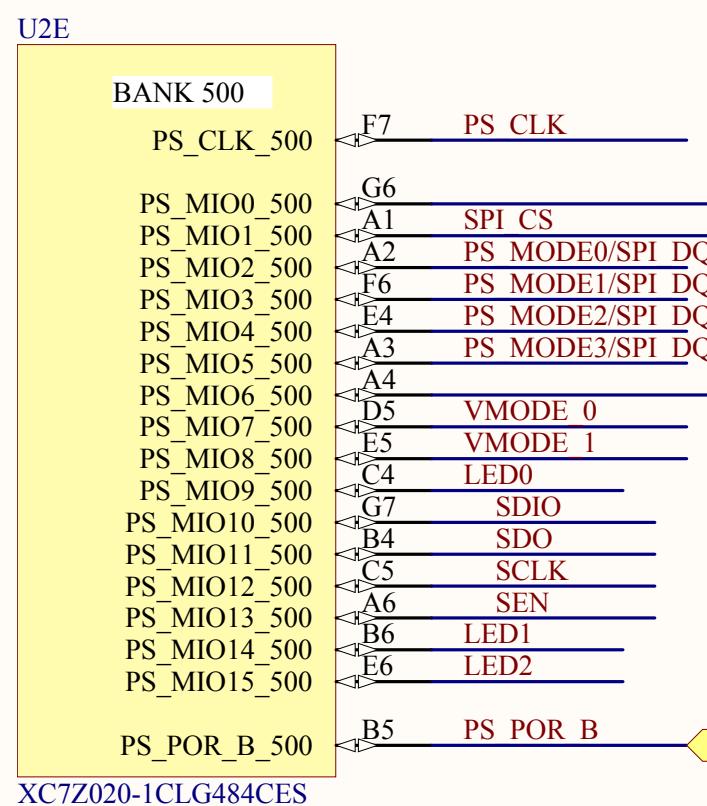


Title

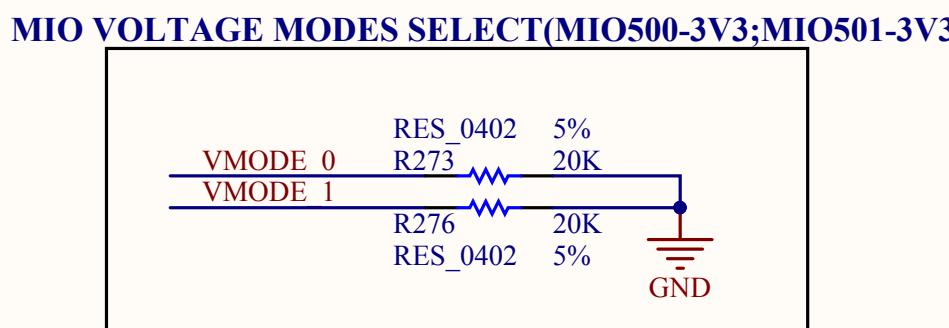
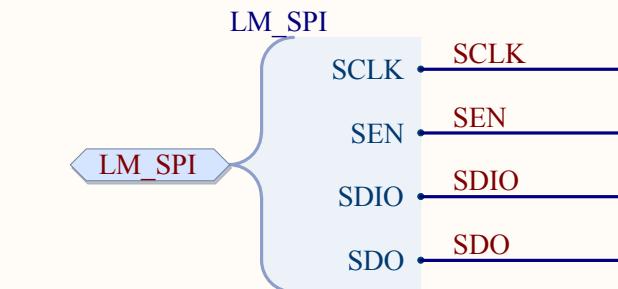
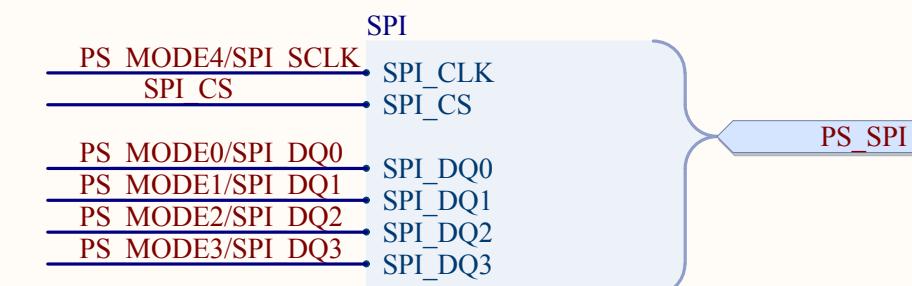
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\ZYNQ_PL_Bank_34.SchDoc	Drawn By:



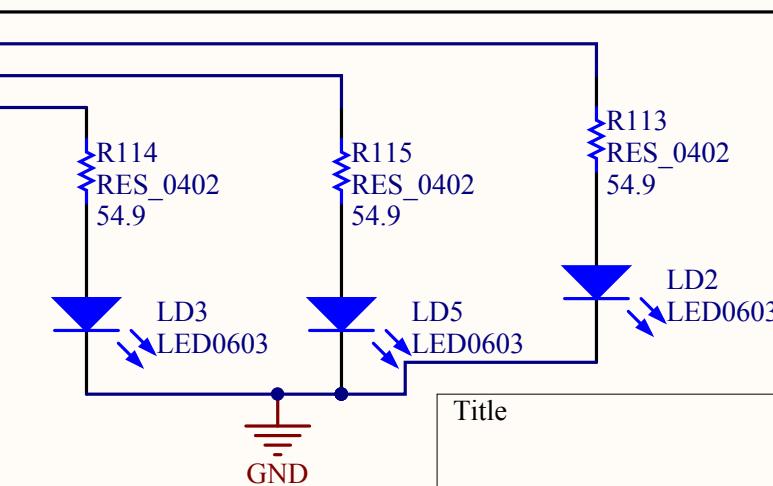
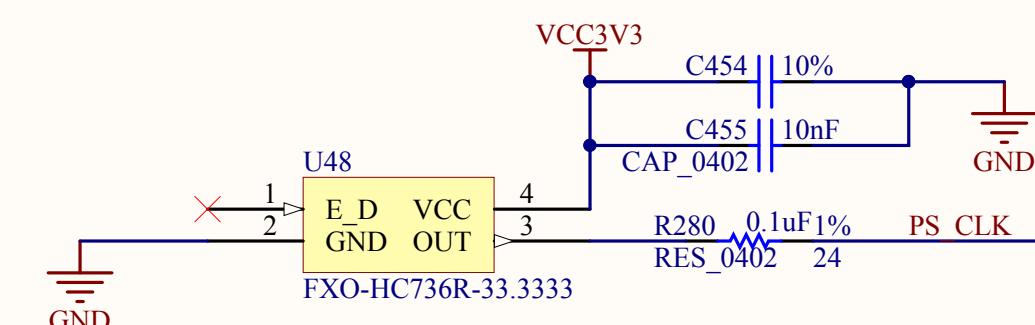
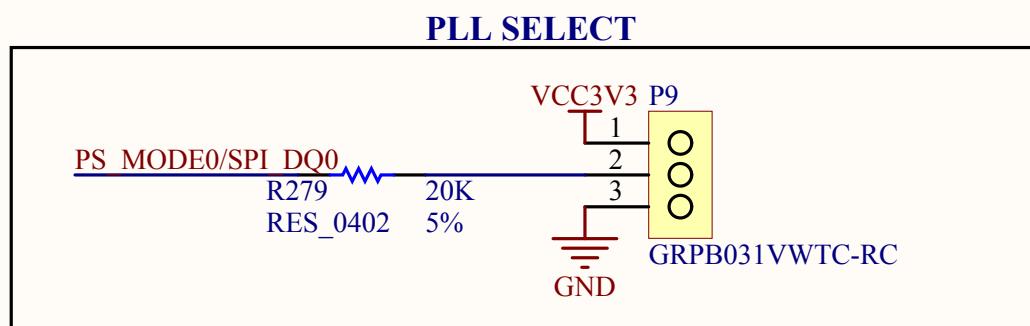
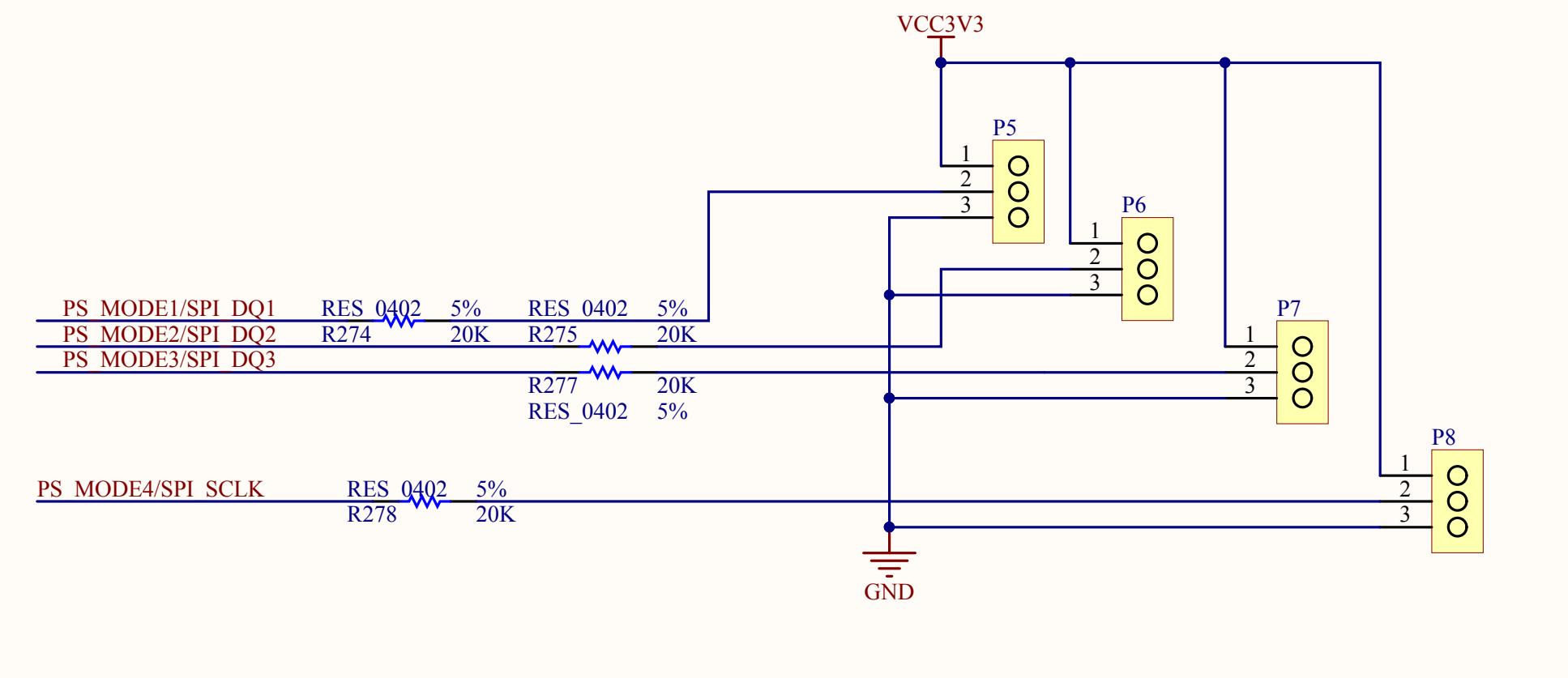
Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\ZYNQ_PL_Bank_35.SchDoc	Drawn By:

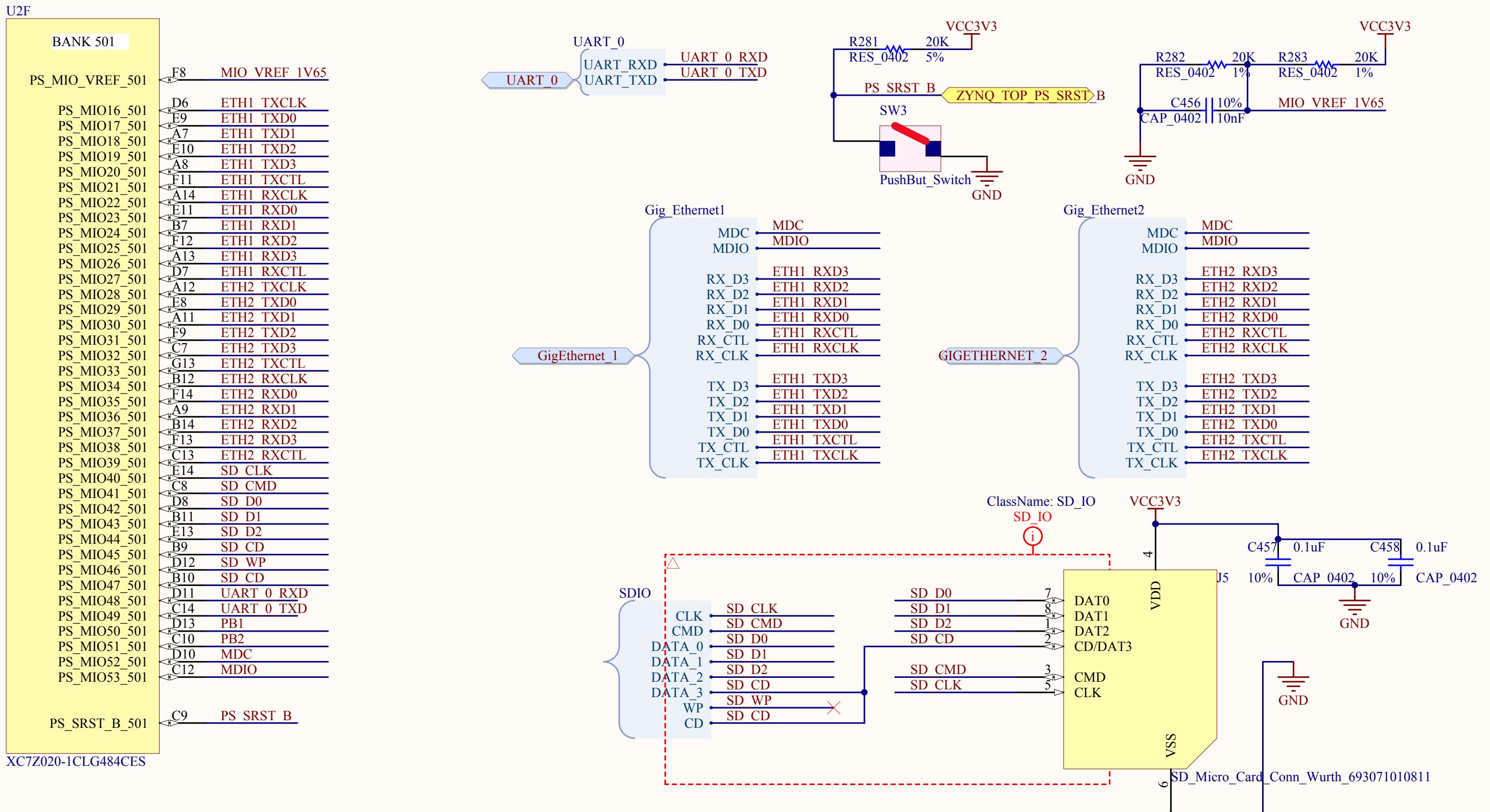


'PWR\_SHDN\_TRIG' SHOULD BE ONLY A TRIGGER:  
TO BE MADE HIGH FOR LIMITED CLOCK CYCLES &  
THEN, TURNED LOW

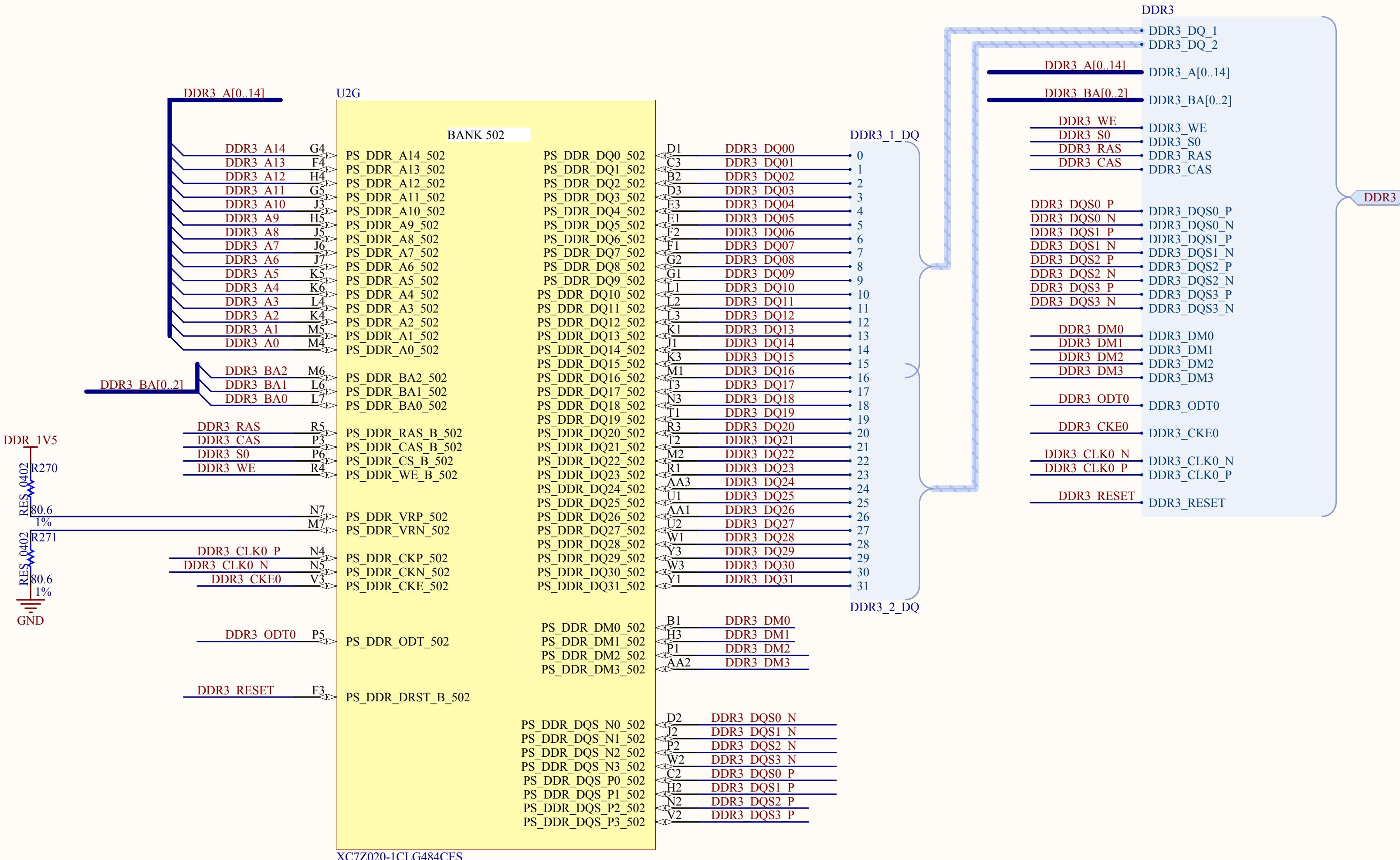


### BOOT ROM SELECT



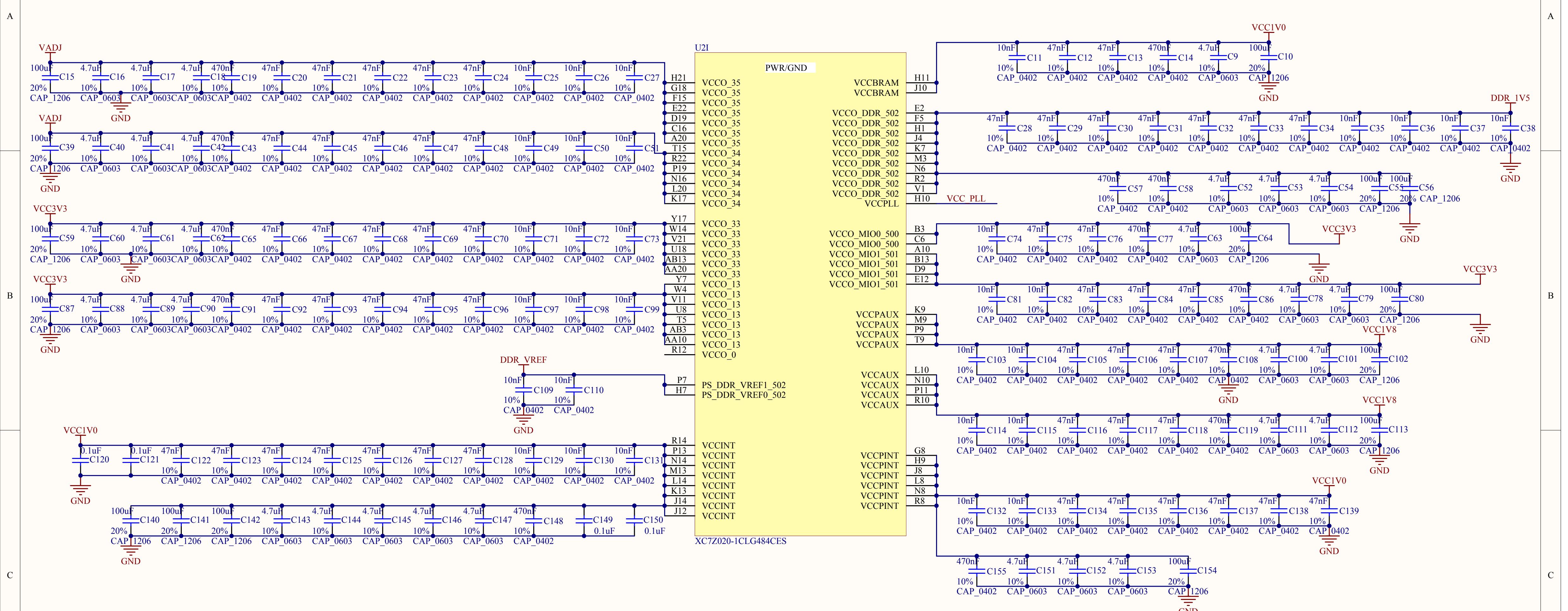


Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\ZYNQ_MIOBank_501.SchDoc	Drawn By:



DDR3	• DDR3_DQ_1
	• DDR3_DQ_2
<b>DDR3_A[0..14]</b>	DDR3_A[0..14]
<b>DDR3_BA[0..2]</b>	DDR3_BA[0..2]
DDR3_WE	DDR3_WE
DDR3_S0	DDR3_S0
DDR3_RAS	DDR3_RAS
DDR3_CAS	DDR3_CAS
DDR3_DQS0_P	DDR3_DQS0_P
DDR3_DQS0_N	DDR3_DQS0_N
DDR3_DQS1_P	DDR3_DQS1_P
DDR3_DQS1_N	DDR3_DQS1_N
DDR3_DQS2_P	DDR3_DQS2_P
DDR3_DQS2_N	DDR3_DQS2_N
DDR3_DQS3_P	DDR3_DQS3_P
DDR3_DQS3_N	DDR3_DQS3_N
DDR3_DM0	DDR3_DM0
DDR3_DM1	DDR3_DM1
DDR3_DM2	DDR3_DM2
DDR3_DM3	DDR3_DM3
DDR3_ODT0	DDR3_ODT0
DDR3_CKE0	DDR3_CKE0
DDR3_CLK0_N	DDR3_CLK0_N
DDR3_CLK0_P	DDR3_CLK0_P
DDR3_RESET	DDR3_RESET

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\ZYNN DDR3 Bank 502.Sch	Drawn By:



Title		
Size	Number	Revision
A3		
Date:	6/4/2013	Sheet of
File:	C:\Users\...\ZYNNQ_Power.SchDoc	Drawn By:

A

A

B

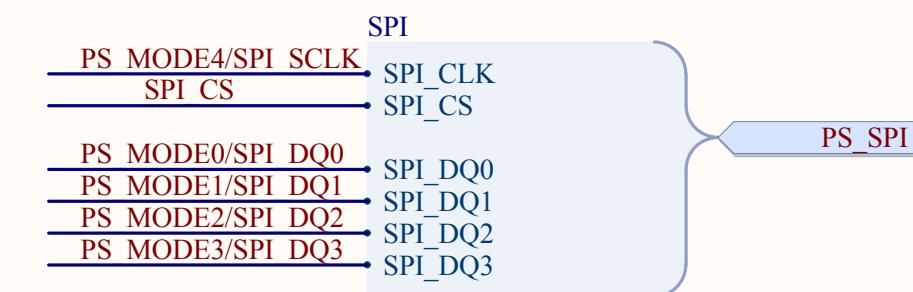
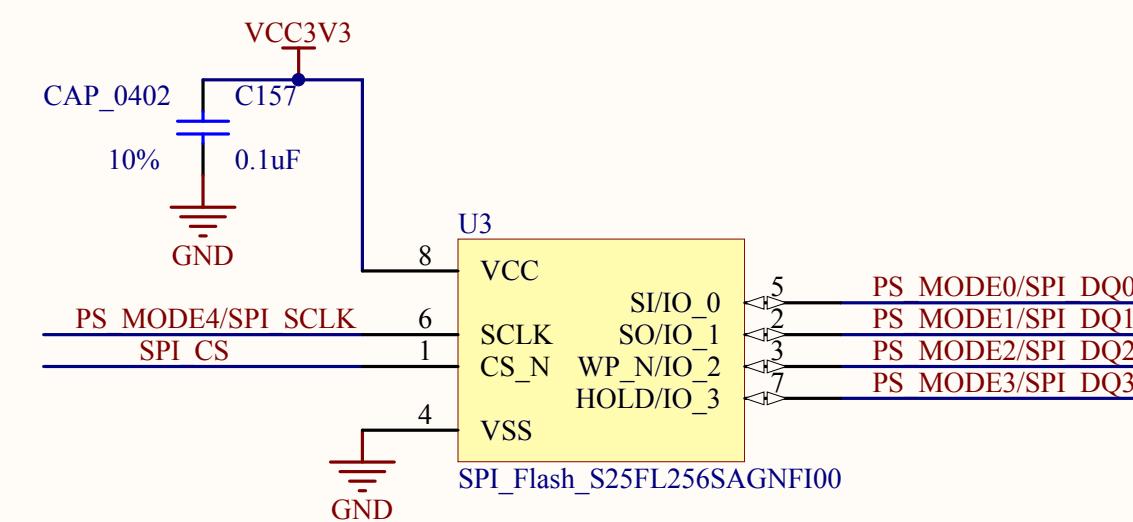
B

C

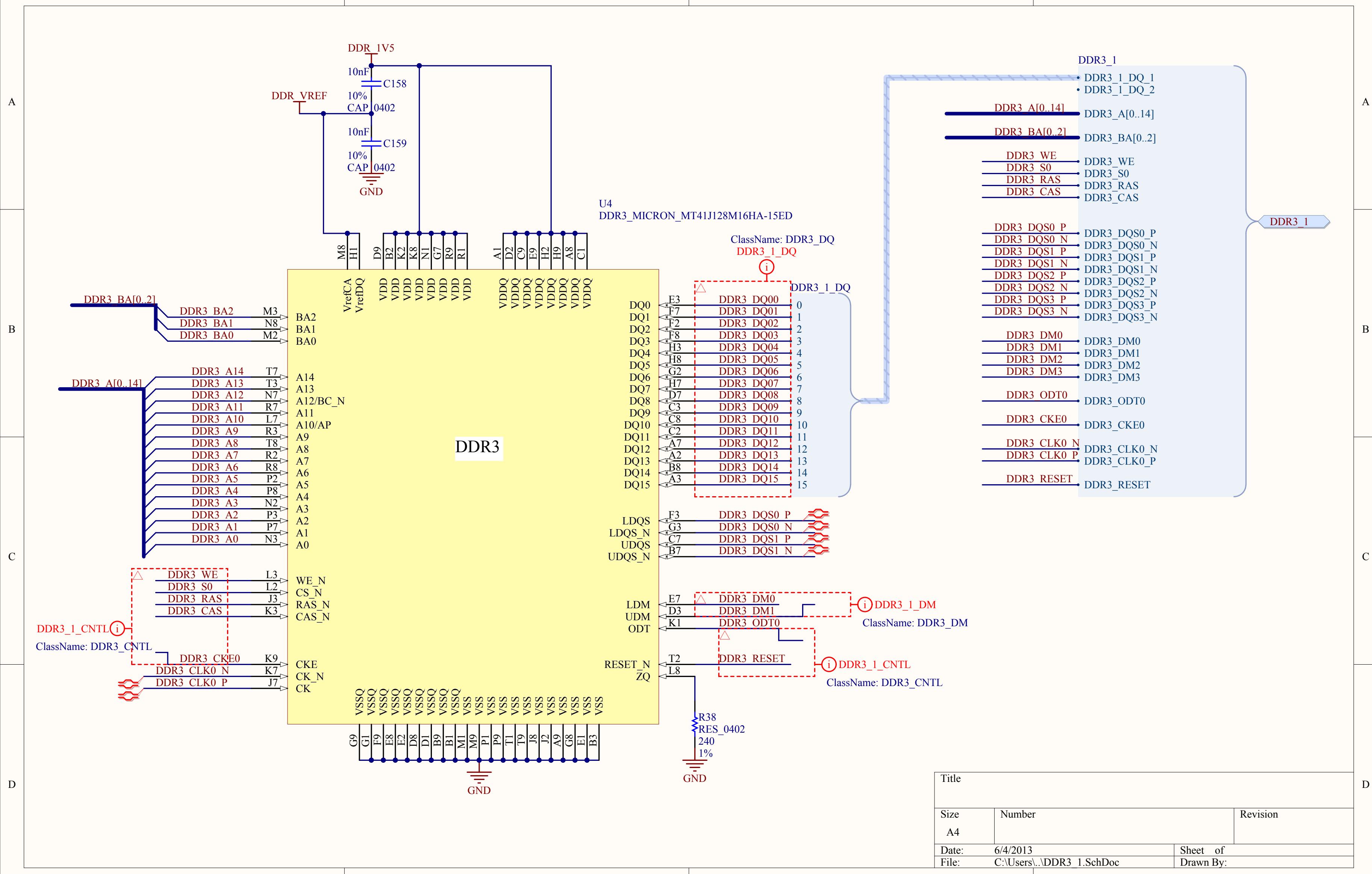
C

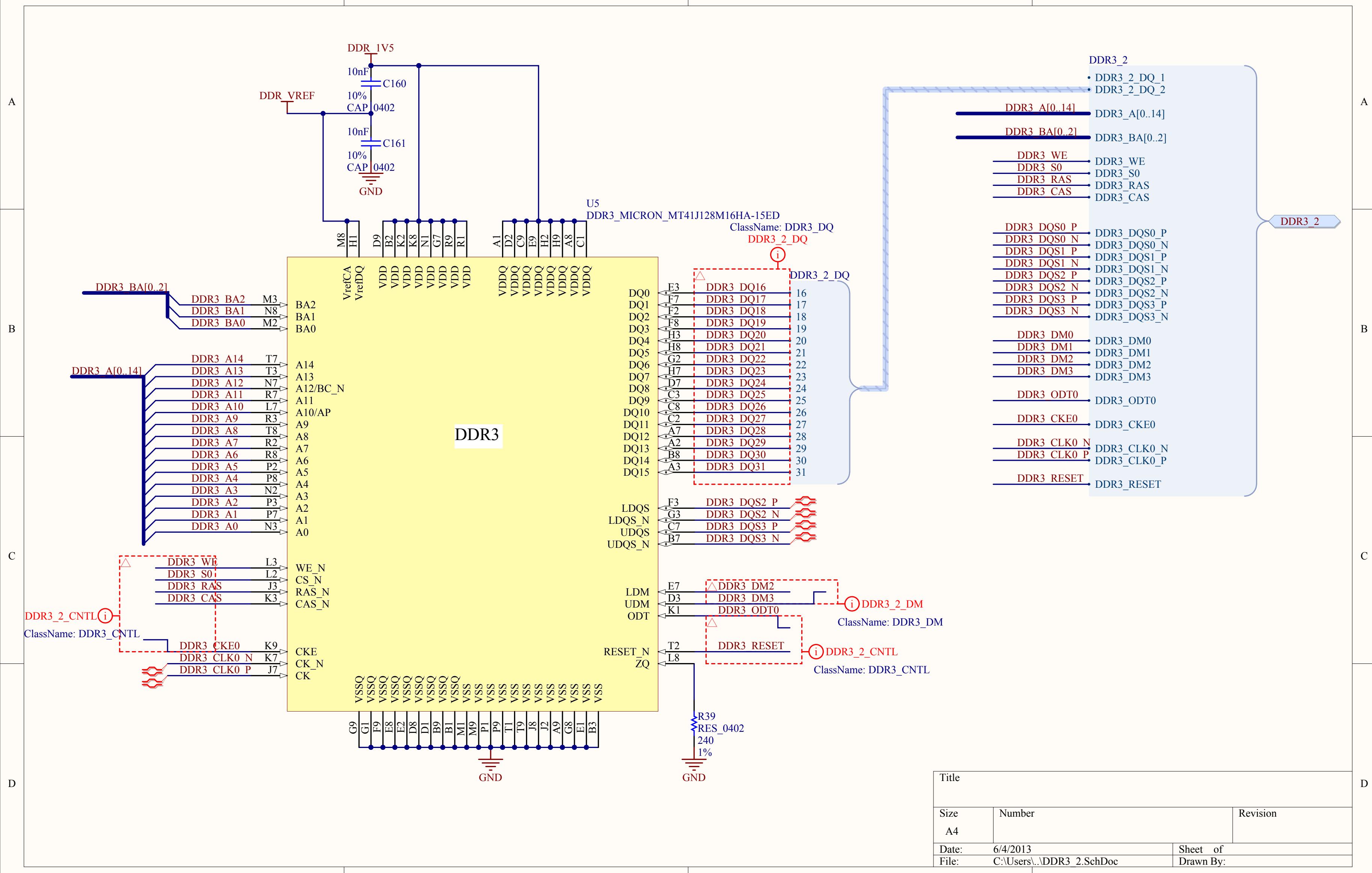
D

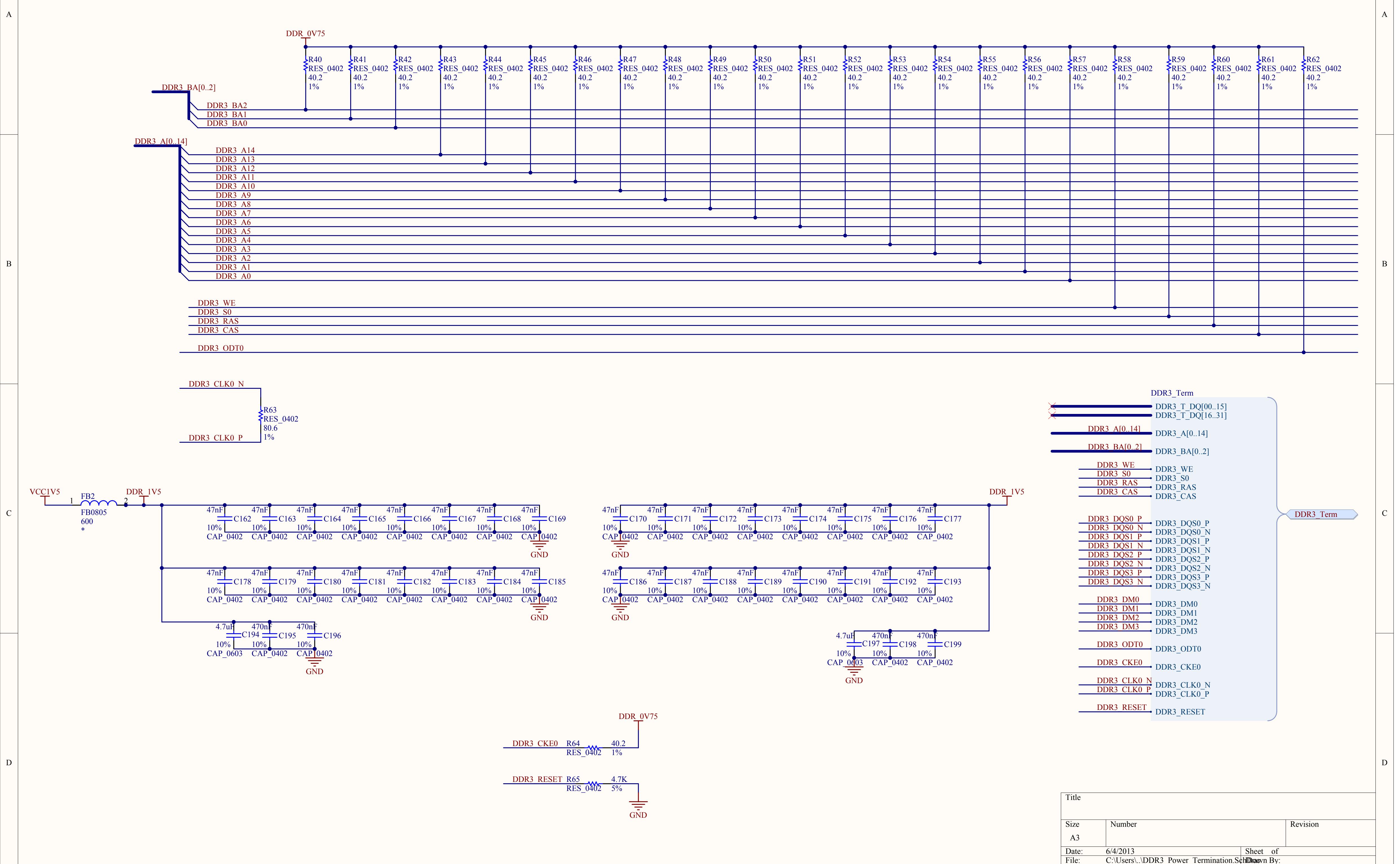
D

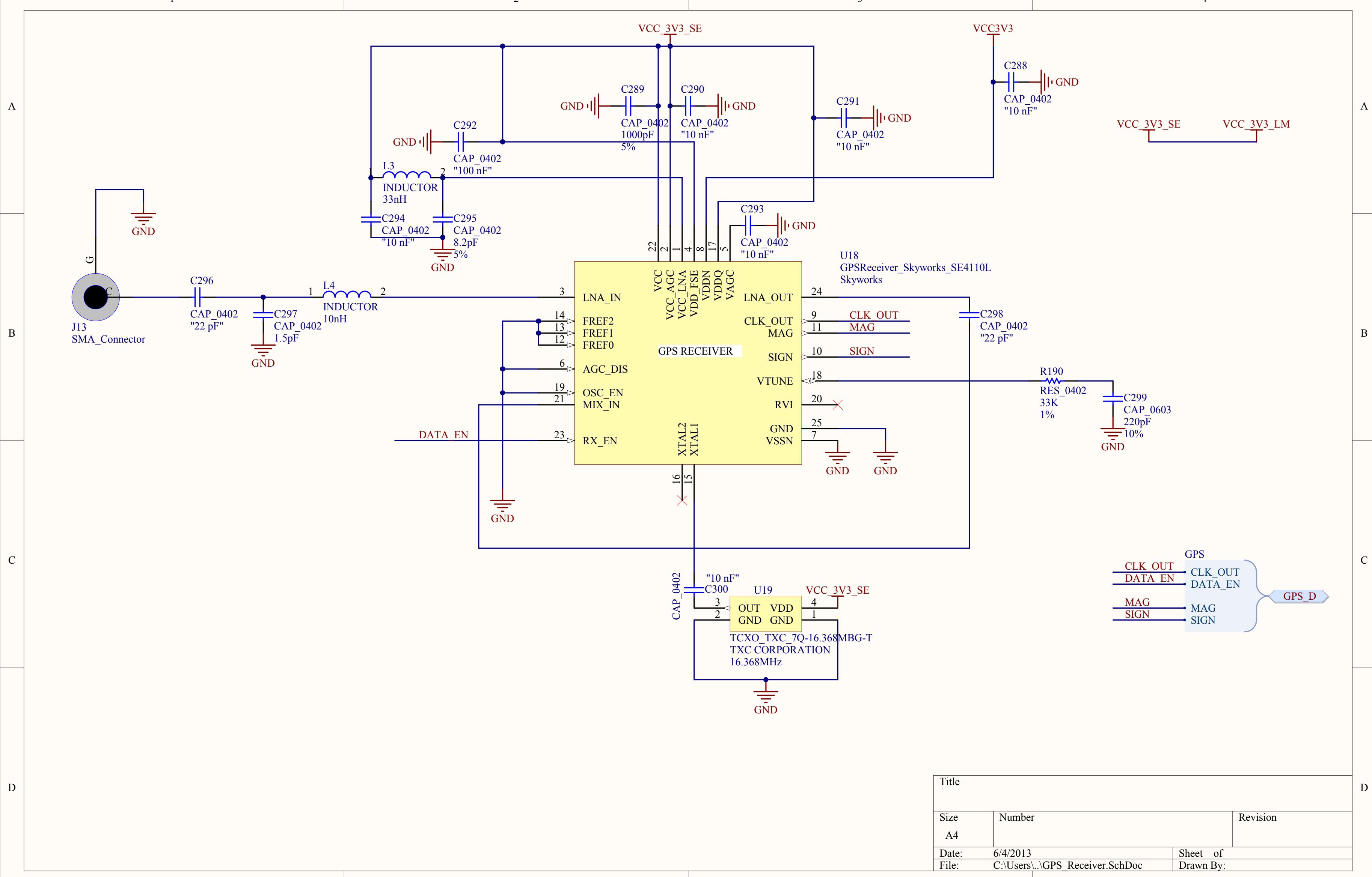


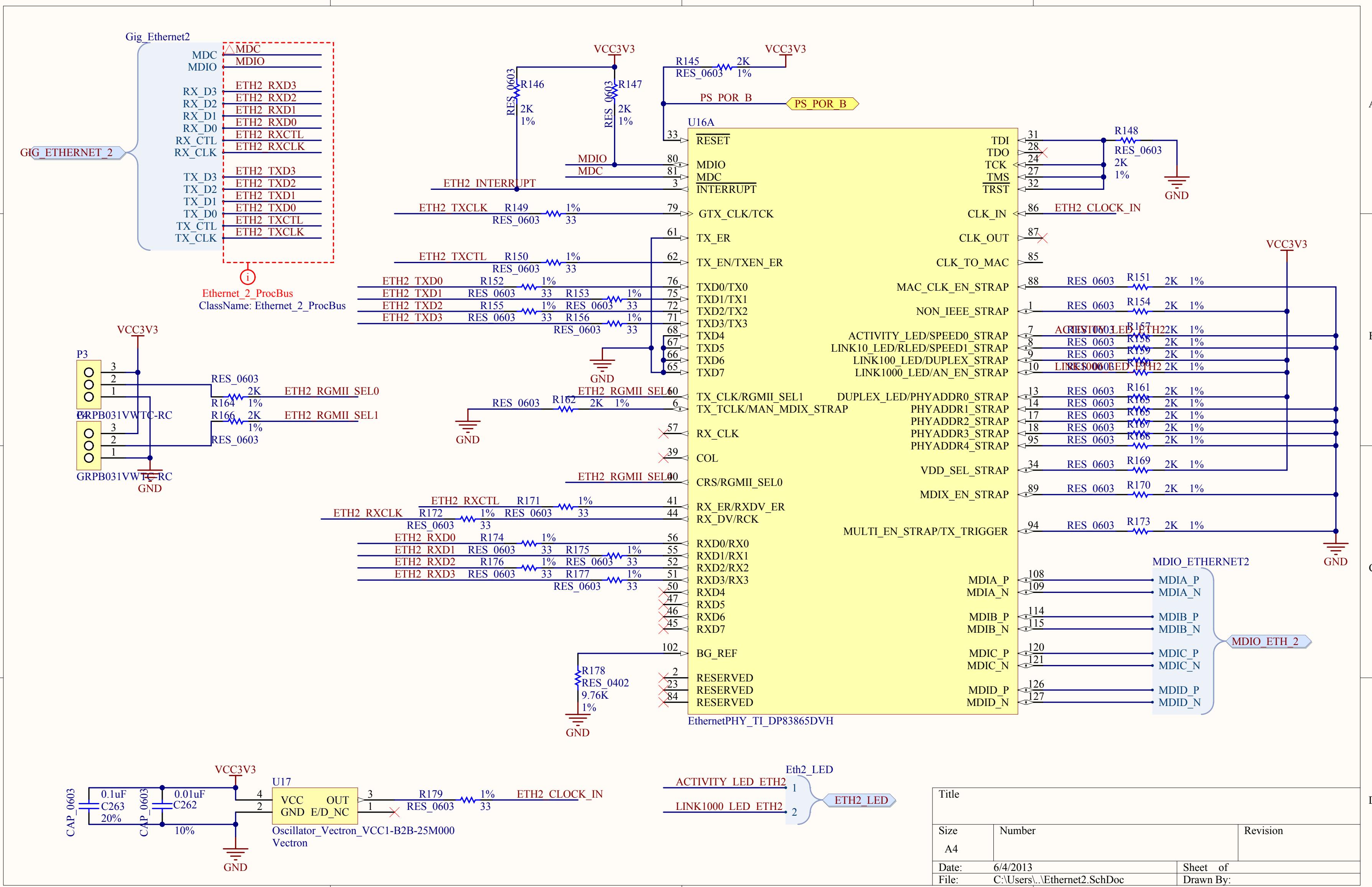
Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\BootFlash_SPI.SchDoc	Drawn By:











A

A

B

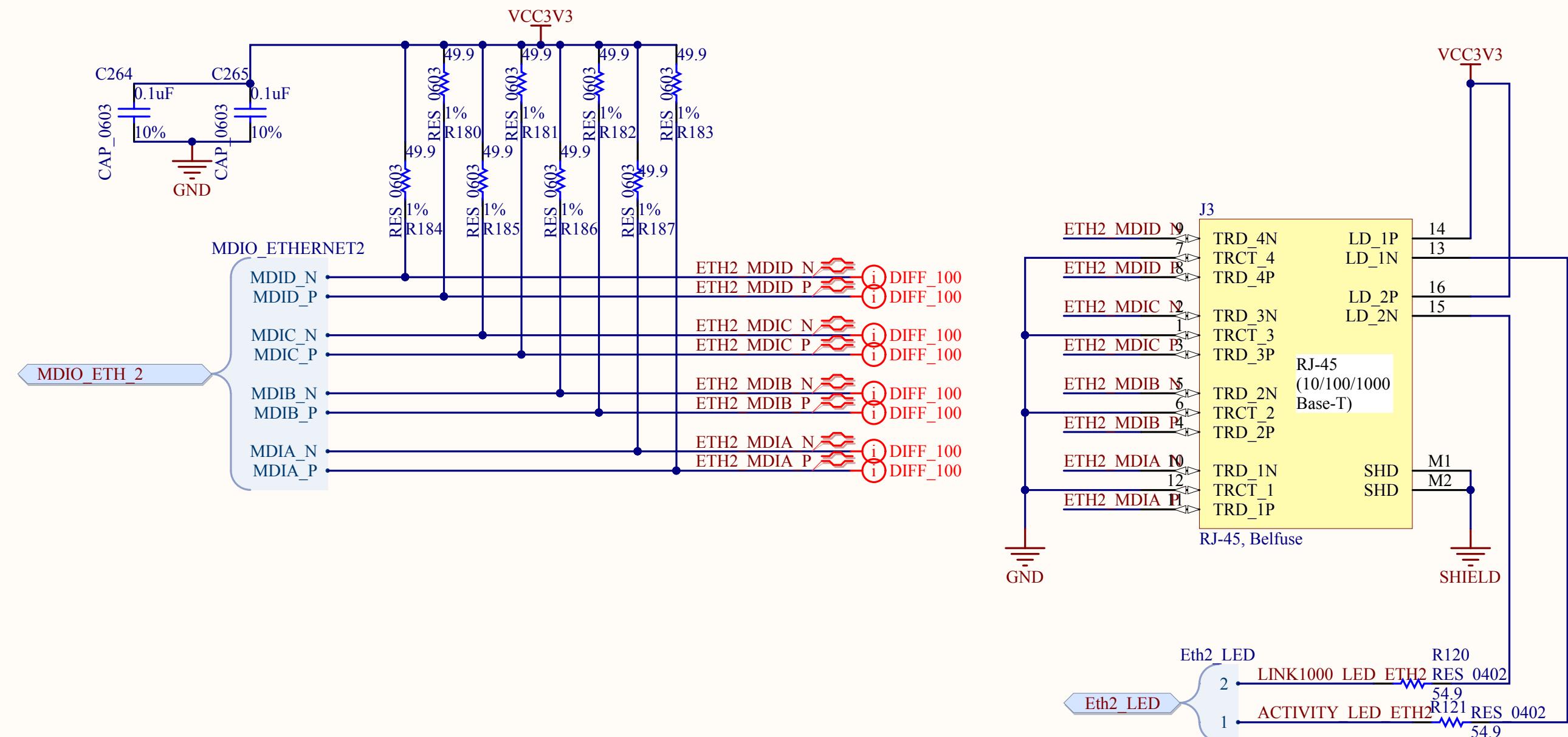
B

C

C

D

D



Title

Size

A4

Number

Revision

Date: 6/4/2013

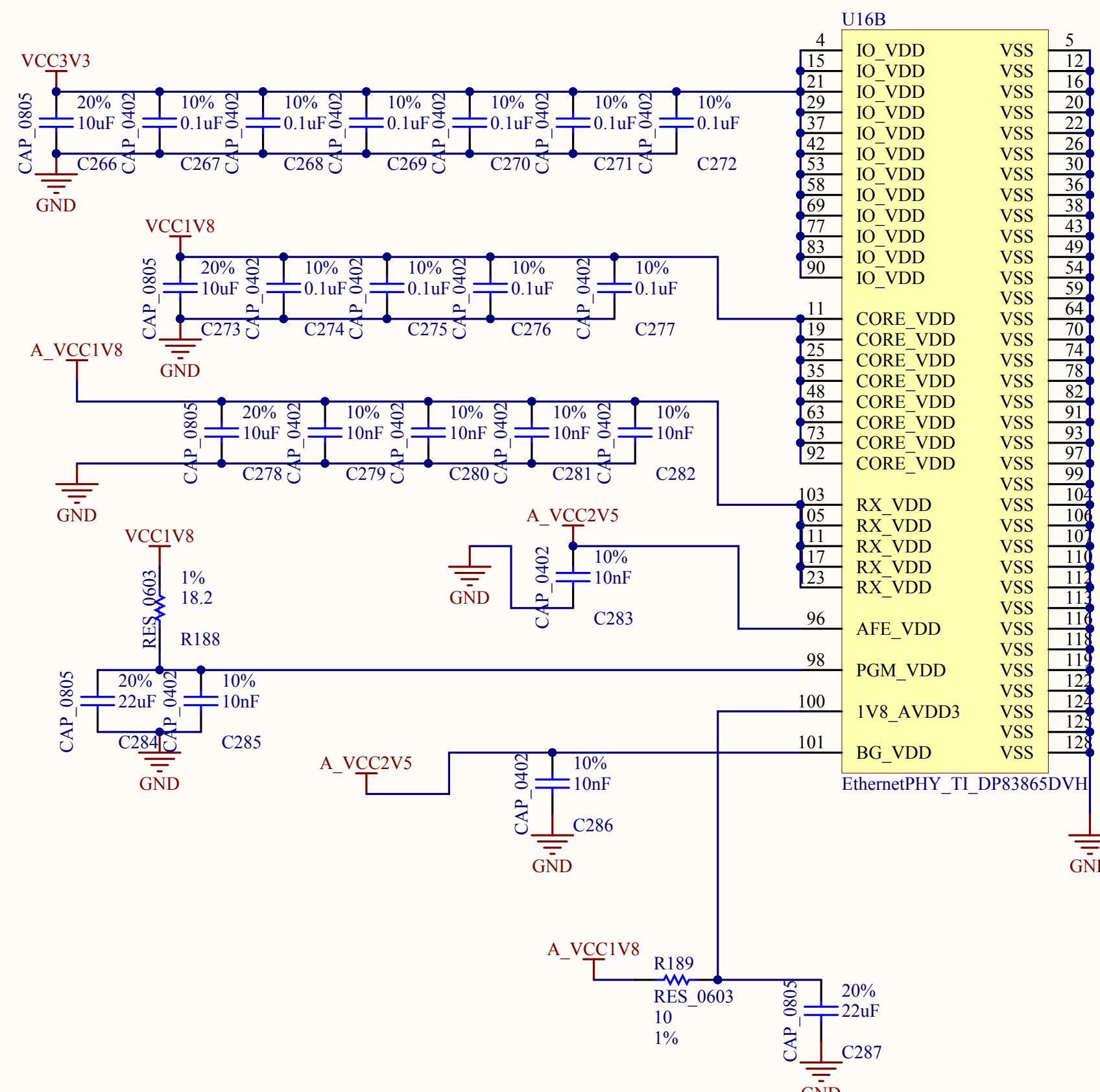
Sheet of

File: C:\Users\...\Ethernet2\_MDIO.SchDoc

Drawn By:

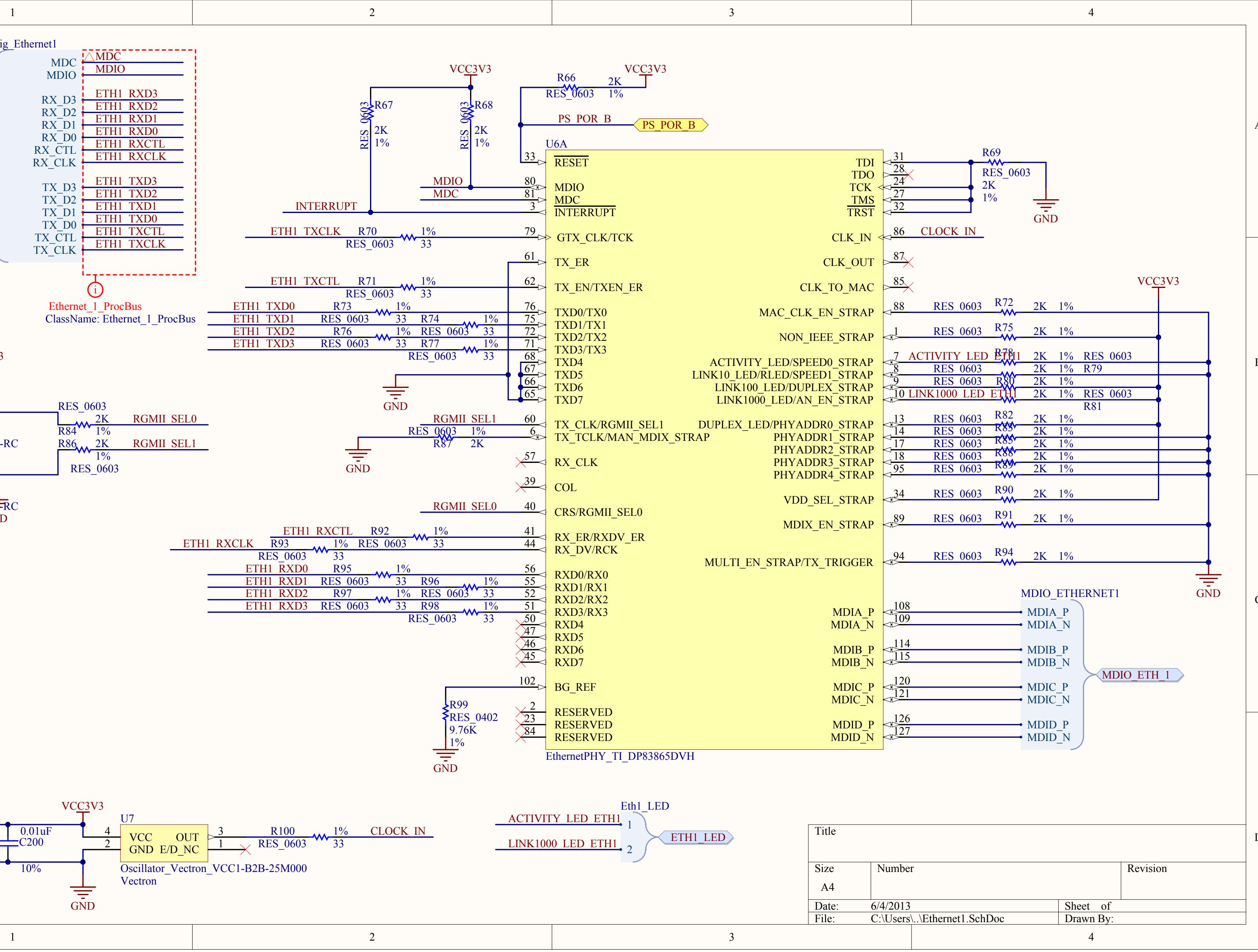
A

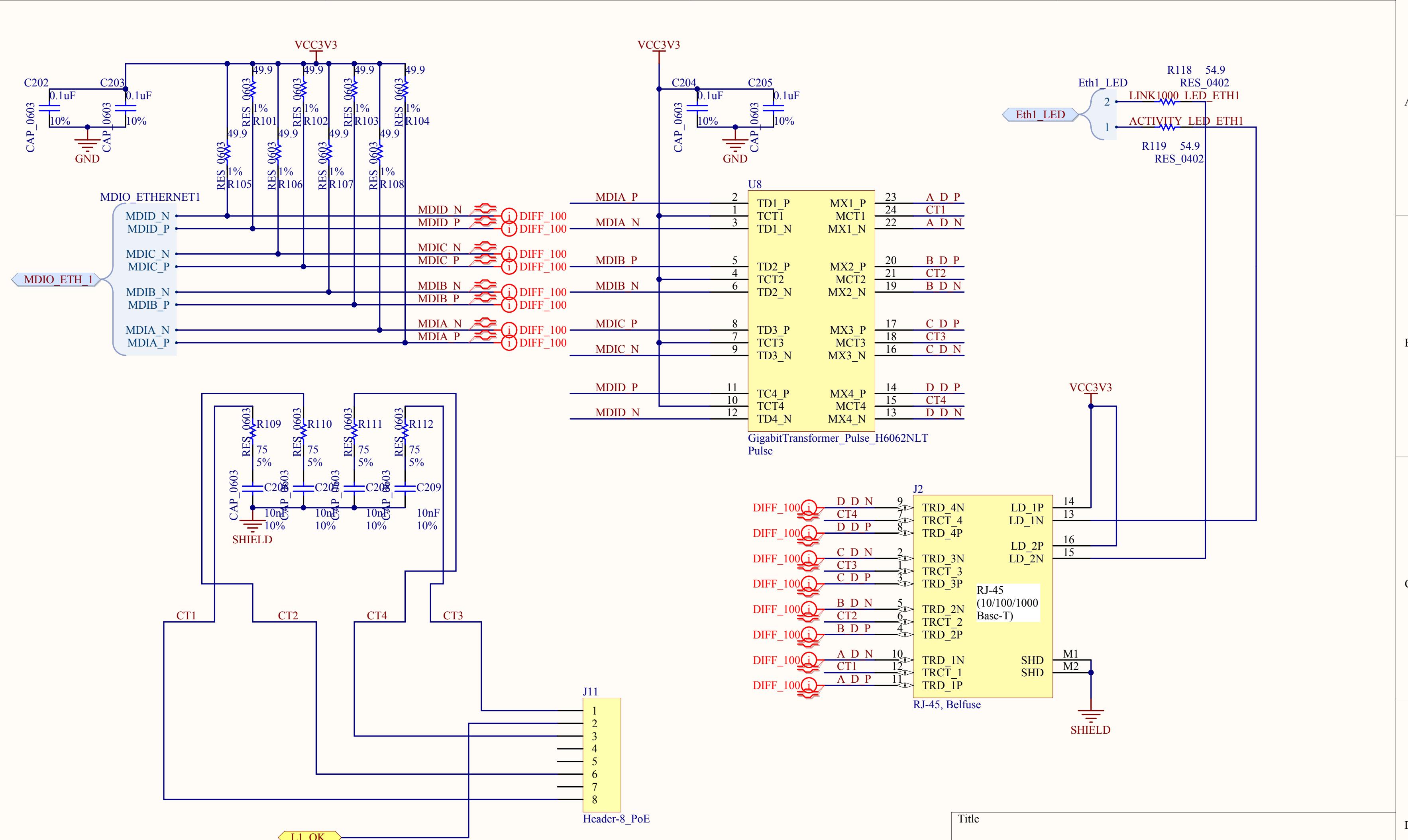
A



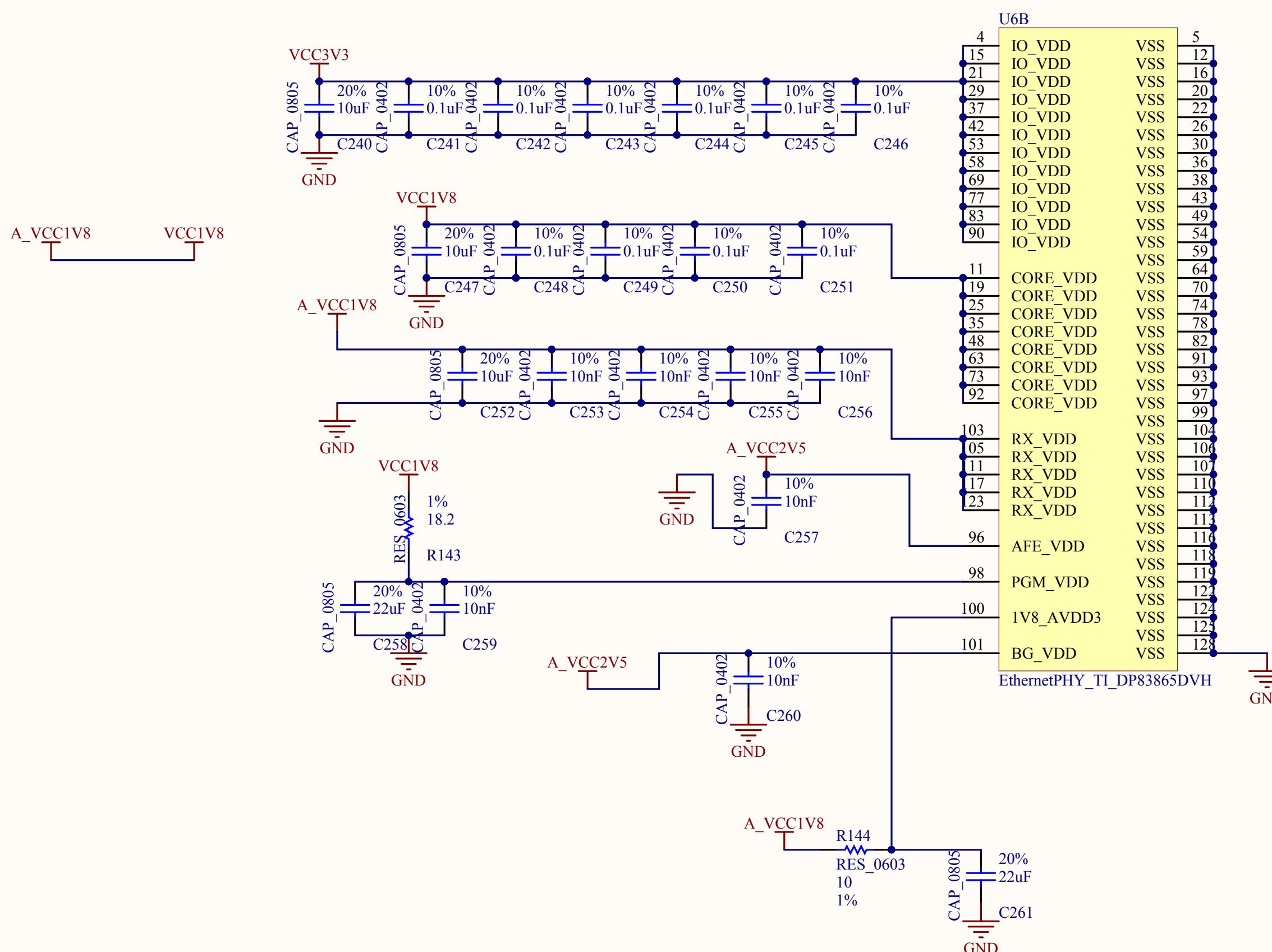
Title

Size A4	Number	Revision
Date:	6/4/2013	Sheet of
File:	C:\Users\..\Ethernet2 Power.SchDoc	Drawn By:





A



Title

Size

A4

Number

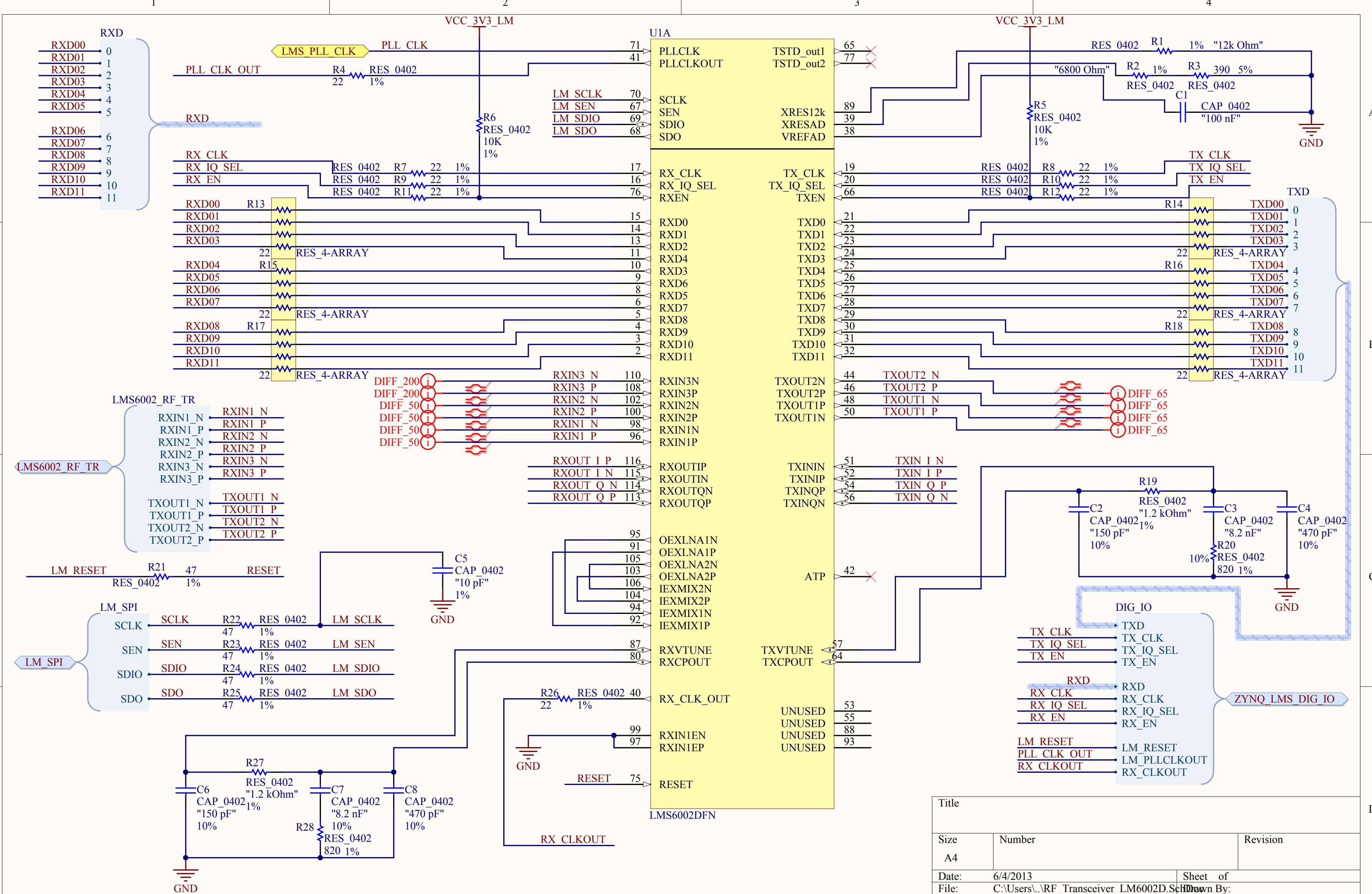
Revision

Date: 6/4/2013

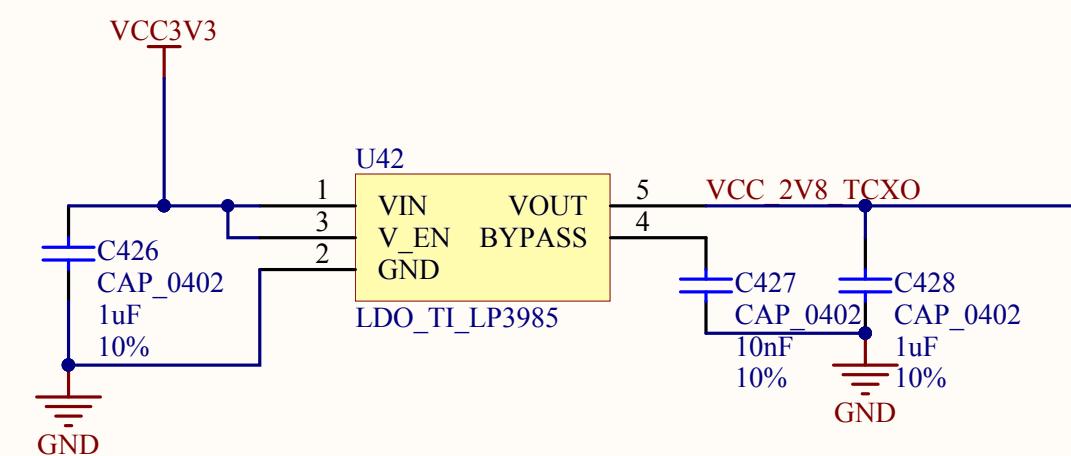
Sheet of

File: C:\Users\.\Ethernet1 Power.SchDoc

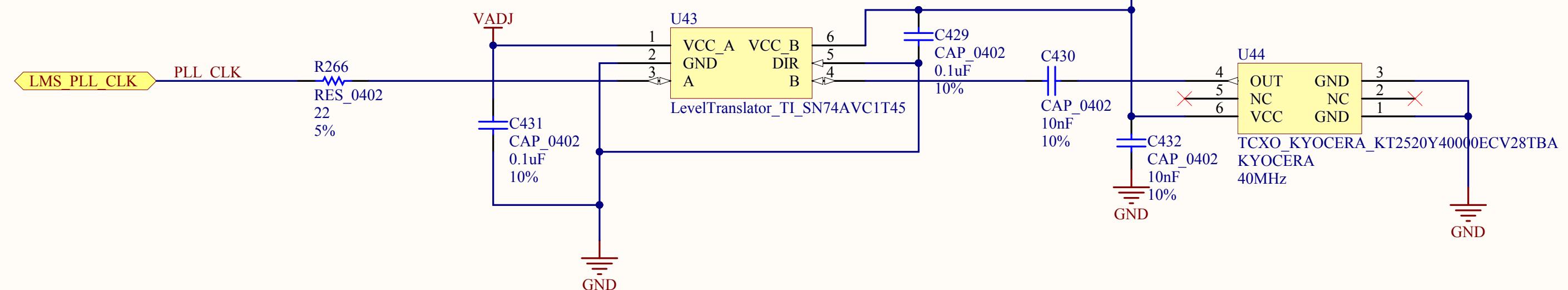
Drawn By:



A



A



B

C

C

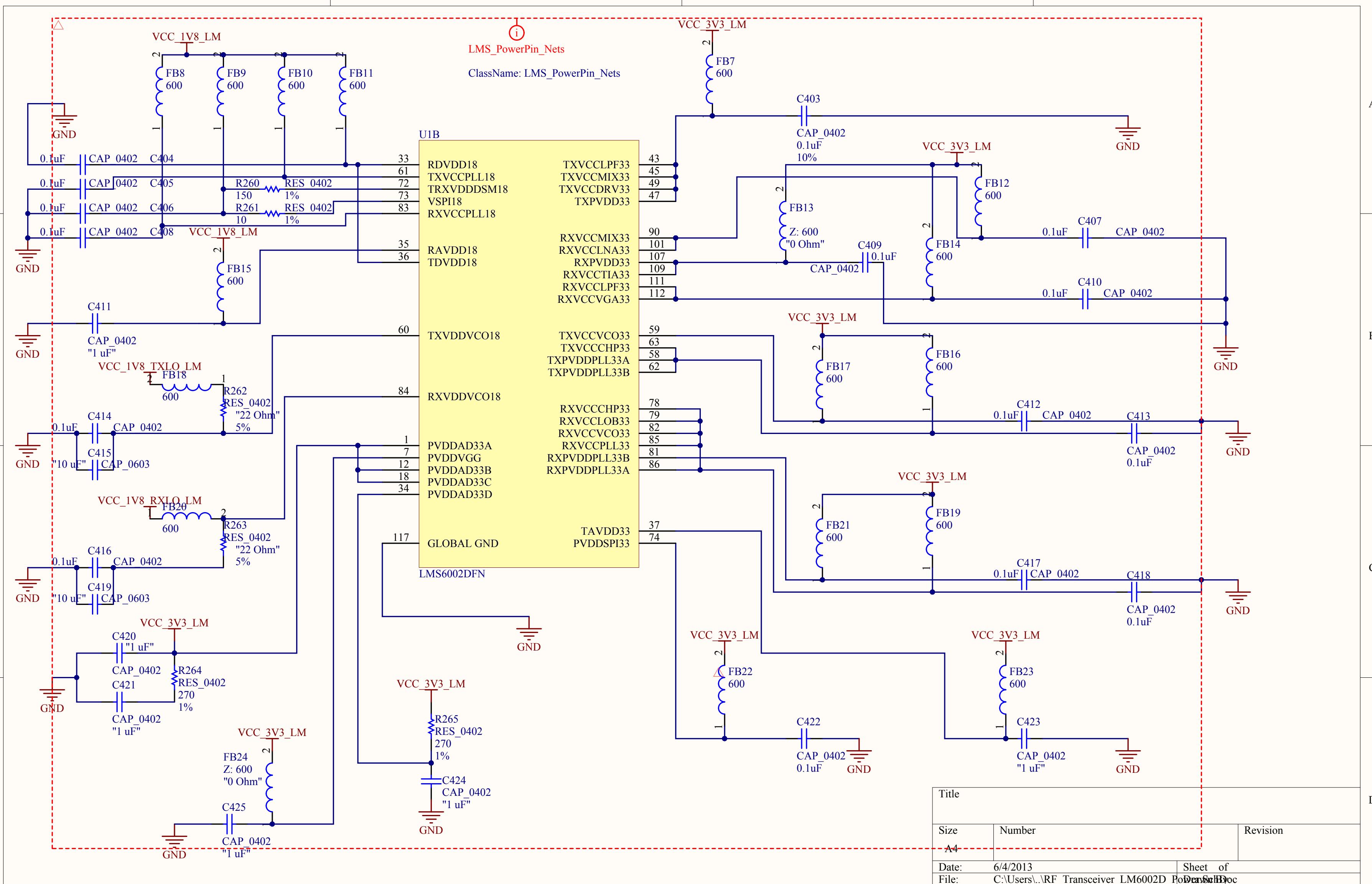
D

D

Title

Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\RF Transceiver LMS6002 PLD\6WKBchDoc	

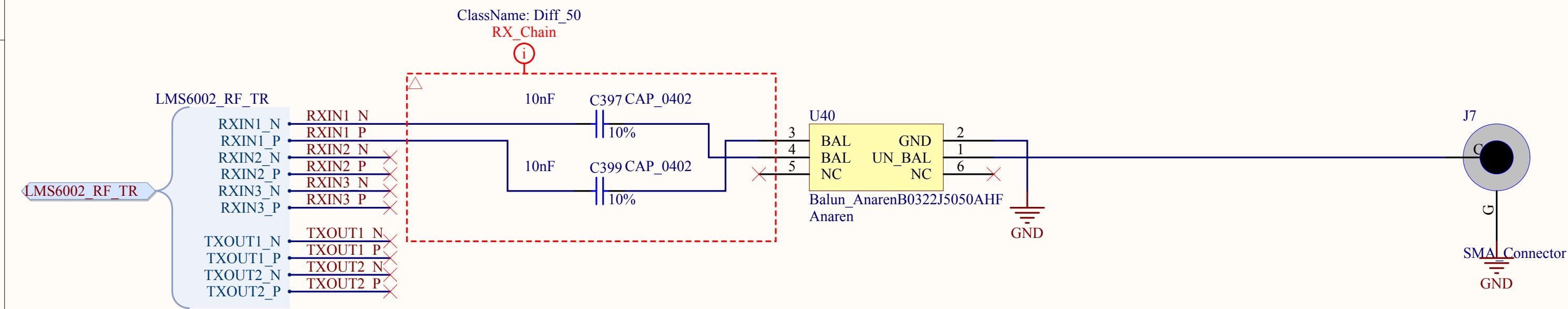
1 2 3 4



1 2 3 4

A

A



B

B

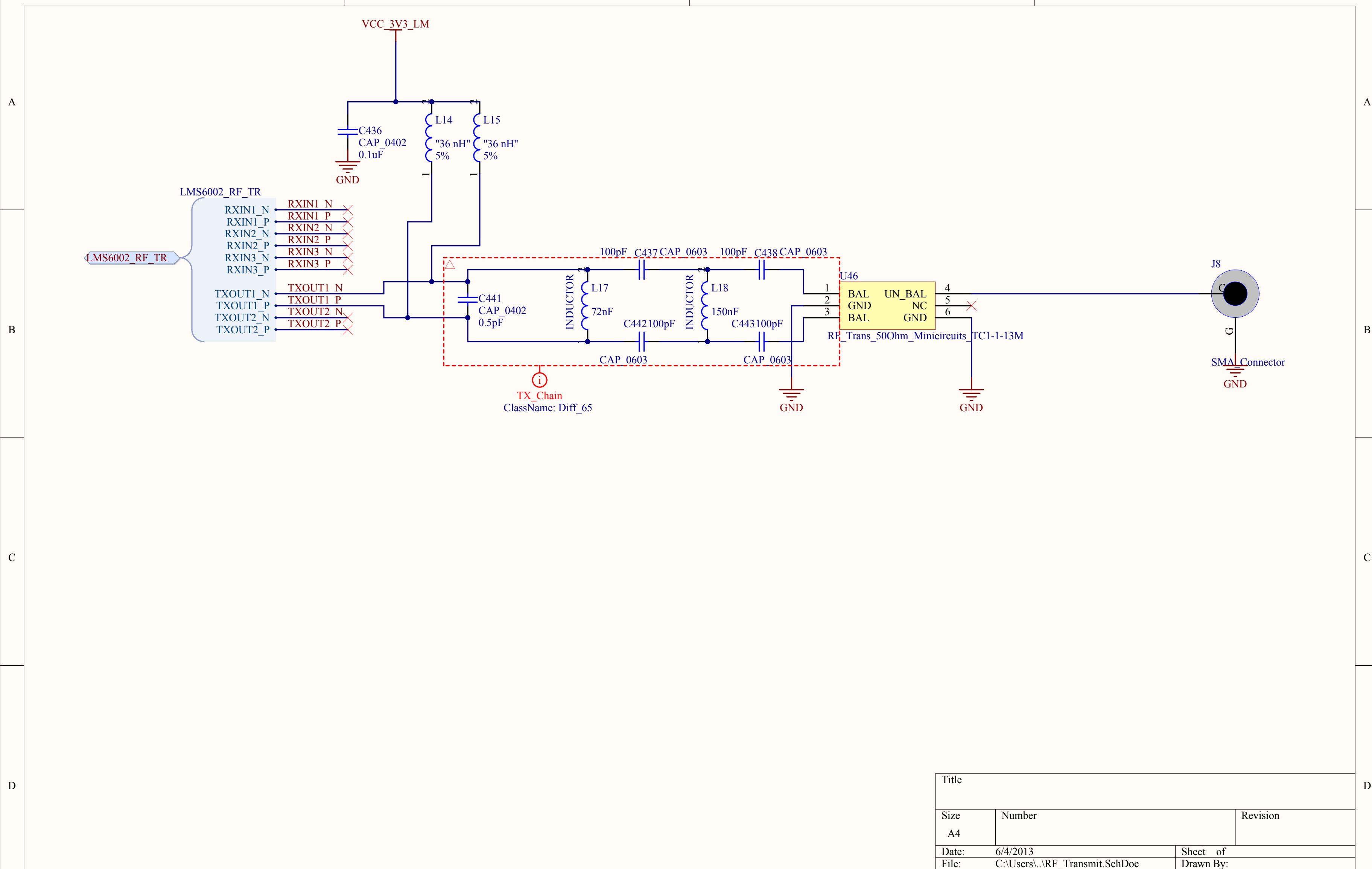
C

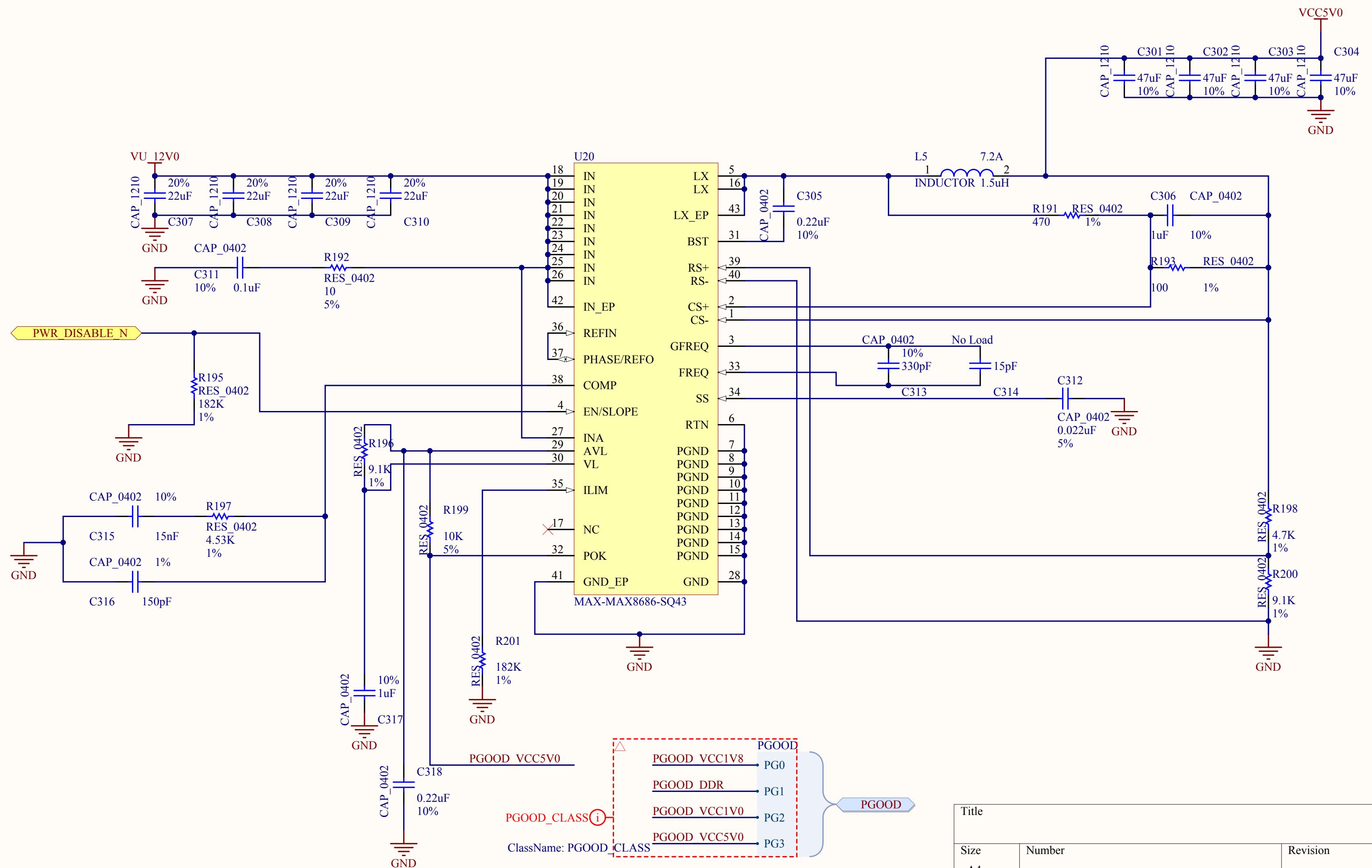
C

D

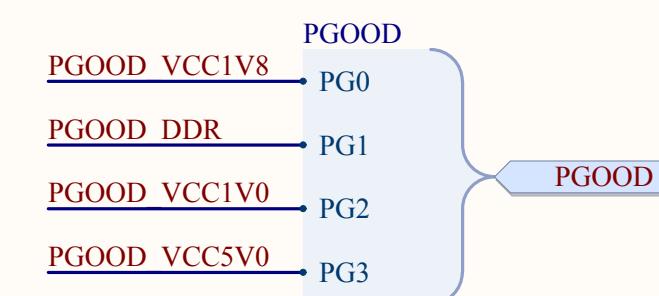
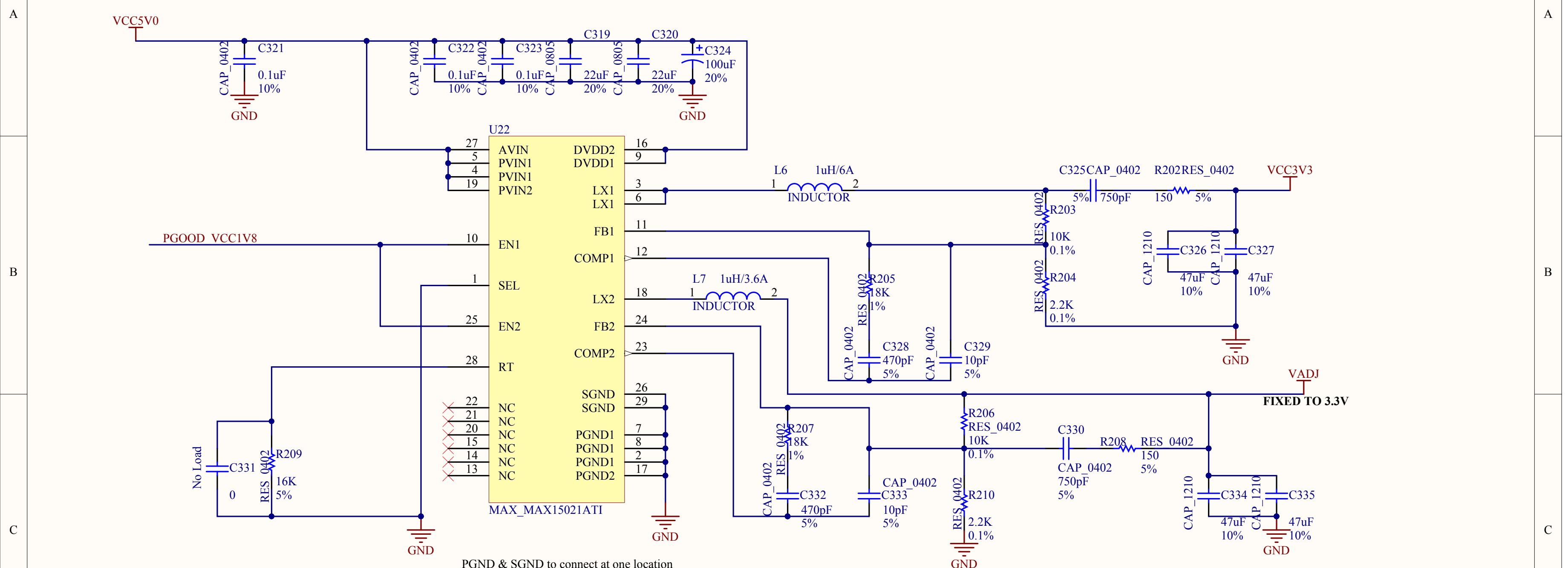
D

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\RF_Receive.SchDoc	Drawn By:

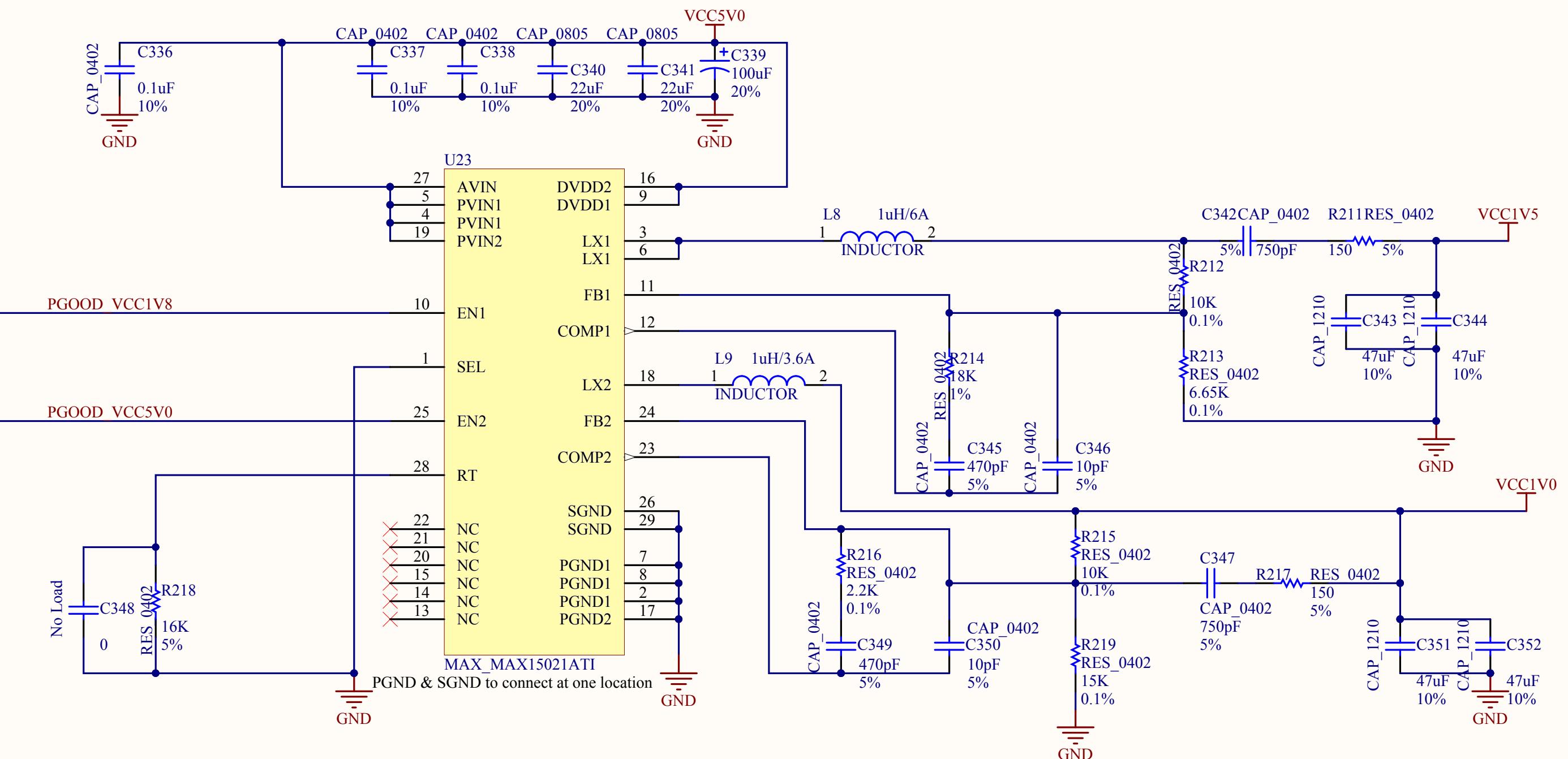




Title	
Size	Number
A4	
Date:	6/4/2013
File:	C:\Users\..\Power Regulators Digital 1.\$DRAFT By:



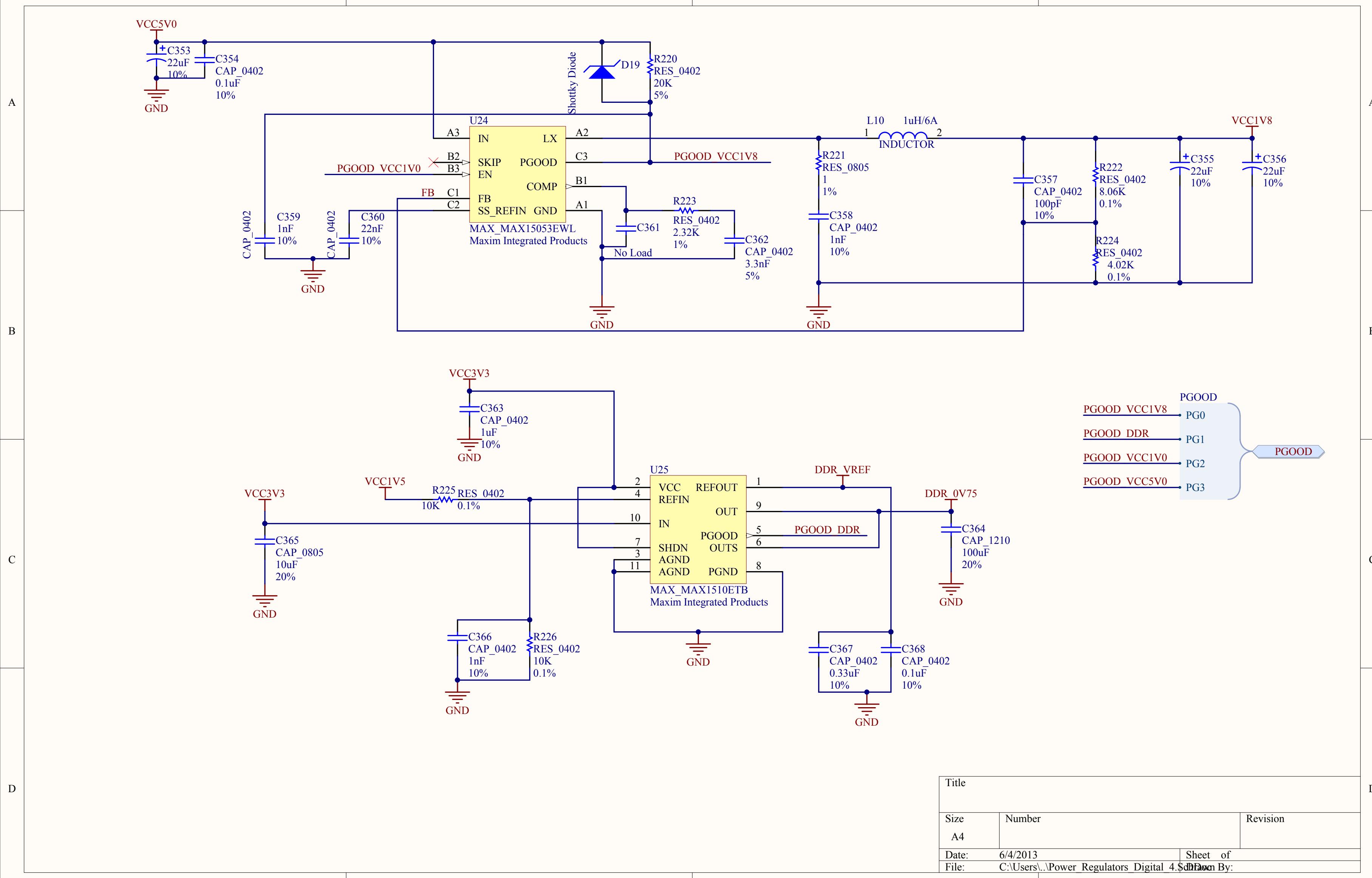
Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\Power Regulators Digital 2.schDoc	By:

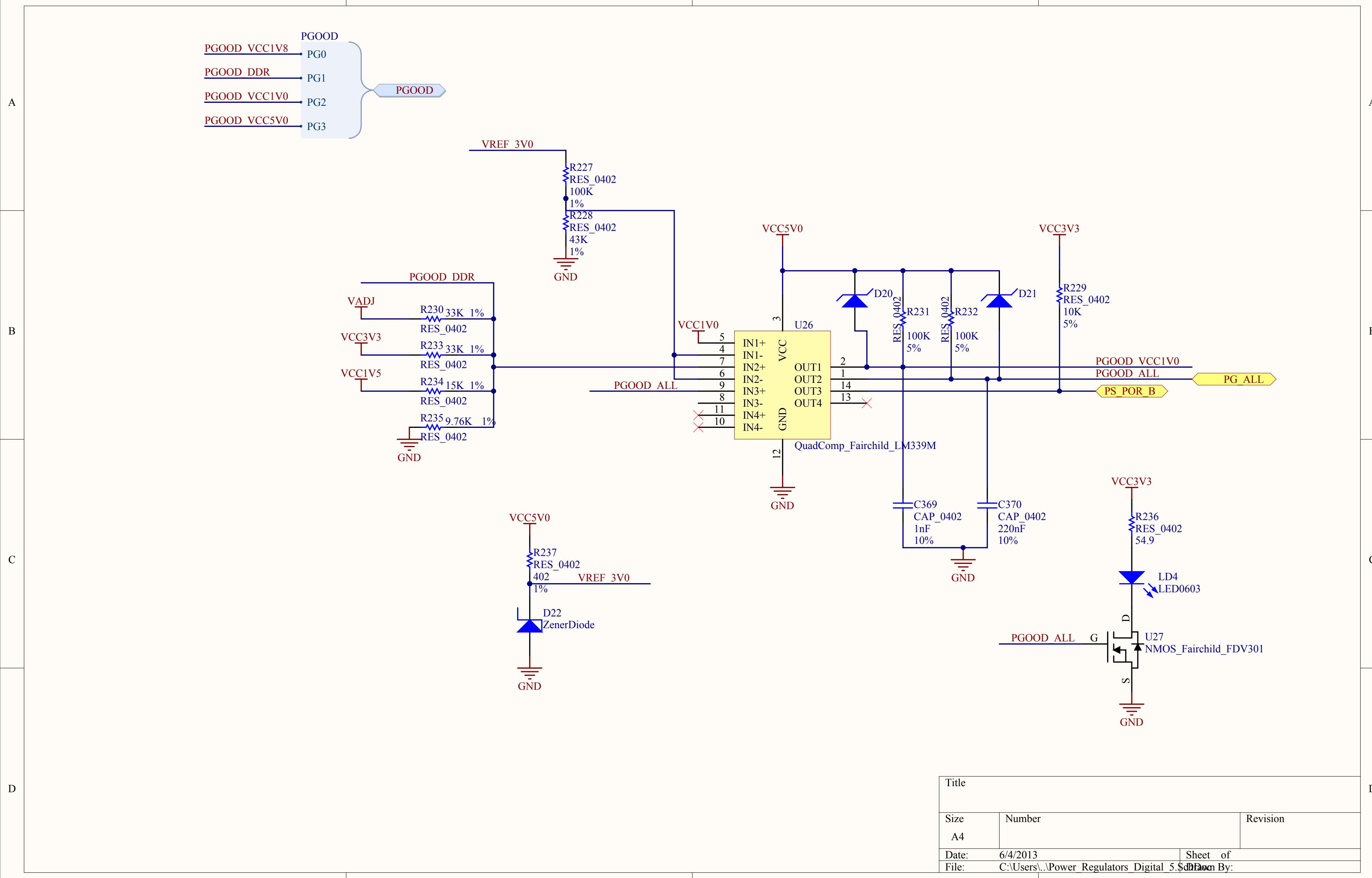


PGOOD  
PGOOD DDR  
PGOOD VCC1V0  
PGOOD VCC5V0

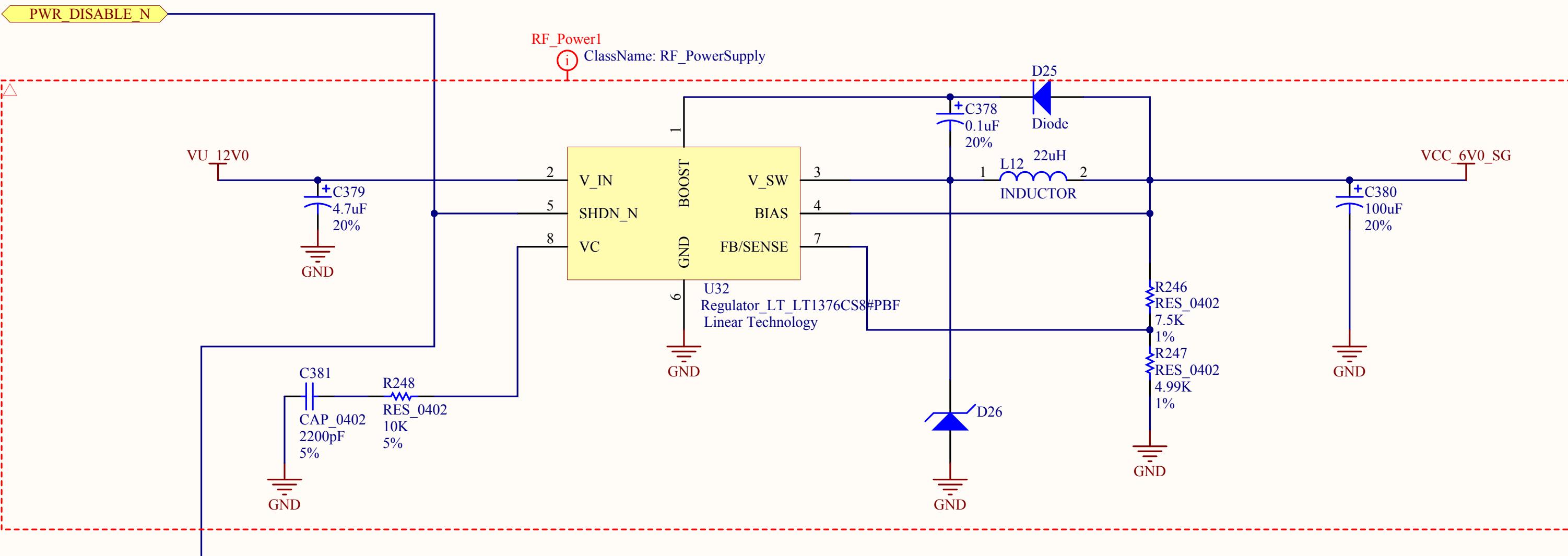
PGOOD

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\Power Regulators Digital 3.schDoc	3

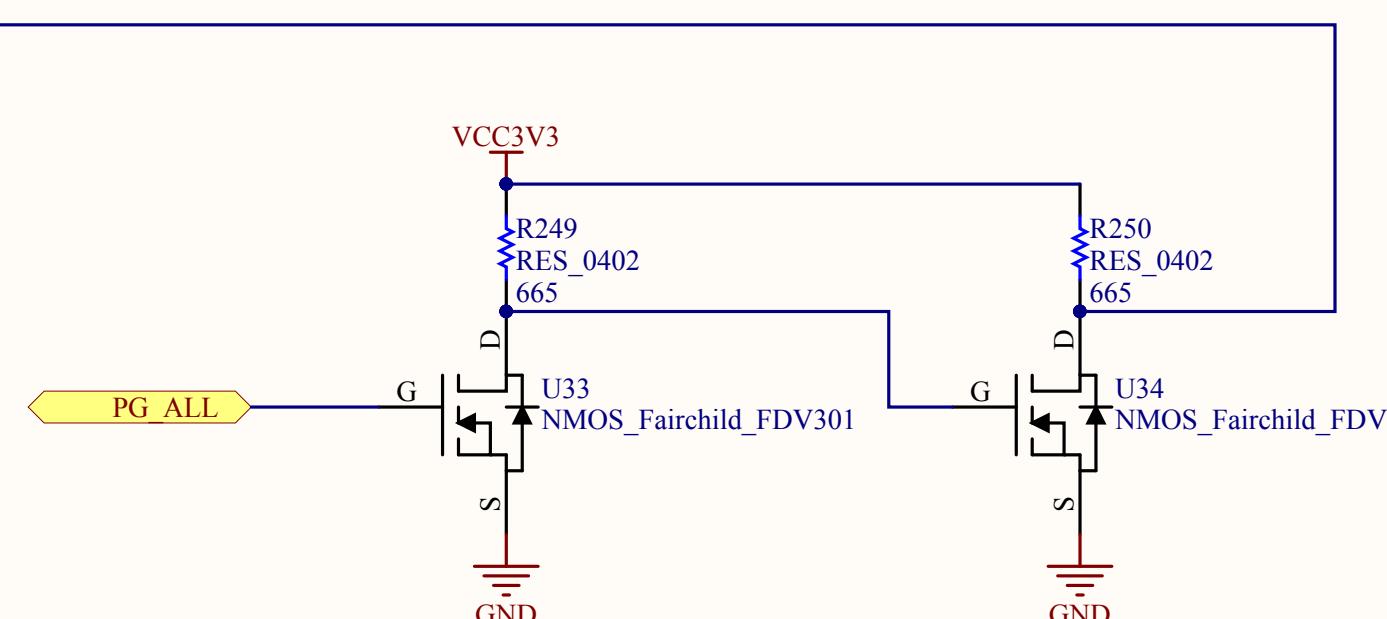




A



B

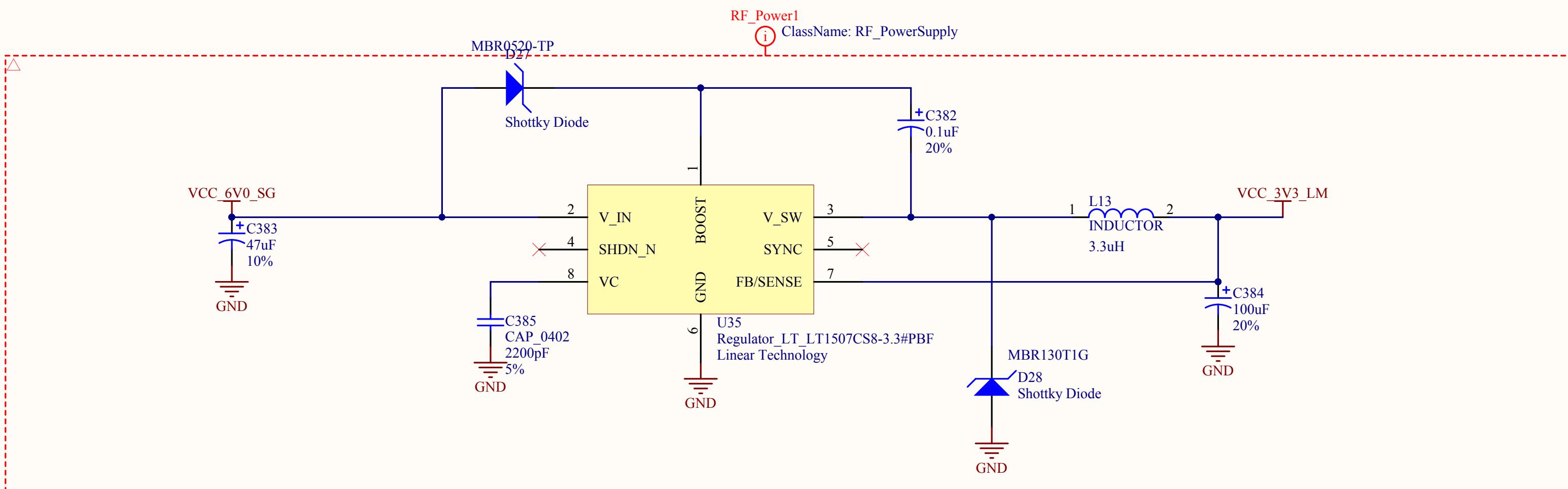


C

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\Power_Regulators_RF_2.SchDoc	Drawn By:

A

A



B

B

C

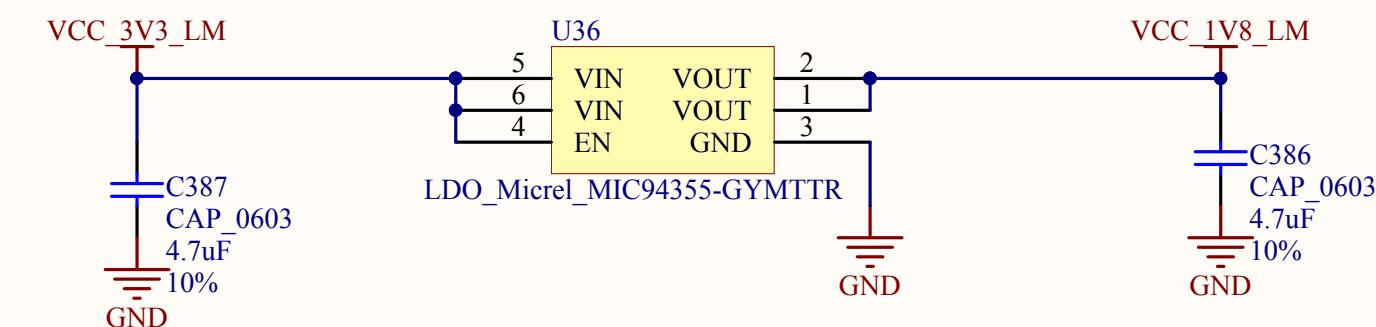
C

D

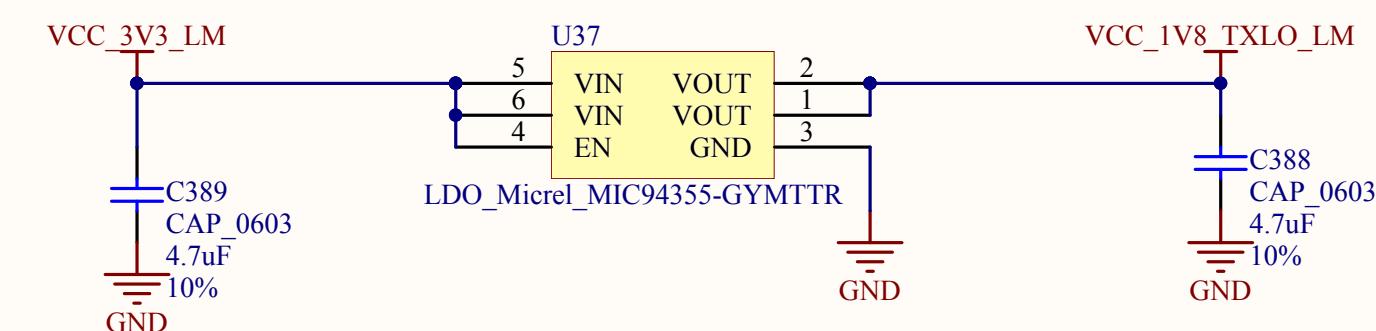
D

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\Power_Regulators_RF_3.SchDoc	Drawn By:

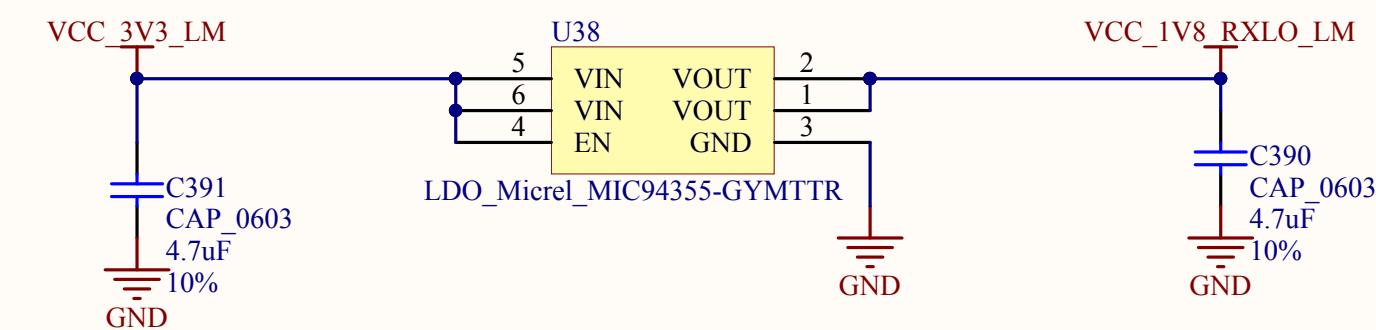
A



B



C



D

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\Power_Regulators_RF_4.SchDoc	Drawn By:

A

A

B

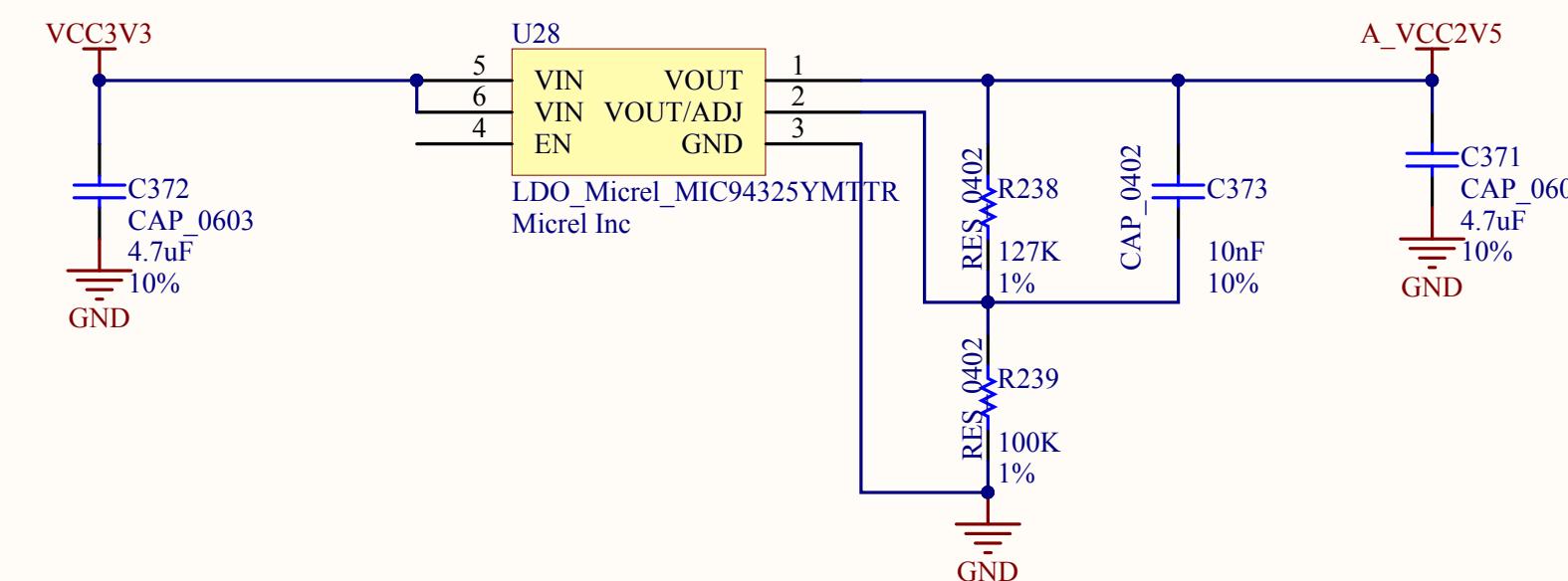
B

C

C

D

D



Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\Power_Regulators_Ether2V5.SchDoc	Download By:

A

A

B

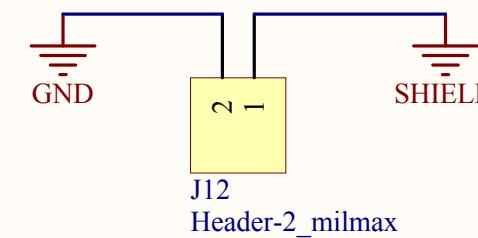
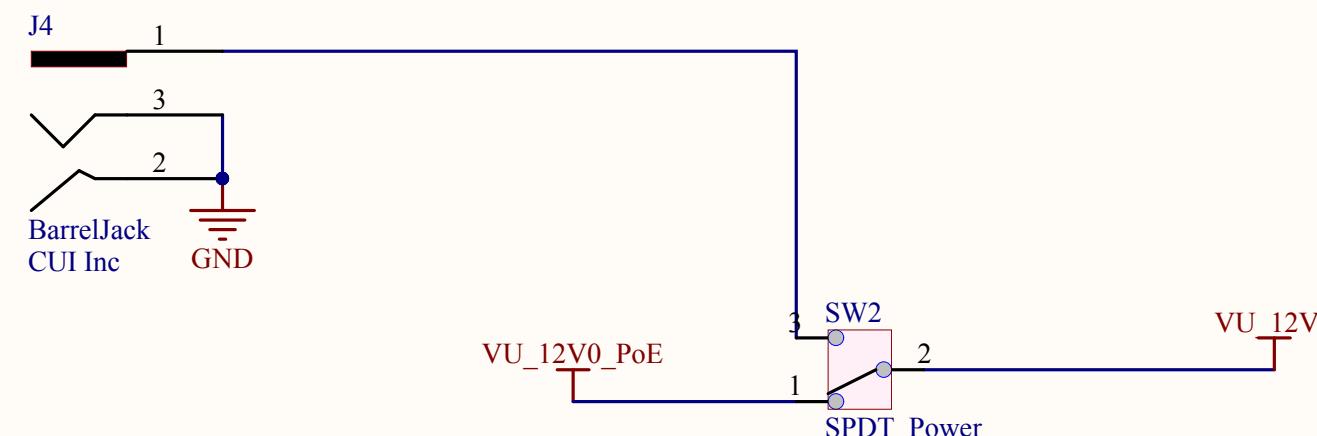
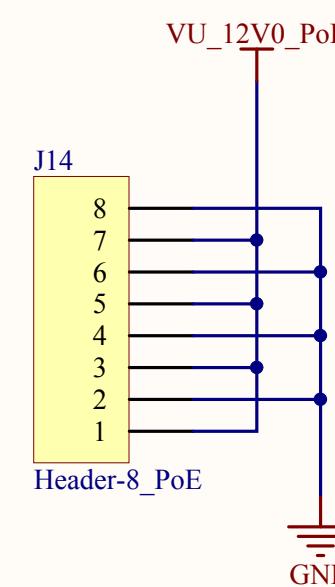
B

C

C

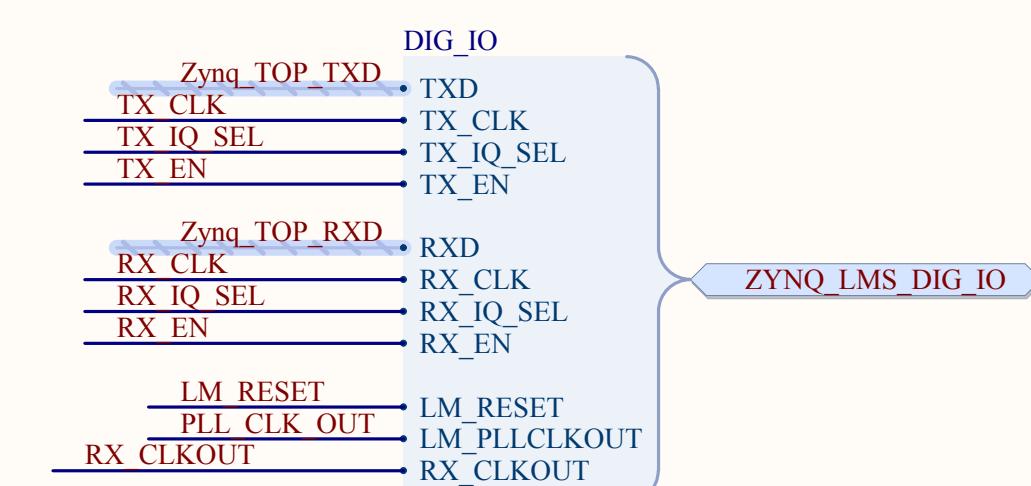
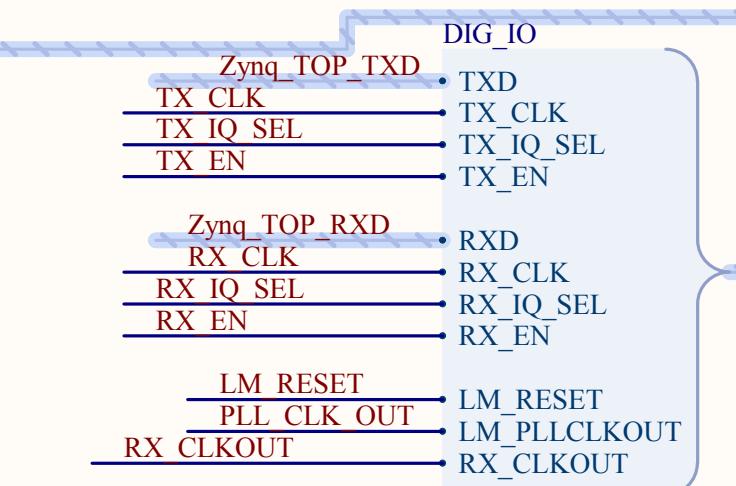
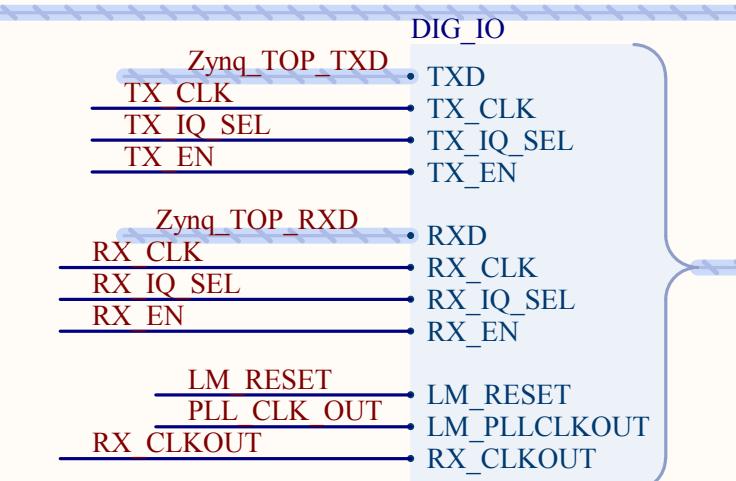
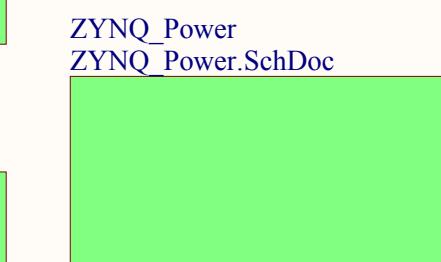
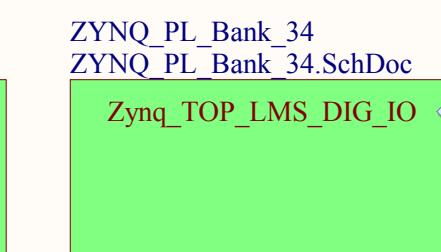
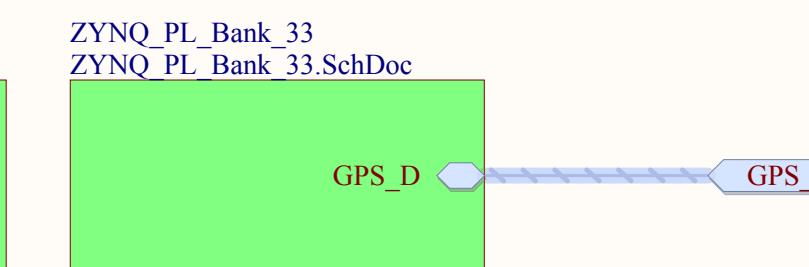
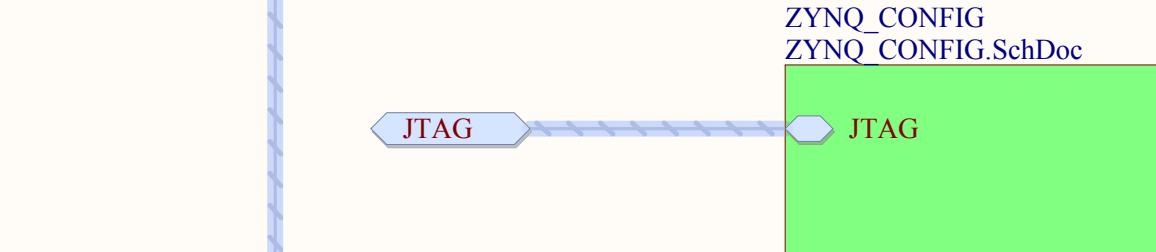
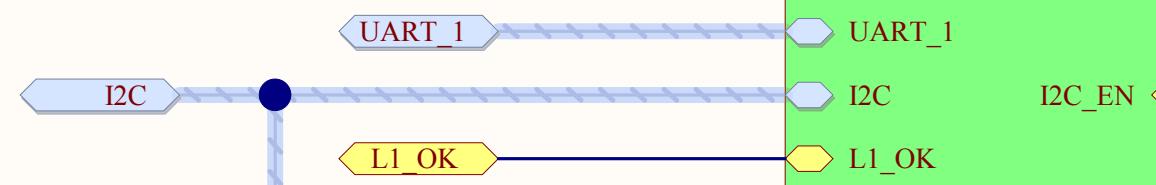
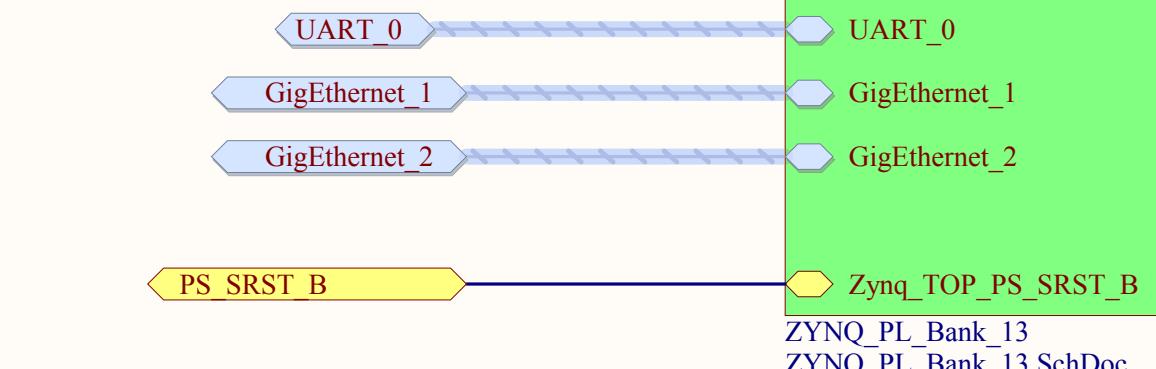
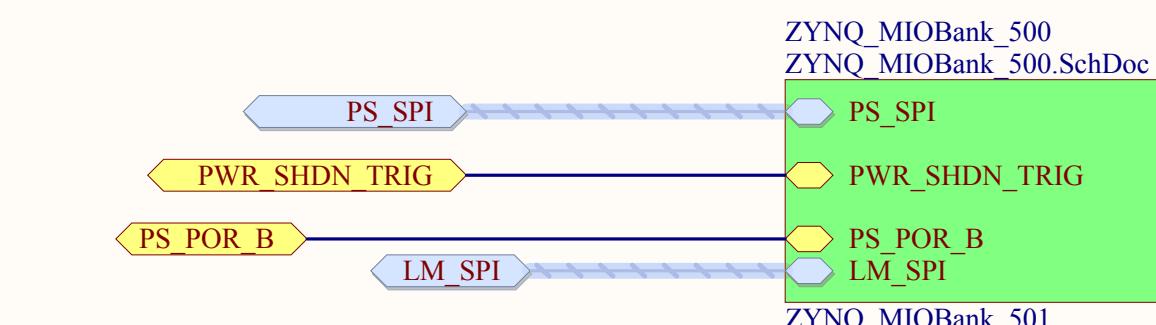
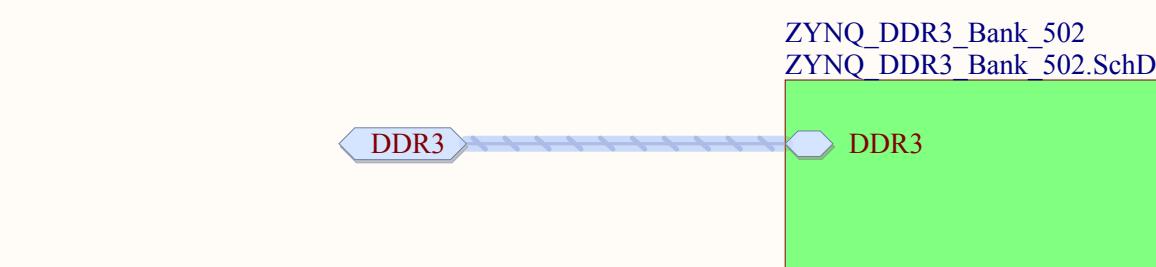
D

D



Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\PowerSwitch.SchDoc	Drawn By:

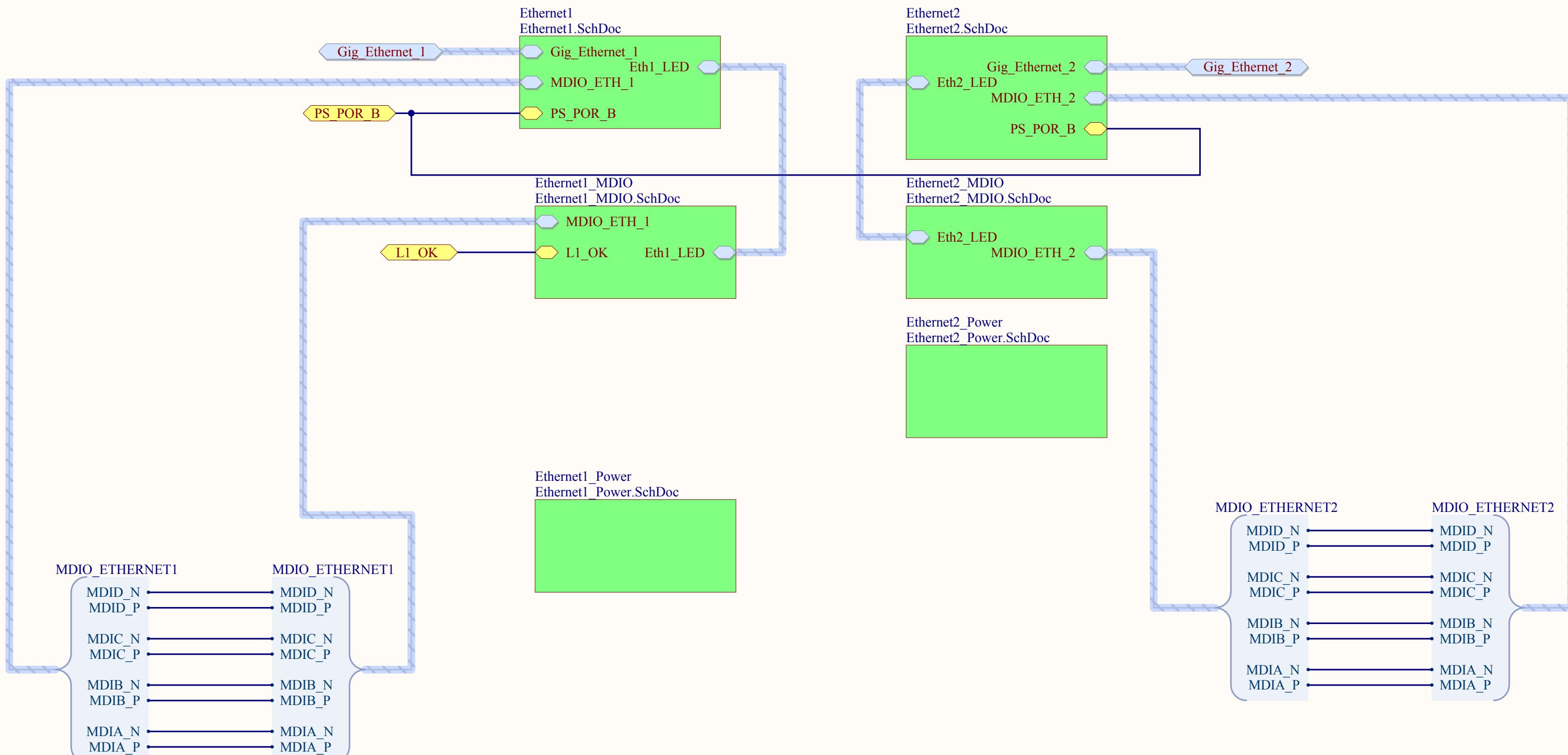
A



Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\ZYNQ_TOP_LEVEL.SchDoc	Drawn By:

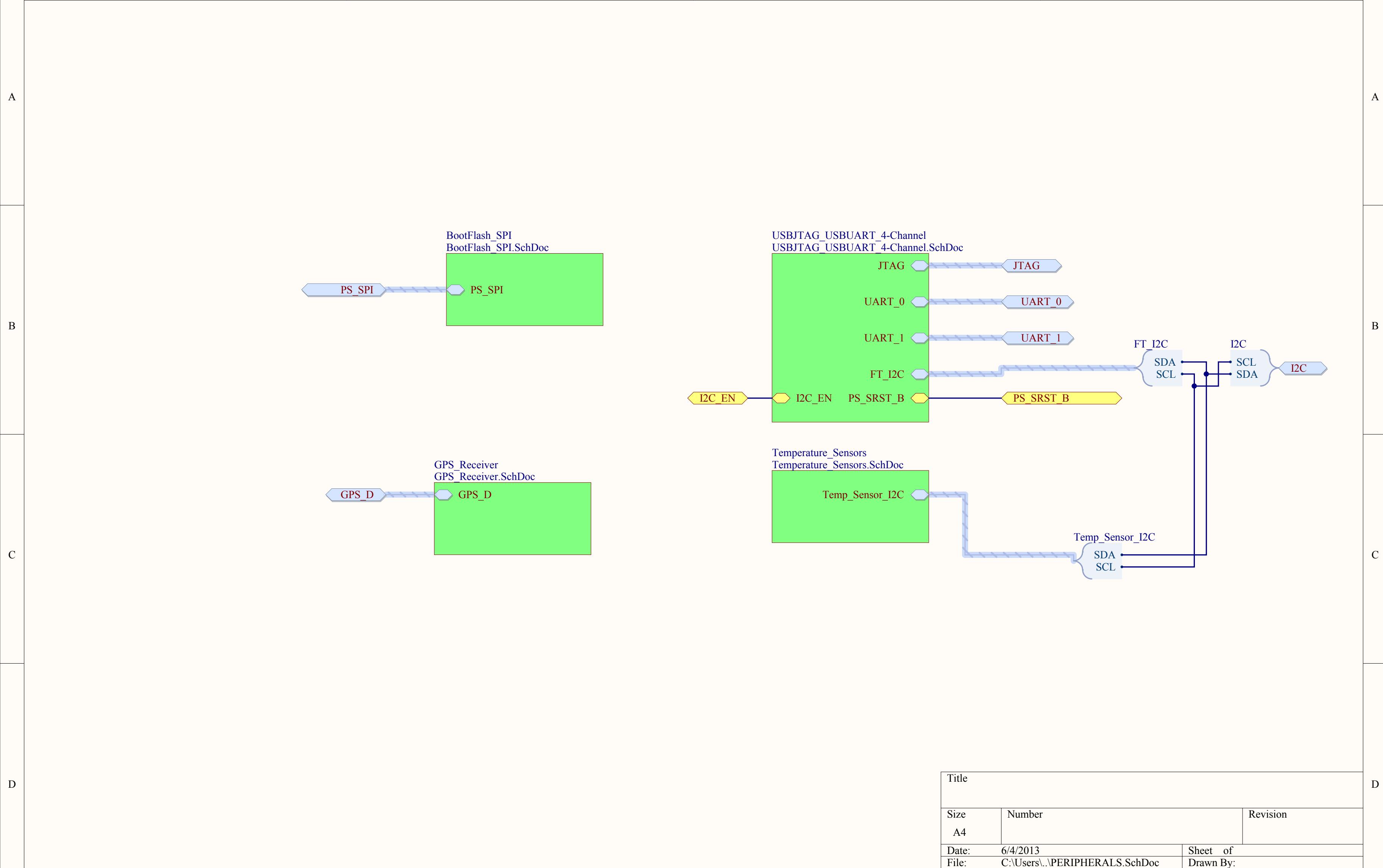
A

A



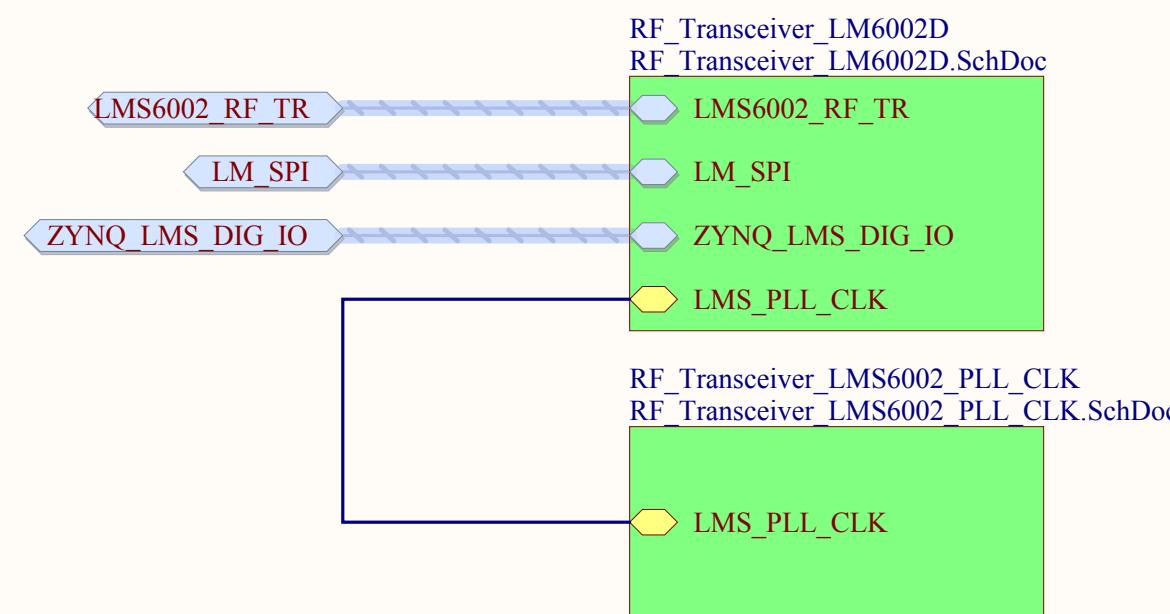
Title

Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\...\ETHERNET_TOP_LEVEL.SchDoc	Drawn By:



A

A



B

B

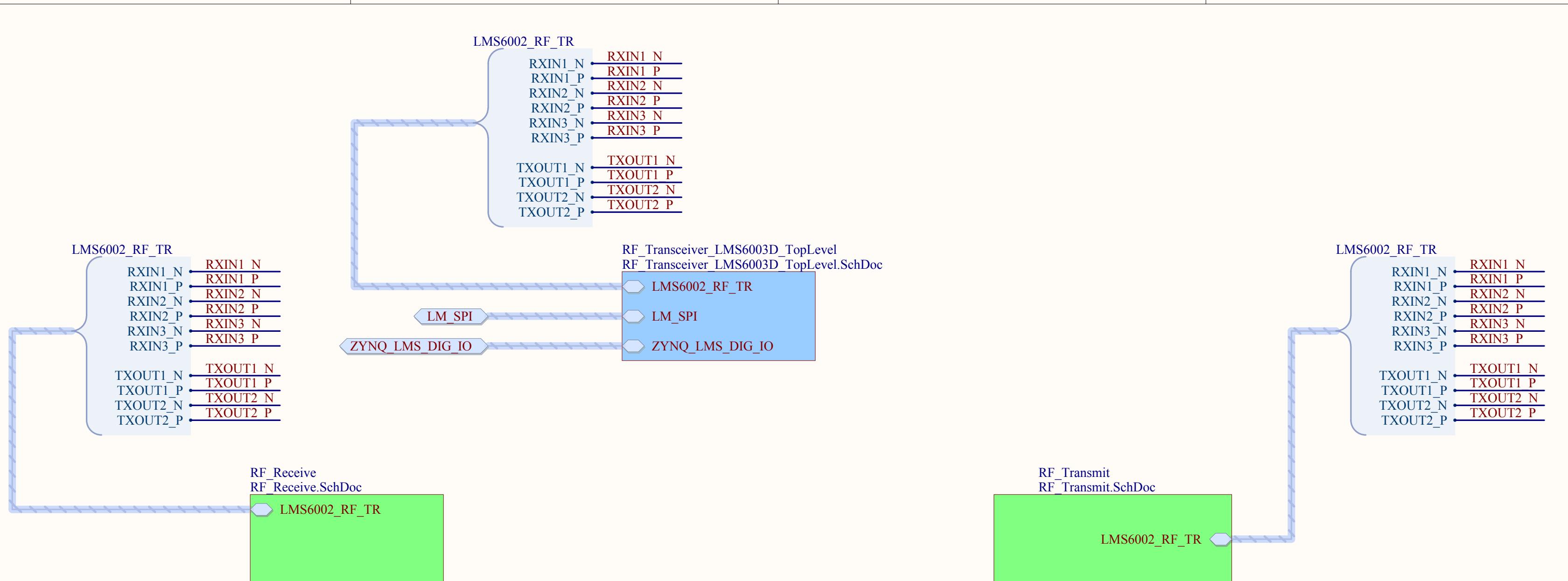
C

C

D

D

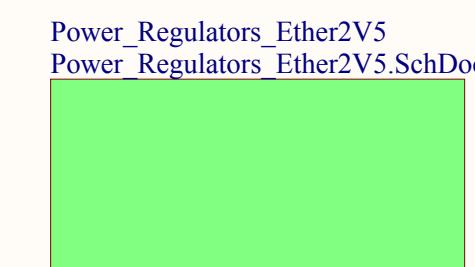
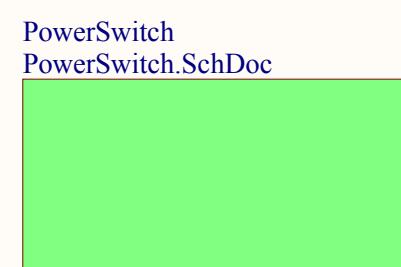
Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\RF Transceiver_LMS6003D	TopLevelSchDoc



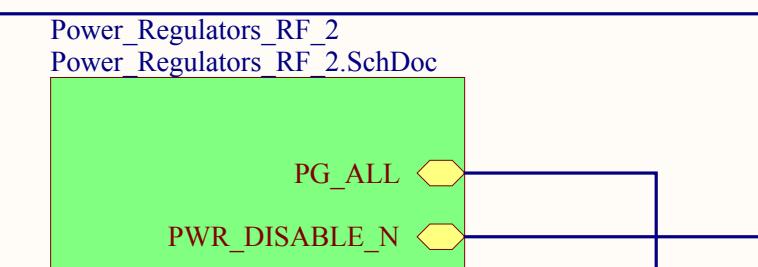
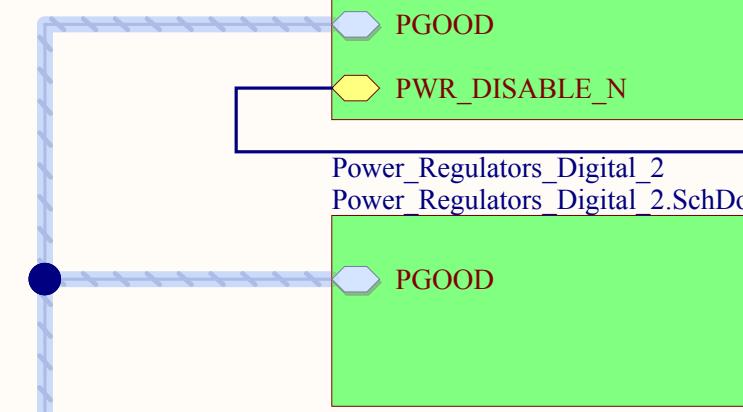
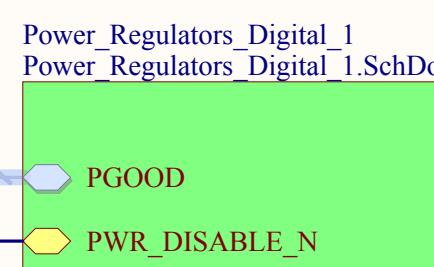
Title

Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\RF TOP LEVEL.SchDoc	Drawn By:

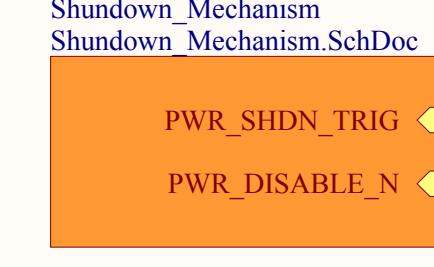
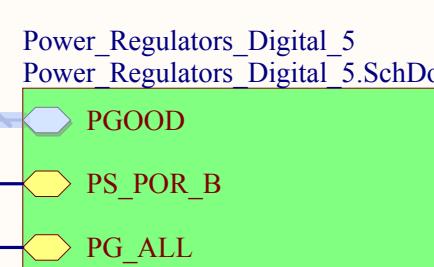
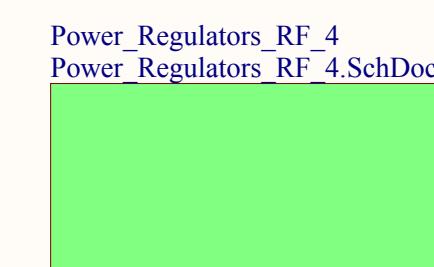
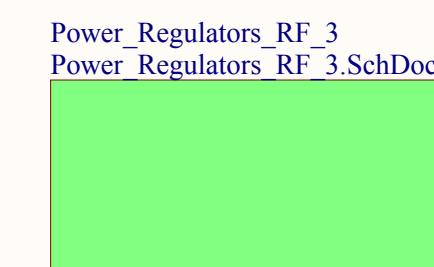
A



B



C



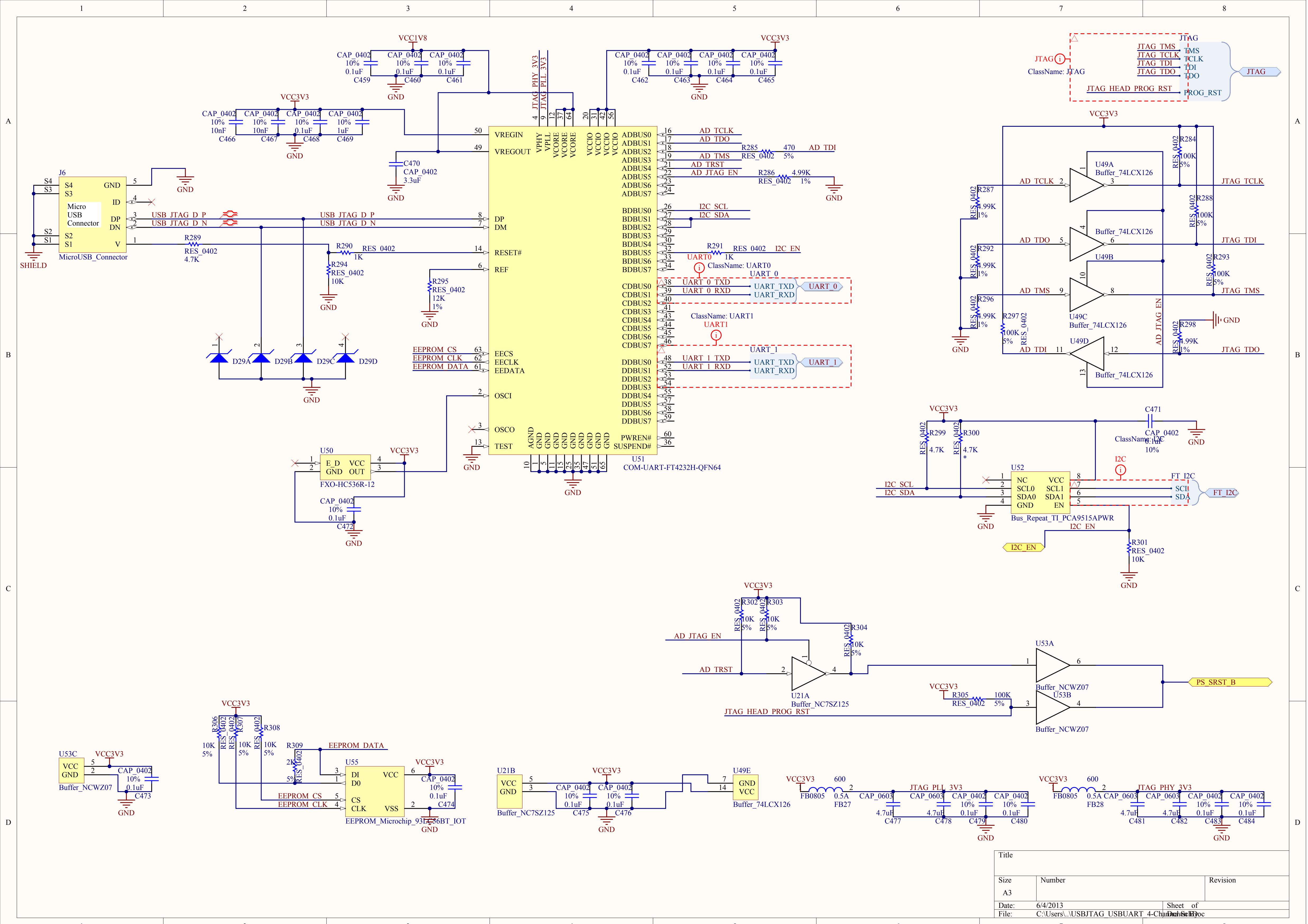
PS POR B → PS POR B → PG\_ALL

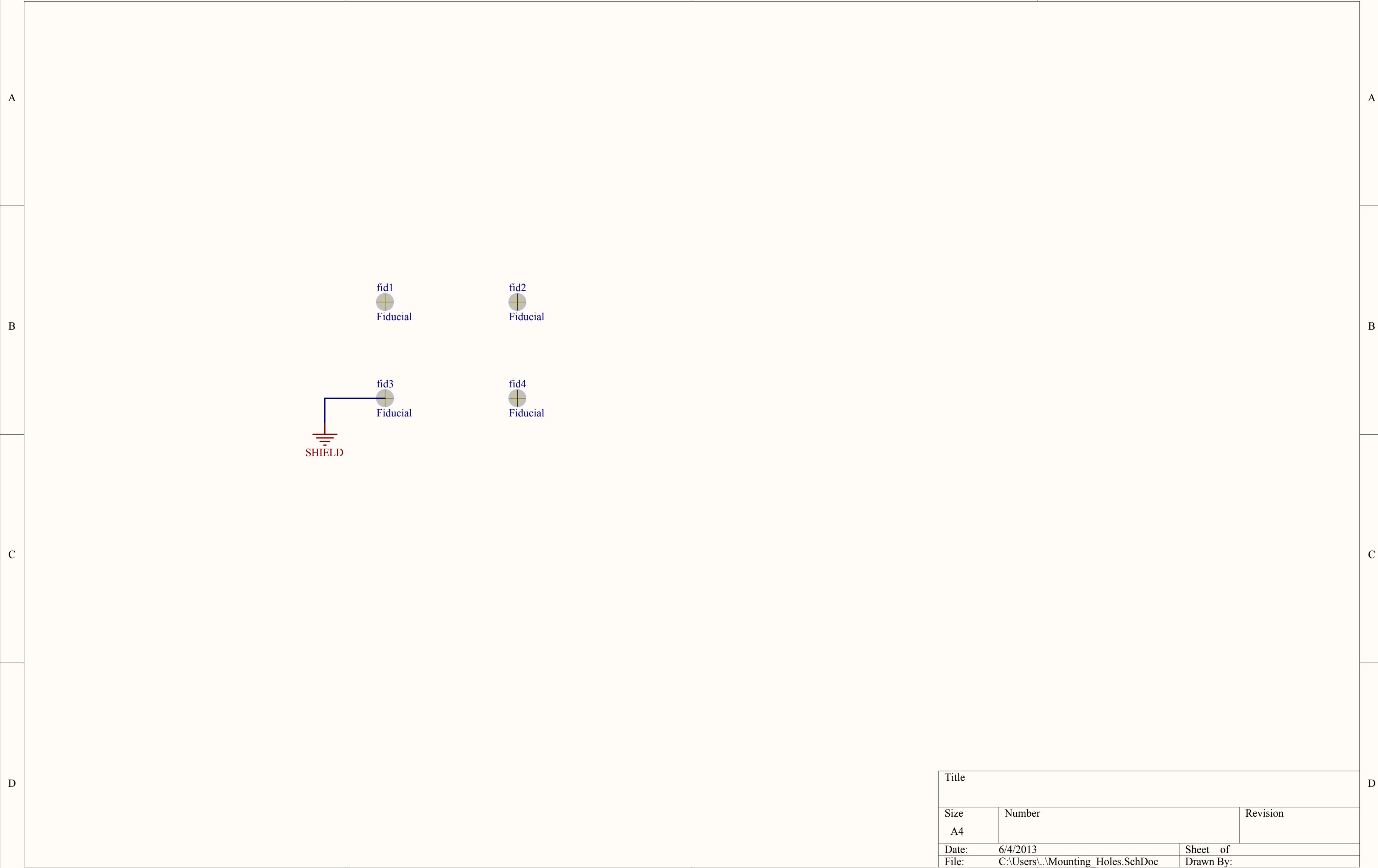
PWR SHDN TRIG

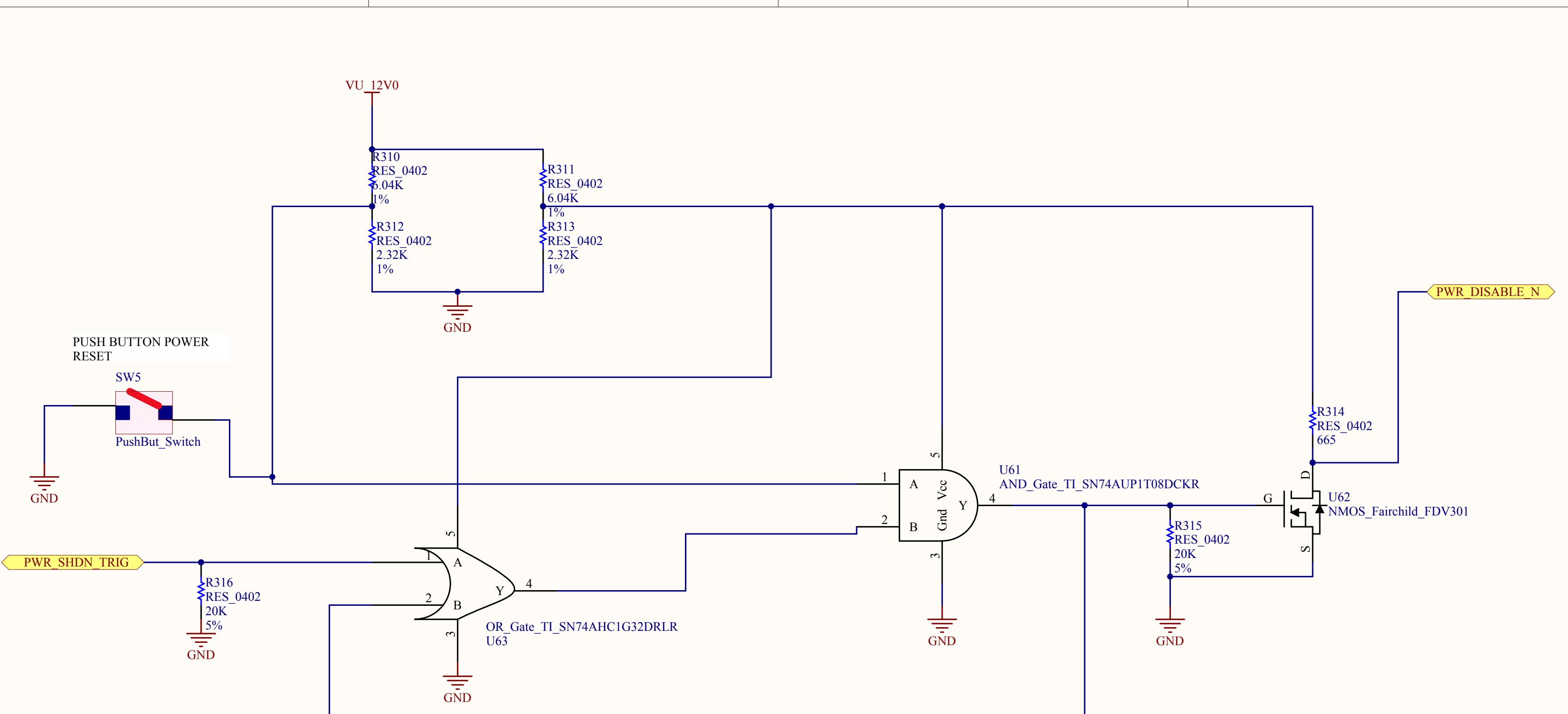
D

Title

Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\.\Power Distribution TopLevel.SchDoc	1







Title

Size

A4

Number

Revision

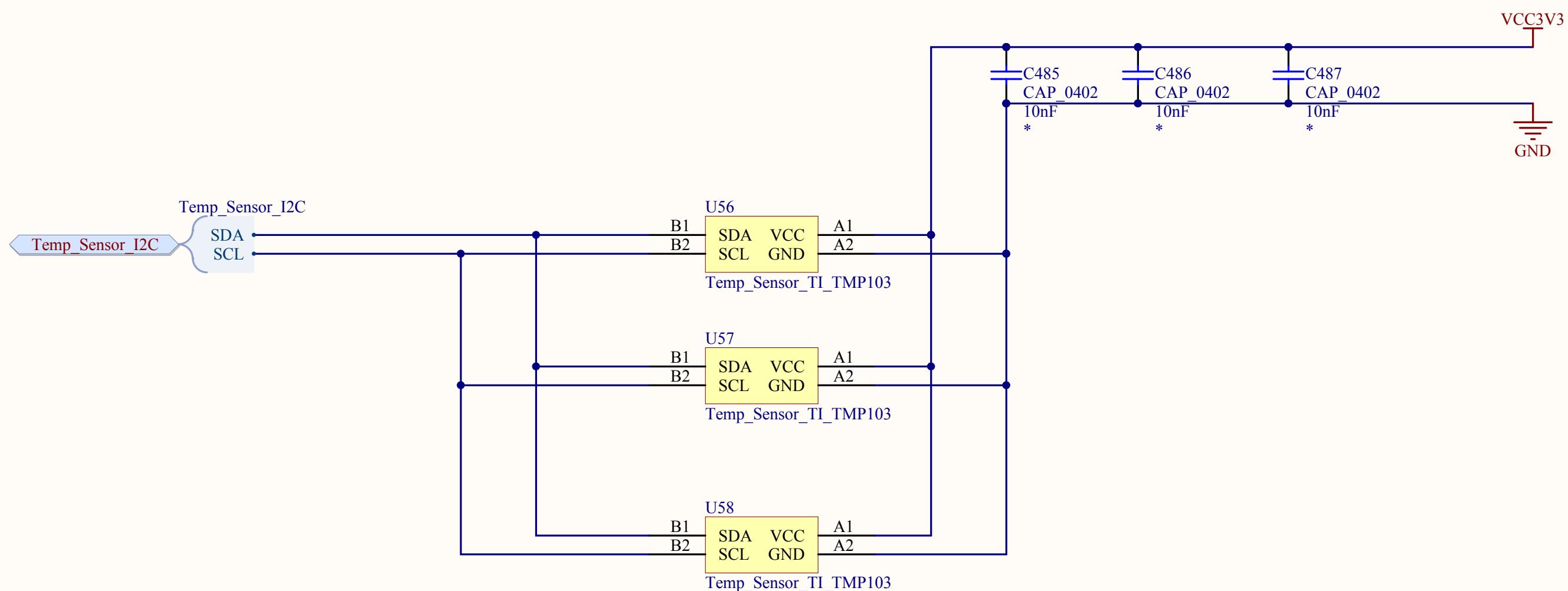
Date: 6/4/2013

Sheet of

File: C:\Users\.\Shutdown Mechanism.SchDoc Drawn By:

A

A



B

B

C

C

D

D

Title		
Size	Number	Revision
A4		
Date:	6/4/2013	Sheet of
File:	C:\Users\..\Temperature Sensors.SchDoc	Drawn By: