

ZYNQ_TOP_LEVEL
ZYNQ_TOP_LEVEL.SchDoc

PS_POR_B
PWR_SHDN_TRIG

LM_SPI
ZYNQ_LMS_DIG_IO

GigEthernet_1
GigEthernet_2

L1_OK

PS_SPI

GPS_D

UART_0

UART_1

JTAG

I2C

PS_SRST_B

I2C_EN

DDR3

Power_Distribution_TopLevel
Power_Distribution_TopLevel.SchDoc

PS_POR_B
PWR_SHDN_TRIG

RF_TOP_LEVEL
RF_TOP_LEVEL.SchDoc

LM_SPI
ZYNQ_LMS_DIG_IO

ETHERNET_TOP_LEVEL
ETHERNET_TOP_LEVEL.SchDoc

Gig_Ethernet_1
Gig_Ethernet_2

PS_POR_B
L1_OK

PERIPHERALS
PERIPHERALS.SchDoc

PS_SPI

GPS_D

UART_0

UART_1

JTAG

I2C

PS_SRST_B

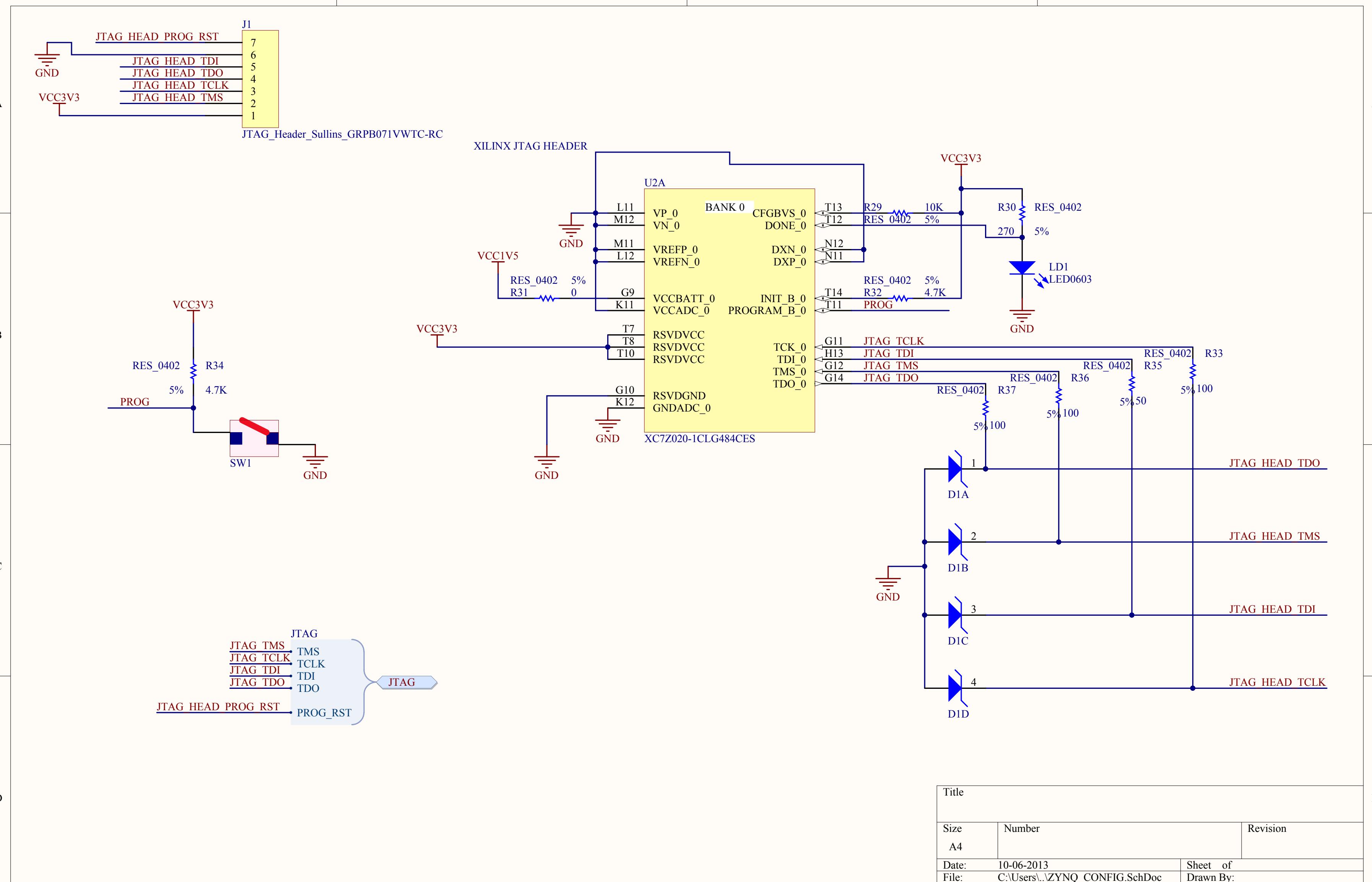
I2C_EN

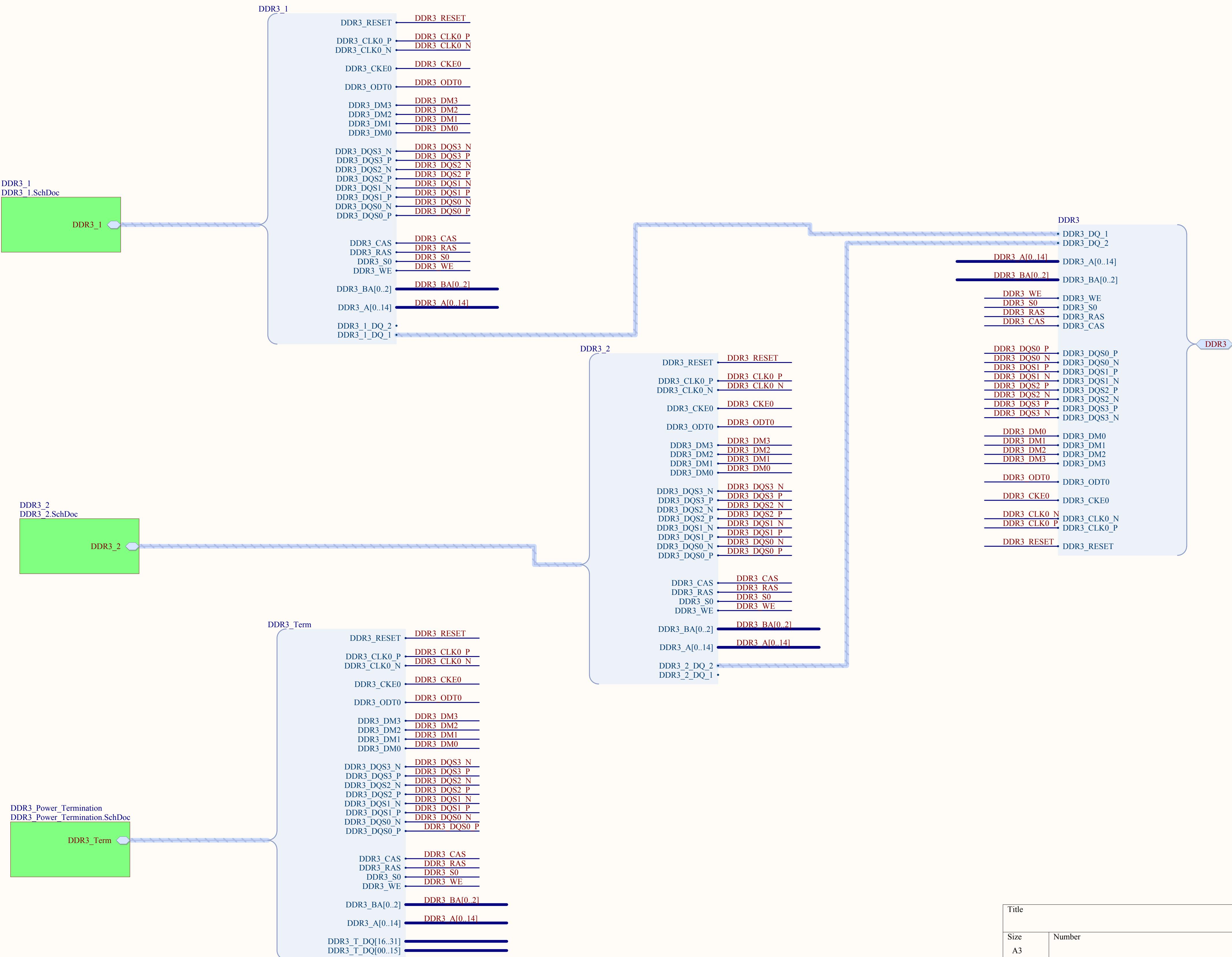
DDR3_TOP_LEVEL
DDR3_TOP_LEVEL.SchDoc

DDR3

Mounting_Holes
Mounting_Holes.SchDoc

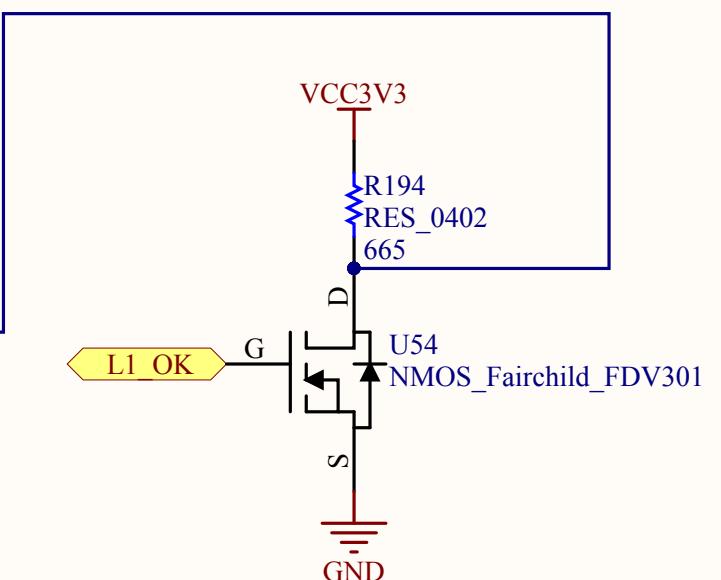
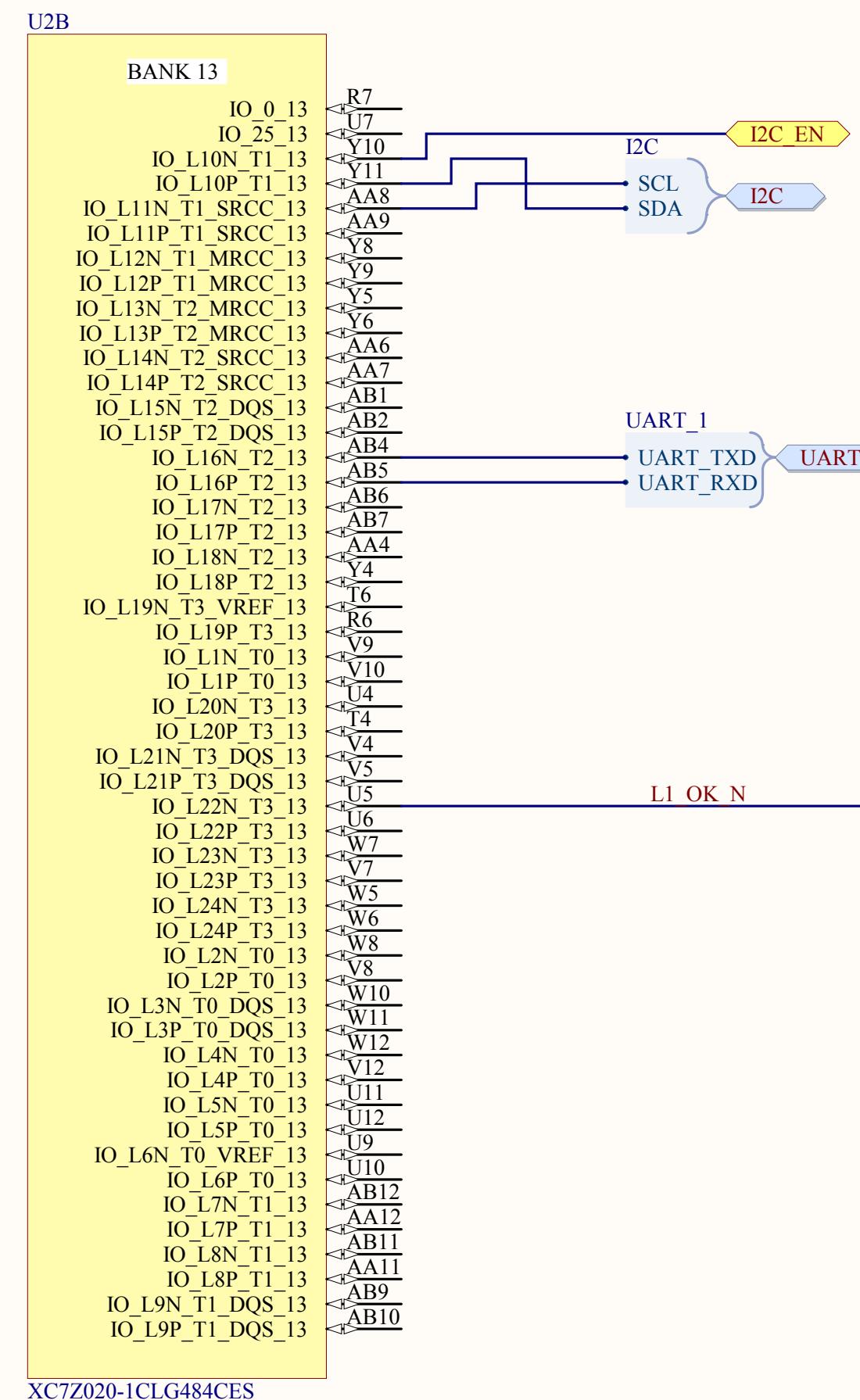
Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\COMRAD_TOP_LEVEL.SchDoc	Drawn By:





A

A



B

B

C

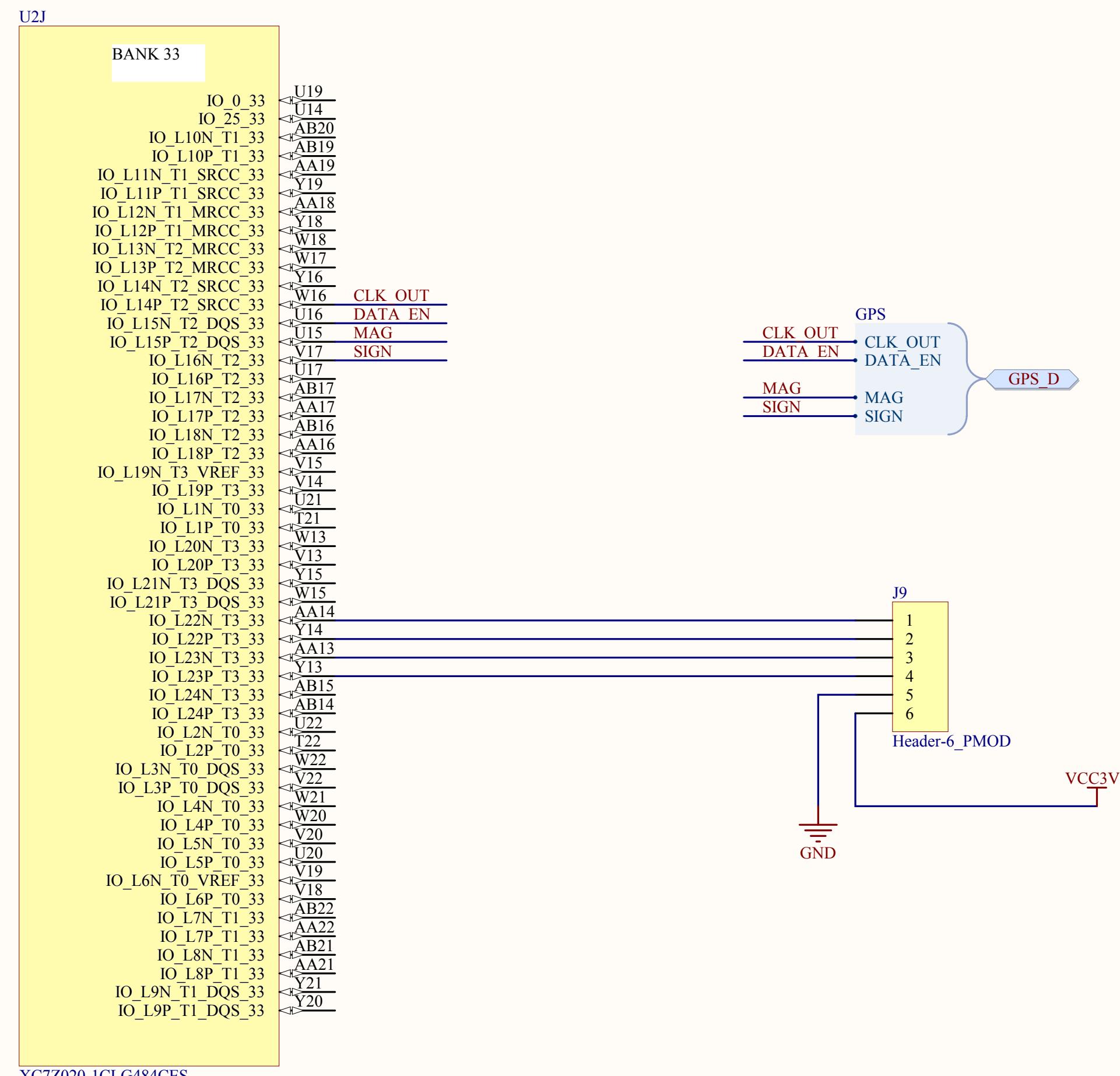
C

D

D

Title		
Size	Number	Revision
A4		
Date: 10-06-2013	Sheet of	
File: C:\Users\..\\ZYNQ_PL_Bank_13.SchDoc	Drawn By:	

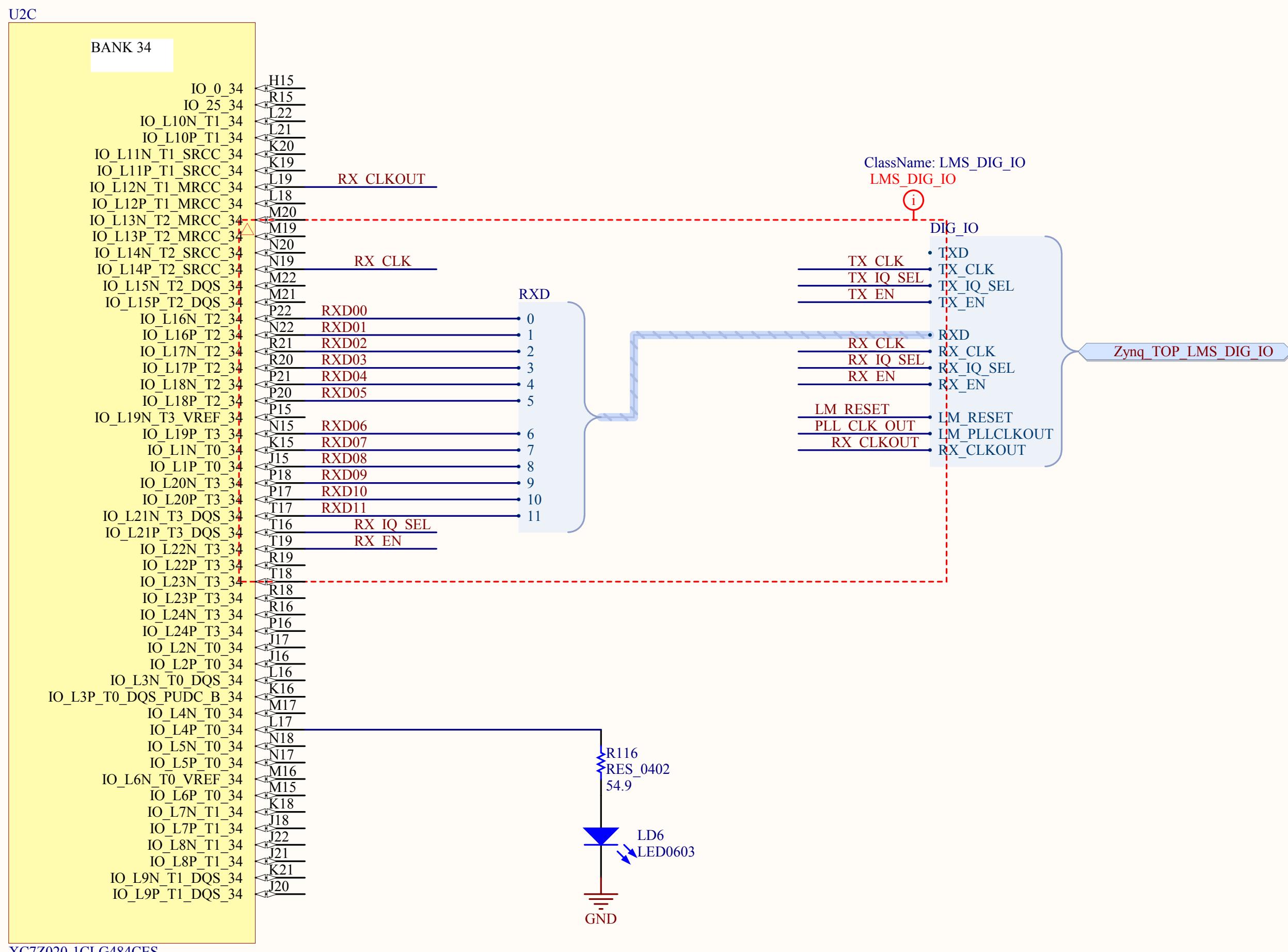
A



Title

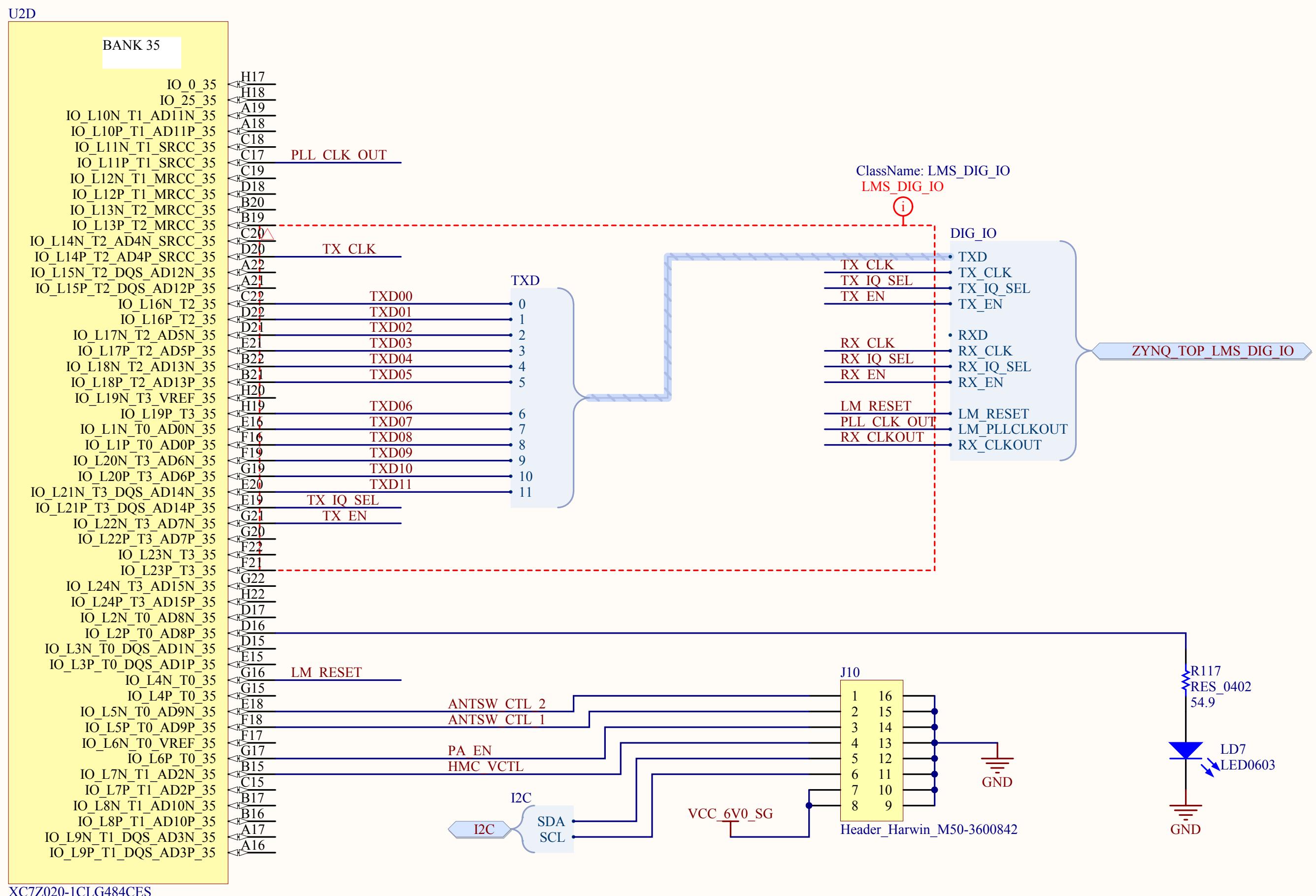
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\ZYNQ_PL_Bank_33.SchDoc	Drawn By:

A

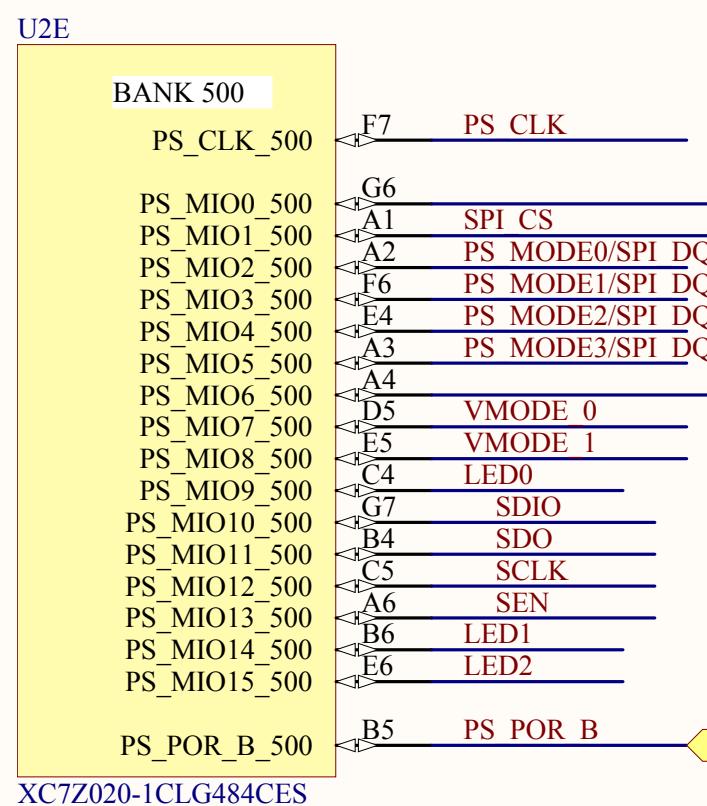


Title

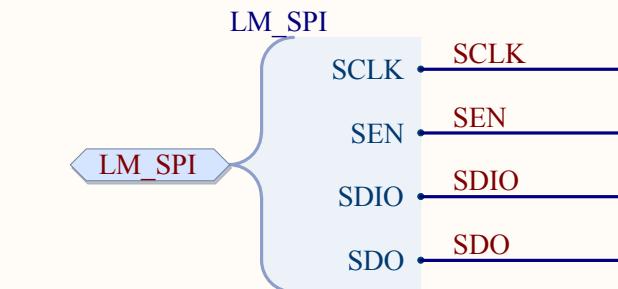
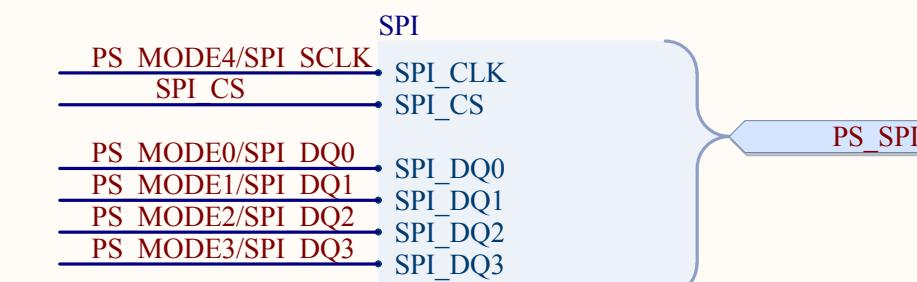
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\ZYNQ_PL_Bank_34.SchDoc	Drawn By:



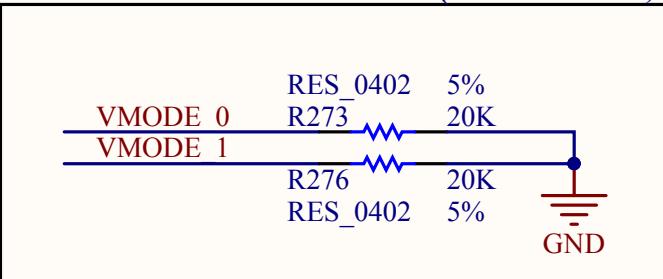
Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\ZYNQ_PL_Bank_35.SchDoc	Drawn By:



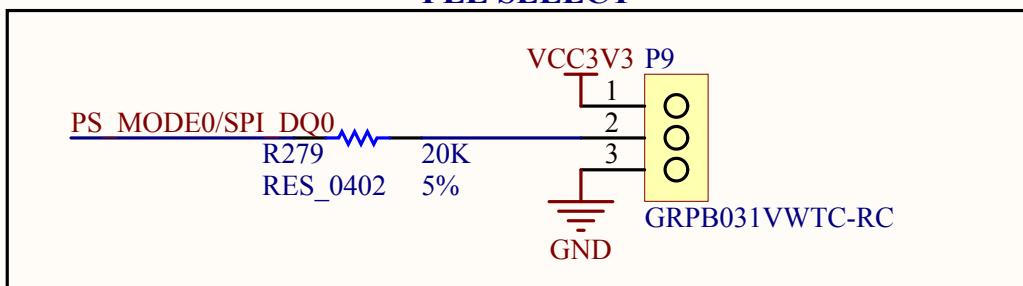
'PWR_SHDN_TRIG' SHOULD BE ONLY A TRIGGER:
TO BE MADE HIGH FOR LIMITED CLOCK CYCLES &
THEN, TURNED LOW



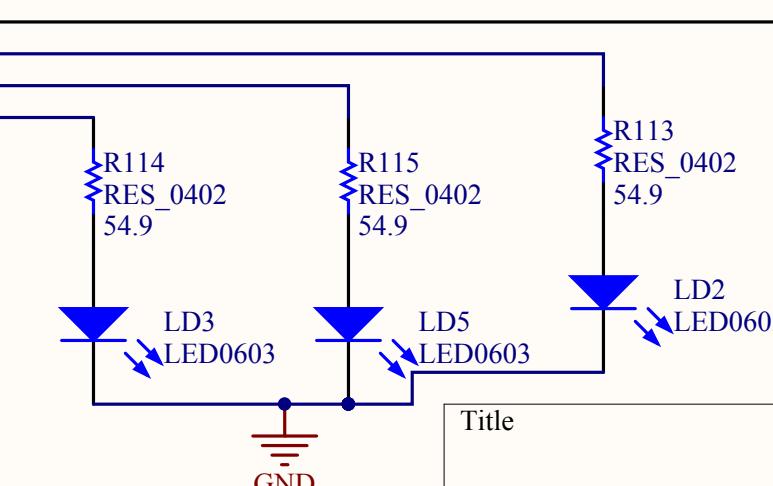
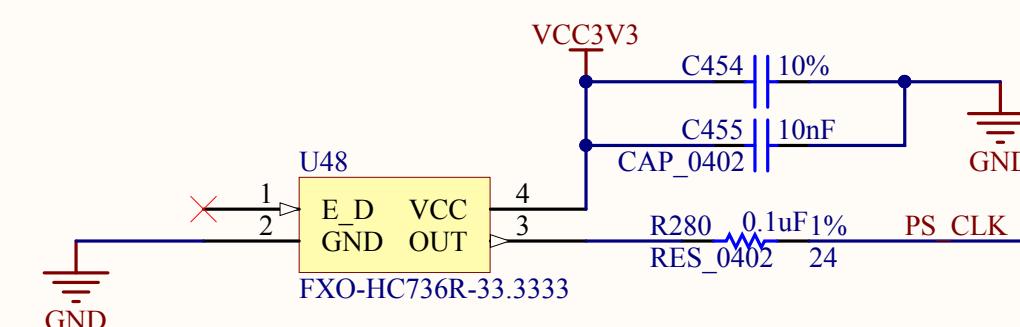
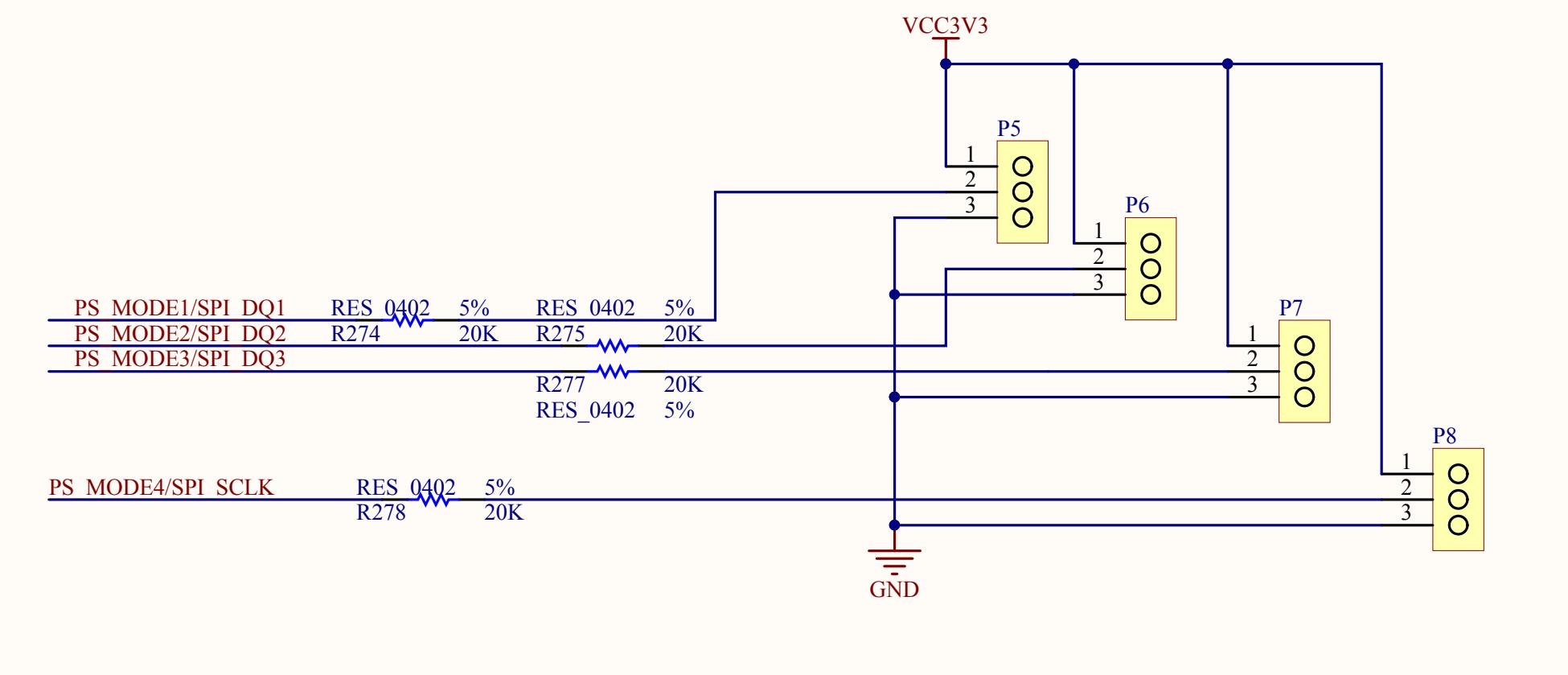
MIO VOLTAGE MODES SELECT(MIO500-3V3;MIO501-3V3)



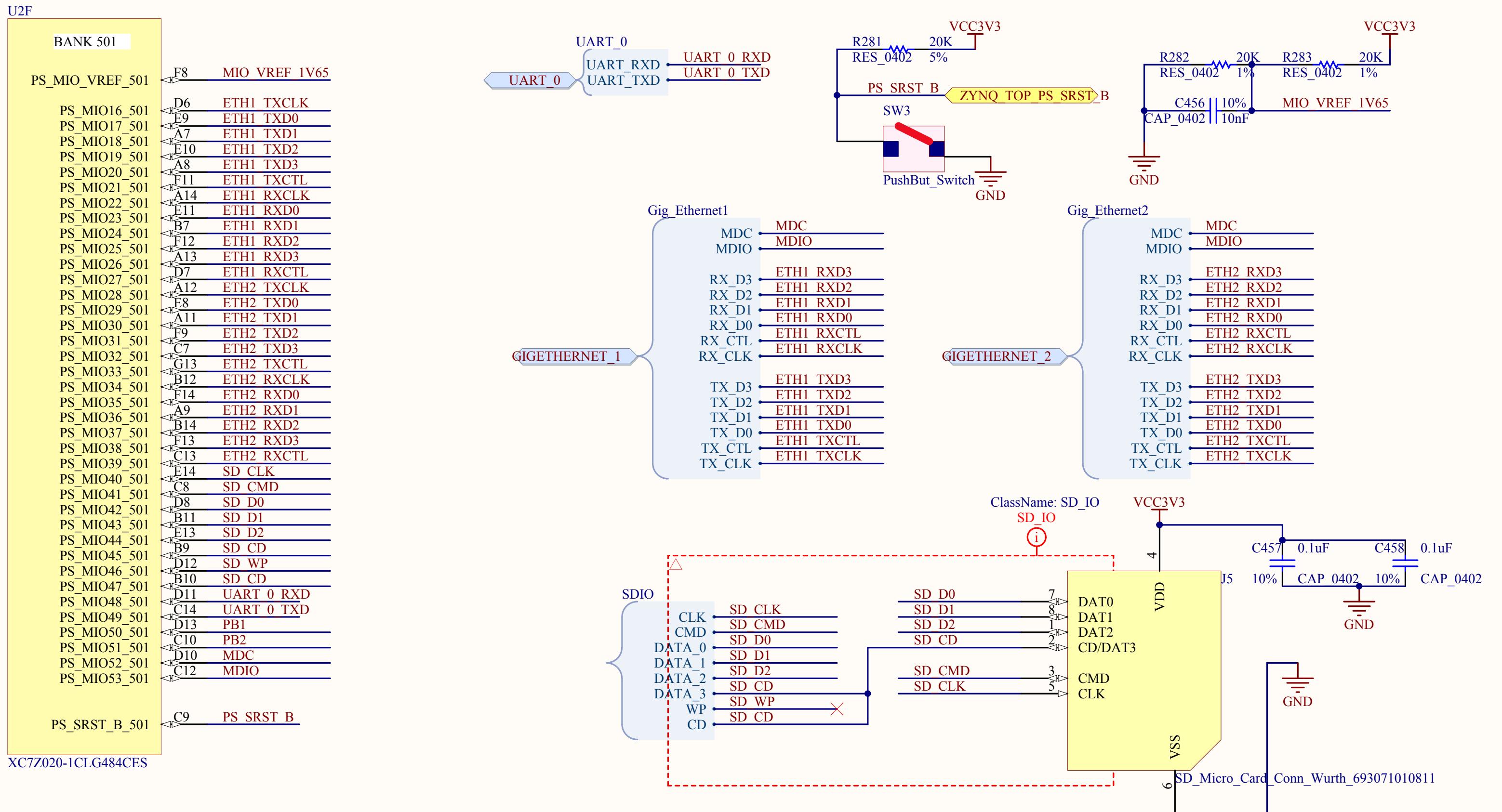
PLL SELECT



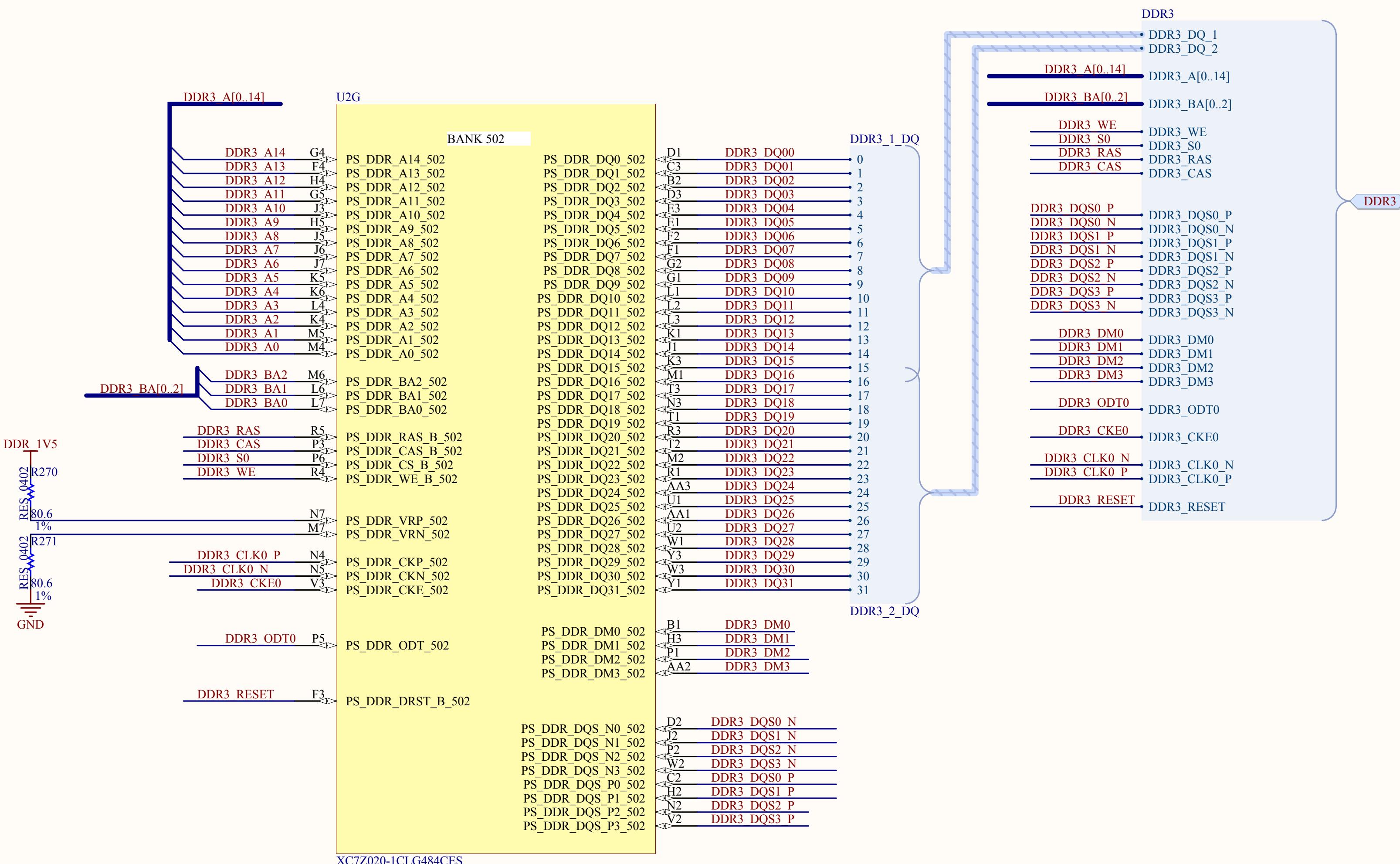
BOOT ROM SELECT



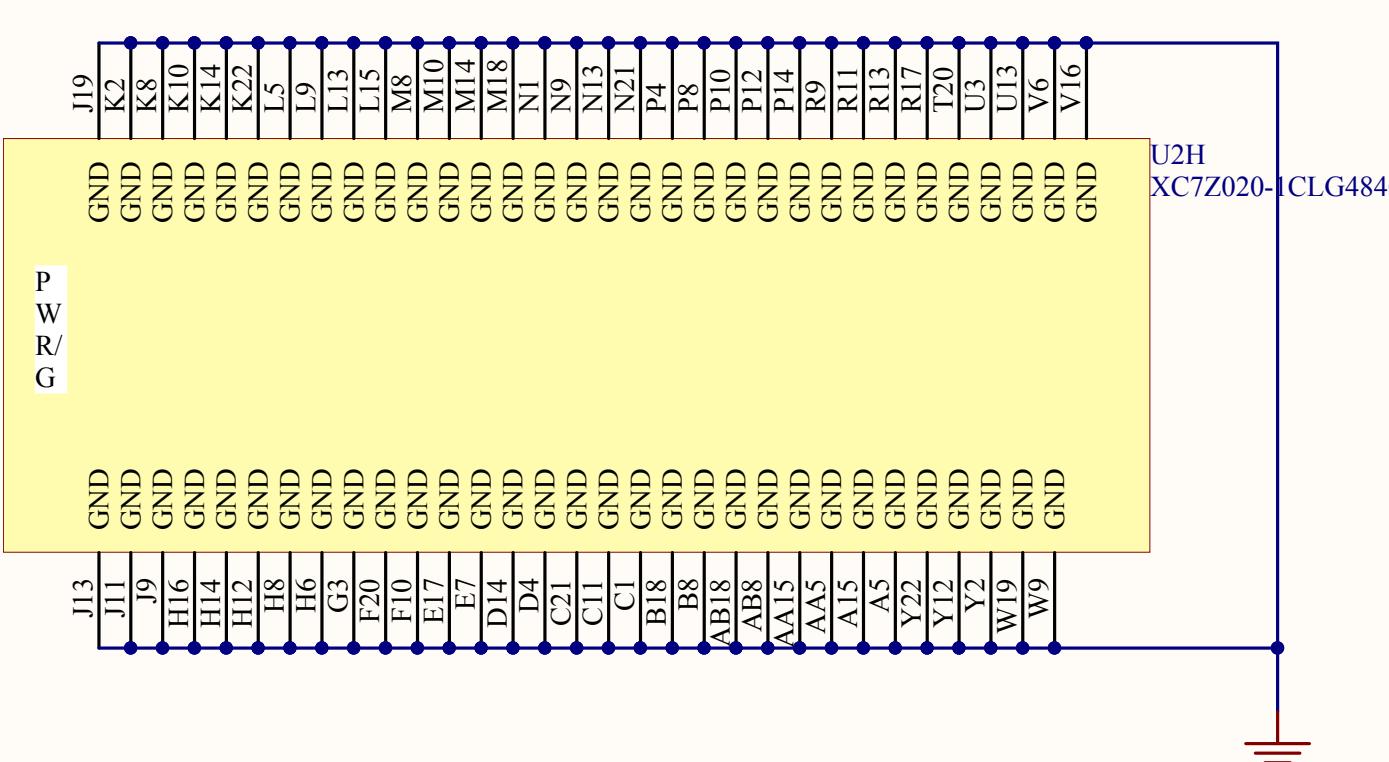
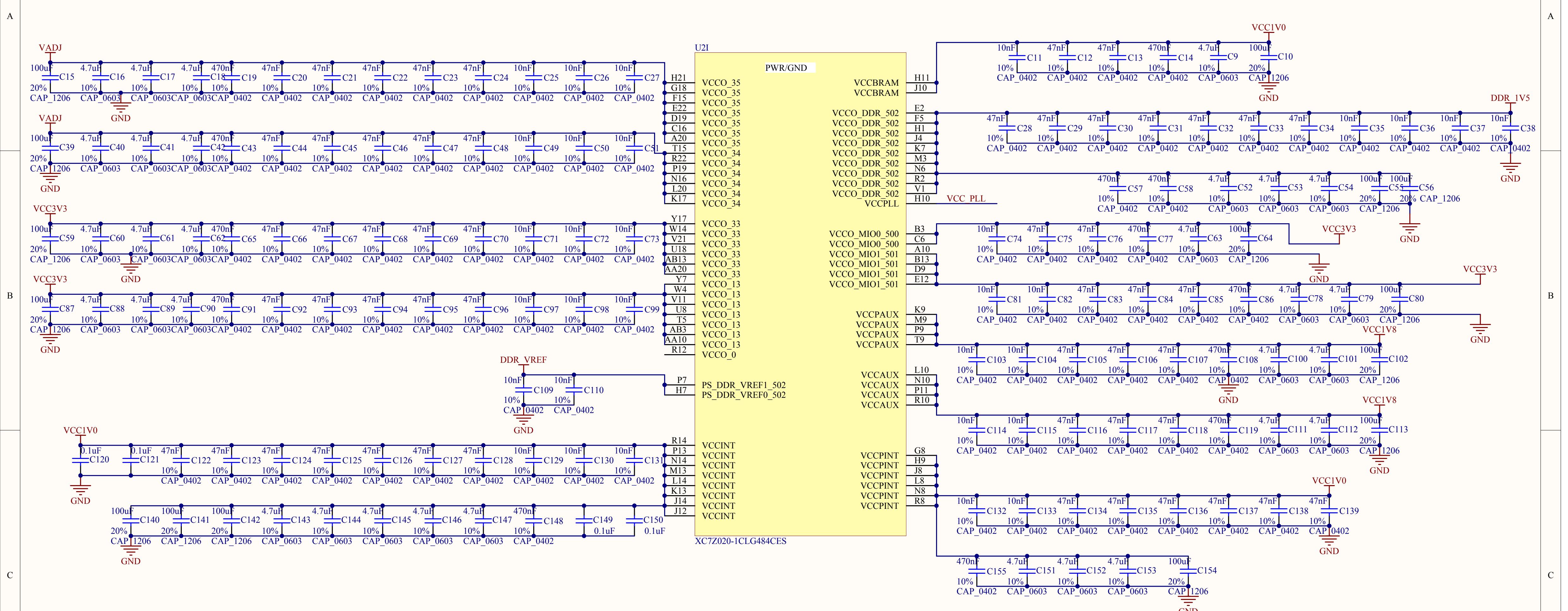
Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\ZYNN_MIOBank_500.SchDoc	Drawn By:



Title		
Size A4	Number	Revision
Date:	10-06-2013	Sheet of
File:	C:\Users\..\ZYNQ	MIOBank 501.SchDocDrawn By:



Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\ZYNNQ_DDR3_Bank_502.Sch	Drawn By:



Title		
Size	Number	Revision
A3		
Date:	10-06-2013	Sheet of
File:	C:\Users...\ZYNNQ_Power.SchDoc	Drawn By:

A

A

B

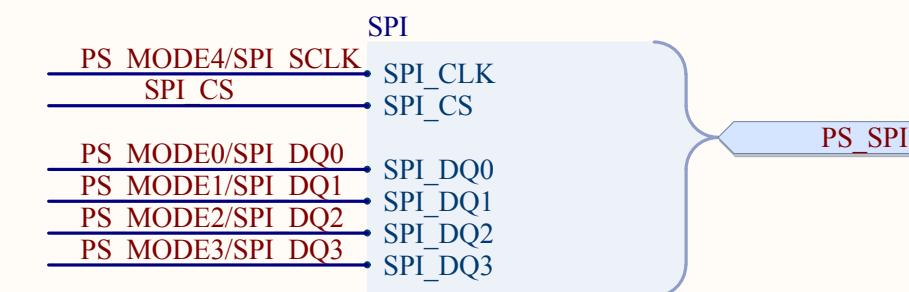
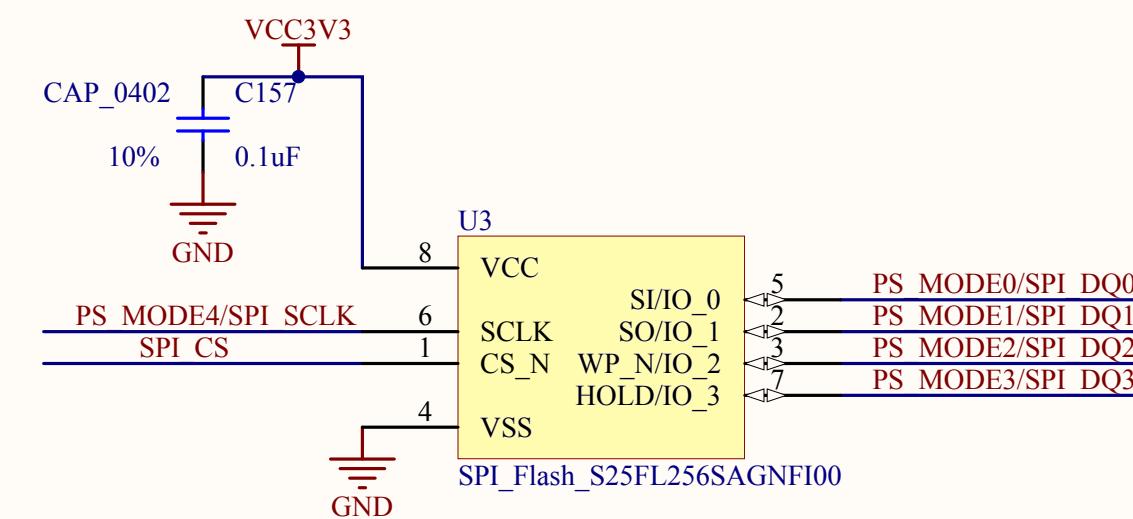
B

C

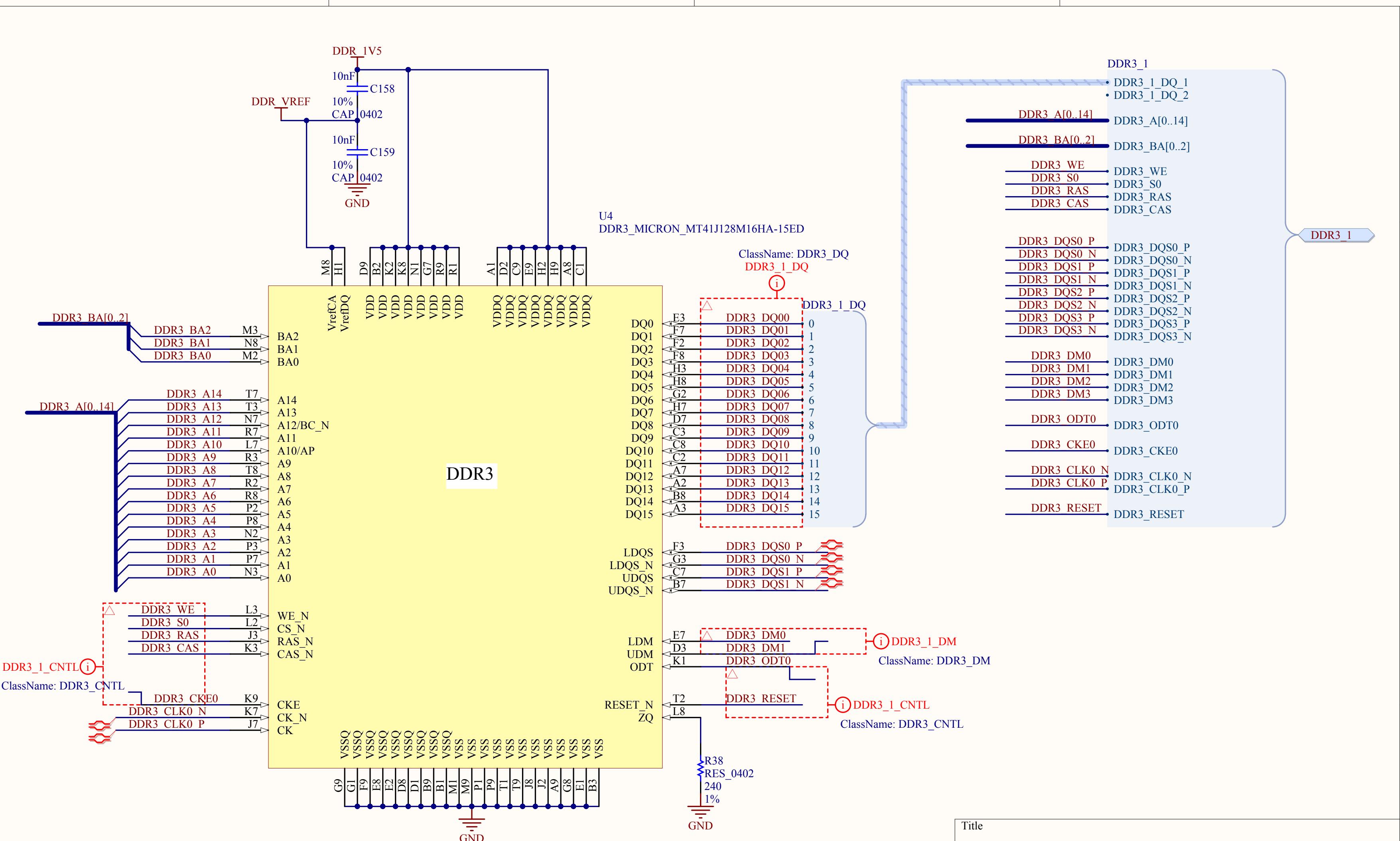
C

D

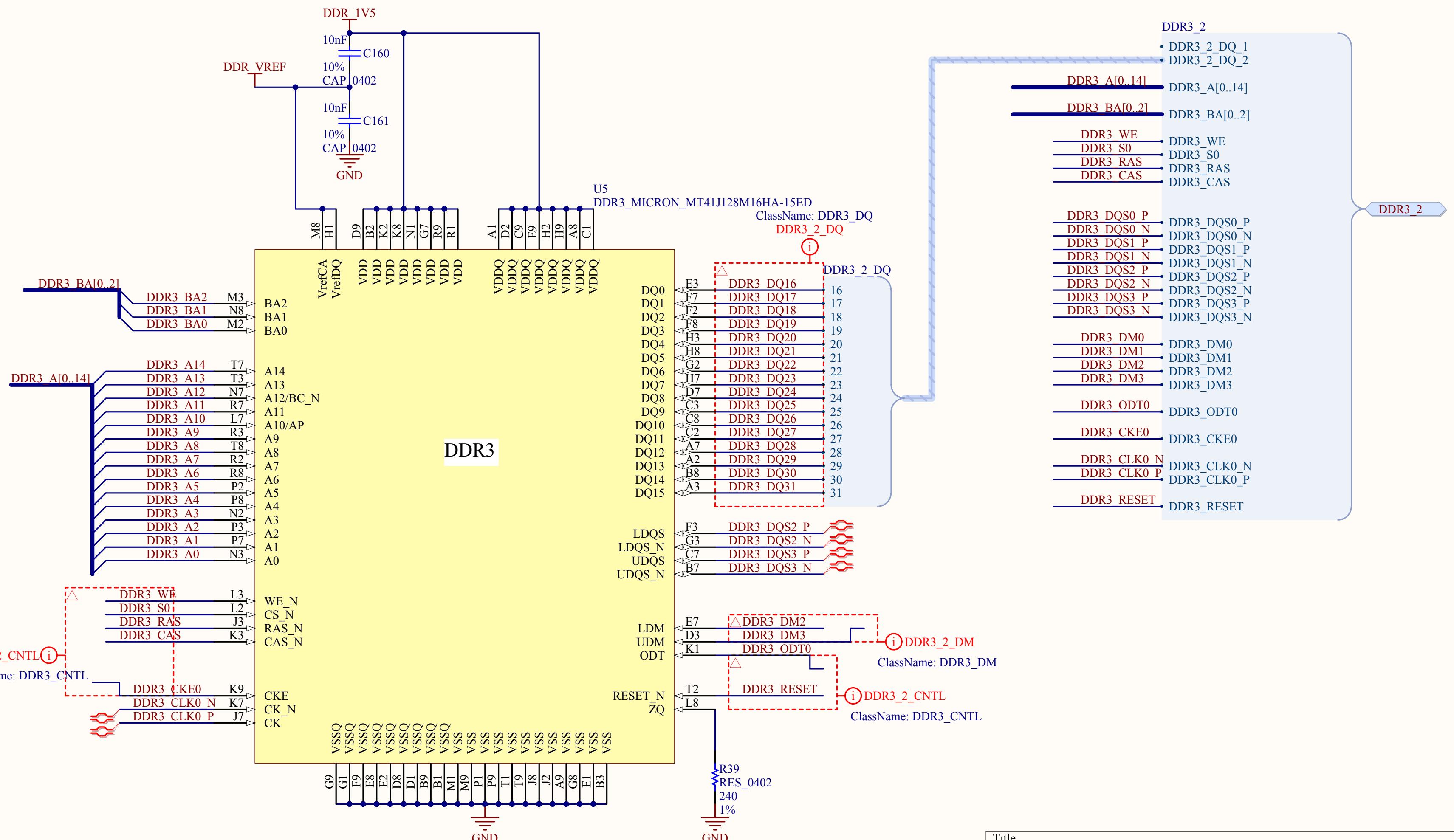
D



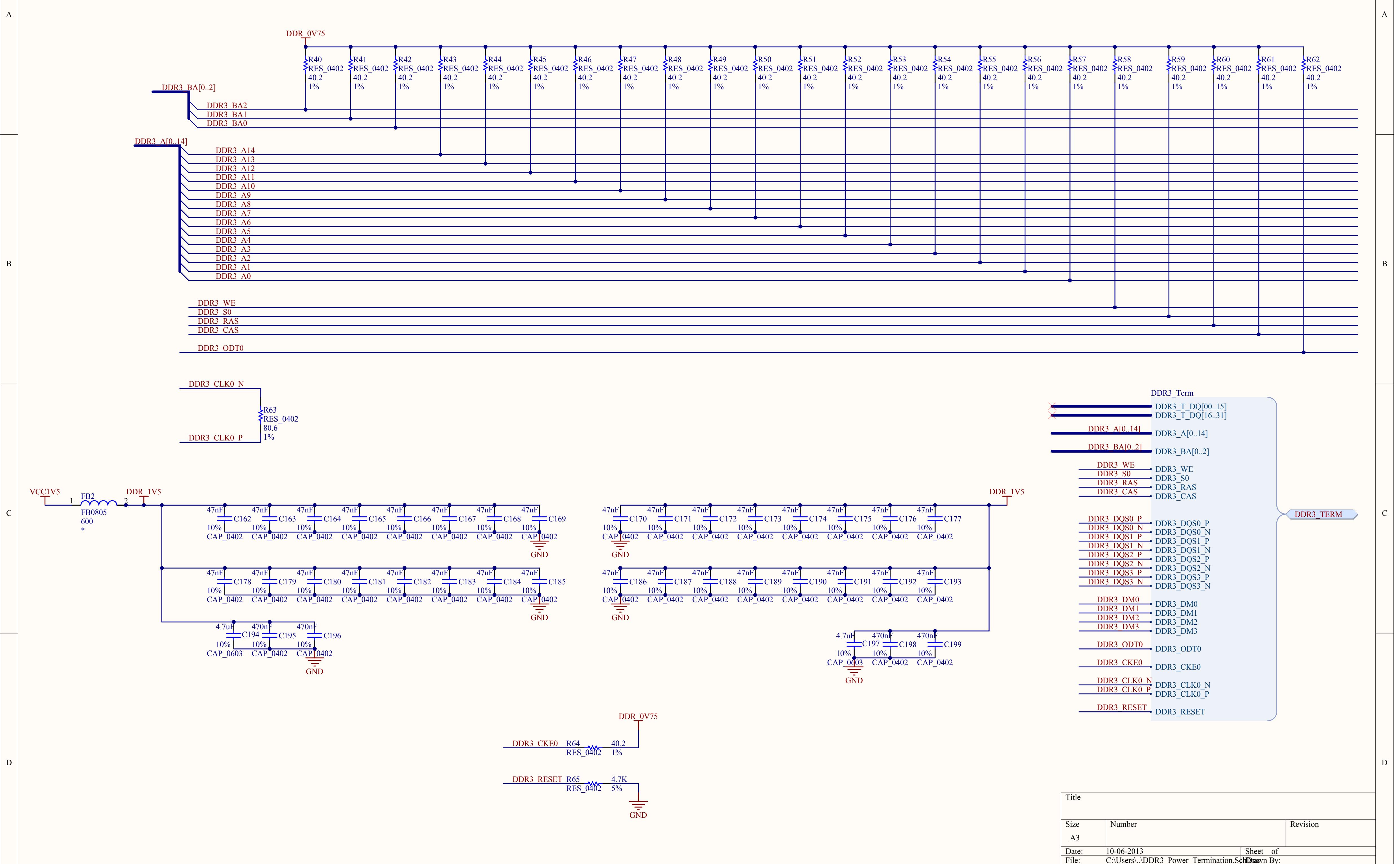
Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\BootFlash_SPI.SchDoc	Drawn By:

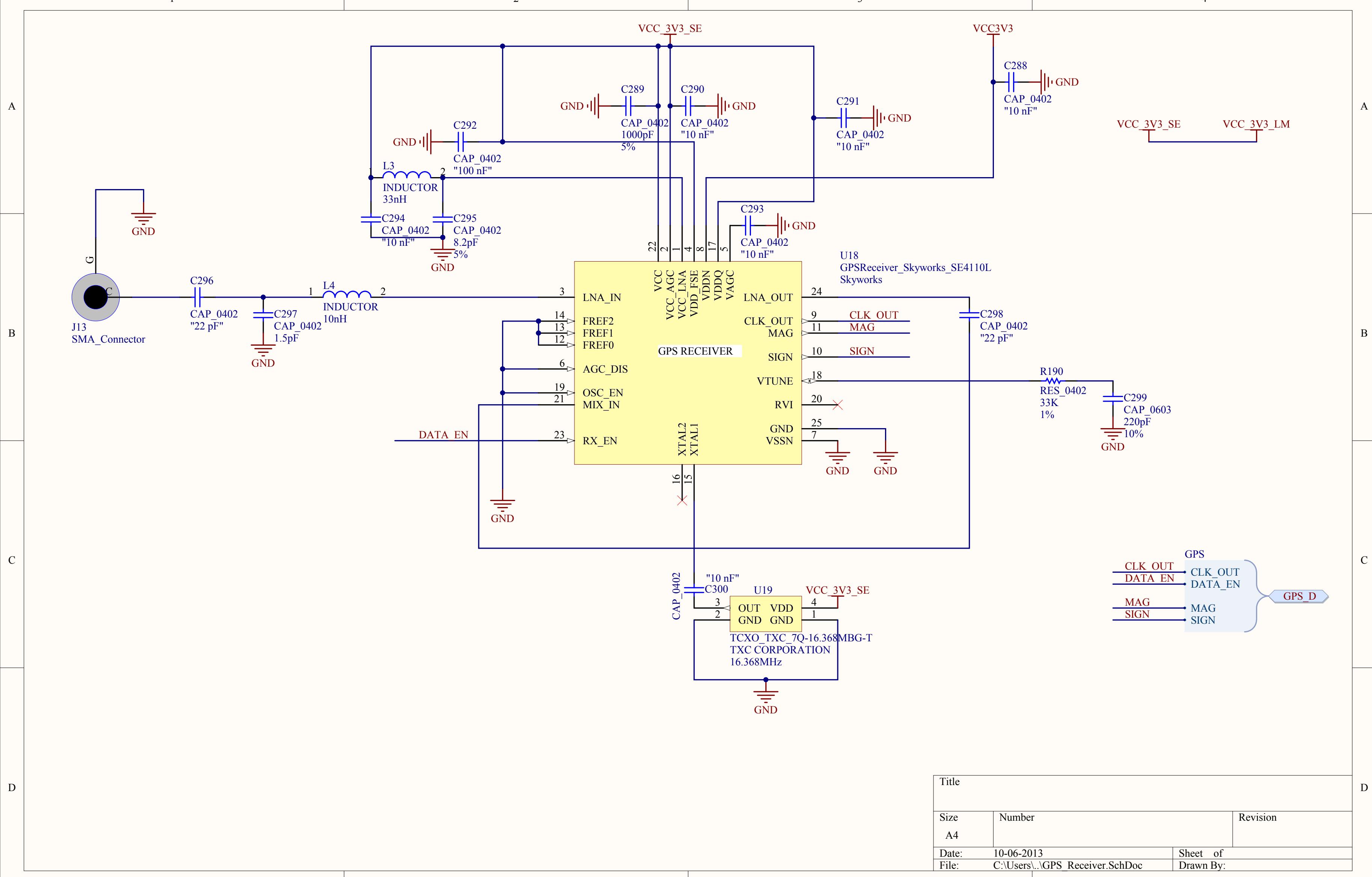


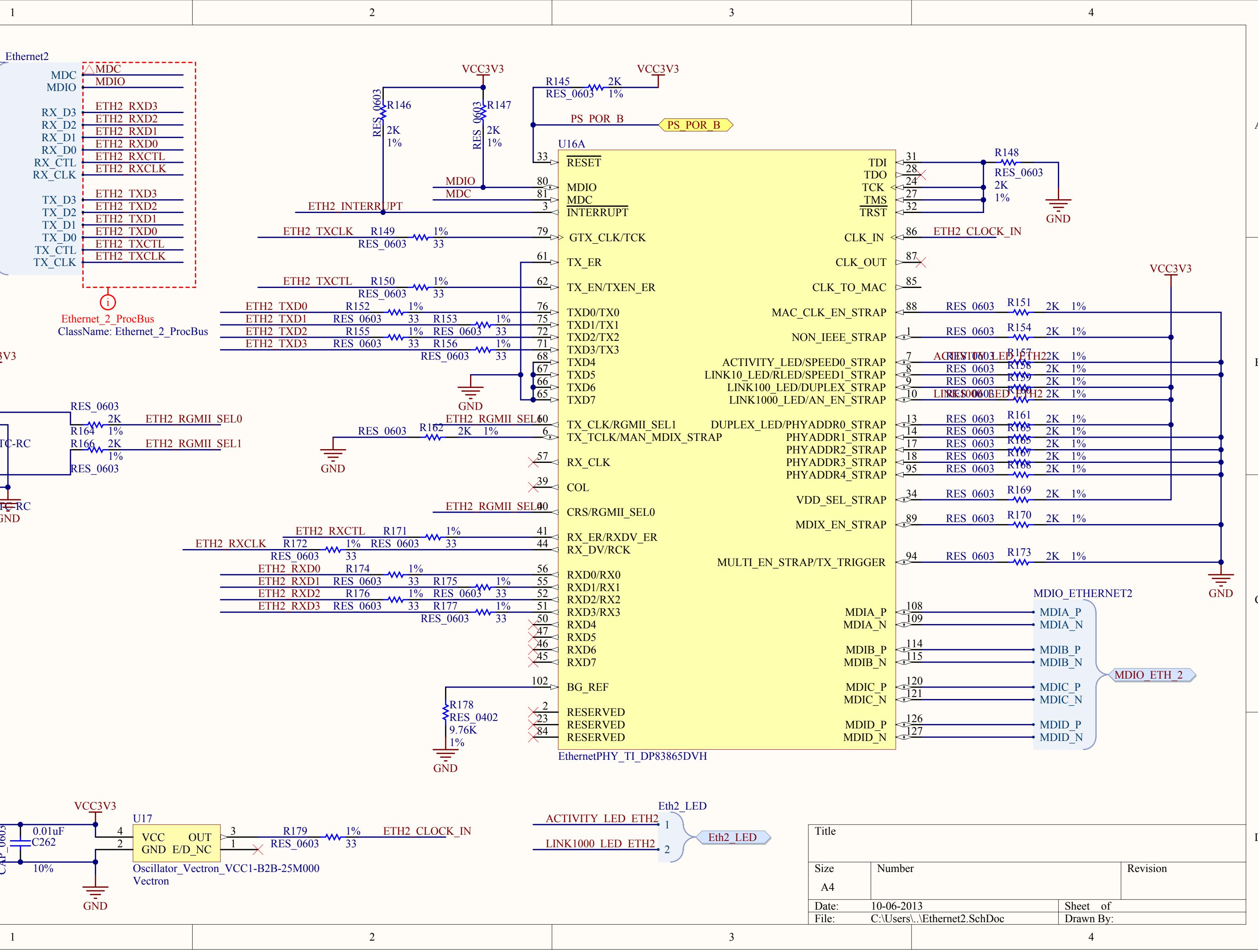
Title		
Size A4	Number	Revision
Date:	10-06-2013	Sheet of
File:	C:\Users\..\DDR3_1.SchDoc	Drawn By:



Title		
Size A4	Number	Revision
Date:	10-06-2013	Sheet of
File:	C:\Users\..\DDR3_2.SchDoc	Drawn By:







Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Ethernet2.SchDoc	Drawn By:

A

A

B

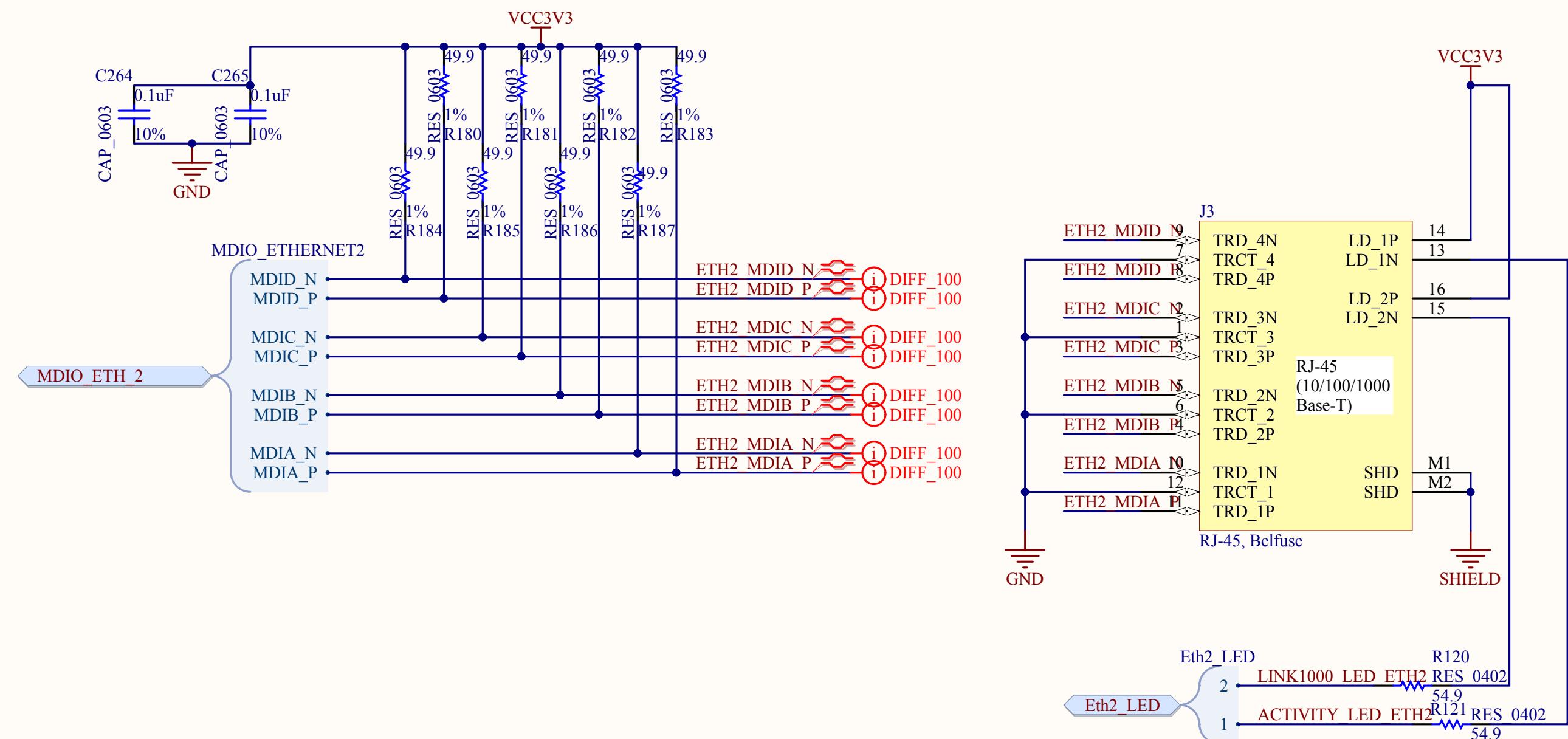
B

C

C

D

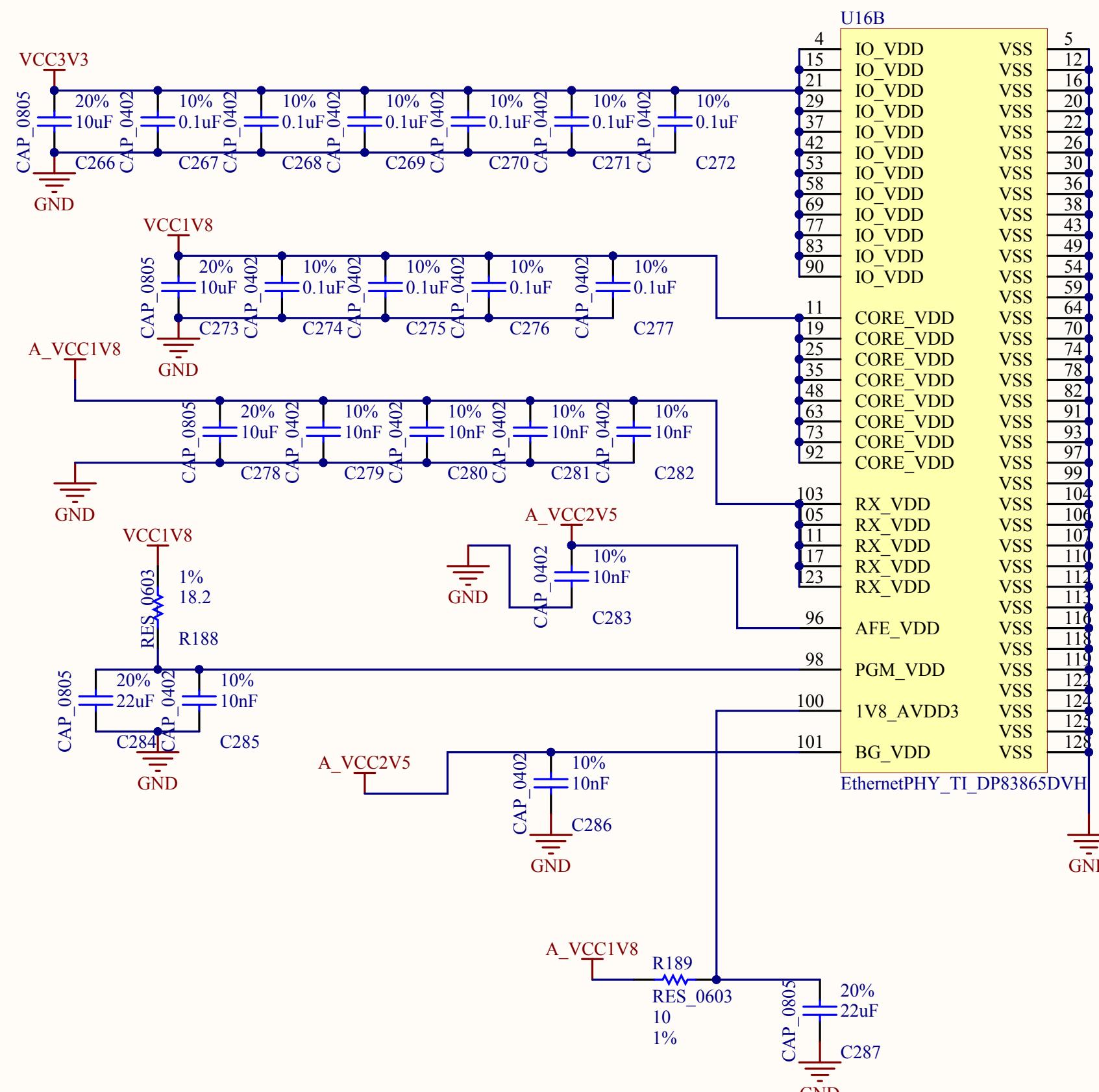
D



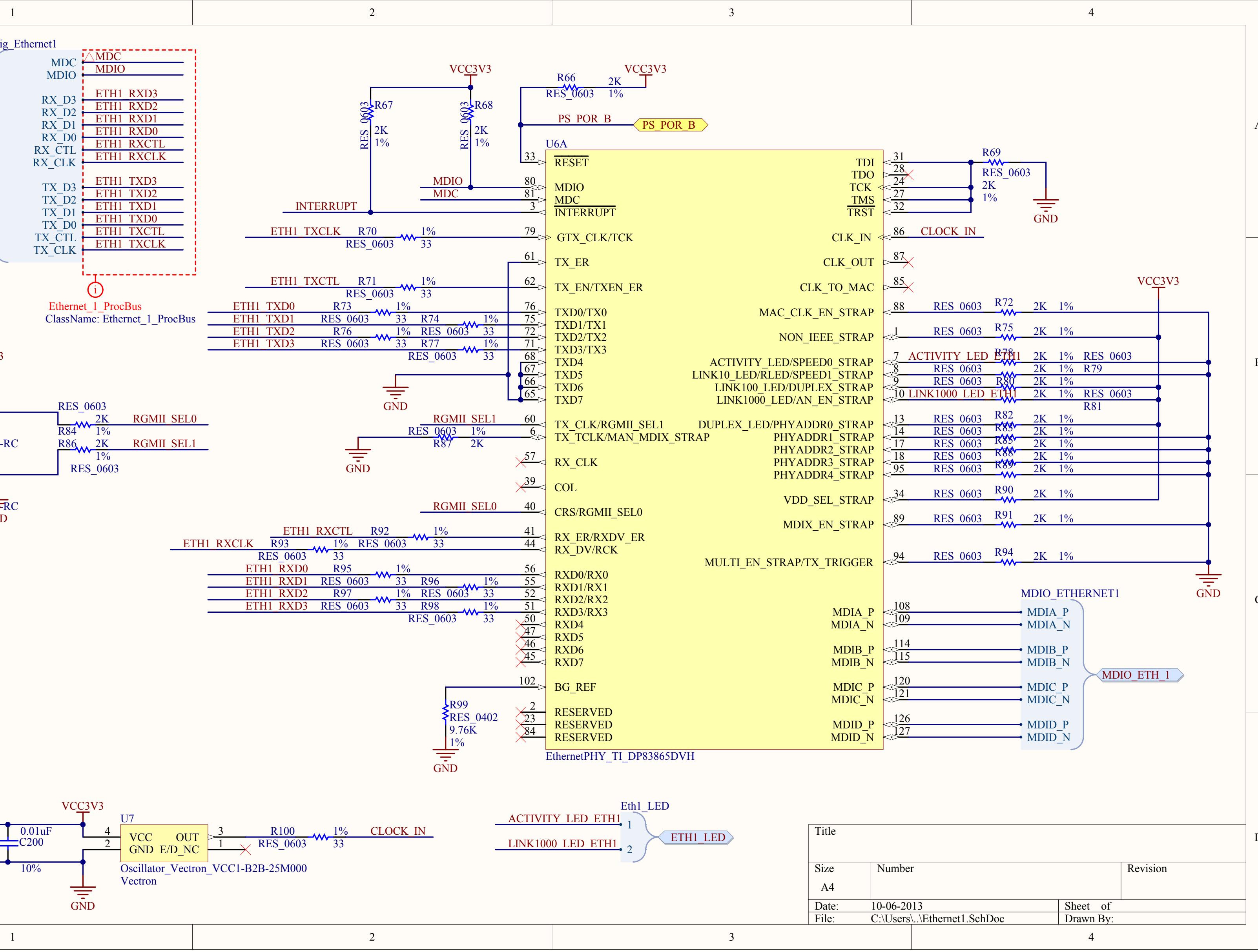
Title

Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Ethernet2 MDIO.SchDoc	Drawn By:

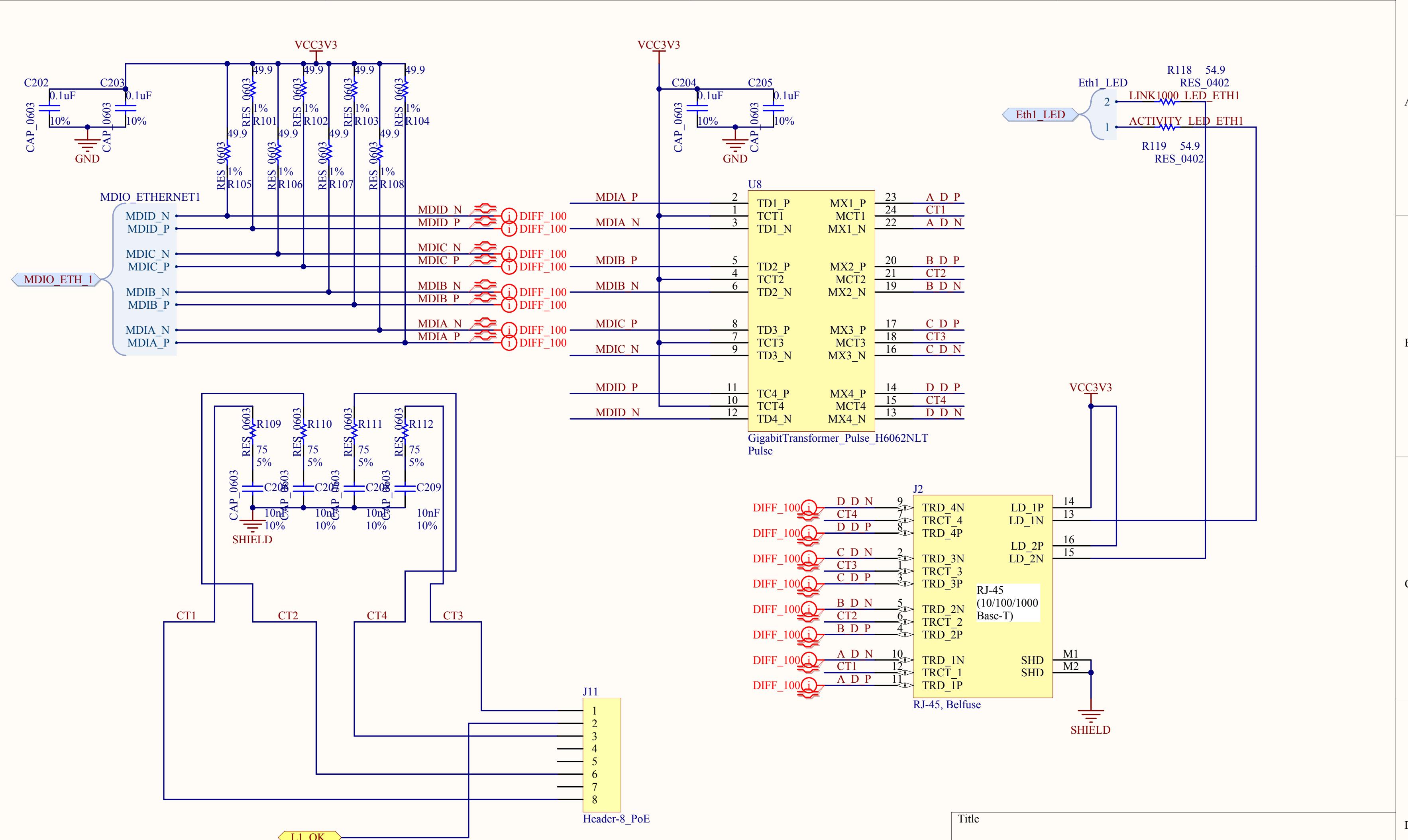
A



Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Ethernet2_Power.SchDoc	Drawn By:

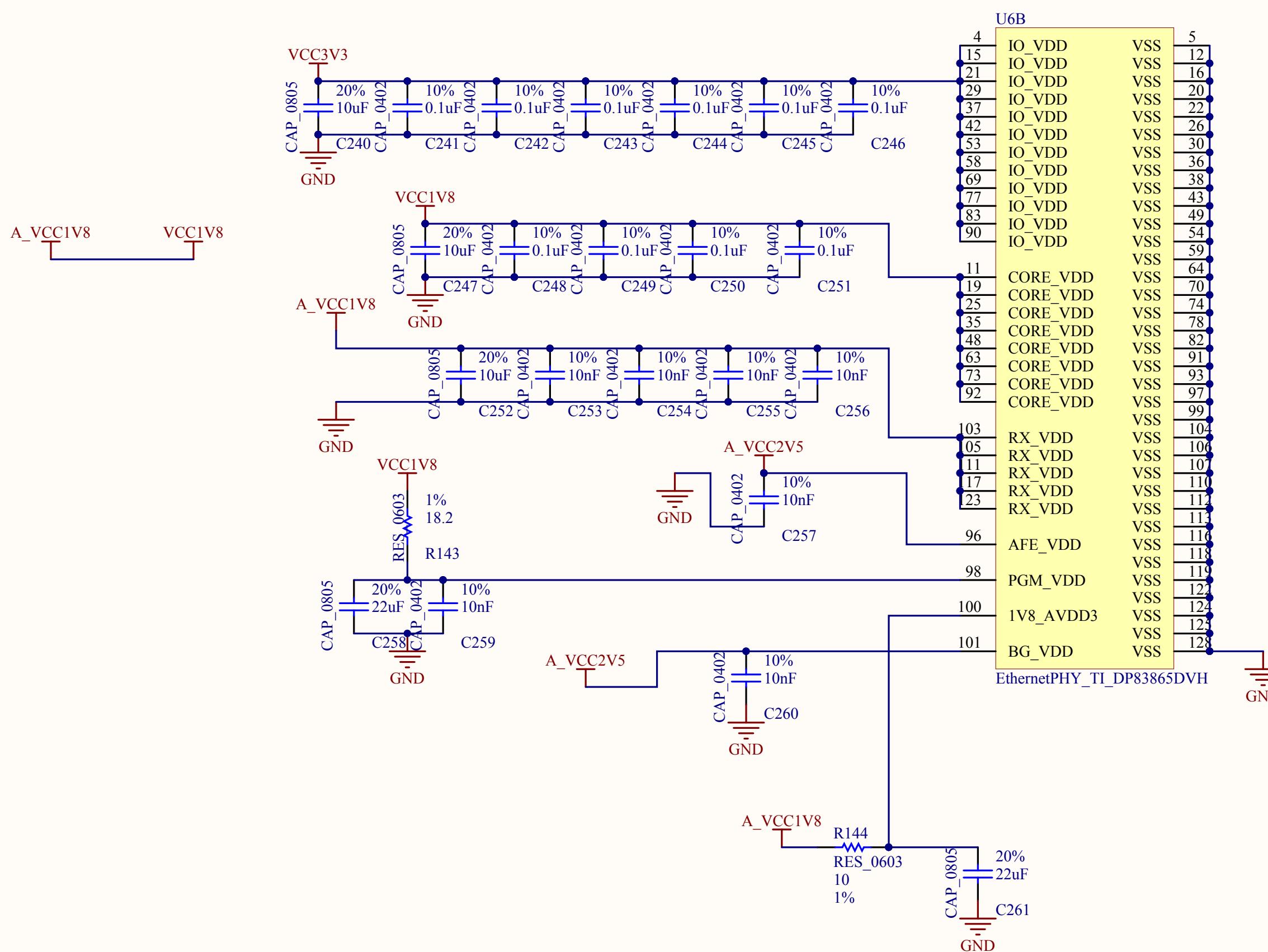


Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Ethernet1.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\...\Ethernet1 MDIO.SchDoc	Drawn By:

A



Title

Size

A4

Number

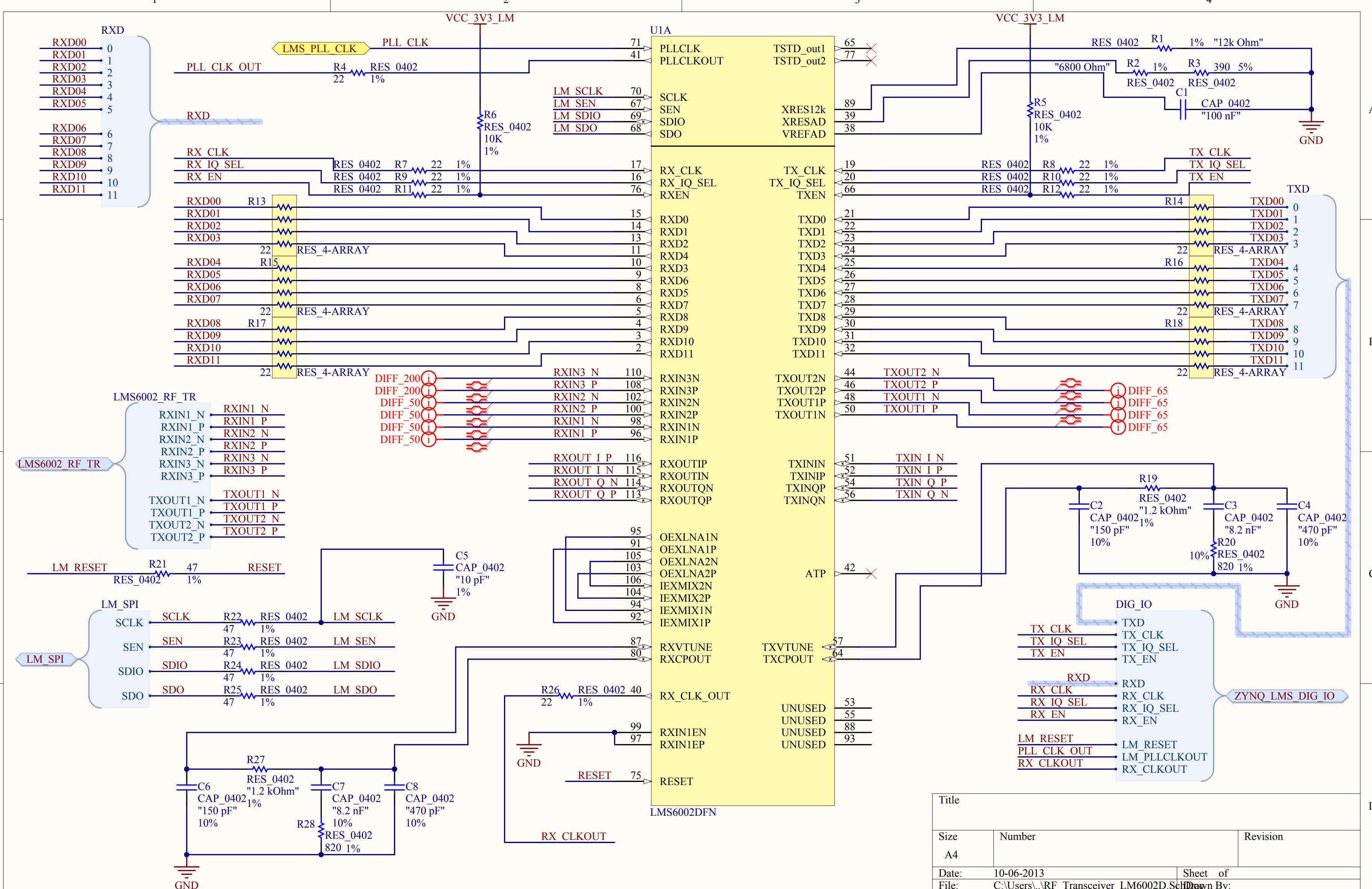
Revision

Date: 10-06-2013

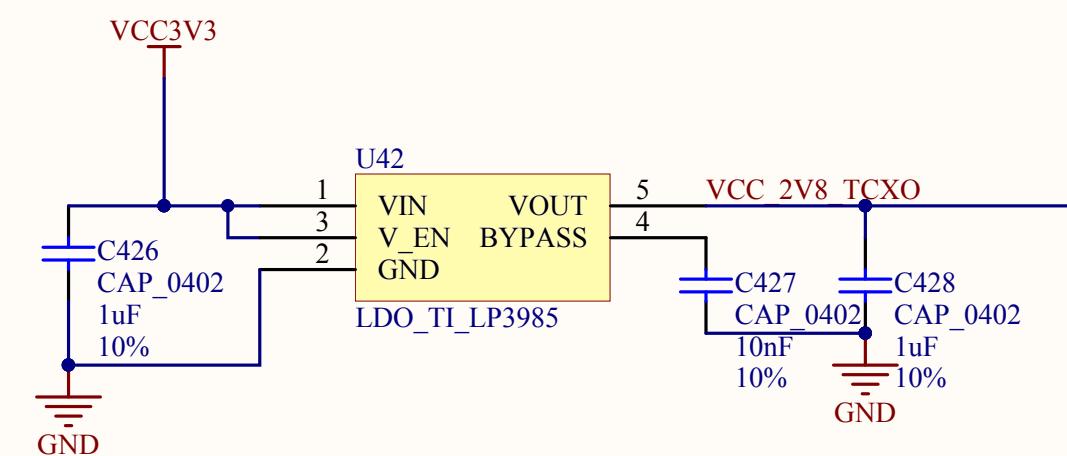
Sheet of

File: C:\Users\.\Ethernet1_Power.SchDoc

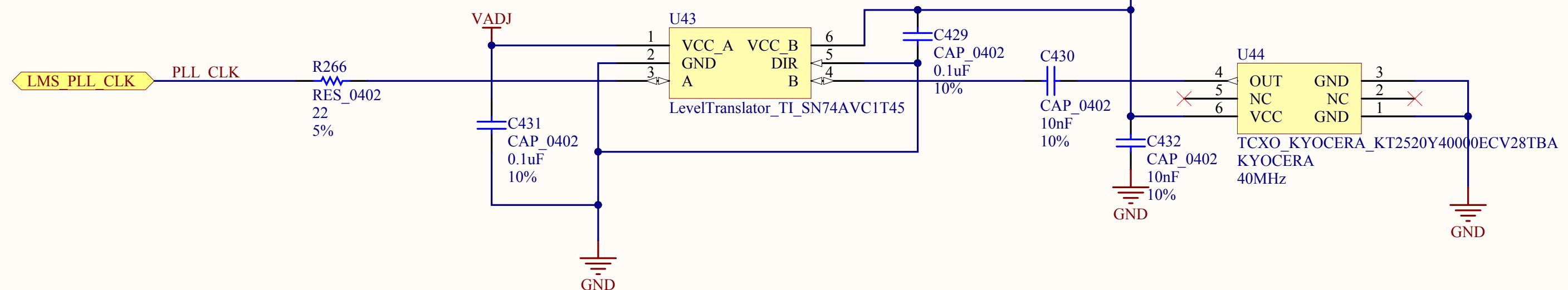
Drawn By:



A



A



B

C

C

D

D

Title

Size

A4

Number

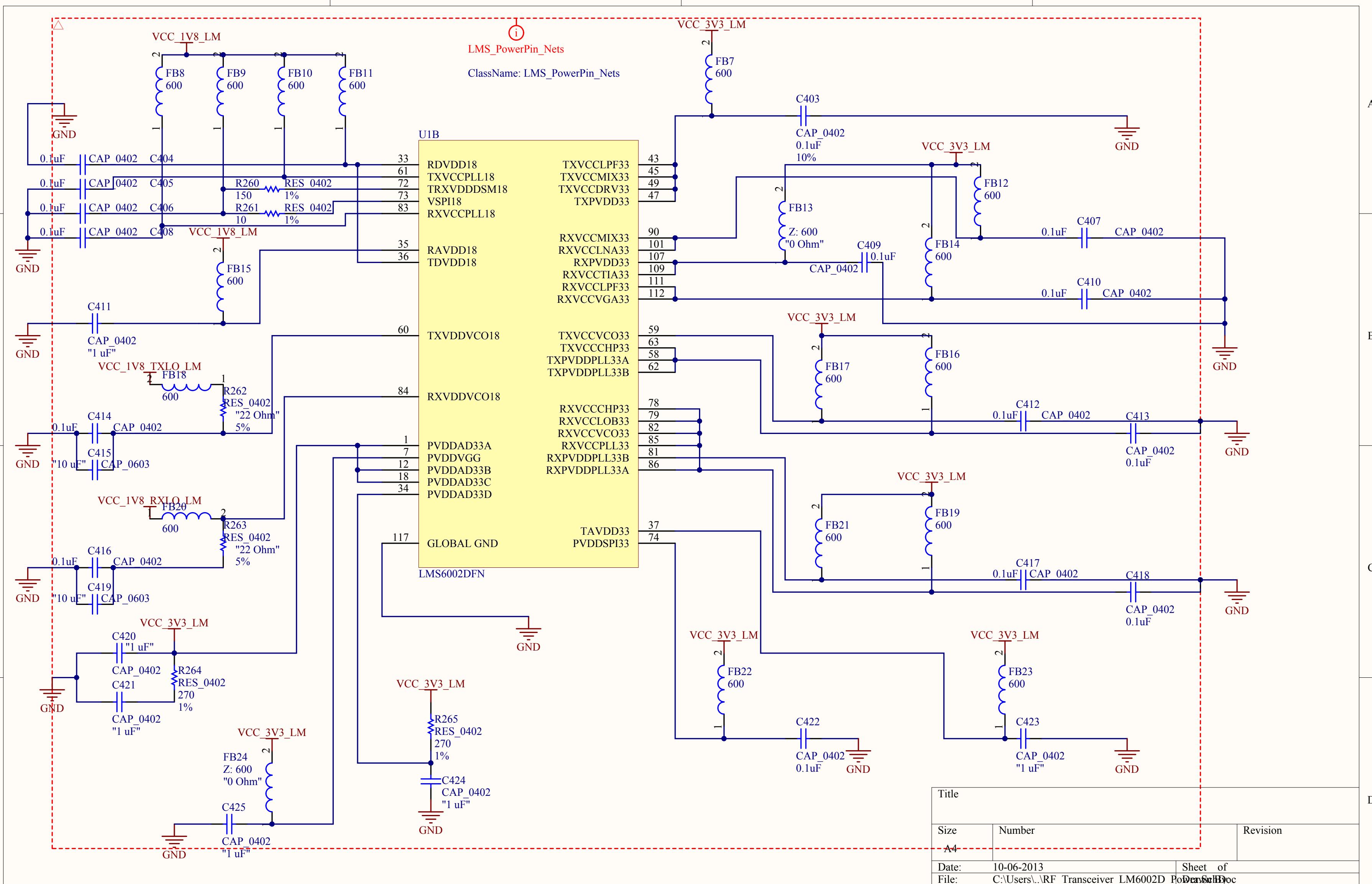
Revision

Date: 10-06-2013

Sheet of

File: C:\Users\..\RF Transceiver LMS6002 PLD\rfw\KBSchDoc

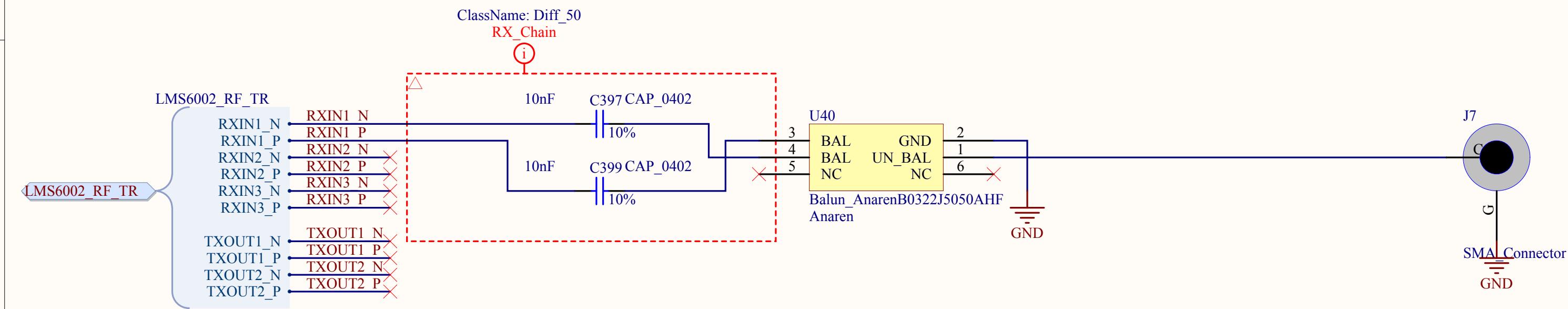
1 2 3 4



1 2 3 4

A

A



B

B

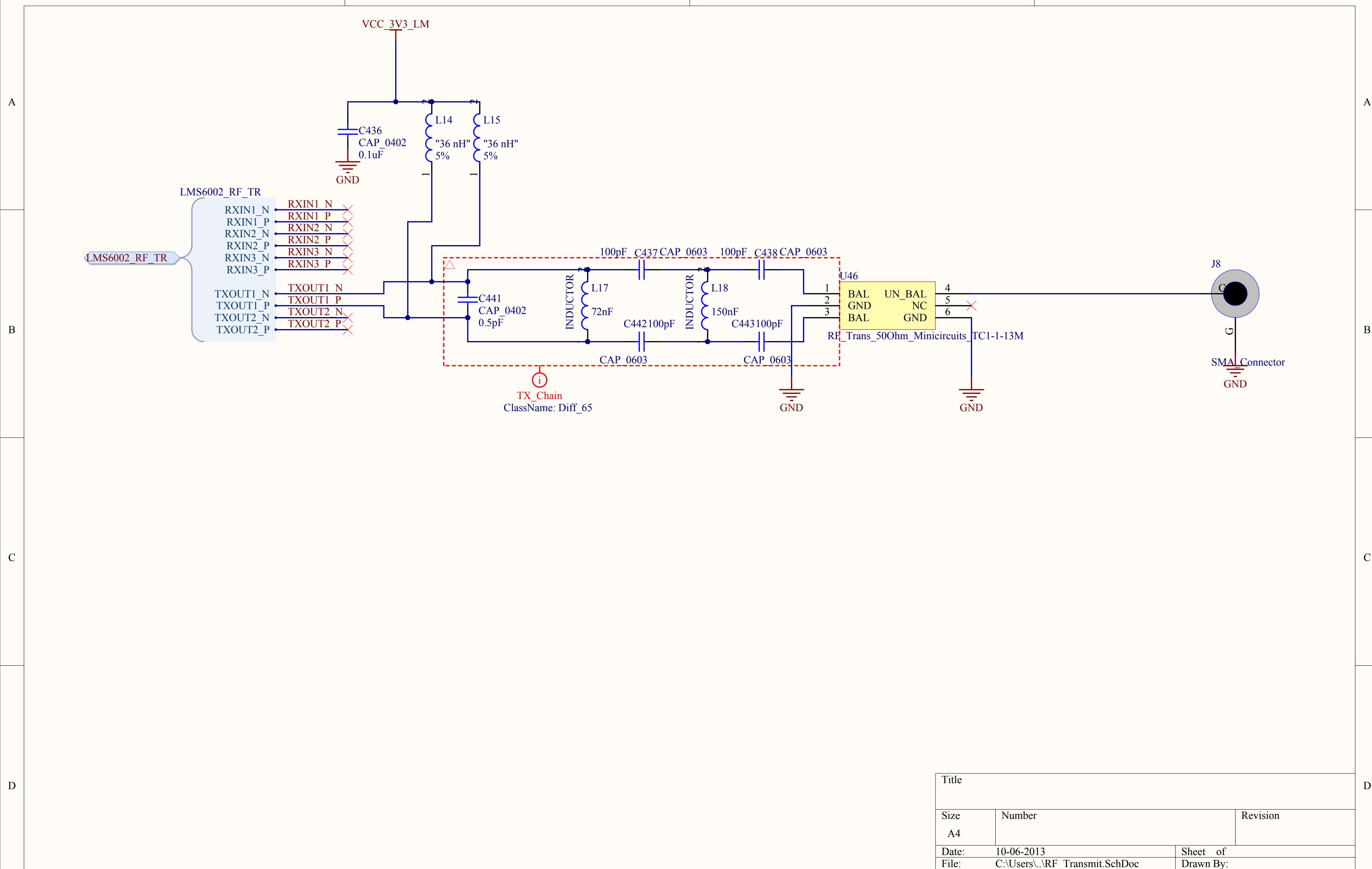
C

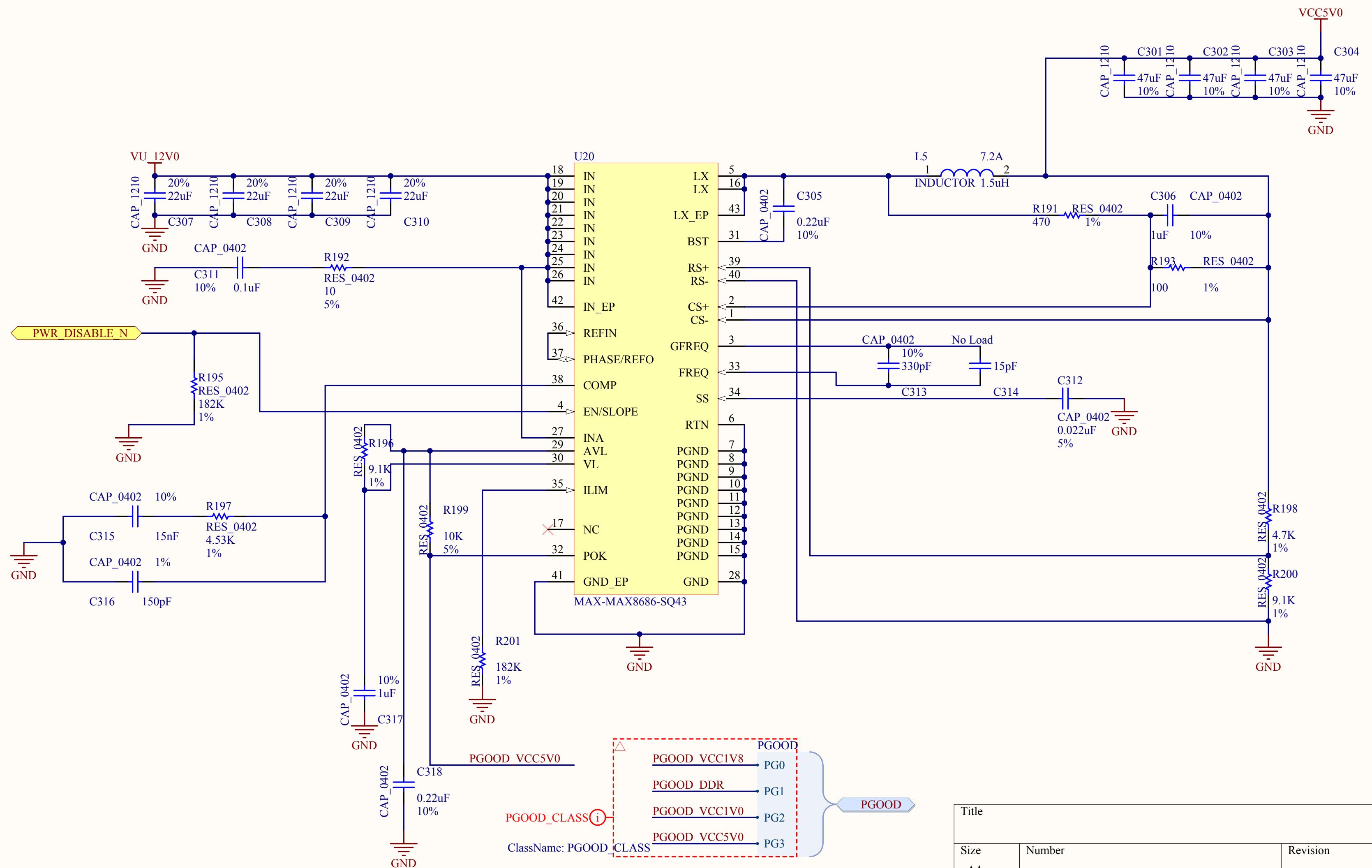
C

D

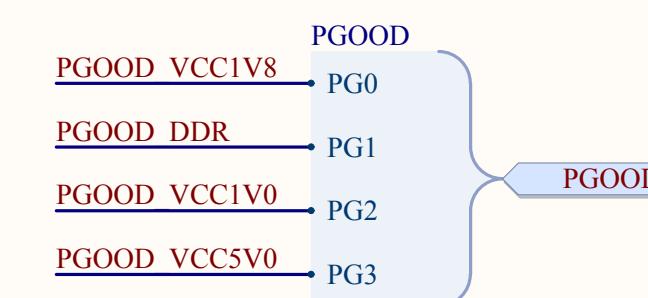
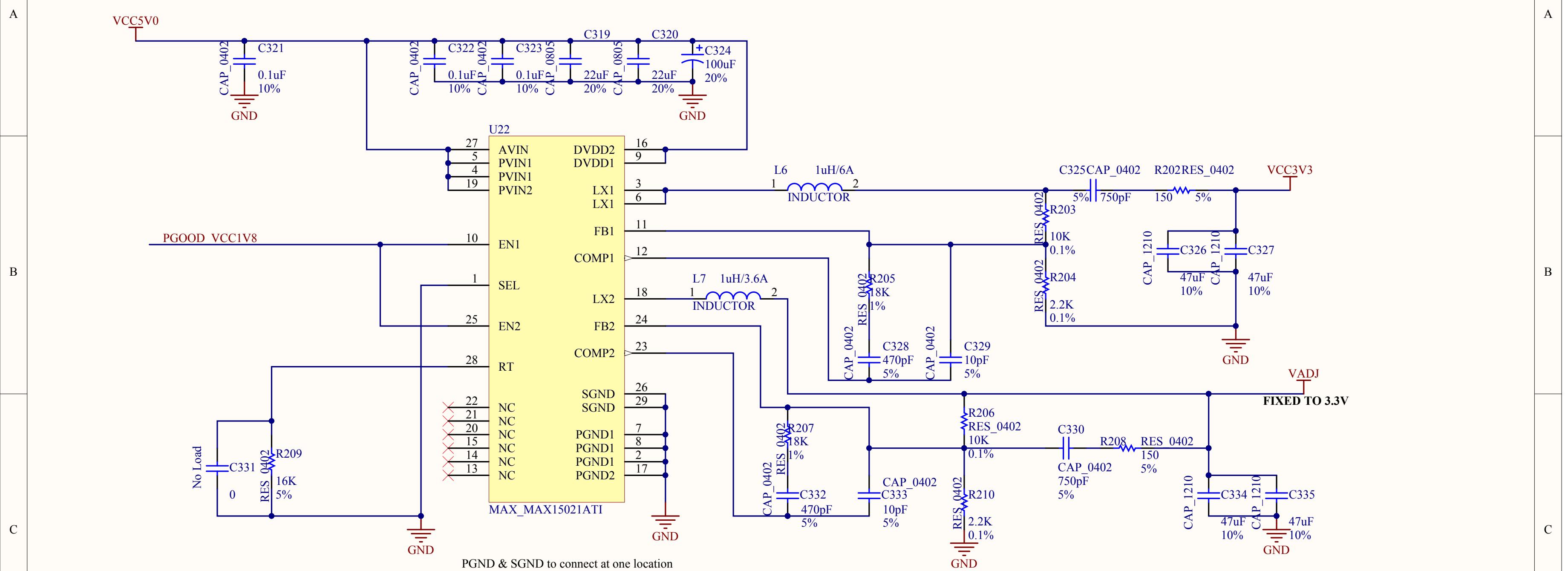
D

Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\RF_Receive.SchDoc	Drawn By:

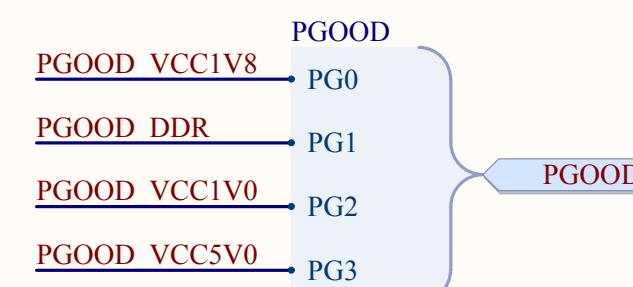
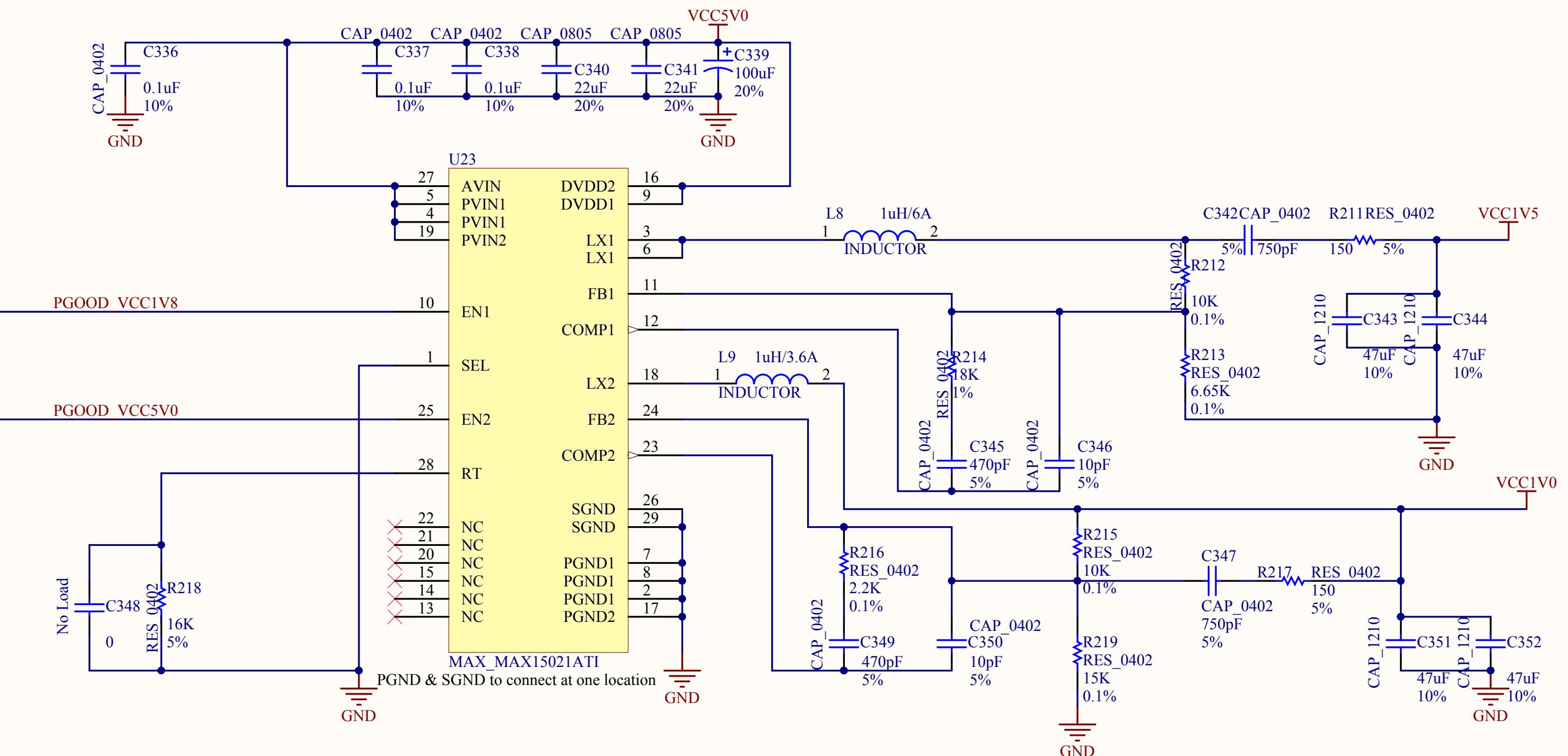




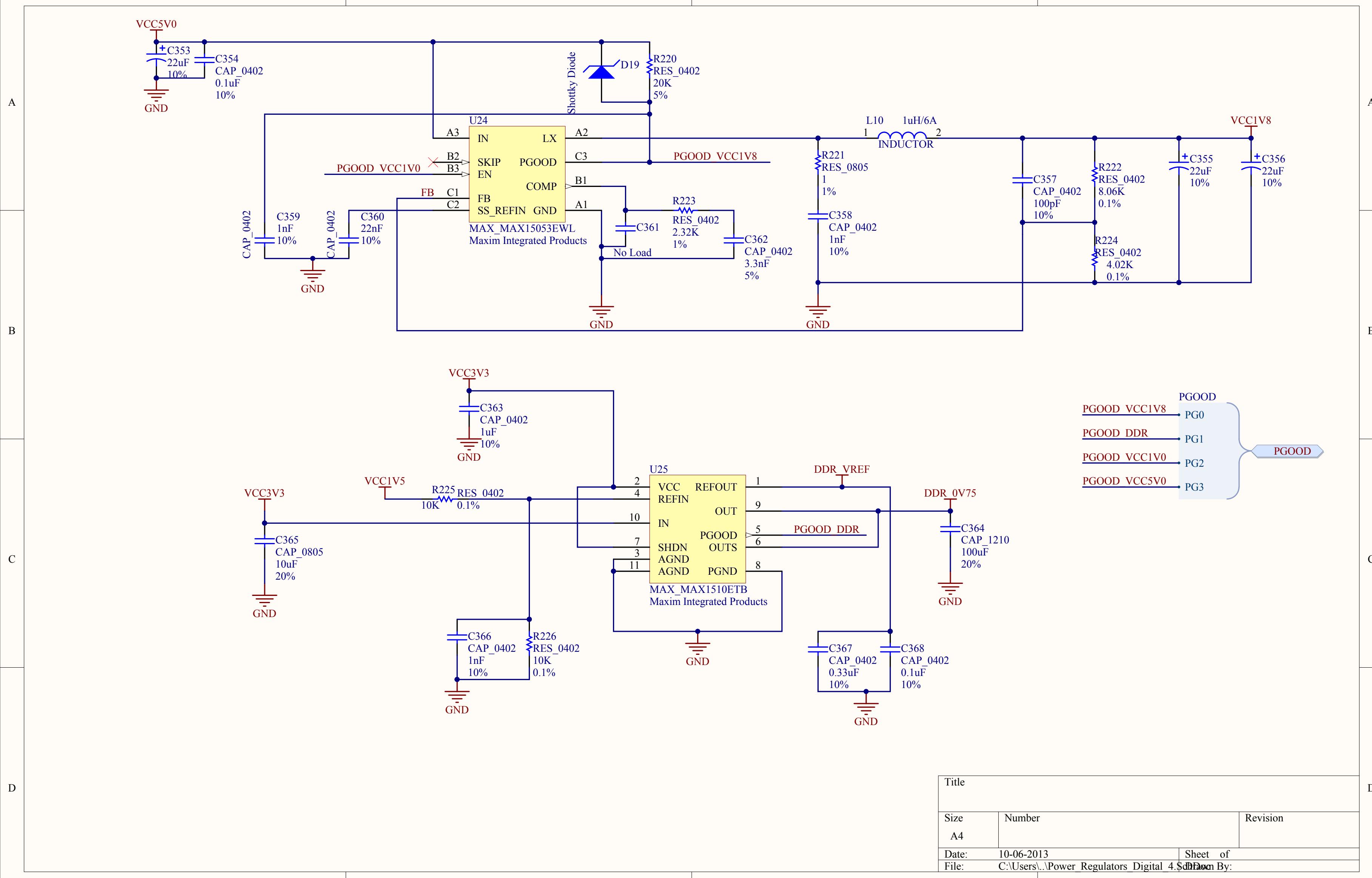
Title	
Size	Number
A4	
Date:	10-06-2013
File:	C:\Users\..\Power Regulators Digital 1.\$D\$E\$on By:

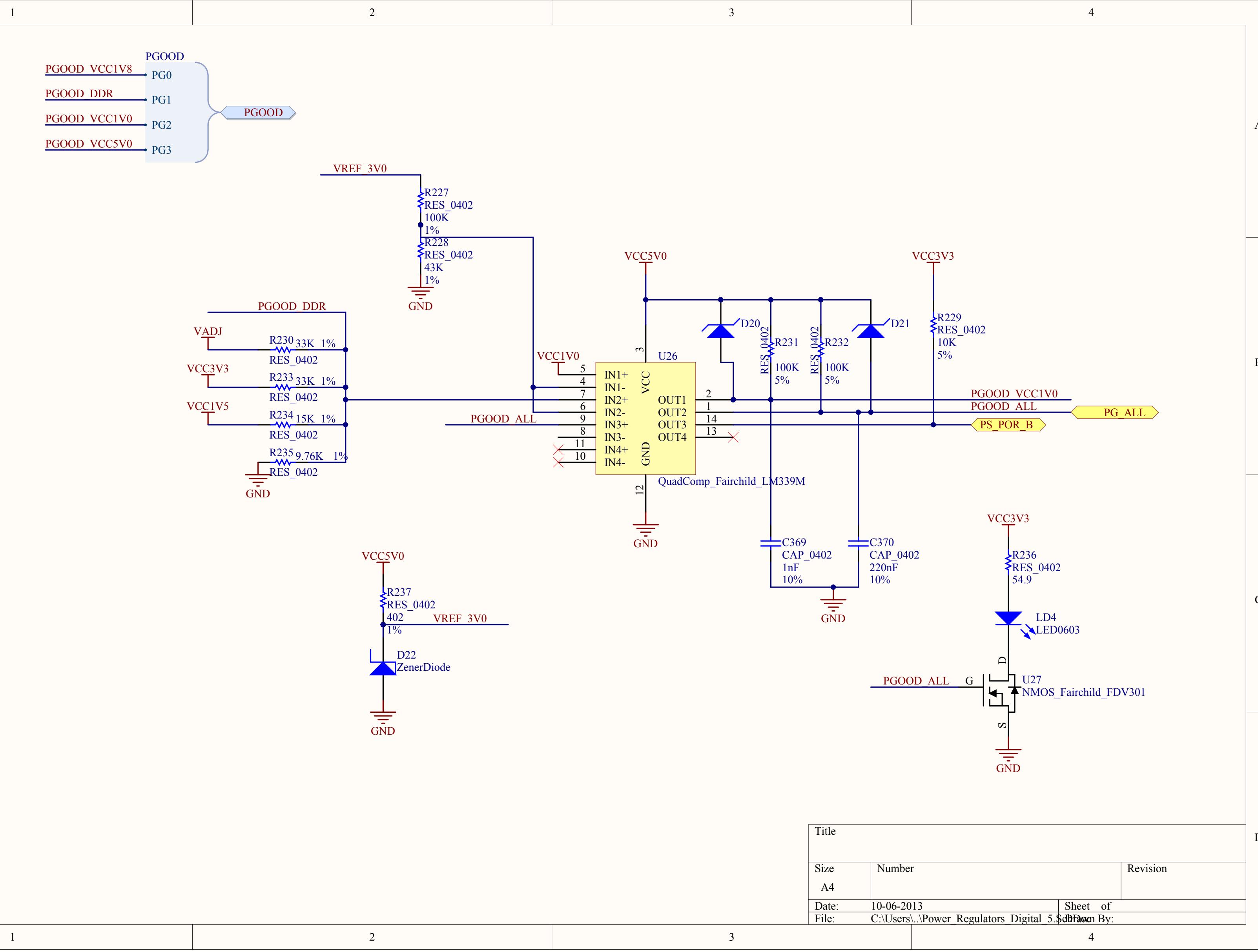


Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Power Regulators Digital 2.schDoc	

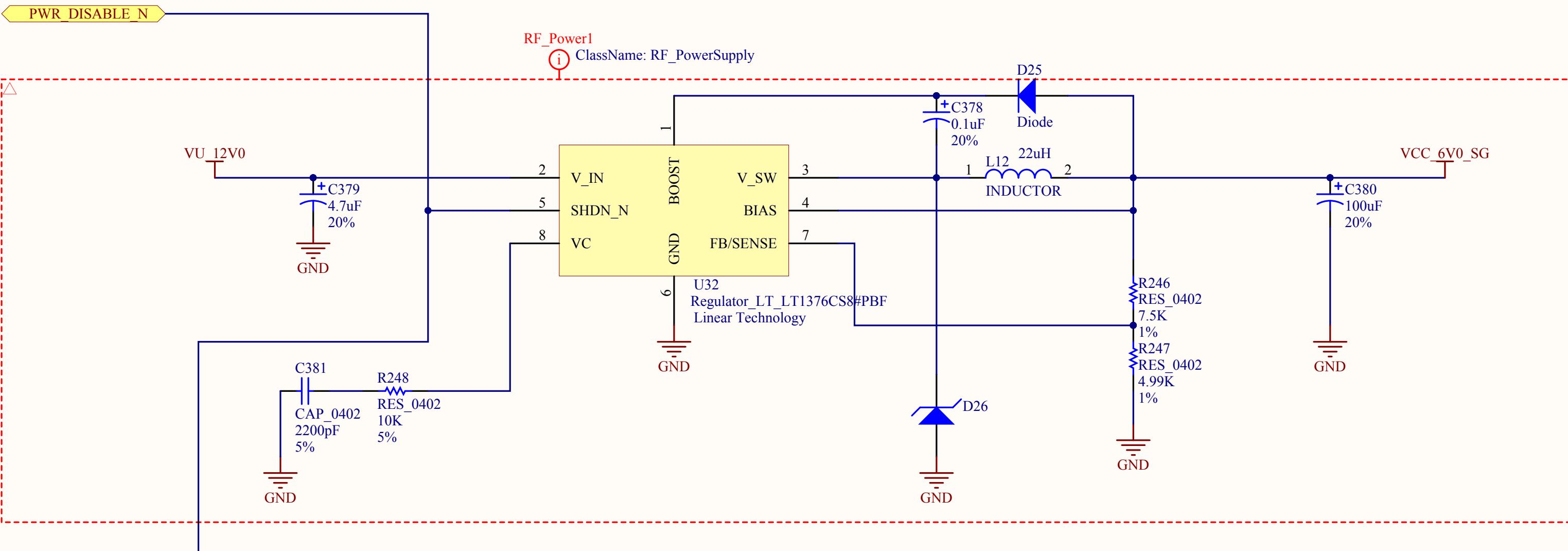


Title		
Size A4	Number	Revision
Date:	10-06-2013	Sheet of
File:	C:\Users\..\Power Regulators Digital 3.SD	Download By:

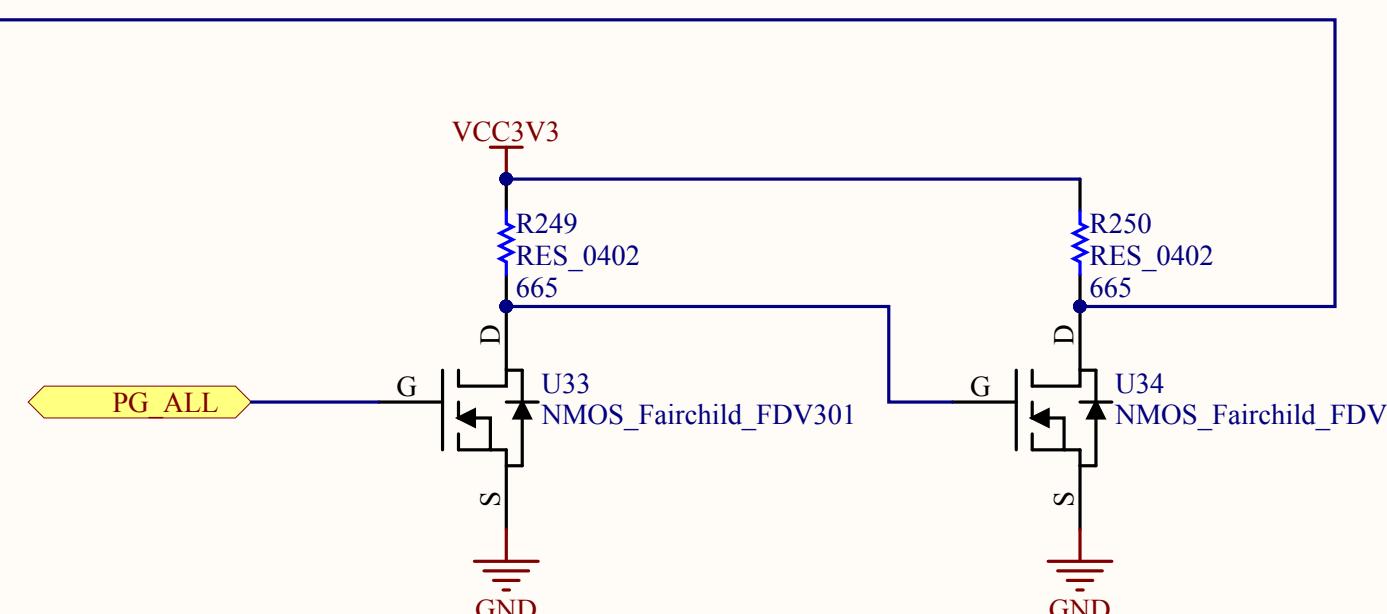




A



B



Title

Size

A4

Number

Revision

Date: 10-06-2013

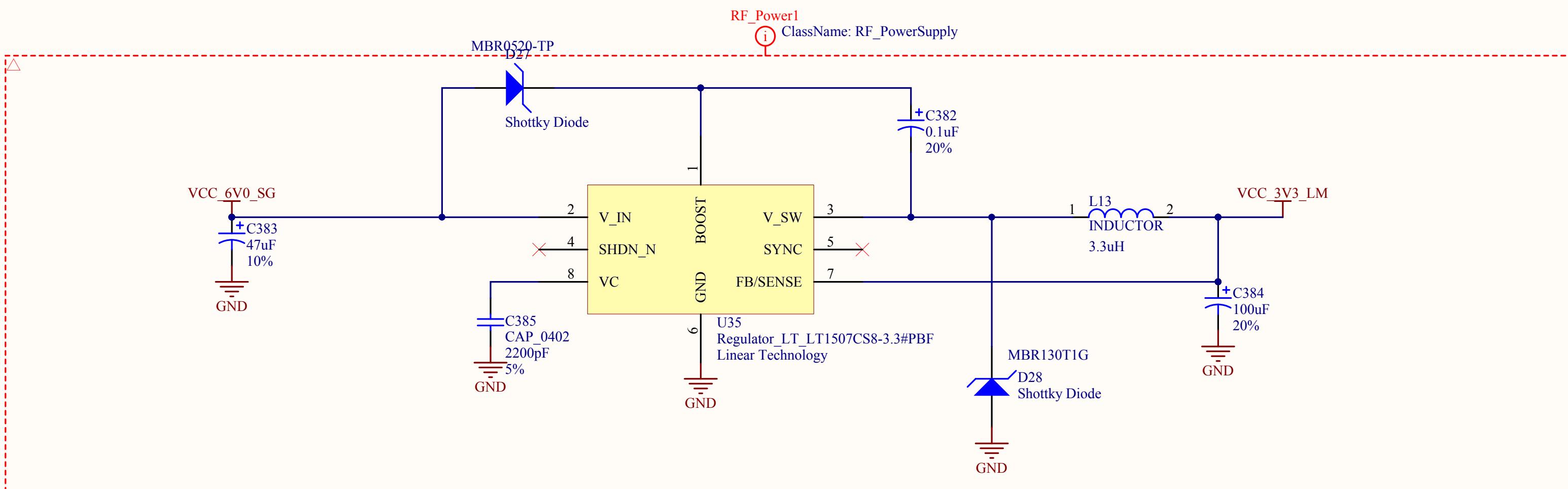
Sheet of

File: C:\Users\.\Power_Regulators_RF_2.SchDoc

Drawn By:

A

A



B

B

C

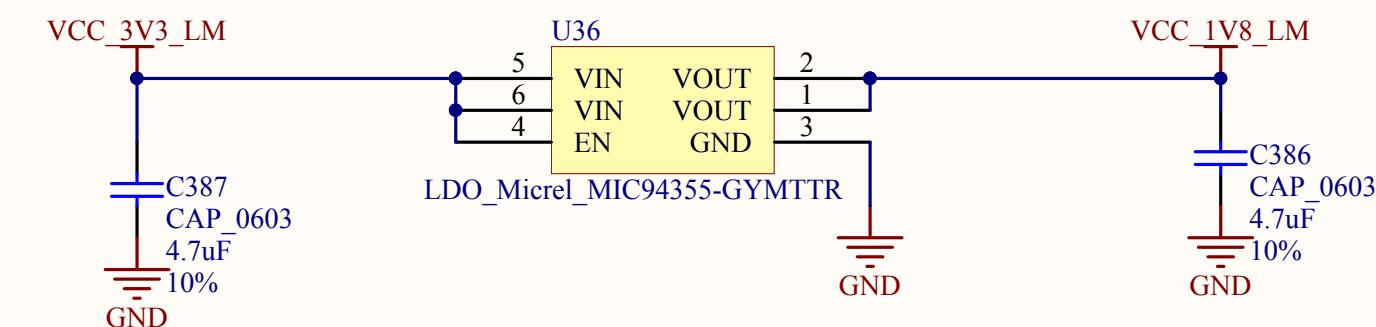
C

D

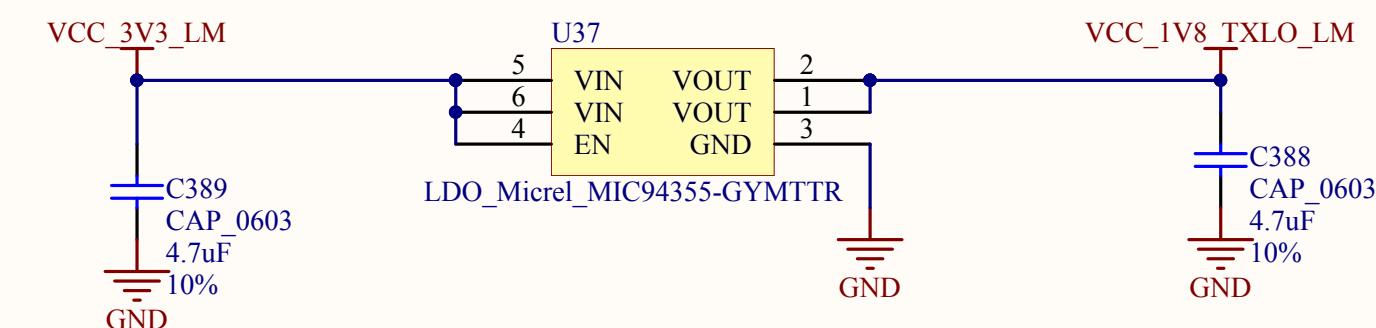
D

Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Power_Regulators_RF_3.SchDoc	Drawn By:

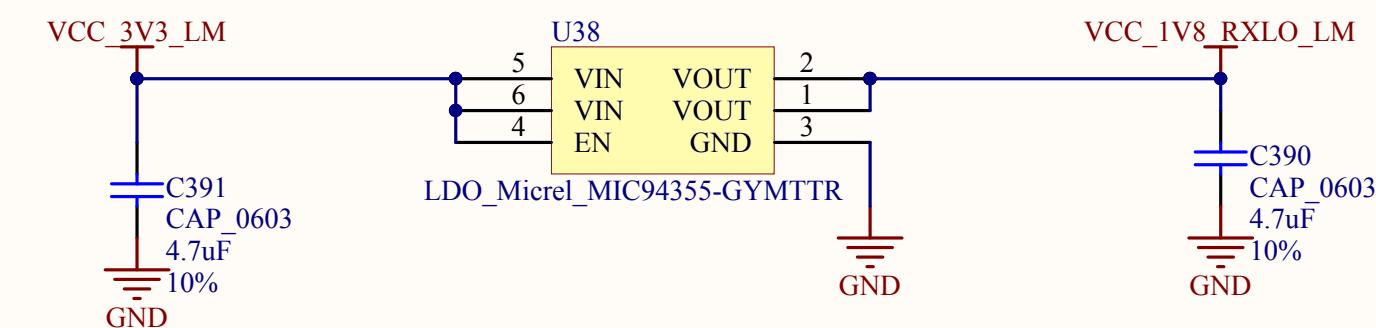
A



B



C



D

Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\Power_Regulators_RF_4.SchDoc	Drawn By:

A

A

B

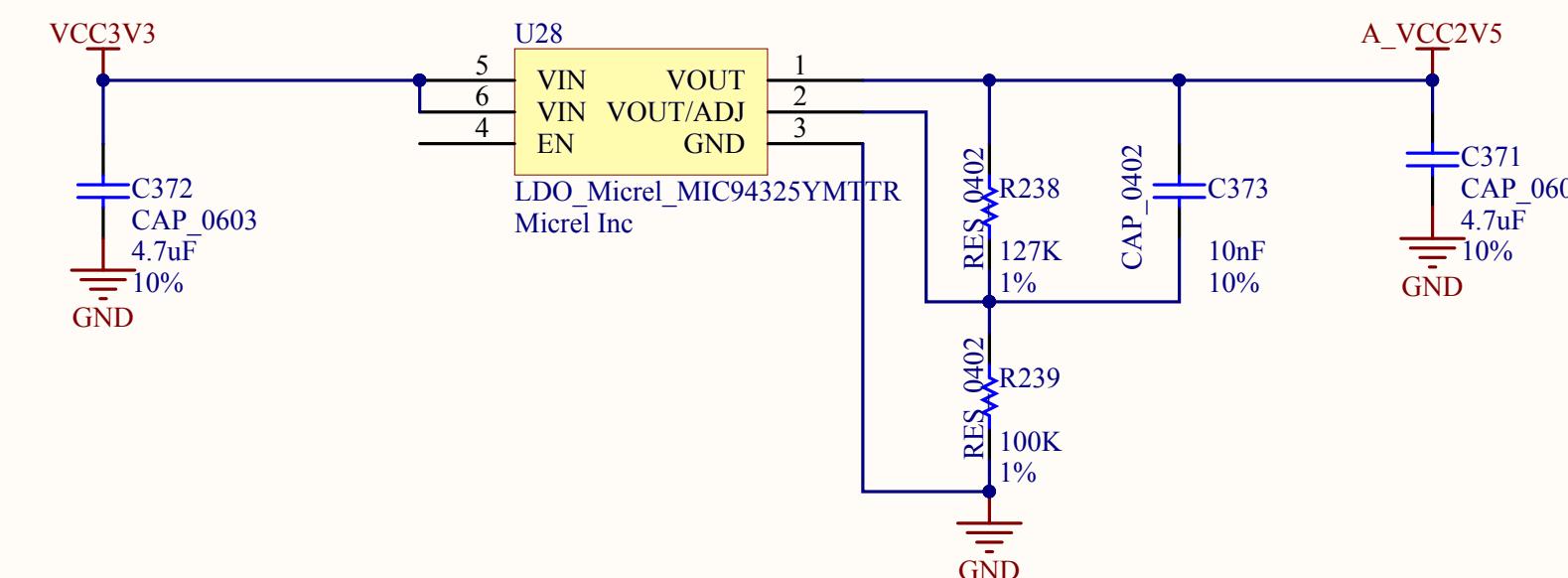
B

C

C

D

D



Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\Power_Regulators_Ether2V5.SchDoc	

A

A

B

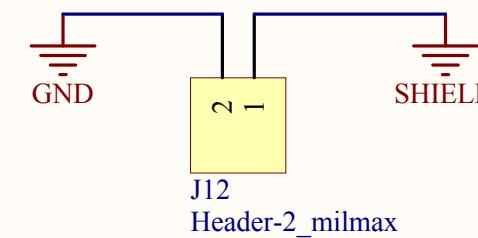
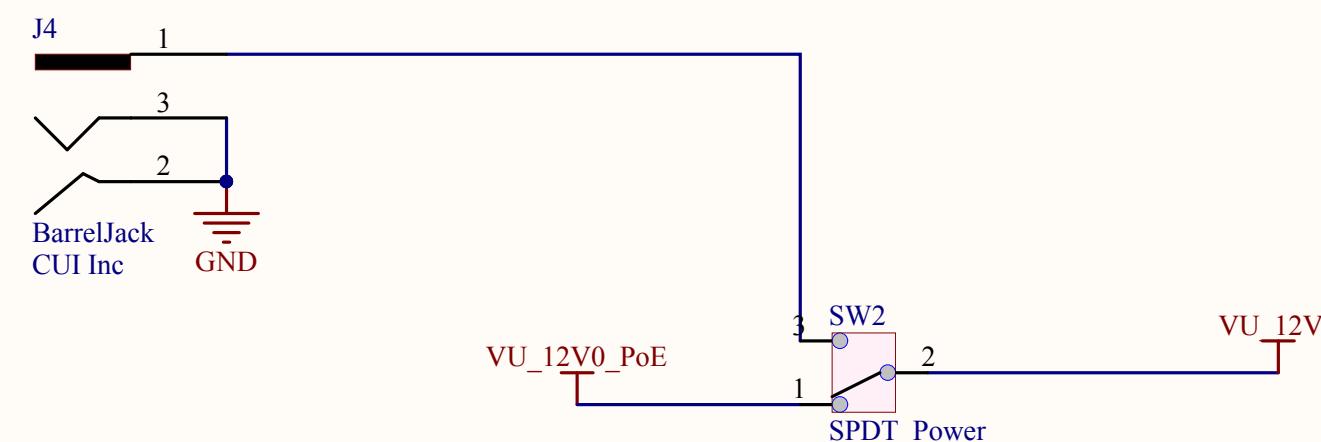
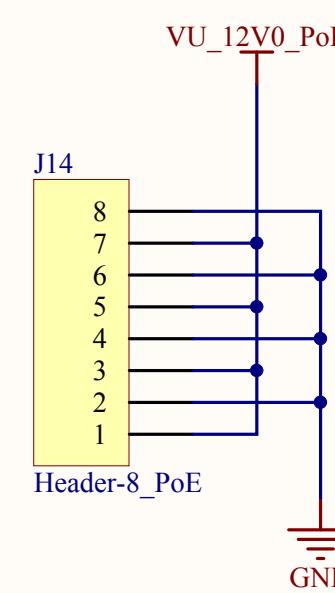
B

C

C

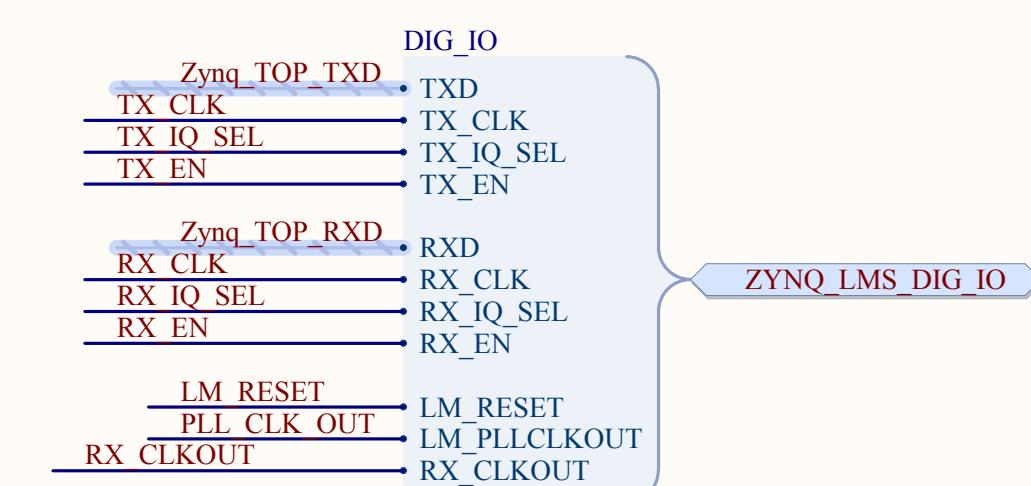
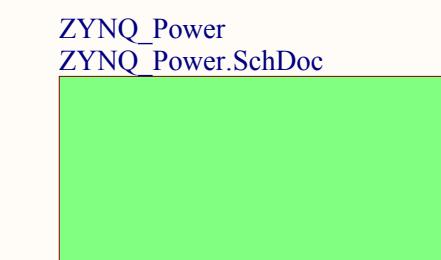
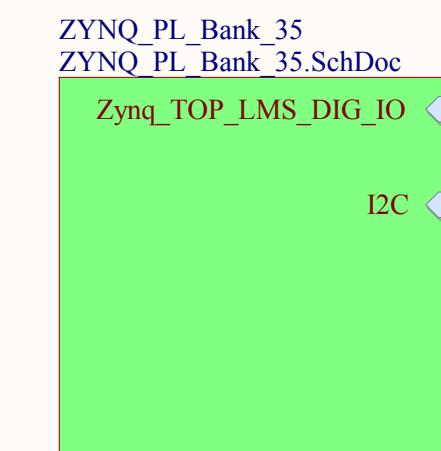
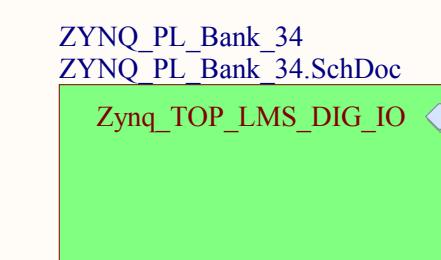
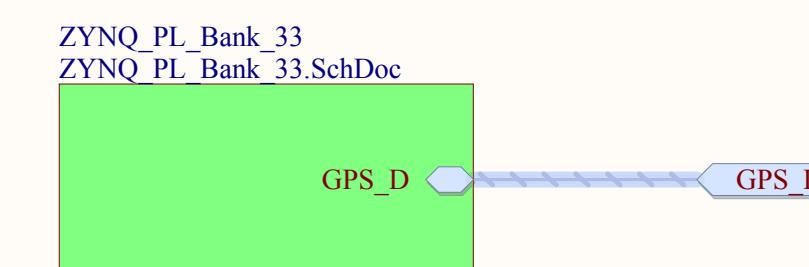
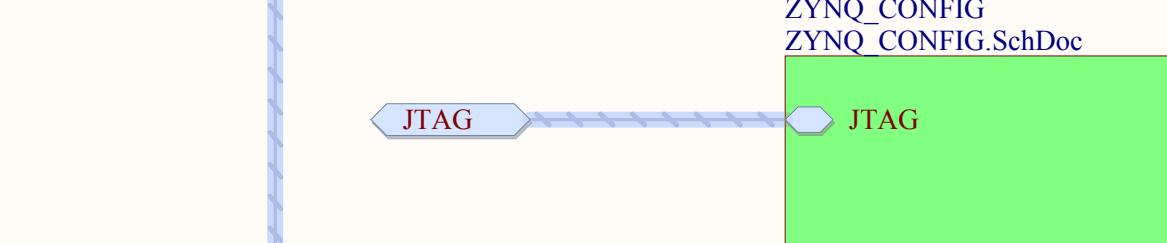
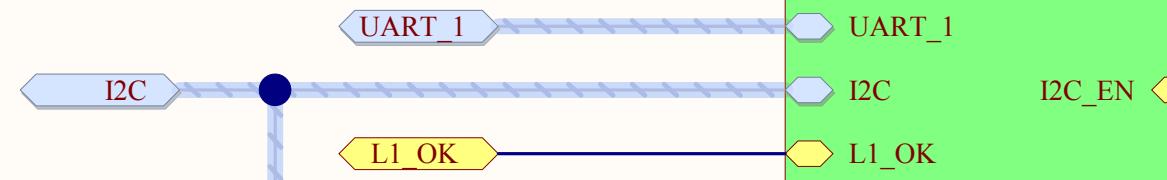
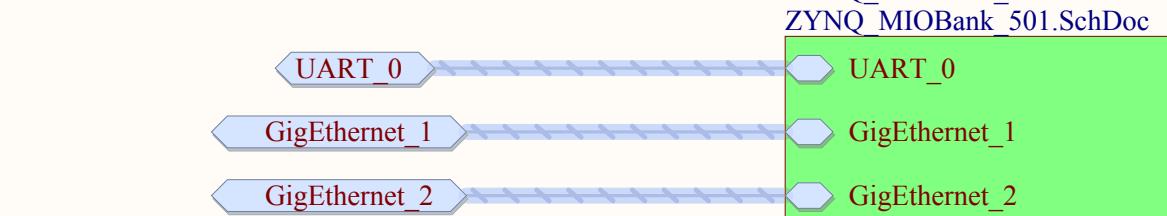
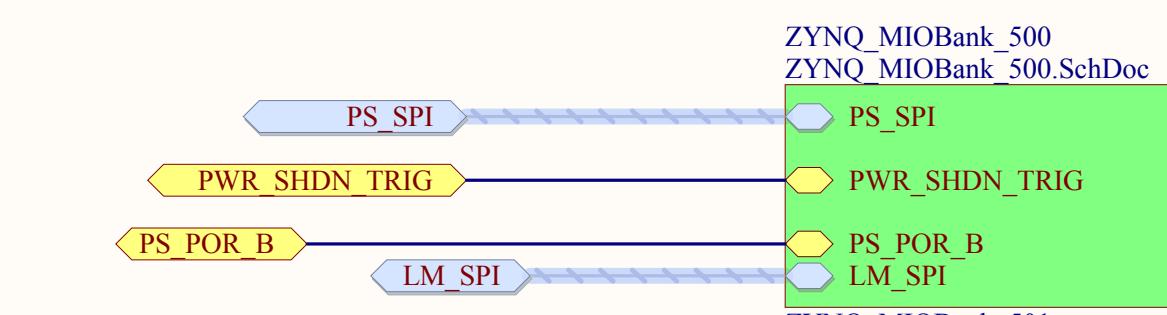
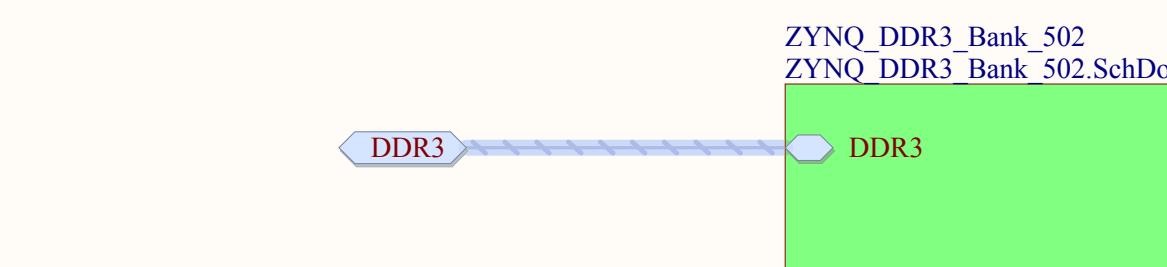
D

D



Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\PowerSwitch.SchDoc	Drawn By:

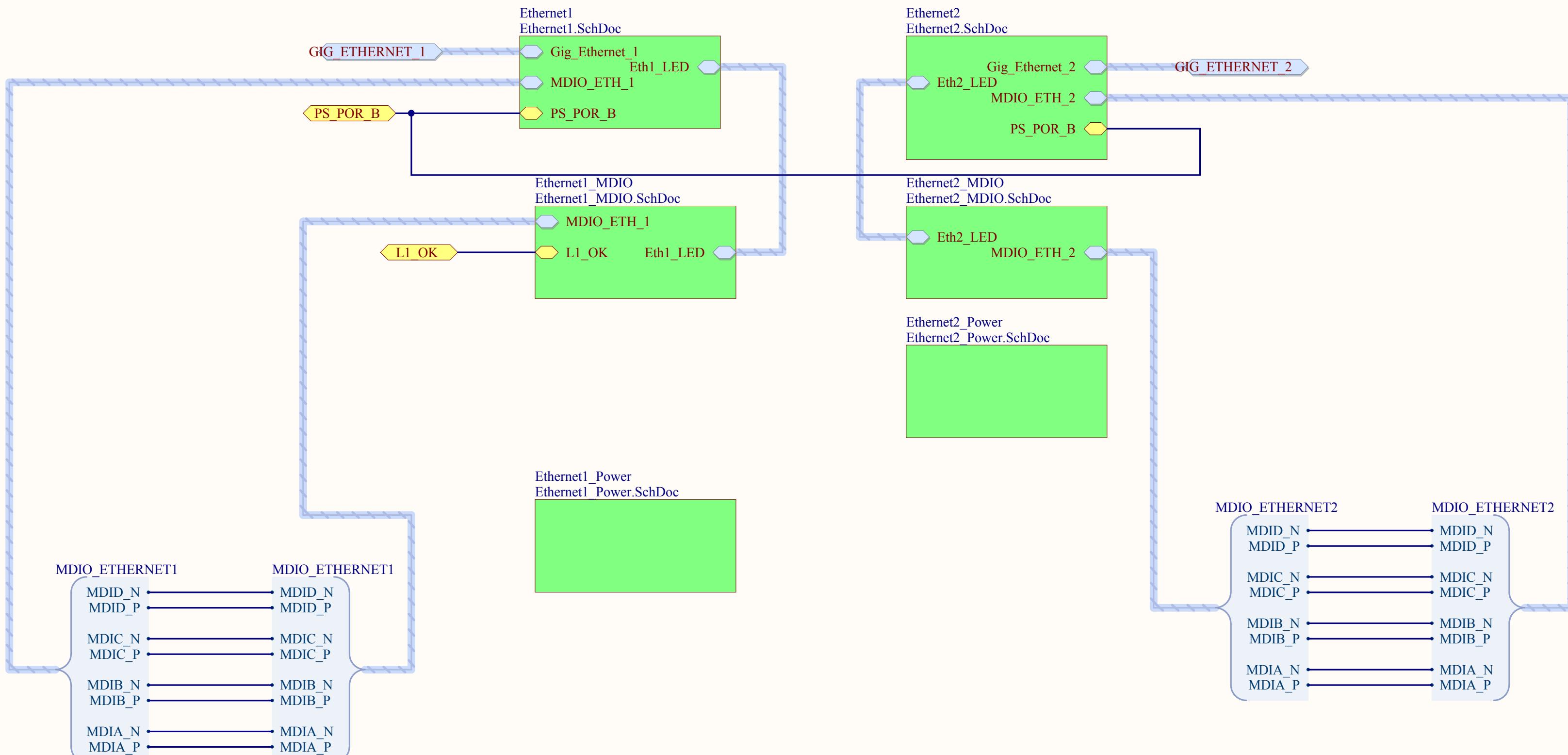
A



Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\ZYNQ_TOP_LEVEL.SchDoc	Drawn By:

A

A



Title

Size

A4

Number

Revision

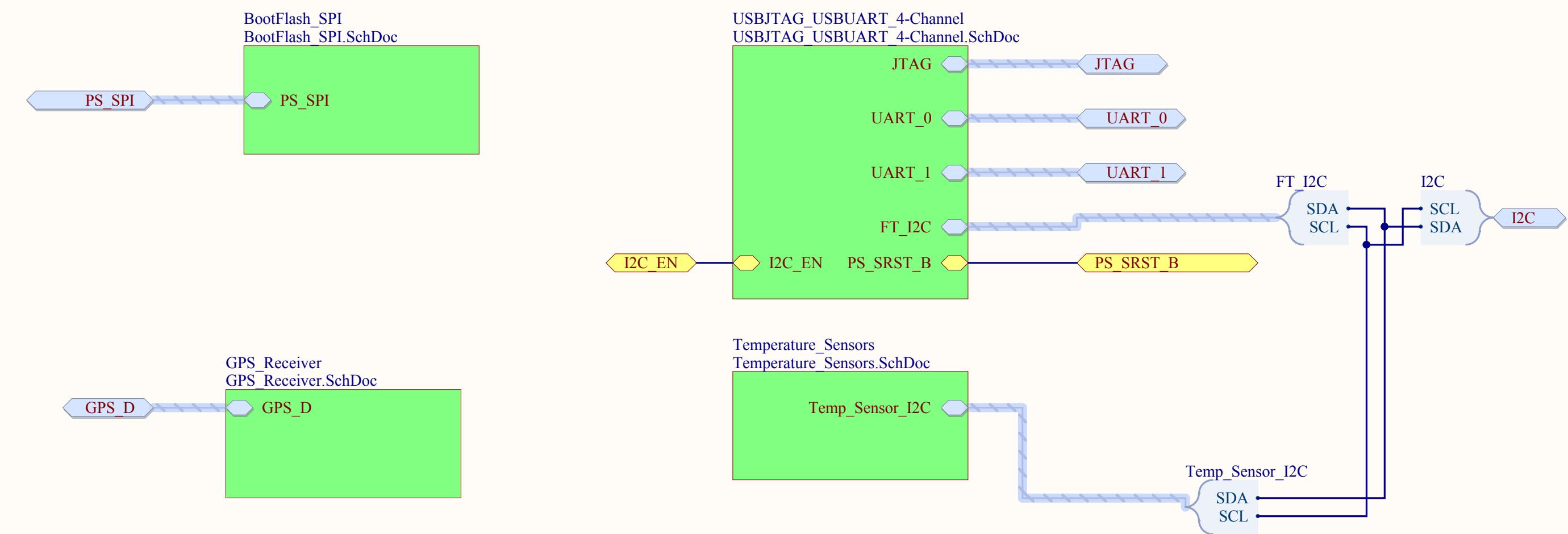
Date: 10-06-2013

Sheet of

File: C:\Users\.\ETHERNET_TOP_LEVEL.SchDoc Drawn By:

A

A

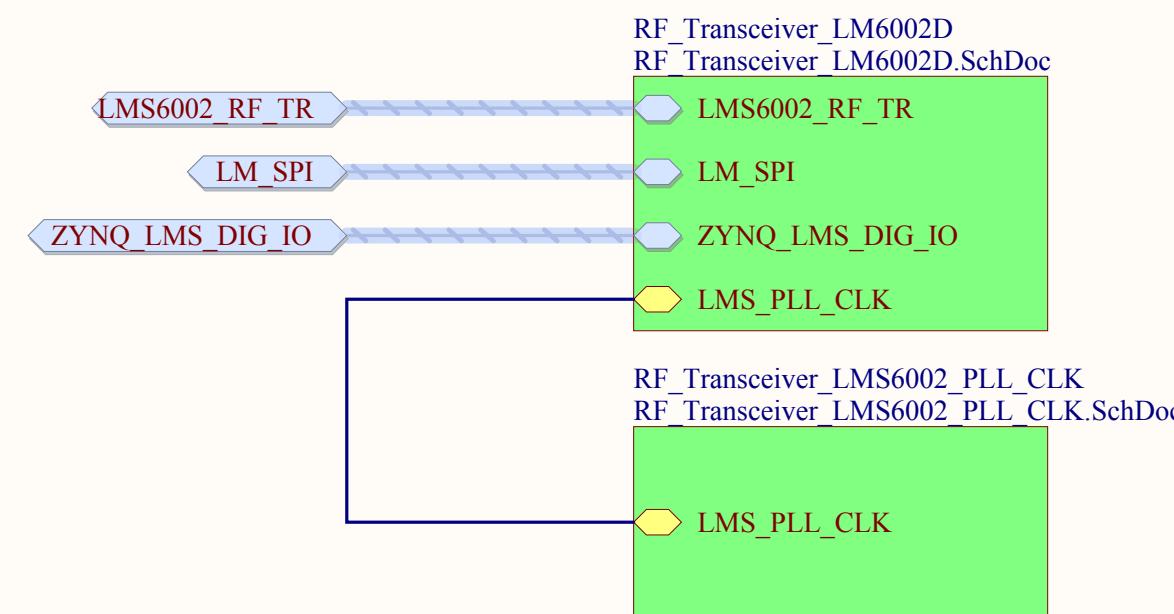


Ti

Size A4	Number	Revision
Date:	10-06-2013	Sheet of
File:	C:\Users\..\PERIPHERALS.SchDoc	Drawn By:

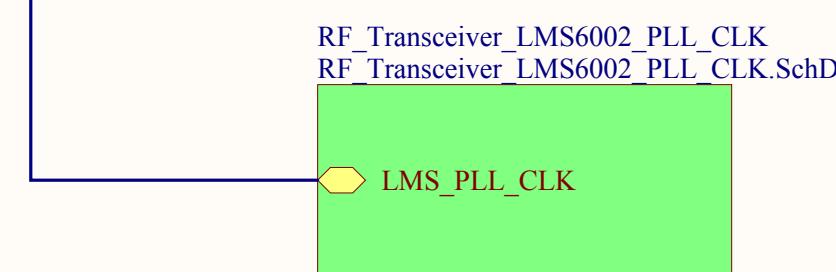
A

A



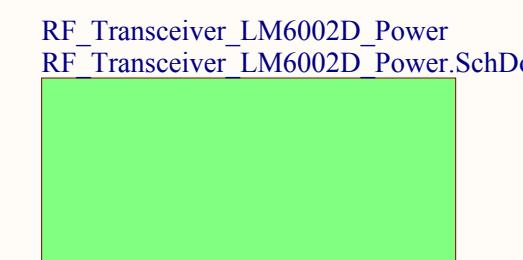
B

B



C

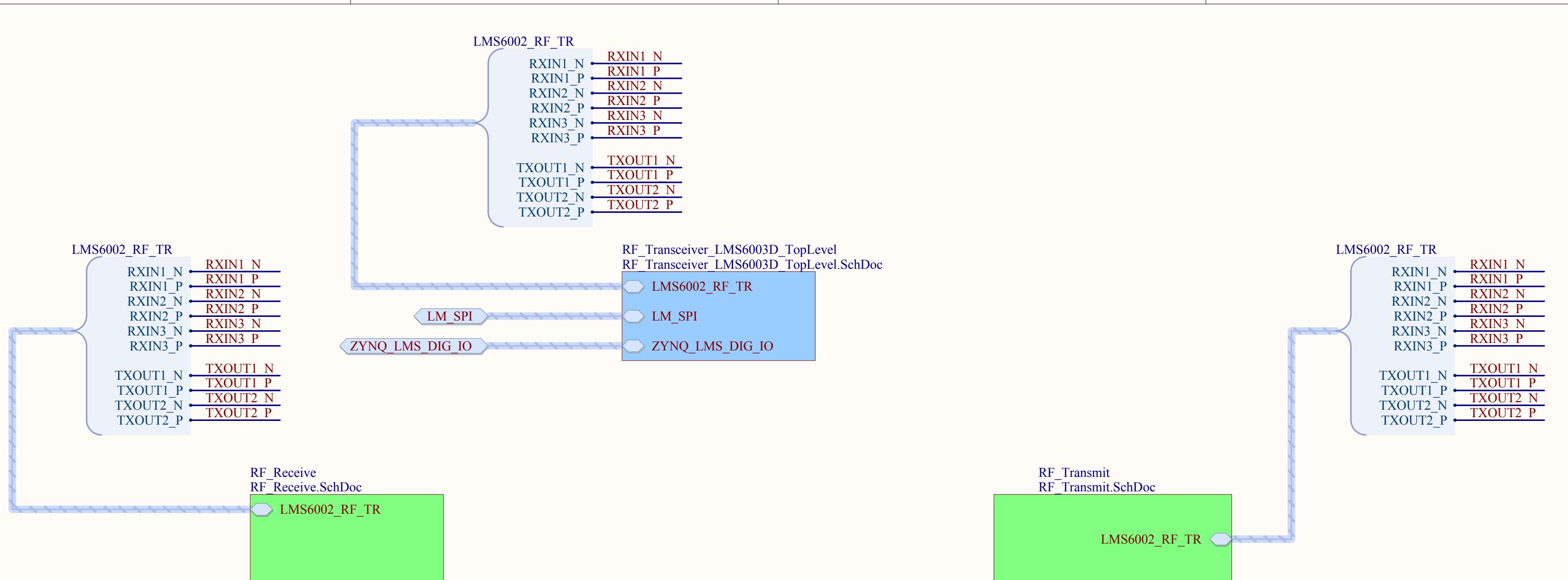
C



D

D

Title		
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\RF Transceiver LMS6003D	TopLevel.SchDoc



Title

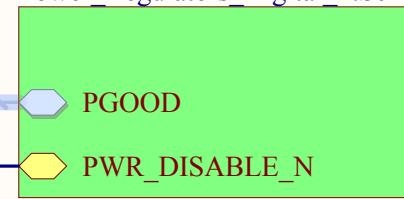
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\..\RF TOP LEVEL.SchDoc	Drawn By:

A

PowerSwitch
PowerSwitch.SchDoc



Power_Regulators_Digital_1
Power_Regulators_Digital_1.SchDoc



Power_Regulators_Digital_2
Power_Regulators_Digital_2.SchDoc



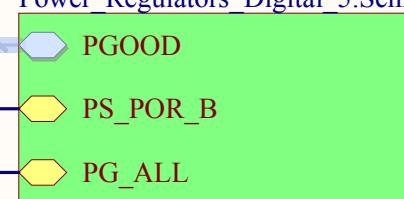
Power_Regulators_Digital_3
Power_Regulators_Digital_3.SchDoc



Power_Regulators_Digital_4
Power_Regulators_Digital_4.SchDoc

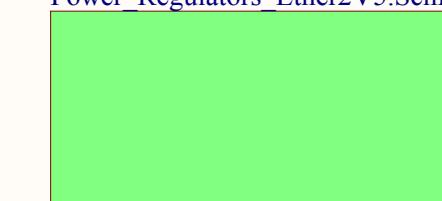


Power_Regulators_Digital_5
Power_Regulators_Digital_5.SchDoc

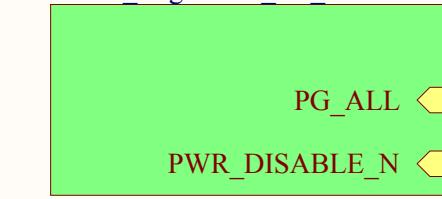


PS POR B

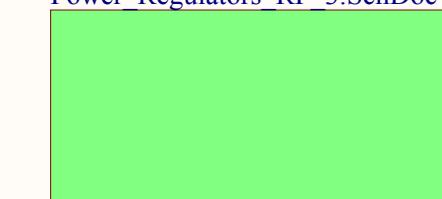
Power_Regulators_Ether2V5
Power_Regulators_Ether2V5.SchDoc



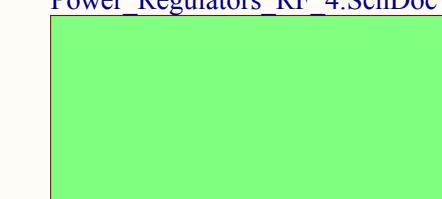
Power_Regulators_RF_2
Power_Regulators_RF_2.SchDoc



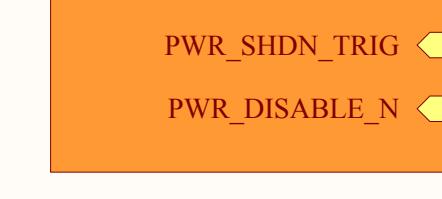
Power_Regulators_RF_3
Power_Regulators_RF_3.SchDoc



Power_Regulators_RF_4
Power_Regulators_RF_4.SchDoc



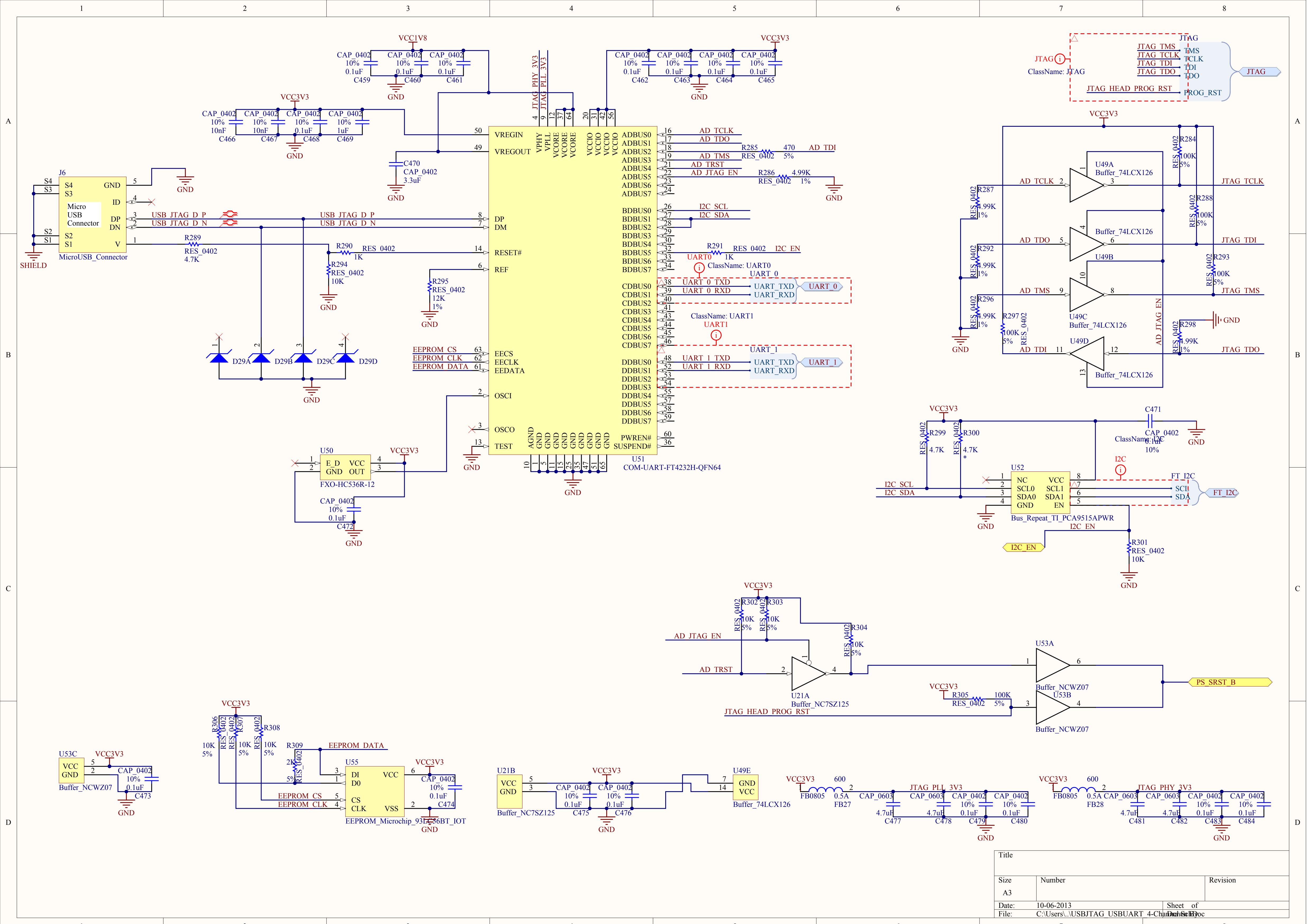
Shundown_Mechanism
Shundown_Mechanism.SchDoc

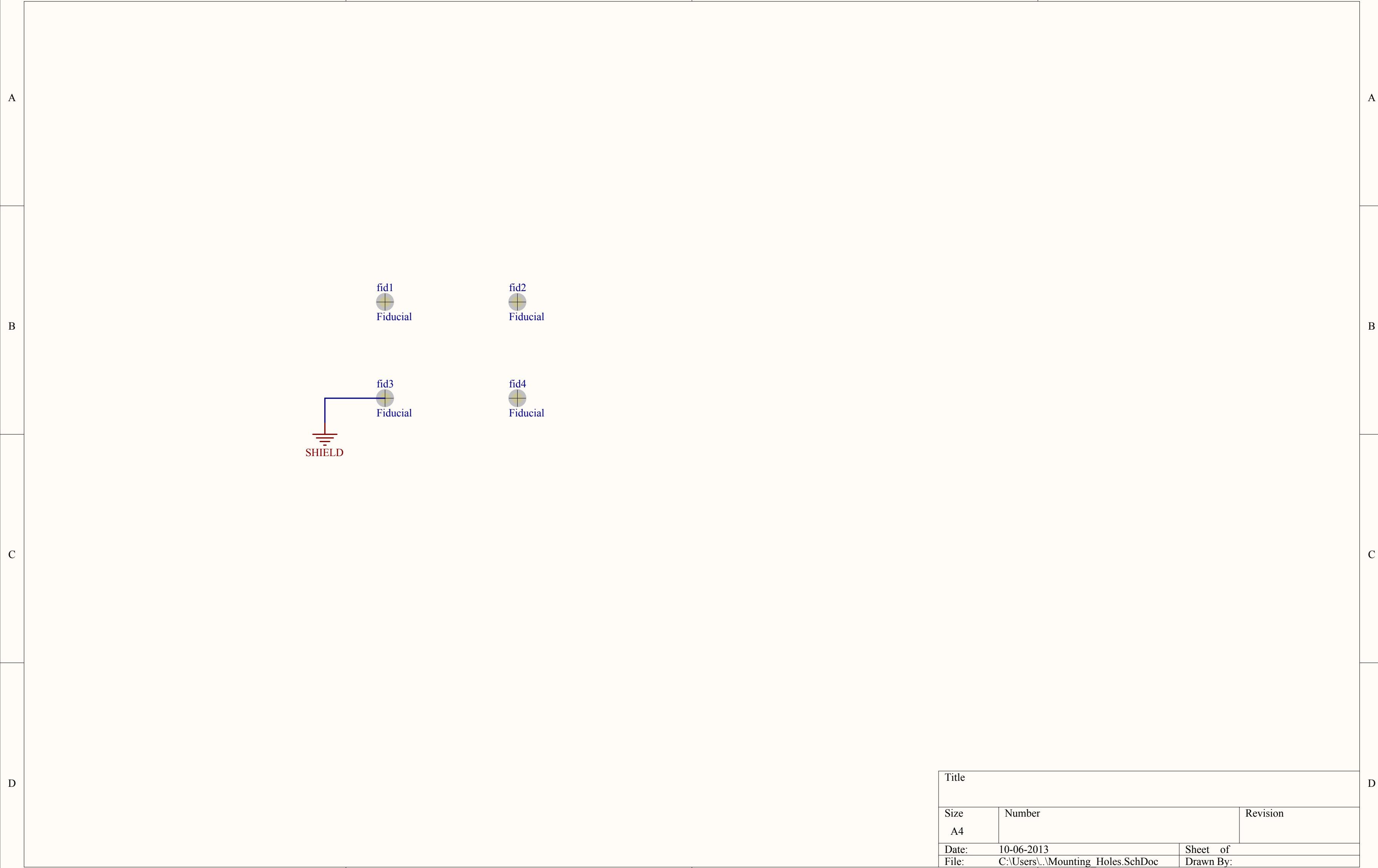


PWR SHDN TRIG

Title

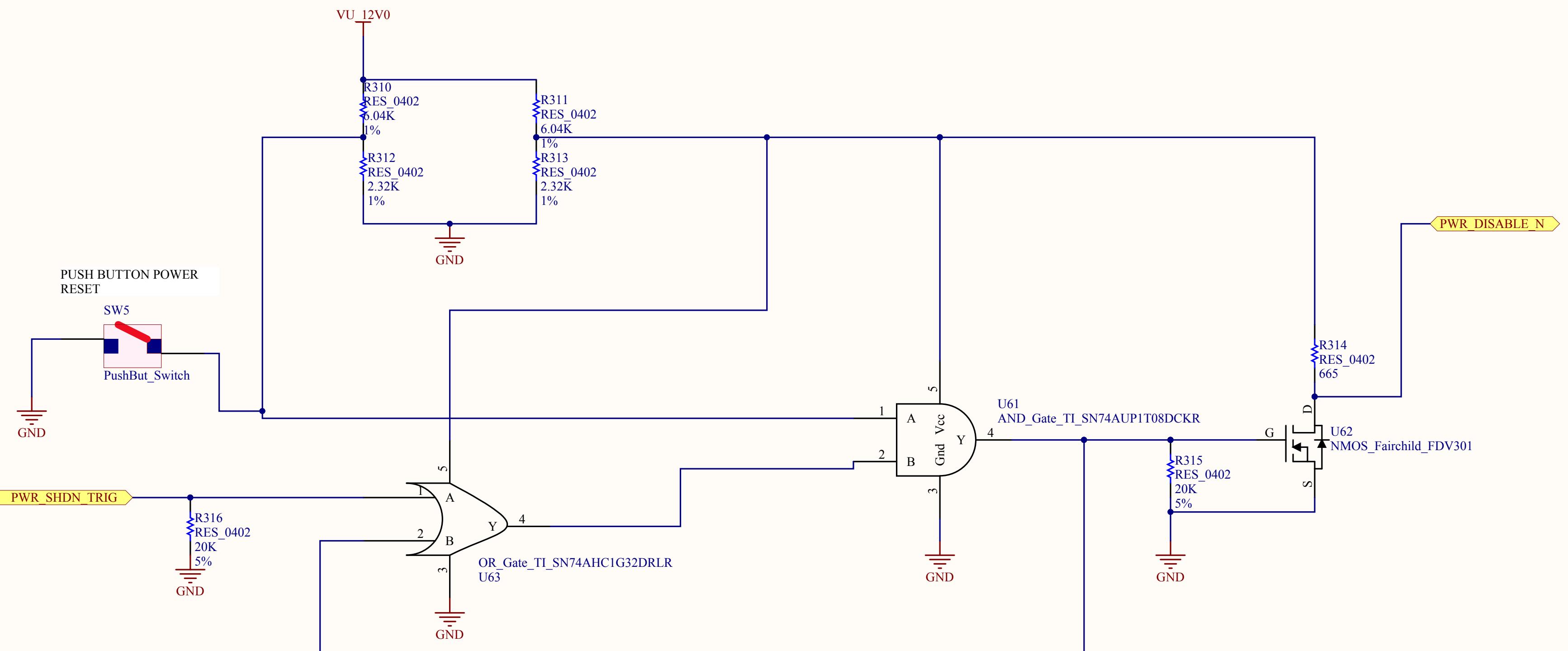
Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Power Distribution TopLevel.SchDoc	SheetBy:





A

A

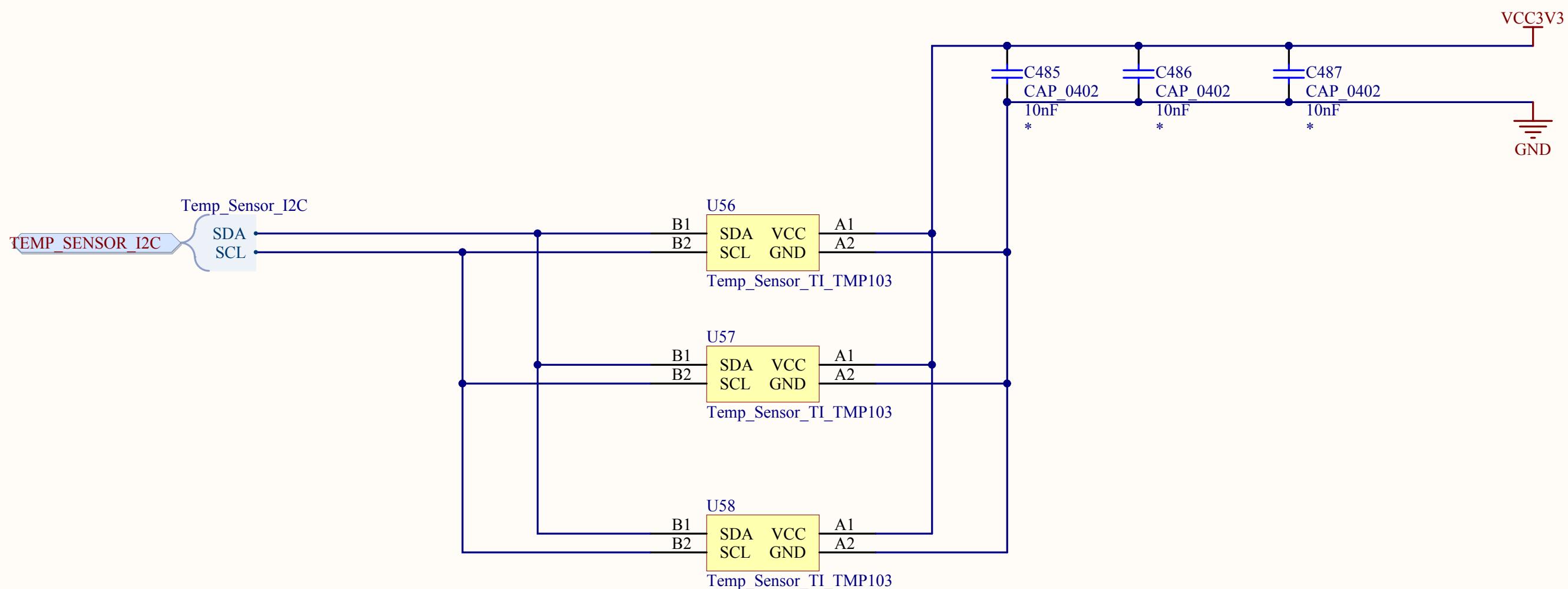


Title

Size	Number	Revision
A4		
Date:	10-06-2013	Sheet of
File:	C:\Users\.\Shutdown Mechanism.SchDoc	Drawn By:

A

A



B

B

C

C

D

D

Title		
Size	Number	Revision
A4		
Date: 10-06-2013	Sheet of	
File: C:\Users\.\Temperature Sensors.SchDoc		Drawn By: