# 1. Description

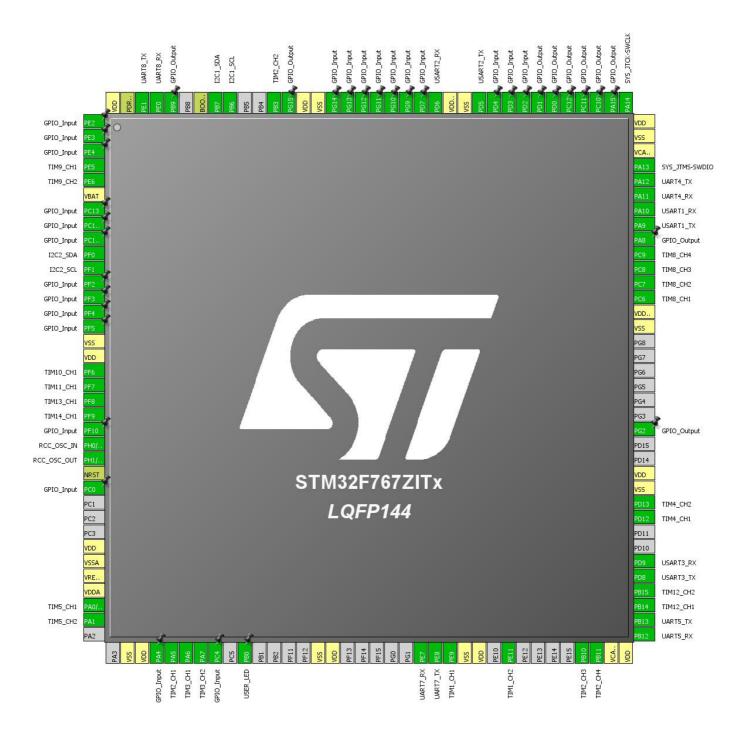
## 1.1. Project

Project Name	F767_Hermit_main
Board Name	F767_Hermit_main
Generated with:	STM32CubeMX 4.23.0
Date	03/23/2018

## 1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

## 2. Pinout Configuration



# 3. Pins Configuration

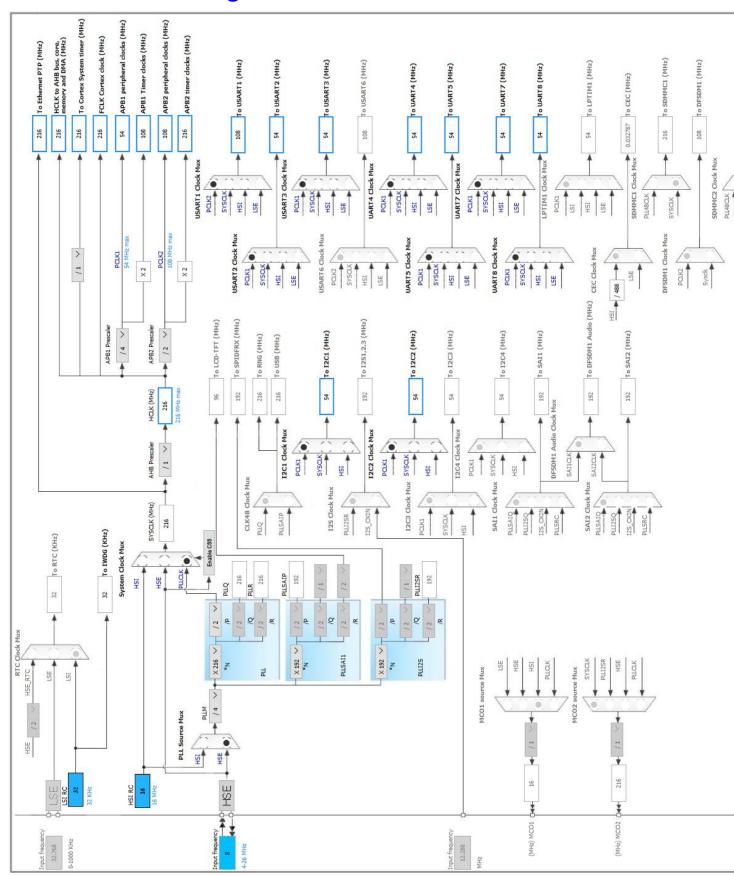
Pin Number LQFP144         Pin Name (function after reset)         Pin Type         Alternate Function(s)         Labe           1         PE2 *         I/O         GPIO_Input           2         PE3 *         I/O         GPIO_Input           3         PE4 *         I/O         GPIO_Input           4         PE5         I/O         TIM9_CH1           5         PE6         I/O         TIM9_CH2           6         VBAT         Power           7         PC13 *         I/O         GPIO_Input           8         PC14/OSC32_IN *         I/O         GPIO_Input           9         PC15/OSC32_OUT *         I/O         GPIO_Input           10         PF0         I/O         I2C2_SDA           11         PF1         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
Teset	
1 PE2 * I/O GPIO_Input 2 PE3 * I/O GPIO_Input 3 PE4 * I/O GPIO_Input 4 PE5 I/O TIM9_CH1 5 PE6 I/O TIM9_CH2 6 VBAT Power 7 PC13 * I/O GPIO_Input 8 PC14/OSC32_IN * I/O GPIO_Input 9 PC15/OSC32_OUT * I/O GPIO_Input 10 PF0 I/O I2C2_SDA 11 PF1 I/O GPIO_Input 13 PF3 * I/O GPIO_Input 14 PF4 * I/O GPIO_Input 15 PF5 * I/O GPIO_Input 16 VSS Power 17 VDD Power	
2 PE3 * I/O GPIO_Input  3 PE4 * I/O GPIO_Input  4 PE5 I/O TIM9_CH1  5 PE6 I/O TIM9_CH2  6 VBAT Power  7 PC13 * I/O GPIO_Input  8 PC14/OSC32_IN * I/O GPIO_Input  9 PC15/OSC32_OUT * I/O GPIO_Input  10 PF0 I/O I2C2_SDA  11 PF1 I/O I2C2_SCL  12 PF2 * I/O GPIO_Input  13 PF3 * I/O GPIO_Input  14 PF4 * I/O GPIO_Input  15 PF5 * I/O GPIO_Input  16 VSS Power  17 VDD Power  18 PF6 I/O TIM10_CH1	
3 PE4 * I/O GPIO_Input  4 PE5 I/O TIM9_CH1  5 PE6 I/O TIM9_CH2  6 VBAT Power  7 PC13 * I/O GPIO_Input  8 PC14/OSC32_IN * I/O GPIO_Input  9 PC15/OSC32_OUT * I/O GPIO_Input  10 PF0 I/O I2C2_SDA  11 PF1 I/O I2C2_SCL  12 PF2 * I/O GPIO_Input  13 PF3 * I/O GPIO_Input  14 PF4 * I/O GPIO_Input  15 PF5 * I/O GPIO_Input  16 VSS Power  17 VDD Power  18 PF6 I/O TIM10_CH1	
4         PE5         I/O         TIM9_CH1           5         PE6         I/O         TIM9_CH2           6         VBAT         Power           7         PC13 *         I/O         GPIO_Input           8         PC14/OSC32_IN *         I/O         GPIO_Input           9         PC15/OSC32_OUT *         I/O         GPIO_Input           10         PF0         I/O         I2C2_SDA           11         PF1         I/O         GPIO_Input           12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
5         PE6         I/O         TIM9_CH2           6         VBAT         Power           7         PC13 *         I/O         GPIO_Input           8         PC14/OSC32_IN *         I/O         GPIO_Input           9         PC15/OSC32_OUT *         I/O         GPIO_Input           10         PF0         I/O         I2C2_SDA           11         PF1         I/O         I2C2_SCL           12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
6         VBAT         Power           7         PC13 *         I/O         GPIO_Input           8         PC14/OSC32_IN *         I/O         GPIO_Input           9         PC15/OSC32_OUT *         I/O         GPIO_Input           10         PF0         I/O         I2C2_SDA           11         PF1         I/O         I2C2_SCL           12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
7 PC13 * I/O GPIO_Input  8 PC14/OSC32_IN * I/O GPIO_Input  9 PC15/OSC32_OUT * I/O GPIO_Input  10 PF0 I/O I2C2_SDA  11 PF1 I/O I2C2_SCL  12 PF2 * I/O GPIO_Input  13 PF3 * I/O GPIO_Input  14 PF4 * I/O GPIO_Input  15 PF5 * I/O GPIO_Input  16 VSS Power  17 VDD Power  18 PF6 I/O TIM10_CH1	
8         PC14/OSC32_IN *         I/O         GPIO_Input           9         PC15/OSC32_OUT *         I/O         GPIO_Input           10         PF0         I/O         I2C2_SDA           11         PF1         I/O         I2C2_SCL           12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
9 PC15/OSC32_OUT * I/O GPIO_Input  10 PF0 I/O I2C2_SDA  11 PF1 I/O I2C2_SCL  12 PF2 * I/O GPIO_Input  13 PF3 * I/O GPIO_Input  14 PF4 * I/O GPIO_Input  15 PF5 * I/O GPIO_Input  16 VSS Power  17 VDD Power  18 PF6 I/O TIM10_CH1	
10         PF0         I/O         I2C2_SDA           11         PF1         I/O         I2C2_SCL           12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
11         PF1         I/O         I2C2_SCL           12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
12         PF2 *         I/O         GPIO_Input           13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
13         PF3 *         I/O         GPIO_Input           14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
14         PF4 *         I/O         GPIO_Input           15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
15         PF5 *         I/O         GPIO_Input           16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
16         VSS         Power           17         VDD         Power           18         PF6         I/O         TIM10_CH1	
17         VDD         Power           18         PF6         I/O         TIM10_CH1	
18 PF6 I/O TIM10_CH1	
10 DE7 1/O TIM11 CH1	
19 PF7 I/O TIM11_CH1 20 PF8 I/O TIM13_CH1	
22         PF10 *         I/O         GPIO_Input           23         PH0/OSC_IN         I/O         RCC_OSC_IN	
24 PH1/OSC_OUT I/O RCC_OSC_OUT	
25 NRST Reset	
26 PC0 * I/O GPIO_Input	
30 VDD Power	
31 VSSA Power	
32 VREF+ Power	
33 VDDA Power	
34 PA0/WKUP I/O TIM5_CH1	
35 PA1 I/O TIM5_CH2	
35 PAT 1/O TIMIS_CH2  38 VSS Power	
39 VDD Power	
40 PA4 * I/O GPIO_Input	
41 PA5 I/O TIM2_CH1	

Pin Number LQFP144	Pin Name (function after	Pin Type	Alternate Function(s)	Label
LQII ITT	reset)		r unotion(s)	
42	PA6	I/O	TIM3_CH1	
43	PA7	1/0	TIM3_CH2	
44	PC4 *	1/0	GPIO_Input	
46	PB0 *	1/0	GPIO_Output	USER_LED
51	VSS	Power	01 10_Output	OOLK_LLD
52	VDD	Power		
58	PE7	I/O	UART7_RX	
59	PE8	I/O	UART7_TX	
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	
69	PB10	I/O	TIM2_CH3	
70	PB11	I/O	TIM2_CH4	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	UART5_RX	
74	PB13	I/O	UART5_TX	
75	PB14	I/O	TIM12_CH1	
76	PB15	I/O	TIM12_CH2	
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Output	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	TIM8_CH2	
98	PC8	I/O	TIM8_CH3	
99	PC9	I/O	TIM8_CH4	
100	PA8 *	I/O	GPIO_Output	
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	UART4_RX	
104	PA12	I/O	UART4_TX	
105	PA13	I/O	SYS_JTMS-SWDIO	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15 *	I/O	GPIO_Output	
111	PC10 *	I/O	GPIO_Output	
112	PC11 *	I/O	GPIO_Output	
113	PC12 *	I/O	GPIO_Output	
114	PD0 *	I/O	GPIO_Output	
115	PD1 *	I/O	GPIO_Output	
116	PD2 *	I/O	GPIO_Input	
117	PD3 *	I/O	GPIO_Input	
118	PD4 *	I/O	GPIO_Input	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6	I/O	USART2_RX	
123	PD7 *	I/O	GPIO_Input	
124	PG9 *	I/O	GPIO_Input	
125	PG10 *	I/O	GPIO_Input	
126	PG11 *	I/O	GPIO_Input	
127	PG12 *	I/O	GPIO_Input	
128	PG13 *	I/O	GPIO_Input	
129	PG14 *	I/O	GPIO_Input	
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	
133	PB3	I/O	TIM2_CH2	
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	воото	Boot		
140	PB9 *	I/O	GPIO_Output	
141	PE0	I/O	UART8_RX	
142	PE1	I/O	UART8_TX	
143	PDR_ON	Reset		
144	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

## 5.1. I2C1

12C: 12C

## 5.1.1. Parameter Settings:

## **Timing configuration:**

Standard Mode I2C Speed Mode

100 I2C Speed Frequency (KHz) Rise Time (ns) 300 \* Fall Time (ns) 0 Coefficient of Digital Filter Enabled Analog Filter

Timing 0x10E06996 \*

## **Slave Features:**

Clock No Stretch Mode Disabled General Call Address Detection Disabled Primary Address Length selection 7-bit **Dual Address Acknowledged** Disabled Primary slave address

## 5.2. I2C2

12C: 12C

## 5.2.1. Parameter Settings:

## Timing configuration:

I2C Speed Mode Standard Mode

100 I2C Speed Frequency (KHz) Rise Time (ns) 300 \* 0 Fall Time (ns) Coefficient of Digital Filter 0 Analog Filter Enabled

Timing 0x10E06996 \*

### **Slave Features:**

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

## 5.3. IWDG

mode: Activated

## 5.3.1. Parameter Settings:

### **Watchdog Clocking:**

IWDG counter clock prescalerIWDG window valueIWDG down-counter reload value4095

## 5.4. RCC

## High Speed Clock (HSE): Crystal/Ceramic Resonator

## 5.4.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3

Flash Latency(WS) 7 WS (8 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Over Drive Enabled

Power Regulatror Voltage Scale Power Regulator Voltage Scale 1

## 5.5. SYS

**Debug: Serial Wire** 

Timebase Source: SysTick

## 5.6. TIM1

**Combined Channels: Encoder Mode** 

## 5.6.1. Parameter Settings:

## **Counter Settings:**

Prescaler (PSC - 16 bits value)	1300 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	60000 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable
Trigger Output (TRGO) Parameters:	
Master/Slave Mode	Disable (no

Disable (no sync between this TIM (Master) and its Slaves Master/Slave Mode

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR) Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### **Encoder:**

**Encoder Mode Encoder Mode TI1** \_\_\_\_ Parameters for Channel 1 \_\_\_\_ Polarity Falling Edge \* IC Selection Direct Prescaler Division Ratio No division Input Filter 2 \* Parameters for Channel 2 \_\_\_\_ Polarity Falling Edge \*

Direct IC Selection Prescaler Division Ratio No division

Input Filter 2 \*

## 5.7. TIM2

**Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3** 

#### **Channel4: PWM Generation CH4**

## 5.7.1. Parameter Settings:

### **Counter Settings:**

Prescaler (PSC - 16 bits value) 5 \*

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 999 \*

Internal Clock Division (CKD) No Division auto-reload preload Disable

### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

**PWM Generation Channel 1:** 

Mode PWM mode 1

Pulse (32 bits value) 0
Fast Mode Disable
CH Polarity High

**PWM Generation Channel 2:** 

Mode PWM mode 1

Pulse (32 bits value) 0
Fast Mode Disable
CH Polarity High

**PWM Generation Channel 3:** 

Mode PWM mode 1

Pulse (32 bits value) 0
Fast Mode Disable
CH Polarity High

**PWM Generation Channel 4:** 

Mode PWM mode 1

Pulse (32 bits value) 0
Fast Mode Disable
CH Polarity High

## 5.8. TIM3

**Combined Channels: Encoder Mode** 

## 5.8.1. Parameter Settings:

Counter Settings:			
Prescaler (PSC - 16 bits value)	1300 *		
Counter Mode	Up		
Counter Period (AutoReload Register - 16 bits value )	60000 *		
Internal Clock Division (CKD)	No Division		
auto-reload preload	Disable		
Trigger Output (TRGO) Parameters:			
Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves		
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)		
Encoder:			
Encoder Mode	Encoder Mode TI1		
Parameters for Channel 1			
Polarity	Falling Edge *		
IC Selection	Direct		
Prescaler Division Ratio	No division		
Input Filter	2 *		
Parameters for Channel 2			
Polarity	Falling Edge *		
IC Selection	Direct		
Prescaler Division Ratio	No division		

2 \*

## 5.9. TIM4

Input Filter

**Combined Channels: Encoder Mode** 

## 5.9.1. Parameter Settings:

## **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 60000 \*

Internal Clock Division (CKD) No Division auto-reload preload Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

1300 \*

Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Encoder:	
Encoder Mode	Encoder Mode TI1
Parameters for Channel 1	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
Parameters for Channel 2	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
5.10. TIM5	
	J_
Combined Channels: Encoder Mod	ue .
5.10.1. Parameter Settings:	
Counter Settings:	
Prescaler (PSC - 16 bits value)	1500 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	60000 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Trigger Output (TRGO) Parameters:	
Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Encoder:	
Encoder Mode	Encoder Mode TI1
Parameters for Channel 1	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
Parameters for Channel 2	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter 0

## 5.11. TIM6

mode: Activated

## 5.11.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 432 \*
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value ) 50000-1 \*
auto-reload preload Disable

## **Trigger Output (TRGO) Parameters:**

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

## 5.12. TIM8

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

## 5.12.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

10 \*

Up

999 \*

Repetition Counter (RCR - 16 bits value) 0

auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

**BRK Sources Configuration** 

- Digital Input- DFSDMDisable

#### **Break And Dead Time management - BRK2 Configuration:**

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

**BRK2 Sources Configuration** 

- Digital Input- DFSDMDisable

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High
CH Idle State Reset

#### **PWM Generation Channel 2:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High
CH Idle State Reset

#### **PWM Generation Channel 3:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High
CH Idle State Reset

#### **PWM Generation Channel 4:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High
CH Idle State Reset

## 5.13. TIM9

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

## 5.13.1. Parameter Settings:

## **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

A32 \*

Up

No Division

Disable

## **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

#### **PWM Generation Channel 2:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

## 5.14. TIM10

mode: Activated

**Channel1: PWM Generation CH1** 

## 5.14.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

A32 \*

Up

No Division

Disable

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

## 5.15. TIM11

mode: Activated

**Channel1: PWM Generation CH1** 

### 5.15.1. Parameter Settings:

### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

A32 \*

Up

No Division

Disable

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

#### 5.16. TIM12

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

## 5.16.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

216 \*

Up

No Division

Disable

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

**PWM Generation Channel 2:** 

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

## 5.17. TIM13

mode: Activated

**Channel1: PWM Generation CH1** 

## 5.17.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

Disable

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

## 5.18. TIM14

mode: Activated

**Channel1: PWM Generation CH1** 

## 5.18.1. Parameter Settings:

### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

216 \*

Up

No Division

Disable

**PWM Generation Channel 1:** 

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

## 5.19. UART4

**Mode: Asynchronous** 

## 5.19.1. Parameter Settings:

## **Basic Parameters:**

Baud Rate 115200

Word Length 9 Bits (including Parity) \*

Parity Even \*
Stop Bits 1

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Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

## 5.20. UART5

## **Mode: Asynchronous**

## 5.20.1. Parameter Settings:

**Basic Parameters:** 

Baud Rate 115200

Word Length 9 Bits (including Parity) \*

Parity Even \*

Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun Enable DMA on RX Error MSB First Disable

## 5.21. UART7

**Mode: Asynchronous** 

## 5.21.1. Parameter Settings:

**Basic Parameters:** 

Baud Rate 9600 \*

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

## 5.22. UART8

**Mode: Asynchronous** 

## 5.22.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

## 5.23. USART1

**Mode: Asynchronous** 

## 5.23.1. Parameter Settings:

**Basic Parameters:** 

Baud Rate 115200

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable Disable TX Pin Active Level Inversion RX Pin Active Level Inversion Disable Disable **Data Inversion** TX and RX Pins Swapping Disable Overrun Enable DMA on RX Error Enable MSB First Disable

## 5.24. USART2

**Mode: Asynchronous** 

## 5.24.1. Parameter Settings:

**Basic Parameters:** 

Baud Rate 115200

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable
TX Pin Active Level Inversion Disable

RX Pin Active Level Inversion Disable
Data Inversion Disable
TX and RX Pins Swapping Disable
Overrun Enable
DMA on RX Error Enable
MSB First Disable

## 5.25. USART3

**Mode: Asynchronous** 

## 5.25.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Data Inversion Disable TX and RX Pins Swapping Disable Overrun Enable DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 6. System Configuration

## 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	Very High	
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	Very High *	
RCC	PH0/OSC_I N	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0/WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	TIM9_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM10	PF6	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM11	PF7	TIM11_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM13	PF8	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM14	PF9	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PA11	UART4_RX	Alternate Function Push Pull	Pull-up	Very High	
	PA12	UART4_TX	Alternate Function Push Pull	Pull-up	Very High	
UART5	PB12	UART5_RX	Alternate Function Push Pull	Pull-up	Very High	
	PB13	UART5_TX	Alternate Function Push Pull	Pull-up	Very High	
UART7	PE7	UART7_RX	Alternate Function Push Pull	Pull-up	Very High	
	PE8	UART7_TX	Alternate Function Push Pull	Pull-up	Very High	
UART8	PE0	UART8_RX	Alternate Function Push Pull	Pull-up	Very High	
	PE1	UART8_TX	Alternate Function Push Pull	Pull-up	Very High	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	Very High	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	Very High	
USART2	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	Very High	
	PD6	USART2_RX	Alternate Function Push Pull	Pull-up	Very High	
USART3	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	Very High	
	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	Very High	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PC14/OSC3 2_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC15/OSC3 2_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

## 6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	Medium *

## USART1\_RX: DMA2\_Stream2 DMA request Settings:

Mode: Circular \*

Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*

Peripheral Data Width: Byte
Memory Data Width: Byte

## 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	2	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	3	0
DMA2 stream2 global interrupt	true	1	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt		unused	
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt		unused	
TIM8 trigger and commutation interrupts and TIM14 global interrupt		unused	
TIM8 capture compare interrupt		unused	
TIM5 global interrupt		unused	
UART4 global interrupt	unused		
UART5 global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
FPU global interrupt		unused	
UART7 global interrupt	unused		
UART8 global interrupt	unused		

<sup>\*</sup> User modified value

# 7. Power Consumption Calculator report

## 7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
мси	STM32F767ZITx
Datasheet	029041_Rev4

#### 7.2. Parameter Selection

Temperature	25
Vdd	3.3

# 8. Software Project

## 8.1. Project Settings

Name	Value
Project Name	F767_Hermit_main
Project Folder	C:\Users\ryouma\OneDrive\\18\\F767_Hermit_main
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F7 V1.8.0

## 8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	