1. Description

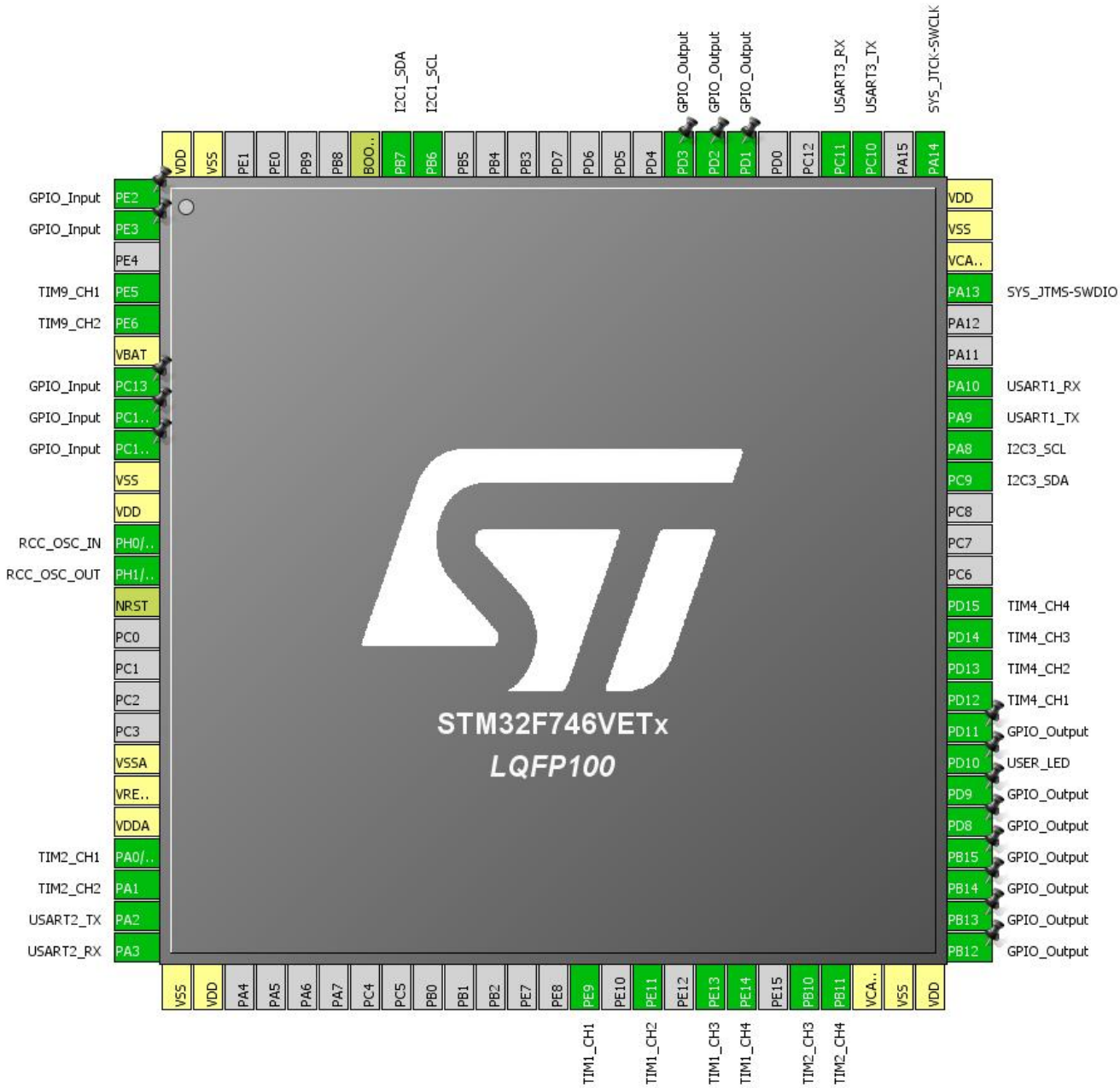
1.1. Project

Project Name	F746_Elk_main
Board Name	F746_Elk_main
Generated with:	STM32CubeMX 4.23.0
Date	03/23/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



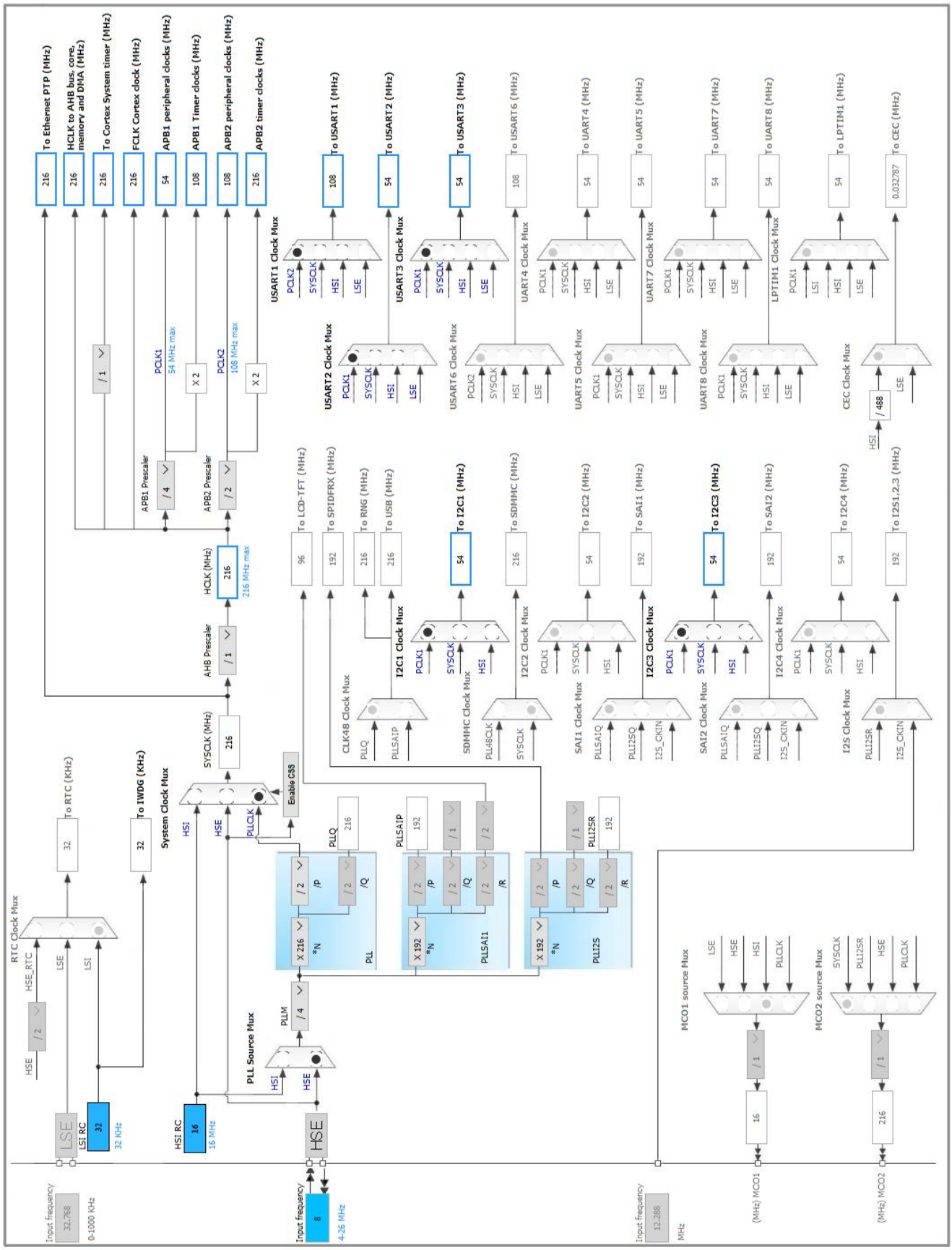
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	
2	PE3 *	I/O	GPIO_Input	
4	PE5	I/O	TIM9_CH1	
5	PE6	I/O	TIM9_CH2	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	
8	PC14/OSC32_IN *	I/O	GPIO_Input	
9	PC15/OSC32_OUT *	I/O	GPIO_Input	
10	VSS	Power		
11	VDD	Power		
12	PH0/OSC_IN	I/O	RCC_OSC_IN	
13	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
22	PA0/WKUP	I/O	TIM2_CH1	
23	PA1	I/O	TIM2_CH2	
24	PA2	I/O	USART2_TX	
25	PA3	I/O	USART2_RX	
26	VSS	Power		
27	VDD	Power		
39	PE9	I/O	TIM1_CH1	
41	PE11	I/O	TIM1_CH2	
43	PE13	I/O	TIM1_CH3	
44	PE14	I/O	TIM1_CH4	
46	PB10	I/O	TIM2_CH3	
47	PB11	I/O	TIM2_CH4	
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	
52	PB13 *	I/O	GPIO_Output	
53	PB14 *	I/O	GPIO_Output	
54	PB15 *	I/O	GPIO_Output	
55	PD8 *	I/O	GPIO_Output	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
56	PD9 *	I/O	GPIO_Output	
57	PD10 *	I/O	GPIO_Output	USER_LED
58	PD11 *	I/O	GPIO_Output	
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
61	PD14	I/O	TIM4_CH3	
62	PD15	I/O	TIM4_CH4	
66	PC9	I/O	I2C3_SDA	
67	PA8	I/O	I2C3_SCL	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
82	PD1 *	I/O	GPIO_Output	
83	PD2 *	I/O	GPIO_Output	
84	PD3 *	I/O	GPIO_Output	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. I2C1

I2C: I2C

5.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**1000 ***
Fall Time (ns)	**300 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x40D32A31 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.2. I2C3

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**1000 ***
Fall Time (ns)	**300 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x40D32A31 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. IWDG

mode: Activated

5.3.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**32 ***
IWDG window value	4095
IWDG down-counter reload value	4095

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.5. SYS

Debug: Serial Wire
Timebase Source: SysTick

5.6. TIM1

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**15 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable

CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.7. TIM2

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.8. TIM4

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.9. TIM6

mode: Activated

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**432 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**50000-1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.10. TIM9

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.11. USART1

Mode: Asynchronous

5.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.12. USART2

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.13. USART3

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	TIM9_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART3	PC10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PC11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC14/OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC15/OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	**Medium ***

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	2	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	3	0
DMA2 stream2 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746VETx
Datasheet	027590_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	F746_Elk_main
Project Folder	C:\Users\ryouma\OneDrive\\18\\F746_Elk_main
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F7 V1.8.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No