1. Description

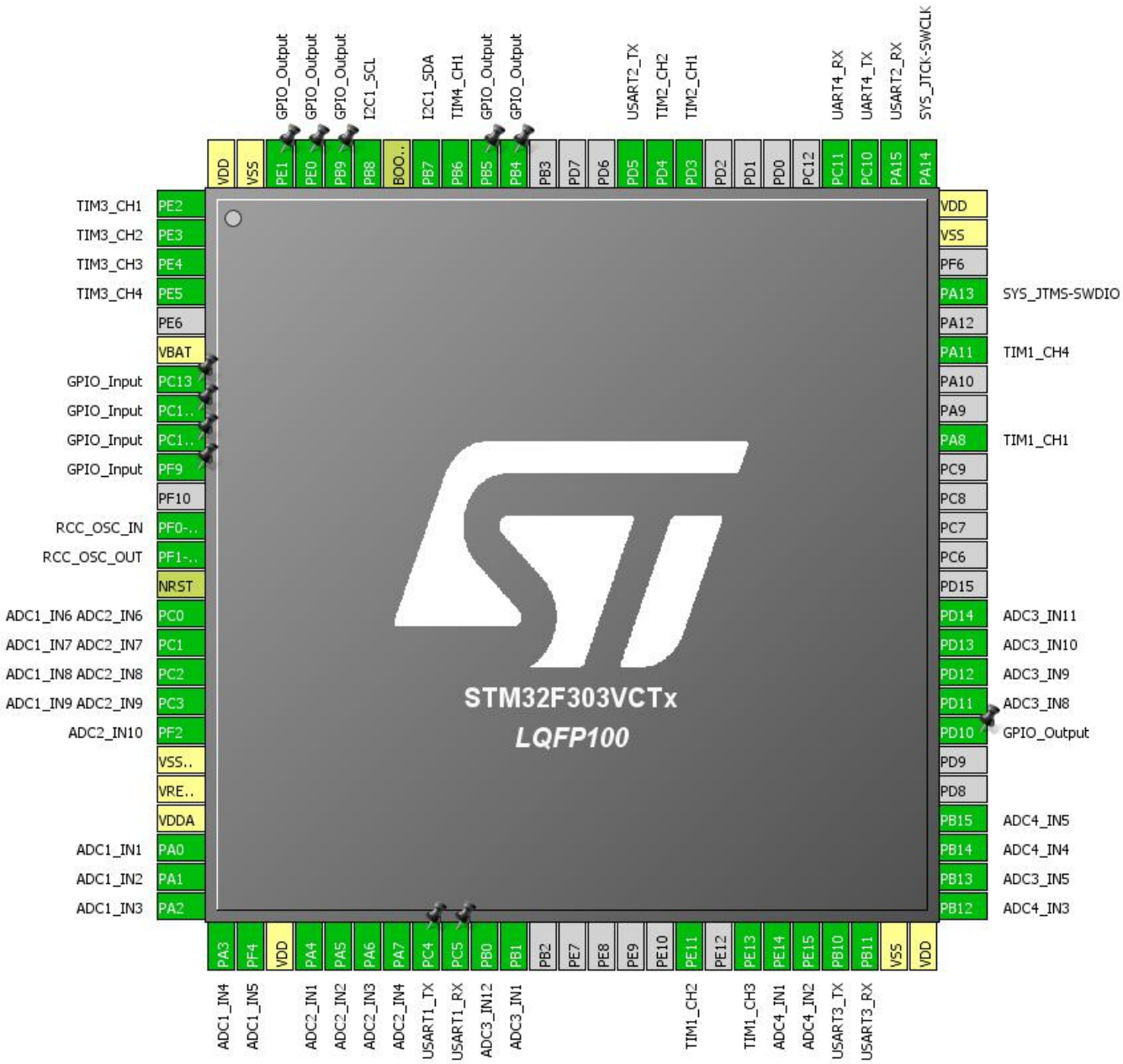
1.1. Project

Project Name	F303VCT6_main
Board Name	custom
Generated with:	STM32CubeMX 4.27.0
Date	02/28/2019

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



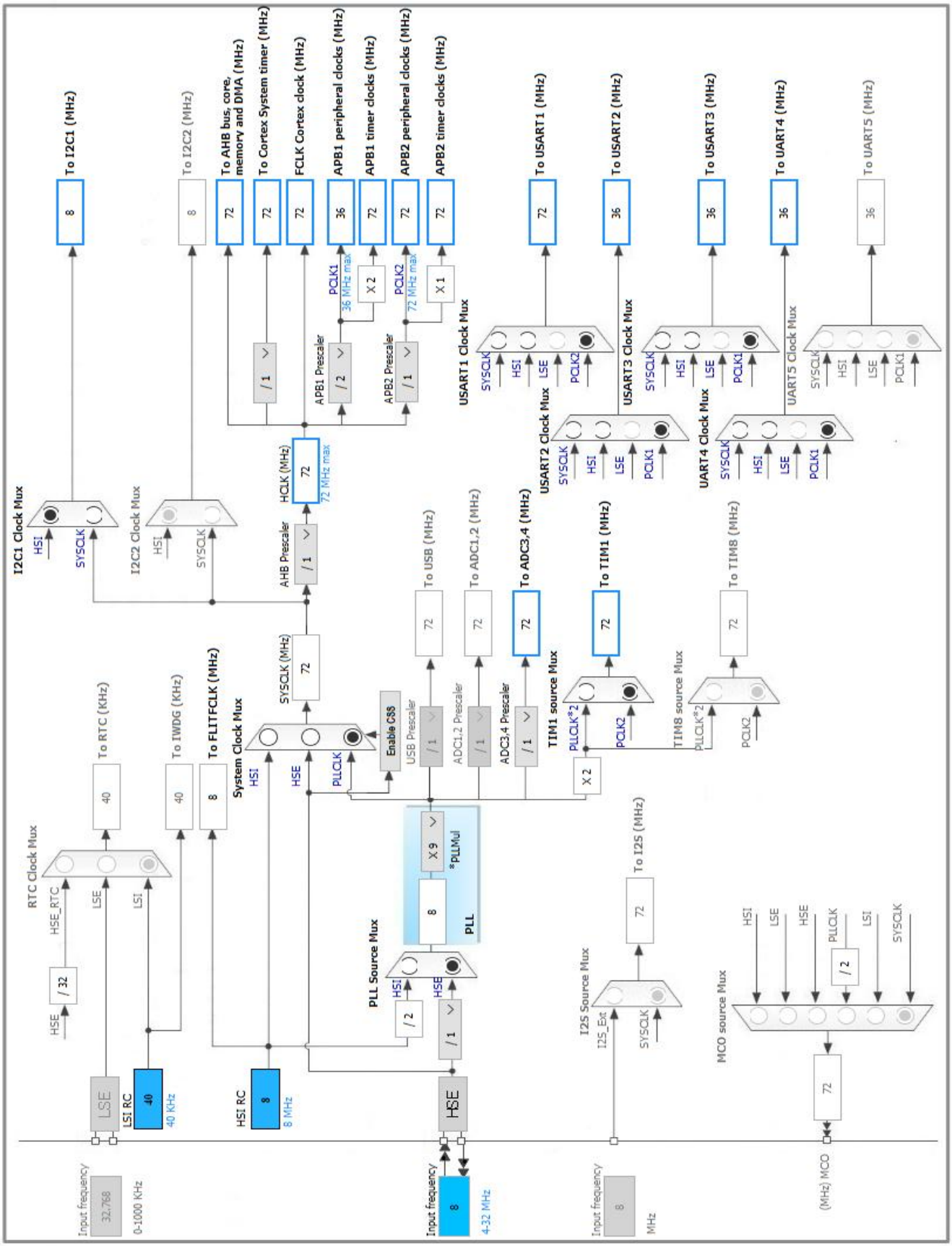
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	TIM3_CH1	
2	PE3	I/O	TIM3_CH2	
3	PE4	I/O	TIM3_CH3	
4	PE5	I/O	TIM3_CH4	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	
8	PC14-OSC32_IN *	I/O	GPIO_Input	
9	PC15-OSC32_OUT *	I/O	GPIO_Input	
10	PF9 *	I/O	GPIO_Input	
12	PF0-OSC_IN	I/O	RCC_OSC_IN	
13	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_IN6, ADC2_IN6	
16	PC1	I/O	ADC1_IN7, ADC2_IN7	
17	PC2	I/O	ADC1_IN8, ADC2_IN8	
18	PC3	I/O	ADC1_IN9, ADC2_IN9	
19	PF2	I/O	ADC2_IN10	
20	VSSA/VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0	I/O	ADC1_IN1	
24	PA1	I/O	ADC1_IN2	
25	PA2	I/O	ADC1_IN3	
26	PA3	I/O	ADC1_IN4	
27	PF4	I/O	ADC1_IN5	
28	VDD	Power		
29	PA4	I/O	ADC2_IN1	
30	PA5	I/O	ADC2_IN2	
31	PA6	I/O	ADC2_IN3	
32	PA7	I/O	ADC2_IN4	
33	PC4	I/O	USART1_TX	
34	PC5	I/O	USART1_RX	
35	PB0	I/O	ADC3_IN12	
36	PB1	I/O	ADC3_IN1	
42	PE11	I/O	TIM1_CH2	
44	PE13	I/O	TIM1_CH3	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PE14	I/O	ADC4_IN1	
46	PE15	I/O	ADC4_IN2	
47	PB10	I/O	USART3_TX	
48	PB11	I/O	USART3_RX	
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	ADC4_IN3	
52	PB13	I/O	ADC3_IN5	
53	PB14	I/O	ADC4_IN4	
54	PB15	I/O	ADC4_IN5	
57	PD10 *	I/O	GPIO_Output	
58	PD11	I/O	ADC3_IN8	
59	PD12	I/O	ADC3_IN9	
60	PD13	I/O	ADC3_IN10	
61	PD14	I/O	ADC3_IN11	
67	PA8	I/O	TIM1_CH1	
70	PA11	I/O	TIM1_CH4	
72	PA13	I/O	SYS_JTMS-SWDIO	
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	USART2_RX	
78	PC10	I/O	UART4_TX	
79	PC11	I/O	UART4_RX	
84	PD3	I/O	TIM2_CH1	
85	PD4	I/O	TIM2_CH2	
86	PD5	I/O	USART2_TX	
90	PB4 *	I/O	GPIO_Output	
91	PB5 *	I/O	GPIO_Output	
92	PB6	I/O	TIM4_CH1	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9 *	I/O	GPIO_Output	
97	PE0 *	I/O	GPIO_Output	
98	PE1 *	I/O	GPIO_Output	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

IN6: IN6 Single-ended

IN7: IN7 Single-ended

IN8: IN8 Single-ended

IN9: IN9 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**9 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***

Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 5 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 6 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	**Channel 7 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**8 ***
Channel	**Channel 8 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**9 ***
Channel	**Channel 9 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN6: IN6 Single-ended

IN7: IN7 Single-ended

IN8: IN8 Single-ended

IN9: IN9 Single-ended

IN10: IN10 Single-ended

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable

Number Of Conversion	**9 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 6 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 7 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	**Channel 8 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**8 ***

Channel	**Channel 9 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**9 ***
Channel	**Channel 10 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.3. ADC3

IN1: IN1 Single-ended

IN5: IN5 Single-ended

IN8: IN8 Single-ended

IN9: IN9 Single-ended

IN10: IN10 Single-ended

IN11: IN11 Single-ended

IN12: IN12 Single-ended

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***

Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**7 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 5 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 8 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 9 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 10 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 11 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset

Offset	0
Rank	**7 ***
Channel	**Channel 12 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.4. ADC4

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

5.4.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**5 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 5 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.5. I2C1

I2C: I2C

5.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**300 ***
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00401D2A ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.7. SYS

Debug: Serial Wire
Timebase Source: SysTick

5.8. TIM1

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**8 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.9. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.10. TIM3

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.11. TIM4

Channel1: PWM Generation CH1

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.12. TIM6

mode: Activated

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**36 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.13. UART4

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.14. USART1

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.15. USART2

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First	Disable

5.16. USART3

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN6	Analog mode	No pull up pull down	n/a	
	PC1	ADC1_IN7	Analog mode	No pull up pull down	n/a	
	PC2	ADC1_IN8	Analog mode	No pull up pull down	n/a	
	PC3	ADC1_IN9	Analog mode	No pull up pull down	n/a	
	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	
	PA2	ADC1_IN3	Analog mode	No pull up pull down	n/a	
	PA3	ADC1_IN4	Analog mode	No pull up pull down	n/a	
	PF4	ADC1_IN5	Analog mode	No pull up pull down	n/a	
ADC2	PC0	ADC2_IN6	Analog mode	No pull up pull down	n/a	
	PC1	ADC2_IN7	Analog mode	No pull up pull down	n/a	
	PC2	ADC2_IN8	Analog mode	No pull up pull down	n/a	
	PC3	ADC2_IN9	Analog mode	No pull up pull down	n/a	
	PF2	ADC2_IN10	Analog mode	No pull up pull down	n/a	
	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	
	PA5	ADC2_IN2	Analog mode	No pull up pull down	n/a	
	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	
	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	
ADC3	PB0	ADC3_IN12	Analog mode	No pull up pull down	n/a	
	PB1	ADC3_IN1	Analog mode	No pull up pull down	n/a	
	PB13	ADC3_IN5	Analog mode	No pull up pull down	n/a	
	PD11	ADC3_IN8	Analog mode	No pull up pull down	n/a	
	PD12	ADC3_IN9	Analog mode	No pull up pull down	n/a	
	PD13	ADC3_IN10	Analog mode	No pull up pull down	n/a	
	PD14	ADC3_IN11	Analog mode	No pull up pull down	n/a	
ADC4	PE14	ADC4_IN1	Analog mode	No pull up pull down	n/a	
	PE15	ADC4_IN2	Analog mode	No pull up pull down	n/a	
	PB12	ADC4_IN3	Analog mode	No pull up pull down	n/a	
	PB14	ADC4_IN4	Analog mode	No pull up pull down	n/a	
	PB15	ADC4_IN5	Analog mode	No pull up pull down	n/a	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_OUT					
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE11	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull up pull down	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull up pull down	Low	
TIM2	PD3	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PD4	TIM2_CH2	Alternate Function Push Pull	No pull up pull down	Low	
TIM3	PE2	TIM3_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PE3	TIM3_CH2	Alternate Function Push Pull	No pull up pull down	Low	
	PE4	TIM3_CH3	Alternate Function Push Pull	No pull up pull down	Low	
	PE5	TIM3_CH4	Alternate Function Push Pull	No pull up pull down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull up pull down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PC11	UART4_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
USART1	PC4	USART1_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PC5	USART1_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
USART2	PA15	USART2_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PD5	USART2_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
GPIO	PC13	GPIO_Input	Input mode	No pull up pull down	n/a	
	PC14-OSC32_IN	GPIO_Input	Input mode	No pull up pull down	n/a	
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull up pull down	n/a	
	PF9	GPIO_Input	Input mode	No pull up pull down	n/a	
	PD10	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB4	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PE0	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull up pull down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
ADC2	DMA2_Channel3	Peripheral To Memory	Low
ADC3	DMA2_Channel5	Peripheral To Memory	Low
ADC4	DMA2_Channel4	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC4: DMA2_Channel4 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word

Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	4	0
Timer 6 interrupt and DAC underrun interrupts	true	5	0
DMA2 channel3 global interrupt	true	1	0
DMA2 channel4 global interrupt	true	0	0
DMA2 channel5 global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
ADC3 global interrupt	unused		
UART4 global interrupt / UART4 wake-up interrupt through EXTI line 34	unused		
ADC4 interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303VCTx
Datasheet	023353_Rev13

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	F303VCT6_main
Project Folder	I:\\\\F303VCT6_main
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report