1. Description

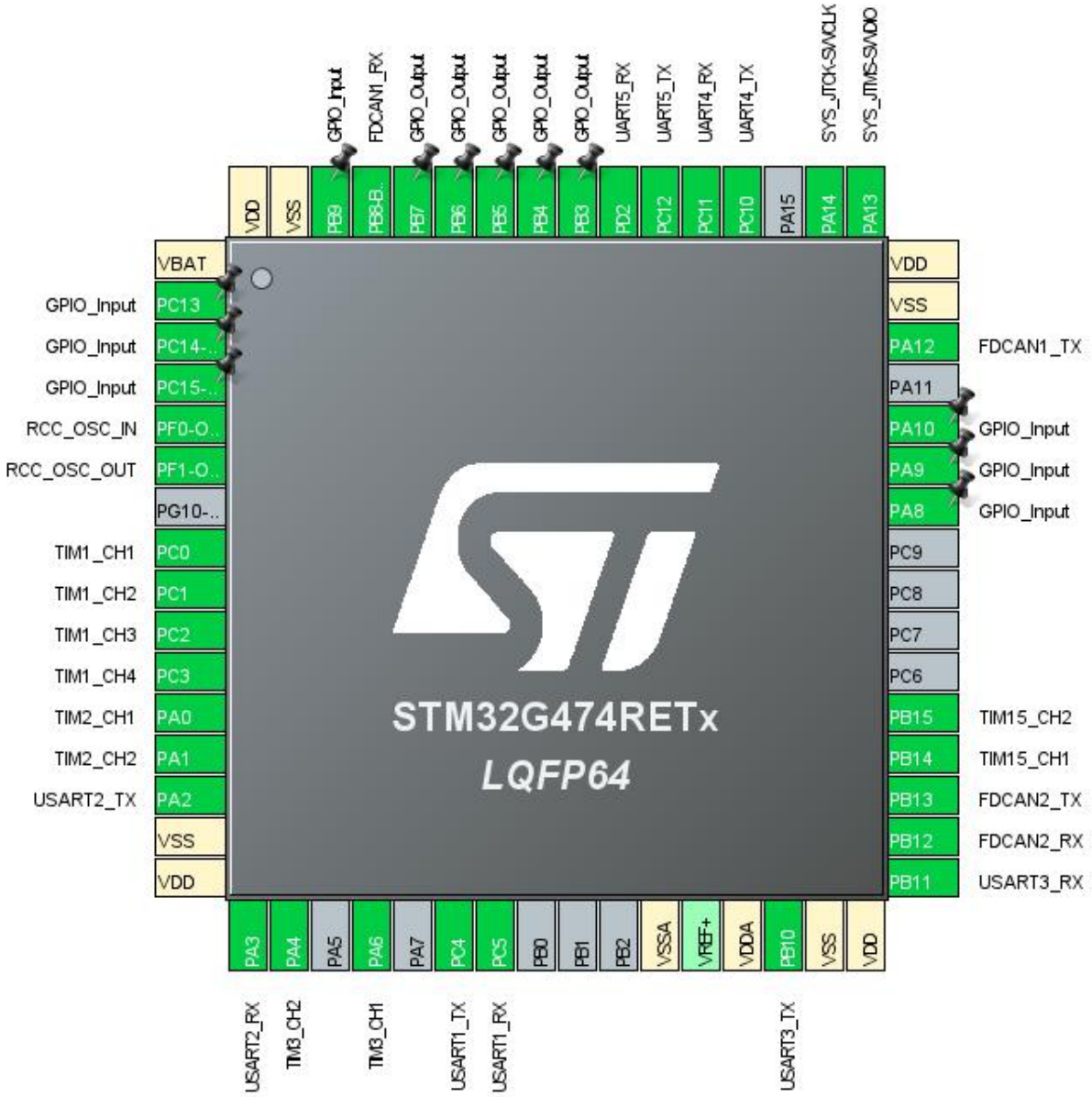
1.1. Project

Project Name	G474_Saramander_Sentry
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	01/17/2020

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



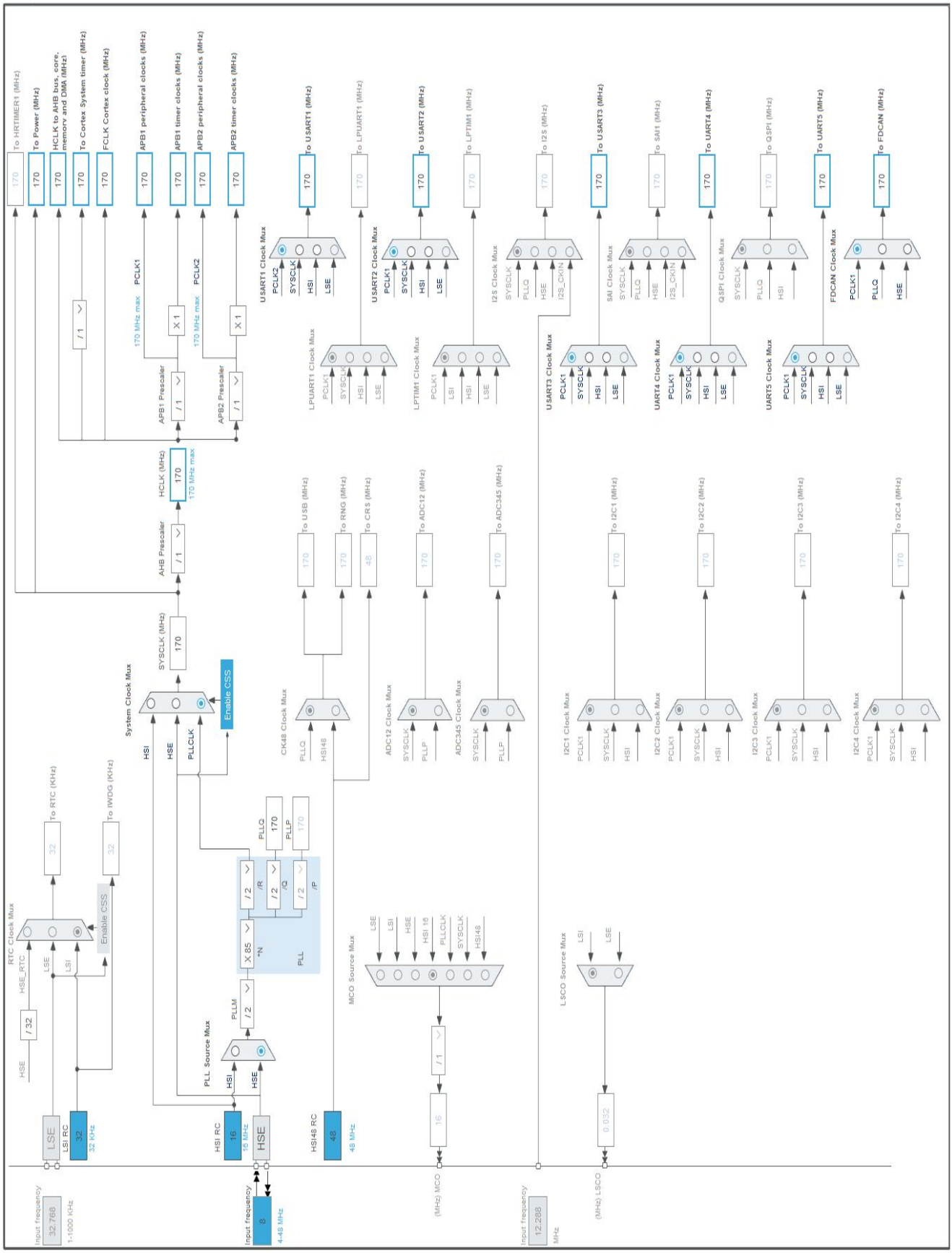
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Input	
3	PC14-OSC32_IN *	I/O	GPIO_Input	
4	PC15-OSC32_OUT *	I/O	GPIO_Input	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
8	PC0	I/O	TIM1_CH1	
9	PC1	I/O	TIM1_CH2	
10	PC2	I/O	TIM1_CH3	
11	PC3	I/O	TIM1_CH4	
12	PA0	I/O	TIM2_CH1	
13	PA1	I/O	TIM2_CH2	
14	PA2	I/O	USART2_TX	
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	USART2_RX	
18	PA4	I/O	TIM3_CH2	
20	PA6	I/O	TIM3_CH1	
22	PC4	I/O	USART1_TX	
23	PC5	I/O	USART1_RX	
27	VSSA	Power		
29	VDDA	Power		
30	PB10	I/O	USART3_TX	
31	VSS	Power		
32	VDD	Power		
33	PB11	I/O	USART3_RX	
34	PB12	I/O	FDCAN2_RX	
35	PB13	I/O	FDCAN2_TX	
36	PB14	I/O	TIM15_CH1	
37	PB15	I/O	TIM15_CH2	
42	PA8 *	I/O	GPIO_Input	
43	PA9 *	I/O	GPIO_Input	
44	PA10 *	I/O	GPIO_Input	
46	PA12	I/O	FDCAN1_TX	
47	VSS	Power		
48	VDD	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	PA13	I/O	SYS_JTMS-SWDIO	
50	PA14	I/O	SYS_JTCK-SWCLK	
52	PC10	I/O	UART4_TX	
53	PC11	I/O	UART4_RX	
54	PC12	I/O	UART5_TX	
55	PD2	I/O	UART5_RX	
56	PB3 *	I/O	GPIO_Output	
57	PB4 *	I/O	GPIO_Output	
58	PB5 *	I/O	GPIO_Output	
59	PB6 *	I/O	GPIO_Output	
60	PB7 *	I/O	GPIO_Output	
61	PB8-BOOT0	I/O	FDCAN1_RX	
62	PB9 *	I/O	GPIO_Input	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	G474_Saramander_Sentry
Project Folder	C:\Users\ryouma\Documents\GitHub\RoboMaster_Salamander_okadatech\G474
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.1.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474RETx
Datasheet	DS12288_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. FDCAN1

Mode: Classic Master

7.1.1. Parameter Settings:

Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

7.2. FDCAN2

Mode: Classic Slave

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2

Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

7.3. GPIO

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	8WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.6. TIM1

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable

- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM2

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Encoder:

Encoder Mode	Encoder Mode TI1
Slave Mode Preload Activation	Disable
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.8. TIM3

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Encoder:

Encoder Mode	Encoder Mode TI1
Slave Mode Preload Activation	Disable
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.9. TIM15

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.10. UART4

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. UART5

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable

Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. USART1

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. USART2

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.14. USART3

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FDCAN1	PA12	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8-BOOT0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PC0	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC1	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC2	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC3	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA4	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM15	PB14	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PC4	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC14-OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
UART4 global interrupt / UART4 wake-up interrupt through EXTI line 34	unused		
UART5 global interrupt / UART5 wake-up interrupt through EXTI line 35	unused		
FPU global interrupt	unused		
FDCAN2 interrupt 0	unused		
FDCAN2 interrupt 1	unused		

*** User modified value**

9. Software Pack Report