1. Description

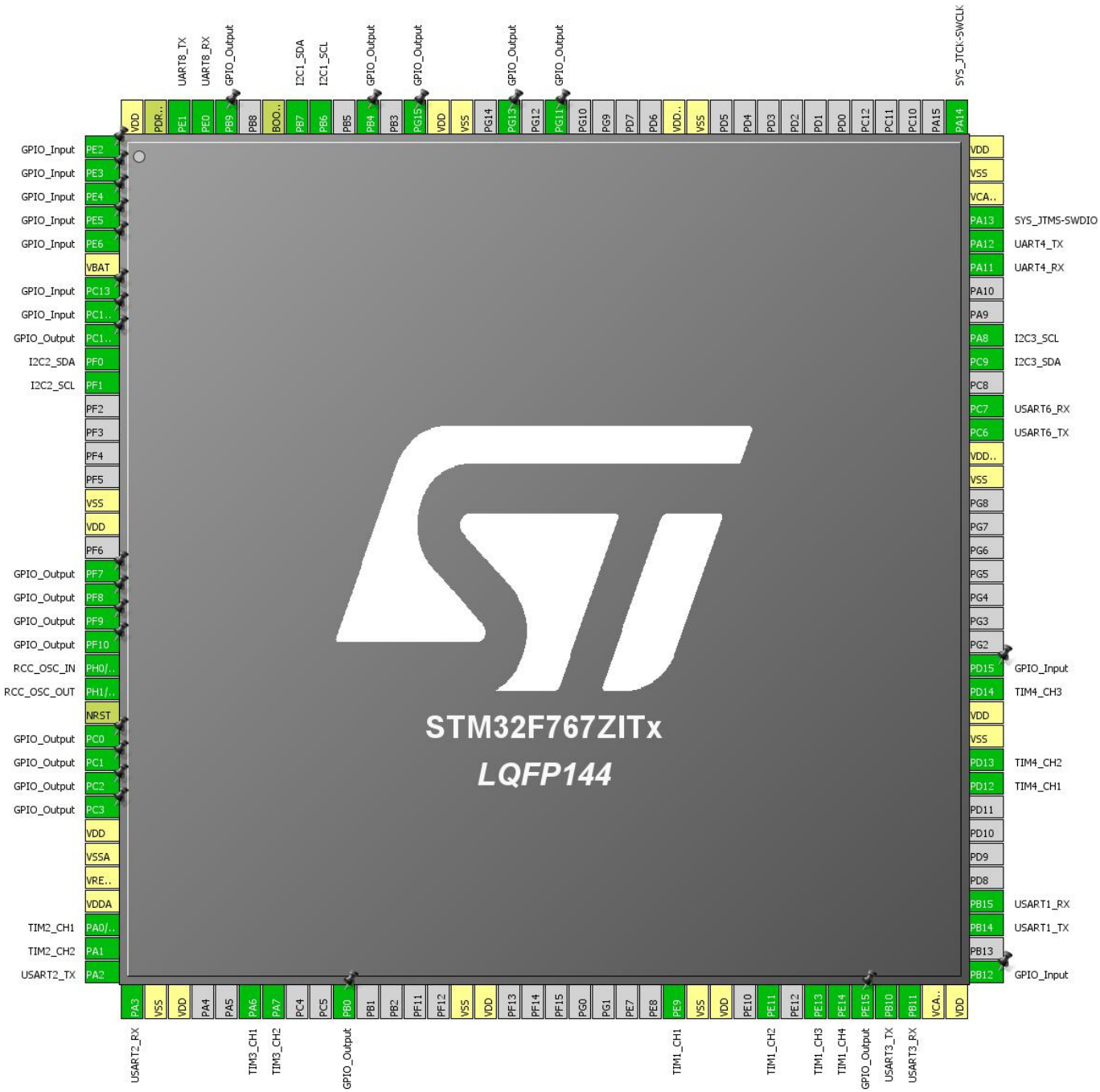
1.1. Project

Project Name	F767_main
Board Name	F767_main
Generated with:	STM32CubeMX 4.23.0
Date	03/06/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

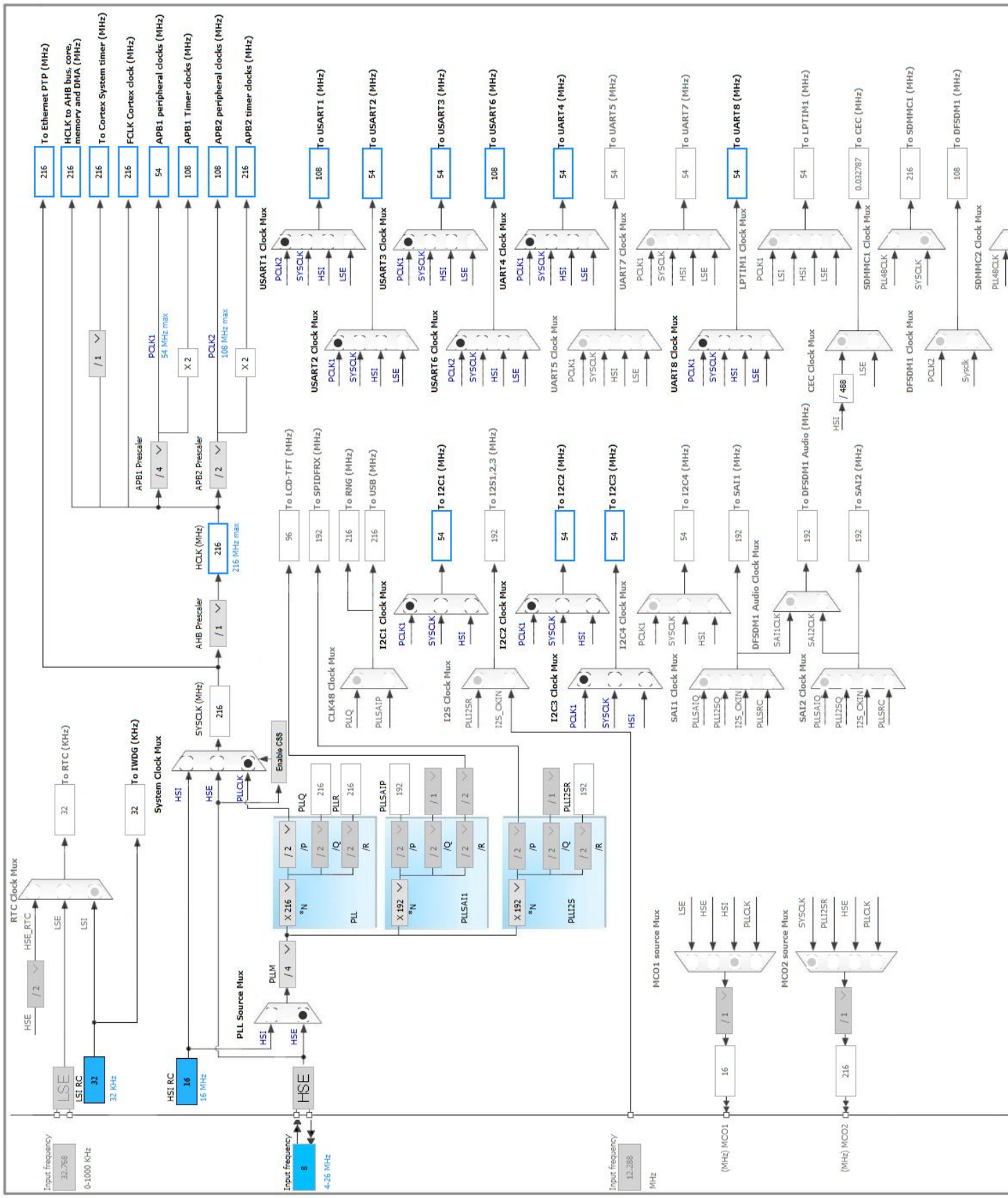
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	
2	PE3 *	I/O	GPIO_Input	
3	PE4 *	I/O	GPIO_Input	
4	PE5 *	I/O	GPIO_Input	
5	PE6 *	I/O	GPIO_Input	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	
8	PC14/OSC32_IN *	I/O	GPIO_Input	
9	PC15/OSC32_OUT *	I/O	GPIO_Output	
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
19	PF7 *	I/O	GPIO_Output	
20	PF8 *	I/O	GPIO_Output	
21	PF9 *	I/O	GPIO_Output	
22	PF10 *	I/O	GPIO_Output	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	
27	PC1 *	I/O	GPIO_Output	
28	PC2 *	I/O	GPIO_Output	
29	PC3 *	I/O	GPIO_Output	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM2_CH1	
35	PA1	I/O	TIM2_CH2	
36	PA2	I/O	USART2_TX	
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
42	PA6	I/O	TIM3_CH1	
43	PA7	I/O	TIM3_CH2	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
46	PB0 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	
66	PE13	I/O	TIM1_CH3	
67	PE14	I/O	TIM1_CH4	
68	PE15 *	I/O	GPIO_Output	
69	PB10	I/O	USART3_TX	
70	PB11	I/O	USART3_RX	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Input	
75	PB14	I/O	USART1_TX	
76	PB15	I/O	USART1_RX	
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	TIM4_CH3	
86	PD15 *	I/O	GPIO_Input	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
99	PC9	I/O	I2C3_SDA	
100	PA8	I/O	I2C3_SCL	
103	PA11	I/O	UART4_RX	
104	PA12	I/O	UART4_TX	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
120	VSS	Power		
121	VDDSDMMC	Power		
126	PG11 *	I/O	GPIO_Output	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
128	PG13 *	I/O	GPIO_Output	
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	
134	PB4 *	I/O	GPIO_Output	
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
140	PB9 *	I/O	GPIO_Output	
141	PE0	I/O	UART8_RX	
142	PE1	I/O	UART8_TX	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. I2C1

I2C: I2C

5.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**1000 ***
Fall Time (ns)	**300 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x40D32A31 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.2. I2C2

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**1000 ***
Fall Time (ns)	**300 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x40D32A31 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. I2C3

I2C: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**1000 ***
Fall Time (ns)	**300 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x40D32A31 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. IWDG

mode: Activated

5.4.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**64 ***
IWDG window value	4095
IWDG down-counter reload value	4095

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.7. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: Output Compare CH4

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**21 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division

Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

Output Compare Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.8. TIM2

Combined Channels: Encoder Mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**60000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.9. TIM3

Combined Channels: Encoder Mode

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**7 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**2 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**2 ***

5.10. TIM4

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**108 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.11. TIM6

mode: Activated

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**215 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.12. UART4

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.13. UART8

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.14. USART1

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.15. USART2

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.16. USART3

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable

DMA on RX Error	Enable
MSB First	Disable

5.17. USART6

Mode: Asynchronous

5.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PA11	UART4_RX	Alternate Function Push Pull	Pull-up	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA12	UART4_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
UART8	PE0	UART8_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PE1	UART8_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART1	PB14	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PB15	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC14/OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC15/OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
UART4_RX	DMA1_Stream2	Peripheral To Memory	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low

UART4_RX: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream1 global interrupt	true	3	0
DMA1 stream2 global interrupt	true	2	0
DMA1 stream5 global interrupt	true	1	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	4	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
UART4 global interrupt	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
UART8 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

7.3. Sequence

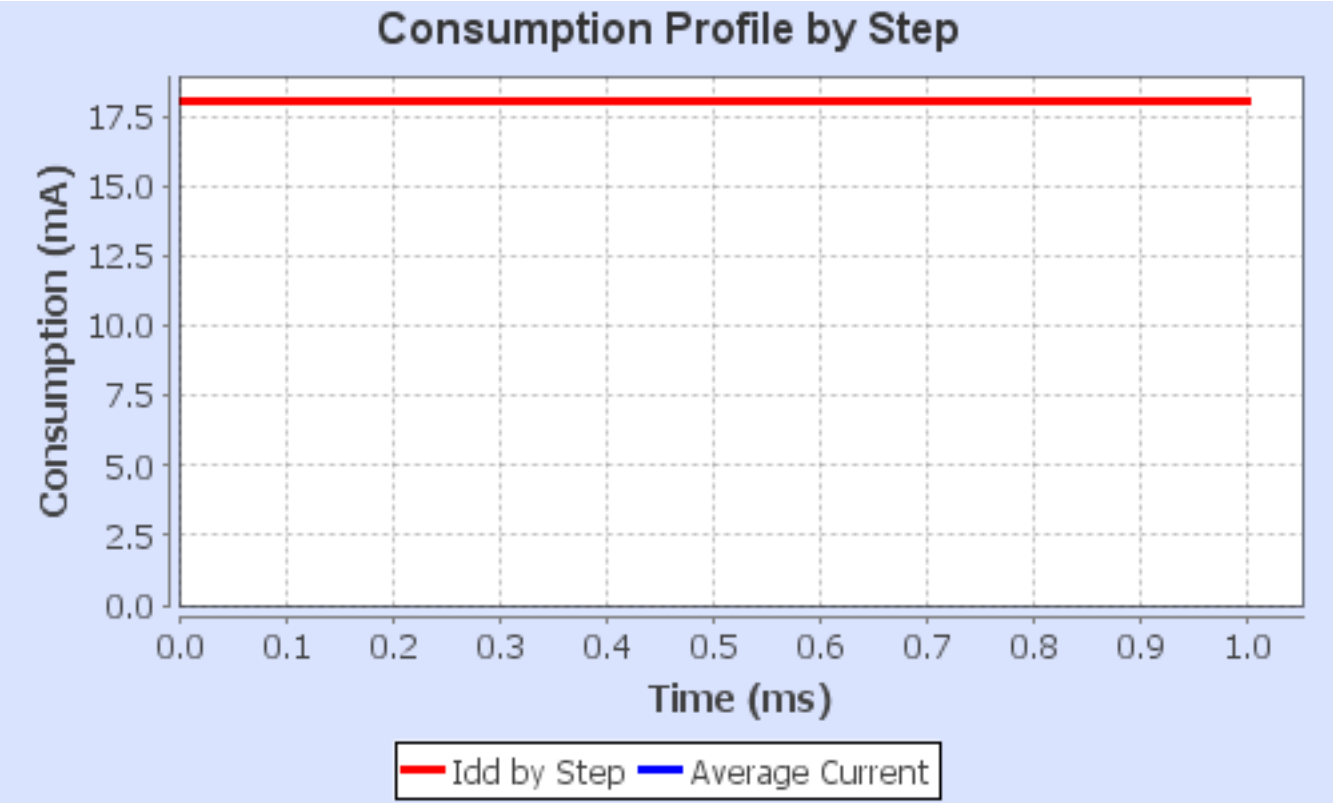
Step	Step1
Mode	SLEEP
Vdd	3.3
Voltage Source	Vbus
Range	Scale1-High
Fetch Type	RAM/FLASH REGON
Clock Configuration	HSE PLL
Clock Source Frequency	4 MHz
CPU Frequency	216 MHz
Peripherals	
Additional Cons.	0 mA
Average Current	18 mA
Duration	1 ms
DMIPS	462.24002
Ta Max	102.62
Category	In DS Table

7.4. RESULTS

Sequence Time	1 ms	Average Current	18 mA

Battery Life	0	Average DMIPS	462.24 DMIPS

7.5. Chart



8. Software Project

8.1. Project Settings

Name	Value
Project Name	F767_main
Project Folder	G:\\\Atolic_HAL\F767_main
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F7 V1.8.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No