Onur Kayıran

CONTACT INFORMATION

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Penn State University
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RESEARCH INTERESTS

Computer Architecture, GPU Architectures, CPU-GPU Heterogeneous Architectures

EDUCATION

The Pennsylvania State University, University Park, PA, USA **Fall 2010 - Present**
Ph.D. Candidate in Computer Science and Engineering, *Advisor*: Chita Das
`Proposed Thesis`: Memory-aware Scheduling Techniques for Many-core Architectures
GPA: 3.88

San Jose State University, San Jose, CA, USA **Fall 2008 - Spring 2010**
Master of Science in Computer Engineering
GPA: 3.79

Middle East Technical University, Ankara, Turkey **Fall 2003 - Fall 2007**
Bachelor of Technology in Electrical and Electronics Engineering

AWARDS AND HONORS

Best Paper Nomination, PACT 2013
Student Travel Grant: PACT 2013
College of Engineering Fellowship, Penn State University, 2010

PUBLICATIONS

[**MICRO 2014**] **Onur Kayiran**, Nachiappan CN, Adwait Jog, Rachata Ausavarungnirun, Mahmut Kandemir, Gabriel Loh, Onur Mutlu, Chita Das, *Managing Concurrency in Heterogeneous CPU-GPU Architectures*, In 47^{th} International Symposium on Micro Architecture (MICRO), Cambridge, UK, Dec 2014

[**PACT 2013**] **Onur Kayiran**, Adwait Jog, Mahmut Kandemir, Chita Das, *Neither More Nor Less: Optimizing Thread-Level Parallelism for GPGPUs*, In 22^{nd} International Conference on Parallel Architectures and Compilation Techniques (PACT), Edinburgh, Scotland, September, 2013

[**ISCA 2013**] Adwait Jog, **Onur Kayiran**, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *Orchestrated Scheduling and Prefetching for GPGPUs*, In 40^{th} International Symposium on Computer Architecture (ISCA), Tel Aviv, Israel, June, 2013

[**ASPLOS 2013**] Adwait Jog, **Onur Kayiran**, Nachiappan CN, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance*, In 18^{th} International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Houston, TX, USA, March, 2013

Papers Under Submission

[**HPCA 2015**] Adwait Jog, **Onur Kayiran**, Ashutosh Pattnaik, Mahmut Kandemir, Onur Mutlu, Ravishankar Iyer, Chita Das,
A Case for Criticality Aware Memory Scheduling in GPUs, In the 21^{st} IEEE International Symposium on High Performance Computer Architecture (HPCA), Bay Area, CA, Feb 2015

[**HPCA 2015**] Amin Jadidi, **Onur Kayiran**, Adwait Jog, Mahmut Kandemir, Chita Das,
Kernel-Based Energy Optimization in GPGPUs, In the 21^{st} IEEE International Symposium on High Performance Computer Architecture (HPCA), Bay Area, CA, Feb 2015

[**ASPLOS 2015**] Adwait Jog, **Onur Kayiran**, Tuba Kesten, Ashutosh Pattnaik, Evgeny Bolotin, Niladrish Chatterjee, Steve Keckler, Mahmut Kandemir, Chita Das,
Anatomy of GPU Memory System for Multi-Application Execution, In the 20^{th} International Conference on Architectural Support for Programming Languages and Operating Systems Architecture (ASPLOS), Istanbul, Turkey, Mar 2015

Research and Industrial Experience

Graduate Research Assistant, Penn State **Fall 2012 - Present**
Advisor: Prof. Chita Das, High Performance Computing Lab (HPCL) **University Park, PA**
- Proposed techniques for managing concurrency in CPU-GPU architectures.
- Proposed a CTA-Aware warp scheduling policy to mitigate contention in GPU memory system.
- Evaluated the trade-off between DRAM access locality and criticality in GPUs.
- Proposed a coordinated scheduling and prefetching mechanism to improve GPU performance.

Samsung SISA, Graduate Research Intern **Summer 2013**
Manager: Michael Shebanow **San Jose, CA**
Mentor: Mike Butler
Researched on energy-efficient cache management policies.

Talks and Poster Sessions

Neither More Nor Less: Optimizing Thread-Level Parallelism for GPGPUs,
– PACT 2013, Edinburgh, UK, September 2013

Teaching Experience

Teaching Assistant, CMPEN 331, Computer Orginazation and Design **Spring 2012**
Teaching Assistant, CMPEN 331, Computer Orginazation and Design **Fall 2011**
Teaching Assistant, CMPEN 331, Computer Orginazation and Design **Spring 2011**
Teaching Assistant, CMPEN 270, Digital Design: Theory and Practice **Fall 2010**

Skills

C/C++, Perl/Bash Scripting, GPGPU-Sim, CACTI, MATLAB, GDB, Verilog, VHDL, MIPS Assembly, CUDA, Spice, Cadence, Synopsys

Service and Memberships

Independent Reviewer:
HPCA 2014
Secondary Reviewer: ISCA, MICRO, HPCA, PACT, ICCAD, DAC, PPoPP, LCTES
Memberships: IEEE, ACM and ACM SIGARCH student member

Courses @ Penn State

Topics in Computer Architecture	Performance Evaluation	Multiprocessor Architecture
Algorithm Design & Analysis	VLSI Digital Circuit	Data Center Architectures
Numerical Linear Algebra	Data Structures & Algorithms	

Course Projects

Implementation of a CC-NUMA Machine
- Developed micro-benchmarks to perform scalability studies on the simulated CC-NUMA machine

Case Study on GPGPU interconnects
- Formulated performance model for GPGPU interconnects

Digital Audio Processor
- Designed and implemented an FPGA-based guitar processor

Goal-scoring Robot
- Designed and implemented a sensor-based robot that finds a ball in a field, and sends it to goal

Undergraduate Internships

Summer Intern, Ankara, Turkey **Summer 2006**
ASELSAN, Microwave and Systems Technologies
Developed software for a defense-industry product

Summer Intern, Ankara, Turkey **Summer 2005**
Tumer Engineering R&D Department
Implemented a PIC-based controller

Citizenship

Turkish citizen
F1 Visa in USA