3 Flash program memory and data EEPROM (FLASH)

3.1 Introduction

The non-volatile memory (NVM) is composed of:

- Up to 192 Kbytes of Flash program memory. This area is used to store the application code.
- Up to 6 Kbytes of data EEPROM
- An information block:
  - Up to 8 Kbytes of System memory
  - Up to 8x4 bytes of user Option bytes
  - Up to 96 bytes of factory Option bytes

3.2 NVM main features

The NVM interface features:

- Read interface organized by word, half-word or byte in every area
- Programming in the Flash memory performed by word or half-page
- Programming in the Option bytes area performed by word
- Programming in the data EEPROM performed by word, half-word or byte (granularity of the data EEPROM is one word, erase/write endurance cycles are linked to one word granularity)
- Erase operation performed by page (in Flash memory, data EEPROM and Option bytes)
- Option byte Loader
- ECC (Error Correction Code): 6 bits stored for every word to recognize and correct just one error
- Mass erase operation
- Read / Write protection
- PCROP protection
- Low-power mode
- Category 5 devices only:
  - Dual-bank memory with read-while-write
  - Dual-bank boot capability allowing to boot either from Bank 1 or Bank 2 at startup
  - Bank swapping capability.

3.3 NVM functional description

3.3.1 NVM organization

The NVM is organized as 32-bit memory cells that can be used to store code, data, boot code or Option bytes.

The memory array is divided into pages. A page is composed of 32 words (or 128 bytes) in Flash program memory and System memory, and 1 single word (or 4 bytes) in data EEPROM and Option bytes areas (user and factory). The erase/write endurance cycles are linked to one page granularity for Flash program memory and one single word granularity for data EEPROM.

A Flash sector is made of 32 pages (or 4 Kbytes). The sector is the granularity of the write protection.

Table 5. NVM organization (category 3 devices)

NVM	NVM addresses	Size (bytes)	Name	Description
Flash program memory(1)	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1	
	-	-	-	
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31	
	. . .	. . .	. . .	. . .
	0x0800 7000 - 0x0800 707F	128 bytes	Page 224	sector 7
	0x0800 7080 - 0x0800 70FF	128 bytes	Page 225	
	-	-	-	
	0x0800 7F80 - 0x0800 7FFF	128 bytes	Page 255	
	. . .	. . .	. . .	. . .
	0x0800 F000 - 0x0800 F07F	128 bytes	Page 480	sector 15
	0x0800 F080 - 0x0800 F0FF	128 bytes	Page 481	
	-	-	-	
	0x0800 FF80 - 0x0800 FFFF	128 bytes	Page 511	
Data EEPROM	0x0808 0000 - 0x0808 07FF	2 Kbytes	-	Data EEPROM
Information block	0x1FF0 0000 - 0x1FF0 0FFF	4 Kbytes	-	System memory
	0x1FF8 0020 - 0x1FF8 007F	96 bytes	-	Factory Options
	0x1FF8 0000 - 0x1FF8 001F	32 bytes	-	User Option bytes

1. For 32 Kbyte category 3 devices, the Flash program memory is divided into 256 pages of 128 bytes each.

Table 6. NVM organization for UFB = 0 (192 Kbyte category 5 devices)

NVM	NVM addresses	Size (bytes)	Name	Description	
Flash program memory	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0	Bank 1
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1		
	-	-	-		
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31		
	. . .	. . .	. . .	. . .	
	0x0800 7000 - 0x0800 707F	128 bytes	Page 224	sector 7	
	0x0800 7080 - 0x0800 70FF	128 bytes	Page 225		
	-	-	-		
	0x0800 7F80 - 0x0800 7FFF	128 bytes	Page 255		
	. . .	. . .	. . .	. . .	
	-	-	-		
	0x0801 7F80- 0x0801 7FFF	128 bytes	Page 767	sector 23	
	0x0801 8000 - 0x0801 807F	128 bytes	Page 768	sector 24	Bank 2
	. . .	. . .	. . .	. . .	
	0x0802 F000 - 0x0802 F07F	128 bytes	Page 1504	sector 47	
	0x0802 F080 - 0x0802 F0FF	128 bytes	Page 1505		
	-	-	-		
	0x0802 FF80 - 0x0802 FFFF	128 bytes	Page 1535		
Data EEPROM	0x0808 0000 - 0x0808 0BFF	6 Kbytes	-	Data EEPROM Bank 1	
	0x0808 0C00 - 0x0808 17FF		-	Data EEPROM Bank 2	
Information block	0x1FF0 0000 - 0x1FF0 1FFF	8 Kbytes	-	System memory	
	0x1FF8 0020 - 0x1FF8 007F	96 bytes	-	Factory Options	
	0x1FF8 0000 - 0x1FF8 001F	32 bytes	-	User Option bytes	

Table 7. Flash memory and data EEPROM remapping (192 Kbyte category 5 devices)

NVM	Description	NVM addresses		Remapped addresses	
		MEM_MODE = 0, BOOT0= 0 and UFB = 0	MEM_MODE = 0, BOOT0= 0 and UFB = 1	MEM_MODE = 0, BOOT0= 0 and UFB = 0	MEM_MODE = 0, BOOT0= 0 and UFB = 1
Flash program memory	Bank 1	0x0800 0000 - 0x0801 7FFF	0x0801 8000 - 0x0802 FFFF	0x0000 0000 - 0x0001 7FFF	0x0001 8000 - 0x0002 FFFF
	Bank 2	0x0801 8000 - 0x0802 FFFF	0x08000 0000 - 0x0801 7FFF	0x0001 8000 - 0x0002 FFFF	0x0000 0000 - 0x0001 7FFF
Data EEPROM	Bank 1	0x0808 0000 - 0x0808 0BFF	0x0808 0C00 - 0x0808 17FF	0x0008 0000 - 0x0008 0BFF	0x0008 0C00 - 0x0008 17FF
	Bank 2	0x0808 0C00 - 0x0808 17FF	0x0808 0000 - 0x0008 0BFF	0x0008 0C00 - 0x0008 17FF	0x0008 0000 - 0x0008 0BFF

Table 8. NVM organization for UFB = 0 (128 Kbyte category 5 devices)

NVM	NVM addresses	Size (bytes)	Name	Description	
Flash program memory	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0	Bank 1
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1		
	-	-	-		
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31		
	. . .	. . .	. . .	. . .	
	0x0800 7000 - 0x0800 707F	128 bytes	Page 224	sector 7	
	0x0800 7080 - 0x0800 70FF	128 bytes	Page 225		
	-	-	-		
	0x0800 7F80 - 0x0800 7FFF	128 bytes	Page 255		
	. . .	. . .	. . .	. . .	
	0x0800 FF80- 0x0800 FFFF	128 bytes	Page 511	sector 15	
	0x0801 0000 - 0x0801 007F	128 bytes	Page 512	sector 16	Bank 2
	. . .	. . .	. . .	. . .	
	0x0801 F000 - 0x0801 F07F		Page 992	sector 31	
	-	-	-		
	0x0801 FF80 - 0x0801 FFFF	128 bytes	Page 1023		
Data EEPROM	0x0808 0000 - 0x0808 0BFF	6 Kbytes	-	Data EEPROM Bank 1	
	0x0808 0C00 - 0x0808 17FF		-	Data EEPROM Bank 2	

Table 8. NVM organization for UFB = 0 (128 Kbyte category 5 devices) (continued)

NVM	NVM addresses	Size (bytes)	Name	Description
Information block	0x1FF0 0000 - 0x1FF0 1FFF	8 Kbytes	-	System memory
	0x1FF8 0020 - 0x1FF8 007F	96 bytes	-	Factory Options
	0x1FF8 0000 - 0x1FF8 001F	32 bytes		User Option bytes

Table 9. Flash memory and data EEPROM remapping (128 Kbyte category 5 devices)

NVM	Description	NVM addresses		Remapped addresses	
		MEM_MODE = 0, BOOT0= 0 and UFB = 0	MEM_MODE = 0, BOOT0= 0 and UFB = 1	MEM_MODE = 0, BOOT0= 0 and UFB = 0	MEM_MODE = 0, BOOT0= 0 and UFB = 1
Flash program memory	Bank 1	0x0800 0000 - 0x0800 FFFF	0x0801 0000 - 0x0801 FFFF	0x0000 0000 - 0x0000 FFFF	0x0001 0000 - 0x0001 FFFF
	Bank 2	0x0801 0000 - 0x0801 FFFF	0x0800 0000 - 0x0800 FFFF	0x0001 0000 - 0x0001 FFFF	0x0000 0000 - 0x0000 FFFF
Data EEPROM	Bank 1	0x0808 0000 - 0x0808 0BFF	0x0808 0C00 - 0x0808 17FF	0x0008 0000 - 0x0008 0BFF	0x0008 0C00 - 0x0008 17FF
	Bank 2	0x0808 0C00 - 0x0808 17FF	0x0808 0000 - 0x0808 0BFF	0x0008 0C00 - 0x0008 17FF	0x0008 0000 - 0x0008 0BFF

Table 10. NVM organization for UFB = 0 (64 Kbyte category 5 devices)(1)

NVM	NVM addresses	Size (bytes)	Name	Description	
Flash program memory	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0	Bank 1
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1		
	-	-	-		
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31		
	. . .	. . .	. . .	. . .	
	0x0800 F000 - 0x0800 F07F	128 bytes	Page 480	sector 15	
	-	-	-		
	-	-	-		
	0x0800 FF80 - 0x0800 FFFF	128 bytes	Page 511		
Data EEPROM	0x0808 0C00 - 0x0808 17FF	3 Kbytes	-	Data EEPROM Bank 2	
Information block	0x1FF0 0000 - 0x1FF0 1FFF	8 Kbytes	-	System memory	
	0x1FF8 0020 - 0x1FF8 007F	96 bytes	-	Factory Options	
	0x1FF8 0000 - 0x1FF8 001F	32 bytes		User Option bytes	

1. Flash memory and data EEPROM remapping is not possible on 64 Kbyte category 5 devices.

3.3.2 Dual-bank boot capability

Category 5 devices have two Flash memory banks: Bank 1 and Bank 2. They feature an additional boot mechanism which allows booting either from Bank 2 or from Bank 1 depending on BFB2 bit status (bit 23 in FLASH_OPTR register).

- When the BFB2 bit is set and the boot pins are configured to boot from Flash memory (BOOT0 = 0 and BOOT1 = x), the device maps the System memory at address 0. It boots from the System memory after reset and Standby and executes (during approximately 440 µs) the embedded bootloader code which implements the dual-bank boot mechanism:
  a) The System memory code first checks Bank 2. If it contains a valid code (see note below), it sets the UFB bit in SYSCFG_CFGR1 register to map Bank 2 at address 0x0800 0000, jumps to the application code located in Bank 2, and leaves the bootloader.
  b) If the code located in Bank 2 is not valid, the System memory code checks Bank 1 code. If it is valid (see note below), it jumps to the application located in Bank 1 (UFB is kept at '0' so that Bank 1 remains mapped at address 0x0800 0000).
  c) If both Bank 2 and Bank 1 do not contain valid code (see note below), the normal bootloader operations are executed when the protection level2 is disabled. Otherwise, the System memory code jumps to Bank 1 regardless of its validity. Refer to *Table 11* for more details.
- When BFB2 bit is reset (default state), the dual-bank boot mechanism is not performed.

Note: The code is considered as valid when the first data located at the bank start address (which should be the stack pointer) points to a valid address (stack top address).

For category 5 devices, the Flash memory Bank 1 and Bank 2, System memory or SRAM can be selected as the boot area, as shown in *Table 11* below.

Table 11. Boot pin and BFB2 bit configuration

Protection level	BFB2 bit	Boot mode selection		Boot mode	Aliasing
		nBOOT1 option bit	BOOT0 pin		
0 or 1	0	X	0	User Flash memory	User Flash memory Bank1 is selected as the boot area.
		1	1	System memory	Boot on System memory to execute bootloader.
		0	1	Embedded SRAM	Boot on Embedded SRAM
	1	X	0	System memory	Boot on System memory to execute dual bank boot mechanism. If Bank 2 and Bank 1are not valid, bootloader is executed for Flash update.
		1	1	System memory	Boot on System memory to execute bootloader.
		0	1	Embedded SRAM	Boot on Embedded SRAM.