3 Flash program memory and data EEPROM (FLASH)

3.1 NVM introduction

- Up to 512 Kbytes of Flash program memory
- Memory organization (dual bank; for Cat.4, Cat.5 and Cat.6 devices only):
  - Up to 512 Kbytes of Flash program memory and up to 16 Kbytes of data EEPROM
  - Up to 8 Kbytes of system memory and up to 64 bytes of option bytes

Each bank in dual bank devices is organized as follows:

- 192/256 Kbytes of program memory and 6/8 Kbytes of data (for Cat.4, Cat.5 and Cat.6 devices only)
- 4 Kbytes of system memory, 32 bytes of option bytes

Flash memory interface (FLITF) features:

- Flash memory read operations: read access is performed by 64 or 32 bits
- Flash memory program/erase operations
- Read while write (RWW) from one bank to the other
- Read/write protection
- Write access is performed by 32 bits
- Option byte loader reset
- Low power mode:
  - Flash memory in Power down mode when the STM32L1xxxx is in the Standby mode or the Stop mode
  - Flash memory can be placed in Power down or Idle mode when the STM32L1xxxx is in the Sleep mode
  - Flash memory can be placed in Power down or Idle mode when the STM32L1xxxx is in the Run mode

Note: The DMA can only access Flash memory module with read operations.

Note: Code execution is not possible from Data EEPROM.

3.2 NVM organization

The memory is organized as Program memory blocks, data EEPROM blocks and information blocks. *Table 8*, *Table 9*, *Table 10* and *Table 11* show the memory organization (the maximum configuration for given product category). See device datasheet for Flash program memory size and data EEPROM memory size availability.

The Flash program memory block is divided into sectors of 4 Kbytes each, and each sector is further split up into 16 pages of 256 bytes each. The sector is the write protection granularity. The pages are the erase granularity for the program memory block.

The Flash program memory pages can be written using a half page programming or a fast word programming operation.

Data EEPROM can be erased and written by:

- Double word
- Word/ Fast word
- Half word / Fast half word
- Byte / Fast byte

During a write/erase operation to the NVM (except Half Page programming or Double-word erase/write), any attempt to read the same bank of NVM stalls the bus. The read operation is executed correctly once the programming operation is completed. This means that code or data fetches cannot be performed while a write/erase operation is ongoing in the same bank.

For more details, refer to *Section 3.4.2: Erasing memory on page 64* and *Section 3.4.3: Programming memory on page 65*.

Table 8. NVM module organization (Cat.1 and Cat.2 devices)

Block	Name		Memory addresses	Size
Program memory	Sector 0	Page 0	0x0800 0000 - 0x0800 00FF	256 bytes
		Page 1	0x0800 0100 - 0x0800 01FF	256 bytes
		Page 2	0x0800 0200 - 0x0800 02FF	256 bytes
		Page 3	0x0800 0300 - 0x0800 03FF	256 bytes
		Page 4 to 7	0x0800 0400 - 0x0800 07FF	1 Kbyte
		Page 8 to 11	0x0800 0800 - 0x0800 0BFF	1 Kbyte
		Page 12 to 15	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Sector 1		0x0800 1000 - 0x0800 1FFF	4 Kbytes
	Sector 2		0x0800 2000 - 0x0800 2FFF	4 Kbytes
	Sector 3		0x0800 3000 - 0x0800 3FFF	4 Kbytes
	. . .		. . .	. . .
	Sector 30		0x0801 E000 - 0x0801 EFFF	4 Kbytes
	Sector 31		0x0801 F000 - 0x0801 FFFF	4 Kbytes
Data EEPROM			0x0808 0000 - 0x0808 0FFF	4096 bytes

Table 8. NVM module organization (Cat.1 and Cat.2 devices) (continued)

Block	Name		Memory addresses	Size
Information block	System memory	Page 0	0x1FF0 0000 - 0X1FF0 00FF	256 bytes
		Page 1	0x1FF0 0100 - 0X1FF0 01FF	256 bytes
		Page 2	0x1FF0 0200 - 0X1FF0 02FF	256 bytes
		Page 3	0x1FF0 0300 - 0X1FF0 03FF	256 bytes
		. . .	. . .	. . .
		Page 15	0x1FF0 0F00 - 0X1FF0 0FFF	256 bytes
	Option bytes		0x1FF8 0000 - 0X1FF8 001F	32 bytes
	Factory information		0x1FF8 0020 - 0X1FF8 00FF	224 bytes

Table 9. NVM module organization (Cat.3 devices)

Block	Name		Memory addresses	Size
Program memory	Sector 0	Page 0	0x0800 0000 - 0x0800 00FF	256 bytes
		Page 1	0x0800 0100 - 0x0800 01FF	256 bytes
		Page 2	0x0800 0200 - 0x0800 02FF	256 bytes
		Page 3	0x0800 0300 - 0x0800 03FF	256 bytes
		Page 4 to 7	0x0800 0400 - 0x0800 07FF	1 Kbyte
		Page 8 to 11	0x0800 0800 - 0x0800 0BFF	1 Kbyte
		Page 12 to 15	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Sector 1	Page 16 to 31	0x0800 1000 - 0x0800 1FFF	4 Kbytes
	Sector 2	Page 32 to 47	0x0800 2000 - 0x0800 2FFF	4 Kbytes
	Sector 3	Page 48 to 63	0x0800 3000 - 0x0800 3FFF	4 Kbytes
	. . .	. . .	. . .	. . .
	Sector 30	Page 478 to 495	0x0801 E000 - 0x0801 EFFF	4 Kbytes
	Sector 31	Page 496 to 511	0x0801 F000 - 0x0801 FFFF	4 Kbytes
	Sector 32 to Sector 47	Page 512 to 767	0x0802 0000 - 0x0802 FFFF	64 Kbytes
	Sector 48 to Sector 63	Page 768 to 1023	0x0803 0000 - 0x0803 FFFF	64 Kbytes
Data EEPROM			0x0808 0000 - 0x0808 1FFF	8 Kbytes

Table 9. NVM module organization (Cat.3 devices) (continued)

Block	Name		Memory addresses	Size
Information Block	System memory	Page 0	0x1FF0 0000 - 0x1FF0 00FF	256 bytes
		Page 1	0x1FF0 0100 - 0x1FF0 01FF	256 bytes
		Page 2	0x1FF0 0200 - 0x1FF0 02FF	256 bytes
		Page 3	0x1FF0 0300 - 0x1FF0 03FF	256 bytes
		. . .	. . .	. . .
		Page 15	0x1FF0 0F00 - 0x1FF0 0FFF	256 bytes
		Page 16 to 31	0x1FF0 1000 - 0x1FF0 1FFF	4 Kbytes
	Option bytes		0x1FF8 0000 - 0x1FF8 001F	32 bytes
	Factory information		0x1FF8 0020 - 0x1FF8 00FF	224 bytes

Table 10. NVM module organization (Cat.4 devices)

Block	Name		Memory addresses	Size
Program memory bank 1	Sector 0	Page 0	0x0800 0000 - 0x0800 00FF	256 bytes
		Page 1	0x0800 0100 - 0x0800 01FF	256 bytes
		Page 2	0x0800 0200 - 0x0800 02FF	256 bytes
		Page 3	0x0800 0300 - 0x0800 03FF	256 bytes
		Page 4 to 7	0x0800 0400 - 0x0800 07FF	1 Kbyte
		Page 8 to 11	0x0800 0800 - 0x0800 0BFF	1 Kbyte
		Page 12 to 15	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Sector 1	Page 16 to 31	0x0800 1000 - 0x0800 1FFF	4 Kbytes
	Sector 2	Page 32 to 47	0x0800 2000 - 0x0800 2FFF	4 Kbytes
	Sector 3	Page 48 to 63	0x0800 3000 - 0x0800 3FFF	4 Kbytes
	. . .	. . .	. . .	. . .
	Sector 30	Page 478 to 495	0x0801 E000 - 0x0801 EFFF	4 Kbytes
	Sector 31	Page 496 to 511	0x0801 F000 - 0x0801 FFFF	4 Kbytes
	Sector 32 to Sector 47	Page 512 to 767	0x0802 0000 - 0x0802 FFFF	64 Kbytes
Program memory bank 2	Sector 48 to Sector 79	Page 768 to 1279	0x0803 0000 - 0x0804 FFFF	128 Kbytes
	Sector 80 to Sector 95	Page 1280 to 1535	0x0805 0000 - 0x0805 FFFF	64 Kbytes
Data EEPROM bank 1			0x0808 0000 - 0x0808 17FF	6 Kbytes

Table 10. NVM module organization (Cat.4 devices) (continued)

Block	Name		Memory addresses	Size
Data EEPROM bank 2			0x0808 1800 - 0x0808 2FFF	6 Kbytes
System memory bank 1		Page 0	0x1FF0 0000 - 0x1FF0 00FF	256 bytes
		Page 1	0x1FF0 0100 - 0x1FF0 01FF	256 bytes
		Page 2	0x1FF0 0200 - 0x1FF0 02FF	256 bytes
		Page 3	0x1FF0 0300 - 0x1FF0 03FF	256 bytes
		. . .	. . .	. . .
		Page 15	0x1FF0 0F00 - 0x1FF0 0FFF	256 bytes
System memory bank 2		Page 16 to 31	0x1FF0 1000 - 0x1FF0 1FFF	4 Kbytes
Option bytes bank 1			0x1FF8 0000 - 0x1FF8 001F	32 bytes
Factory information bank 1			0x1FF8 0020 - 0x1FF8 007F	96 bytes
Option bytes bank 2			0x1FF8 0080 - 0x1FF8 009F	32 bytes
Factory information bank 2			0x1FF8 00A0 - 0x1FF8 00FF	96 bytes

Table 11. NVM module organization (Cat.5 devices)

Block	Name		Memory addresses	Size
Program memory bank 1	Sector 0	Page 0	0x0800 0000 - 0x0800 00FF	256 bytes
		Page 1	0x0800 0100 - 0x0800 01FF	256 bytes
		Page 2	0x0800 0200 - 0x0800 02FF	256 bytes
		Page 3	0x0800 0300 - 0x0800 03FF	256 bytes
		Page 4 to 7	0x0800 0400 - 0x0800 07FF	1 Kbyte
		Page 8 to 11	0x0800 0800 - 0x0800 0BFF	1 Kbyte
		Page 12 to 15	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Sector 1	Page 16 to 31	0x0800 1000 - 0x0800 1FFF	4 Kbytes
	Sector 2	Page 32 to 47	0x0800 2000 - 0x0800 2FFF	4 Kbytes
	Sector 3	Page 48 to 63	0x0800 3000 - 0x0800 3FFF	4 Kbytes
	. . .	. . .	. . .	. . .
	Sector 30	Page 478 to 495	0x0801 E000 - 0x0801 EFFF	4 Kbytes
	Sector 31	Page 496 to 511	0x0801 F000 - 0x0801 FFFF	4 Kbytes
	Sector 32 to Sector 63	Page 512 to 1023	0x0802 0000 - 0x0803 FFFF	128 Kbytes

Table 11. NVM module organization (Cat.5 devices) (continued)

Block	Name		Memory addresses	Size
Program memory bank 2	Sector 64 to Sector 95	Page 1024 to 1535	0x0804 0000 - 0x0805 FFFF	128 Kbytes
	Sector 96 to Sector 127	Page 1536 to 2047	0x0806 0000 - 0x0807 FFFF	128 Kbytes
Data EEPROM bank 1			0x0808 0000 - 0x0808 1FFF	8 Kbytes
Data EEPROM bank 2			0x0808 2000 - 0x0808 3FFF	8 Kbytes
System memory bank 1		Page 0	0x1FF0 0000 - 0x1FF0 00FF	256 bytes
		Page 1	0x1FF0 0100 - 0x1FF0 01FF	256 bytes
		Page 2	0x1FF0 0200 - 0x1FF0 02FF	256 bytes
		Page 3	0x1FF0 0300 - 0x1FF0 03FF	256 bytes
		. . .	. . .	. . .
		Page 15	0x1FF0 0F00 - 0x1FF0 0FFF	256 bytes
System memory bank 2		Page 16 to 31	0x1FF0 1000 - 0x1FF0 1FFF	4 Kbytes
Option bytes bank 1			0x1FF8 0000 - 0x1FF8 001F	32 bytes
Factory information bank 1			0x1FF8 0020 - 0x1FF8 007F	96 bytes
Option bytes bank 2			0x1FF8 0080 - 0x1FF8 009F	32 bytes
Factory information bank 2			0x1FF8 00A0 - 0x1FF8 00FF	96 bytes

Table 12. NVM module organization (Cat.6 devices)

Block	Name		Memory addresses	Size
Program memory bank 1	Sector 0	Page 0	0x0800 0000 - 0x0800 00FF	256 bytes
		Page 1	0x0800 0100 - 0x0800 01FF	256 bytes
		Page 2	0x0800 0200 - 0x0800 02FF	256 bytes
		Page 3	0x0800 0300 - 0x0800 03FF	256 bytes
		Page 4 to 7	0x0800 0400 - 0x0800 07FF	1 Kbyte
		Page 8 to 11	0x0800 0800 - 0x0800 0BFF	1 Kbyte
		Page 12 to 15	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Sector 1	Page 16 to 31	0x0800 1000 - 0x0800 1FFF	4 Kbytes
	Sector 2	Page 32 to 47	0x0800 2000 - 0x0800 2FFF	4 Kbytes
	Sector 3	Page 48 to 63	0x0800 3000 - 0x0800 3FFF	4 Kbytes
	. . .	. . .	. . .	. . .
	Sector 30	Page 478 to 495	0x0801 E000 - 0x0801 EFFF	4 Kbytes
	Sector 31	Page 496 to 511	0x0801 F000 - 0x0801 FFFF	4 Kbytes
	Sector 32 to Sector 47	Page 512 to 767	0x0802 0000 - 0x0802 FFFF	64 Kbytes
Program memory bank 2	Sector 48 to Sector 79	Page 768 to 1279	0x0804 0000 - 0x0805 FFFF	128 Kbytes
	Sector 80 to Sector 95	Page 1280 to 1535	0x0806 0000 - 0x0806 FFFF	64 Kbytes
Data EEPROM bank 1			0x0808 0000 - 0x0808 1FFF	8 Kbytes
Data EEPROM bank 2			0x0808 2000 - 0x0808 3FFF	8 Kbytes
System memory bank 1		Page 0	0x1FF0 0000 - 0x1FF0 00FF	256 bytes
		Page 1	0x1FF0 0100 - 0x1FF0 01FF	256 bytes
		Page 2	0x1FF0 0200 - 0x1FF0 02FF	256 bytes
		Page 3	0x1FF0 0300 - 0x1FF0 03FF	256 bytes
		. . .	. . .	. . .
		Page 15	0x1FF0 0F00 - 0x1FF0 0FFF	256 bytes
System memory bank 2		Page 16 to 31	0x1FF0 1000 - 0x1FF0 1FFF	4 Kbytes
Option bytes bank 1			0x1FF8 0000 - 0x1FF8 001F	32 bytes
Factory information bank 1			0x1FF8 0020 - 0x1FF8 007F	96 bytes
Option bytes bank 2			0x1FF8 0080 - 0x1FF8 009F	32 bytes
Factory information bank 2			0x1FF8 00A0 - 0x1FF8 00FF	96 bytes

3.3 Read interface

3.3.1 Relation between CPU clock frequency and Flash memory read time

The Flash memory is read by 64 bits or 32 bits.

64-bit access is configured by setting the ACC64 bit in the Flash access control register (FLASH_ACR). This access mode accelerates the execution of program operations. Prefetch is useful when the Flash memory cannot be accessed for a CPU cycle. In this case, the number of wait states (LATENCY) must be correctly programmed in the Flash access control register (FLASH_ACR) according to the frequency of the CPU clock (HCLK) and the supply voltage of the device. *Table 13* shows the correspondence between wait states and CPU clock frequency.

Table 13. Number of wait states (WS) according to CPU clock (HCLK) frequency

HCLK frequency (MHz)			Wait states (LATENCY)
V_{DD} range 1.65 V to 3.6 V		V_{DD} range 1.71 V to 3.6 V	
Range 3	Range 2	Range 1	
$f_{HCLK} \leq 2.1$ MHz (in Cat.1 devices) $f_{CPU} \leq 4.2$ MHz (in Cat.2, Cat.3, Cat.4, Cat.5 and Cat.6 devices)	$f_{HCLK} \leq 8$ MHz	$f_{HCLK} \leq 16$ MHz	0 WS (1 HCLK cycle)
$f_{HCLK} \leq 4.2$ MHz (in Cat.1 devices) $f_{HCLK} \leq 8$ (in Cat.2, Cat.3, Cat.4, Cat.5 and Cat.6 devices)	$f_{HCLK} \leq 16$ MHz	$f_{HCLK} \leq 32$ MHz	1 WS (2 HCLK cycles)

It is also possible to access the Flash memory by 32 bits. This is done by clearing the ACC64 bit in FLASH_ACR. In this case, prefetch has to be disabled. 32-bit access reduces the consumption, so it is used when the CPU frequency is low. In this case, the number of wait states must be 0.

After reset, the used clock is the MSI (2 MHz) with 0 WS configured in the FLASH_ACR register. 32-bit access is enabled and prefetch is disabled.

ST strongly recommends to use the following software sequences to tune the number of wait states needed to access the Flash memory with the CPU frequency.