3 Flash program memory and data EEPROM (FLASH)

3.1 Introduction

The non-volatile memory (NVM) is composed of:

- Up to 128 Kbytes of Flash program memory. This area is used to store the application code.
- Up to 512 bytes of data EEPROM
- An information block:
  - Up to 8 Kbytes of System memory
  - Up to 8x4 bytes of user Option bytes
  - Up to 96 bytes of factory Option bytes

3.2 NVM main features

The NVM interface features:

- Read interface organized by word, half-word or byte in every area
- Programming in the Flash memory performed by word or half-page
- Programming in the Option bytes area performed by word
- Programming in the data EEPROM performed by word, half-word or byte (granularity of the data EEPROM is one word, erase/write endurance cycles are linked to one word granularity)
- Erase operation performed by page (in Flash memory, data EEPROM and Option bytes)
- Option byte Loader
- ECC (Error Correction Code): 6 bits stored for every word to recognize and correct just one error
- Mass erase operation
- Read / Write protection
- PCROP protection
- Low-power mode

3.3 NVM functional description

3.3.1 NVM organization

The NVM is organized as 32-bit memory cells that can be used to store code, data, boot code or Option bytes.

The memory array is divided into pages. A page is composed of 32 words (or 128 bytes) in Flash program memory and System memory, and 1 single word (or 4 bytes) in data EEPROM and Option bytes areas (user and factory). The erase/write endurance cycles are

linked to one page granularity for Flash program memory and one single word granularity for data EEPROM.

A Flash sector is made of 32 pages (or 4 Kbytes). The sector is the granularity of the write protection.

Table 6. NVM organization (category 1 devices)

NVM	NVM addresses	Size (bytes)	Name	Description
Flash program memory	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1	
	-	-	-	
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31	
	. . .	. . .	. . .	. . .
	0x0800 3000 - 0x0800 307F	128 bytes	Page 96	sector 3
	0x0800 3080 - 0x0800 30FF	128 bytes	Page 97	
	-	-	-	
	0x0800 3F80 - 0x0800 3FFF	128 bytes	Page 127	
Data EEPROM	0x0808 0000 - 0x0808 007F	128 bytes		Data EEPROM
Information block	0x1FF0 0000 - 0x1FF0 0FFF	4 Kbytes		System memory
	0x1FF8 0020 - 0x1FF8 007F	96 bytes		Factory Options
	0x1FF8 0000 - 0x1FF8 001F	32 bytes		User Option bytes

Table 7. NVM organization (category 2 devices)

NVM	NVM addresses	Size (bytes)	Name	Description
Flash program memory	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1	
	-	-	-	
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31	
	. . .	. . .	. . .	. . .
	0x0800 7000 - 0x0800 707F	128 bytes	Page 224	sector 7
	0x0800 7080 - 0x0800 70FF	128 bytes	Page 225	
	-	-	-	
	0x0800 7F80 - 0x0800 7FFF	128 bytes	Page 255	
Data EEPROM	0x0808 0000 - 0x0808 00FF	256 bytes		Data EEPROM

Table 7. NVM organization (category 2 devices) (continued)

NVM	NVM addresses	Size (bytes)	Name	Description
Information block	0x1FF0 0000 - 0x1FF0 0FFF	4 Kbytes		System memory
	0x1FF8 0020 - 0x1FF8 007F	96 bytes		Factory Options
	0x1FF8 0000 - 0x1FF8 001F	32 bytes		User Option bytes

Table 8. NVM organization (category 3 devices)

NVM	NVM addresses	Size (bytes)	Name	Description
Flash program memory(1)	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1	
	-	-	-	
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31	
	. . .	. . .	. . .	. . .
	0x0800 7000 - 0x0800 707F	128 bytes	Page 224	sector 7
	0x0800 7080 - 0x0800 70FF	128 bytes	Page 225	
	-	-	-	
	0x0800 7F80 - 0x0800 7FFF	128 bytes	Page 255	
	. . .	. . .	. . .	. . .
	0x0800 F000 - 0x0800 F07F	128 bytes	Page 480	sector 15
	0x0800 F080 - 0x0800 F0FF	128 bytes	Page 481	
	-	-	-	
	0x0800 FF80 - 0x0800 FFFF	128 bytes	Page 511	
Data EEPROM	0x0808 0000 - 0x0808 00FF	256 bytes	-	Data EEPROM
Information block	0x1FF0 0000 - 0x1FF0 0FFF	4 Kbytes	-	System memory
	0x1FF8 0020 - 0x1FF8 007F	96 bytes	-	Factory Options
	0x1FF8 0000 - 0x1FF8 001F	32 bytes	-	User Option bytes

1. For 32 Kbyte category 3 devices, the Flash program memory is divided into 256 pages of 128 bytes each.

Table 9. NVM organization (category 5 devices)

NVM	NVM addresses	Size (bytes)	Name	Description
Flash program memory	0x0800 0000 - 0x0800 007F	128 bytes	Page 0	sector 0
	0x0800 0080 - 0x0800 00FF	128 bytes	Page 1	
	-	-	-	
	0x0800 0F80 - 0x0800 0FFF	128 bytes	Page 31	
	. . .	. . .	. . .	. . .
	0x0800 7000 - 0x0800 707F	128 bytes	Page 224	sector 7
	0x0800 7080 - 0x0800 70FF	128 bytes	Page 225	
	-	-	-	
	0x0800 7F80 - 0x0800 7FFF	128 bytes	Page 255	
	. . .	. . .	. . .	. . .
	0x0800 FF80- 0x0800 FFFF	128 bytes	Page 511	sector 15
	0x0801 0000 - 0x0801 007F	128 bytes	Page 512	sector 16
	. . .	. . .	. . .	. . .
	0x0801 F000 - 0x0801 F07F		Page 992	sector 31
	-	-	-	
	0x0801 FF80 - 0x0801 FFFF	128 bytes	Page 1023	
Data EEPROM	0x0808 0000 - 0x0808 01FF	512 Kbytes	-	Data EEPROM
Information block	0x1FF0 0000 - 0x1FF0 1FFF	8 Kbytes	-	System memory
	0x1FF8 0020 - 0x1FF8 007F	96 bytes	-	Factory Options
	0x1FF8 0000 - 0x1FF8 001F	32 bytes		User Option bytes

3.3.2 Reading the NVM

Protocol to read

To read the NVM content, take any address from *Section 3.3.1: NVM organization*. The clock of the memory interface must be running. (see MIFEN bit in *Section 7.3.12: AHB peripheral clock enable register (RCC_AHBENR)*).

Depending on the clock frequency, a 0 or a 1 wait state can be necessary to read the NVM.

The user must set the correct number of wait states (LATENCY bit in the FLASH_ACR register). No control is done to verify if the frequency or the power used is correct, with respect to the number of wait states. A wrong number of wait states can generate wrong read values (high frequency and 0 wait states) or a long time to execute a code (low frequency with 1 wait state).

You can read the NVM by word (4 bytes), half-word (2 bytes) or byte.

It is not possible to read the NVM during a write/erase operation. If a write/erase operation is ongoing, the reading will be in a wait state until the write/erase operation completes, stalling the master that requested the read operation, except when the address is read-protected. In this case, the error is sent to the master by a hard fault or a memory interface flag; no stall is generated and no read is waiting.

Relation between CPU frequency/Operation mode/NVM read time

The device (and the NVM) can work at different power ranges. For every range, some master clock frequencies can be set. *Table 10* resumes the link between the power range and the frequencies to ensure a correct time access to the NVM.

Table 10. Link between master clock power range and frequencies

Name	Power range	Maximum frequency (with 1 wait state)	Maximum frequency (without wait states)
Range 1	1.65 V - 1.95 V	32 MHz	16 MHz
Range 2	1.35 V - 1.65 V	16 MHz	8 MHz
Range 3	1.05 V - 1.35 V	4.2 MHz	4.2 MHz

Table 11 shows the delays to read a word in the NVM. Comparing the complete time to read a word (Ttotal) with the clock period, you can see that in Range 3 no wait state is necessary, also with the maximum frequency (4.2 MHz) allowed by the device. Ttotal is the time that the NVM needs to return a value, and not the complete time to read it (from memory to Core through the memory interface); all remaining time is lost.

Table 11. Delays to memory access and number of wait states

Name	Ttotal	Frequency	Period	Number of wait state required
Range 1	46.1 ns	32 MHz	31.25	1
		16 MHz	62.5	0
Range 2	86.8 ns	16 MHz	62.5	1
		8 MHz	125	0