NORTHERN MICHIGAN UNIVERSITY
Department of Electronics
Winter Semester 1997

ET 211: DIGITAL ELECTRONICS (4 credits)

Lecture: JC 117 Monday, Tuesday, Wednesday 9:00AM
Laboratory: JC 204 Thursday 9:00AM to 10:40AM

Instructor: R. M. Laurie
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Office Hours: Monday 10AM-11AM, Noon-1PM; Tuesday 10AM-Noon;
Wednesday 10AM-11AM, 1PM-2PM; Thursday 5-6PM; Friday 11PM-Noon.
Also by arrangement Monday 3PM-5PM, Tuesday 3PM-4PM (Tell me first)

Course Summary

This course will explore both combinational and sequential digital circuits and their implementation using integrated circuits. Topics include logic gates, flip-flops, number systems, digital coding, counters, multiplexers, and adders. ET110 is the prerequisite.
DD 105 concurrent enrollment.

Books

Digital Systems - Principles & Appliations, 6th Ed., Ronald J. Tocci, 1995, Prentice-Hall
Lab Manual - A Troubleshooting Approach, 6th Ed., Ronald J. Tocci, 1995, Prentice-Hall

Grades

Scores received from three exams and lab reports will be used to compute final grades. Note that the best 3 scores on 4 exams will be used to calculate final grades. The point values and grading scale are described below. I encourage students to study together and will not curve scores. Class attendance is mandatory.

SCORES:			SCALE: (% of points)			
Exam 1	100 *		A	93 - 100	C	73 - 76
Exam 2	100 *		A-	90 - 92	C-	70 - 72
Exam 3	100 *		B+	87 - 89	D+	67 - 69
Final Exam	100 *		B	83 - 86	D	63 - 66
Laboratory	100		B-	80 - 82	D-	60 - 62
Total	= 400 *		C+	77 - 79	F	59 and below

* Best 3 of 4 exams

Laboratory

A lab report is required for each lab. The lab report should contain an *Objective* section, a *Theory* section, a *Results* section, and a *Conclusion* section. See lab reports handout for detailed description. Grading will be 80% objective (results, explanations, conclusions) and 20% subjective (neatness, clarity, conciseness, extra work). The lab report is due one week after the lab is assigned. If the lab report is late, 20% will be deducted for each workday late. Lab attendance is mandatory. You will receive a zero for the lab if you are absent, unless a valid documented reason is provided.

NOTICE: *If you have a need for disability-related accommodations or services, please inform the Coordinator of Disability Services in the Disability Services Office at 405 Cohodas (Tel: 227-1550). Reasonable and effective accommodations and services will be provided to students if requests are made in a timely manner, with appropriate documentation, in accordance with federal, state, and university guidelines.*

ET 211 Course Schedule - Winter Semester 1997

Date:	Topics:	Read Before Class:
Jan 13	Introduction	
Jan 14	Binary Counting and Logic Gates (AND, OR, NOT)	1.0 to 1.5, 3.0 to 3.5
Jan 15	Boolean Algebra and Logic Gates (NAND, NOR)	3.6 to 3.9
Jan 17	No Lab	
Jan 20	Boolean Algebra Theorums	3.10 to 3.11
Jan 21	Boolean Algebra Simplification	4.3
Jan 22	Digital IC's	4.9 to 4.13
Jan 24	LAB: Exercise 8 - Simplification Using Boolean Theorums	Do all parts.
Jan 27	NAND/NOR Universality and Bubbles	3.12 to 3.13
Jan 28	Bubbles in Circuits and ANSI Representations	3.14 to 3.15
Jan 29	SOP Design	4.1 to 4.2, 4.4
Jan 31	LAB: Exercise 10 - The Universality of NAND and NOR Gates	Do all parts.
Feb 3	Karnaugh Map Reduction	4.5
Feb 4	Number Systems: Decimal, Binary, Hexadecimal	2.0 to 2.2, 2.4
Feb 5	Review	Study
Feb 7	*** EXAM 1 ***	Study
Feb 10	Signed 2's Complement Numbers, Addition, Subtraction	6.0 to 6.4
Feb 11	Exclusive-OR and Exclusive NOR Circuits and Binary Adders	4.6, 6.10 to 6.11
Feb 12	Binary Adders	6.12 to 6.15
Feb 14	LAB: Exercise 20 - Binary Adders and 2's Complement System	Do parts a to h.
Feb 17	Codes: BCD, Gray, ASCII	2.5 to 2.8
Feb 18	BCD Addition and BCD Adder, Hexadecimal Addition	6.7, 6.8, 6.16
Feb 19	Sequential Circuits and Flip-Flops	5.0, 5.4 to 5.9
Feb 21	LAB: Exercise 15 - Flip Flops I: Latches and clocked Flip Flops	Do parts k to r
Feb 24	Symbols and Timing	5.10 to 5.12
Feb 25	Frequency Division, Counting, Asynchronous Counters	5.19, 7.0 to 7.5
Feb 26	Troubleshooting	5.23, 5.25
Feb 28	LAB: Exercise 21 - Asynchronous IC Counters	Do parts h and i
Mar 10	Synchronous Counters and BCD	7.6 to 7.13
Mar 11	Data Storage and Shifting Applications	5.18, 5.20
Mar 12	Shift Register Counters and the Logic Analyzer	7.14 to 7.15
Mar 14	LAB: Exercise 26 - Shift Register Counters / Logic Analyzer Demo	Do all parts
Mar 17	Frequency and Clock Applications	7.16 to 7.17
Mar 18	Register IC's and Troubleshooting	7.19 to 7.24
Mar 19	Review	Study
Mar 21	*** EXAM 2 ***	Study
Mar 24	Schmitt Triggers and Multivibrators	5.21, 5.22, 5.24
Mar 25	Terminology and TTL Family	8.0 to 8.6
Mar 26	Open Collector and Tristate Outputs	8.7 to 8.8
Mar 28	LAB: Exercise 17 - Schmitt Trigger and Multivibrator	Do a to d and k to n
Mar 31	ECL, MOS, and CMOS Families and Interfacing	8.9 to 8.17, Handout
Apr 1	Decoders	9.1
Apr 2	BCD to 7 Segment Decoder/Drivers and LCD displays	9.2, 9.3
Apr 4	LAB: Project Phase 1	Definition and Design
Apr 7	Encoders and Troubleshooting	9.4, 9.6
Apr 8	Multiplexers	9.7, 9.8
Apr 9	Demultipexers and Magnitude Comparator	9.9, 9.12
Apr 11	LAB: Project Phase 2	Implementation
Apr 14	Digital to Analog Conversion	10.0 to 10.2, 10.4, 10.5
Apr 15	Analog to Digital Conversion and	10.8 to 10.10
Apr 16	Review	Study
Apr 18	*** EXAM 3 ***	Study
Apr 21	Buses, Memory, and Microprocessor Terminology	Handout
Apr 22	Buses, Memory, and Microprocessor Operation	Handout
Apr 23	Review	Study
Apr 25	LAB: Project Phase 3	Check Off and Submit
May 1	*** FINAL EXAM ***	