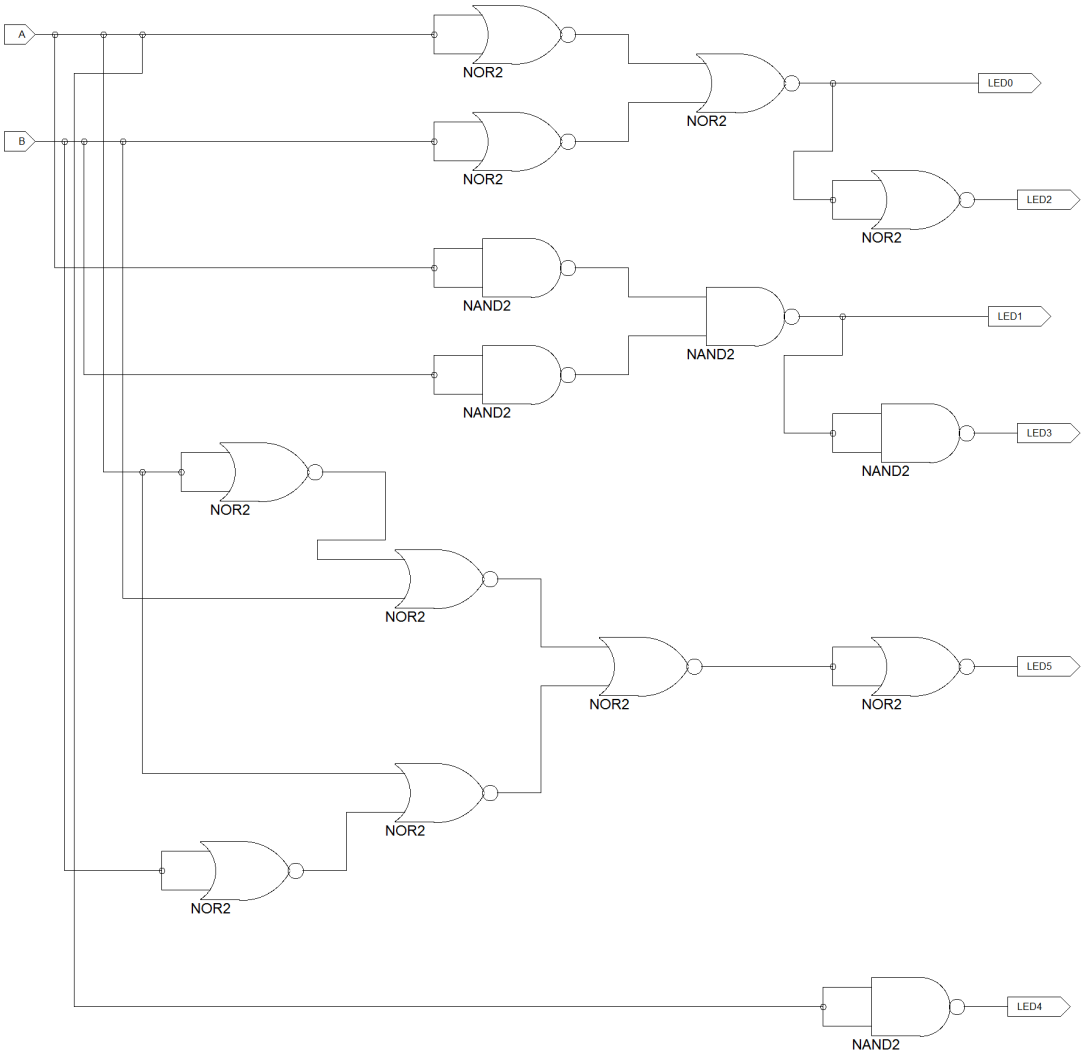
Class:	CECS 201, Section 7
Lab:	4
Title:	Gate Substitution and Boolean Alg
Student Name:	Barry Joseph Okonoboh
Due Date:	07:00:00 P.M., 16, March 2015
Instructor:	Dan Cregg

b. **Introduction.** This lab involves observing the outputs of the AND, OR, NAND, NOR, NOT and XOR logic gates, with varying input.

c. **Project Description.** This lab is similar to lab 3 with the restriction that the AND gate be built using NOR gates, the OR gates using NAND gates, the NAND gate using NOR gates, the NOR gate using NAND gates, the XOR gate using NOR gates, and the NOT gates using NAND gates.

d. **Schematic.**



Truth Table.

A	B	AB	$A+B$	$\overline{AB}$	$\overline{A+B}$	$A \oplus B$	$\overline{A}$
0	0	0	0	1	1	0	1
0	1	0	1	1	0	1	1
1	0	0	1	1	0	1	0
1	1	1	1	0	0	0	0