Class: CECS 201, Section 7

Lab: 8

Title: Latches and Flip-Flops

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Introduction. We investigate the functions of an S-R Latch, a D Flip-Flop, a T Flip-flop and a J-K Flip-Flip, and the differences between them.

Project Description. S-R Latch's Truth Table

S	R	Q_1
0	0	Q_1
0	1	0
1	0	1
1	1	??

For the S-R latch, we notice that if the clock rises from 0 to 1, then

- Q_1 will be set to 1 if S=1 and R=0.
- Q_1 will be set to 0 if S=0 and R=1.
- Q_1 's state will be unchanged if S = R = 0.
- indeterminate if S = R = 1.

Also the state of Q_1 does not change if the clock is not set.

D Flip-Flop's Truth Table

D	Q
0	0
1	1

On a positive clock edge, Q will attain the value of input D. If the clock is not set, then varying the input D will have no effect on Q, as evidenced in the lab.

T Flip-Flop's Truth Table

Т	Q	Q_{next}	Operation
0	0	0	Hold
0	1	1	Hold
1	0	1	Toggle
1	1	0	Toggle

The T Flip-Flops stores the value of its output if T is 0. But if T is 1, it negates the value in Q. The Q_{next} columns holds the future value of Q on a positive clock edge.

J-K Flip-Flop's Truth Table

J	K	Q	Q_{next}	Operation
0	0	0	0	Hold
0	0	1	1	Hold
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	1	Toggle
1	1	1	0	Toggle

As the lab and Truth Table showed us, a J-K Flip-Flop is a combination of a D Flip-Flop and a T-Flip Flop. We can select particular values for J and K so that it can mimic the behavior of a D Flip-Flop or a T-Flip Flop.

Schematic.

