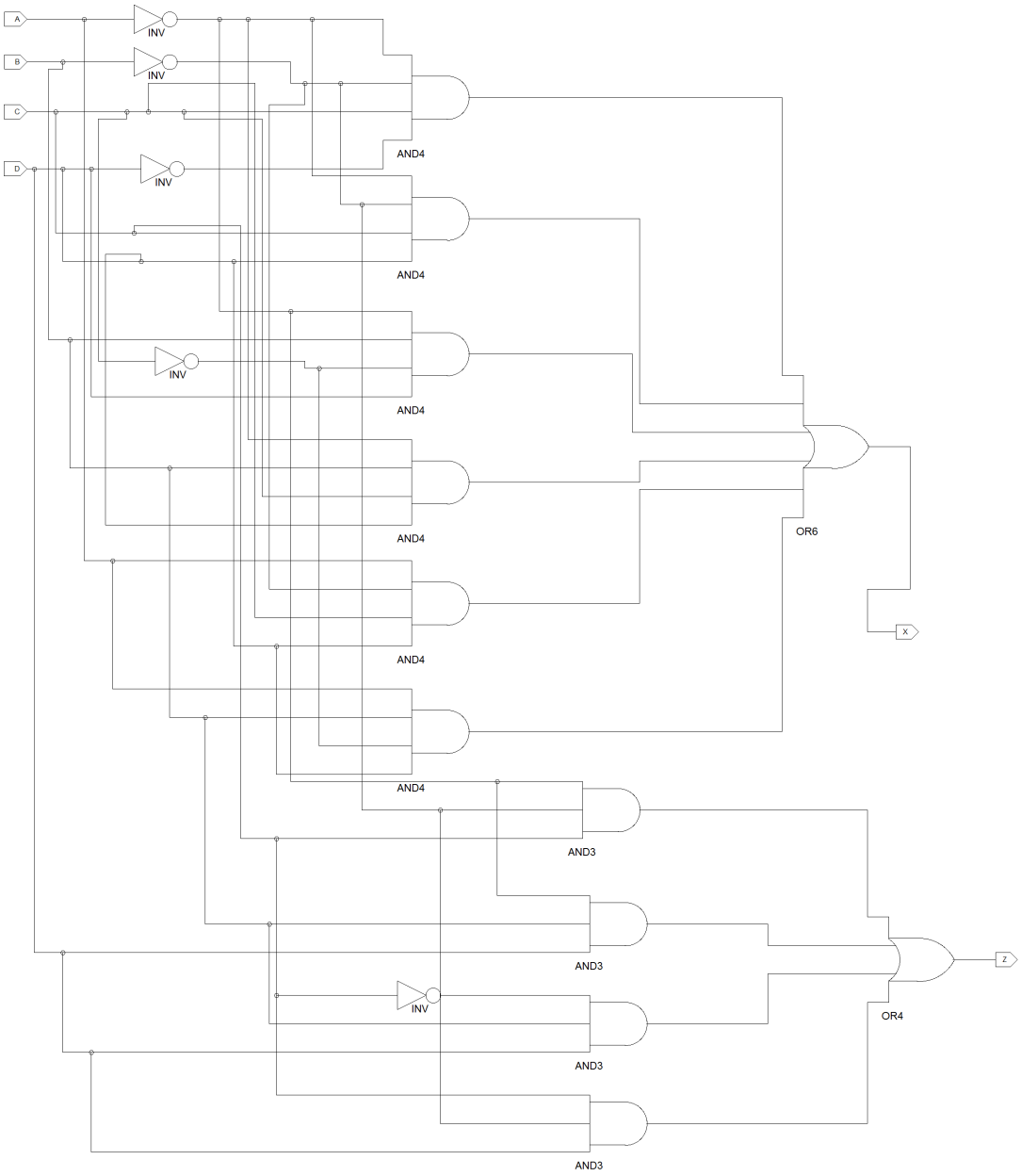
Class:	CECS 201, Section 7
Lab:	7
Title:	7 Segment Decoder
Student Name:	Barry Joseph Okonoboh
Due Date:	11:59:59 P.M., 23, March 2015
Instructor:	Dan Cregg

b. **Introduction.** This lab involves using logic gates to determine if a four bit unsigned number is a prime.

c. **Project Description.** The four bits of the number are mapped to four inputs A, B, C and D. If the number represented by the bits is true, then the output is 1; otherwise, it is 0. A Karnaugh map is used to simplify the equation and both the simplified and unsimplified equations are simultaneously tested using the Diligent board.

d. **Schematic.**


A
B
C
D
INV
INV
INV
INV
AND4
AND4
AND4
AND4
AND4
AND4
OR6
X
AND3
AND3
AND3
INV
OR4
Z

Truth Table.

A	B	C	D	ledA	ledB	ledC	ledD	ledE	ledF	ledG	ledEnable
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	0	1	1	1	1	0
0	0	1	0	0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0	1	1	0	0
0	1	0	0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	1	0	0	0
0	1	1	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	1	0	0	0	0
1	0	1	1	1	1	0	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1	0
1	1	0	1	1	0	0	0	0	1	0	0
1	1	1	0	0	1	1	0	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0	0