Class:	CECS 201, Section 7
Lab:	3
Title:	Logic Gates
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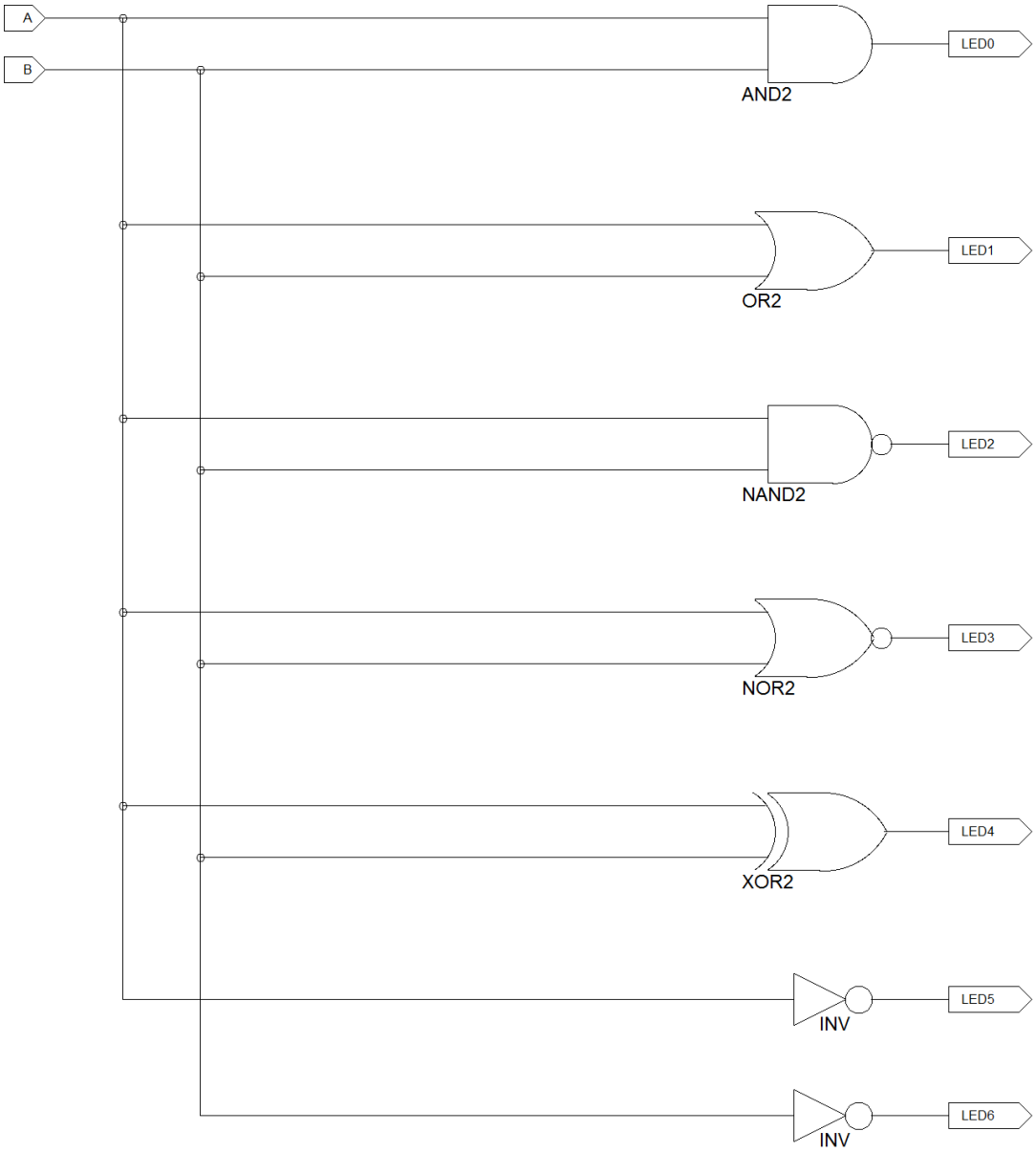
Due Date:	16, March 2015
Instructor:	Dan Cregg

b. **Introduction.** This lab involves observing the outputs of the AND, OR, NAND, NOR, NOT and XOR logic gates, with varying input.

c. **Project Description.** This lab has a single schematic that includes the six gates mentioned above. There are two inputs, A and B, and they are both connected to the inputs of all the gates. Each output of the gates in the schematic is mapped to exactly one LED, so that its behavior may be observed upon altering the inputs.

d. **Schematic.**



Truth Table.

A	B	AB	$A+B$	$\overline{AB}$	$\overline{A+B}$	$A \oplus B$	$\overline{A}$
0	0	0	0	1	1	0	1
0	1	0	1	1	0	1	1
1	0	0	1	1	0	1	0
1	1	1	1	0	0	0	0