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MIXED SIGNAL LETTER

An efficient approach to enhance bulk-driven amplifiers

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Abstract In this paper, a single-stage class AB bulk-driven amplifier operating in weak inversion region is proposed. The presented amplifier benefits from an improved high input swing structure using quasi-floating-gate technique. The composite transistors and recycling configuration used at the input stage enable the input differential pair to operate under low supply voltages with larger transconductance as compared to the conventional models at no expense of power budget. The circuit is designed in 0.18 µm CMOS technology and simulation results show 61.5 dB low frequency gain with the gain bandwidth of 30.15 kHz and 55.3 V/ms average slew rate. The total current of 275 nA and 0.6 V supply voltage make the proposed amplifier a suitable choice for ultra-low-power applications.

Keywords Weak inversion · Bulk driven · Quasi-floating gate · High input swing

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1 Introduction

In recent years, demand for portable systems has significantly increased and necessity of battery-operated systems working at low power supply voltages is observed more than ever. Besides, the decrease in supply voltage of interested circuits due to technology scaling, forces the circuits to operate at supply voltages in the range of 1 V or below [1, 2]. For instance, biomedical and sensor applications should operate at low power supply like 0.6 V due to their portability and environment limitations. Digital circuits are not the problem, for they can satisfy the low supply voltage conditions with existing techniques. However, the main concern comes from analog circuits. As compared to digital structure, the worsened analog properties of transistors in fine line CMOS technologies makes it difficult to design transconductors with high linearity, low noise and low power consumption. As feature size scales down, the intrinsic gain of transistors is decreased continuously [1–5].

Data converters encompass several analog building blocks including integrators, sample and hold circuits, and gain stages in which operational transconductance amplifiers (OTAs) are utilized. The accuracy, speed and distortion of analog to digital converters (ADCs) are strongly dependent on the low frequency gain, GBW, linearity and input noise of the employed OTA [5, 6]. The OTAs using conventional structures with lowered supply voltage suffer from threshold limitation and performance degradation such as signal to noise ratio and dynamic range. Although low-voltage analog circuit design can be achieved using low threshold voltage devices, it has found not to be a cost effective solution due to the requirement of nonstandard processes [6, 7]. Therefore, it is better to look for feasible techniques, such as bulk driven, floating gate and quasi-floating gate MOSFETs to overcome the threshold limitation

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[8–11]. Using these techniques to design low-voltage CMOS circuits are desirable, since a large input signal can be applied without cutting off the input transistors. It is noteworthy that the bulk-driven input differential pair suffers from lower (*gmb*/*gm*) ratio in CMOS technologies leading to a lower performance [1, 2]. Thus, new techniques to improve low frequency gain, GBW and slew rate are indispensable.

To enhance the transconductance of a conventional folded cascode (FC) structure, recycling topology [12, 13], additional drivers [14], current shunt technique [15, 16], positive feedback [17] and self-cascoding structures with new paths [17, 18] have already been used. These upgraded structures can be reconfigured again as bulk-driven topologies using composite transistors [2]. However, these modifications do not provide sufficient (*gmb*/*gm*) ratio especially at low supply voltages. Therefore, positive feedback source degeneration technique has been employed in [1] to enhance the efficiency of a weak-inversion FC amplifier. Moreover, the quasi-floating gate technique has been used in [19] to inject the input signal to the gate terminals of the source degenerated transistors. In fact, this technique helps bulk-driven input differential pair to employ gate's transconductance (*gm*) beside the bulk's transconductance (*gmb*) without degradation of the input dynamic range [8, 20]. The other interesting method is employing non-linear current sources as a tail current to increase output currents which charge and discharge load capacitors during slewing phase [21–23]. This method also enhances transconductance and slew rate that leads to higher low frequency gain, GBW, slew rate and lower input referred noise.

In this paper, a single stage bulk-driven current recycling structure with enhanced transconductance using quasi-floating-gate method is presented. The gate terminals of the input differential pair with two current sources are used as floating-gate transistors to increase the transconductance without decreasing the input swing due to its bulk-driven topology. These improvements lead to higher low frequency gain (for an accurate final value) and higher GBW and slew rate (for shorter settling time) while the input referred noise is significantly decreased because of higher transconductance. The remainder of the paper is organized as follows: Sect. 2 illustrates the proposed structure and compares it with the self-cascode and enhanced structures based on mathematical analyses for frequency and transient characteristics. Section 3 reports the simulation results of the designed amplifiers and finally, the conclusions are given in Sect. 4.

2 Proposed class AB structure

Among many OTA structures, the folded cascode (FC) topologies with pMOS input differential pair are often selected due to their lower flicker noise and ability to operate in low supply situation. The self-cascode FC amplifier which has been configured as a bulk-driven topology using composite transistors is shown in Fig. 1. According to analysis in [7], the composite transistors (M3/M5 and M4/M6 in Fig. 1) provide an independent node of the gate-source voltage that is very useful as a folded node in the rail-to-rail structures. This is because it helps the input differential pair to retain its drain voltage constant and consequently its transconductance when the circuit suffers from a large input swing.

In addition, to enhance the (*gmb*/*gm*) ratio of the conventional bulk-driven input differential pair, the enhanced folded cascode (EFC) structure has been presented in [2] which is shown in Fig. 2. For optimum utilization of the DC current through the transistors M3 and M4 in Fig. 2, an additional input differential pair M1b/M2b is used to employ M3 and M4 as new drivers. In order to apply input signal to the gates of the new drivers (M3 and M4), the other two composite transistors are used to create the required current mirrors M3b:M3 and M4b:M4. Thus, the input signal converts to current by M1b/M2b and goes through the new current mirrors to enhance transconductance using M3 and M4. Furthermore, two transistors M1c and M2c are used as current sources to provide the bias current of the cascode transistors M5b and M6b. The DC current of these transistors finally goes through M3b and M4b and emerges with small signal current which is coming from input. Therefore, it can decrease the transferred transconductance to the output node through the new paths. To compensate

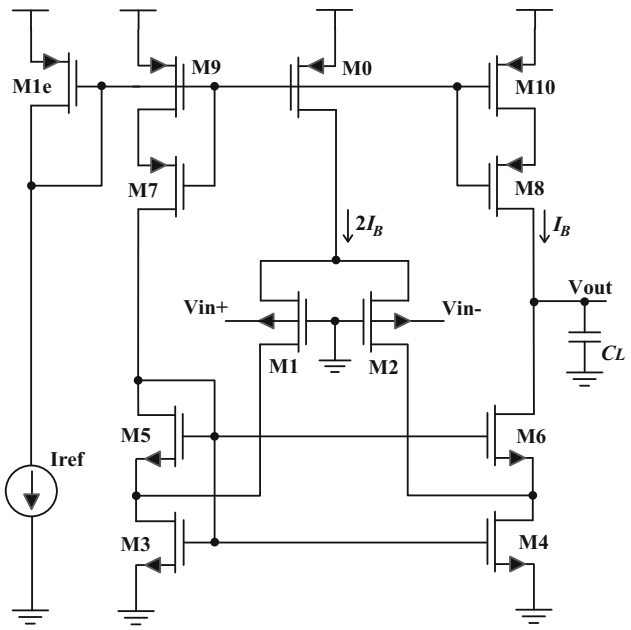

Fig. 1 Self-cascode FC amplifier

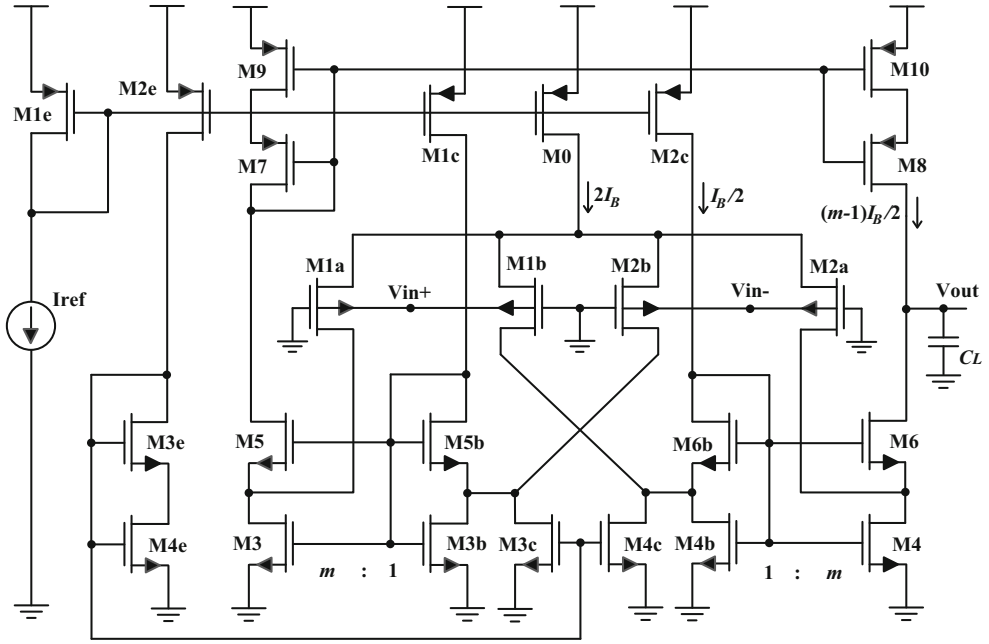

Fig. 2 Enhanced FC amplifier

such transconductance reduction, transistors M3c and M4c can be used as current shunt technique to steer the DC current of M5b and M6b and prevent combining small signal current with DC current. It's clear from Fig. 2 that the added transistors M3c and M4c need voltage bias leading to more power budget by transistors M2e–M4e. All of these improvements result an enhancement in the GBW and slew rate while the power budget is 20% more than the self-cascode FC structure.

The proposed folded cascode (PFC) amplifier that is upgraded using quasi-floating gate technique is shown in Fig. 3. The enhanced input differential pair is configured using four matched transistors M1a, M2a, M1b and M2b with equal size ratio. To enhance transconductance, the gate terminals of the input transistors are connected to their bulk terminals (input signal) through capacitors C_1 and C_2. These improvements are obtained by applying the input signal to both gate and bulk terminals of the input differential pair and consequently a significant enhancement in transconductance is achieved. In addition, the input signal can be applied to the gate terminals of transistors M1c and M2c that are working as current controller transistors. It also leads to transconductance improvement since these transistors can operate as a gate-driven common source amplifier. As a result, the transistors M3b and M4b steer a small signal current. Accordingly, to prevent extra power consumption, the transistors M3c and M4c and their bias circuit M2e–M4e from Fig. 2 can be removed in Fig. 3. It also leads to better phase margin for the proposed structure as compared to the enhanced one.

2.1 Small signal analysis

All transistors with floating gate need a bias for their gate which is provided by a large-valued resistor R_{Large}. Such resistors must be too large to prevent any attenuation from the input signal to the floating gates. They can be realized using several methods that have been presented in [24, 25], but the simple approach is employing a reverse-biased diode-connected pMOS transistor. Therefore, the role of the transistors M1d–M4d is to create a large-valued resistor for biasing floating gates of the enhanced transistors M1a–M2c. This technique creates a high-pass filter whose cutoff frequency is about

$$f_{cutoff} = \frac{1}{2\pi R_{Large} C_i} \tag{1}$$

where R_{Large} and C_i are the resistor realized by each M1d-M4d transistors, and each of the C_1–C_4 capacitors, respectively. Due to the use of a large resistor, the cutoff frequency can be transferred under 0.1 Hz to avoid frequency response limitation. In addition, the amplitude of the input signal referred to the floating gate through the capacitors C_i can be calculated by

$$A_G = A_B \times \frac{C_i}{C_i + C_G} \tag{2}$$

where A_G and A_B are the amplitude of the input signal at the gate and bulk nodes, respectively, and C_G is the gate capacitor of the input transistors. In practice, C_G can be neglected as compared to C_i, if C_i is selected much bigger

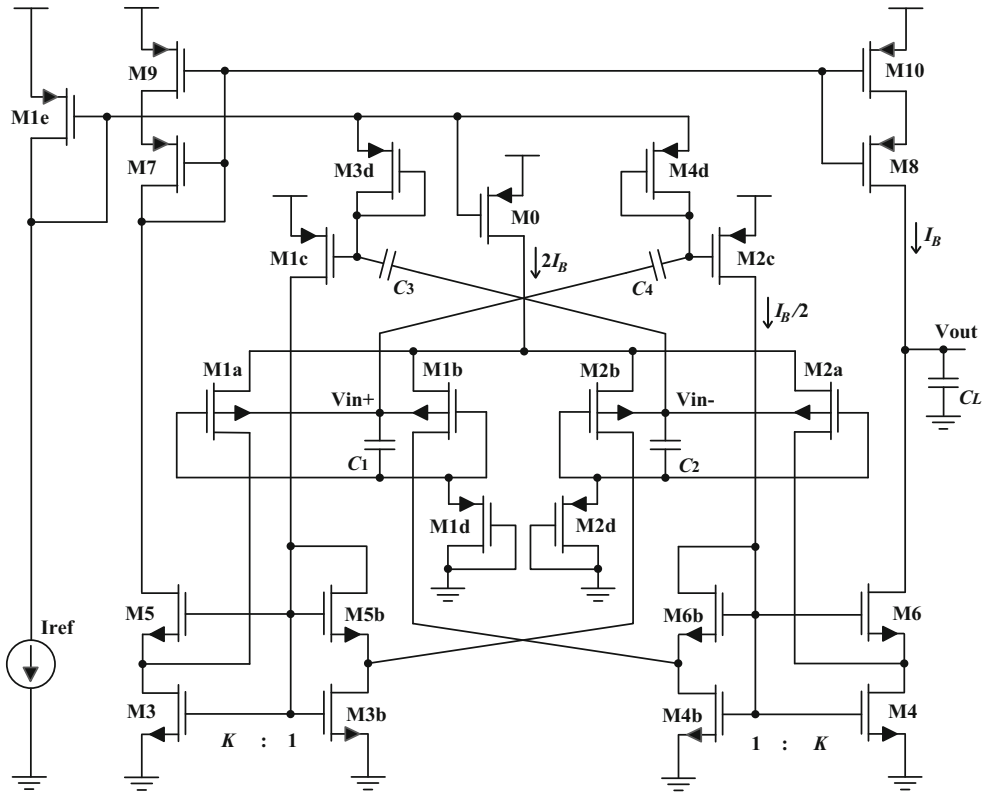

Fig. 3 Proposed FC amplifier

than C_G. Consequently, it can be mentioned that the bulk and gate nodes of a quasi-floating gate transistor are isolated from each other in terms of DC operation and are connected to each other in terms of AC operation. Thus, a high input swing can be observed for the proposed structure. According to the above discussions, and also as $gmb_1 = 2gmb_{1a}$ and $gm_{1a} = gm_{1c}$, the small signal transconductance of the self-cascode, enhanced and proposed FC structures can be given by

$$Gm_{FC} = gmb_1 = (2\eta)gm_{1a} \tag{3}$$

$$Gm_{EFC} = (1+m)gmb_{1a} = (\eta + \eta m)gm_{1a} \tag{4}$$

$$\begin{aligned} Gm_{PFC} &= (1+k)(gmb_{1a} + gm_{1a}) + kgm_{1c} \\ &= (1+\eta+\eta k+2k)gm_{1a} \end{aligned} \tag{5}$$

where gm and gmb are gate's and bulk's transconductances, respectively, η is the (gmb/gm) ratio, and m and k are the current gain factors of driver current mirrors M3b:M3 and M4b:M4 in Figs. 2, 3, respectively. By choosing $k = 1.5$ and $m = 3$ the power budget will be approximately the same for all structures. Given that η is about 0.3 in the working bias point, Eq. (5) shows 7.92 and 3.96 times enhancement in transconductance and consequently low frequency gain and GBW for the proposed amplifier over the self-cascode and enhanced amplifiers, respectively. The added capacitors C_1–C_4 increase die area of the proposed amplifier. Besides, for some cases that the amplifier has a high gain and the amplifier's speed is more important than the low frequency gain, the capacitors C_1–C_4 can be decreased.

2.2 Large signal analysis

The simplified large signal model of the proposed structure during slewing phase is shown in Fig. 4, when Vin+ is much greater than Vin−. Under this situation, a large positive voltage is coupled to the gate terminals of the transistors M1a, M1b and M2c by the floating capacitors C_1 and C_4. Thus, these transistors enter the cut-off region and their drain voltages decrease which force M4, M4b, M6 and M6b also to inter the cut-off region. On the other hand, a large negative voltage is coupled to the gate terminals of the transistors M2a, M2b and M1c through the floating capacitors C_2 and C_3. Besides, the transistor M2a enters to deep triode region due to increasing drain voltage of M4 and consequently its drain current significantly decreases. Therefore, the transistor M2b caries all the tail current ($2I_B$) into M3b. In addition, the other large current comes from M1c into M3b. Actually, the coupled negative large voltage to the gate of M1c significantly increases its

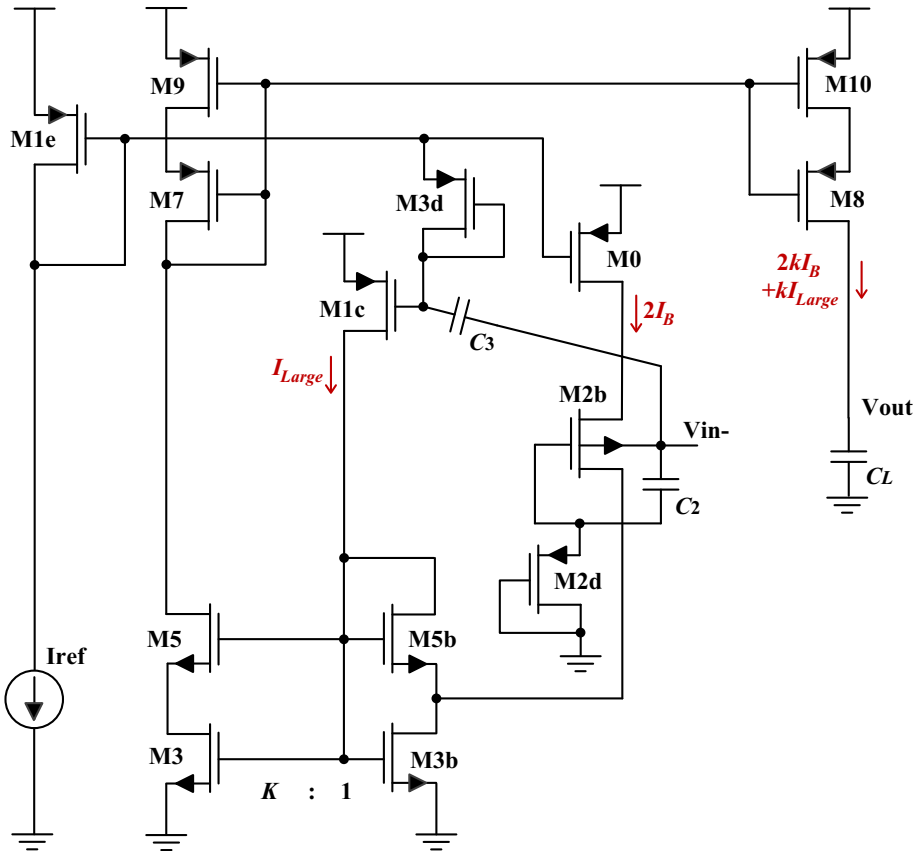

Fig. 4 Large signal model of the proposed FC amplifier during slewing phase

drain current which results in raising the gate voltages of transistors M3, M3b, M5 and M5b. Finally, the drain current of M3b mirrors into the load capacitor C_L by a ratio of k. Therefore, based on the above discussion and analyses in [4], the slew rate of three structures can be calculated by

$$SR_{FC} = \frac{(I_{D,1} - I_{D,2})}{C_L} \tag{6}$$

$$SR_{EFC} = \frac{(m+1)(I_{D,1a} - I_{D,2a})}{C_L} \tag{7}$$

$$SR_{PFC} = \frac{k(2I_B + I_{Large})}{C_L} \tag{8}$$

where $I_{D,1}$, $I_{D,2}$, $I_{D,1a}$ and $I_{D,2a}$ are the drain currents of transistors M1, M2, M1a and M2a, respectively. It is worth mentioning that in the self-cascode and enhanced structures all of the tail current never flows through one of the differential pair transistors during slewing phase. As the bulk voltage variations does not make a significant change in the drain current in contrast with floating gate which leads transistor to cut-off or triode regions. Therefore, the slew rate of a bulk-driven structure is calculated based on the difference between the drain current of the input transistors during slewing phase. However, I_{Large} in Eq. (8) shows a slew rate depended on the input signal amplitude which is resulted from a class AB configuration. This equation presents a significant improvement in the slew rate of the proposed structure as compared to the other bulk-driven structures.

2.3 Noise analysis

The noise current power referred to the drain of a MOS transistor is known by (9) that includes the thermal and flicker noise [2].

$$\overline{i_o^2} = \left[4K_B T\gamma gm + \frac{k_f gm^2}{C_{ox}LWf}\right] \tag{9}$$

where the symbols have their usual meanings as was stated in [2]. Based on the Eqs. (3)–(5), the input referred thermal noise of the three amplifiers can be simplified by Eqs. (10), (11) and (12).

$$\overline{V^2_{iT\ FC}} = \frac{8K_B T\gamma}{gmb_1}\left[1 + \frac{gm_3}{gmb_1} + \frac{gm_9}{gmb_1}\right] \tag{10}$$

$$\overline{V^2_{iT\ EFC}} = \frac{8K_B T\gamma}{(m+1)gmb_{1a}}\left[\frac{1+m^2}{m+1} + \frac{(3m+1)gm_3}{(m+1)gmb_{1a}} + \frac{gm_9}{(m+1)gmb_{1a}}\right] \tag{11}$$

$$\overline{V^2_{\substack{iT\\PFC}}} = \frac{8K_BT\gamma}{\left(1+k+\frac{1}{\eta}+\frac{2k}{\eta}\right)^2 gmb_{1a}} \times \left[\left(1+k^2\right)+(2k+1)\frac{gm_3}{gmb_{1a}}+\frac{gm_9}{gmb_{1a}}\right] \quad (12)$$

Given that $gmb_{1a} = gmb_1/2$, $gm_{3,PFC} = 3gm_{3,FC}/4$, $k = 1.5$, $m = 3$ and $\eta = 0.3$ the input referred thermal noise of the EFC and PFC amplifiers are derived in (13) and (14).

$$\overline{V^2_{\substack{iT\\EFC}}} = \frac{8K_BT\gamma}{gmb_1}\left[\frac{5}{4}+\frac{7.5}{4}\frac{gm_3}{gmb_1}+\frac{1}{4}\frac{gm_9}{gmb_1}\right] \quad (13)$$

$$\overline{V^2_{\substack{iT\\PFC}}} = \frac{8K_BT\gamma}{(5.6)^2 gmb_1}\left[\frac{3.25}{4}+\frac{gm_3}{gmb_1}+\frac{1}{4}\frac{gm_9}{gmb_1}\right] \quad (14)$$

Based on the weak inversion region's specifications [1] and assuming $\eta_n = \eta_p$, the input referred flicker noise expressions of the amplifiers can be expressed by

$$\overline{V^2_{\substack{if\\FC}}} = 2\frac{K_{Fp}}{\eta^2 C_{ox} f}\left[\frac{\eta^2}{(WL)_1}+\frac{K_{Fn}}{K_{Fp}}\frac{4}{(WL)_3}+\frac{1}{(WL)_9}\right] \quad (15)$$

$$\overline{V^2_{\substack{if\\EFC}}} = 2\frac{K_{Fp}}{\eta^2 C_{ox} f} \times \left[\frac{(1+m^2)\eta^2}{(m+1)^2(WL)_{1a}}+\frac{K_{Fn}}{K_{Fp}}\frac{m^2(2m+1)}{(m+1)^2(WL)_3}+\frac{(m-1)[m^2+(m-1)]}{(m+1)^2(WL)_9}\right] \quad (16)$$

$$\overline{V^2_{\substack{if\\PFC}}} = 2\frac{K_{Fp}}{\eta^2\left(1+k+\frac{1}{\eta}+\frac{2k}{\eta}\right)^2 C_{ox} f} \times \left[\frac{(1+k^2)\eta^2}{(WL)_{1a}}+\frac{K_{Fn}}{K_{Fp}}\frac{k^2(1+k)}{(WL)_3}+\frac{(k-1)(k^2)+(k-1)^2}{(WL)_9}\right] \quad (17)$$

By assuming that the channel length of devices are the same with their counterparts in all structures, and substituting W_1 in terms of W_{1a}, $W_{3,FC}$ in terms of $W_{3,PFC}$, the input referred flicker noise of the enhanced and proposed amplifiers are concluded in (18) and (19).

$$\overline{V^2_{\substack{if\\EFC}}} = 2\frac{K_{Fp}}{\eta^2 C_{ox} f}\left[\frac{5}{4}\frac{\eta^2}{(WL)_1}+\frac{21}{4}\frac{K_{Fn}}{K_{Fp}}\frac{1}{(WL)_3}+\frac{9}{4}\frac{1}{(WL)_9}\right] \quad (18)$$

$$\overline{V^2_{\substack{if\\PFC}}} = 2\frac{K_{Fp}}{\eta^2 C_{ox} f}\left[\frac{6.5}{(14.8)^2}\frac{\eta^2}{(WL)_1}+\frac{7.5}{(14.8)^2}\frac{K_{Fn}}{K_{Fp}}\frac{1}{(WL)_3}+\frac{1.38}{(14.8)^2}\frac{1}{(WL)_9}\right] \quad (19)$$

All terms in (19) and (14) are smaller than their counterparts in (18) and (13), respectively. Therefore, from the above equations it can be concluded that the proposed structure significantly reduces total input referred noise. This advantage makes the amplifier suitable for ultra-low-power and low-frequency applications. Besides, the die area of the proposed structure is increased due to the existence of four floating capacitors C_1–C_4.

3 Simulation results

In order to confirm the improved specifications of the proposed design, all of the self-cascode, enhanced and proposed FC amplifiers are simulated in 0.18 μm CMOS technology. The value of the supply voltage is set to 0.6 V, while all transistors operate in the weak inversion region. All of the three designs have the same quiescent bias current (I_{ref} = 25 nA). The load capacitor is equal to 12 pF and capacitors C_1–C_4 are considered 1 pF. The device sizes and other elements of the proposed amplifier are given in Table 1. Since the amplifiers are designed to work in low frequency applications, the size of transistors is considered to be large [2]. It is worth to mention that, beside this deficiency, transistor size has a reverse relationship with flicker noise.

The open-loop AC response is shown in Fig. 5. The low frequency gain of the self-cascode, enhanced and proposed amplifiers is 40.6, 50.2 and 61.5 dB, respectively. In addition, thanks to the transconductance enhancement, the GBW of the proposed OTA reaches to 30.15 kHz, while the self-cascode and enhanced OTAs are 4.38 and 8.22 kHz, respectively. Furthermore, the phase margin of the self-cascode, enhanced and proposed amplifiers are

Table 1 Device sizes (μm) and other elements of the designed amplifiers

Parameter	Self-cascode	Enhanced	Proposed
$(W/L)_{1e,2e}$	1 × 28.4/4	1 × 28.4/4	1 × 28.4/4
$(W/L)_0$	4 × 28.4/4	4 × 28.4/4	4 × 28.4/4
$(W/L)_{1,2}$	6 × 54.4/1	–	–
$(W/L)_{1a,2a}$	–	3 × 54.4/1	3 × 54.4/1
$(W/L)_{1b,2b}$	–	3 × 54.4/1	3 × 54.4/1
$(W/L)_{1c,2c}$	–	1 × 28.4/4	1 × 28.4/4
$(W/L)_{1d–4d}$	–	–	1 × 0.25/19
$(W/L)_{3,4}$	4 × 34.7/4	3 × 34.7/4	3 × 34.7/4
$(W/L)_{3b,4b}$	–	1 × 34.7/4	2 × 34.7/4
$(W/L)_{3c,4c,4e}$	–	1 × 34.7/4	–
$(W/L)_{5,6}$	4 × 56.5/1	4 × 56.5/1	4 × 56.5/1
$(W/L)_{5b,6b,3e}$	–	2 × 56.5/1	2 × 56.5/1
$(W/L)_{7,8}$	2 × 71/1	2 × 71/1	2 × 71/1
$(W/L)_{9,10}$	1 × 63.5/4	1 × 63.5/4	1 × 63.5/4
C_L	12 pF	12 pF	12 pF
$C_{1–4}$	–	–	1 pF
I_{ref}	25 nA	25 nA	25 nA

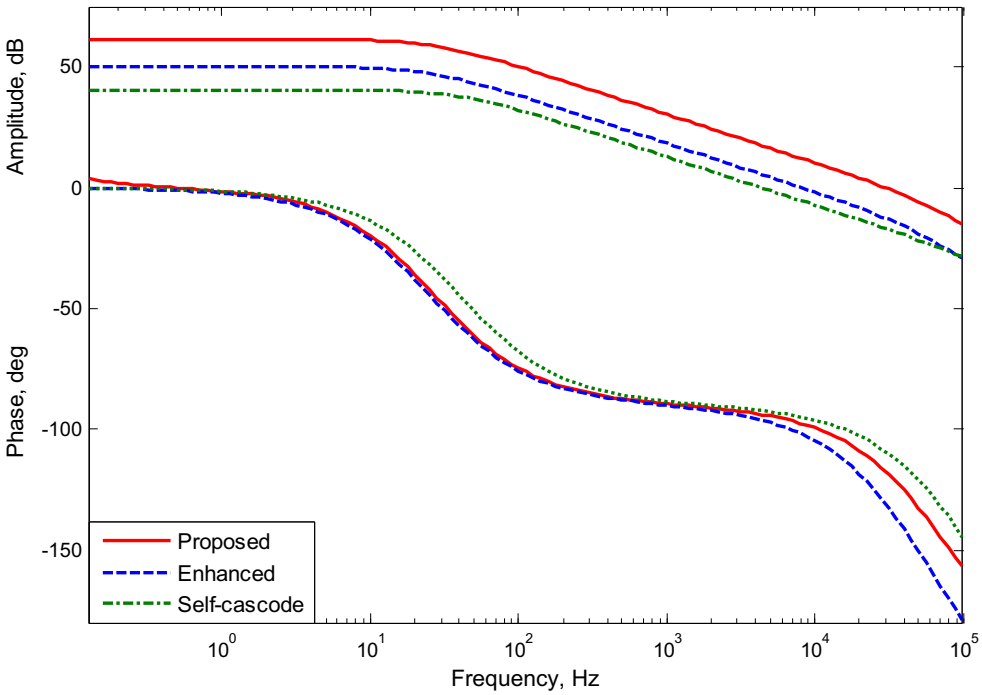

Fig. 5 Open loop frequency response of the designed amplifiers

87.2°, 78.1°, and 62.45°, respectively. Compared to the enhanced OTA, the phase margin of the proposed amplifier shows 15.65° degradation. Therefore, improvement of GBW and low frequency gain is achieved with degradation of the phase margin. In addition, it is clear that the cutoff frequency described in Eq. (1) is transferred under 0.1 Hz because of employing large resistors and floating capacitors.

To study the settling time and slew rate behavior, a large step of 0.4 V at frequency of 2.5 kHz is generated and all three amplifiers are utilized as a voltage follower configuration that is shown in Fig. 6. The large signal transient response of the designed amplifiers is shown in Fig. 7. It indicates that the transient response of the proposed amplifier has significantly improved compared with two others. The 0.1% positive settling time for the self-cascode and enhanced OTAs is respectively 273 and 119 μs. This value for the proposed OTA reaches to 23 μs that indicates a 417% improvement in comparison with the enhanced OTA. For the self-cascode, enhanced and proposed designs, the average slew rate is 3.2, 7.2, and 55.3 V/ms, respectively. In other words, the proposed OTA's slew rate is almost 7.7 times that of the enhanced OTA.

To verify the maximum input/output swing a sinusoidal wave with 0.4 V_{PP} amplitude at 100 Hz is applied to the proposed OTA in a voltage follower configuration and results are shown in Fig. 8. The input swing will not face any limitation owing to the bulk-driven and floating gate techniques utilized at the input. Besides, because of the

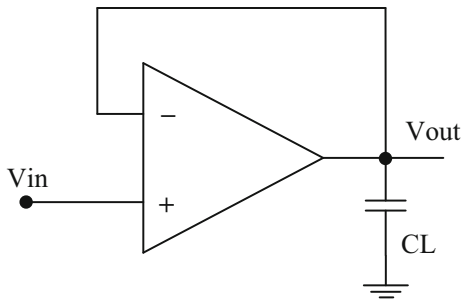

Fig. 6 Voltage follower configuration

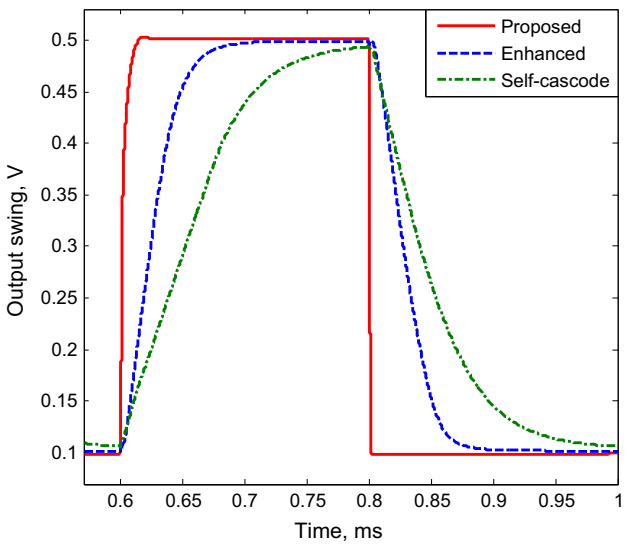

Fig. 7 Large step response of the designed amplifiers

cascode structure, the output swing is limited on 0.4 V_{pp} swing for 0.12% total harmonic distortion (THD). Therefore, it can be mentioned that the linearity of the proposed structure is not degenerated despite the use of quasi-floating gate method. Nonetheless, the bulk-driven input differential pairs suffer from input current due to the leakage currents through the bulk terminal especially for large input signals. In other words, the source-bulk PN junction of the input drivers M1a, M2a, M1b and M2b are biased in the forward region (in the weak inversion) when the bulk voltage (N region) is lower than the source voltage (P region). Simulation results show a 161 pA input current for the proposed amplifier when the input voltage reaches to zero. To reduce such leakage currents, some layout and fabrication approaches presented in [4, 11, 26] must be used. In addition, the leakage currents through transistors M1d–M4d that play role of large resistors can increase the input offset. This effect can be also reduced by employing chopping technique [27, 28] and some efficient structures as large resistors presented in [24, 25]. Nonetheless, the measured input offset of the proposed amplifier is 7.2 mV.

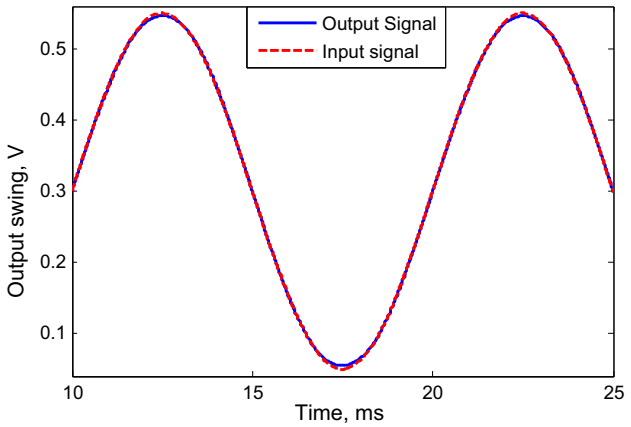

Fig. 8 The input and output waveforms of the proposed amplifier with maximum input/output swing

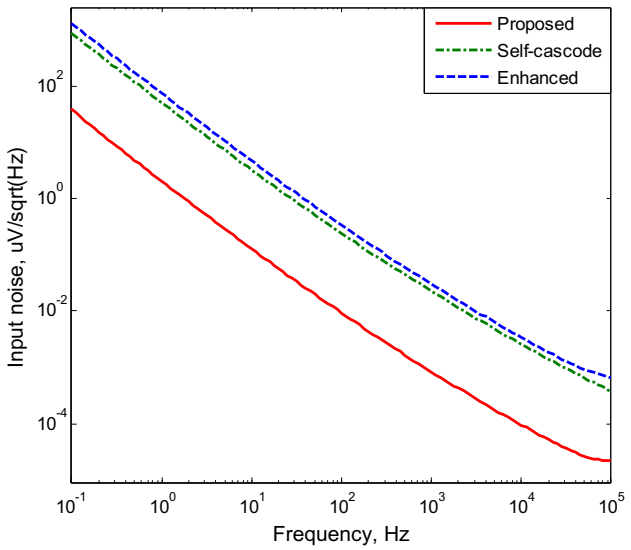

Fig. 9 Input referred noise for all designed amplifiers

Figure 9 shows the input referred noise for three considered designs. The input referred noise @ 0.1 Hz for the self-cascode, enhanced and proposed OTAs are 29.2, 35.6 and 6.25 $\mu V/\sqrt{Hz}$, respectively, which shows noise performance improvement in the proposed design. This result is consistent with the Eqs. (14) and (19) that were previously explained.

Mismatch and process variations have a direct impact on the major design factors of a circuit. For the proposed design, Monte-Carlo analysis, corner analysis and supply variations effects are studied considering their influence on GBW, phase margin, low frequency gain and positive settling time. The results are listed in Table 2. Based on the Gaussian distribution, Monte-Carlo analysis with standard deviation of MOS dimension (W, L), threshold voltage and floating capacitors in 0.18 µm CMOS technology was performed. The results for 1000 runs are demonstrated in Fig. 10. According to the results, the considered factors of the proposed OTA do not experience substantial changes over process variations. Because the size of transistors are considered to be large and the proposed OTA has a self-biasing topology. In addition, the corner analysis and supply voltage variations (around 20% of the V_{DD}) do not have also a significant effect on the considered factors of the proposed design.

Table 2 Important specifications of the proposed amplifier in Monte-Carlo analysis, process corners and power supply variations

Parameter	Corner analysis				Supply variation		Monte-Carlo analysis	
	SF	FF	SS	FS	V_{DD} − 20%	V_{DD} + 20%	Average	SD
Unity gain bandwidth (kHz)	30.23	30.3	30	30	29.8	30.4	31.15	0.49
Phase margin (°)	62.44	62.4	62.66	62.63	62.6	62.38	62.4	0.51
Low frequency gain (dB)	61.2	60.9	59.8	59.5	54.9	63	60.3	1.16
Average slew rate (V/ms)	57.9	52.1	59.3	56.7	51.3	58.6	55.7	0.91
0.1% settling time (t_{s+}/t_{s-}) (µs)	24/15	20/12	17/14	25/11	15/10	22/13	23/13.3	0.61/0.54

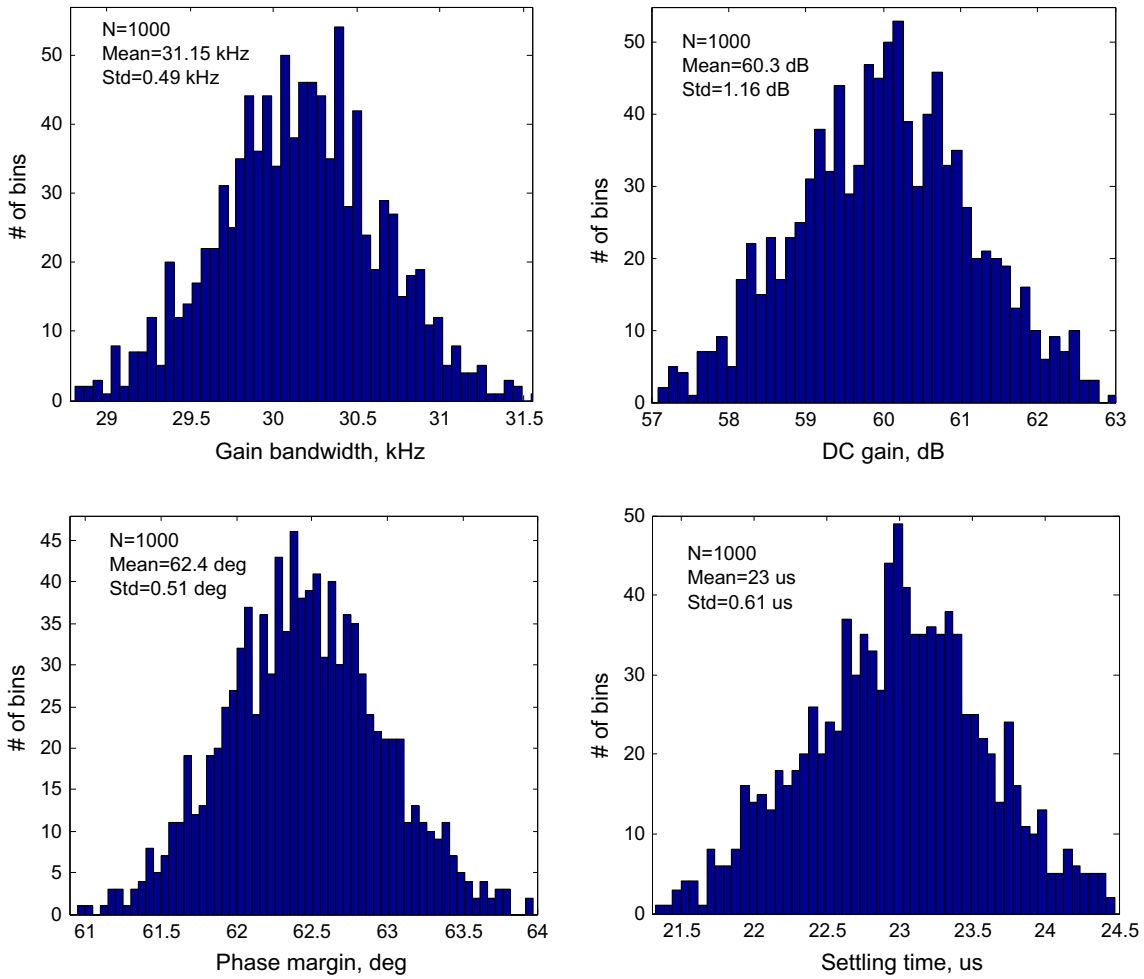

Fig. 10 Monte-Carlo simulation results of the proposed amplifier

Table 3 Specifications of the proposed OTA in comparison with the other works

Parameter	Self-cascode	Enhanced	Proposed	[1]	[2]	[18]
Power supply (V)	0.6	0.6	0.6	0.25	0.6	0.5
Technology (μm)	0.18	0.18	0.18	0.13	0.18	0.18
Power dissipation (nW)	150	180	165	18	400	26
Capacitive load (pF)	12	12	12	15	15	15
GBW (kHz)	4.38	8.22	30.15	1.88	19.1	3.26
Phase margin (°)	87.2	78.1	62.45	52.5	60	68.9
PSRR @ 10 Hz	103.3	50.3	67.9	–	–	–
Low frequency gain (dB)	40.6	50.2	61.5	60	82	67.8
Average slew rate (V/ms)	3.2	7.2	55.3	0.7	12	0.72
0.1% settling time (t_{s+}/t_{s-}) (μs)	273/255	119/112	23/13	–	75	–
THD @ 100 Hz (400 mV_{pp}) (%)	0.69	0.36	0.12	–	0.16	–
Maximum input/output signal swing (mV)	600/400	600/400	600/400	250/150	600/500	500/400
Input referred noise @ 0.1 Hz ($\mu V/\sqrt{Hz}$)	29.2	35.6	6.25	20	–	–
Maximum input current (pA)	154	152	161	3	–	–
Input offset (mV)	2.9	2.7	7.2	2.8	–	6.8
FOM_1 (kHz × pF/nW)	0.35	0.55	2.2	1.56	0.71	1.88
FOM_2 (V/ms) × pF/nW)	0.26	0.48	4	0.58	0.45	0.42

To compare the proposed amplifier with the other designed counterparts, two figures of merit (FOM) have been defined in Eqs. (20) and (21). Finally, the intended factors along with the comparison results are summarized in Table 3.

$$FoM_1 = \frac{(GBW)(C_L)}{Power\ dissipation} \tag{20}$$

$$FoM_2 = \frac{(Slew\ rate)(C_L)}{Power\ dissipation} \tag{21}$$

4 Conclusion

A single-stage class AB bulk-driven amplifier with enhanced transconductance is proposed. Utilizing composite transistors and bulk-driven technique lead to a stabilized rail-to-rail input swing. In addition, thanks to the quasi-floating gate and recycling configuration, the transconductance has been significantly improved. Simulation results in 0.18 μm CMOS technology shows that the proposed OTA improves 588% GBW, 20.9 dB low frequency gain and 1630% slew rate over the self-cascode OTA, with just 10% expense in power budget.

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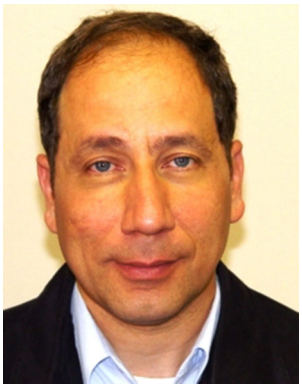

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