Design and Analysis of Low Noise Optimization Amplifier Using Reconfigurable Slotted Patch Antenna

Article *in* Wireless Personal Communications · August 2017

DOI: 10.1007/s11277-017-4774-2

6 authors, including:

sandeep kumar
Inje University
19 PUBLICATIONS **10** CITATIONS
SEE PROFILE

Binod K. Kanaujia
Jawaharlal Nehru University
167 PUBLICATIONS **548** CITATIONS
SEE PROFILE

Wireless Pers Commun
DOI 10.1007/s11277-017-4774-2

Design and Analysis of Low Noise Optimization Amplifier Using Reconfigurable Slotted Patch Antenna

Sandeep Kumar[1] · Binod Kumar Kanaujia[2] · Santanu Dwari[3] · Ganga Prasad Pandey[4] · Dinesh Kumar Singh[5] · Anil Kumar Gautam[6]

Abstract This paper approaches a novel design theory of Low noise amplifier using reconfigurable rectangular shaped slotted patch antenna for 10.3–14 GHz receiver applications. In this approach, a Berkeley short-channel4 metal oxide field effect transistor (BSIM4, MOSFET) device is loaded in rectangular slotted patch antenna which results in wide band frequency of operation. To understand the design and analysis of low noise amplifier, an equivalent circuit model is extracted from the rectangular slotted patch

✉ Binod Kumar Kanaujia
bkkanaujia@ieee.org

Sandeep Kumar
fedrer.engg@gmail.com

Santanu Dwari
santanu_dwari@rediffmail.com

Ganga Prasad Pandey
ganga.mait@gmail.com

Dinesh Kumar Singh
dinesh12dk@gmail.com

Anil Kumar Gautam
gautam1575@yahoo.co.in

[1] Department of Nano-science and Engineering, Center for Nano Manufacturing, Inje University, Gimhae 621-749, Republic of Korea

[2] School of Computational ad Integrative Sciences, JawaharLal Nehru University, New Delhi 110067, Delhi, India

[3] Department of Electronics Engineering, IIT (ISM), Dhanbad 826004, Jharkhand, India

[4] Department of Information and Communication Technology, Pandit Deendayal Petroleum University, Gandhinagar, Gujarat, India

[5] Department of Electronics and Communication, G L Bajaj Institute of Technology and Management, Greater Noida, UP, India

[6] School of Information and Communication Technology, Gautam Budh University, Greater Noida, UP, India

Published online: 07 August 2017

antenna using finite element method (FEM) simulator where the slotted effect is considered. An extraction of equivalent model from the slotted patch antenna results in the L–C circuit which is used to perform an impedance transformation for low noise amplifier. A 12 GHz low noise amplifier using L–C circuit can improve performance parameters as per designer's requirement. A reconfigurable MOS loaded slotted patch antenna is verified using momentum microwave simulator and a wide bandwidth of 9 GHz in the frequency range of 10.3–19.3 GHz is achieved. The Low noise amplifier is simulated with TSMC 0.09 μm mixed signal/RF CMOS process technology. The post-layout circuit simulation results show that the proposed common source LNA with L–C network achieves a maximum power gain of 20 dB with the −3 dB bandwidth from the range of 10.3–13.6 GHz. A reflection coefficient of −14 dB and minimum noise figure of 1.6 dB is achieved. The power dissipation is 2.5 mW at 1.2 V supply voltage.

Keywords Low noise amplifier · Slotted antenna · Reconfigurable · CMOS

1 Introduction

In the last few years, reconfigurable slotted antennas have become attractive design approach which is alternative to the fixed antenna as it provides controllable radiating properties such as resonance and bandwidth for various wireless applications. A feature of switchable frequency bands is typically achieved through a varactor diode or tuned capacitance and tunable combination of reactance which is offered by the RF diodes [1, 2]. Frequency reconfigurable antennas are capable of changing their resonant frequency to operate at specific band along with the multi-serviced radio spectrum. Such capability is also of interest for cognitive radio systems [3]. Significant advancements on frequency agile antennas were reported in the last few decades, such as in [4–6]. In [4, 5] the patch antenna radiating edges are loaded with varactor diodes to allow for electronic tuning, whereas in [6] a PIN diode switch controls the length of the current path on the patch surface, producing frequency reconfigurability. In [7–9], Pues et al. established one popular model that is the microstrip transmission line model (TLM) which can be evaluated from patch antenna designs. While a quick and easy model to construct with any mathematics software package, the TLM given by Pues is symmetry bound, meaning that the feed as well as any additional components must lie on the midline of the patch antenna.

The complementary metal oxide semiconductor (CMOS) technology is still considered as attractive choice due to its numerous advantages like low cost, small size, low power consumption and high level of integration. Despite of having several advantages, the design of low noise amplifier (LNA) using CMOS for receiver applications faces many challenges and difficulties which need to be overcome [10]. A number of LNA's based on CMOS technologies have also been reported by earlier authors. The 40-GHz three-stage cascaded TFMS tuned amplifier using 0.18 μm CMOS technology demonstrates a peak gain of 7 dB [11]. The 0.13 μm CMOS coplanar waveguide (CPW) amplifier with three-stage cascaded configuration achieves a peak gain of 19 dB at 40-GHz [12]. The noise optimization technique used for CMOS LNA with on-chip low Q inductors at 10-GHz obtains 12.93 dB gain but loses the reverse isolation parameters [13]. The author needs to pay more attention to NF, gain and reverse isolation while designing an LNA. The integration of MURATA pass-band filter with patch antenna at 10-GHz achieves a return loss of 24 dB [14]. A reconfigurable Varactor loaded slot patch antenna achieved dual band frequency of operation in 2 to 4.5 GHz [15].

In this performance, a low noise amplifier (LNA) is designed using L–C circuit extracted from the reconfigurable slotted patch antenna resulting in a wide band frequency of operation. This CMOS LNA achieves 3 GHz wide bandwidth with low optimized noise figure. Section 2 describes MOS loaded slotted patch antenna design consideration. Analysis and design of CMOS LNA using extracted L–C matching network are presented in Sect. 3, the results are discussed in Sect. 4, and these are followed by conclusions in Sect. 5.

2 MOS Loaded Slotted Patch Antenna Design Consideration

2.1 MOS Loaded Rectangular Slot Patch Antenna Structure

The basic structures of the MOS loaded slotted rectangular shaped patch antenna are shown in Fig. 1. All the structures are of a coaxial feed with a rectangular slot cut on the patch surface. The rectangular patch has the dimensions of length and width as 19 mm × 19 mm and is supported by a dielectric substrate of RT duriod 5880 of permittivity $\varepsilon_r = 2.2$, thickness $h = 3.175$ mm, and loss tangent $\tan\delta = .0009$. The slot on the patch surface is shown in Fig. 1 (i) where L_s' and W_s' are 10 mm and 1 mm respectively. The patch is fed by coaxial fed probe at a distance L'' of 4.3 mm from the left edge of the patch and w''' of 6.5 mm from lower edge of the patch. The other dimensions of patch antenna are $w' = 38$ mm, $L' = 38$ mm, $w'' = 15.7$ mm, $w_1 = 11.9$ mm and $w_2 = 8.3$ mm. The slot is loaded with a BSIM4 MOS model whose length is taken as .09 μm and width is calculated as 126 μm using the equation as given in (1). Here C_{ox} is the gate oxide capacitance, C_{gs} is the gate source capacitance and L_{min} is the channel length.

$$W = \frac{3}{2}\frac{c_{gs}}{L_{\min} c_{ox}} \tag{1}$$

In rectangular patch antenna, three slots are cut on patch surface with a single MOS device across each gap. The MOS model is embedded on each slot of patch surface to control the current path length with proper bias application. To build the DC biasing circuit, two ports are applied on gate and drain terminals of MOS device while source is grounded. The real time behavior of MOS device is drawn from two capacitances mainly naming C_{gs} (gate to source) and C_{ds} (drain to source) when biasing network is applied. These capacitances show tuning characteristics in the frequency band of operation for slotted microstrip antenna. In addition, a slit of length 0.2 mm is also cut on the patch to provide d.c isolation between the gate and grain voltages. The simulation behavior and resonance mechanism is discussed in next subsection.

2.2 Simulation Modeling and Resonance Mechanism

A momentum microwave (MM) simulator is performed using Agilent Technologies' advanced design system in order to predict the performance of MOS loaded slot patch antenna. A simple rectangular patch antenna is designed at 10 GHz and simulation, achieves the return loss of −14 dB within frequency range of 9.5–10.3 GHz. As one rectangular slot is cut on patch, the current path of slot elements changes and due to which lower and upper bands are affected. The two resonating frequencies of 11.6 and 14.6 GHz with wide bandwidth of 6.5 GHz in the frequency range of 11–17.5 GHz have been

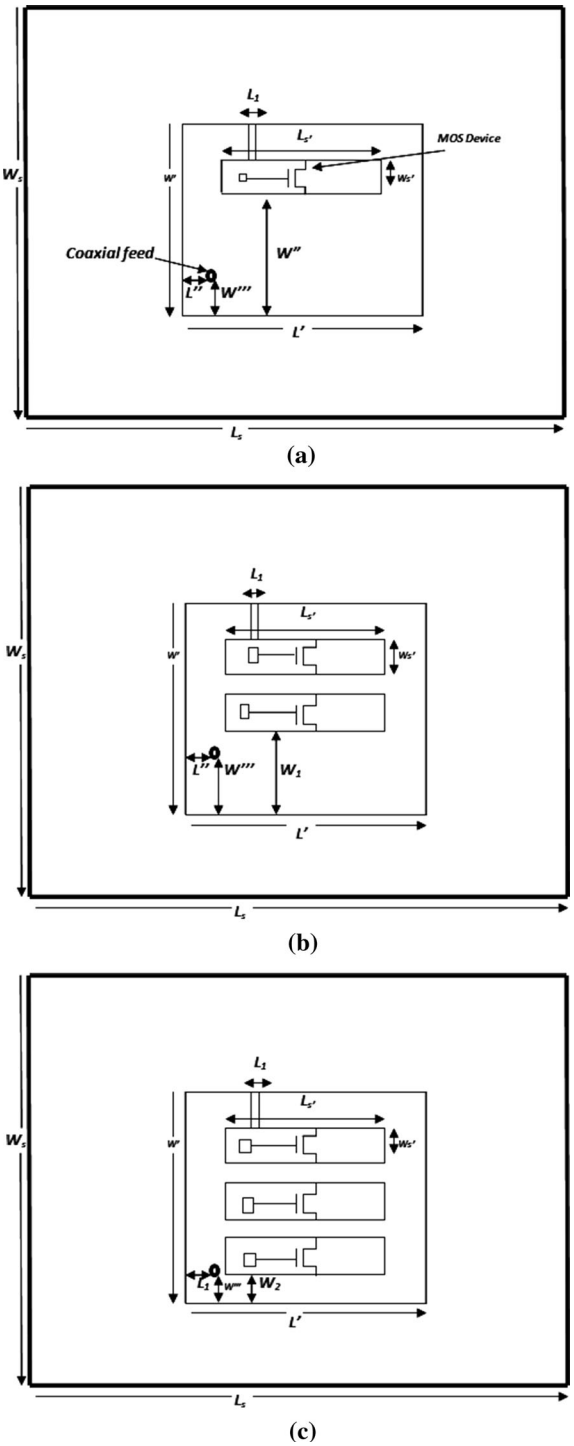

Fig. 1 Slotted rectangular patch antenna geometries with **a** One MOS load **b** Two MOS load **c** Three MOS load

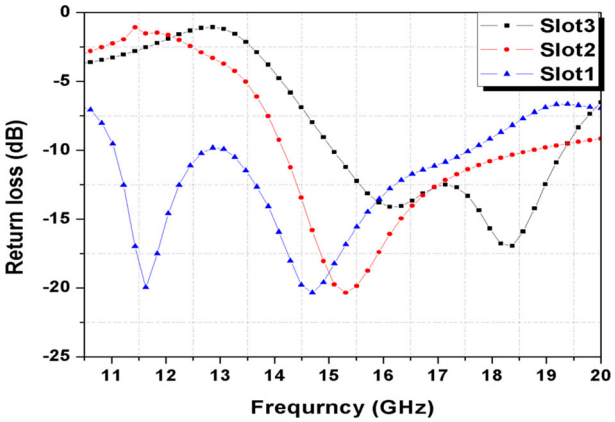

Fig. 2 Variation of return loss with frequency of the proposed antenna without MOS

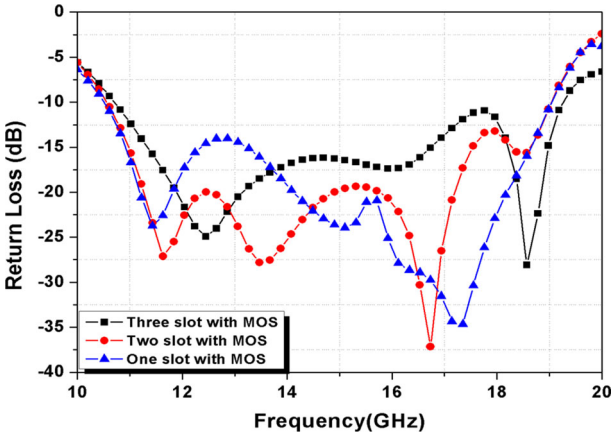

Fig. 3 Variation of return loss with frequency with MOS devices

achieved. This wide band response is reduced by 1.8 GHz when second and third rectangular slots of same dimensions as of first have been added on the patch surface which can be seen in Fig. 2. The return loss of rectangular slots patch antenna without loaded MOS devices gives impedance bandwidth of 6.5, 4.4 and 4.3 GHz respectively. To better understand the reconfigurable wide band mechanism of the proposed antenna, MOS devices is used in each slot on the patch surface. As shown in Fig. 3, it is observed that by adding MOS devices with proper DC biasing, much wider bandwidth could be achieved. By applying one BSIM4 MOS model on first slot in the patch, two resonating frequencies are shifted on lower and upper side within wide band range of 10.3–19 GHz. By embedding MOS in one slot in the patch, impedance bandwidth is enhanced by approx 2.2 GHz with resonating frequencies of 11.4 and 17.3 GHz respectively. Now, when a MOS is added on second slot on the patch, four resonating frequencies as 11.6, 13.4, 16.7 and 18.5 GHz are excited with much wider bandwidth of 8.8 GHz. In the similar way while applying MOS on third slot, more than 9 GHz bandwidth could be achieved. From the above given data, it reveals that at the lower frequency, the current distribution is

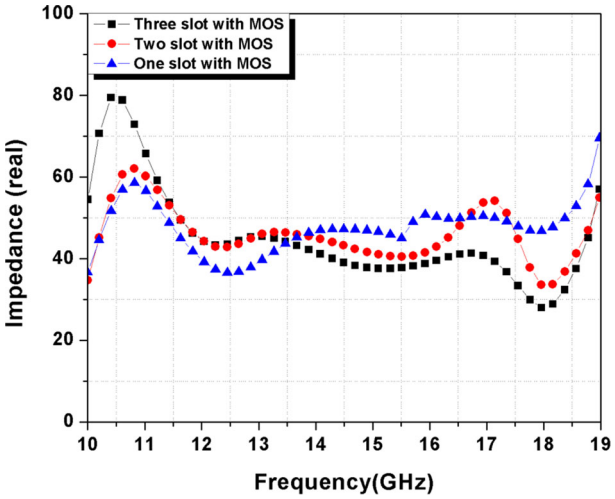

Fig. 4 Variation of real impedance with frequency

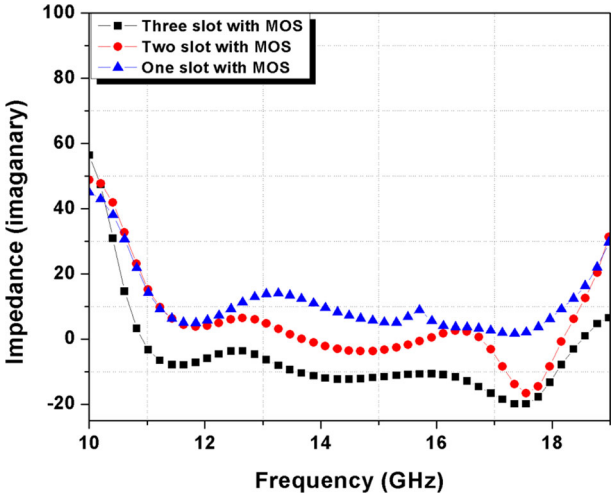

Fig. 5 Variation of imaginary impedance with the frequency

similar to the one of a plain patch but it diverts around the slot where the current path becomes longer. This reason explains why the first frequency is lower than the original resonant frequency. At the higher frequency, the current passes through the MOS device in the middle of the slot. Thus the lumped capacitors are equivalently seen in series with the antenna capacitance, reducing its overall value, and hence the second frequency is higher than the original resonant frequency. Moreover, shifted frequencies on the lower and upper side within desired frequency of operation also indicate the feature of reconfigurability. The real and imaginary impedance of MOS loaded slot patch antenna achieves approx $(50 + j0)\Omega$ condition within desired band of frequency as shown in Figs. 4 and 5 respectively. The far fields in polar plot form of the proposed antenna without MOS are

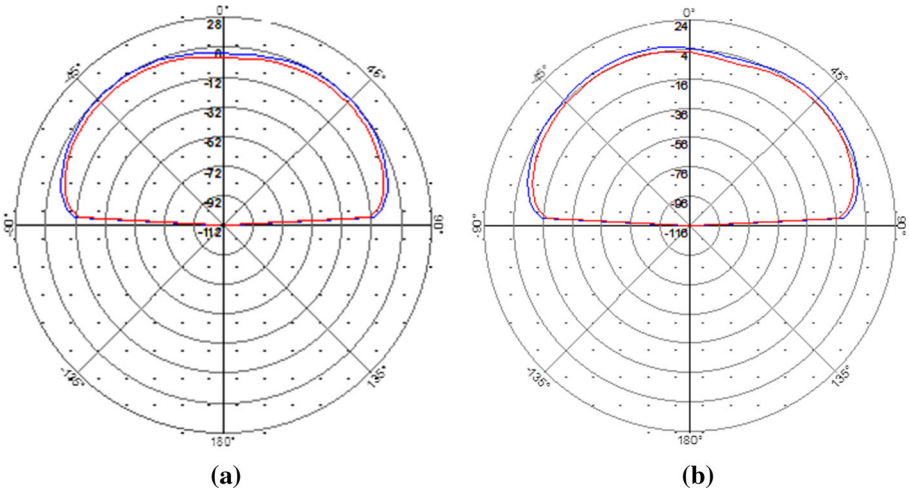

Fig. 6 Variation of gain and directivity of proposed antenna when theta rotates −90° to 90° at resonating frequencies of **a** 11.6 GHz and **b** 14.6 GHz

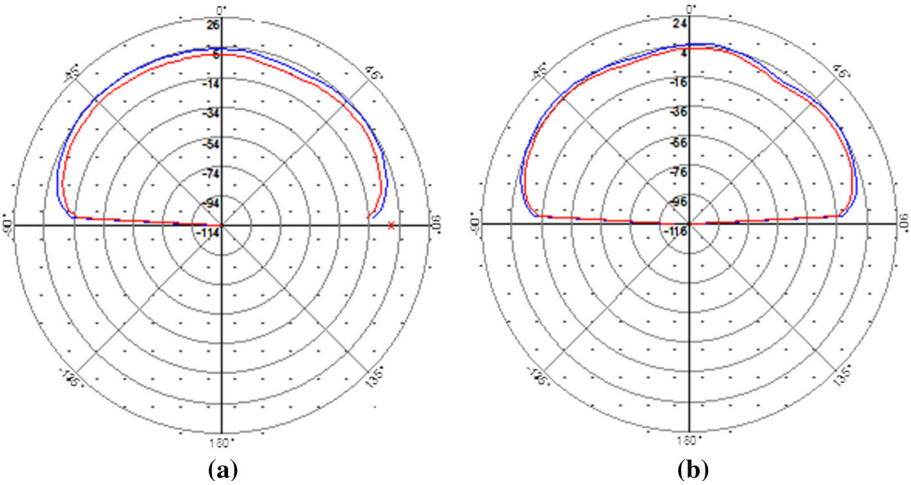

Fig. 7 Variation of gain and directivity of proposed antenna when theta rotates −90° to 90° at resonating frequencies of **a** 15.3 GHz and **b** 16.2 GHz

shown from Figs. 6, 7 and 8. As shown in Fig. 6, 0° axes which are perpendicular to the top face of the antenna show the gain and the directivity within the range of −20 dB when theta rotates from −90° to +90°.

2.3 Extracted L–C Circuit Model Analysis

Figure 9 show an equivalent model of rectangular slotted patch antenna which is extracted with the help of electromagnetic (EM) software package in ADS. The equivalent model consists of two capacitors (C_1 and C_2) which are connected in parallel with an inductor

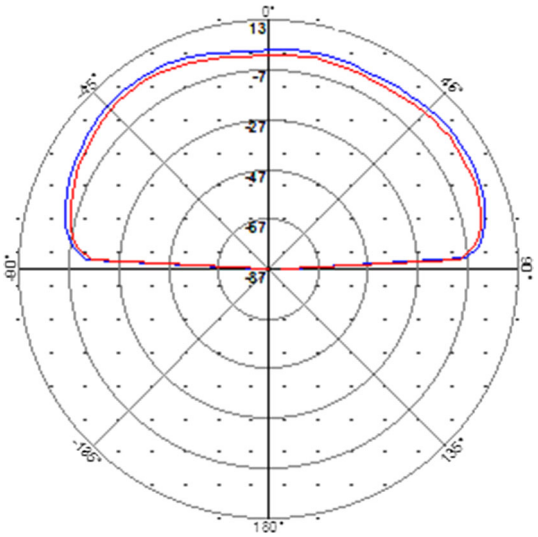

Fig. 8 Variation of gain and directivity of proposed antenna when theta rotates −90° to 90° at resonating frequency of 18.3 GHz

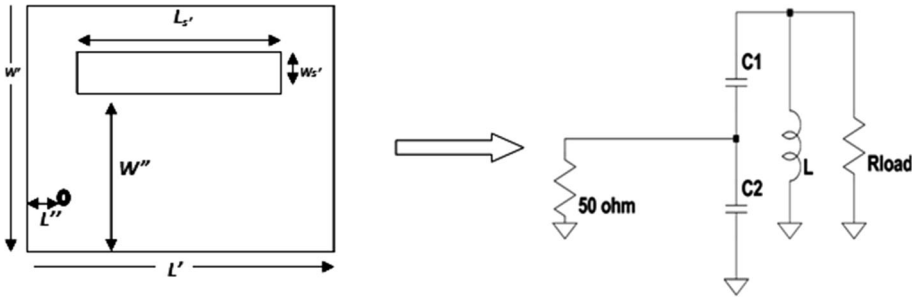

Fig. 9 Equivalent model of proposed rectangular slotted patch antenna i.e. L–C circuit

(L) resulting in an L–C circuit. The source of 50 Ω in L–C network is represented by coaxial feed probe. To better understand the extracted model, a rectangular slot patch antenna is further divided into individual C circuit and L circuit respectively and can be seen in Fig. 10. The approximate equivalent circuit of extracted L–C model is shown in Fig. 11.

From these individual circuits, R_s' for C and L circuit is given as in Eqs. (2) and (3) respectively.

$$R_s' = R_s\left(\frac{C_1}{C_2}\right)^2 \tag{2}$$

$$R_s' = R_s\left(\frac{m}{m_1}\right)^2 \tag{3}$$

The equivalent capacitance (CT') will resonate with inductor in parallel with C_1 in series with C_2 and shown in Eq. (4).

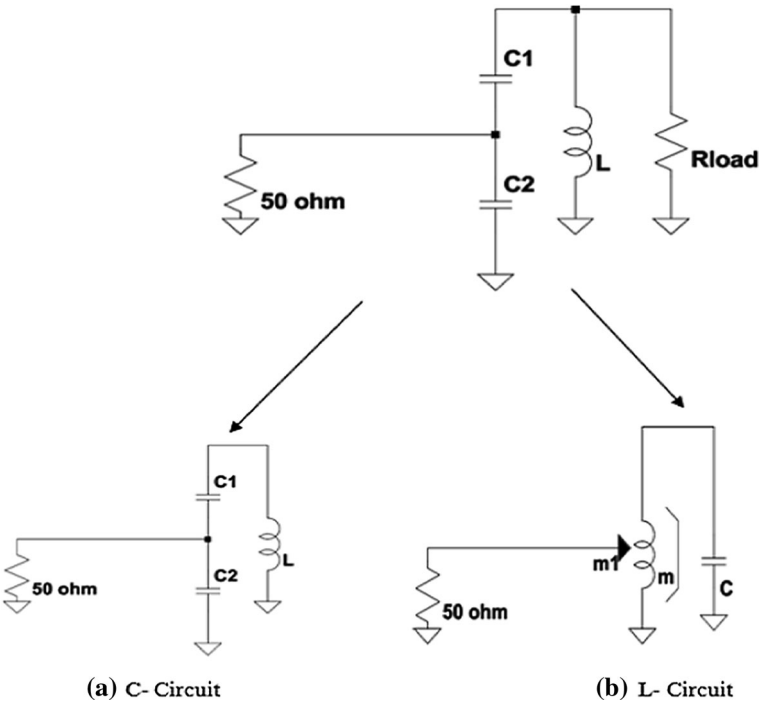

Fig. 10 Equivalent model breaks into individual L- and C-circuit

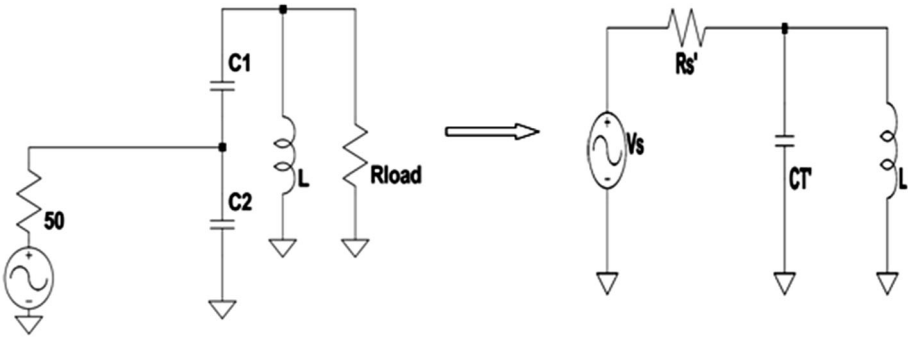

Fig. 11 Approximated equivalent model of extracted L–C circuit

$$CT' = \frac{C_1 C_2}{C_1 + C_2} \tag{4}$$

The calculated values of components for equivalent model of slot patch antenna are analyzed and simulated in ADS software which achieves wide bandwidth of around 9.7 GHz within the band range of 10.7–19 GHz as seen in Fig. 12. From this figure it is observed that first resonant frequency i.e. 11.6 GHz is same as first resonant of one slotted patch antenna while second resonant frequency is slightly shifted towards right side within desired band range of operation. This is due to reactance offered by lumped components of

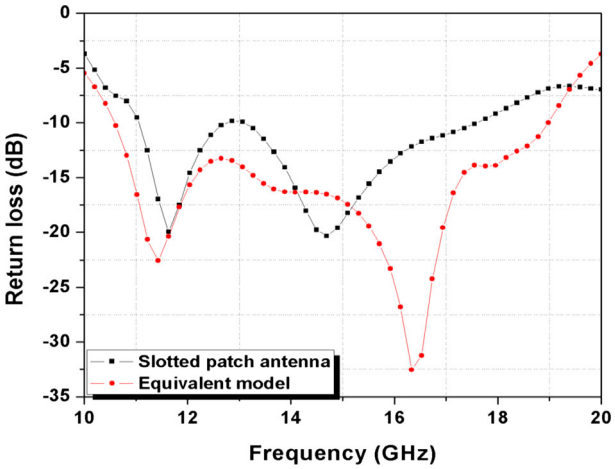

Fig. 12 Variation of return loss with frequency

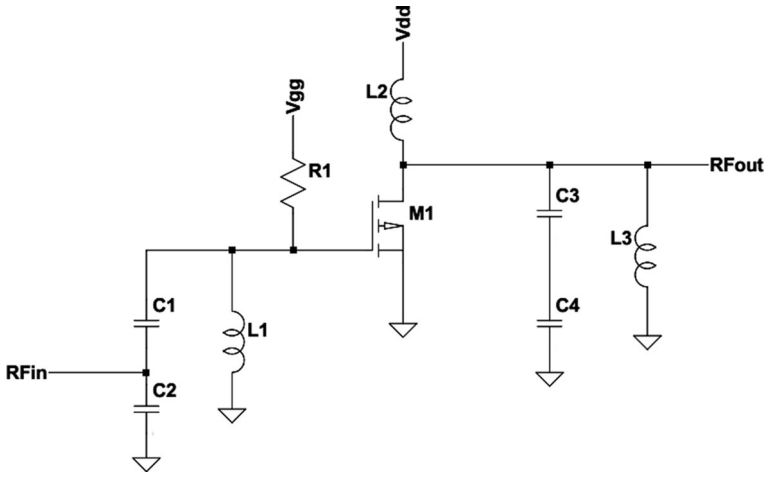

Fig. 13 Schematic of CMOS LNA using L–C matching network circuit

equivalent model which is approx 5 times larger than the slotted patch antenna. This result in wide bandwidth by 3 GHz. Good correlation is achieved between the circuit model and slotted patch antenna as shown in Fig. 12.

3 LNA Circuit Design and Analysis

Figure 13 shows LNA design in 10.3–14 GHz using extracted L–C circuit matching technique. It is important to note after the mathematical analysis of extracted equivalent model of slotted patch antenna that could be used for impedance transformation in the LNA design. It is possible to extract passive network (L and C) from any slotted patch antenna with the help of software package or using transmission line model [15]. The best

achievement of this work is to make a low noise amplifier using extracted passive network which is used as an input and output impedance matching circuit. A low noise amplifier consists of single stage common source (CS) for the amplification. The CS stage is the popular architecture for the LNA design that provides low noise figure and high gain. In this circuit design, only single stage CS amplifier offers good performance because of extracted L–C circuit of antenna which transforms the 50 Ω impedance to CS stage. In order to analyze the CMOS LNA, firstly the cut off frequency is calculated using the equation in (5) [16].

$$\omega_T = g_m C_{gs} \tag{5}$$

g_m is the transconductance of the device and C_{gs} is the gate to source capacitance. The value of $C_{gs} \approx \frac{1}{\omega_o^2 L_1}$ where ω_o is the designed frequency. The width of the device M1 is chosen using the formula as given in Eq. (6).

$$W = \frac{3}{2}\frac{C_{gs}}{C_{ox} \cdot L_{\min}} \tag{6}$$

An LNA is designed and simulated in ADS using TSMC 90 nm CMOS process. This design is operated using biasing of V_{dd} and V_{gg} respectively. The other component values of the LNA schematic are given in Table 1.

4 Results and Discussion

The major goals should be kept in mind that impedance matching is essential for achieving the performance parameters of LNA design. Here, this purpose is resolved by extracted passive network from the slotted patch antenna which is used to offer impedance matching for the MOS device. The input matching network consists of two capacitors which are parallel connected to the inductor and offers output impedance of (78Ω + 20j) that is compensated by value of resistance R_1 up to approx (50Ω + j0) condition and matched properly to the input impedance of MOS device. In a similar manner, output impedance of MOS should be matched to the input impedance of the extracted L–C circuits which is used

Table 1 Components values of CMOS LNA

Components	Values
*C*1	0.5 pF
*C*2	0.5 pF
*C*3	26.6 pF
*C*4	172 pF
*L*1	0.5 nH
*L*2	0.8 nH
*L*3	3.3 nH
*W (M*1*)*	125 µm
*L (M*1*)*	0.09 µm
*R*1	75 Ω
Vdd	1.6 V

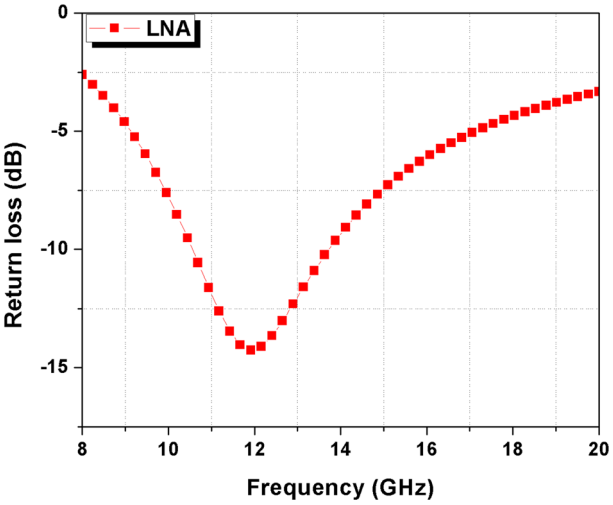

Fig. 14 Variation of return loss with the frequency

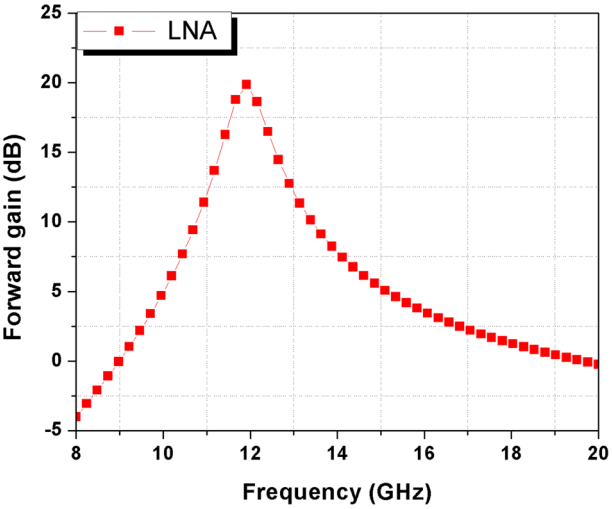

Fig. 15 Variation of forward gain with the frequency

as an output matching network for the LNA design. Using the S-parameter analysis in ADS platform, CMOS LNA design results in a wide band frequency of operation. In Fig. 14 the variation of return loss with frequency achieves the value of −14 dB at resonating frequency of 12 GHz within the range of 10.5–13.5 GHz. The return loss variation indicates better matching in the LNA design which may be helpful in achieving other performance parameters. It is well known that noise figure and gain are the essential requirements of an amplifier. In LNA circuit, source is grounded and drain is inductively loaded that achieves high gain of 22 dB at 12 GHz as shown in Fig. 15. The plot of noise figure is shown in Fig. 16. This figure reveals that low value of 1.6 dB with sharp flatness is achieved.

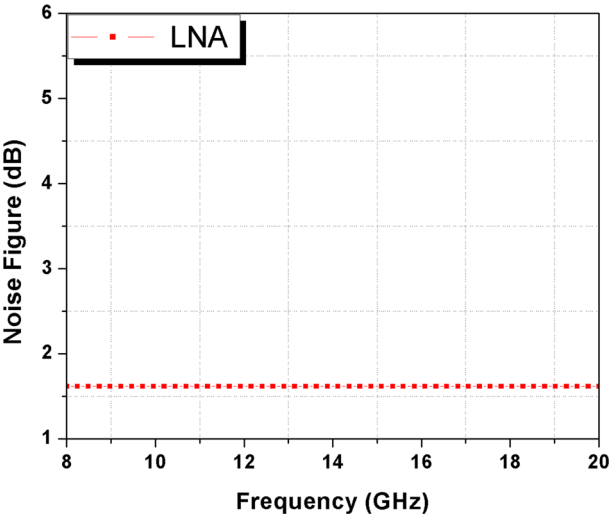

Fig. 16 Variation of Noise figure with frequency

5 Conclusion

It is concluded that a CMOS low noise amplifier operates using the extracted L–C circuit from reconfigurable slotted patch antenna that results in a wideband which slightly cover the X-band and Ku-band applications. The slotted patch antenna with MOS also achieves much wider bandwidth of 9 GHz. The post layout simulation result of CMOS LNA achieves a maximum power gain of 20 dB with the −3 dB bandwidth in the range of 10.3–13.6 GHz. The return loss at 12 GHz with flatness of 1.6 dB noise figure is obtained.

Acknowledgement This work was supported by Inje University Grant 2016 and 2017.

References

1. Al-Attar, T., & Lee, T. H. (2005). Monolithic integrated millimeter-wave IMPATT transmitter in standard CMOS technology. *IEEE Transactions on Microwave Theory and Techniques, 53,* 3557–3561.
2. Al-Attar, T., Mulligan, M. D., Lee, T. H. (2004) Lateral IMPATT Diodes in Standard CMOS Technology. In *IEEE international electron devices meeting* (pp. 459–462).
3. Tawk, Y., Costantine, J., Avery, K., & Christodoulou, C. G. (2011). Imple-mentation of a cognitive radio front-end using rotatable controlled re-configurable antennas. *IEEE Transactions on Antennas and Propagation, 59,* 1773–1778.
4. Schaubert, D., Farrar, F., Sindoris, A., & Hayes, S. (1981). Microstrip an-tennas with frequency agility and polarization diversity. *IEEE Transactions on Antennas and Propagation, 29,* 118–123.
5. Bhartia, P., & Bahl, I. J. (1982). Frequency agile microstrip antennas. *Microwave Journal, 25*, 67–70.
6. Yang, F., & Rahamt-Samii, Y. (2005). Patch antennas with switchable slots (PASS) in wireless communications: Concepts, designs, applications. *IEEE Antennas Propagation, 47,* 13–29.
7. Pues, H., & van de Capelle, A. (1984). Accurate transmission-line model for the rectangular microstrip antenna. *Microwaves, Optics and Antennas, IEE Proceedings H, 131,* 334–340.
8. Hammerstad, E., Jensen, O. (1980) Accurate models for microstrip computer-aided design. *Microwave symposium Digest, IEEE MTT-S International,* 407–409.
9. Kirschning, M., Jansen, R. H., & Koster, N. H. L. (1981). Accurate model for open end effect of microstrip lines. *Electronics Letters, 17,* 123–125.

10. Kumar, S., kanaujia, B. K., Pandey, G. P., & Singh, D. K. (2015). A miniurazation approach towards 40 GHz single chip reciever system for MMW Communication networks. *Wireless Personal communication*. doi:10.1007/s11277-015-2688-4.
11. Shigematsu, H., Hirose, T., Brewer, F., & Rodwell, M. (2005). Millimeter wave CMOS circuit design. *IEEE Transactions on Microwave Theory and Techniques, 53,* 472–477.
12. Doan, C. H., Emami, S., Nikneiad, A. M., & Brodersen, R. W. (2005). Millimeter-wave CMOS design. *IEEE Journal of Solid-State Circuits, 40,* 144–155.
13. Sun, K. J., Tsai, Z. M., Lin, K. L., & Wang, H. (2006). A noise optimization formulation for CMOS low-noise amplifiers with on-chip low-Q inductors. *IEEE Transactions on Microwave Theory and Techniques, 54,* 1554–1560.
14. Queudet, F., Pele, I., Froppier, B., Mahe, Y., Toutain, S. (2002). Integration of pass-band filters in patch antennas. In *32nd European microwave conference, Milan* (Vol. 35, pp. 685–688).
15. Khidre, A., Yang, F., & Elsherbeni, A. Z. (2015). A patch antenna with a Varacter loaded slot for reconfiguarble dual band operation. *IEEE Transcation on Antennas and Propagation, 63,* 755–760.
16. Shaeffer, D. K., & Lee, T. H. (1997). A 1.5-V, 1.5-GHz CMOS low noise amplifier. *IEEE Journal of Solid-State Circuits, 32,* 745–759.

Sandeep Kumar received his B.E. degree (Electronics and Communication Engineering) from Dr. B. R. Ambedkar University Agra in 2008 and M. Tech. degree (VLSI Design) from Gautam Budh University, Uttar Pradesh, India in 2012. He is done Ph.D. (Electronics Engineering) from IIT(ISM), Dhanbad, India in 2016. He is post-Doctoral Researcher in Department of Nanoscience and engineering, Inje university, South Korea. He has published several papers in reputed international journals. His current research interests are focus on Neuromorphic circuits, Terahertz CNT based IC design, Analog RF mixed/signal IC design, Reconfigurable antennas and CMOS based DC–DC converters.

Binod Kumar Kanaujia is currently working as Professor in the School of Computational and Integrative Sciences, Jawaharlal Nehru University, New Delhi since August, 2016. Before joining Jawaharlal Nehru University, he had been in the Department of Electronics & Communication Engineering in Ambedkar Institute of Advanced Communication Technologies & Research (formerly, Ambedkar Institute of Technology), Delhi as a Professor since Feb. 2011 & Associate Professor (2008–2011). Earlier, Dr. Kanaujia held the positions of Lecturer (1996–2005), Reader (2005–2008) and Head of Department in Department of Electronics & Communication Engineering, M.J.P. Rohilkhand University, Bareilly, India. Prior to his career in academics, Dr. Kanaujia had worked as Executive Engineer in the R&D division of M/s UPTRON India Ltd. Dr. Kanaujia had completed his B.Tech. in Electronics Engineering from KNIT Sultanpur, India in 1994. He did his M.Tech. and Ph.D. in 1998 and 2004; respectively from Department of Electronics Engineering, Indian Institute of Technology Banaras Hindu University, Varanasi, India. He has been awarded Junior Research Fellowship by UGC Delhi in the year 2001–02 for his outstanding work in the electronics field. He has a keen research interest in design and modelling of microstrip antenna, dielectric resonator antenna, left-handed metamaterial microstrip antenna, shorted microstrip antenna, ultra-wideband antennas, reconfigurable and circular polarized antennas for wireless communication. He has been credited to publish more than 170 research papers with more than 680 citations with h-index of 15 in several peer-reviewed journals and conferences. He had supervised 50 M.Tech. and 10 Ph.D. research scholars in the field of microwave engineering. He is a reviewer for several journals of international repute i.e. IET Microwaves, Antennas & Propagation, IEEE Antennas and Wireless Propagation Letters, Wireless Personal Communications, Journal

of Electromagnetic Wave and Application, Indian Journal of Radio and Space Physics, IETE Technical Review, International Journal of Electronics, International Journal of Engineering Science, IEEE Transactions on Antennas and Propagation, AEU-International Journal of Electronics and Communication, International Journal of Microwave and Wireless Technologies, etc. Dr. Kanaujia had successfully executed 04 research projects sponsored by several agencies of Government of India i.e. DRDO, DST, AICTE and ISRO. He is also a member of several academic and professional bodies i.e. IEEE, Institution of Engineers (India), Indian Society for Technical Education and The Institute of Electronics and Telecommunication Engineers of India.

Santanu Dwari was born in Howrah, West Bengal, India. He received his B.Tech and M.Tech degree in Radio Physics and Electronics from University of Calcutta, Kolkata, West Bengal, India in the year of 2000 and 2002 respectively and Ph.D. degree from Indian Institute of Technology, Kharagpur, West Bengal, India in the year of 2009. He joined Indian School of Mines, Dhanbad, Jharkhand, India in 2008 where he is currently an Assistant Professor in the Department of Electronics Engineering. He has published seven research papers in referred International Journals. He is carrying out two sponsored research project as Principal Investigator. His research interest includes Antennas, RF planar circuits, Computational Electromagnetic.

Ganga Prasad Pandey received B.Tech. in Electronics Engineering from K. N. I. T. Sultanpur, India in 2000. He completed M.E. in Computer Technology and Application from Delhi College of Engineering Delhi (India) in 2004. Presently, he is Assistant Professor in Electronics and Communication Engineering department of Maharaja Agrasen Institute of Technology, Delhi, India. He is currently working towards his Ph.D. degree from Uttrakhand Technical University. His research interests include active, Reconfigurable, frequency agile microstrip antennas and microwave/millimeter wave integrated circuits and devices.

Dinesh Kumar Singh received B.E. in Electronics and Communication Engineering from Kumaon University, Nainital, in 2003. He is done M.Tech in Digital Communication from RGPV University, Bhopal, India. Currently, he is pursuing Ph.D. from ISM, Dhanbad. His area of interest is microwave Engineering.

Anil Kumar Gautam was born in NOIDA, Uttar Pradesh, India. He received the B.E. degree in Electronics and Communication Engineering from Kumaon Engineering College, Almora, India and the Ph.D. degree in Electronic Engineering from Indian Institute of Technology, Banaras Hindu University, Varanasi, India, in 1999 and 2007, respectively. He joined the Department of Electronics & Communication Engineering, G B Pant Engineering College, Pauri Garhwal, India, in 2000, as an Assistant Professor and he has been an Associate Professor there since 2009. He is an active member of Board of study, Academic council and many other academic committees of GBPEC, Pauri. He is also member of BOS of HNB Garhwal Central University, INDIA and Uttarakhand Technical University, Dehradun, INDIA. He is nominated as Nodal Officer, TSP and SCSP Grants by Government of Uttarakhand and executed several projects under these grants. He has supervised 15 M.Tech. and 01 Ph.D. Thesis and currently supervising 09 Ph.D. theses in the area of Microstrip antenna. He is the author/coauthor of more than 60 research papers published in the refereed international journals and conferences Like IEEE, Microwave and optical Technology Letters, Springer, etc. He is the author of the 12 books in the field of Electronics Engineering in the field of Digital Electronics, Antenna and Microwave Engineering. He is a member of IEEE (USA) and many other technical societies. He is also in reviewers panel of IEEE, Transaction on Antenna and Propagation, *IET Microwaves, Antennas and Propagation,* Personal and wireless communication, Springer, International Journal of Electronics, International Journal of Antenna and Propagation. His main research interests are in design and Modeling of Active Microstrip Antenna, microstrip antennas with Defected Ground Structure, Ultra wide bandwidth antennas, and reconfigurable antennas, reconfiguration antenna array, circular polarized antenna, etc.