Computer Architecture

Project 3

Due. 2017/6/9

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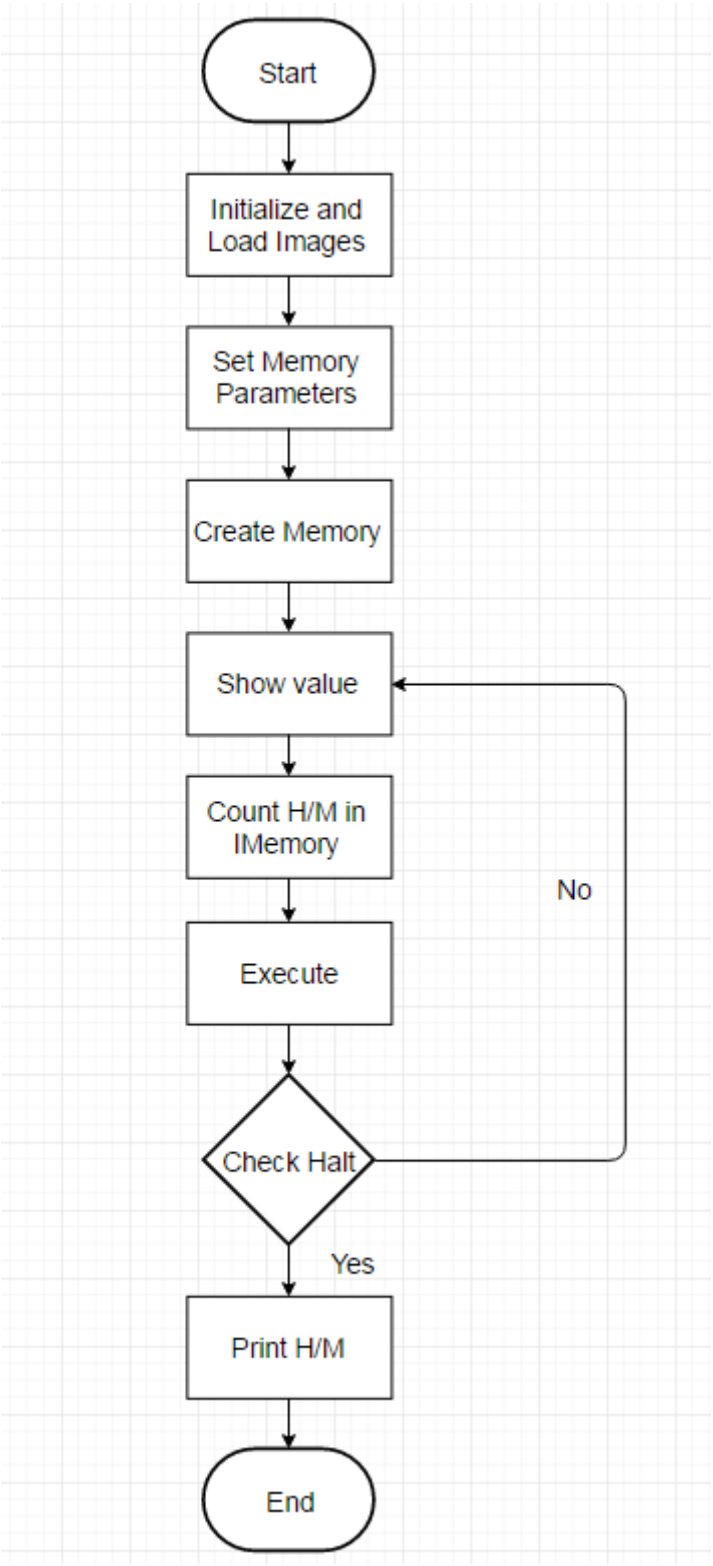
Project Description

1. Flow chart



The picture above is the flow chart about my program. At the beginning, the program will initialize the value of registers and memory arrays to zero, and then read the images in. According to the input, the parameters of IMemory and DMemory are set and then created. For each Instruction, the program will record “hit” or “miss” happened in different places by ICMP. If the instruction is about data access, then “hit”, “miss” in data memory will also be recorded by DCMP. After the instruction is executed, the program will check whether it is halt or not. If so, then the program will print the result in each cache, TLB and page table. If not, the program will print the registers’ values and wait for the next instruction.

2. Detailed description

In instruction.cpp:

In memory.cpp:

These two files are almost same as the file in project 1.

In regfile.cpp:

Same as the file in prpject1.

In simulator.cpp:

This file do the things shown in the flow chart.

In CMP.cpp:

This file uses TLB and page table to translate virtual address (PC), and then uses the result to get data. First, the program will check if there is translated physical address for PC. If so, TLB hit will plus 1 and then find data in cache. If data can be found in cache, then cache hit plus 1. If it cannot be found in cache, then cache miss plus 1 and the program will update cache.

If TLB can’t find according physical address, then TLB miss plus 1 and the program will try to find physical address in page table. If the physical address is found, then the program will do the same thing as TLB hit. The worst case is both TLB and page table miss, then data should be found in disk and update TLB, page table and cache.

Testcase Description

Since I do not know what kind of instruction will have special performance in CMP, I just randomly pick some instruction and put them together.