SPICE Project 2
CMOS Inverter

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1 Device Parameters and Dimensions

Table 1 gives the device specifications that were supplied for both pMOS and nMOS devices. All parameters were then converted in to the CGS unit system for consistancy. Any cell which contains N/A means that that parameter is not applicable for that specific device.

Parameter Name	Parameter	nMOS	pMOS
Channel Length	L	$2.5 \times 10^{-4}\,\mathrm{cm}$	$2.5 \times 10^{-4}\,\mathrm{cm}$
Channel Width	W	$5.0 \times 10^{-4}\,\mathrm{cm}$	$15 \times 10^{-4}\,\mathrm{cm}$
Lateral Diffusion	L_D	$0.2 \times 10^{-4}\,\mathrm{cm}$	$0.2 \times 10^{-4}\,\mathrm{cm}$
Gate Oxide Thickness	t_{ox}	$5.0 \times 10^{-6}\,\mathrm{cm}$	$5.0 \times 10^{-6}\,\mathrm{cm}$
Substrate Acceptor Dopant Concentration	N_a^-	$5.0 \times 10^{16}\,\mathrm{cm}^{-3}$	N/A
Substrate Donor Dopant Concentration	N_d^+	N/A	$5.0 \times 10^{16}\,\mathrm{cm}^{-3}$
Fixed Oxide Charge Density	N_f	$2 \times 10^{10}\,\mathrm{cm}^{-2}$	$2 \times 10^{10}\,\mathrm{cm}^{-2}$
Source/Drain Junction Depth	X_j	$0.2 \times 10^{-4}\,\mathrm{cm}$	$0.2 \times 10^{-4}\,\mathrm{cm}$
Transconductance	λ	$0.02\,\mathrm{V}^{-1}$	$0.02\,\mathrm{V}^{-1}$
Source Area	A_s	$1.0 \times 10^{-7}\,\mathrm{cm}^2$	$3.0 \times 10^{-7}\mathrm{cm}^2$
Drain Area	A_d	$1.0 \times 10^{-7}\,\mathrm{cm}^2$	$3.0 \times 10^{-7}\mathrm{cm}^2$
Source/Drain Acceptor Dopant Concentration	$N^+_{a_{s/s}}$	N/A	$1.0 \times 10^{20}\,\mathrm{cm}^{-3}$
Source/Drain Donor Dopant Concentration	$N^-_{d_{s/d}}$	$1.0 \times 10^{20}\,\mathrm{cm}^{-3}$	N/A

Table 1.

A table with all the SPICE keywords and the corresponding symbols along with the units SPICE expects can be found on page 365 in the Casey textbook. Futhermore k is defined as Boltzmann's Constant and has a value of $8.616 \times 10^{-5}\,\mathrm{eV/K}$.

2 MOSFET Parameter Calculation

All calculations were performed with the aid of a MatLab script which is included in section 8. The first SPICE parameter to be calculated was the threshold voltage, V_T. The first step is to calculate the work function for the n^+-polysilicon gate and p^+-polysilicon gate followed by the work function of the p-type and n-type substrates. Equation 1 shows how the work function

for an n-type polysilicon gate may be calculated.

$$\Phi_M = \Phi_{n^+_{\text{poly}}} = q\,X_{\text{Si}} + (E_c - E_f) \tag{1}$$

From the parameters given we know that an n^+-polysilicon material was used for the nMOS gate material which has $E_f = E_c$ and thus $E_c - E_f = 0$ thus $\boxed{\Phi_{n^+_{\text{poly}}} = q\,X_{\text{Si}} = 4.05\,\text{eV}}$. For the p^+-polysilicon gate material equation 2 gives the work function.

$$\Phi_M = \Phi_{p^+_{\text{poly}}} = q\,X_{\text{Si}} + E_g - (E_f - E_v) \tag{2}$$

Again from the given parameters $E_f = E_v$ and thus $\boxed{\Phi_{p^+_{\text{poly}}} = 5.175\,\text{eV}}$.

The work function for the nMOS p-type substrate and the pMOS n-type substrate must now be calculated.

$$\Phi_S = \Phi_{p_{\text{sub}}} = q\,X_{\text{Si}} + E_g - (E_f - E_v) \tag{3}$$

Where

$$E_f - E_v = -\,k\,T\ln\left(\frac{p}{N_V}\right) \tag{4}$$

while ensuring that $p/N_V < 0.1$. Substituting equation 4 into equation 3 gives $\Phi_{p_{\text{sub}}} = 5.01$ eV. Repeating a similar procedure for the n-type substrate of the pMOS device gives

$$\Phi_S = \Phi_{n_{\text{sub}}} = q\,X_{\text{Si}} + (E_c - E_f) \tag{5}$$

Where

$$E_c - E_f = -\,k\,T\ln\left(\frac{n}{N_c}\right) \tag{6}$$

while ensuring that $n/N_c < 0.1$. These equations give $\boxed{\Phi_{n_{\text{sub}}} = 4.24\,\text{eV}}$.

We may now calculate the ideal flat-band voltage for both nMOS and pMOS devices by using equation 7.

$$\boxed{V^0_{FB_n} = \Phi_M - \Phi_S = -\,0.959\,\text{eV}} \tag{7}$$

$$\boxed{V^0_{FB_{\text{p}}} = 0.961\,\text{eV}} \tag{8}$$

Knowing the ideal flat-band voltage enables us to now calculate the flat-band voltage accounting for fixed charge in the gate oxide.

$$V_{FB} = V^0_{\text{FB}} - \frac{q\,N_f}{C'_{ox}} \tag{9}$$

Where $C'_{ox} = \epsilon_{ox}/t_{ox}$ and $\epsilon_{ox} = 3.9\,\epsilon_0$. $\boxed{C'_{ox} = 69\,\text{fF}}$ for both nMOS and pMOS devices. Thus

$$\boxed{V_{FB_{\text{n}}} = -\,1.01\,\text{eV}} \tag{10}$$

and

$$\boxed{V_{FB_p} = 0.92\,\text{eV}} \tag{11}$$

Lastly we need to calculate the surface potential ψ_s and for inversion $-\,\psi_s = 2\,\psi_b$. ψ_b may be

calculated directly by

$$\boxed{\psi_{b_n} = -\,k\,T\ln\left(\frac{N_a^-}{n_i}\right) = -\,0.399\,\text{eV}} \tag{12}$$

$$\boxed{\psi_{b_p} = k\,T\ln\left(\frac{N_d^+}{n_i}\right) = 0.399\,\text{eV}} \tag{13}$$

Thus the SPICE parameter `PHI=0.7974V`.

Finally with all of these values we may calculate the threshold voltage for the nMOS and pMOS devices.

$$\boxed{V_{T_n} = V_{FB} + 2\,|\psi_b| + \frac{\sqrt{4\,q\,\epsilon_{\text{Si}}\,N_a^-\,|\psi_b|}}{C'_{ox}} = 1.458\,\text{V}} \tag{14}$$

$$\boxed{V_{T_p} = V_{\text{FB}} - 2\,|\psi_{b_n}| - \frac{\sqrt{4\,q\,\epsilon_{\text{Si}}\,N_d^+\,|\psi_{b_n}|}}{C'_{ox}} = -\,1.549\,\text{V}} \tag{15}$$

The next SPICE parameter found was the bulk space-charge parameter, γ. Equation 16 shows the value of γ of an nMOS device, substituting N_d^+ for N_a^- will yield γ_p and since in our case N_a^-=N_d^+, $\boxed{\gamma_n = \gamma_p}$.

$$\boxed{\gamma_n = \frac{\sqrt{2\,q\,\epsilon_{\text{Si}}\,N_a^-}}{C'_{ox}} = 1.866\,\text{V}} \tag{16}$$

The source and drain junction built-in potential, V_{bi} is found easily for both nMOS and pMOS with equation 17.

$$\boxed{V_{bi} = k\,T\ln\left(\frac{N_a^-\,N_d^+}{n_i^2}\right) = 0.994\,\text{V}} \tag{17}$$

Lastly the surface mobility is read from the graph, "Electron and hole mobility in Si as a function of total impurity concentration at room temperature" in the front of Casey. From here we see that for the nMOS device a dopant concentration of the p-substrate gives a mobility of $\boxed{\mu_p = 150\,\text{cm/Vs}}$ after dividing by three to account for strong field effects. For the pMOS device with n-substrate we have a mobility of $\boxed{\mu_n = 316.67\,\text{cm/Vs}}$ again dividing by three to account for strong filed effects. These mobilities allow for the calculation of KP. Where

$$KP = \mu\,C'_{ox} \tag{18}$$

and thus $\boxed{KP_n = 1.04\times10^{-5}\,\text{A/V}^2}$ and $\boxed{KP_p = 2.19\times10^{-5}\,\text{A/V}^2}$.

All remaining parameters needed for SPICE level 2 MOSFET simulation are given in the complete SPICE listings in Section 7. Further parameters were passed when the models defined were invoked, those two are of course shown in the complete SPICE code listings.

3 Question 1: Single Inverter Delay Time

Figure 1 shows the circuit analyzed with all nodes numbered. The SPICE code which corre-

sponds to this circuit may be found in section 7.1.

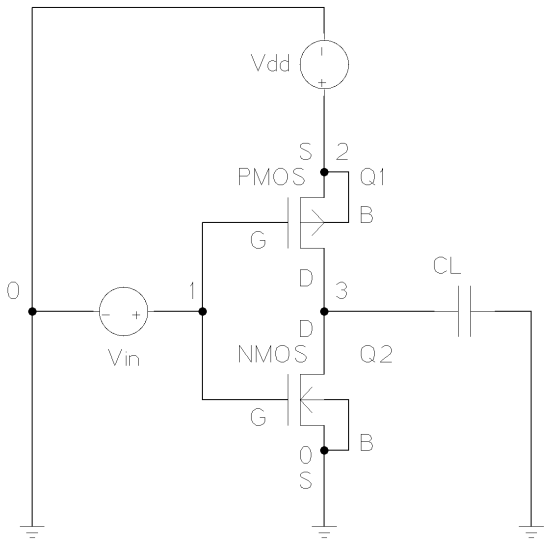

Figure 1.

Figure 2 shows the input voltage (node 1) and the output voltage (node 3) plotted against time. The propagation delay rise time, $\boxed{t_{P_{H\to L}} = 3.86\,\text{ns}}$, while the fall time is $\boxed{t_{P_{L\to H}} = 1.46\,\text{ns}}$.

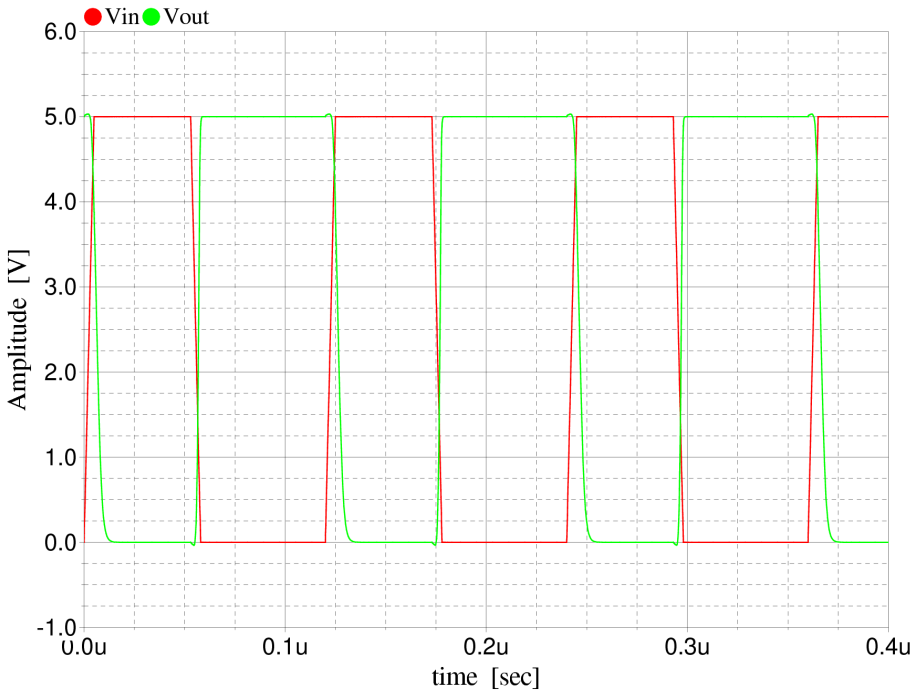

Figure 2.

4 Question 2: Two Inverters Cascaded

For this question the circuit shown in figure 1 was put in to a spice subcircuit and then cascaded. Figure 3 shows the circuit analyzed with all subcircuit nodes numbered and all exterior nodes numbered. The SPICE listing corresponding to this circuit may be found in section 7.2.

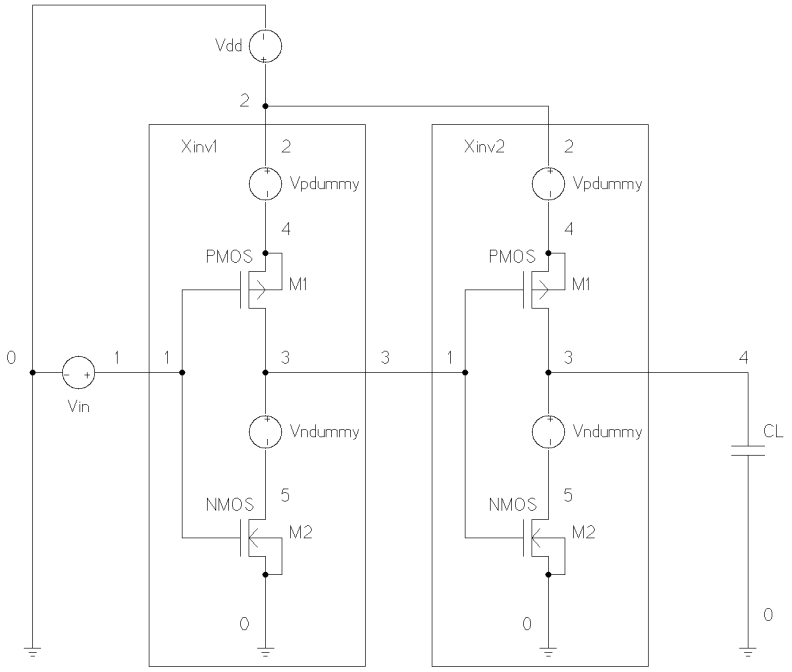

Figure 3.

Figure 4 shows the input voltage and the output voltage against time. For the cascaded circuit the propagation delay rise time is $\boxed{t_{P_{L\to H}} = 2.76\,\text{ns}}$ while the propagation delay fall time is $\boxed{t_{P_{H\to L}} = 3.54\,\text{ns}}$.

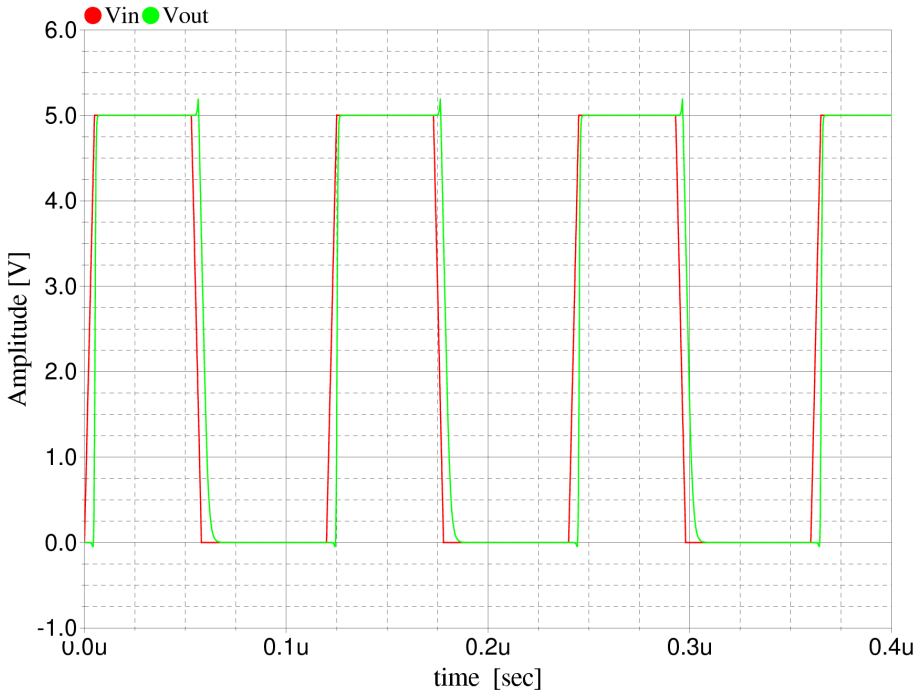

Figure 4.

The power dissipation shown in figure 5 for the pMOS and nMOS transistors are spikes simply because unlike bipolar transistors there is no static power loss for CMOS circuitry. The only charge transfer and thus current flow and hence power is through the charging and discharing of the load capacitances and parasitic device capacitances. The output of the first inverter (node 3 in figure 3) was scaled and plotted so one can see that when the second

inverter's input is going low the pMOS turns on and the device's parasitics must be charged along with the load capacitance up to V_{dd}. The nMOS device turns off during this time and any connected parasitics must also charge to V_{dd}. When the second inverter's input goes high the pMOS device's parasitics along with the load capacitance must be discharged to ground through the nMOS device which has now turned on. The nMOS device's parasitics must now also be discharged to ground or their equilibrium voltage. Also it is important to note that in this cascaded design with inverters of the same size, the gate inputs to the pMOS and nMOS devices in the second inverter is acting as a load on the first inverter device. It is also interesting to note the decrease in $t_{P_{L\to H}}$ as compared to the single inverter. CMOS design is fussy like this as I learned in EE447 and how one can optimize by using different sizes of gates and multiple stages to actually improve CMOS performance. Note again that in figure 5, V_{in} is scaled in order to preserve the readability of the graph.

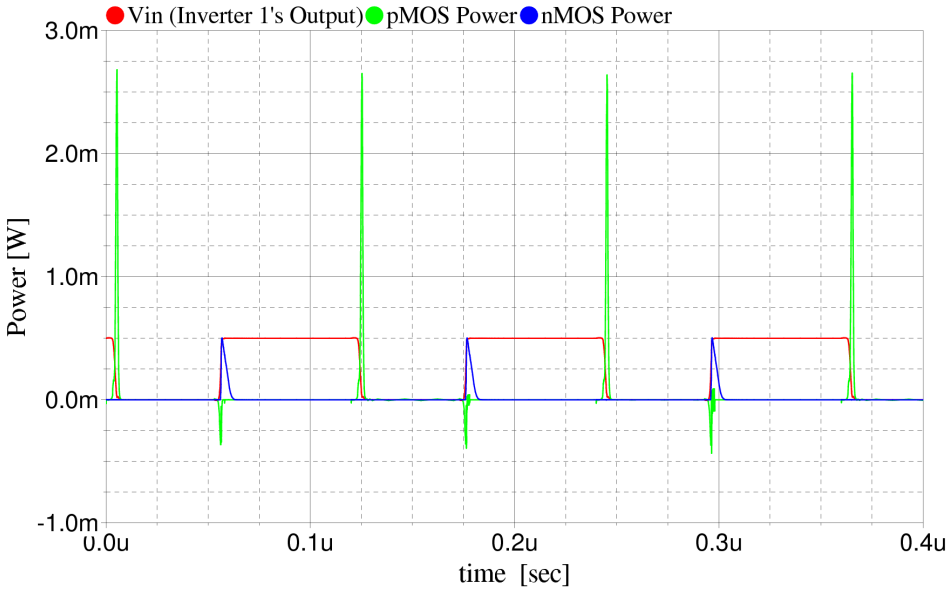

Figure 5.

5 Question 3: Reduced V_{dd}

The effects of the reduced supply voltage, V_{dd} and of course the input voltage V_{in} from 5 V to 3.5 V reduces power consumption as seen in figure 7 but this reduced power comes at the price of the propagation delay times as shown in figure 6. The propagation delay rise time increased to $\boxed{t_{P_{L\to H}} = 4.78\,\text{ns}}$ from a previous value of 2.76 ns. The fall time also suffered and more than doubled from its previous value of 3.54 ns to a new value of $\boxed{t_{P_{H\to L}} = 7.53\,\text{ns}}$. The pMOS maximum power consumption dropped significantly from 2.66 mW at $V_{dd} = V_{in} = 5$ V to only $\boxed{P_p = 0.625\,\text{mW}}$. That's over 75% power drop in the pMOS. The nMOS device with a 5 V source was consuming only 0.5 mW. While the nMOS device being driven from the reduced voltage only consumes $\boxed{P_n = 0.161\,\text{mW}}$ which is again nearly a 75% power decrease.

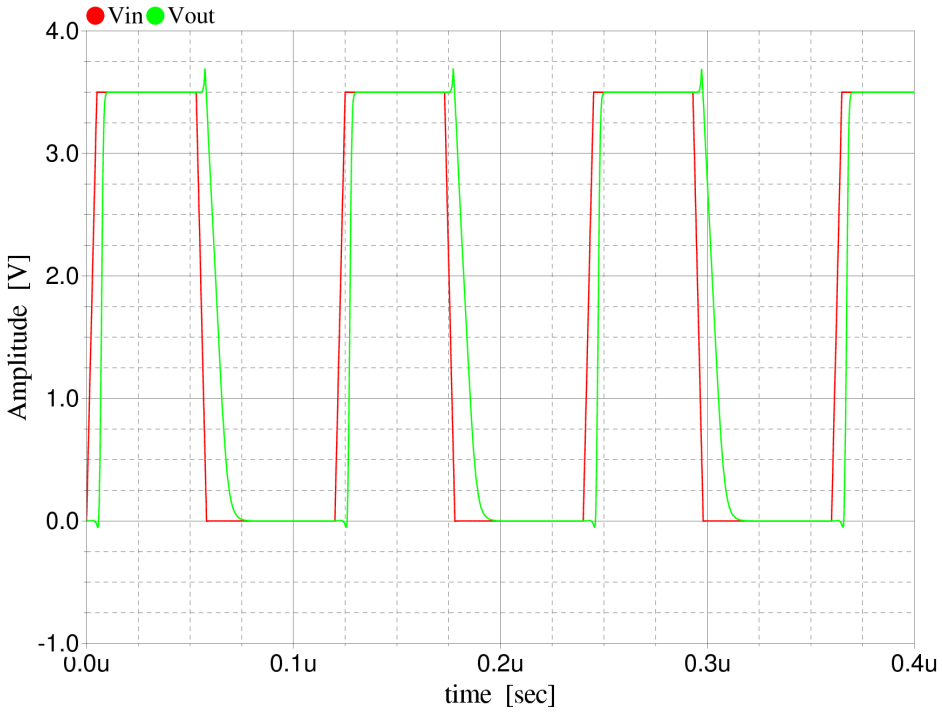

Figure 6.

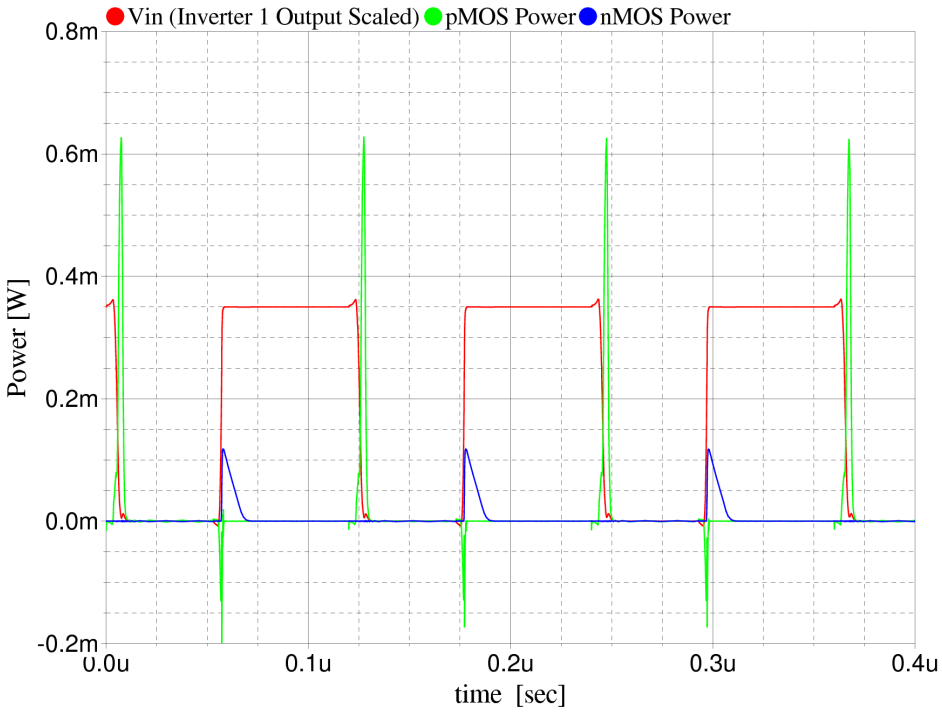

Figure 7.

The plots in figures 6 & 7 were generated from the same SPICE code as shown in section 7.2 except that the line `Vin 1 0 pulse(0v 5v 0ns 5ns 5ns 48ns 120ns)` was modified to `Vin 1 0 pulse(0v 3.5v 0ns 5ns 5ns 48ns 120ns)` and the line `Vdd 2 0 5v` was modified to `Vdd 2 0 3.5v`.

6 Question 4: Improve Reduced Voltage Delay

Motivated by the hint given by you I looked for how to improve the ability for the device to deliver current. The level 1 MOSFET model in SPICE model gives

$$I_D = \frac{W}{L}\,\mu_n\,C'_{ox}[(V_{GS}-V_T)-V_{DS}/2]\,V_{DS} \tag{19}$$

Thus the simplist and most straightforward way I saw to increase I_D was to decrease the oxide thickness, t_{ox}. This would have the net effect of increasing C'_{ox} and thus increasing I_D. I do wonder how practical this method as I am sure there are limits as to how thin one can make the gate oxide before the dialectric breaks down. However I don't really know so I just decreased t_{ox} from 50 nm to a fifth of that to $t_{ox_{\text{new}}} = 10\,\text{nm}$ for both pMOS and nMOS devices. After making this one change in the MatLab code and then entering the new parameter values in my model statements I got the plot shown in figure 8 for V_{in} and V_o.

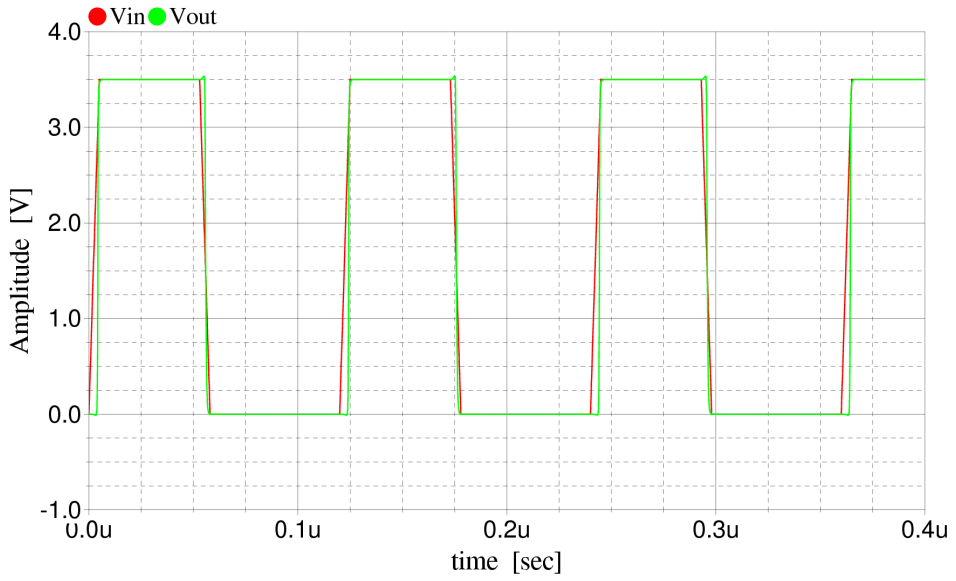

Figure 8.

The SPICE model statements are as follows

```
* NMOS Device
.model nmos1 nmos (LEVEL=2, UO=150, VTO=0.1624, GAMMA=0.3732, PHI=0.7974,
+                  KP=5.1772e-5 ,LAMBDA=0.02, XJ=0.2u, LD=0.2u, PB=0.9939,
+                  NSUB=5e16, NSS=2e10, TOX=10nm,TPG=+1)

* PMOS Device
.model pmos1 pmos (LEVEL=2, UO=316.67, VTO=-0.1788, GAMMA=0.3732, PHI=0.7974,
+                  KP=1.0930e-004, LAMBDA=0.02, XJ=0.2u, LD=0.2u, PB=0.9939,
+                  NSUB=5e16, NSS=2e10, TOX=10nm,TPG=+1)
```

The delay times are very very small. In fact they're smaller than those for the 5 V design. The rise time delay was $t_{P_{L\to H}} = 1.81$ ns and the fall time was $t_{P_{H\to L}} = 0.36$ ns. The power dissipation for the thinner gate oxide design was much higher than either the 5 V and the 3.5 V design. Figure 9 shows that the pMOS power dissipation was around 5 mW and the nMOS power dissipation was near 1.5 mW. This is close to double the power for the pMOS device and triple the power for the nMOS devices for the 5 V case. Thus although we're running with a reduced voltage our power dissipation is actually worse.

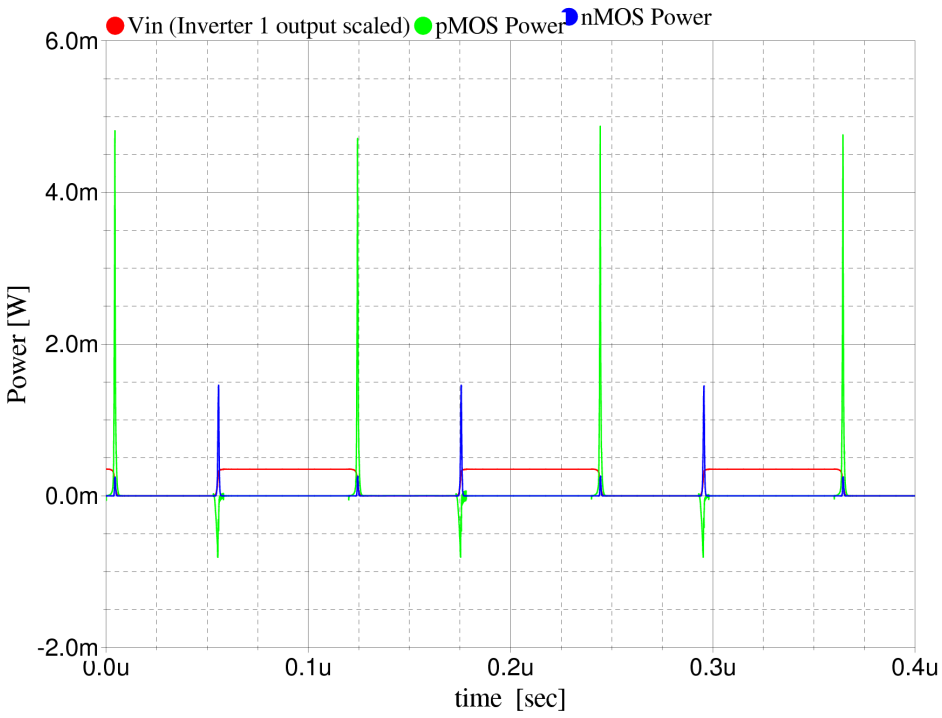

Figure 9.

Overall I guess perhaps the aim was more to keep power consumption down while maintaining a delay on the order fo that found in the 5V circuit. I am also sure playing with dopant levels and other things could benefit the speed.

7 SPICE Code

7.1 Part 1: Simple CMOS Inverter with Capacitive Load

```
* CMOS Inverter
* Tim Starr #45727                    4/20/06
* EE441                               SPICE Project 2

Vin 1 0 pulse(0v 5v 0ns 5ns 5ns 48ns 120ns)
Vdd 2 0 5v

m1 3 1 0 0 nmos1 L=2.5u W=5u  AD=1.0e-11 AS=1.0e-11
m2 3 1 2 2 pmos1 L=2.5u W=15u AD=3.0e-11 AS=3.0e-11
CL 3 0 100fF
*m3 4 3 0 0 nmos1 L=2.5u W=5u  AD=1.0e-11 AS=1.0e-11
*m4 4 3 2 2 pmos1 L=2.5u W=15u AD=3.0e-11 AS=3.0e-11
```

```
*CL 4 0 100fF

* NMOS Device
.model nmos1 nmos (LEVEL=2, UO=150, VTO=1.4581, GAMMA=1.8658, PHI=0.7974,
+                  KP=1.0354e-5 ,LAMBDA=0.02, XJ=0.2u, LD=0.2u, PB=0.9939,
+                  NSUB=5e16, NSS=2e10, TOX=50n,TPG=+1)

* PMOS Device
.model pmos1 pmos (LEVEL=2, UO=316.67, VTO=-1.5488, GAMMA=1.8658, PHI=0.7974,
+                  KP=2.1860e-5, LAMBDA=0.02, XJ=0.2u, LD=0.2u, PB=0.9939,
+                  NSUB=5e16, NSS=2e10, TOX=50nm,TPG=+1)
```

7.2 Part 2: 2-Stage CMOS Inverter Cascaded with Capacitive Load

```
* CMOS Inverter
* Tim Starr #45727                      4/20/06
* EE441                                 SPICE Project 2

Vin 1 0 pulse(0v 5v 0ns 5ns 5ns 48ns 120ns)
Vdd 2 0 5v

Xinv1 1 3 2 cmosinv
Xinv2 3 4 2 cmosinv
CL    4 0 100fF

*              CMOS Inverter
*               In Out Vdd
*               |  |   |
.subckt cmosinv 1  3   2
Vpdummy 2 4 0v
m1 3 1 4 4 pmos1 L=2.5u W=15u AD=3.0e-11 AS=3.0e-11
Vndummy 3 5 0v
m2 5 1 0 0 nmos1 L=2.5u W=5u  AD=1.0e-11 AS=1.0e-11

* NMOS Device
.model nmos1 nmos (LEVEL=2, UO=150, VTO=1.4581, GAMMA=1.8658, PHI=0.7974,
+                  KP=1.0354e-5 ,LAMBDA=0.02, XJ=0.2u, LD=0.2u, PB=0.9939,
+                  NSUB=5e16, NSS=2e10, TOX=50n,TPG=+1)

* PMOS Device
.model pmos1 pmos (LEVEL=2, UO=316.67, VTO=-1.5488, GAMMA=1.8658, PHI=0.7974,
+                  KP=2.1860e-5, LAMBDA=0.02, XJ=0.2u, LD=0.2u, PB=0.9939,
+                  NSUB=5e16, NSS=2e10, TOX=50nm,TPG=+1)
.ends
```

8 MatLab Script for Parameter Calculations

```
clear
clc

%CGS used throughout
% Constants
```

```
k           = 8.616e-5; % eV/K
q           = 1.602e-19;% C
e0          = 8.85e-14; % F/cm
eSi         = 11.7*e0;  % F/cm
eox         = 3.90*e0;  % F/cm
Nc          = 2.84e19;  % cm^-3 at 300K
Nv          = 3.08e19;  % cm^-3 at 300K
ni          = 1.00e10;  % cm^-3 at 300K
Eg          = 1.125;    % eV
qXsi        = 4.05;     % eV
qPhiAl      = 4.10;     % eV
T           = 300;      % K
n_poly      = 2.3e19;   % cm^-3 electron concentration in polysilicon with
                        % Ef=Ec see HW 5 problem 7.8
p_poly      = 2.5e19;   % cm^-3 hole concentration in polysilicon
                        % with Ev=Ef see HW 5 problem 7.8

% NMOS parameters
nmos.L      = 2.5e-4;   % cm
nmos.LD     = 2.0e-5;   % cm
nmos.tox    = 5.0e-6;   % cm
nmos.W      = 5.0e-4;   % cm
nmos.Xj     = 2.0e-5;   % cm
nmos.lambda = 0.02;     % 1/V
nmos.Na     = 5.0e16;   % cm^-3 Source and Drain doping
nmos.Nd     = 1.0e20;   % cm^-3 Substrate doping
nmos.Nf     = 2.0e10;   % cm^-2
nmos.As     = 1.0e-7;   % cm^2
nmos.Ad     = 1.0e-7;   % cm^2
nmos.mu_p   = 450;      % cm^2/(V*s) Substrate hole mobility

% PMOS parameters
pmos.L      = 2.5e-4;   % cm
pmos.LD     = 2.0e-5;   % cm
pmos.tox    = 5.0e-6;   % cm
pmos.W      = 15.0e-4;  % cm
pmos.Xj     = 2.0e-5;   % cm
pmos.lambda = 0.02;     % 1/V
pmos.Na     = 1.0e20;   % cm^-3
pmos.Nd     = 5.0e16;   % cm^-3
pmos.Nf     = 2.0e10;   % cm^-2
pmos.As     = 3.0e-7;   % cm^2
pmos.Ad     = 3.0e-7;   % cm^2
pmos.mu_n   = 950;      % cm^2/(V*s) n-type substrate electron mobility

% Begin NMOS parameter calculations
nmos.UO          = nmos.mu_p/3;                                  % cm^2/(V*s)
nmos.qPhiPolySi  = qXsi;                                            % eV
nmos.qpsisi      = qXsi+Eg+k*T*log(nmos.Na/Nv);                     % eV
nmos.Coxprime    = (eox/nmos.tox);                                  % F
%nmos.LD          = 2.0e-5;                                        % cm
nmos.Vfb0        = nmos.qPhiPolySi - nmos.qpsisi;                   % eV
nmos.Vfb         = nmos.Vfb0 - (q*nmos.Nf)/(nmos.Coxprime);         % eV
nmos.phib        = -k*T*log(nmos.Na/ni);                            % eV
nmos.phis        = -2*nmos.phib;                                    % eV
```

```
nmos.Vt          = nmos.Vfb + 2*abs(nmos.phib) + ...
                   sqrt(4*q*eSi*nmos.Na*abs(nmos.phib))/(eox/nmos.tox); % eV
nmos.gamma       = sqrt(2*q*eSi*nmos.Na)/nmos.Coxprime;              % V^(1/2)
nmos.Vbi         = (k*T)*log(nmos.Na*nmos.Nd/ni^2);                    % V
nmos.PB = nmos.Vbi;
nmos.KP          = nmos.UO*nmos.Coxprime;                              % A/V^2

% Begin PMOS parameter caclulations
pmos.UO          = pmos.mu_n/3;                                  % cm^2/(V*s)
pmos.qPhiPolySi  = qXsi+Eg;                                        % eV
pmos.qpsisi      = qXsi-k*T*log(pmos.Nd/Nc);                       % eV
pmos.Coxprime    = (eox/pmos.tox);                                 % F
pmos.Vfb0        = pmos.qPhiPolySi - pmos.qpsisi;                  % eV
pmos.Vfb         = pmos.Vfb0-(q*pmos.Nf)/pmos.Coxprime;            % eV
pmos.phib        = k*T*log(pmos.Nd/ni);                            % eV
pmos.phis        = -2*pmos.phib;                                   % eV
pmos.Vt          = pmos.Vfb - 2*abs(pmos.phib)- ...
                   sqrt(4*q*eSi*pmos.Nd*abs(pmos.phib))/pmos.Coxprime;  % eV
pmos.gamma       = sqrt(2*q*eSi*pmos.Nd)/pmos.Coxprime;          % V^(1/2)
pmos.Vbi         = (k*T)*log(pmos.Na*pmos.Nd/ni^2);                % V
pmos.PB = pmos.Vbi;
pmos.KP          = pmos.UO*pmos.Coxprime;                          % A/V^2
```