BLG222E – Computer Organization

Midterm 1 Solutions

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İTÜ

Direct addressing mode ($I = 0$) and indirect addressing mode ($I = 1$) will be changed with register-indexed addressing.

- In direct register-indexed addressing ($I = 0$) the effective address (EA) is computed as:

$$EA = AR + TR(11 - 0)$$

- In indirect register-indexed addressing ($I = 1$) the effective address (EA) is computed as:

$$EA = M[AR + TR(11 - 0)]$$

Implement fetch, decode and execute cycles of LDA instruction ($AC \leftarrow M[EA]$, opcode=010) with direct and indirect register-indexed addressing mode using RTL and timing signals T_0, T_1 etc.

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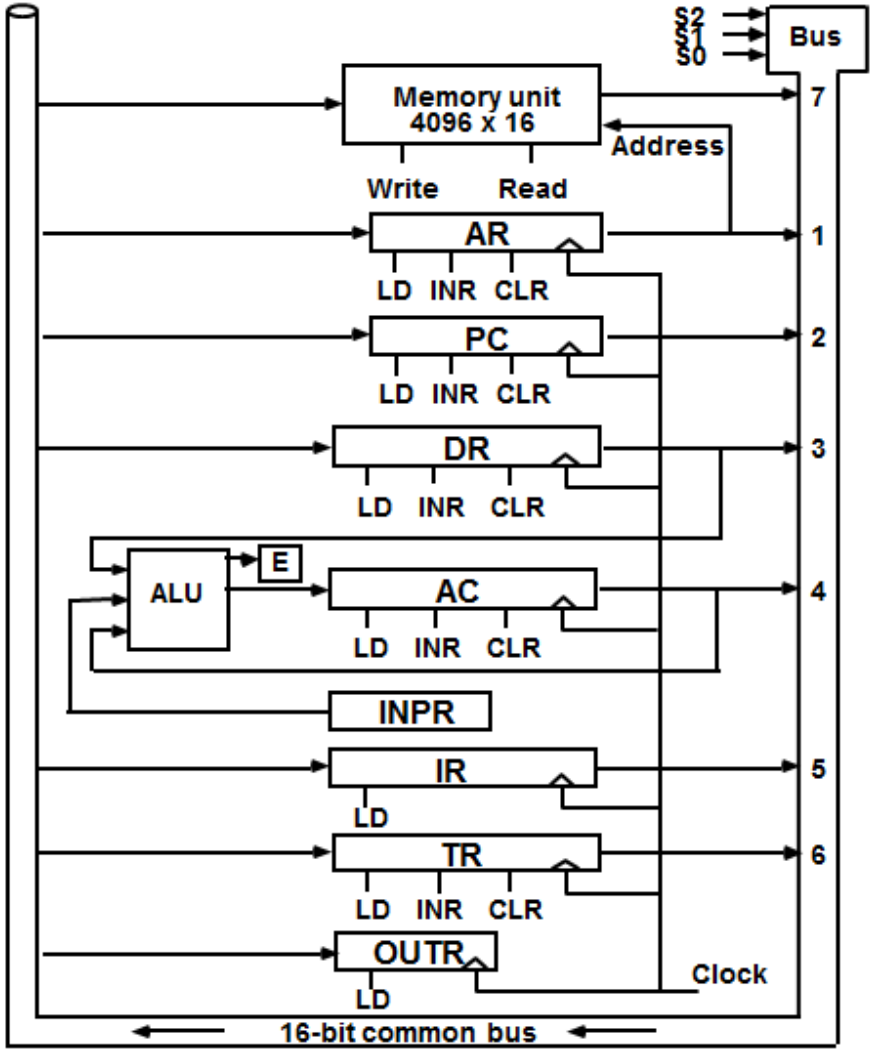
A Simple Computer Architecture



Solution

- $T_0 : AR \leftarrow PC$
- $T_1 : IR \leftarrow M[AR], PC \leftarrow PC + 1$
- $T_2 : D_0 ... D_7 \leftarrow decode\ IR(12...14), AR \leftarrow IR(0...11), I \leftarrow IR(15)$
- $T_3 D_2 : DR \leftarrow AR$
- $T_4 D_2 : AC \leftarrow DR, DR \leftarrow TR$
- $T_5 D_2 : AC \leftarrow AC + DR$
- $T_6 D_2 : AR \leftarrow AC$
- $T_7 D_2 I : AR \leftarrow M[AR]$
- $T_7 D_2 I' : do\ nothing$
- $T_8 D_2 : DR \leftarrow M[AR]$
- $T_9 D_2 : AC \leftarrow DR$

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Consider a new instruction “memory add” (MAD, opcode=110) that adds two numbers at sequential effective addresses of the memory and write the result to the next effective address in memory:

$$M[EA+2] \leftarrow M[EA] + M[EA+1]$$

Write the microinstructions in register transfer language (RTL) that fetches, decodes and executes MAD instruction using timing signals T_0, T_1 etc.

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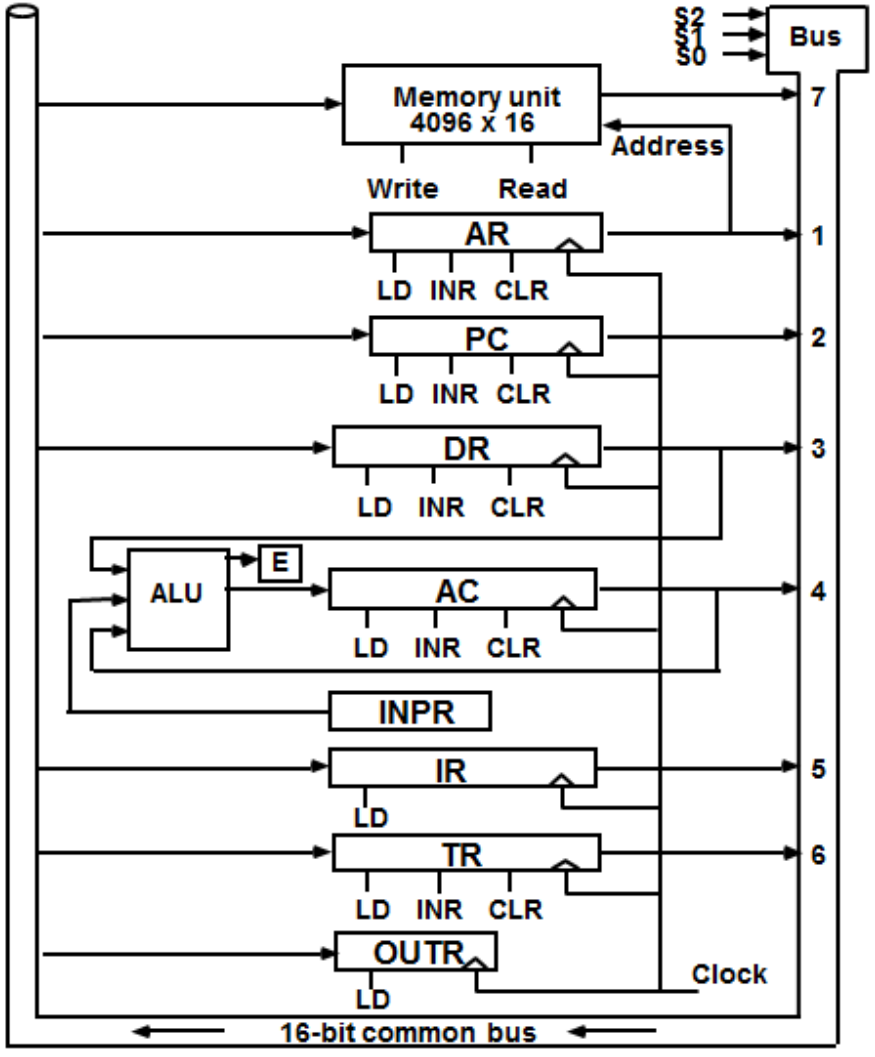
A Simple Computer Architecture



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- $T_3 D_6 I' : do\ nothing$
- $T_4 D_6 : TR \leftarrow AC$
- $T_5 D_6 : DR \leftarrow M[AR], AR \leftarrow AR + 1$
- $T_6 D_6 : AC \leftarrow DR, DR \leftarrow M[AR]$
- $T_7 D_6 : AC \leftarrow AC + DR, AR \leftarrow AR + 1\ , DR \leftarrow TR$
- $T_8 D_6 : M[AR] \leftarrow AC$
- $T_9 D_6 : AC \leftarrow DR$

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