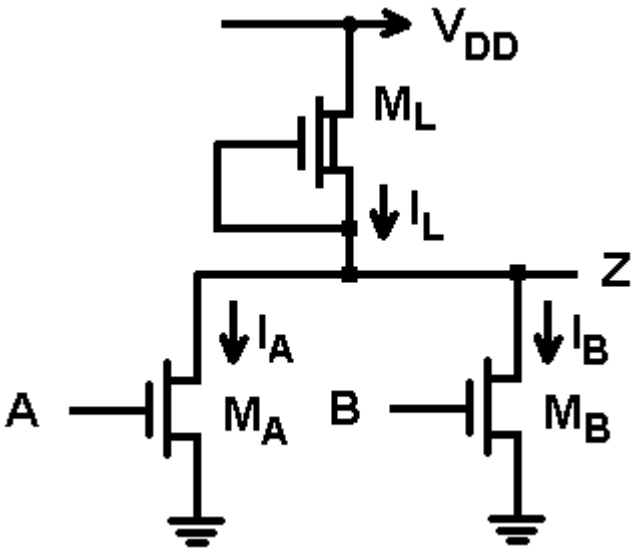
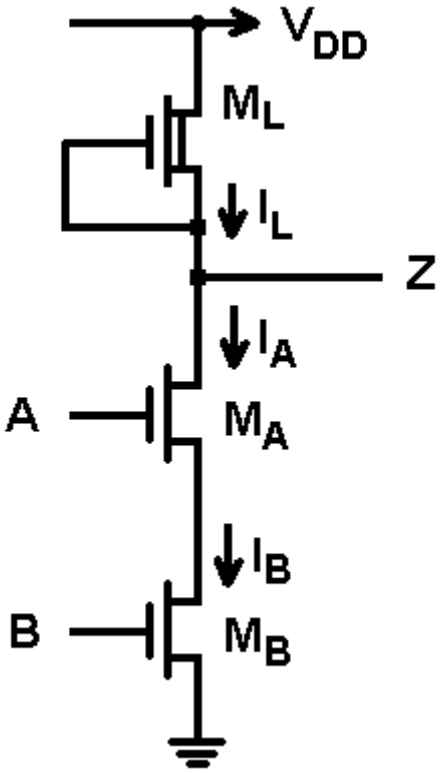
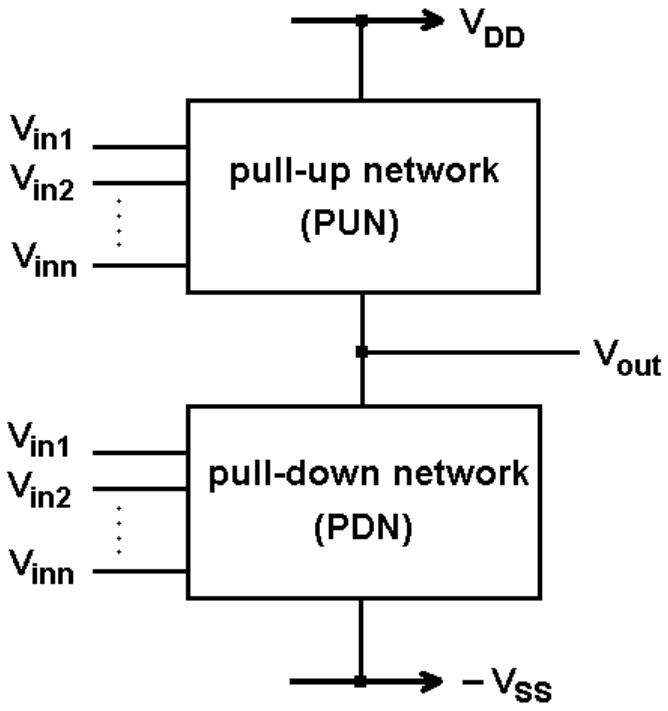
2-input NMOS NOR gate



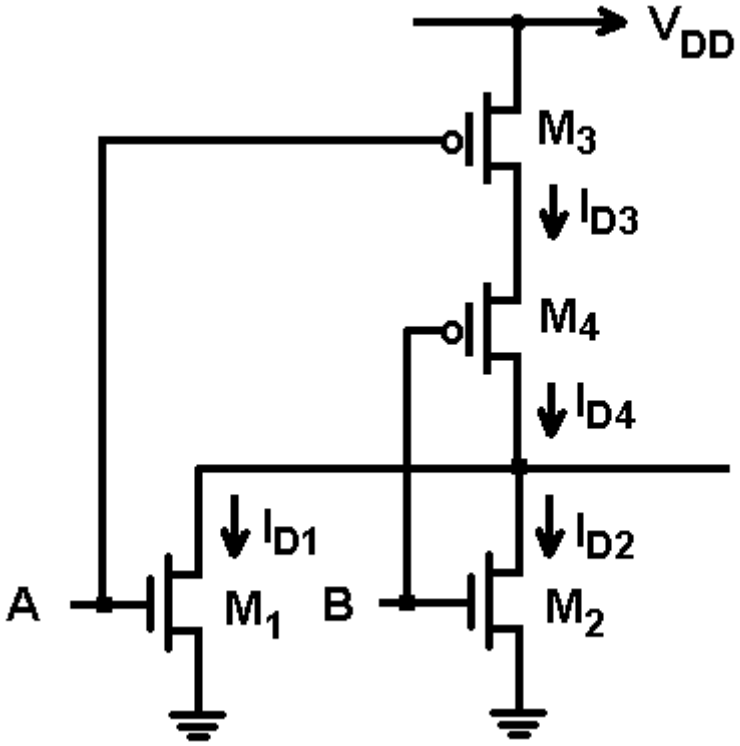
2-input NMOS NAND gate



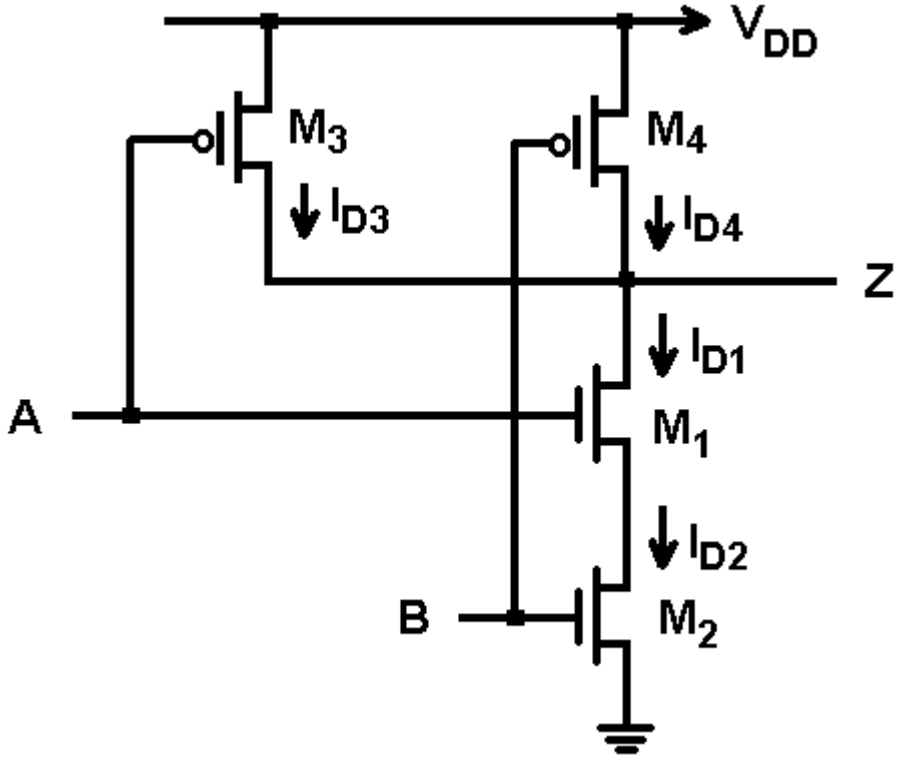


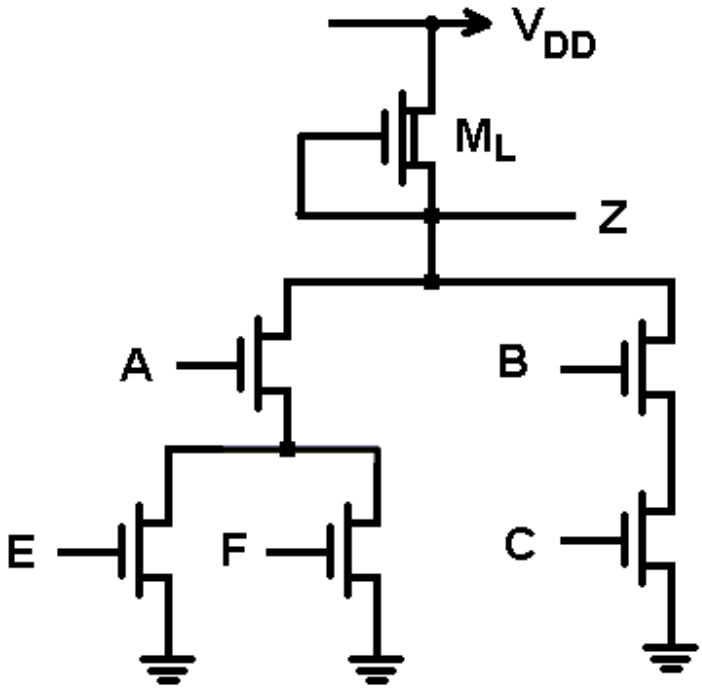
General structure of CMOS gates

2-input CMOS NOR gate



2-input CMOS NAND gate





An example complex NMOS logic circuit

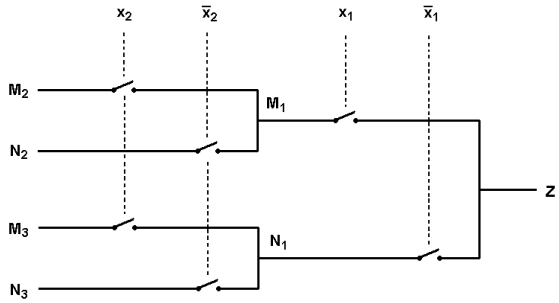
A	B	C	E	F	Z	V_{out}
0	0	0	0	0	1	V_0
0	0	0	0	1	1	V_1
0	0	0	1	0	1	V_2
0	0	0	1	1	1	V_3
0	0	1	0	0	1	V_4
0	0	1	0	1	1	V_5
0	0	1	1	0	1	V_6
0	0	1	1	1	1	V_7
0	1	0	0	0	1	V_8
0	1	0	0	1	1	V_9
0	1	0	1	0	1	V_{10}
0	1	0	1	1	1	V_{11}
0	**1**	**1**	**0**	**0**	**0**	**V_{12}**
0	1	1	0	1	0	V_{13}
0	1	1	1	0	0	V_{14}
0	1	1	1	1	0	V_{15}
1	0	0	0	0	1	V_{16}
1	**0**	**0**	**0**	**1**	**0**	**V_{17}**
1	**0**	**0**	**1**	**0**	**0**	**V_{18}**
1	**0**	**0**	**1**	**1**	**0**	**V_{19}**
1	0	1	0	0	1	V_{20}
1	0	1	0	1	0	V_{21}
1	0	1	1	0	0	V_{22}
1	0	1	1	1	0	V_{23}
1	1	0	0	0	1	V_{24}
1	1	0	0	1	0	V_{25}
1	1	0	1	0	0	V_{26}
1	1	0	1	1	0	V_{27}
1	1	1	0	0	0	V_{28}
1	**1**	**1**	**0**	**1**	**0**	**V_{29}**
1	**1**	**1**	**1**	**0**	**0**	**V_{30}**
1	**1**	**1**	**1**	**1**	**0**	**V_{31}**

A	B	C	E	F	Z	V_{out}
0	1	1	0	0	0	V_{12}
1	0	0	0	1	0	V_{17}
1	0	0	1	0	0	V_{18}
1	0	0	1	1	0	V_{19}
1	1	1	0	1	0	V_{29}
1	1	1	1	0	0	V_{30}
1	1	1	1	1	0	V_{31}

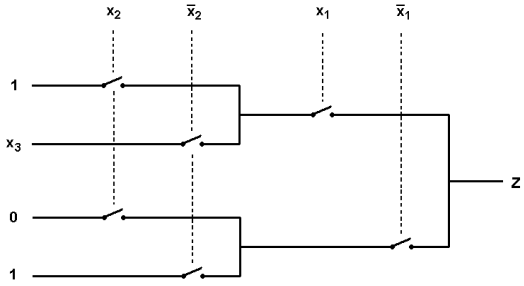
A	B	C	E	F	Z	V_{out}
0	1	1	0	0	0	V_{12}
1	0	0	0	1	0	V_{17}
1	0	0	1	0	0	V_{18}
1	0	0	1	1	0	V_{19}
1	1	1	0	1	0	V_{29}
1	1	1	1	0	0	V_{30}
1	1	1	1	1	0	V_{31}

The truth table of the example complex NMOS logic circuit

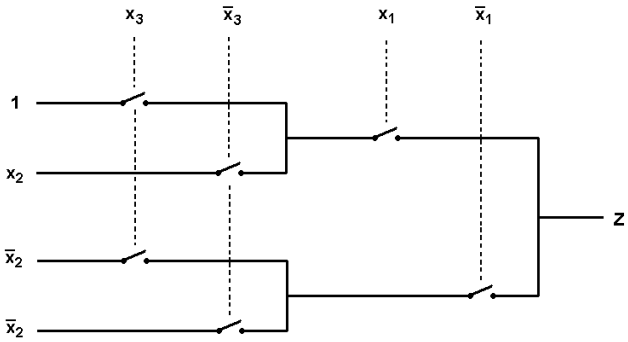
Pass logic



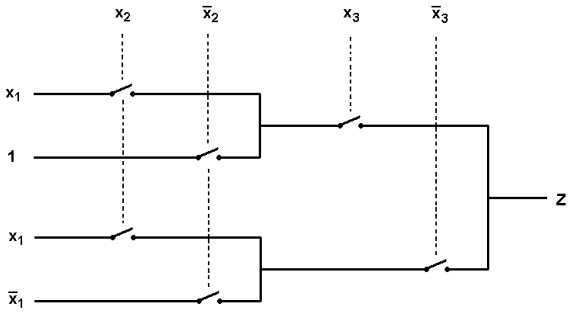
Pass logic circuit after Shannon decomposition applied to a logic function



An example pass logic circuit



Another realization of the example above



Another realization of the example above