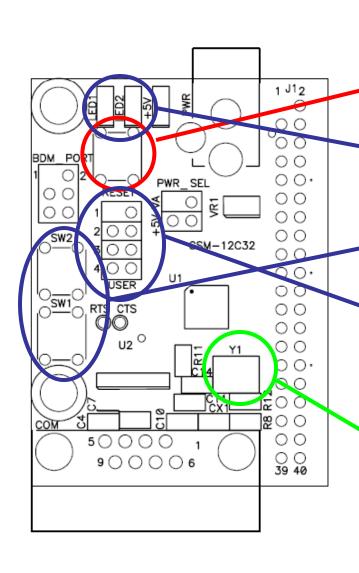


Karta güç verildiği zaman güç LED'i yanar



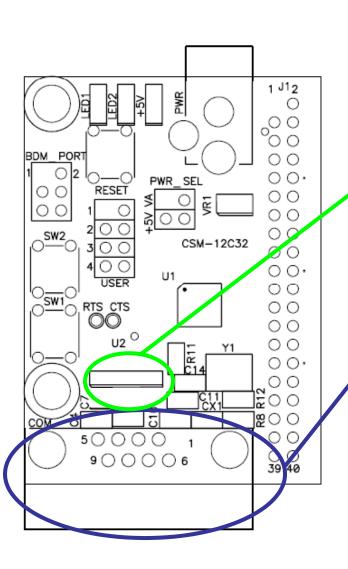
Reset düğmesi: asenkron olarak kartı resetler

Kullanıcı LED'leri

Kullanıcı tuşları

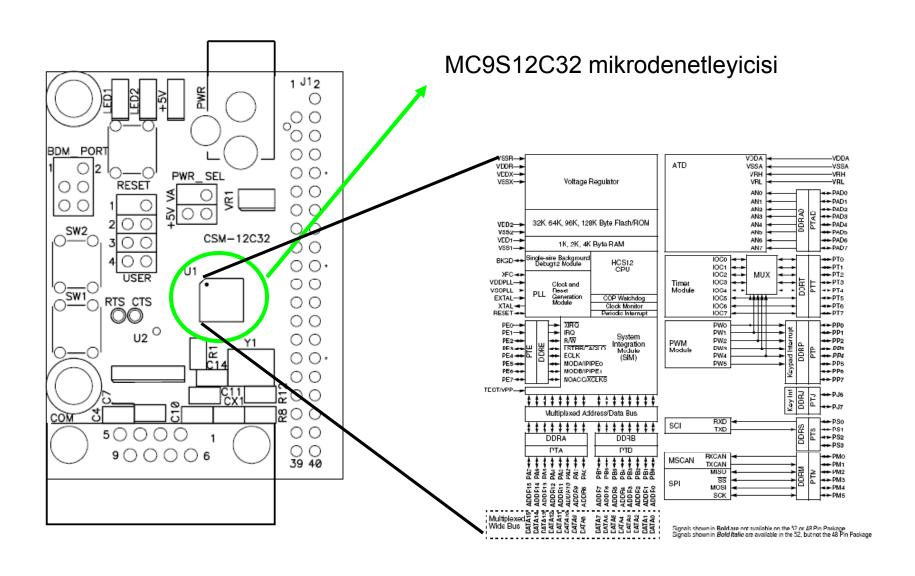
Jumper	On	Off	MCU Signal
User 1	Enable SW1	Disable SW1	PE0/XIRQ*
User 2	Enable SW2	Disable SW2	PP5 /KWP5
User 3	Enable LED1	Disable LED1	PA0
User 4	Enable LED2	Disable LED2	PB4

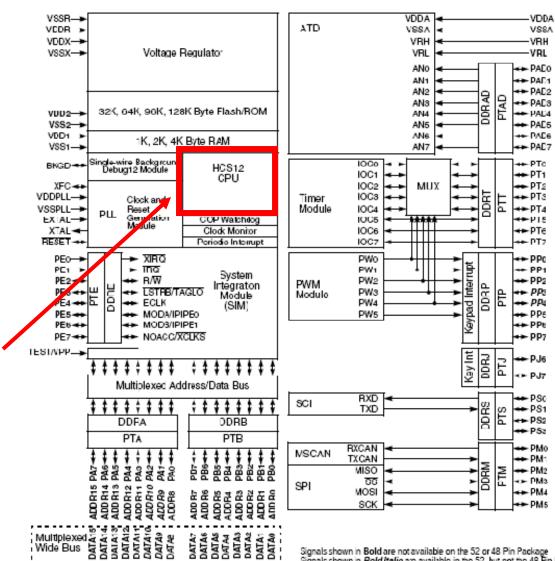
Osilator: 16 MHz. Frekansında osilasyon yapar. Kartın 8MHz saat hızında çalıştırır. Gömülü PLL ile daha yüksek saat hızları sağlanabilir



APS12C32SLK modülü – RS232 bağlantısı ile seri haberleşme

Bilgisayar bağlantısı

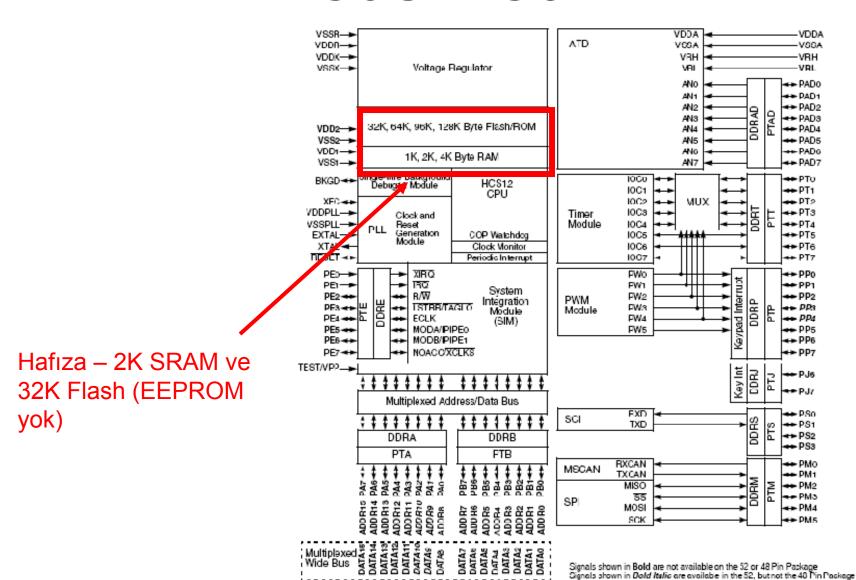




DATA:
DATAS
DATAS
DATAS
DATA3
DATA3
DATA2
DATA2

Mikroişlemci

Signals shown in **Bold** are not available on the 52 or 48 Pin Package Signals shown in Bold Italio are available in the 52, but not the 48 Fin Package



VSSR—➤

VDDN-→

VDDA

VSSA

VRH

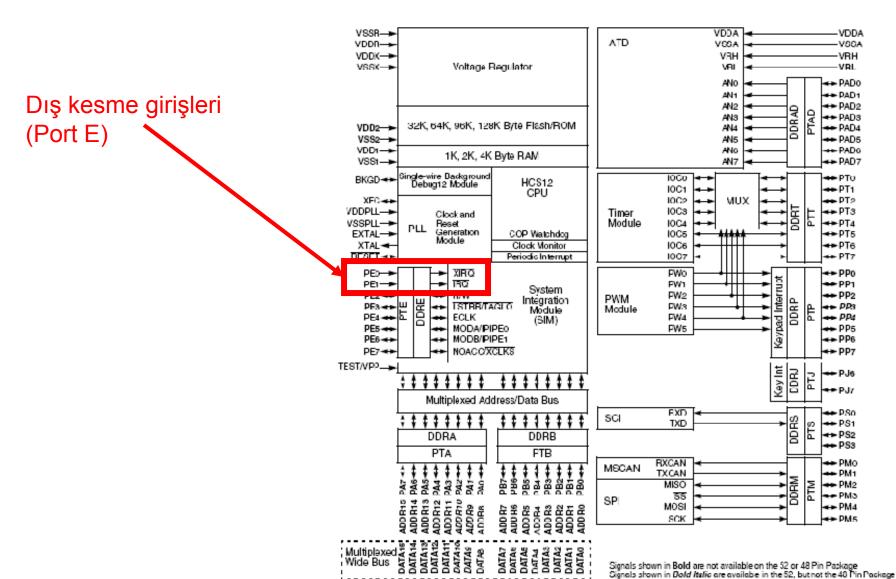
Signals shown in Bold are not available on the 52 or 48 Pin Package Signals shown in *Dold Italia* are available in the 52, but not the 40 Pin Package

ATD

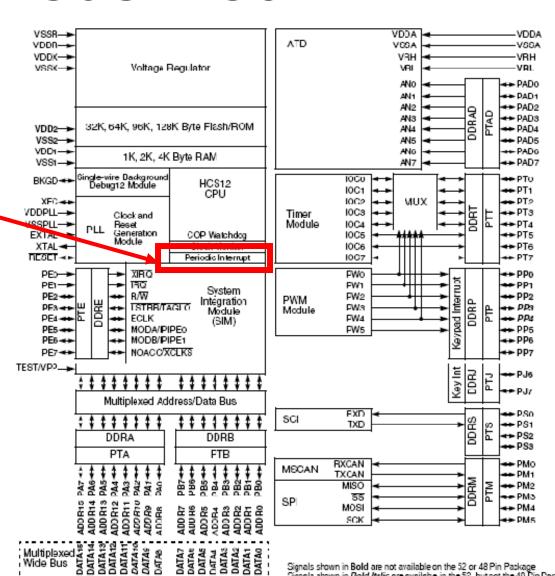
-VDDA

VSSA

VDDX—> VRH. VSSX-> Voltage Begulator VRI VRI. ANo ◆► PADo AN₁ PAD1 AN₂ <> PAD2 DDRAD AN3 ◆► PAD3 32K, 64K, 96K, 128K B/te Flash/ROM VDD2-> AN4 PAD4 VSS2-> AN₅ ◆► PAD5 $VDD1 \longrightarrow$ ANo PADG 1K, 2K, 4K Byte RAM AN7 PAD7 VSS1→ Single-wire Dackground Debug12 Module 48 girişli MC9S12C32'de PT∪ BKGD≪> HCS12 CPU I0C1 **↔** PT1 $10C_2$ MUX PT2 XFC-≪► bu bağlantılar 9 VDDPLL→ 10C3 PT3 Timer ᄪ Clock and VSSPLL→ Module IOC4 PT4 Reset PLL Generation Module EXTAL→ COP Watchdoo 10C5 <>PT5 bulunmamaktadır XTAL≪ Clock Monitor 10C6 <->PT6 RESET⊸> Periodic Interrupt 1007 PT7 XIRQ PWo <> PPo PE0→ PE1-IRQ PW1 PP1 System PE2≪ R/W PW₂ PP2 PWM. Intégration DDRP ISTBB/TAGLO PE3 <> PW3 → PP3 Module Module PE4-**ECLK** PW4 **→** PP4 (SIM) PE5 <→ MODA/PIPEo PW₅ PP5 MODB/IPIPE1 PE6 <>> <-> PP6 PE7≪⊁ NOACC/XCLKS <> PP7 TEST/VPP-> Key Int ------ PJ6 Multiplexed Address/Data Bus EXD DDRS SCI TXD → PS1 <> PS2 DDRA DDRB → PS3 PTA PTB RXCAN → PMo MSCAN TXCAN → PM1 DORM PTM MISO PM2 ~~ PM3 88 SP MOSI <-> PM4 SCK Multiplexed F Wide Bus

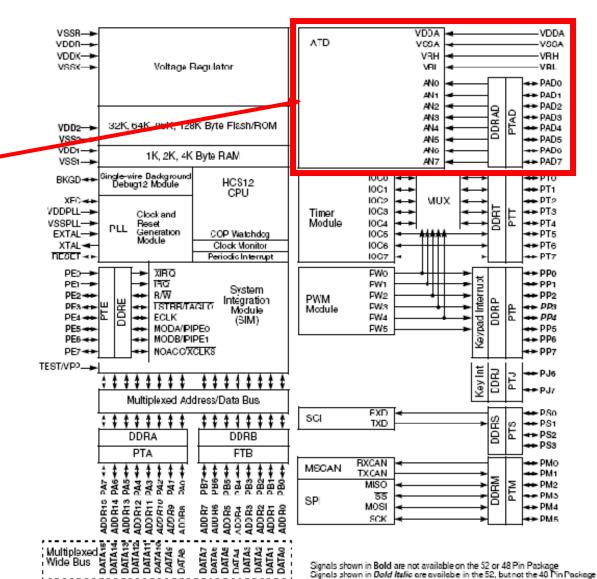


Gerçek zamanlı kesme modülü (RTI)

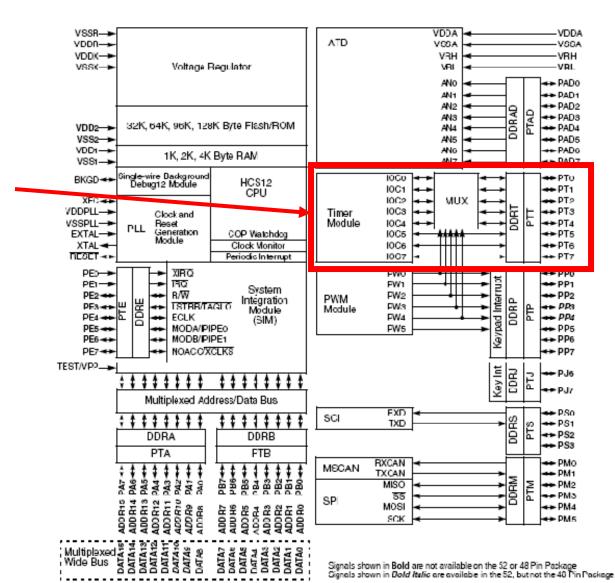


Signals shown in **Bold** are not available on the 52 or 48 Pin Package Signals shown in *Bold Italia* are available in the 52, but not the 40 Pin Package

Analog-sayısal dönüştürüsü – Çıkışlar PAD portundan

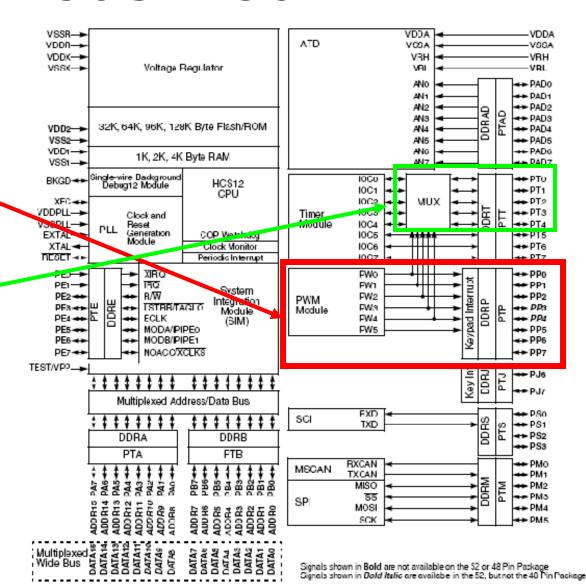


Zamanlama modülü (TIM) – Port T



Darbe genişlik modülasyon modülü.

Giriş/Çıkış TIM ile paylaşılıyor. MODRR register ayarları ile çıkışların TIM/PWM olacağı ayarlanıyor



VSSR—➤

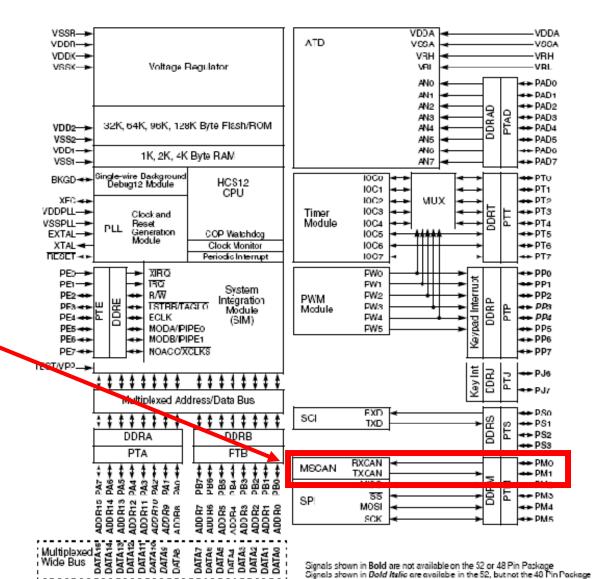
ATD VDDR→ VSSA VSSA VDDX—➤ VRH VRH. VSSX-> Voltage Begulator VRI VRI. ANo ◆► PADo AN₁ PAD1 AN₂ ◆► PAD2 DDRAD PTAD AN3 ◆► PAD3 32K, 64K, 96K, 128K B/te Flash/ROM VDD2-> AN4 PAD4 VSS2-> AN₅ ◆► PAD5 $VDD1 \longrightarrow$ ANo → PADo 1K, 2K, 4K Byte RAM AN7 PAD7 VSS1-> Single-wire Dackground Debug12 Module PT∪ BKGD<> HCS12 CPU I0C1 PT₁ **→** PT₂ XFC-≪+ $10C_2$ MUX DBRT VDDPLL→ 10C3 PT3 Timer ᄪ Clock and VSSPLL→ Module IOC4 <> PT4 Reset PLL Generation Module EXTAL→ COP Watchdoo 10C5 <>PT5 XTAL≪ Clock Monitor 10C6 PTe RESET⊸> Periodic Interrupt 1007 PT7 XIRQ PWo PE0→ → PPo PE1-IRQ PW1 PP1 System PE2≪ R/W PW₂ PP2 PWM. Intégration DDRP DDRE ISTBB/TAGLO → PP3 PE3 <> PW3 Module Module PE4-**ECLK** PW4 **→** PP4 (SIM) PE5 ≪ PW₅ PP5 MODA/PIPEO MODB/IPIPE1 <-> PP6 PE7≪ NOACC/XCLKS <> PP7 TEST/VPP-> 00 RJ * * * * * * * * Multiplexed Address 2 eta Bus EXD ⇔ PSo SCI DDRS PTS TXD → PS1 <> PS2 DDRA DDRB PS3 PTA PTB MSCAN TXCAN → PM1 DDRM 8 4 8 8 8 4 8 PTM MISO PM2 ~~ PM3 88 SP ADDR11 ADDR10 ADDR9 ADDR8 MOSI <-> PM4 SCK DATA SPECIAL PROPERTY OF THE P Signals shown in **Bold** are not available on the 52 or 48 Pin Package

VDDA

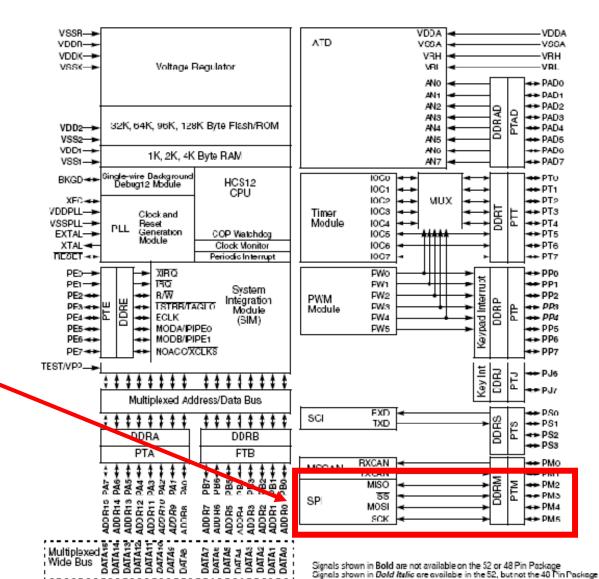
Signals shown in *Bold Italia* are available in the 52, but not the 40 Pin Package

-VDDA

Asenkron seri iletişim (SCI) modülü – Port S

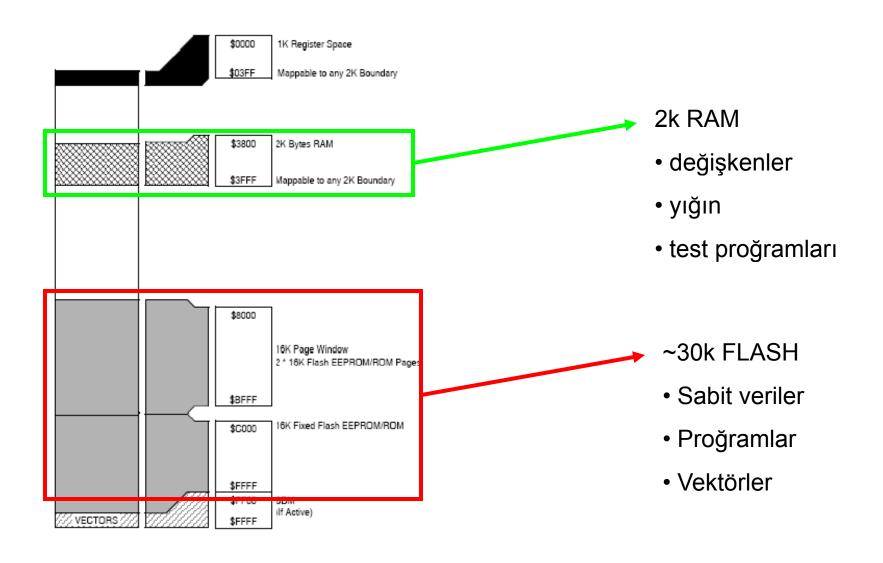


Denetleyici alan ağı (MCAN) modülü



Sekron çevre arayüz modülü (SPI) – Port M

MC9S12C32 - Hafıza



Önümüzdeki Hafta

- Kartı ve bilgisayar proğramını tanıtmak için kısa bir deney
- Deney için gerekli döküman Ninova'da olacak
- HC12S komut seti ve diğer dokümanlar Ninova'da var