İTÜ
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**BLG 322E Computer Architecture**

**Homework 4**

**Direct Memory Access**

2 DMA controllers will be connected to a MC68000 processor. DMACs will send interrupt request from the 2nd level when necessary. DMA controllers have following connections; interrupt request output (IRQ'), bus request (BR') output and bus grant (BG') input.

1. Design the hardware described above with necessary input and output connections. You should show the bus arbiter detailed, while other decoder circuits can be shown as block diagram.
2. How does interrupt priority controller decide priority? Explain.
3. In this system, how does microprocessor understand that it can use the bus? Explain briefly.
4. What is the relation between "TAS" instruction and MC68000 hardware with DMAC? Explain.

## Submission Date: 23.04.2014, Wednesday, 17:00

- Homeworks will be submitted to the homework submission box in the secretary of Computer Engineering Department.
- Homeworks should be done individually. Involving plagiarism may result with negative grade.
- Late submissions will not be considered.