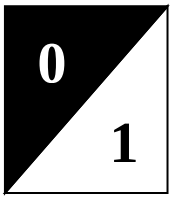
ISTANBUL TECHNICAL UNIVERSITY



COMPUTER ENGINEERING

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO: 8

EXPERIMENT NAME: SEQUENTIAL CIRCUIT DESIGN

EXPERIMENT DATE : 19.04.2013

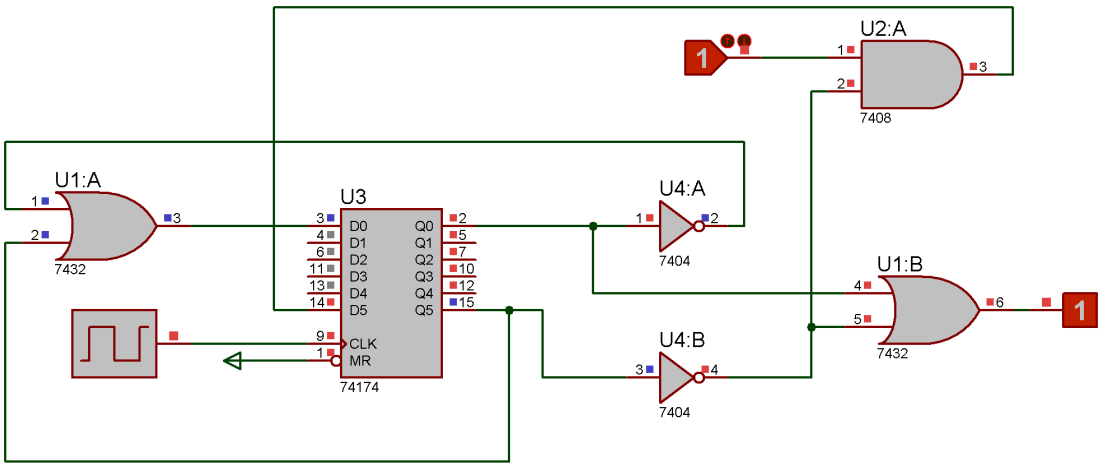
GROUP NO: 6

STUDENTS WHO DID THE EXPERIMENT:

Student no	Name	Surname
040100113	MUSTAFA	UÇAR
040100117	TUĞRUL	YATAĞAN
040100124	EMRE	GÖKREM

ASSISTANT NAME WHO ASSISTED THE EXPERIMENT: DENİZ DEMİRAY

1)



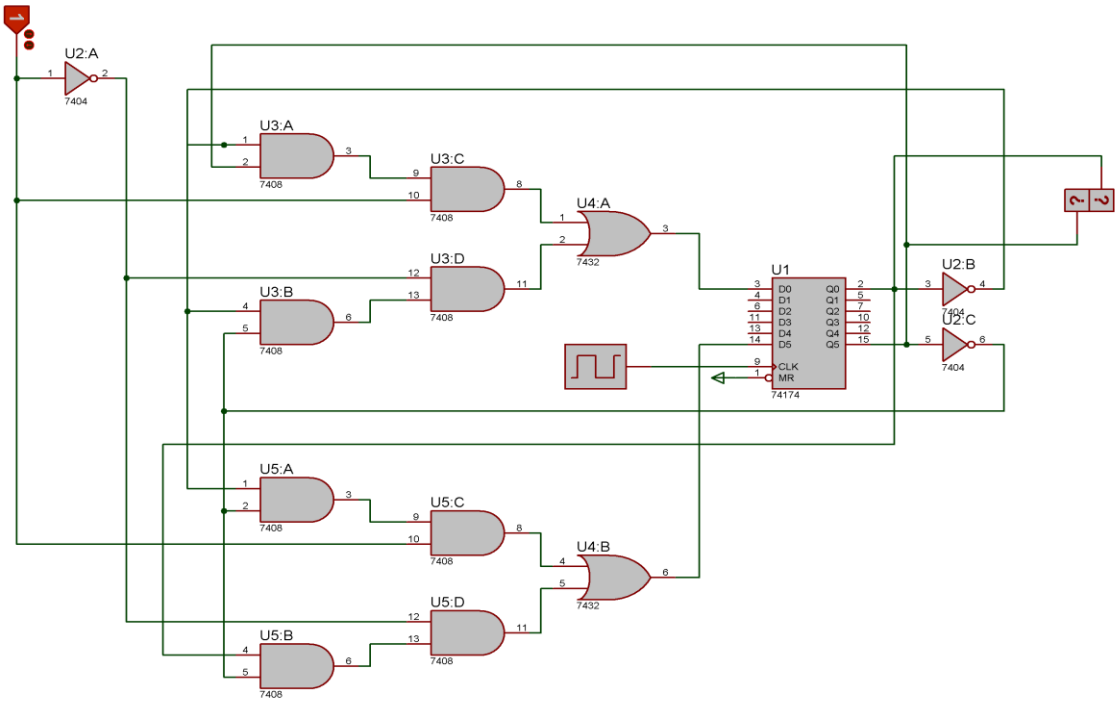
$Q1^{+} = Q1' + Q2$

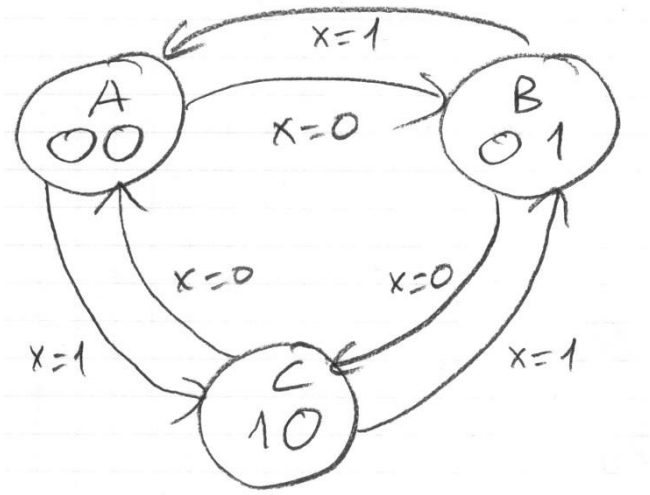
$Q2^{+} = X.Q2'$

$Z = Q1 + Q2'$

$Q1^{+}Q0^{+}/Z$		
Q1Q0\X	**0**	**1**
A – 00	01,1	11,1
B – 01	00,0	10,0
C – 11	01,1	01,1
D - 10	01,1	01,1

2)





S'Z		
S\X	**0**	**1**
A	B	C
B	C	A
C	A	B

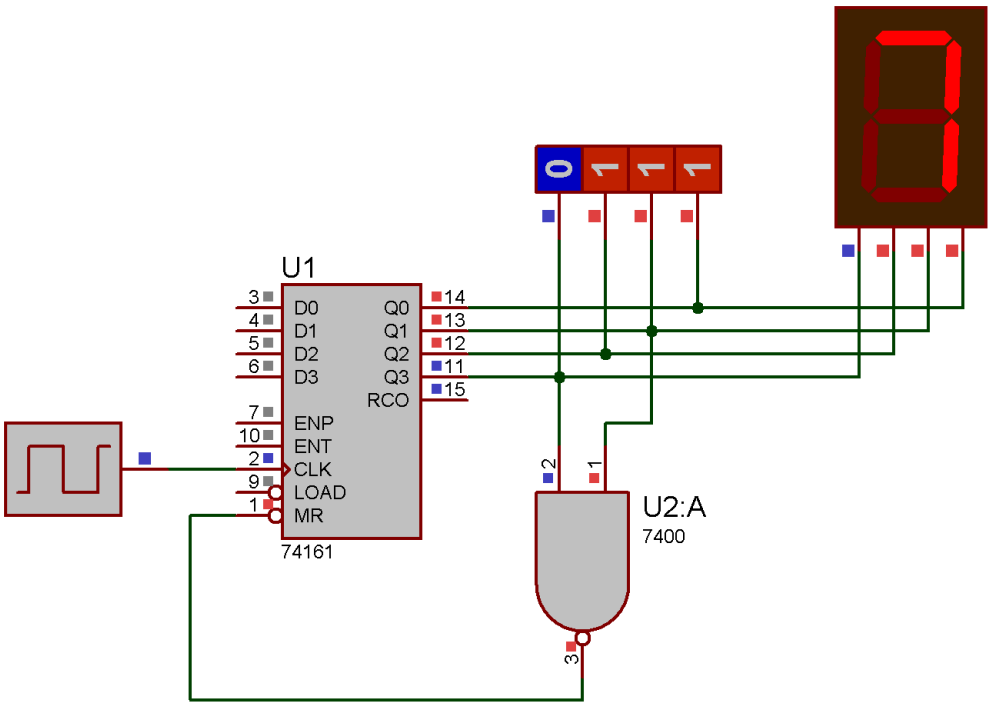
$Q1^+ Q0^+$		
Q1Q0\X	**0**	**1**
00	01	10
01	10	00
10	00	01

D1		
Q1Q0\X	**0**	**1**
00	0	1
01	1	0
10	0	0

D0		
Q1Q0\X	**0**	**1**
00	1	0
01	0	0
10	0	1

D1 = X'Q0Q1' + XQ0'Q1' = Q1'(XQ0' + x'Q0)
D0 = X'Q0Q1' + XQ0'Q1 = Q0'(XQ1 + X'Q1')

3)



When 4th and 2nd bits are becomes 1, it means count is come to 1010. Because 1010 is smallest number that 4th and 2nd bits are 1. If both of them are 1, NAND gate will reset the counter.

4)