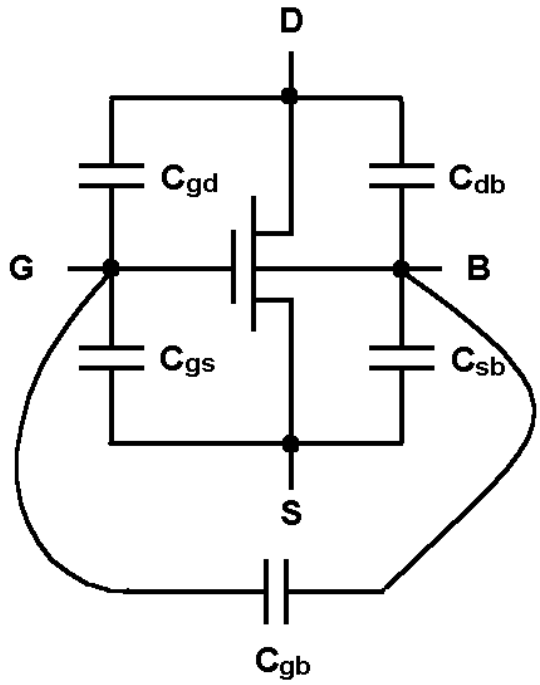
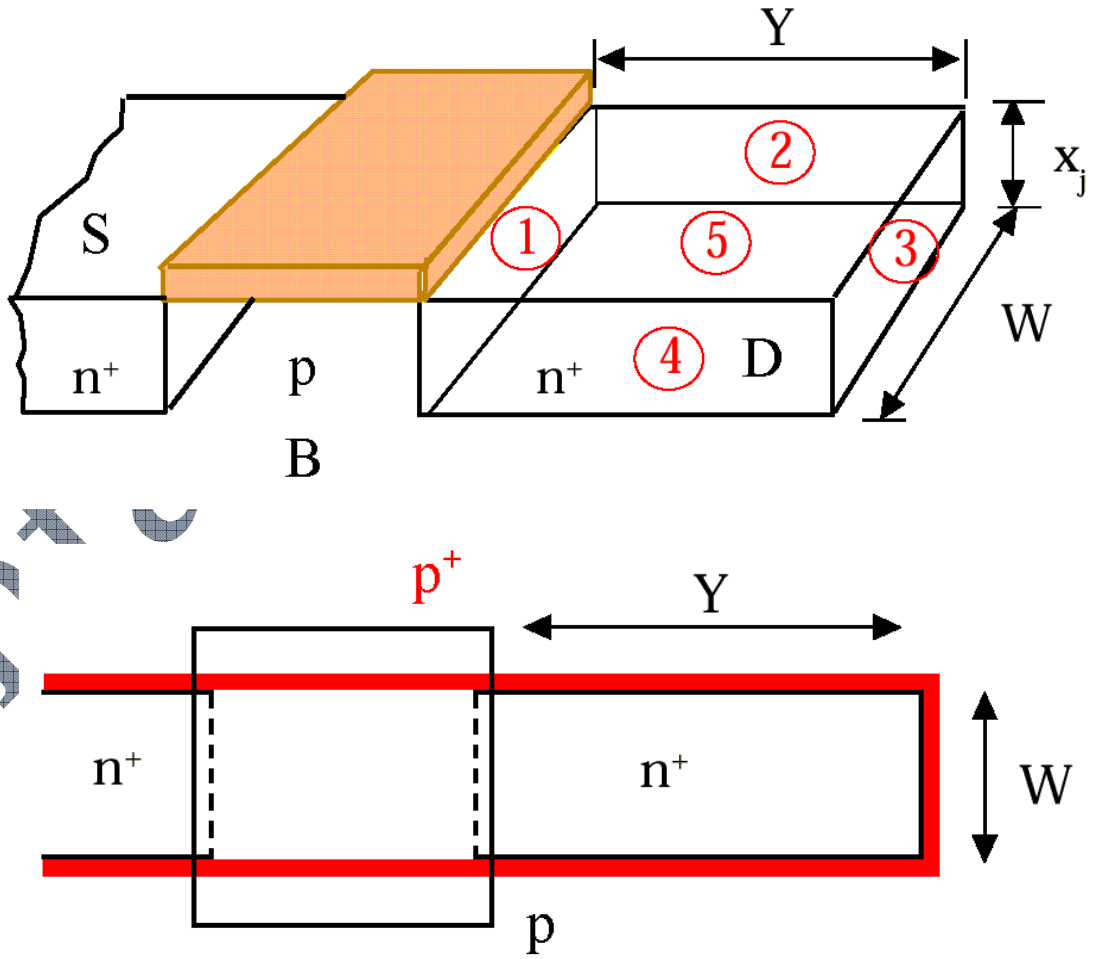
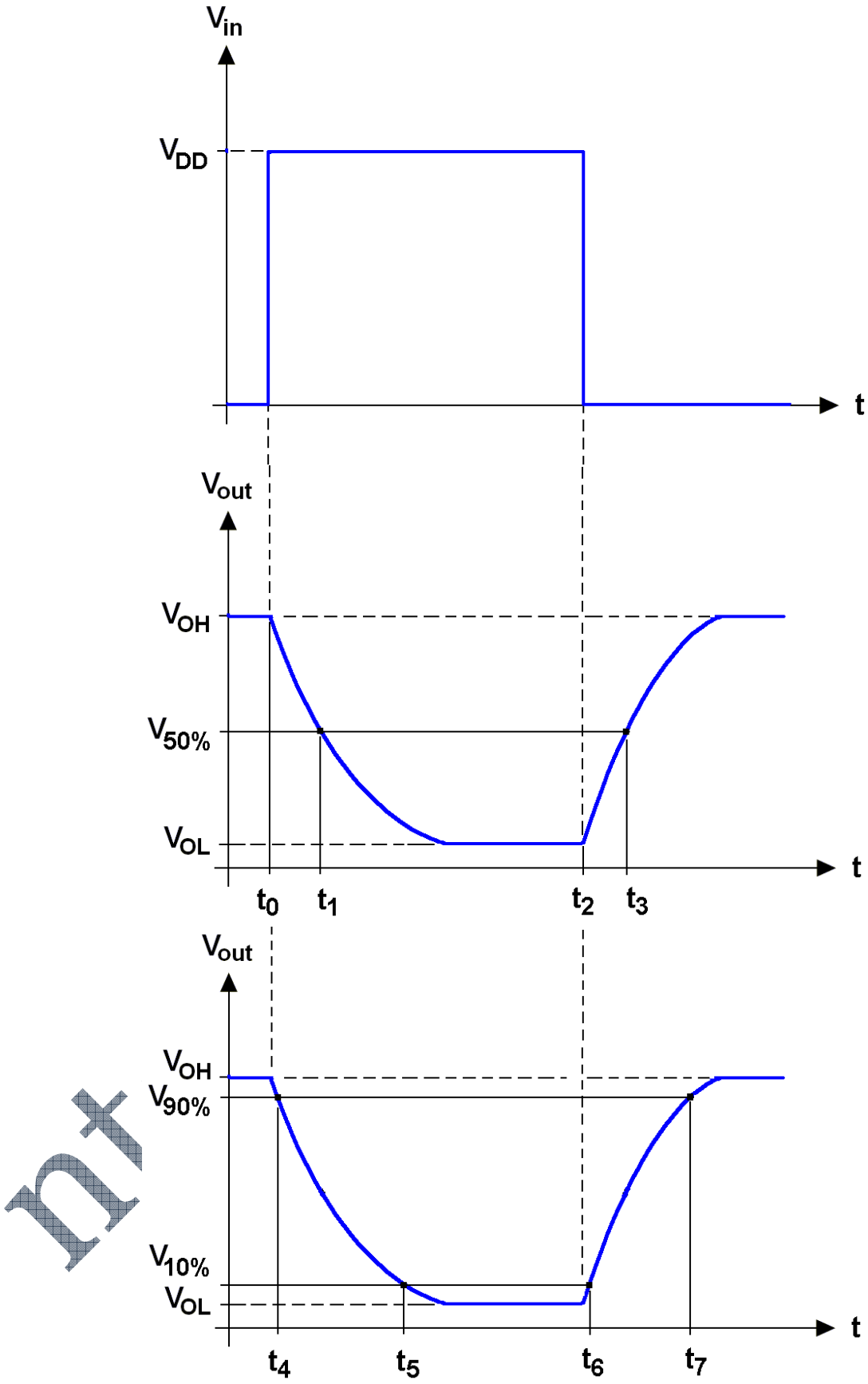


MOSFET capacitances



Cross-section and top view of an NMOS transistor



Definition of propagation delay, rise time and fall time

Propagation delay

For all inverter types:

$$\tau_{PHL} = \frac{C_{tot}}{k_D (V_{OH} - V_{tD})} \left[\frac{2V_{tD}}{V_{OH} - V_{tD}} + \ln\left(\frac{4(V_{OH} - V_{tD})}{V_{OH} + V_{OL}} - 1 \right) \right]$$

For the CMOS inverter:

$$\tau_{PHL} = \frac{C_{tot}}{k_n (V_{DD} - V_{tn})} \left[\frac{2V_{tn}}{V_{DD} - V_{tn}} + \ln\left(\frac{4(V_{DD} - V_{tn})}{V_{DD}} - 1 \right) \right]$$

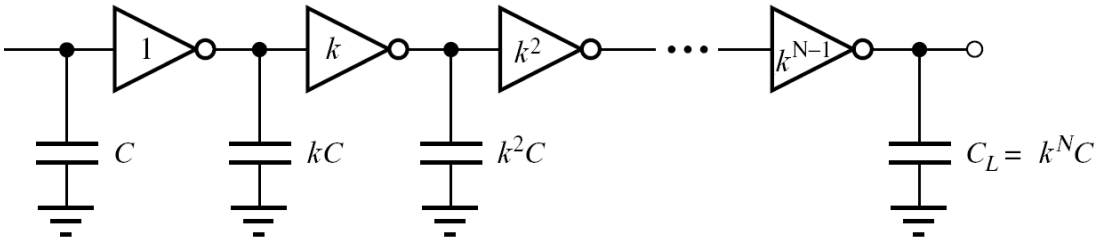
For the depletion-mode NMOS-loaded inverter:

$$\tau_{PLH} = \frac{C_{tot}}{k_L |V_{tL}|} \left[\frac{2(V_{DD} - |V_{tL}| - V_{OL})}{|V_{tL}|} + \ln\left(\frac{2|V_{tL}|}{V_{DD} - V_{50\%}} - 1 \right) \right]$$

For the CMOS inverter:

$$\tau_{PLH} = \frac{C_{tot}}{k_p (V_{DD} - |V_{tp}|)} \left[\frac{2|V_{tp}|}{V_{DD} - |V_{tp}|} + \ln\left(\frac{4(V_{DD} - |V_{tp}|)}{V_{DD}} - 1 \right) \right]$$

Cascade inverters for driving large capacitive loads



$$\tau_B = N k \tau_o$$

$$k^N = \frac{C_L}{C} \quad => \quad k = \left(\frac{C_L}{C}\right)^{1/N}$$

$$\tau_B = N \left(\frac{C_L}{C}\right)^{1/N} \tau_o$$

$$N_{\text{opt}} = \ln\left(\frac{C_L}{C}\right) \qquad k_{\text{opt}} = e \qquad \tau_{B\text{opt}} = \ln\left(\frac{C_L}{C}\right) e\, \tau_o$$

		normalized delay	
C_L/C	n	single inv	staged inverter
2.72	1	2.72	2.72
7.39	2	7.39	5.44
20.09	3	20.09	8.15
54.60	4	54.60	10.87
148.41	5	148.41	13.59
403.43	6	403.43	16.31