REVISION HISTORY

REVISION	DESCRIPTION	DATE
Rev. 1.0	Original	Jun 01, 1997
Rev. 1.1	128Kx 8 Low Voltage CMOS SRAM 之TN8106 body 已作fine tunings,將 I_{SB1}降為0.5uA(LL)、2uA(L)、Vcc range：3.0V~3.6V	Apr 05, 2000
Rev. 1.2	Add STSOP-I Package	Aug 29, 2000
Rev. 1.3	Modify the format of power consumption	Sep 01, 2000
Rev. 1.4	Add speed : -55ns	Dec 01, 2000
Rev. 1.5	Vcc min 3.1→2.7V	Mar 15, 2001
Rev. 1.6	1. The symbols CE1# ,OE# & WE# are revised as $\overline{CE1}$, $\overline{OE}$ & $\overline{WE}$ 2. Add Icc value of 55ns range(access time) 3. V_{OH} is revised as 2.2V 4. I_{SB1} is revised as 100μA	Jun 26, 2001
Rev. 1.7	Revised 32 pin 8mmx13.4mm STSOP Package Outline Dimension	Nov 26, 2001
Rev. 1.8	1. V_{OH} is revised as 2.4V (min.) 2. Revised Package Outline Dimension	Apr 9, 2002
Rev. 1.9	1. Add Operation temperature : Extended temp -20℃~80℃ 2. Add Order information for lead free product	May 09.2003

FEATURES

- Fast access time : 35/55/70ns (max.)
- Low power consumption :
  Operating current : 40/35/30mA (typical)
  Standby current : 2.5μA (typical) L-version
  0.5μA (typical) LL-version
- Power supply range : 2.7V to 3.6V
- Operating temperature :
  Commercial : 0℃~70℃
  Extended : -20℃~80℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 32-pin 600 mil PDIP
  32-pin 450 mil SOP
  32-pin 8x20 mm TSOP-1
  32-pin 8x13.4 mm STSOP

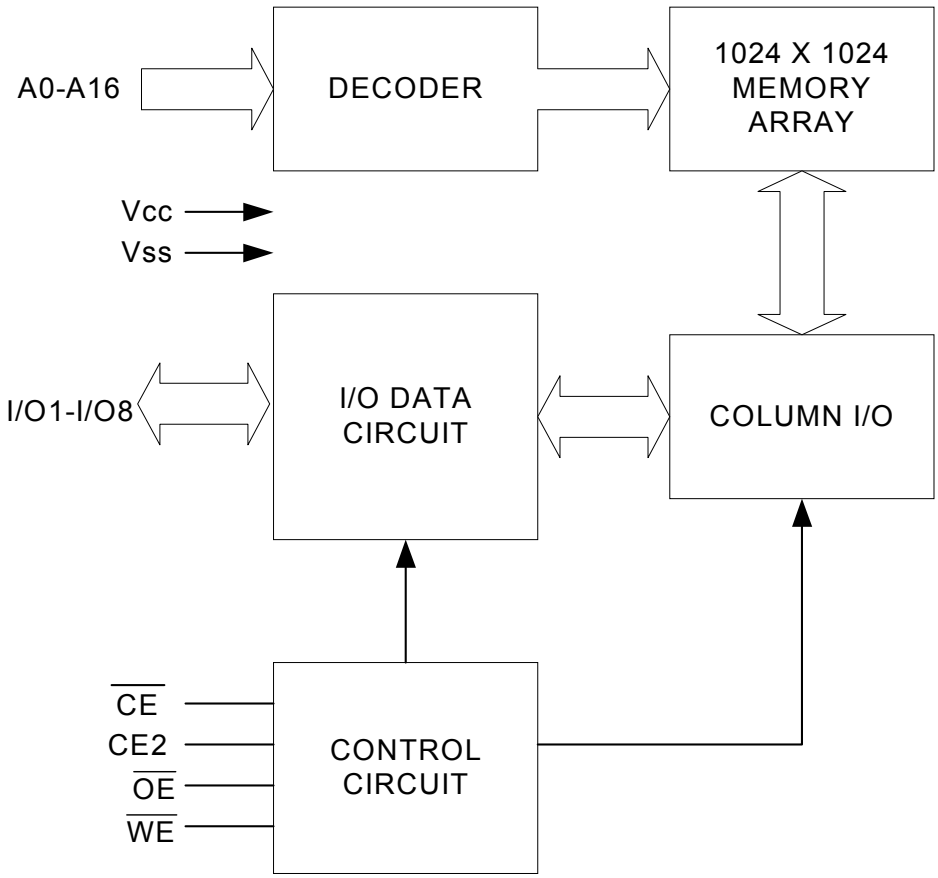
GENERAL DESCRIPTION

The UT62L1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

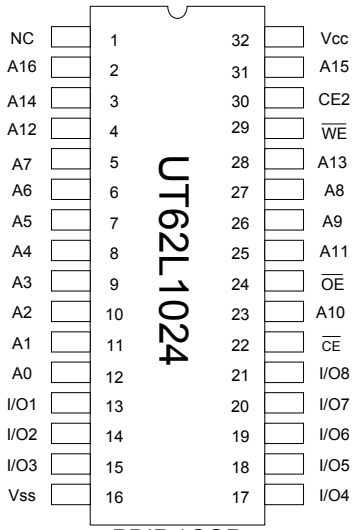
Easy memory expansion is provided by using two chip enable inputs.($\overline{CE}$,CE2) It is particularly well suited for battery back-up nonvolatile memory application.

The UT62L1024 operates from a single 2.7V~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

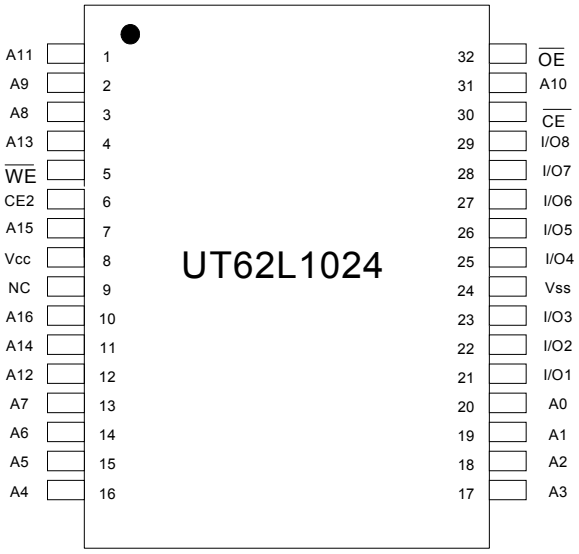
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PDIP / SOP



TSOP-I/STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$,CE2	Chip enable 1,2 Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss		V_{TERM}	-0.5 to +4.6	V
Operating Temperature	Commerical	T_A	0 to +70	℃
	Extended	T_A	-20 to +80	℃
Storage Temperature		T_{STG}	-65 to +150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 sec)		T_{solder}	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC} , I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC} , I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC} , I_{CC1}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V, T_A = 0℃ to +70℃/-20℃ to +80℃(E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}*1			2.0	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}*2			- 0.5	-	0.6	V
Input Leakage Current	I_{IL}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	µA
Output Leakage Current	I_{OL}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ $\overline{CE}$ =V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
Average Operating Power Supply Courrent	I_{CC}	Cycle time =Min. 100% Duty, $\overline{CE}$ =V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0mA	35	-	40	60	mA
			55	-	35	50	mA
			70	-	30	40	mA
	I_{CC1}	Cycle time = 1µs, 100% Duty, $\overline{CE} \leqq$0.2V,CE2$\geqq V_{CC}$-0.2V, $I_{I/O}$ = 0mA		-	-	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ =V_{IH} or CE2 = V_{IL}		-	-	1.0	mA
	I_{SB1}	$\overline{CE} \geqq V_{CC}$-0.2V or CE2$\leqq$0.2V	- L	-	2.5	100 20*4	µA
			- LL	-	0.5	40 10*4	µA

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 10ns.
2. Undershoot : Vss-3.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.
4. Those parameters are for reference only under 50□

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=50pF, I_{OH}/I_{OL}=-1mA/2mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V , T_A = 0℃ to +70℃/-20℃ to +80℃(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L1024-35		UT62L1024-55		UT62L1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	25	-	30	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	25	-	30	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns

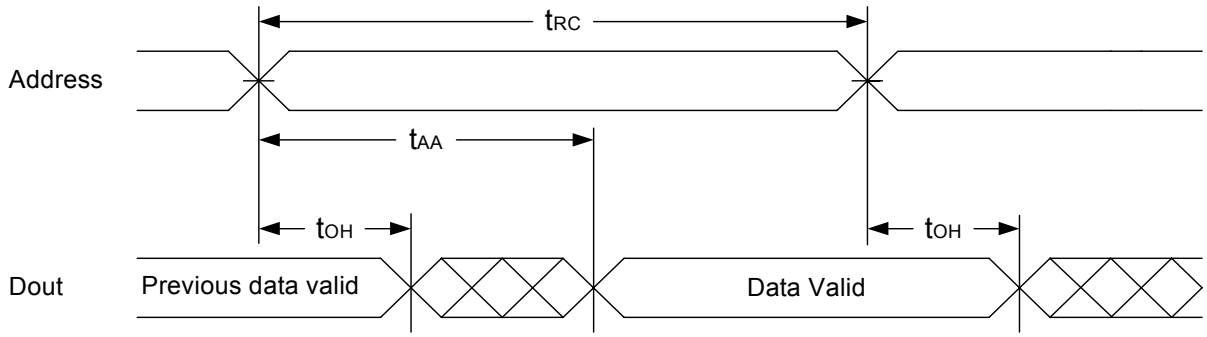
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L1024-35		UT62L1024-55		UT62L1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	40	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

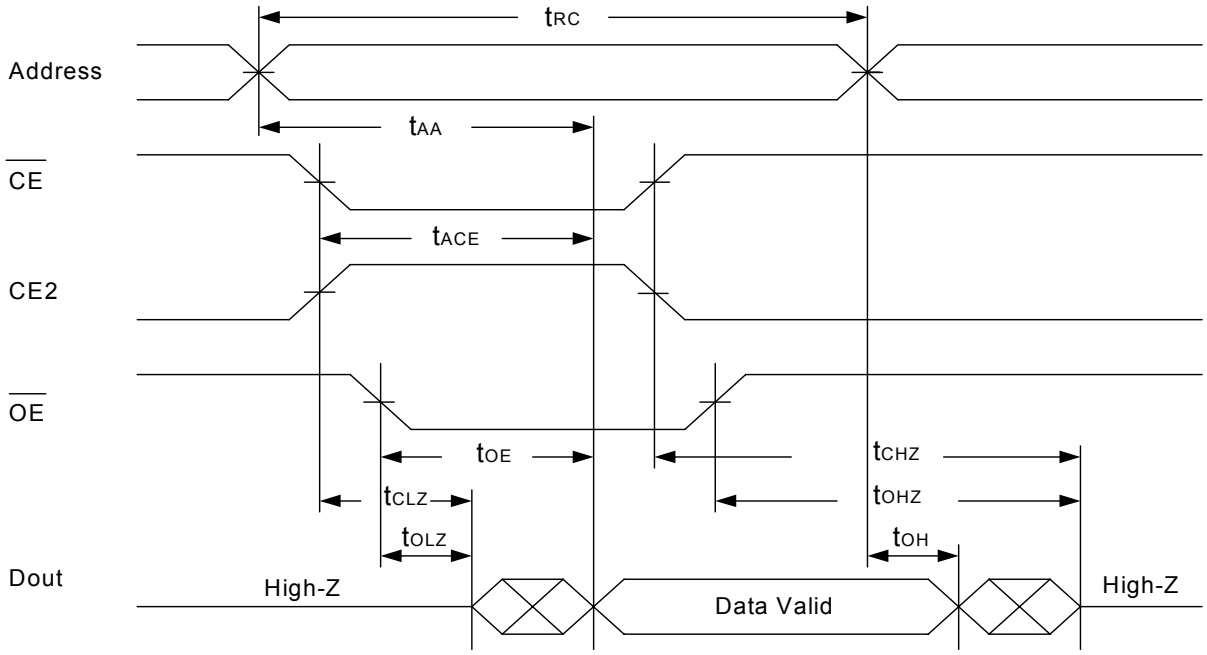
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



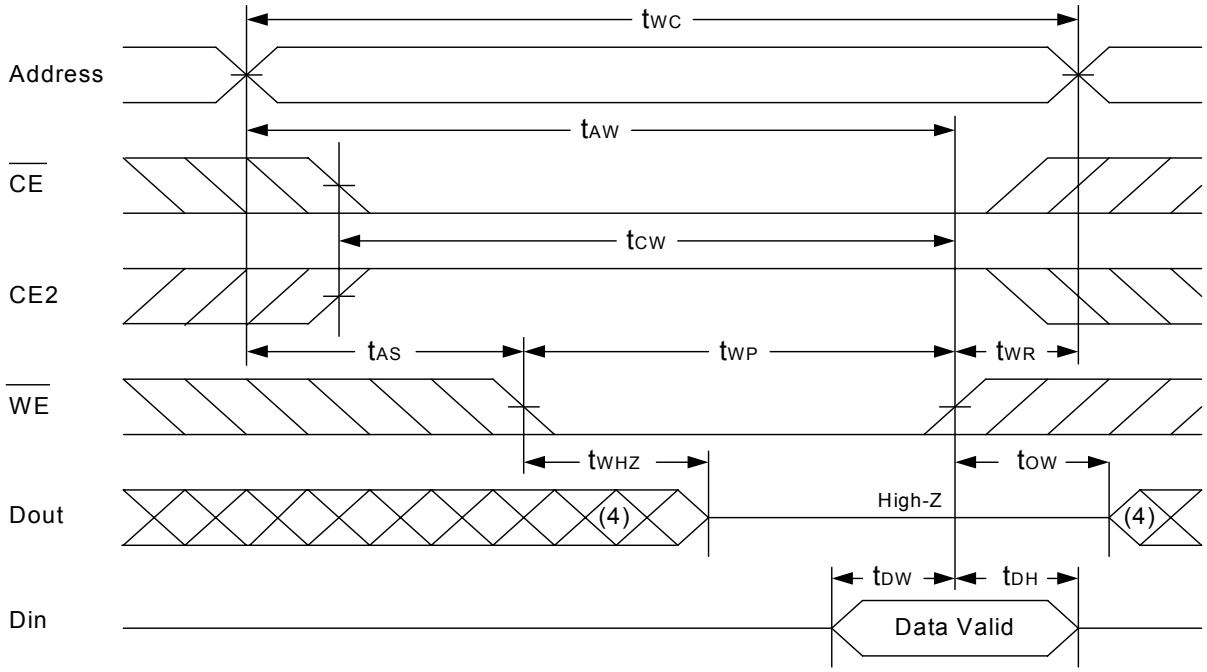
READ CYCLE 2 ($\overline{CE}$ and CE2 and $\overline{OE}$ Controlled) (1,3,4,5)



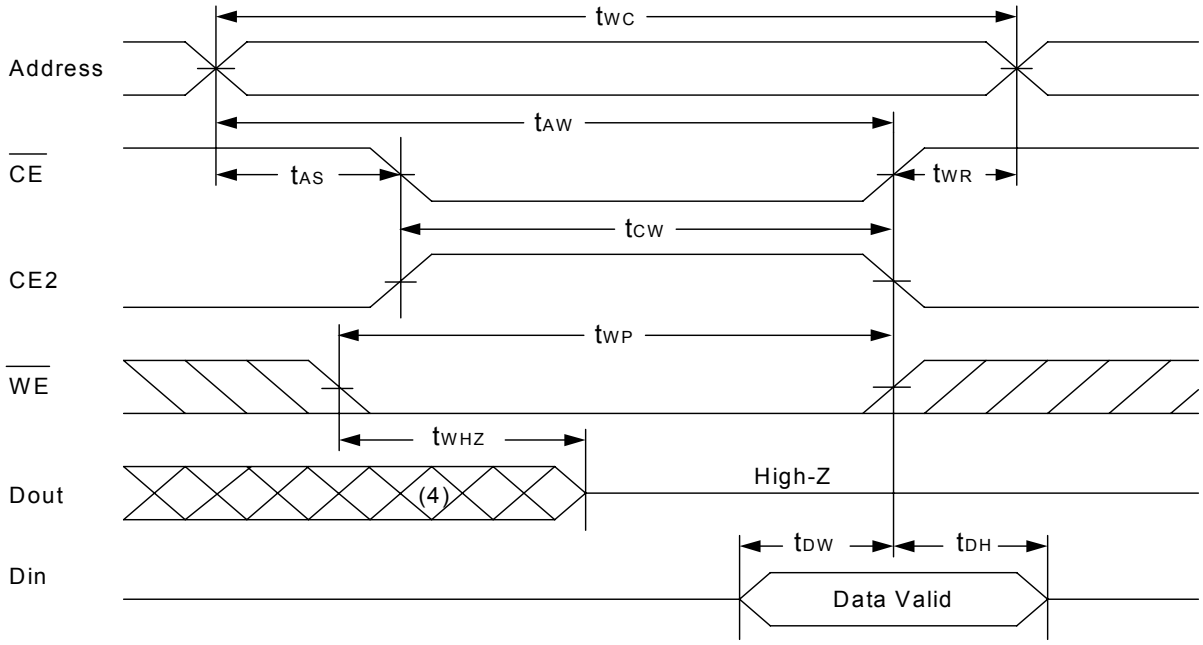
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low, CE2=high.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, CE2=high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ and CE2 Controlled) (1,2,5,6)



Notes :

1. $\overline{WE}$, $\overline{CE}$ must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, high CE2, low $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition and CE2 high transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

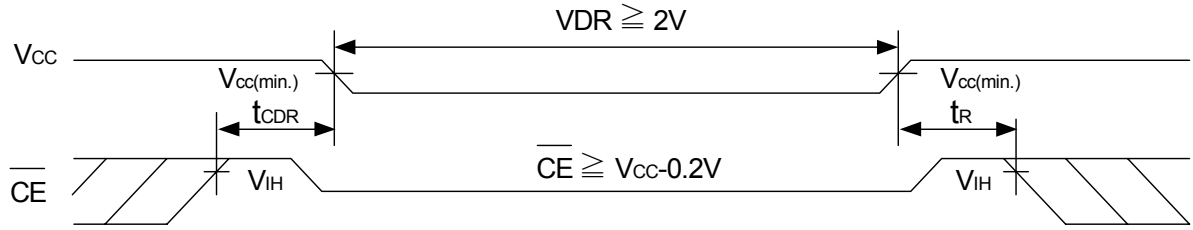
DATA RETENTION CHARACTERISTICS (T_A= 0℃ to +70℃/-20℃ to +80℃(E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V		2.0	-	3.3	V
Data Retention Current	I_{DR}	Vcc=2V $\overline{CE} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V	- L	-	1	40 10*	μA
			- LL	-	0.3	20 5*	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC}*	-	-	ns

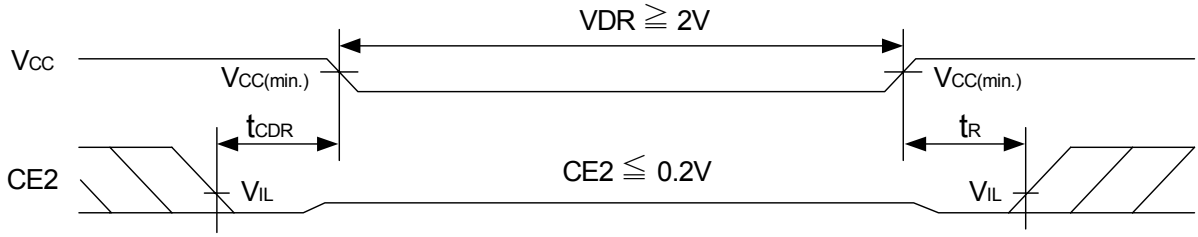
t_{RC}* = Read Cycle Time
*Those parameters are for reference only under 50℃

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE}$ controlled)

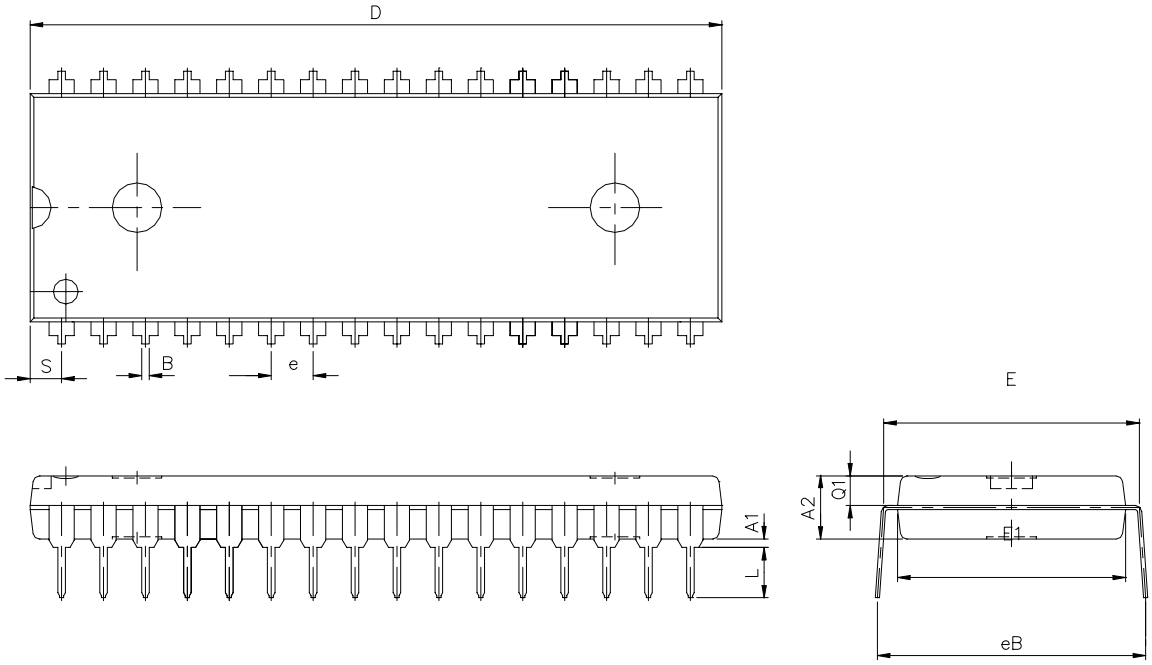


Low Vcc Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

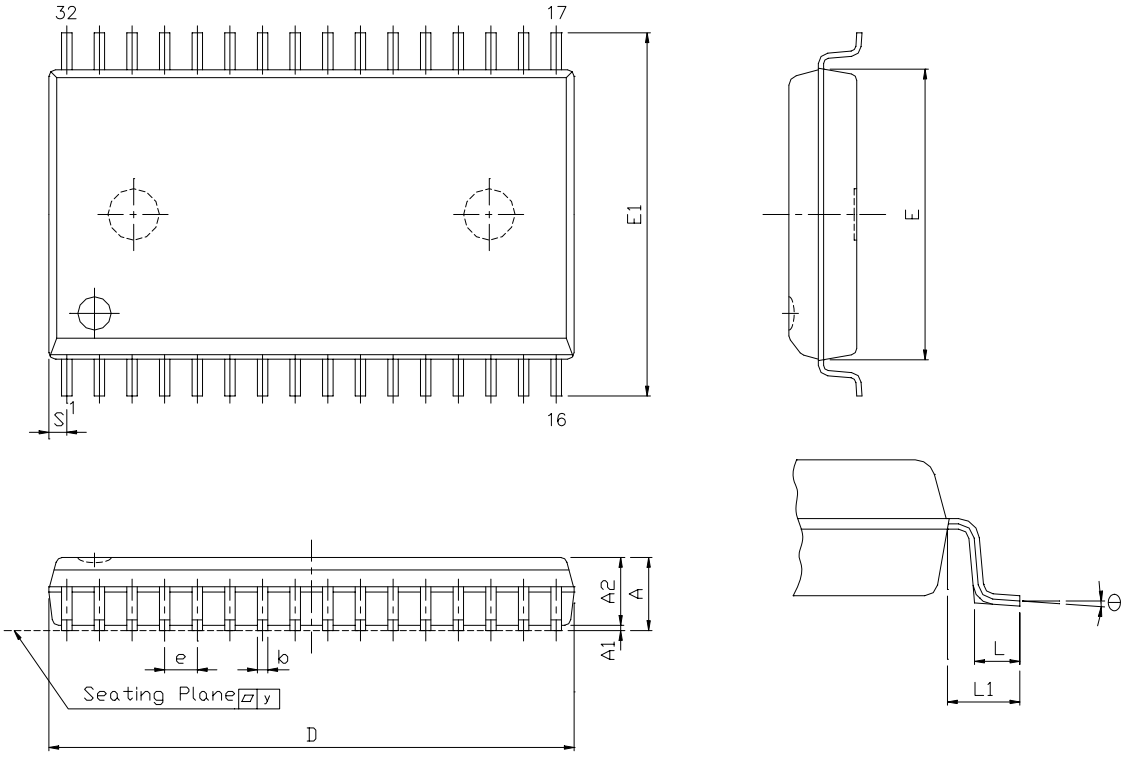
32-pin 600mil PDIP Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.150 ± 0.005	3.810 ± 0.127
B	0.018 ± 0.005	0.457 ± 0.127
D	1.650 ± 0.005	41.910 ± 0.127
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.544 ± 0.004	13.818 ± 0.102
e	0.100 (TYP)	2.540 (TYP)
eB	0.640 ± 0.020	16.256 ± 0.508
L	0.130 ± 0.010	3.302 ± 0.254
S	0.075 ± 0.010	1.905 ± 0.254
Q1	0.070 ± 0.005	1.778 ± 0.127

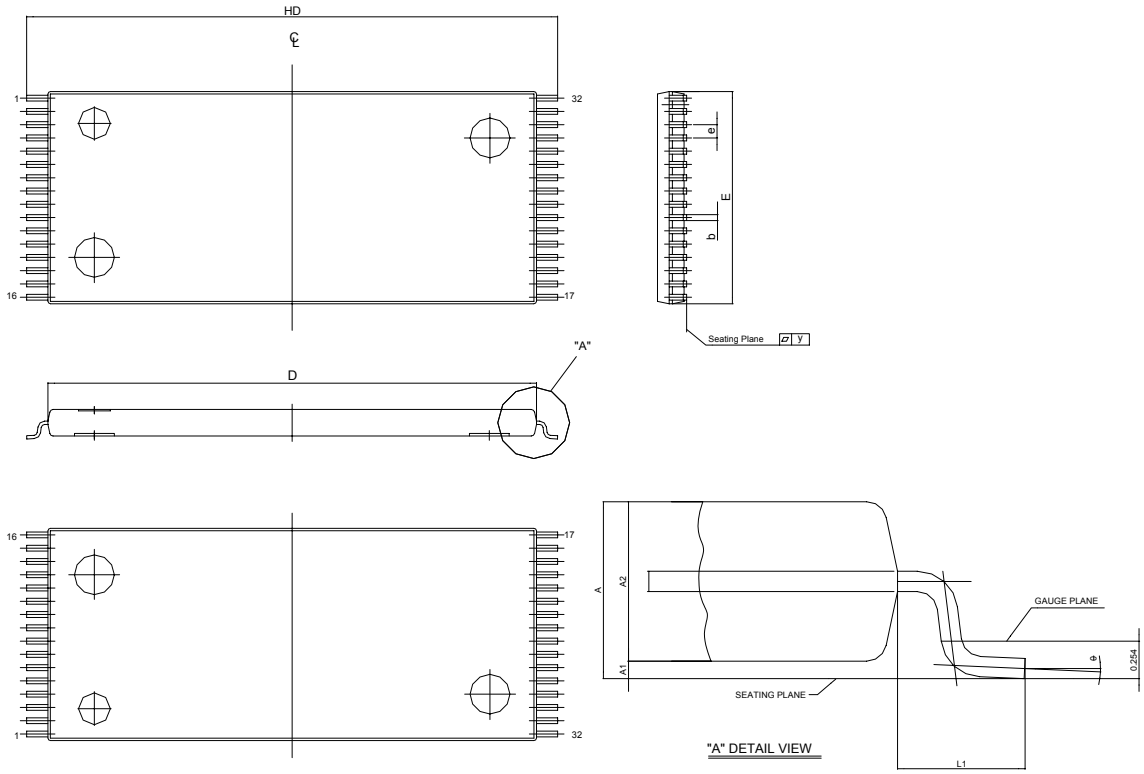
NOTE:
1. D/E1/S dimension do not include mold flash.

32-pin 450mil SOP Package Outline Dimension



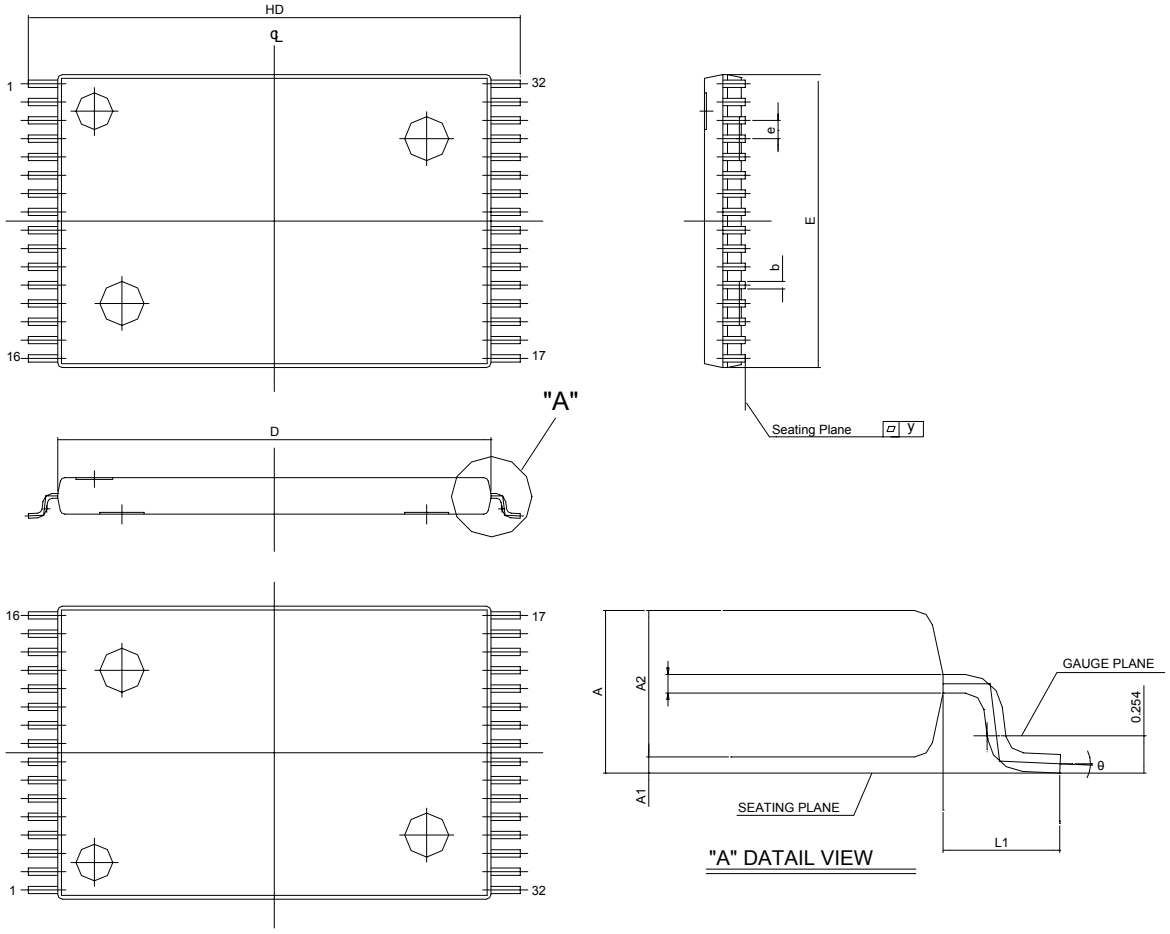
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004 (MIN)	0.102 (MIN)
A2	0.111 (MAX)	2.82 (MAX)
b	0.016 (TYP)	0.406 (TYP)
D	0.817 (MAX)	20.75 (MAX)
E	0.445 ± 0.005	11.303 ± 0.127
E1	0.555 ± 0.012	14.097 ± 0.305
e	0.050 (TYP)	1.270 (TYP)
L	0.0347 ± 0.008	0.881 ± 0.203
L1	0.055 ± 0.008	1.397 ± 0.203
S	0.026 (MAX)	0.660 (MAX)
y	0.004 (MAX)	0.101 (MAX)
θ	0^o ~10^o	0^o ~10^o

32-pin 8mm x 20mm TSOP-Ⅰ Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
D	0.724 ± 0.004	18.40 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ± 0.008	20.00 ± 0.20
L1	0.0315 ± 0.004	0.80 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0° 5°	0° 5°

32-pin 8mm x 13.4mm STSOP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 ± 0.001	0.200 ± 0.025
D	0.465 ± 0.004	11.800 ± 0.100
E	0.315 ± 0.004	8.000 ± 0.100
e	0.020 (TYP)	0.50 (TYP)
HD	0.528 ± 0.008	13.40 ± 0.20.
L1	0.0315 ± 0.004	0.80 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0^o 5^o	0^o 5^o

ORDERING INFORMATION

Commercial temperature :

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) (max) Ta = 50℃	PACKAGE
UT62L1024PC-35L	35	20	32 PIN PDIP
UT62L1024PC-35LL	35	10	32 PIN PDIP
UT62L1024PC-55L	55	20	32 PIN PDIP
UT62L1024PC-55LL	55	10	32 PIN PDIP
UT62L1024PC-70L	70	20	32 PIN PDIP
UT62L1024PC-70LL	70	10	32 PIN PDIP
UT62L1024SC-35L	35	20	32 PIN SOP
UT62L1024SC-35LL	35	10	32 PIN SOP
UT62L1024SC-55L	55	20	32 PIN SOP
UT62L1024SC-55LL	55	10	32 PIN SOP
UT62L1024SC-70L	70	20	32 PIN SOP
UT62L1024SC-70LL	70	10	32 PIN SOP
UT62L1024LC-35L	35	20	32 PIN TSOP-I
UT62L1024LC-35LL	35	10	32 PIN TSOP-I
UT62L1024LC-55L	55	20	32 PIN TSOP-I
UT62L1024LC-55LL	55	10	32 PIN TSOP-I
UT62L1024LC-70L	70	20	32 PIN TSOP-I
UT62L1024LC-70LL	70	10	32 PIN TSOP-I
UT62L1024LS-35L	35	20	32 PIN STSOP
UT62L1024LS-35LL	35	10	32 PIN STSOP
UT62L1024LS-55L	55	20	32 PIN STSOP
UT62L1024LS-55LL	55	10	32 PIN STSOP
UT62L1024LS-70L	70	20	32 PIN STSOP
UT62L1024LS-70LL	70	10	32 PIN STSOP

ORDERING INFORMATION

Extended temp :

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) (max) Ta = 50℃	PACKAGE
UT62L1024PC-35LE	35	20	32 PIN PDIP
UT62L1024PC-35LLE	35	10	32 PIN PDIP
UT62L1024PC-55LE	55	20	32 PIN PDIP
UT62L1024PC-55LLE	55	10	32 PIN PDIP
UT62L1024PC-70LE	70	20	32 PIN PDIP
UT62L1024PC-70LLE	70	10	32 PIN PDIP
UT62L1024SC-35LE	35	20	32 PIN SOP
UT62L1024SC-35LLE	35	10	32 PIN SOP
UT62L1024SC-55LE	55	20	32 PIN SOP
UT62L1024SC-55LLE	55	10	32 PIN SOP
UT62L1024SC-70LE	70	20	32 PIN SOP
UT62L1024SC-70LLE	70	10	32 PIN SOP
UT62L1024LC-35LE	35	20	32 PIN TSOP-I
UT62L1024LC-35LLE	35	10	32 PIN TSOP-I
UT62L1024LC-55LE	55	20	32 PIN TSOP-I
UT62L1024LC-55LLE	55	10	32 PIN TSOP-I
UT62L1024LC-70LE	70	20	32 PIN TSOP-I
UT62L1024LC-70LLE	70	10	32 PIN TSOP-I
UT62L1024LS-35LE	35	20	32 PIN STSOP
UT62L1024LS-35LLE	35	10	32 PIN STSOP
UT62L1024LS-55LE	55	20	32 PIN STSOP
UT62L1024LS-55LLE	55	10	32 PIN STSOP
UT62L1024LS-70LE	70	20	32 PIN STSOP
UT62L1024LS-70LLE	70	10	32 PIN STSOP

ORDERING INFORMATION (for lead free product)

Commercial temperature :

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) (max) Ta = 50℃	PACKAGE
UT62L1024PCL-35L	35	20	32 PIN PDIP
UT62L1024PCL-35LL	35	10	32 PIN PDIP
UT62L1024PCL-55L	55	20	32 PIN PDIP
UT62L1024PCL-55LL	55	10	32 PIN PDIP
UT62L1024PCL-70L	70	20	32 PIN PDIP
UT62L1024PCL-70LL	70	10	32 PIN PDIP
UT62L1024SCL-35L	35	20	32 PIN SOP
UT62L1024SCL-35LL	35	10	32 PIN SOP
UT62L1024SCL-55L	55	20	32 PIN SOP
UT62L1024SCL-55LL	55	10	32 PIN SOP
UT62L1024SCL-70L	70	20	32 PIN SOP
UT62L1024SCL-70LL	70	10	32 PIN SOP
UT62L1024LCL-35L	35	20	32 PIN TSOP-I
UT62L1024LCL-35LL	35	10	32 PIN TSOP-I
UT62L1024LCL-55L	55	20	32 PIN TSOP-I
UT62L1024LCL-55LL	55	10	32 PIN TSOP-I
UT62L1024LCL-70L	70	20	32 PIN TSOP-I
UT62L1024LCL-70LL	70	10	32 PIN TSOP-I
UT62L1024LSL-35L	35	20	32 PIN STSOP
UT62L1024LSL-35LL	35	10	32 PIN STSOP
UT62L1024LSL-55L	55	20	32 PIN STSOP
UT62L1024LSL-55LL	55	10	32 PIN STSOP
UT62L1024LSL-70L	70	20	32 PIN STSOP
UT62L1024LSL-70LL	70	10	32 PIN STSOP

ORDERING INFORMATION (for lead free product)

Extended temperature :

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) (max) Ta = 50℃	PACKAGE
UT62L1024PCL-35LE	35	20	32 PIN PDIP
UT62L1024PCL-35LLE	35	10	32 PIN PDIP
UT62L1024PCL-55LE	55	20	32 PIN PDIP
UT62L1024PCL-55LLE	55	10	32 PIN PDIP
UT62L1024PCL-70LE	70	20	32 PIN PDIP
UT62L1024PCL-70LLE	70	10	32 PIN PDIP
UT62L1024SCL-35LE	35	20	32 PIN SOP
UT62L1024SCL-35LLE	35	10	32 PIN SOP
UT62L1024SCL-55LE	55	20	32 PIN SOP
UT62L1024SCL-55LLE	55	10	32 PIN SOP
UT62L1024SCL-70LE	70	20	32 PIN SOP
UT62L1024SCL-70LLE	70	10	32 PIN SOP
UT62L1024LCL-35LE	35	20	32 PIN TSOP-I
UT62L1024LCL-35LLE	35	10	32 PIN TSOP-I
UT62L1024LCL-55LE	55	20	32 PIN TSOP-I
UT62L1024LCL-55LLE	55	10	32 PIN TSOP-I
UT62L1024LCL-70LE	70	20	32 PIN TSOP-I
UT62L1024LCL-70LLE	70	10	32 PIN TSOP-I
UT62L1024LSL-35LE	35	20	32 PIN STSOP
UT62L1024LSL-35LLE	35	10	32 PIN STSOP
UT62L1024LSL-55LE	55	20	32 PIN STSOP
UT62L1024LSL-55LLE	55	10	32 PIN STSOP
UT62L1024LSL-70LE	70	20	32 PIN STSOP
UT62L1024LSL-70LLE	70	10	32 PIN STSOP

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