IMPORTANT: Besides your calculator and the sheets you use for calculations you are only allowed to have an A4 sized "copy sheet" during this exam. Notes, problems and alike are not permitted. Please submit your "copy sheet" along with your solutions. You may get your "copy sheet" back after your solutions have been graded. **Do not forget to write down units!**

ELE222E INTRODUCTION TO ELECTRONICS (20748)
Midterm Exam #2 ✎ 21 April 2008 🕙 10.00-12.00
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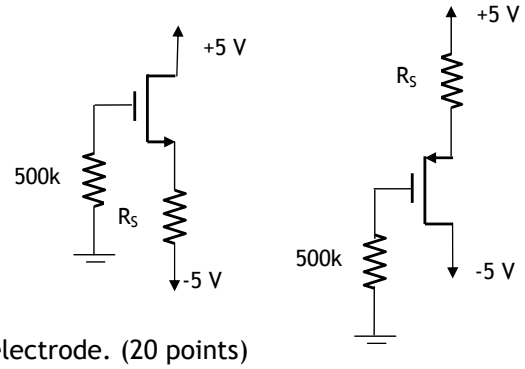
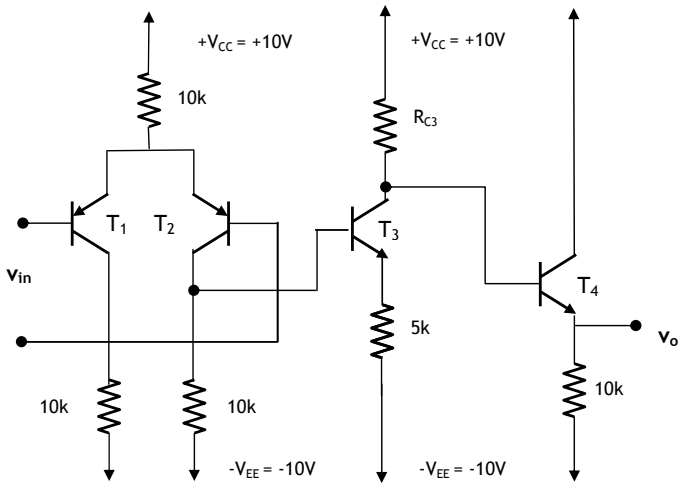
1. You will remember the MOS transistors shown right from the first midterm exam. They have the following parameters:
   $|V_{th}| = 2$ V, $\mu_n C_{ox}(W/L) = \mu_p C_{ox}(W/L) = 2$ mA/V^2, $V_A = 100$ V.



   a. Determine R_S in both cases, such that, when the MOS transistors are working in saturation $I_D = 1$ mA. (10 points)

   b. Determine the voltage gain in both cases, when v_i is applied to the gate and v_o is measured at the source electrode. (20 points)

2. Analyze the 3-stage amplifier circuit below. For all transistors $h_{FE} = h_{fe} = 100$, $V_T = 25$ mV, $|V_{BE}| = 0{,}6$ V, $h_{oe} = h_{re} = 0$.



   a. Find the collector currents of all 4 transistors and value of R_{C3}, such that, waveform distortion at the output V_o is minimum and symmetrical. (20 points)

   b. Design a BJT based current mirror that will provide the current provided by the 10k resistor connected to the common emitters of the differential stage. (10 points)

   c. Calculate the total voltage gain and output resistance of the 3-stage BJT amplifier. (40 points)

   If you could not find collector currents and R_{C3} in (a), you may assume $I_{C1} = I_{C2} = I_{C3} = I_{C4} = 1$ mA and $R_{C3} = 10$k.

GOOD LUCK!

SOLUTIONS:

1. MOS circuits:

   a. *Let's first take the circuit with NMOS:*

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[V_{GS} - V_{th}\right]^2 \Rightarrow V_{GS} = V_{th} \pm \sqrt{\frac{I_D}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}}} = 2V \pm \sqrt{\frac{1mA}{1mA/V^2}} = \begin{cases} 3V \\ 1V \end{cases}$$

   Since $V_{GS} \geq V_{th}$ for channel creation, $V_{GS} = \underline{\underline{3V}}$.

   As $V_G = 0V \Rightarrow V_S = V_G - V_{GS} = -3V$ thus $R_S = \frac{V_S - (-5V)}{1mA} = \underline{\underline{2k}}$

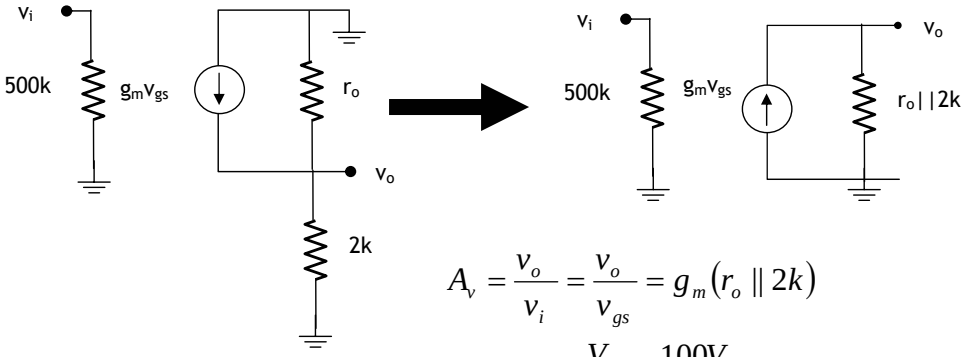
   Now the circuit with PMOS:

$$I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left[V_{GS} - V_{th}\right]^2 \Rightarrow V_{GS} = V_{th} \pm \sqrt{\frac{I_D}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}}} = -2V \pm \sqrt{\frac{1mA}{1mA/V^2}} = \begin{cases} -1V \\ -3V \end{cases}$$

   Since $V_{GS} \leq V_{th}$ for channel creation, $V_{GS} = \underline{\underline{-3V}}$.

   As $V_G = 0V \Rightarrow V_S = V_G - V_{GS} = +3V$ thus $R_S = \frac{+5V - 3V}{1mA} = \underline{\underline{2k}}$

   b. Now the calculation of gain: Whatever circuit we take, we obtain the same small signal circuit



$$A_v = \frac{v_o}{v_i} = \frac{v_o}{v_{gs}} = g_m\left(r_o \parallel 2k\right)$$

where $r_o = \frac{V_A}{I_D} = \frac{100V}{1mA} = \underline{\underline{100k}}$ and

$g_m = \sqrt{\left[2\mu_n C_{ox}\frac{W}{L}\right]I_D} = \underline{\underline{2mA/V}}$, thus $A_v = \frac{v_o}{v_i} = \frac{v_o}{v_{gs}} = g_m\left(r_o \parallel 2k\right) = \underline{\underline{3{,}92(V/V)}}$

2. DC Analysis: The first stage of the 3-stage amplifier is a differential stage. Since both transistors are ideal, their collector currents are the same

$$I_{C1} = I_{C2} = \frac{h_{FE}}{h_{FE}+1}\left[\frac{V_{CC} - V_{EB1}}{2R_E}\right] = \frac{100}{101}\cdot\frac{10V + V_{BE1}}{20k} = \frac{100}{101}\cdot\frac{10V - 0{,}6V}{20k} \cong \underline{\underline{0{,}47mA}}$$

Now, following the blue loop on the next page

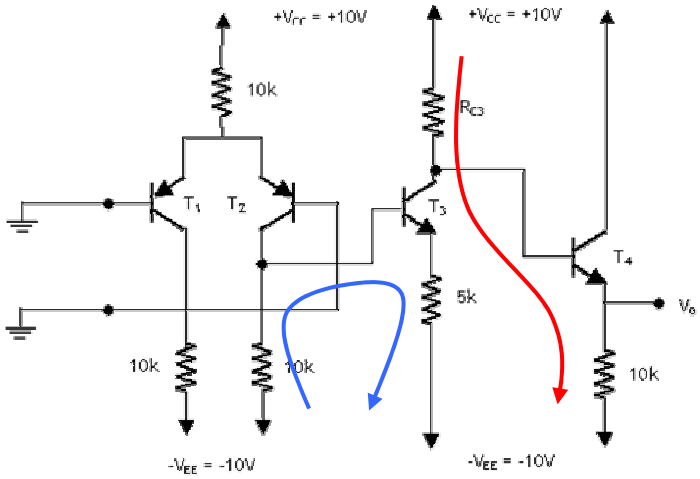
$$-(I_{C2} - I_{B3})10k + V_{BE3} + (h_{FE}+1)I_{B3}5k = 0$$

$$I_{C3} = h_{FE}\frac{10k * I_{C2} - V_{BE3}}{(h_{FE}+1)5k + 10k} = \underline{\underline{0{,}8mA}}$$

We are told that waveform distortion at the output V_o should be minimum and symmetrical. That means $V_0 = 0V$.

$$I_{E4} = \frac{0V - (-V_{EE})}{10k} \text{ or}$$

$$(h_{FE4}+1)I_{B4}10k = 10V$$
$$\Rightarrow I_{C4} = h_{FE4}I_{B4} = \underline{\underline{0{,}99mA}}$$



Also, $V_{B4} = +V_{CC} - R_{C3} * (I_{C3} + I_{B4}) = +10V - R_{C3} * (0{,}91mA + 9{,}9\mu A) = V_{BE4} = 0{,}6V$

Therefore, $R_{C3} = \frac{10V - 0{,}6V}{0{,}8mA + 9{,}9\mu A} = \underline{\underline{11k6}}$

<u>BJT based current mirror design:</u>

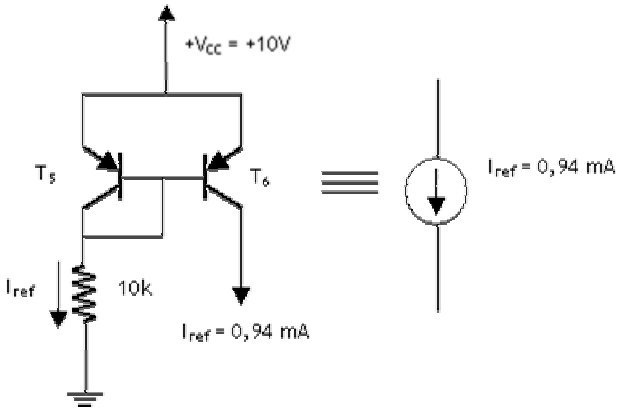
$I_{ref} = 2I_{C1} = 2I_{C2} = 0{,}94$ mA.

On the right is my design. NOTE that the collector of T_6 is connected to the common emitters of the differential stage. At DC $V_{E1} = V_{E2} = 0{,}6$ V, that means, $V_{C6} = 0{,}6$ V. This voltage should keep T_6 in active mode! Does it?

$V_{B6} = 9{,}4$ V. For BC junction to be reverse biased,

$V_{C6} \le V_{B6} - 0{,}6$ V that is $V_{C6} \le 8{,}8$ V.

$V_{C6} = 0{,}6$ V < 8,8 V and THUS this condition is satisfied.



<u>AC Analysis:</u> Let'a first calculate the AC resistances

$$r_{e1} = r_{e2} = \frac{V_T}{I_{C1}} = \frac{25mV}{0{,}47mA} = \underline{\underline{53{,}2\Omega}}; r_{e3} = \frac{V_T}{I_{C3}} = \frac{25mV}{0{,}8mA} = \underline{\underline{31{,}25\Omega}}; r_{e4} = \frac{V_T}{I_{C4}} = \frac{25mV}{0{,}99mA} = \underline{\underline{25{,}25\Omega}}$$

$$A_v = \frac{v_o}{v_{in}} = \frac{v_o}{v_{b4}} \cdot \frac{v_{b4}}{v_{b3}} \cdot \frac{v_{b3}}{v_{in}} = +\frac{R_{e4}}{r_{e4} + R_{e4}} \cdot \left[-\frac{R_{C3} \parallel r_{i4}}{r_{e3} + R_{e3}} \right] \cdot \left[+\frac{R_{C2} \parallel r_{i3}}{2r_{e1}} \right]$$

$$r_{i3} = h_{fe}(r_{e3} + R_{e3}) = 100(31{,}25 + 5k) = \underline{\underline{503k}}$$
$$r_{i4} = h_{fe}(r_{e4} + R_{e4}) = 100(25{,}25 + 10k) = \underline{\underline{1M}}$$

$$\Rightarrow A_v = \frac{10k}{25{,}25 + 10k} \cdot \left[-\frac{11k6 \parallel 1M}{31{,}25 + 5k} \right] \cdot \left[\frac{10k \parallel 503k}{2 * 53{,}2} \right] = 0{,}997 * (-2{,}279) * 92{,}167 \cong \underline{\underline{-209{,}5}}$$

$$r_o = r_{o4} = R_{E4} \parallel \left[r_{e4} + \frac{R_S}{h_{fe}} \right] = R_{E4} \parallel \left[r_{e4} + \frac{r_{o3}}{h_{fe}} \right] = \underline{\underline{139\Omega}} \text{ where } r_{o3} = R_{C3} = \underline{\underline{11k6}}$$