



Microprocessor Systems

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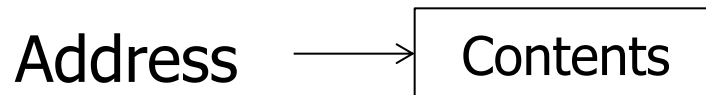
Syllabus

1. Introduction, Number Systems
2. Computer Overview - Memory
3. Memory Design
4. Quiz 1, CPU overview, Instruction format
5. Addressing methods
6. Instruction types
7. Instruction types - cntd
8. Midterm Exam 1
9. Parallel communication interface
10. Serial communication interface
11. Quiz 2, Subroutines, Interrupts, Stack, Coding techniques
12. Coding examples and applications
13. Midterm Exam 2
14. Development of Microprocessor Based Designs



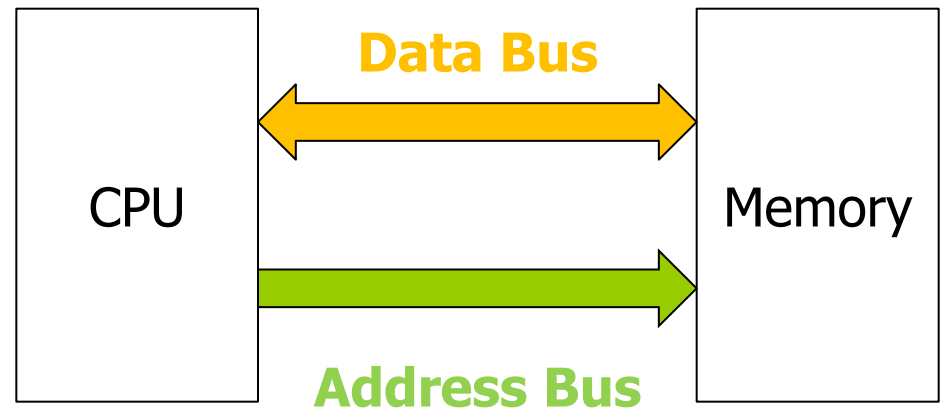
Memory Addressing

- Memory consists of a sequence of directly addressable "locations".
- A memory location is referred to as an information unit.
- An information unit has two components:
 - address
 - contents



Memory Addressing

- Each location in memory has an address that must be supplied before its contents can be accessed.
- The CPU communicates with memory by first identifying the location's address and then passing this address on the address bus.
- The data are transferred between memory and the CPU along the data bus.
- The number of bits that can be transferred on the data bus at once is called the data bus width of the processor.





Dimensions of Memory

- Memory is usually measured by two numbers: its length and its width (Length X Width).
 - The length is the total number of locations.
 - The width is the number of bits in each location.
- The length (total number of locations) is a function of the number of address lines.
 - # of memory locations = $2^{(\text{\# of address lines})}$**
 - A memory chip with 10 address lines would have
 $2^{10} = 1024$ locations (1K)
 - A memory chip with 4K locations would need
 $\log_2 4096 = 12$ address lines

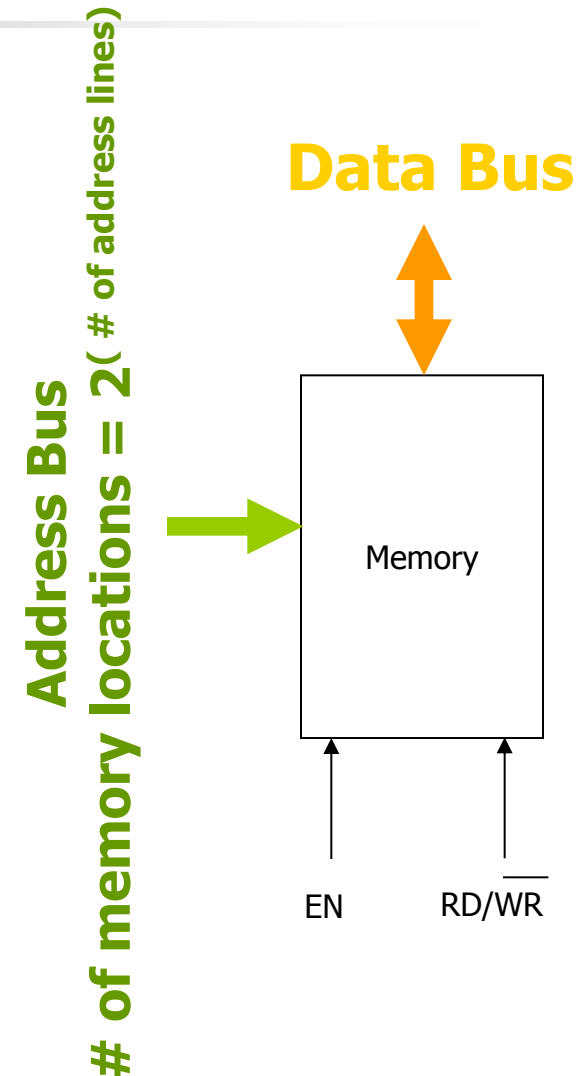


Educational CPU and Memory

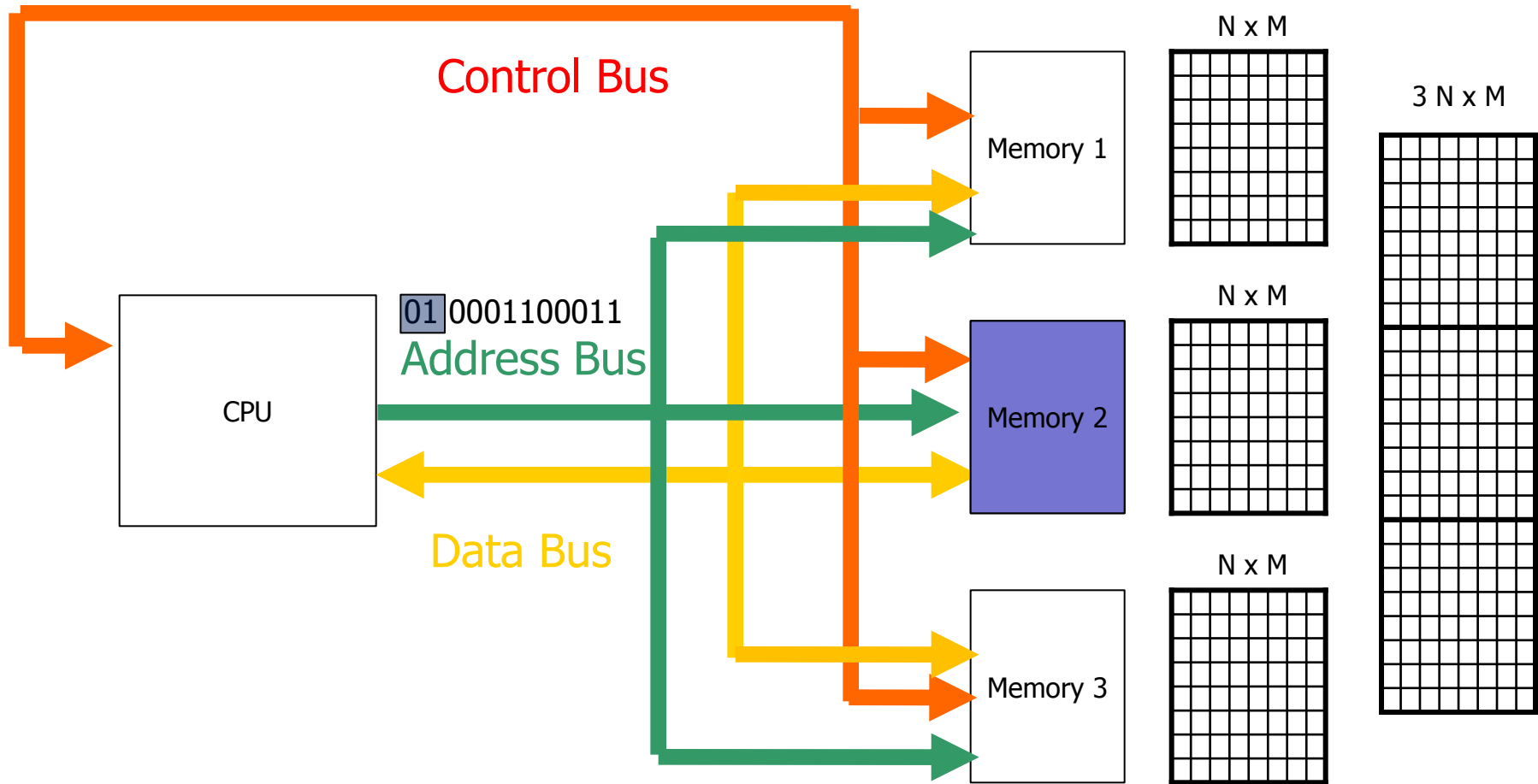
- Educational CPU has 16 address lines. That means it can address
$$2^{16} = 64\text{K memory locations.}$$
- Then it will need 1 memory chip with 64 K locations, or 2 chips with 32 K in each, or 4 with 16 K each or 16 of the 4 K chips, etc.
- How would we use these address lines to control the multiple chips?

Chip Select

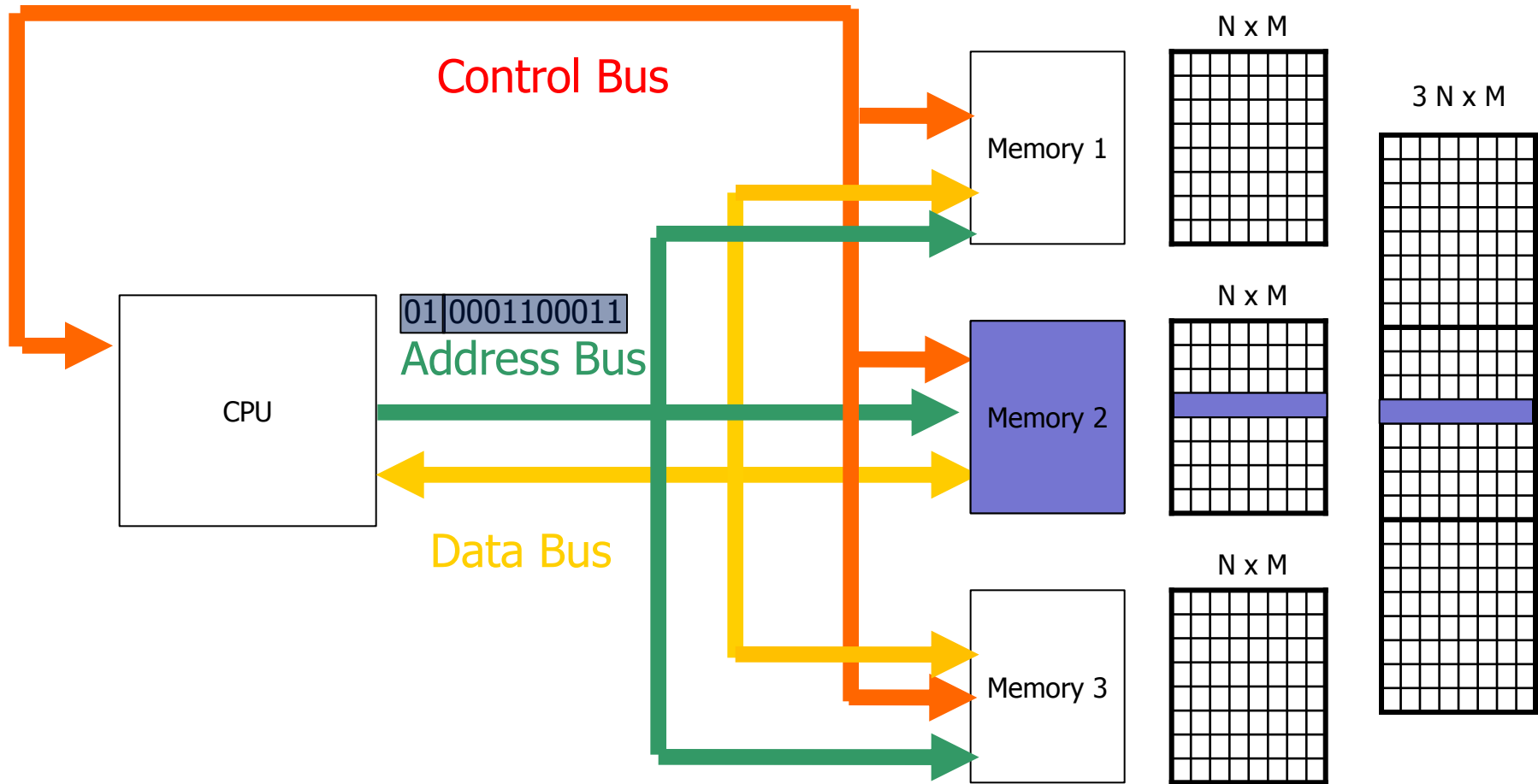
- Usually, each memory chip has a Chip Select (CS) input. The chip will only work if an active signal is applied on that input.
- To allow the use of multiple chips in the make up of memory, we need to use a number of the address lines for the purpose of "chip selection".
- These address lines are decoded to generate the 2^n necessary CS inputs for the memory chips to be used.



Memory Access

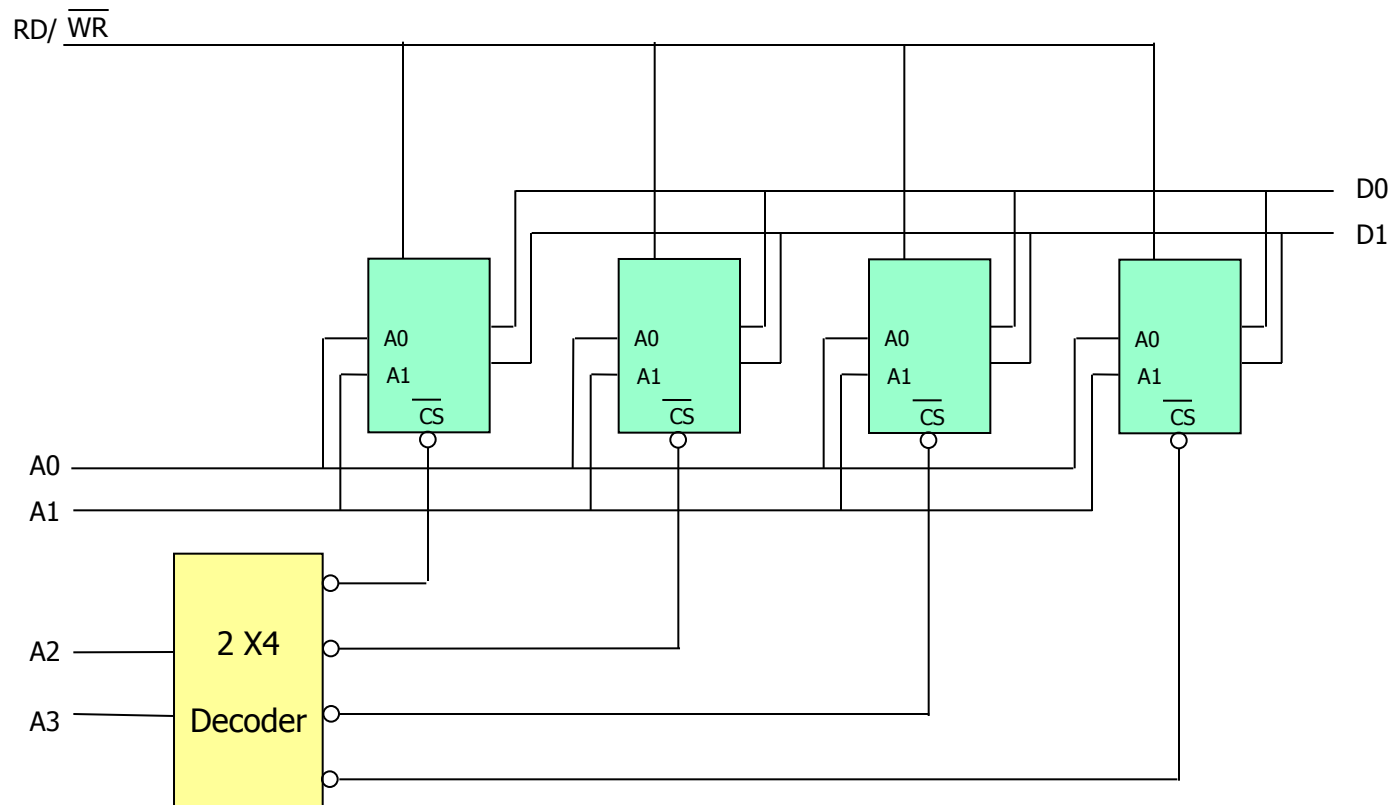


Memory Access



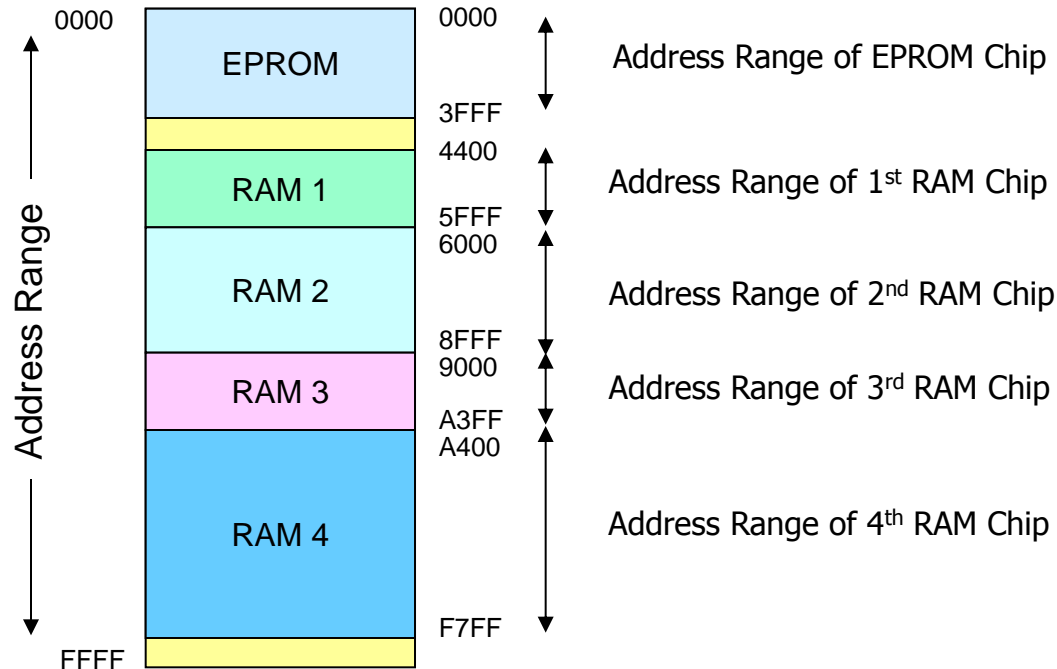
Chip Selection Example

- a memory system made up of 4 of the 4 X 2 memory chips



Memory Map

- Designates the address space for each memory chip



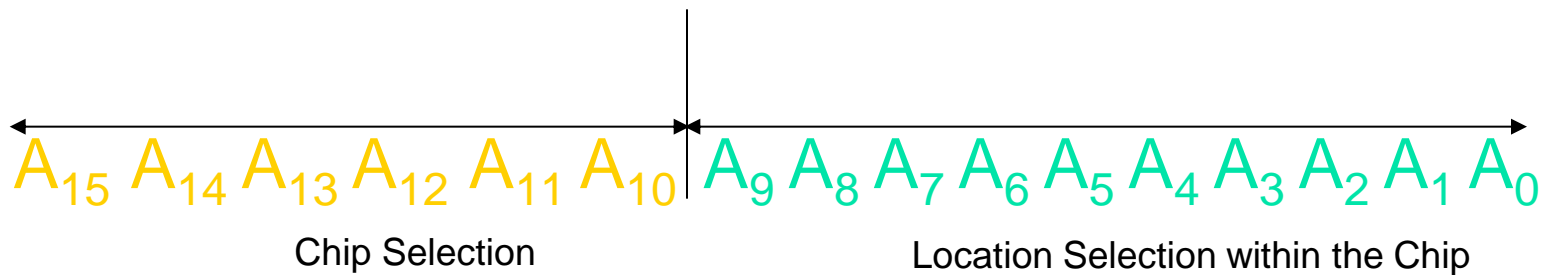


Address Range of a Memory Chip

- The address range of a particular chip is the list of all addresses that are mapped to the chip.
- An 8-bit CPU with 16 address bits can address a total of 64K memory locations.
 - If we use memory chips with 1K locations each, then we will need 64 such chips.
 - The 1K memory chip needs 10 address lines to uniquely identify the 1K locations. ($\log_2 1024 = 10$)
 - That leaves 6 address lines which is the exact number needed for selecting between the 64 different chips ($\log_2 64 = 6$).

Address Range of a Memory Chip

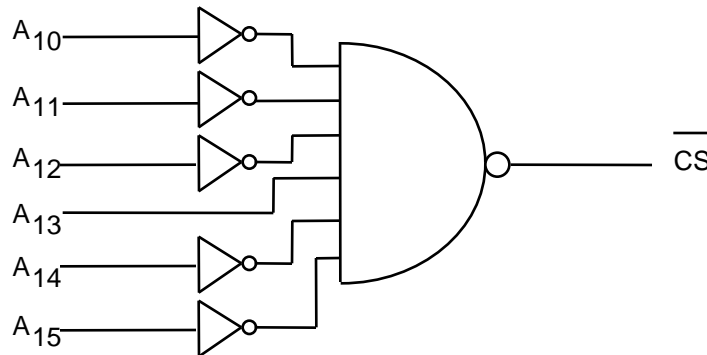
- 16 bit address lines can be separated into two pieces



- Depending on the combination on the address lines A_{15} - A_{10} , the address range of the specified chip is determined.

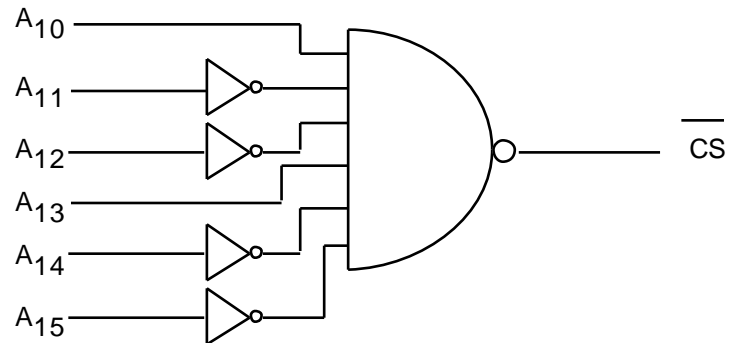
Chip Select Example

- A chip that uses the combination $[A_{15}-A_{10}] = 001000$ would have addresses that range from \$2000 to \$23FF.
 - the 10 address lines on the chip gives a range of xxxx xx00 0000 0000 to xxxx xx11 1111 1111 or \$x000 to \$x3FF for each of the chips.
 - The memory chip in this example would require the following NAND circuit on its chip select input:



Chip Select Example

- If we change the above combination to the following:

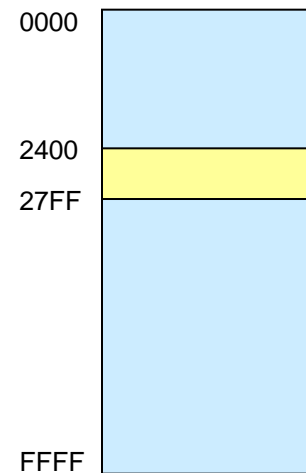
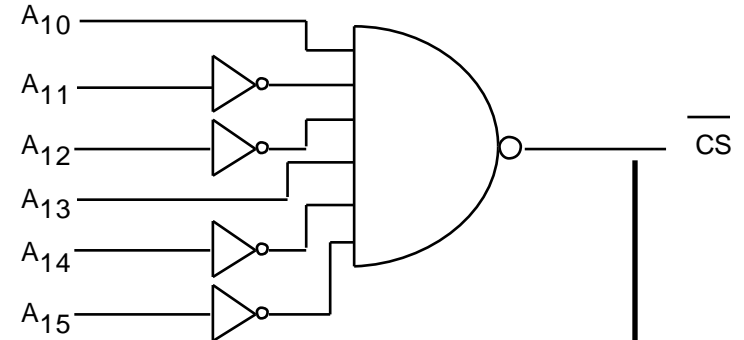
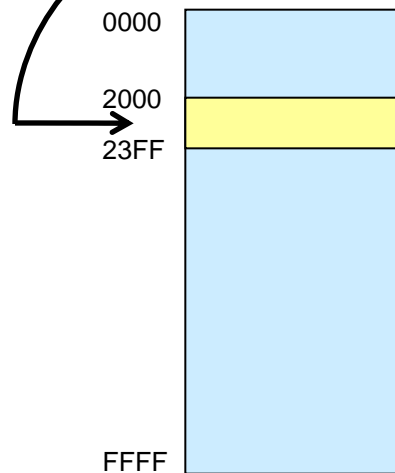
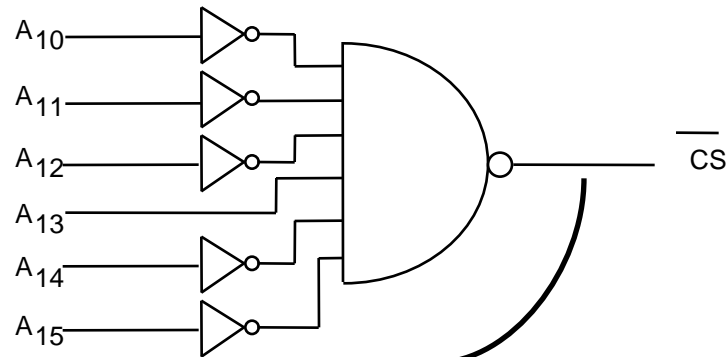


- Now the chip would have addresses ranging from: 2400 to 27FF.

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	=>\$2400
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	=>\$27FF

- Changing the combination of the address bits connected to the chip select changes the address range for the memory chip.

Chip Select Example





Memory Organization

- Example: For a CPU with 8-bit data bus and 16-bit address bus, build the memory that spans between \$0000 and \$1FFF with 2Kx8 memory chips.
- What is the required memory space?
- How many 2K chips are needed?

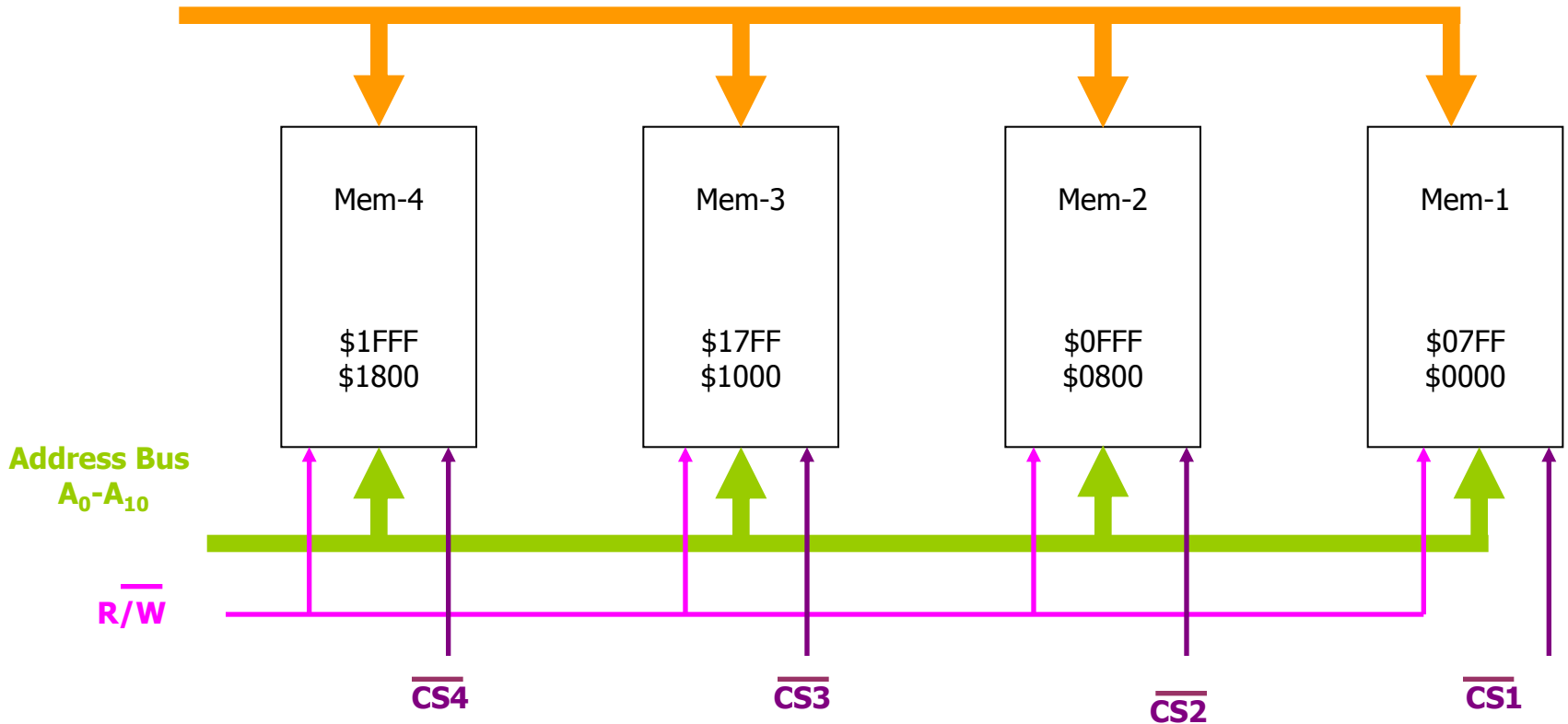


Memory Organization

A ₁₅ A ₁₄ A ₁₃ A ₁₂		A ₁₁ A ₁₀ A ₉ A ₈		A ₇ A ₆ A ₅ A ₄		A ₃ A ₂ A ₁ A ₀		
0000	0	0000	0	0000	0000	0000		\$0000
0000	0	0111	0	1111	1111	1111		\$07FF
0000	0	1000	1	0000	0000	0000		\$0800
0000	0	1111	1	1111	1111	1111		\$0FFF
0001	0	0000	0	0000	0000	0000		\$1000
0001	0	0111	0	1111	1111	1111		\$17FF
0001	1	1000	1	0000	0000	0000		\$1800
0001	1	1111	1	1111	1111	1111		\$1FFF

- CS is determined using A12 and A11

Data Bus D₀-D₇





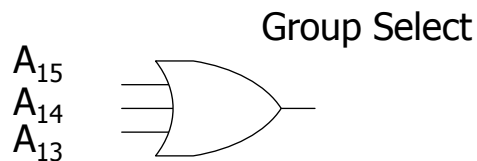
Memory Organization

- Chip select is done with address bits that are not used within the memory chip.

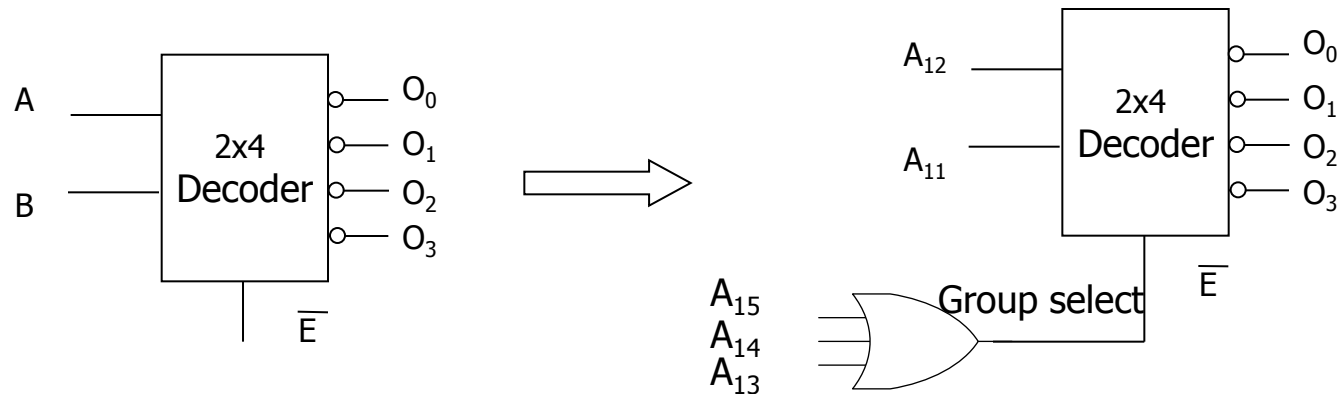
	A_{15}	A_{14}	A_{13}		A_{12}	A_{11}	$A_{10} \dots$
Memory 1	0	0	0		0	0	Used to address locations within a memory chip
Memory 2	0	0	0		0	1	
Memory 3	0	0	0		1	0	
Memory 4	0	0	0		1	1	

Memory Organization

- A_{15} , A_{14} , A_{13} remain at low at all times. They can be used to form another Chip Select (Group Select)



- A_{12} and A_{11} can be used to select memory chips with 2x4 decoder



Memory Organization

Data Bus D₀-D₇

Address Bus
A₀-A₁₀

R/ \overline{W}

$\overline{CS4}$

$\overline{CS3}$

$\overline{CS2}$

$\overline{CS1}$

A₁₂

A₁₁

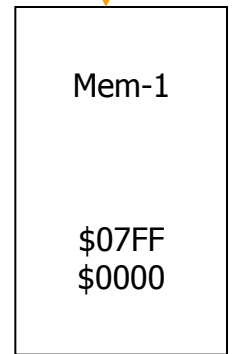
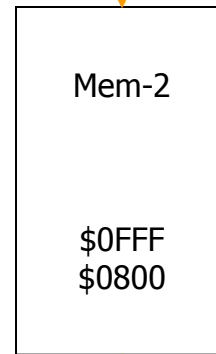
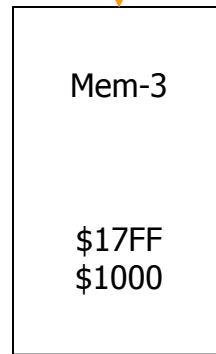
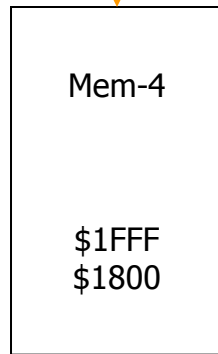
2x4
Decoder

Grp. Select

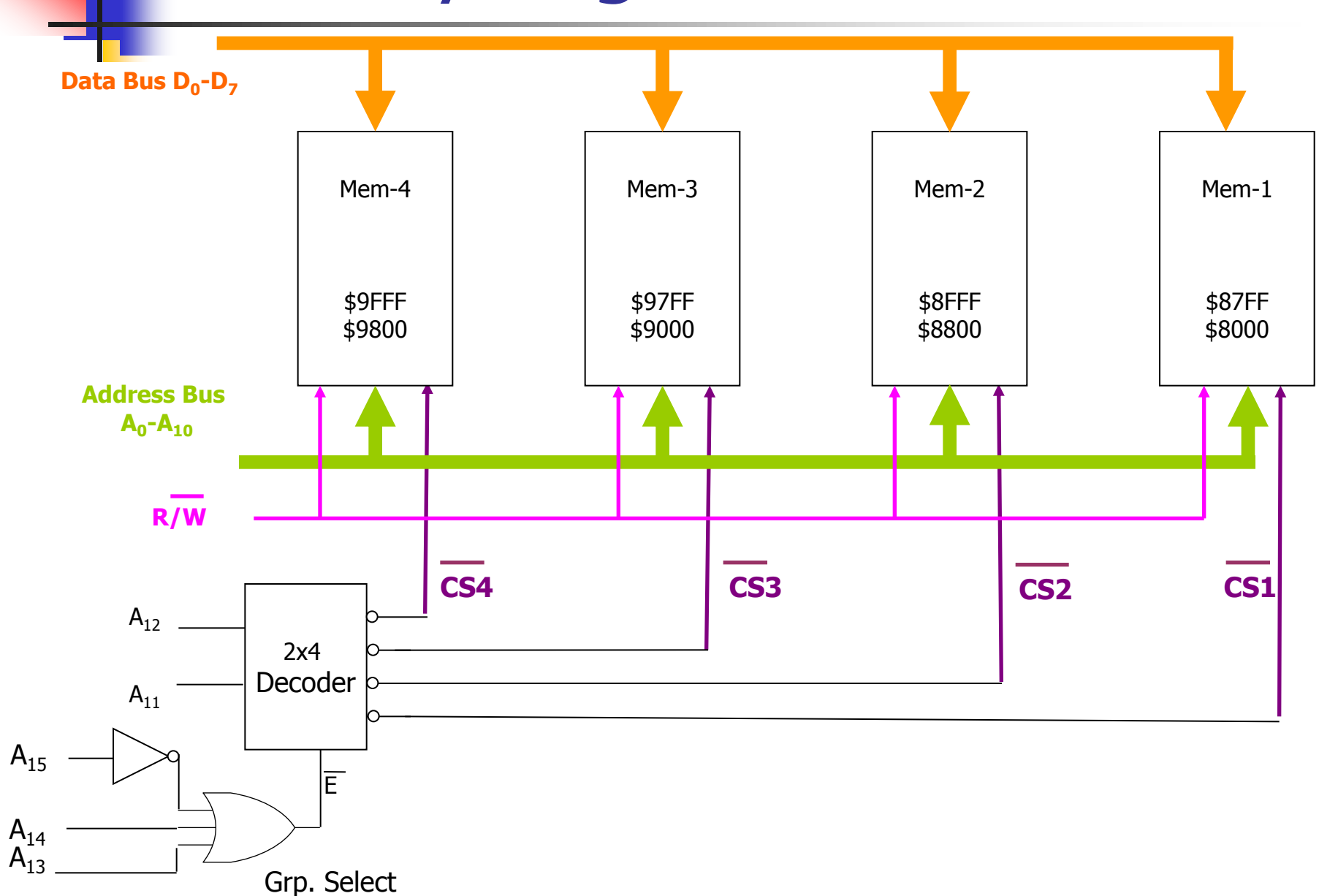
\overline{E}

A₁₅
A₁₄
A₁₃

Question: If A₁₅ is inverted, what is the memory base address ?



Memory Organization



Memory Organization

Example: Organize 8Kx1 memory chips to obtain 8Kx8 memory

