Istanbul Technical University
Faculty of Computer and Informatics
Computer Engineering Department
Graduation Project Plan

A PROCESSOR DESIGN ON FPGA

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AIM OF THE PROJECT

Using advantage of field programmable gate arrays (FPGA) dynamic digital design capability, every processor architecture and organization can be simulated on it. This gives a chance of compare different architecture design advantages and disadvantages. Also new architecture designs can be tested on FPGA's before final production. In this project a RISC processor will be created with a newly design architecture and instruction set. Actual processor architectures will be examined and mixture of their design will inspire the new architecture at the design stage of the project. Learning design and working mechanism of processors are main aim of this project.

SCOPE OF THE PROJECT

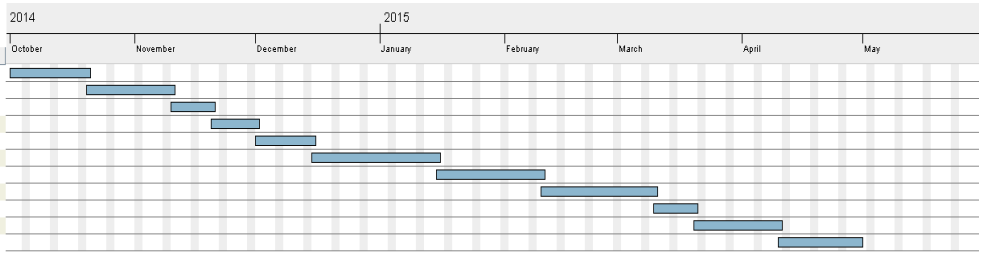
FPGA's can be used in many areas. Processor design is one of them. In this project it is only used for design environment. So FPGA design is a tool for the project, not the aim of the project. Dynamic structure of FPGA's lead to change processors modules according to needs. For example; a second serial communication module can easily be imported in FPGA processors but it is not possible for integrated microprocessors, whole microprocessor must change for this one requirement. Also FPGA's make easy to design process of processors. After the successful design processor design can be converted to ASIC (Application Specific Integrated Circuit) as one integrated circuit. So these FPGA designed processor can be used in all areas which normally microprocessor are being used.

ESTIMATIONS ABOUT THE PROJECT

In this project, some development, analysis and simulation tools for FPGA design will be used. The necessary tools will be chosen according to physical FPGA board/equipment. Physical equipment will be provided by adviser and necessary software tools will be supplied by manufacturer of FPGA under student license. The study will take approximately 1 academic year (2 academic term). Necessary researches will be done in first half of the first academic term and development and documentation will be done in the rest of the time.

SCHEDULE

Name	Begin date	End date
Organization design	10/1/14	10/20/14
Architecture design	10/20/14	11/10/14
Instruction set design	11/10/14	11/20/14
Understanding how to use FPGA kit	11/20/14	12/1/14
Understanding how to program in Verilog	12/1/14	12/15/14
Writing ALU	12/15/14	1/15/15
Writing registers and BUS	1/15/15	2/10/15
Writing pipelining mechanism	2/10/15	3/10/15
Implementing RAM ROM	3/10/15	3/20/15
Executing code in RAM	3/20/15	4/10/15
Writing assembler for new instruction set	4/10/15	4/30/15



RESOURCES

Some well-known computer architecture and computer organization books can be used as source in research phase of the project. However in development phase of the project, there is no need to specific book or resource. Any tutorials about FPGA's on the internet or books can be used as source.