LAB 1

BOOLEAN ALGEBRA

1. INTRODUCTION

The aim of this experiment is examining the axioms and theorems of Boolean algebra in an experimental environment.

2. PRELIMINARY

- Revise the axioms and theorems of Boolean algebra.
- Employing the axioms of Boolean algebra, prove the equalities given below.
  - A+A.B=A
  - (A+B)*(A+B')=A
- Find the duals of the equalities given above and prove them using the axioms of Boolean algebra.
- Find the complementary of the function F=X+Y.Z using de Morgan theorem and draw the logic circuits of F and F'.
- Reduce the logic function given below using the axioms and theorems of Boolean algebra.

  F(A,B,C)=A'.B'.D'+B.C'.D'+AB'D'+BC'D+BCD'

3. EQUIPMENTS AND COMPONENTS

- C.A.D.E.T.
- 74xx04 NOT gate
- 74xx08 AND gate
- 74xx32 OR gate

“xx” may be S, LS, C, HC, HCT. These letters specify the inner structure of the logic gates. S and LS are the elements of the TTL family whereas C, HC and HCT are the elements of the CMOS family. Although their inner structures are different, their usages and functionalities are the same.

4. EXPERIMENTS

4.1. EXPERIMENT #1

Make the circuits of the logic theorems given in "Preliminary" section which are A+A.B=A and (A+B)*(A+B') = A. Using the truth tables and logic circuits of the theorems, show the truth of them. Inputs are provided by switches and outputs are monitored by LEDs.

4.2. EXPERIMENT #2

Make the circuit of the dual of the theorem A+A.B=A. Using the truth table and the logic circuit of the theorem, show the truth of it.

4.3. EXPERIMENT #3

Make the circuit of the function F' which is obtained using de Morgan theorem in the "Preliminary" section which is F=X+Y.Z. Check the truth of your circuit using the truth table of F.

4.4. EXPERIMENT #4

Make the circuit of the reduced logical function in the 5th part in "TODOs before experiment" section. Check the truth of your circuit using the truth table of the reduced function.

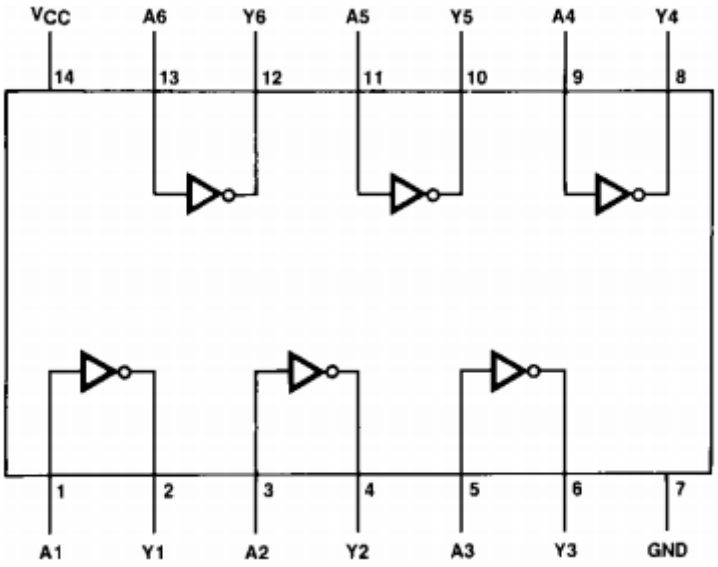
5. REQUIRED STAFF FOR THE REPORT

- Write your report with respect to "Report Guideline".
- Draw all logical circuits you installed properly and give the obtained results.
- Explain the mistake made in the operation below.

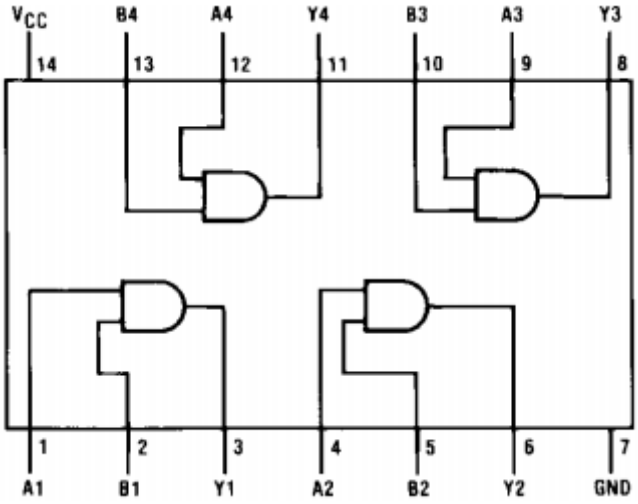
Using de Morgan theorem, complementary of the function F(A,B,C,D) = A+B.C+D is being obtained. For F'(A,B,C,D)=A'.B'+C'.D', when the input value ABCD = 0001 is provided, both F and F' produce output 1.

6. APPENDIX

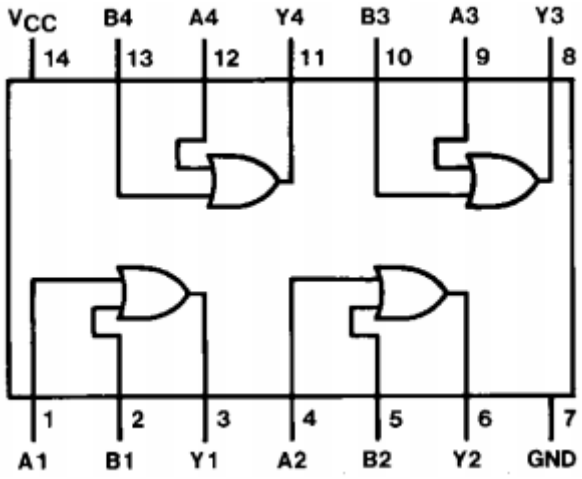
Connection Diagrams of 74xx04 74xx08 and 74xx32 logic gates.



74xx04



74xx08



74xx32