

**IMPORTANT:** Besides your calculator (**cell phones are not allowed, any attempt to use cell phones will be strictly penalized**) and the sheets you use for calculations you are only allowed to have an A4 sized "copy sheet" during this exam. Notes, problems and alike are not permitted. Please submit your "copy sheet" along with your solutions. You may get your "copy sheet" back after your solutions have been graded. *Do not forget to write down units and convert units carefully!*

---

## ELE222E INTRODUCTION TO ELECTRONICS

Final Exam  25 May 2011  9.00-11.00

Zümray DOKUR ÖLMEZ, Metin YAZGI, Bülent YAĞCI, Rıza Can TARCAN,  
Türker KÜYEL, İnci ÇİLESİZ

---

Student number and name: \_\_\_\_\_

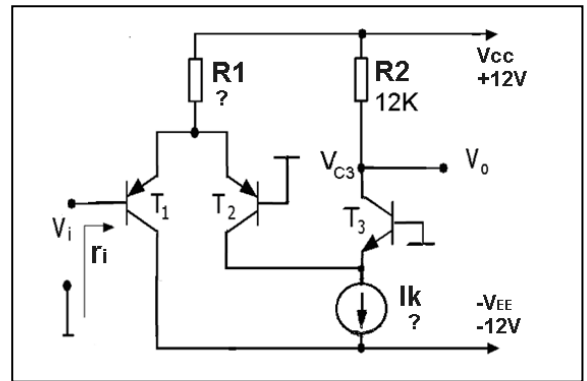
### Mandatory Problem (30 points):

The two BJTs  $T_1$  and  $T_2$  shown in the figure are identical. Their parameters are  $h_{FE} = \beta_F = 250$ ,  $|V_{BE}| = 0,6$  V,  $V_{CEsat} = 0,2$  V,  $V_T = 25$  mV and  $V_A = \infty$ .

a) The design requires  $V_{C3} = 6$  V for  $V_i = 0$  V, and  $v_o/v_i = 100$ . Find the resistor value for  $R_1$  and the current  $I_k$ . (15 points)

Note:  $R_1$  is much larger than  $r_{e1}$  and  $r_{e2}$ .

b) Taking into account the saturation and cutoff conditions for  $T_3$ , find the variance of output voltage ( $V_o$ ) and the corresponding variance of the input voltage ( $V_i$ ) (15 points)



GOOD LUCK!

**Mandatory Problem (40 points):**

- (A) For the transistors shown below  $h_{fe} = h_{FE} = 200$ ,  $V_{BE} = 0,6V$ ,  $V_{CESAT} = 0,2V$  and  $V_T = 25mV$ . You can assume  $h_{re} \approx 0$  and  $h_{oe} \approx 0$ . All capacitors are ideal.
- a) Find  $R_3$ ,  $R_4$  and  $R_5$  for  $I_C = 1mA$ ,  $V_{CE} = 4V$  and  $r_i = 10k\Omega$  (10 points)
- b) Calculate  $v_o/v_i$ . (10 points).

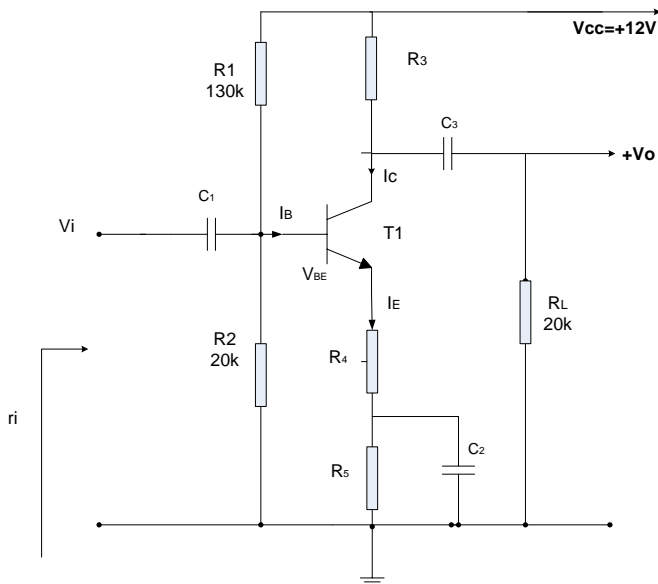


Figure-1

(a)  $R_3 = \underline{\hspace{2cm}}$   $R_4 = \underline{\hspace{2cm}}$   $R_5 = \underline{\hspace{2cm}}$

(b)  $v_o/v_i = \underline{\hspace{2cm}}$

- (B) For the MOS shown below  $V_T = 1V$ ,  $V_A = 100V$ ,  $0,5\mu_n C_{ox}(W/L) = 2mA/V^2$ , and all capacitors are ideal.
- a) Calculate biasing currents and voltages. (10 points)
- b) Calculate input resistance  $r_i$  and  $v_o/v_i$ . (10 points)

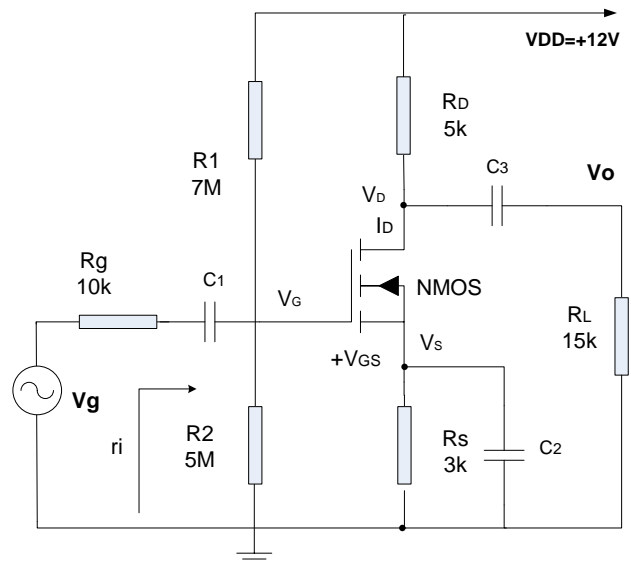


Figure-2

(a)  $V_{G_s} = \underline{\hspace{2cm}}$  V  $V_{D_s} = \underline{\hspace{2cm}}$  V  
 $V_{S_s} = \underline{\hspace{2cm}}$  V  $V_{G_{S_s}} = \underline{\hspace{2cm}}$  V

$I_{D_s} = \underline{\hspace{2cm}}$  mA

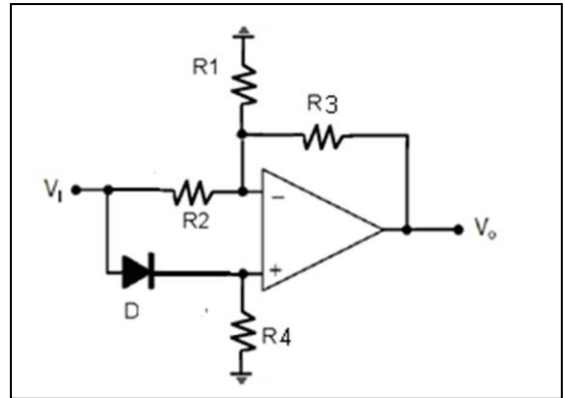
(b)  $r_{i_s} = \underline{\hspace{2cm}}$   $v_o/v_i = \underline{\hspace{2cm}}$

**GOOD LUCK!**

**Elective Problem (30 points):** The OPAMP and the diode shown in the figure have ideal properties. The OPAMP saturation voltages at the output are  $V_o^+ = 5\text{ V}$  and  $V_o^- = -5\text{ V}$ .

a) Find the gain of the circuit for both  $V_i > 0$  and  $V_i < 0$ . (15 points)

b) Find  $R_2$  and  $R_3$  for  $V_o = 2|V_i|$  ( $R_1 = R_4 = 10\text{ k}$ ). For which values of  $V_i$  is  $V_o = 2|V_i|$  valid? (15 points)



**GOOD LUCK!**

The circuit diagram shows a two-stage CMOS amplifier. The first stage is a common-source amplifier with NMOS M1 and PMOS M2. The input signal  $V_i$  is applied to the gate of M1. The gate of M2 is biased at  $V_{gn}$ . The output of the first stage is  $V_{fn}$ . The second stage is another common-source amplifier with NMOS M3 and PMOS M4. The input signal  $V_{fp}$  is applied to the gate of M3. The gate of M4 is biased at  $V_{gp}$ . The output of the second stage is  $V_o$ . The circuit includes various voltage sources (V1-V7), resistors (R1, R2), and capacitors (C1, C2).

and channel length modulation parameter  $\lambda = \frac{1}{V_A}$  is  $5 \text{ V}^{-1}$ .

- Your answers must be accurate within 1-2%.

Page 4