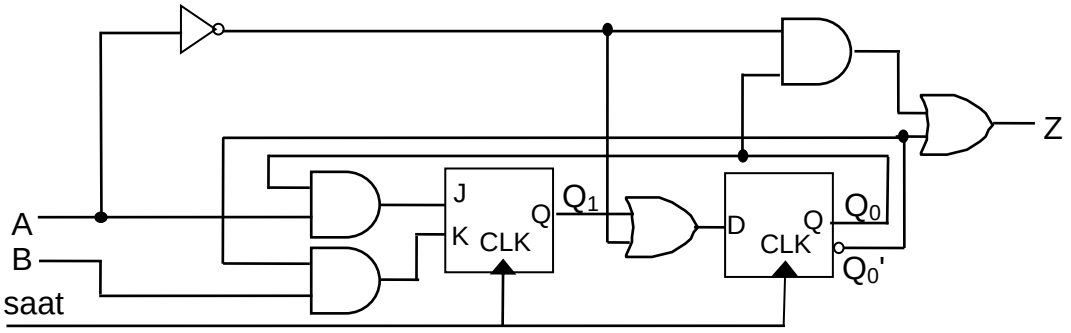
Fall 2012-2013

Problem Session 3

1)

a) Analyze the given clocked synchronous circuit. Construct the State/Output table. Draw the state diagram of the circuit.

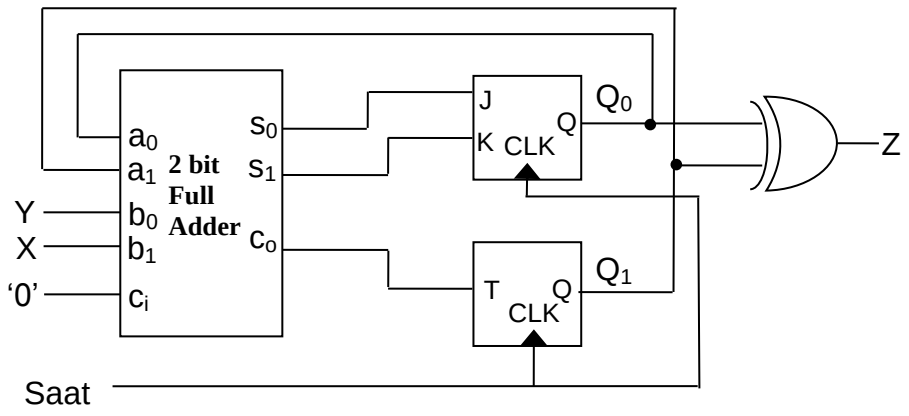
b) Under the assumption that the circuit is in state Q1=1, Q0=0, draw the timing diagram that shows the values of Q1,Q0,Z, when the input sequence is AB=01,01,11,00.



2)

a) Analyze the given clocked synchronous circuit. Construct the State/Output table. Draw the state diagram of the circuit.

b) Under the assumption that the circuit is in state Q1=1, Q0=0, draw the timing diagram that shows the values of Q1,Q0,Z, when the input sequence is XY=11,11,10,00.



3)

a) Analyze the given circuit by different input values. Can this circuit be used as a memory unit? Explain?

b) What is propagation delay for edge triggered T flip flop? Draw the timing diagram and explain.