BLG311E – FORMAL LANGUAGES AND AUTOMATA

2013 SPRING

RECITEMENT 1

1) 8 bit registers of A, B and C contain 3 unequal, positive integers. Design an ASM to find the median of these values. With a start signal (S) the machine will start working by loading initial values of A, B and C. After the execution, 8 bit register D will contain the median. A combinational subtraction circuit will be used for comparison along with a carry flag (E).

a) Sketch the ASM diagram of the machine, defined above.
b) Design and sketch the controller unit assigning each state to a D flip-flop.
c) Design and sketch data unit. State the input signals of the units you have used.

2) An array of 7 unsigned integers is sorted in ascending order. An ASM that calculates the order of a given integer will be designed. Binary search will be used as the search method. A combinational subtraction circuit will be used for comparison along with carry (C) and zero (Z) flags .

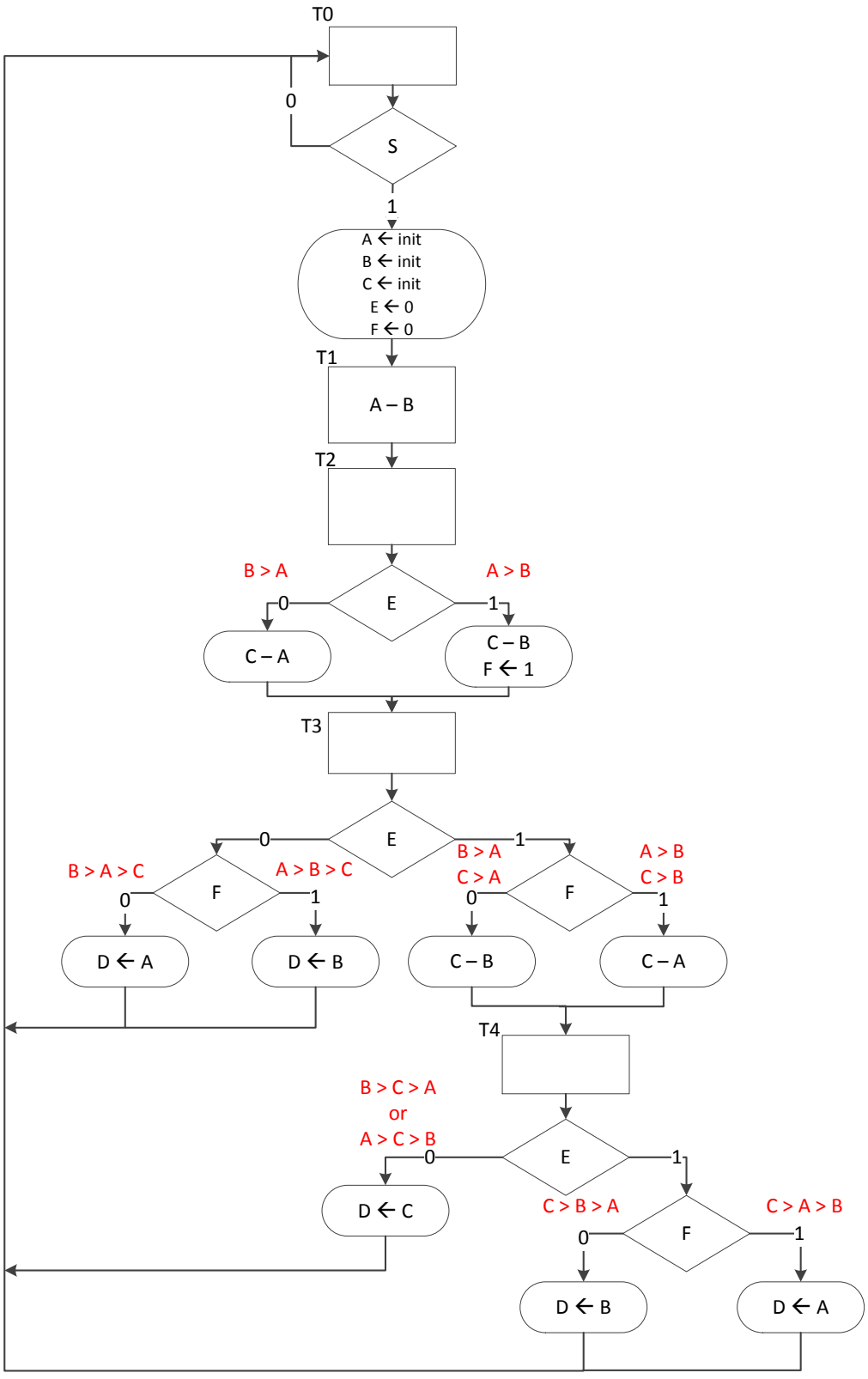
When the control signal S is set to "1" the integers will be loaded to the R_1-R_7 registers. R_8 register will contain the integer to look for (assume that the integer to look for is in the array). When the machine completes execution, ORDER register will contain the order of the integer.
For example,

Array: 4 5 8 12 32 35 40
The integer to look for: 32
The value in ORDER register after ASM is executed: 5

a) Design the circuit for the Z flag.
b) Sketch the ASM diagram of the machine.
c) Design and sketch data unit. State the input signals of the units you have used.
d) Design and sketch the controller unit assigning each state to a D flip-flop.

Solution 1

a) ASM diagram



b) Control unit:

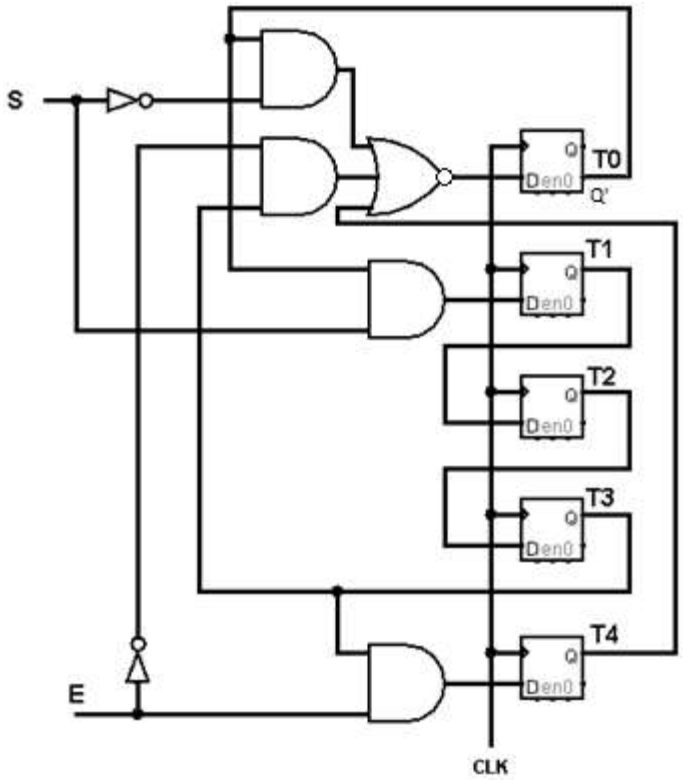
$T_0 = s'T_0 + E'T_3 + T_4$

$T_1 = sT_0$

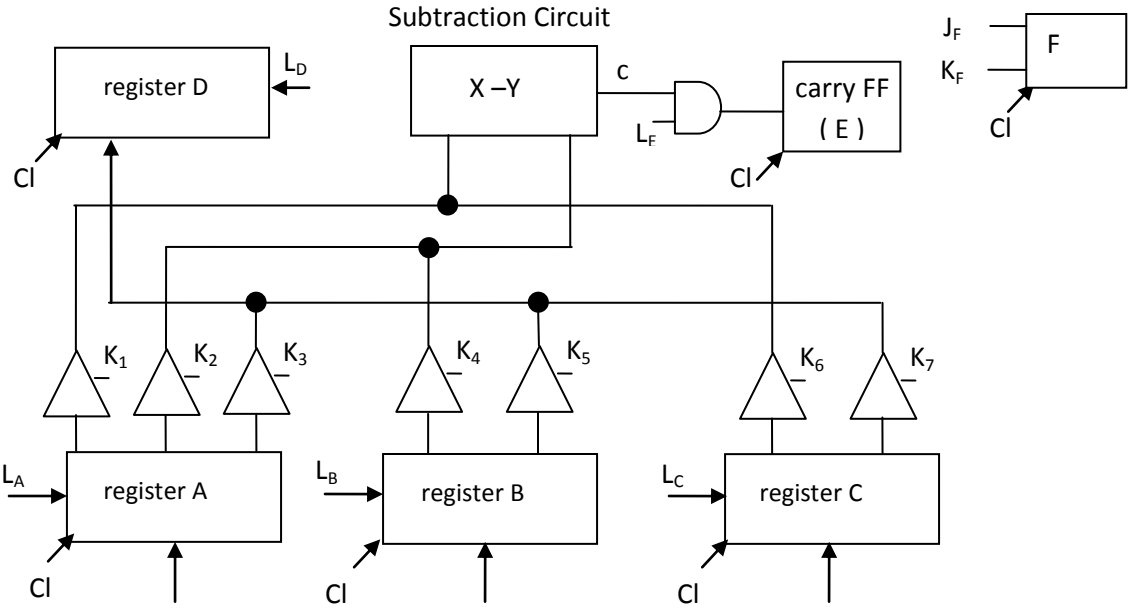
$T_2 = T_1$

$T_3 = T_2$

$T_4 = ET_3$



c) Data unit:



$L_A = L_B = L_C = sT_0$

$L_D = T_3E' + T_4$

$L_E = sT_0 + T_1 + T_2 + T_3E$

$J_F = ET_2$

$K_F = sT_0$

$K_1 = T_1$

$K_2 = T_2E' + T_3EF$

$K_3 = T_3E'F' + T_4EF$

$K_4 = T_1 + T_2E + T_3EF'$

$K_5 = T_3E'F + T_4EF'$

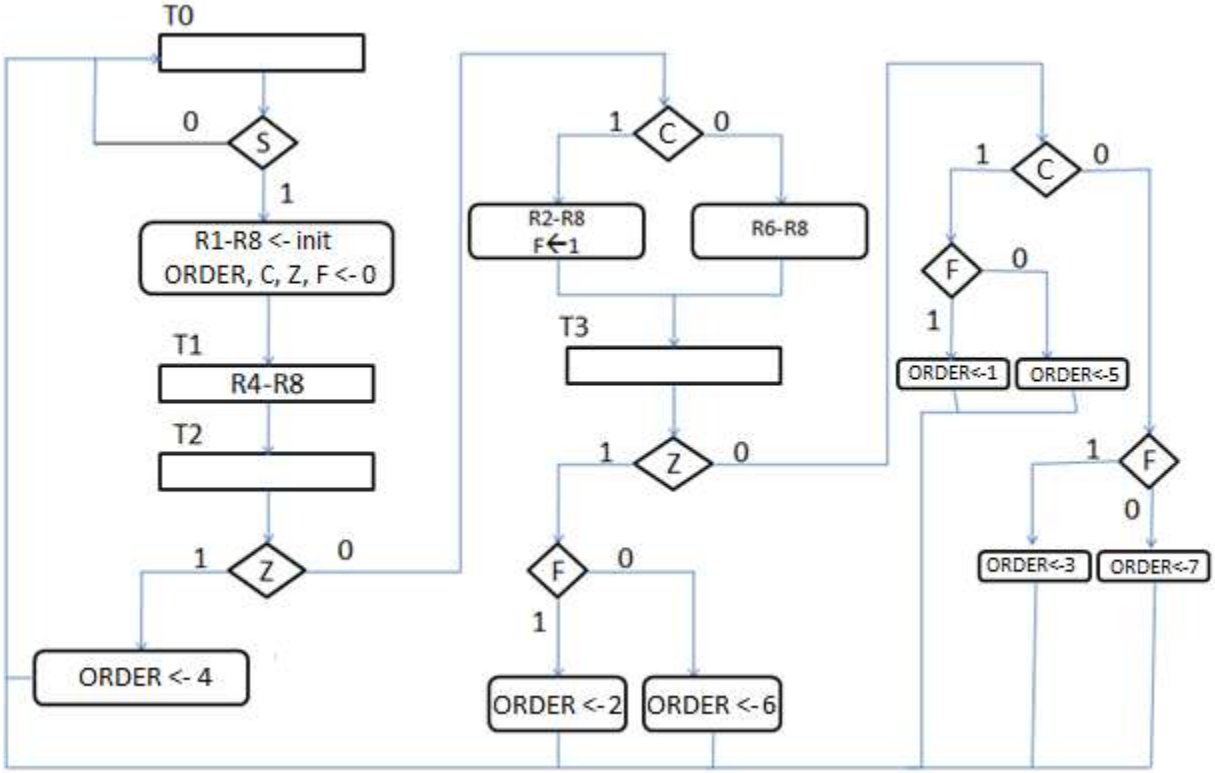
$K_6 = T_2 + T_3E$

$K_7 = T_4E'$

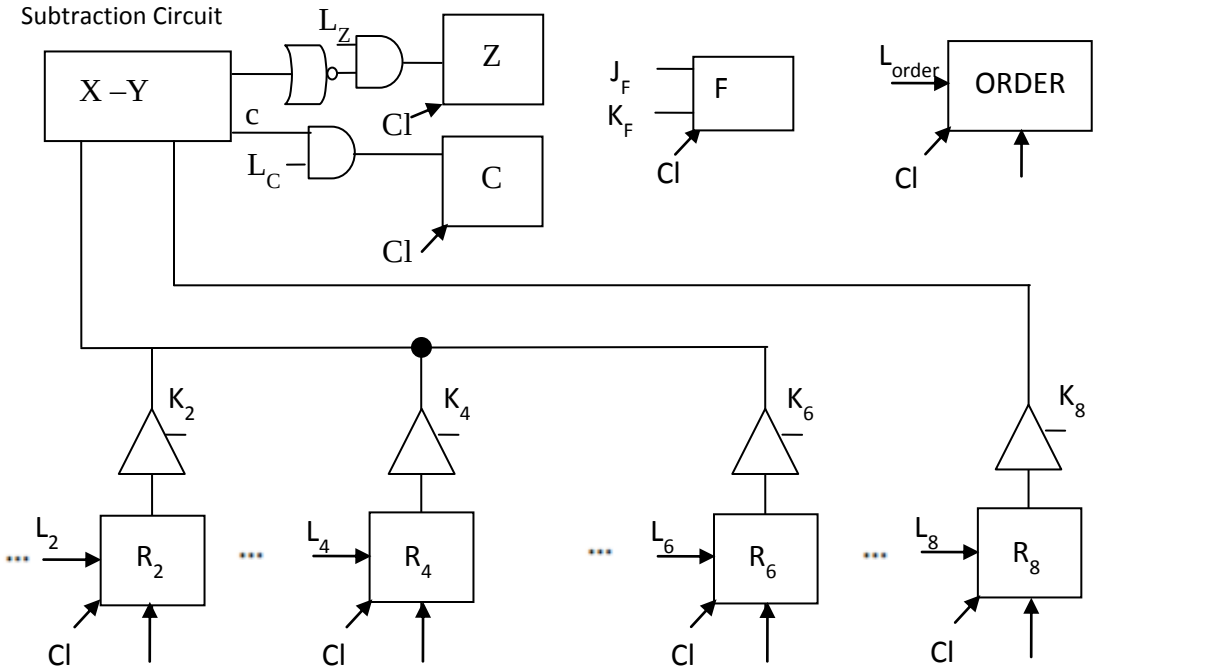
Solution 2

a) All bits of the subtraction circuit can be inputted to a NOR gate to create the Z bit. This bit will only be set if the two inputs to the subtraction are equal.

b) ASM Diagram:



c) Data unit:



Input signals of the elements and the data processor of the ASM is given below.

$L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = L_8 = sT_0$

$L_{order} = T_2Z + T_3$

$L_C = L_Z = sT_0 + T_1 + T_2Z'$

$J_F = T_2Z'C$

$K_F = sT_0$

$K_2 = T_2Z'C$

$K_4 = T_1$

$K_6 = T_2Z'C'$

$K_8 = T_1 + T_2Z'$

d) Control unit:

$T_0 = s'T_0 + ZT_2 + T_3$

$T_1 = sT_0$

$T_2 = T_1$

$T_3 = Z'T_2$