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FORMAL LANGUAGES AND AUTOMATA

HW-1

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1. You are asked to design a division circuit using ASM, that conforms with the following properties

   a) Circuit starts operation by enabling ('1') a control bit S,
   b) In the beginning of the operation two unsigned 8 bit numbers should be loaded to registers A and B; if B=0 an overflow flag should be set and the circuit should jump to the last step skipping division operation.
   c) The circuit should perform A/B operation and store the result in C register and the remainder in D register,
   d) After storing the results, the circuit should wait for the control bit S to be disabled ('0') and go back to starting state.

   You should assume that an adder/subtractor and necessary number of registers are present. Registers have synchronous reset, increment and parallel loading capabilities.

   In this context,
   a) Draw ASM flowchart
   b) Design control unit
   c) Design data processor. Also provide the boolean expressions that control the digital components in the system.

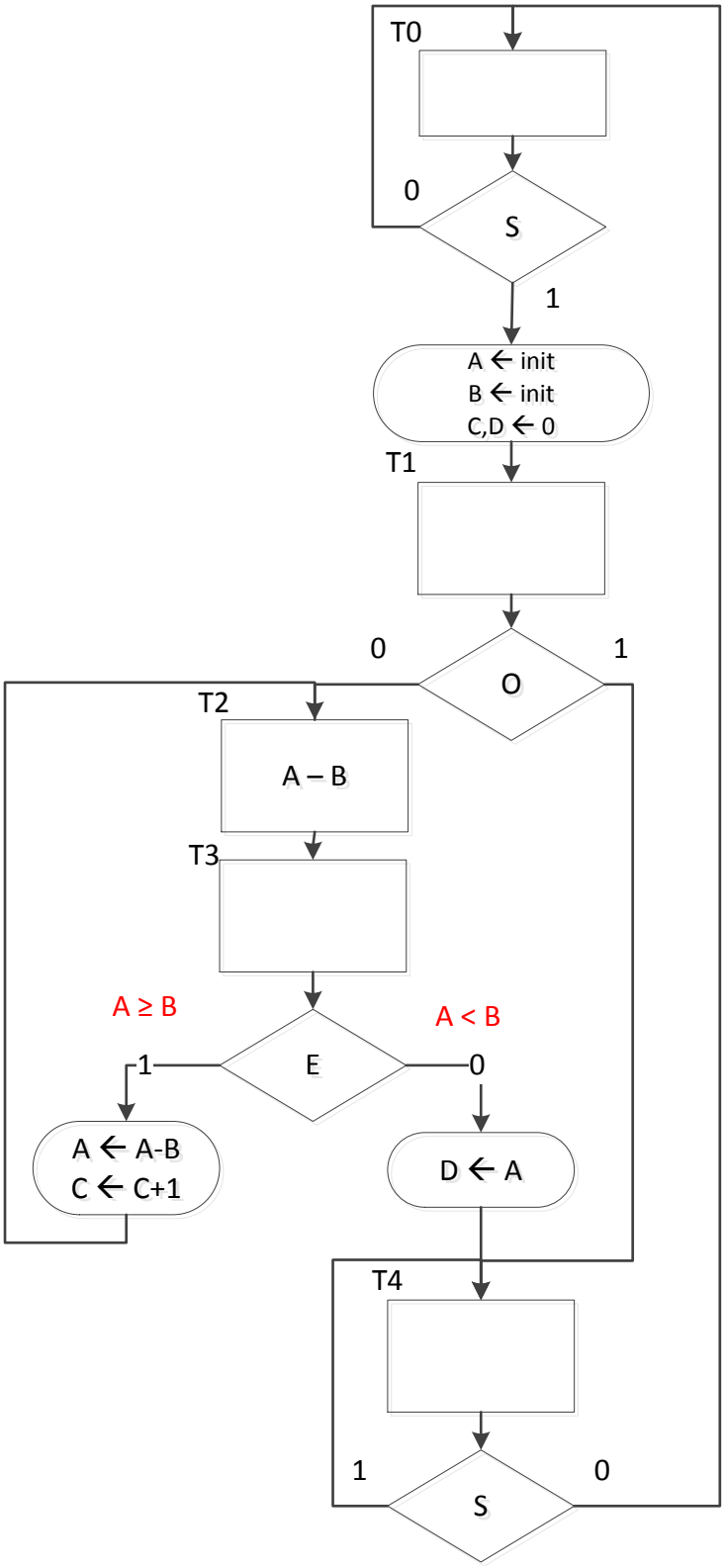
2. Reduce the states of the incompletely specified Mealy machine below and draw the state transition table of the reduced machine in Moore model.

	I_1	I_2	I_3	I_4	I_5
A	D-0	D-0	-	-	B-0
B	E-0	D-0	B-1	-	C-0
C	-	D-0	-	A-0	A-0
D	C-1	C-0	E-0	B-0	-
E	D-1	C-0	-	-	E-1

Submission Deadline: 7 March 2013

SOLUTIONS

1) a)



b)

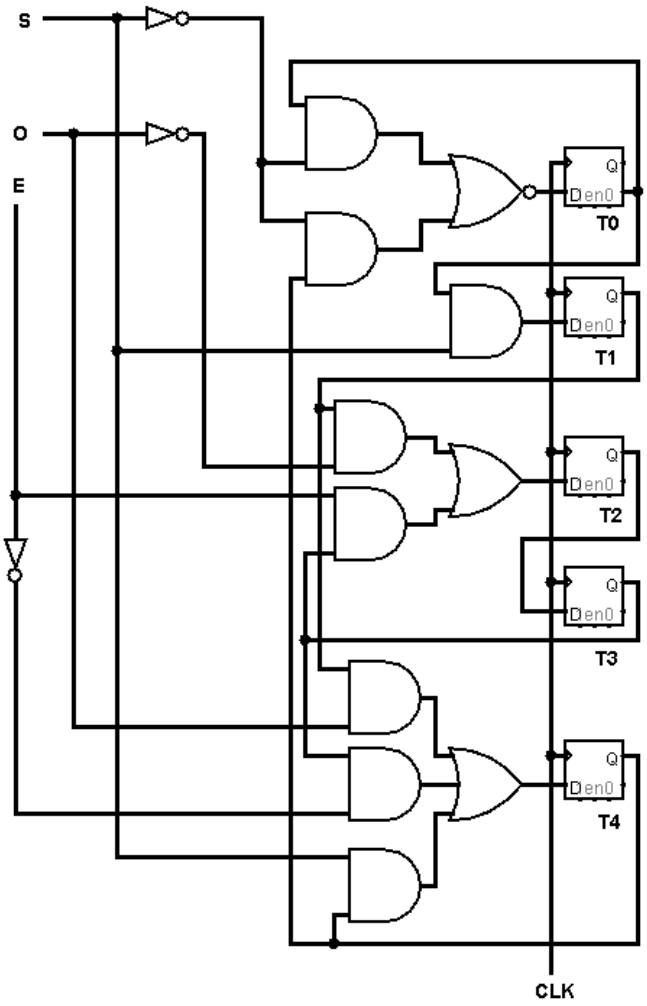
$T_0 = S'T_0 + S'T_4$

$T_1 = ST_0$

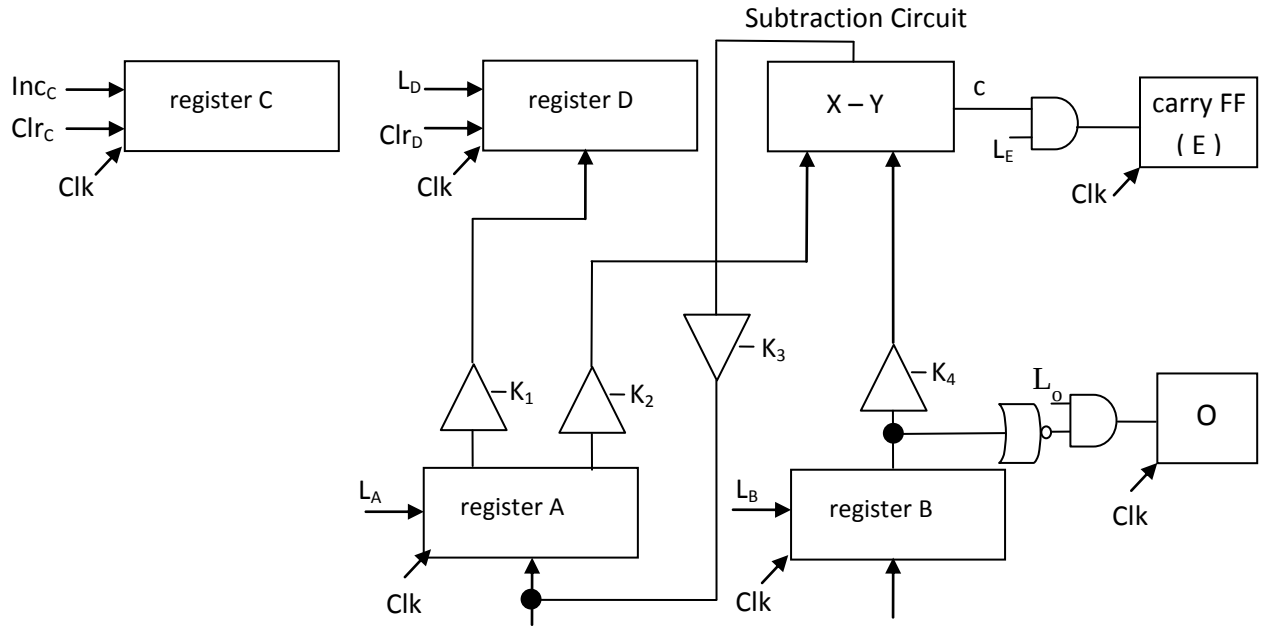
$T_2 = O'T_1 + ET_3$

$T_3 = T_2$

$T_4 = OT_1 + E'T_3 + ST_4$



c)



$L_A = sT_0 + ET_3$
$L_B = Clr_C = Clr_D = L_O = sT_0$
$Inc_C = ET_3$
$L_D = E'T_3$
$L_E = T_2$

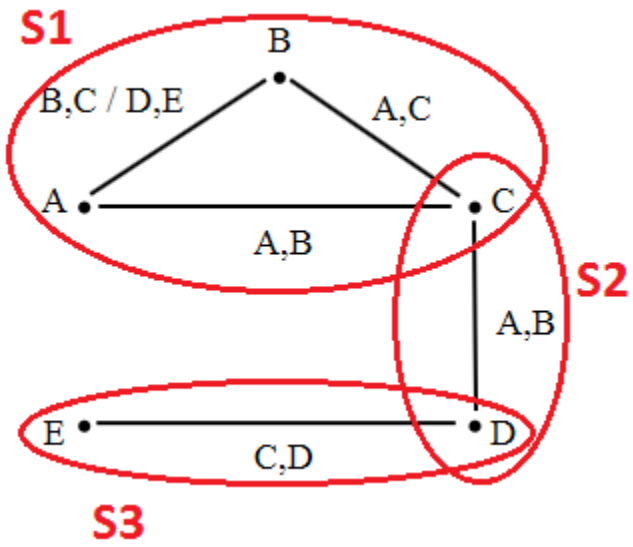
$K_1 = E'T_3$
$K_2 = K_4 = T_2$
$K_3 = ET_3$

2)

State dependency table:

	A	B	C	D
B	B-C D-E			
C	A-B	A-C		
D	-	-	A-B	
E	-	-	-	C-D

Relation graph (Complete cover):



Mealy model reduced machine:

	I_1	I_2	I_3	I_4	I_5
S1	S3-0	S2,S3-0	S1-1	S1-0	S1-0
S2	S1,S2-1	S2-0	S3-0	S1-0	S1-0
S3	S2-1	S1,S2-0	S3-0	S1-0	S3-1

Moore model reduced machine:

		I_1	I_2	I_3	I_4	I_5	O
U	**S1-0**	Y	W,Y	V	U	U	0
V	**S1-1**	Y	W,Y	V	U	U	1
W	**S2-0**	V,X	W	Y	U	U	0
X	**S2-1**	V,X	W	Y	U	U	1
Y	**S3-0**	X	U,W	Y	U	Z	0
Z	**S3-1**	X	U,W	Y	U	Z	1