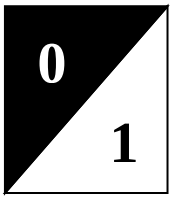
ISTANBUL TECHNICAL UNIVERSITY



COMPUTER ENGINEERING

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO: 6

EXPERIMENT NAME: USING BUS IN DIGITAL CIRCUITS

EXPERIMENT DATE : 05.04.2013

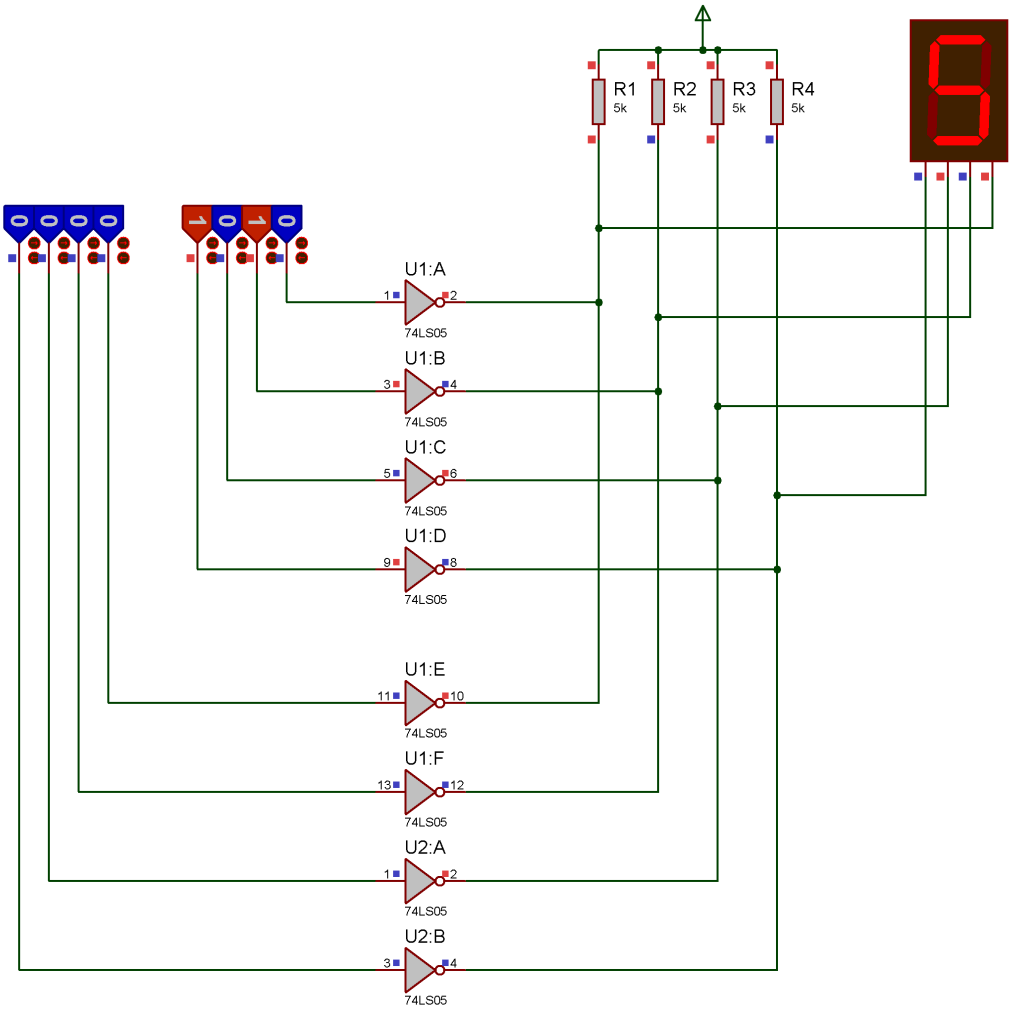
GROUP NO: 6

STUDENTS WHO DID THE EXPERIMENT:

Student no	Name	Surname
040100113	MUSTAFA	UÇAR
040100117	TUĞRUL	YATAĞAN
040100124	EMRE	GÖKREM

ASSISTANT NAME WHO ASSISTED THE EXPERIMENT: NEZİHA AKALIN

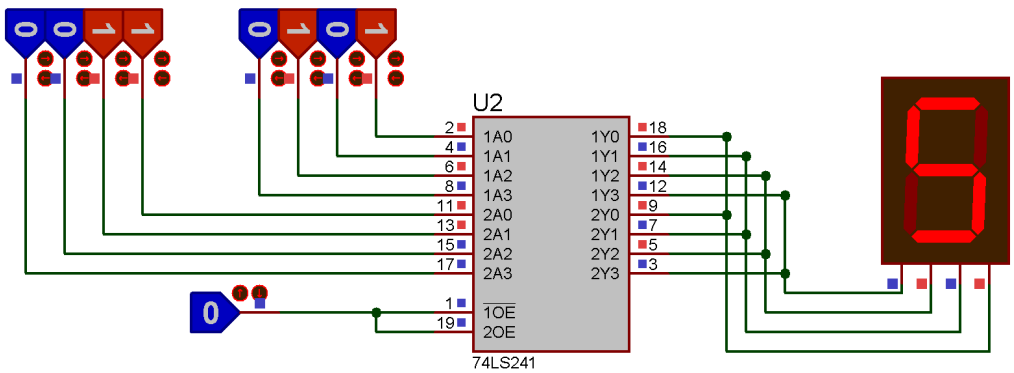
1-)



Rc(alt)= 4,2/ (8-0,4*N) → N=1 → Rc(alt) = 0.552 ohm
Rc(üst)=3/(0,1*K+0,02*N) → K = 2 → Rc(üst) = 13.63 ohm

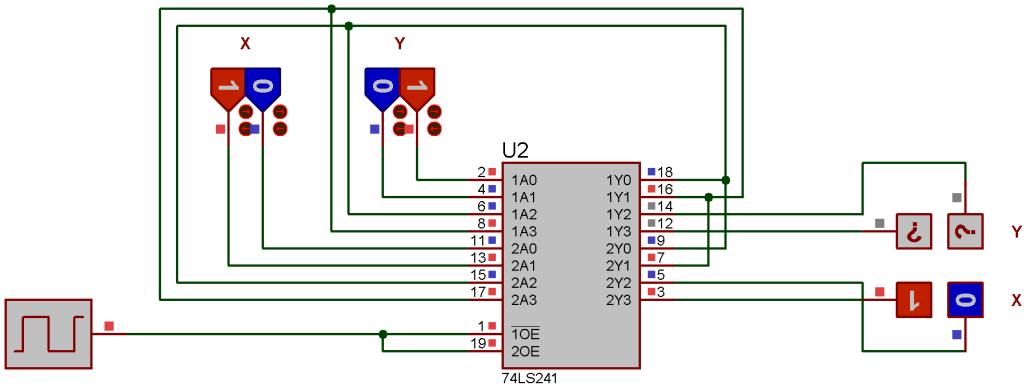
When atleast one of outputs is logic 0, and then Vcc point ties to the ground. So we obtain a passive driver.

2-)



When inputs are entered to the 3-state buffers, only one of them is allowed to pass (high or low).

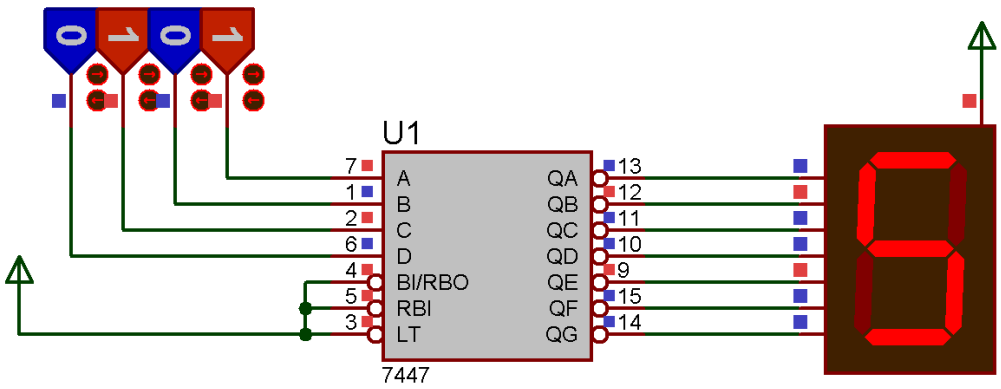
3 -)



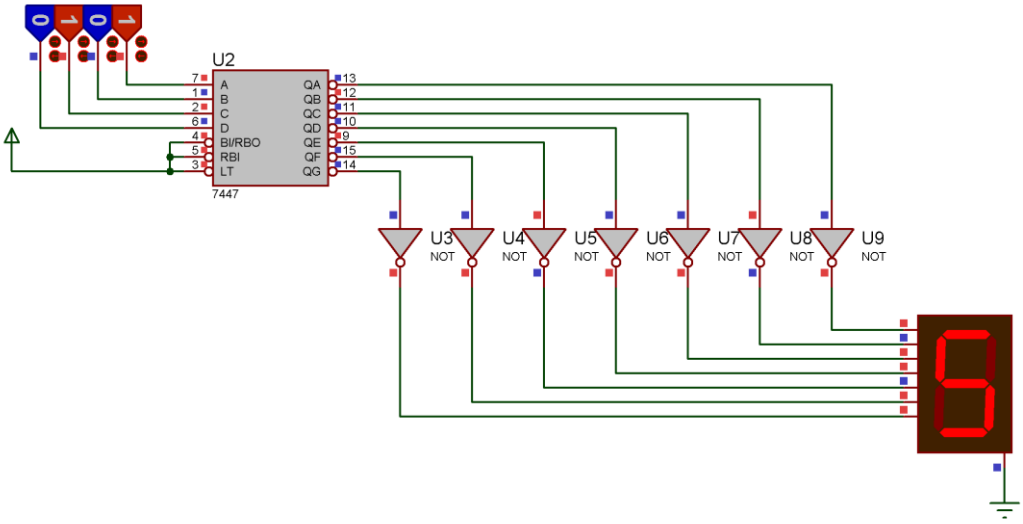
2-bit inputs are entered to the bus.
Choice between two of them is determined by clock signal.
While one input login is taking clock, other one is taking invert of clock. Depends on the clock signals value, only one of the inputs is allowed to pass.

4-)

a-)



b-)


U2
A
B
C
D
BI/RBO
RBI
LT
QA
QB
QC
QD
QE
QF
QG
7447
U3
NOT
U4
NOT
U5
NOT
U6
NOT
U7
NOT
U8
NOT
U9
NOT