QUESTION 3: [30 Points]

Assume that the ALU (Adder and Logic Unit) in Figure 3 has only the following features:

Feature 1: *ALU can perform the following logical operations:*

AND (AC←AC ∧ M[AR])

XOR (AC←AC ⊕ DR).

Feature 2: *ALU cannot perform the subtraction directly. However, it can perform complement and add operations to perform subtraction.*

Considering the basic computer in Figure 3 with the ALU defined above, write the sequence of register transfer statements needed to execute the commands in the table below.

HINT-1: Fetch and Decode is already done in T0, T1, T2,and T3 cycles.

HINT-2: Addressing mode bit (IR[15]) is already checked.

HINT-3: EA is the effective address in the AR at the time where the commands start executing.

Symbol	***Opcode***	***Symbolic Representation***	***Description***
XOR	000	AC← AC ⊕ *M[EA]*	XOR with AC
SUB	001	AC←AC-M[EA]	Subtract memory from AC
EXC	010	AC←M[EA], M[EA]←AC	Exchange AC and memory
BPA	011	If (AC>0) Then (PC←EA)	Branch if AC positive and non-zero

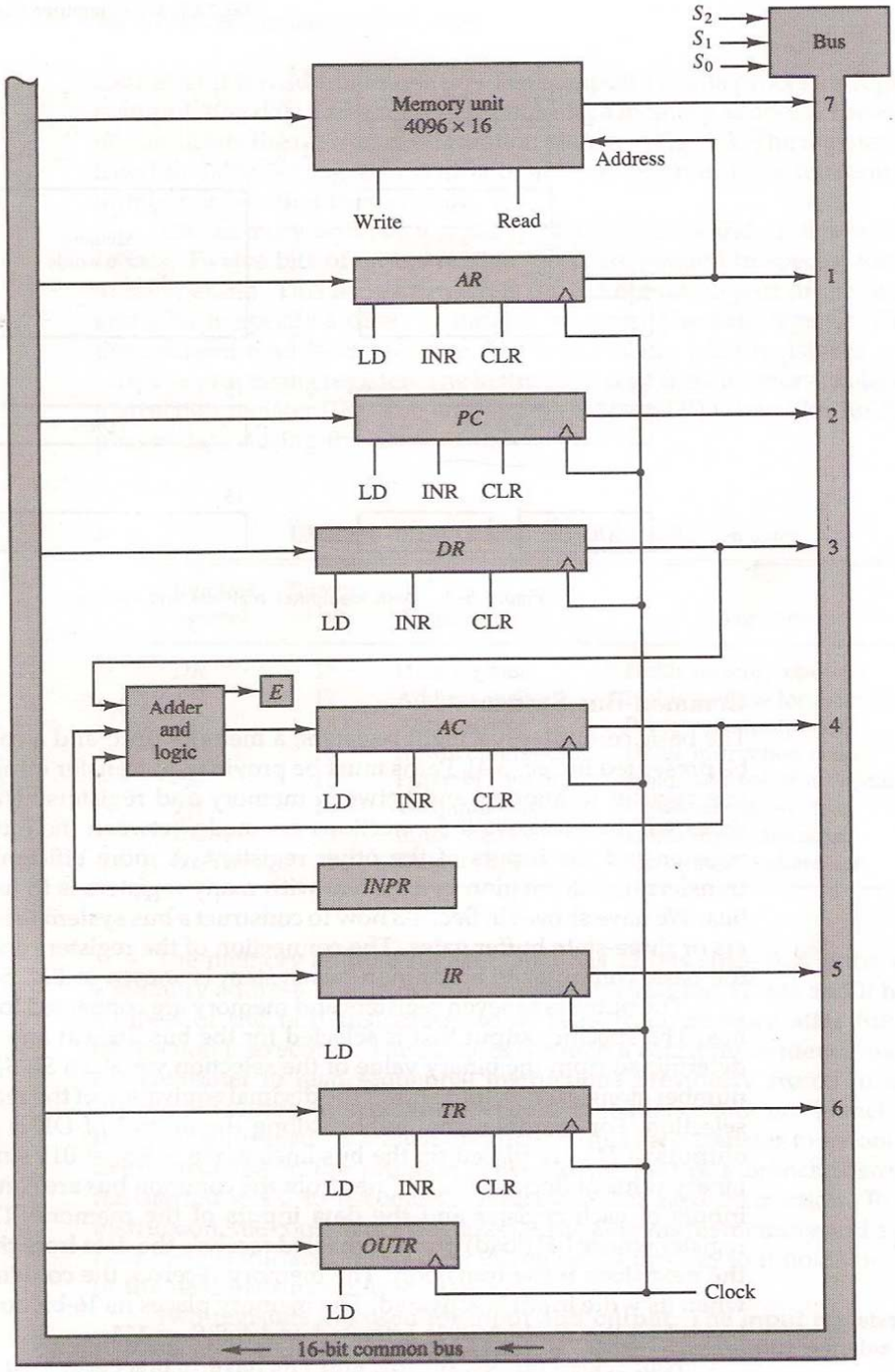

Figure 5-4 Basic computer registers connected to a common bus.

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FIGURE 3

XOR:

D0T4: DR← M[AR]

D0T5: AC←AC⊕*DR* , SC←0

SUB:

D1T4: DR← M[AR]

D1T5: DR←AC, AC←DR,

D1T6: AC← AC'

D1T7: AC←AC*+1*

D1T8: AC← AC+DR, SC←0

EXC

D2T4: DR← M[AR]

D2T5: M[AR]←AC, *AC←DR, SC←0*

BPA

D3T4: if(AC=0 AND AC(15)=0

Then

PC← AR, SC←0