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# **MT7668AUN, MT7668AEN, MT7668ASN Datasheet**

**802.11a/b/g/n/ac Wi-Fi 2T2R + Bluetooth v5.0 Combo Chip**

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# 1 System overview

## 1.1 General Description

MT7668A is highly integrated single chip which features a low power 2x2 11a/b/g/n/ac dual-band Wi-Fi subsystem and a Bluetooth subsystem. The Wi-Fi subsystem contains the 802.11a/b/g/n/ac radio, baseband, and MAC that are designed to meet both the low power and high throughput application. MT7668A has a 32-bit RISC MCU that handles Wi-Fi and Bluetooth tasks, and an ARM Cortex-R4 MCU that could offload data frame processing in Wi-Fi host driver. The Bluetooth subsystem contains the Bluetooth radio, baseband, link controller. It also uses the 32-bit RISC MCU for the Bluetooth protocols.

## 1.2 Features

### 1.2.1 Technology and package

- Highly integrated 28nm RFCMOS technology
- 9x9 QFN 76 pins package

### 1.2.2 Power management and clock source

- Integrate high efficiency power management unit with single 3.3V power supply input
- MT7668ASN support 26MHz,40MHz,52MHz crystal clock with low power operation in idle mode
- MT7668AUN, MT7668AEN support 40MHz crystal clock with low power operation in idle mode
- Buffered clock output for co-clock with other SOC chipset

### 1.2.3 Platform

- 32-bit RISC MCU for Wi-Fi/Bluetooth protocols
- ARM Cortex-R4 MCU for Wi-Fi offload
- Embedded SRAM/ROM
- UART interface with hardware flow control
- Programmable and multiplexed GPIO pins
- MT7668AUN - USB device fully compliant to USB v3.0 specification
- MT7668AEN - PCIe device fully compliant to PCIe v2.1 specification
- MT7668ASN - SDIO device fully compliant to SDIO v3.0 specification

### 1.2.4 WLAN

- IEEE 802.11 a/b/g/n/ac compliant
- Support 20MHz, 40MHz, 80Mhz bandwidth in 2.4GHz band 5GHz band
- Dual-band 2T2R mode
  - MT7668AUN data rate up to 600Mbps with USB3.0
  - MT7668AEN data rate up to 600Mbps with PCIe2.1
  - MT7668ASN data rate up to 450Mbps with SDIO3.0
- Support MU-MIMO RX and DBDC (dual band dual concurrent)
- Support STBC, LDPC, TX Beamformer and RX Beamformee
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11 d/e/h/i/j/k/mc/r/v/w support

- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Optional external LNA and PA support.

### 1.2.5 Bluetooth

- Bluetooth specification 2.1+EDR
- Bluetooth 4.2 Low Energy (LE)
- Bluetooth 5.0
- ANT/ANT+
- Integrated BALUN and PA
- Scatternet support: Up to 7 piconets simultaneously with background inquiry/page scan
- Up to 7 BT link + 32 BLE link
- Support SCO and eSCO link with re-transmission
- Support wide-band speech and hardware accelerated SBC codec for A2DP streaming
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH

### 1.2.6 Miscellaneous

- Integrate 8Kbit efuse to store device specific information and RF calibration data.
- Advanced FDD/TDD mode Wi-Fi/Bluetooth coexistence scheme

## 1.3 Block Diagram

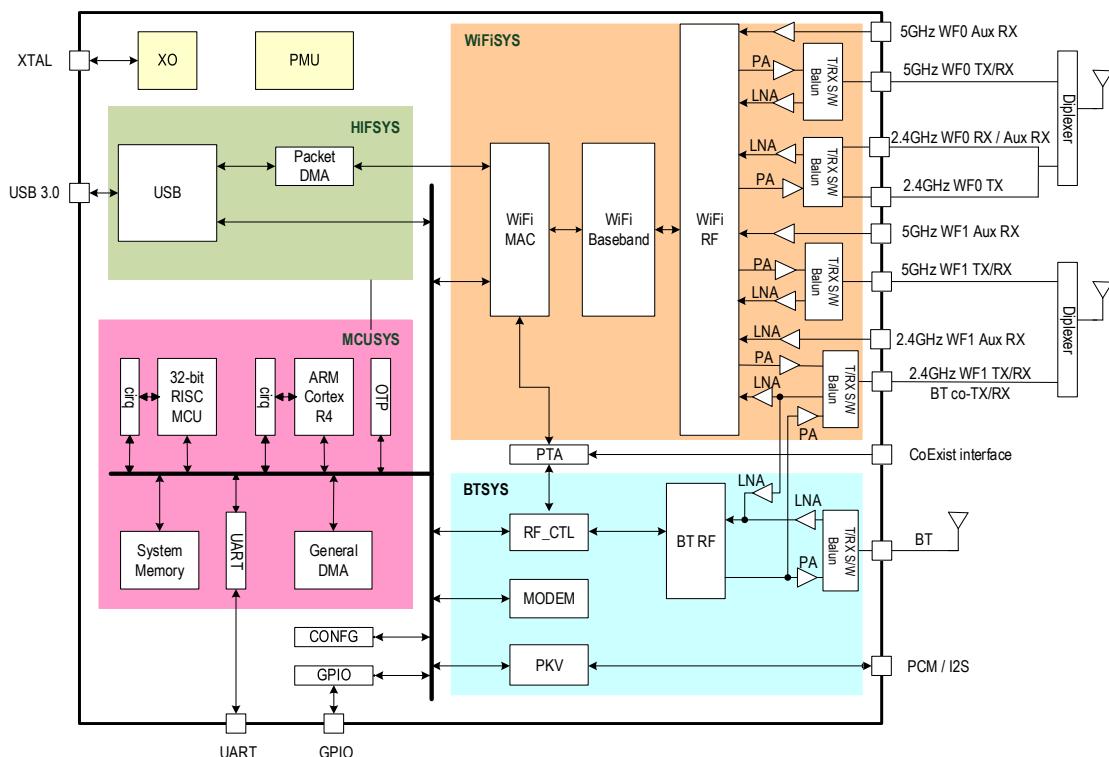


Figure 1 MT7668AUN system-on-chip block diagram

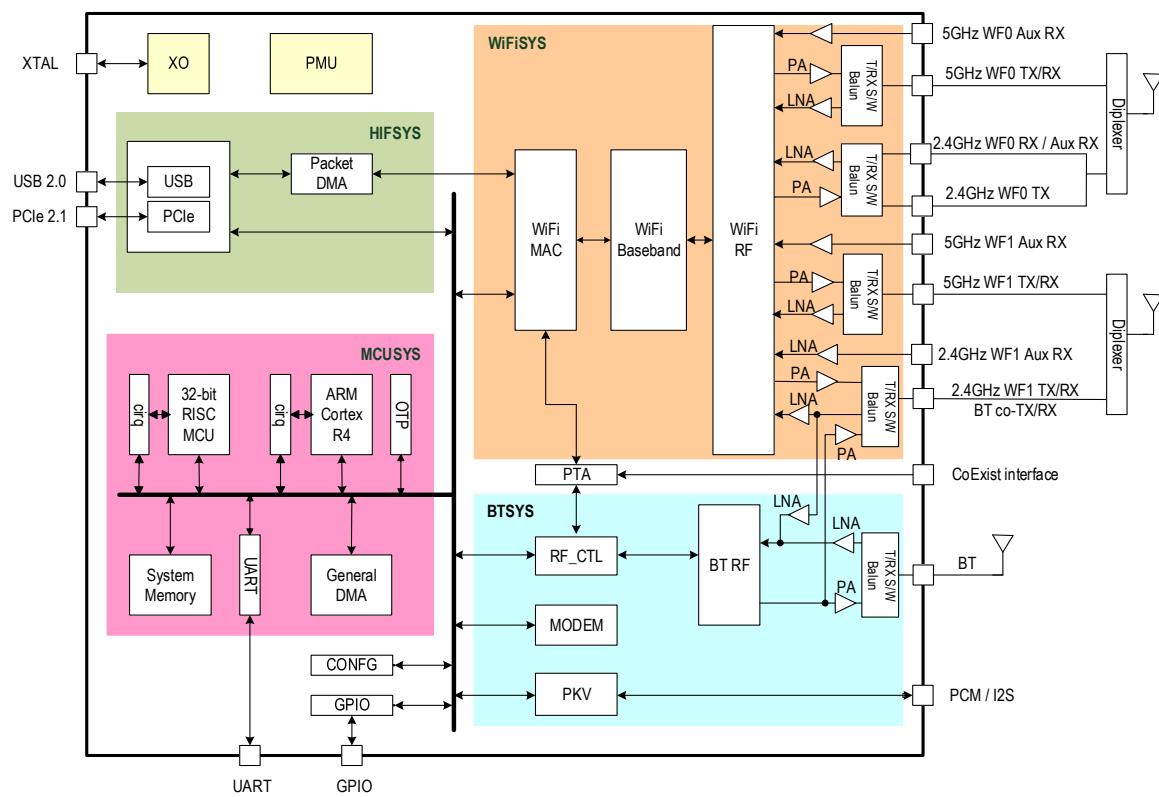


Figure 2 MT7668AEN system-on-chip block diagram

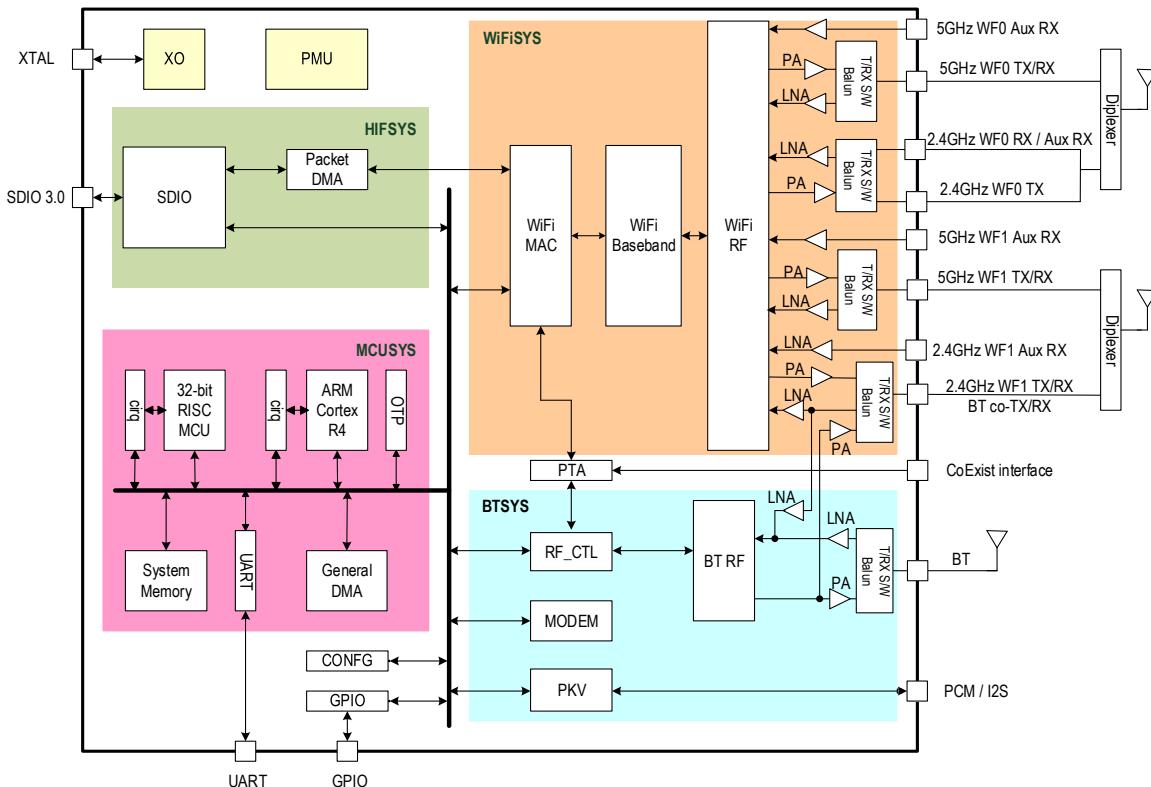


Figure 3 MT7668ASN system-on-chip block diagram

## 2 Functional Description

### 2.1 Overview

MT7668A is designed to support high data throughput over Wi-Fi. The host interface USB3.0 / PCIe2.1 / SDIO3.0 are integrated to provide stable bandwidth between the host platform and MT7668A. The clock rate of the internal bus fabric can also support the throughput requirement. The clock rate of MCU is also configurable for different kinds of scenarios.

MT7668A supports low power requirement. Multiple power domains are implemented on chip. It defines a deep sleep mode, in which only the AON domain is powered on, while other OFF domains are shut off by the power switches integrated on chip. In deep sleep mode, the PMU could be further configured to be in a low power state to save the power consumption. The power, clock, and reset schemes of MT7668A are described in 2.2.

MT7668A has two CPU subsystems. One is ARM cortex R4 subsystem, and the other is a 32-bit RISC MCU subsystem. Both CPU has their local memory. They also have common memory space for MEMORY and memory-mapped hardware engine. There are several options of clock frequency to provide the optimal performance with the best power consumption. The 32-bit RISC MCU is used to do clock control, power management, and host interface configuration. It also handles Wi-Fi MAC operations, and Bluetooth LC operations and audio functions. ARM cortex R4 is used to do host CPU offload for Wi-Fi. PDMA (packet DMA) engines are integrated to support on-the-fly data buffer management. The architecture of 32-bit RISC MCU subsystem is described in 2.3. The architecture of CR4 subsystem id described in 2.4.

MT7668A features USB3.0 / PCIe2.1 / SDIO3.0 for the host interface. The configuration and the feature set of the interface are described in 2.5.

MT7668A has the Wi-Fi MAC, BBP, and the RF subsystems, which provide the best-in-class radio and low power performance. The architecture of Wi-Fi subsystem is described in 2.6.

MT7668A has the Bluetooth LC/BB and the RF subsystems. The architecture of Bluetooth subsystem is described in 2.7.

### 2.2 Chip architecture

The section describes the power, clock, and reset schemes in MT7668A.

#### 2.2.1 Chip power plan

The external power source can be directly supplied to the Power Management Unit, digital IOs, USB/PCIe PHY, and RF circuitry on MT7668A. The on-chip Power Management Unit contains 1 switching regulator and a number of LDOs. It converts the 3.3V input to other power rails.

PMU:

- 3.3V to 2.2V by ALDO for RF circuit.
- 3.3V to 1.8V by PHYLDO for digital IOs and USB/PCIe PHY circuit.

- 3.3V to 1.35V by the switching regulator (Buck converter) for CLDO and RF circuit.
- 1.35V to 1.15V by CLDO for digital circuit.

RF:

- 1.35V to lower voltages by the RF LDOs for RF circuits.

The power scheme is illustrated in the diagram below.

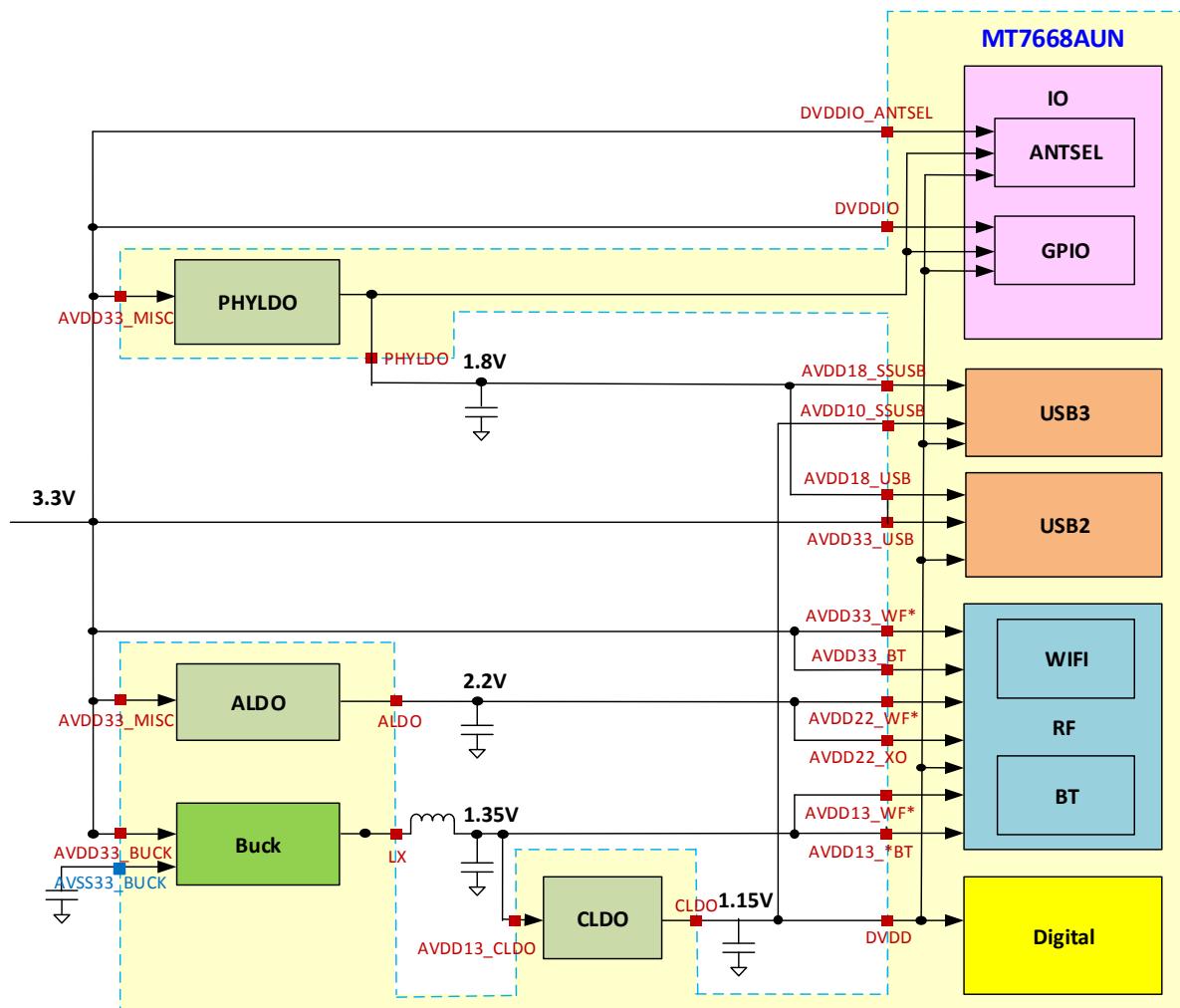


Figure 4 MT7668AUN chip power plan

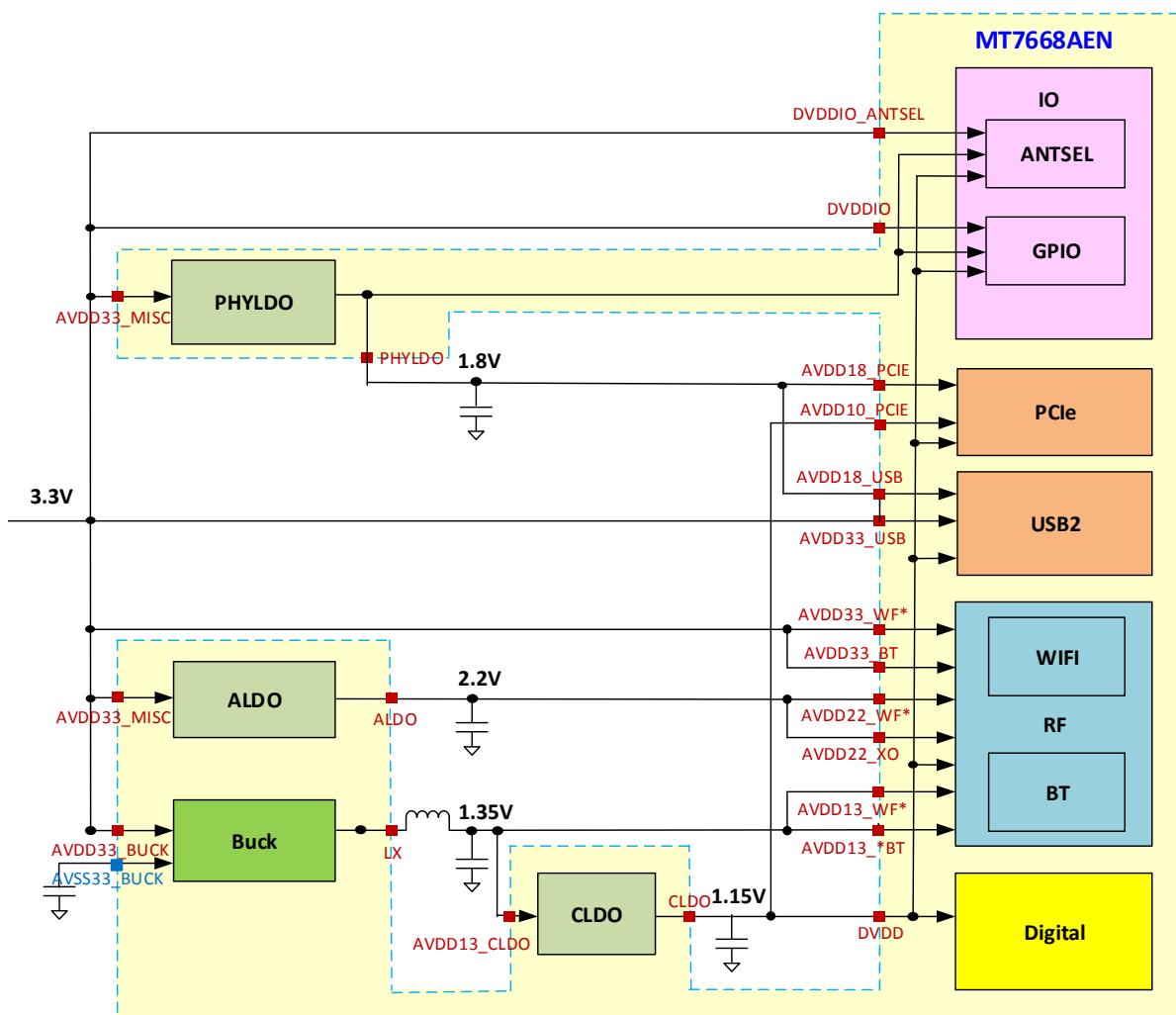
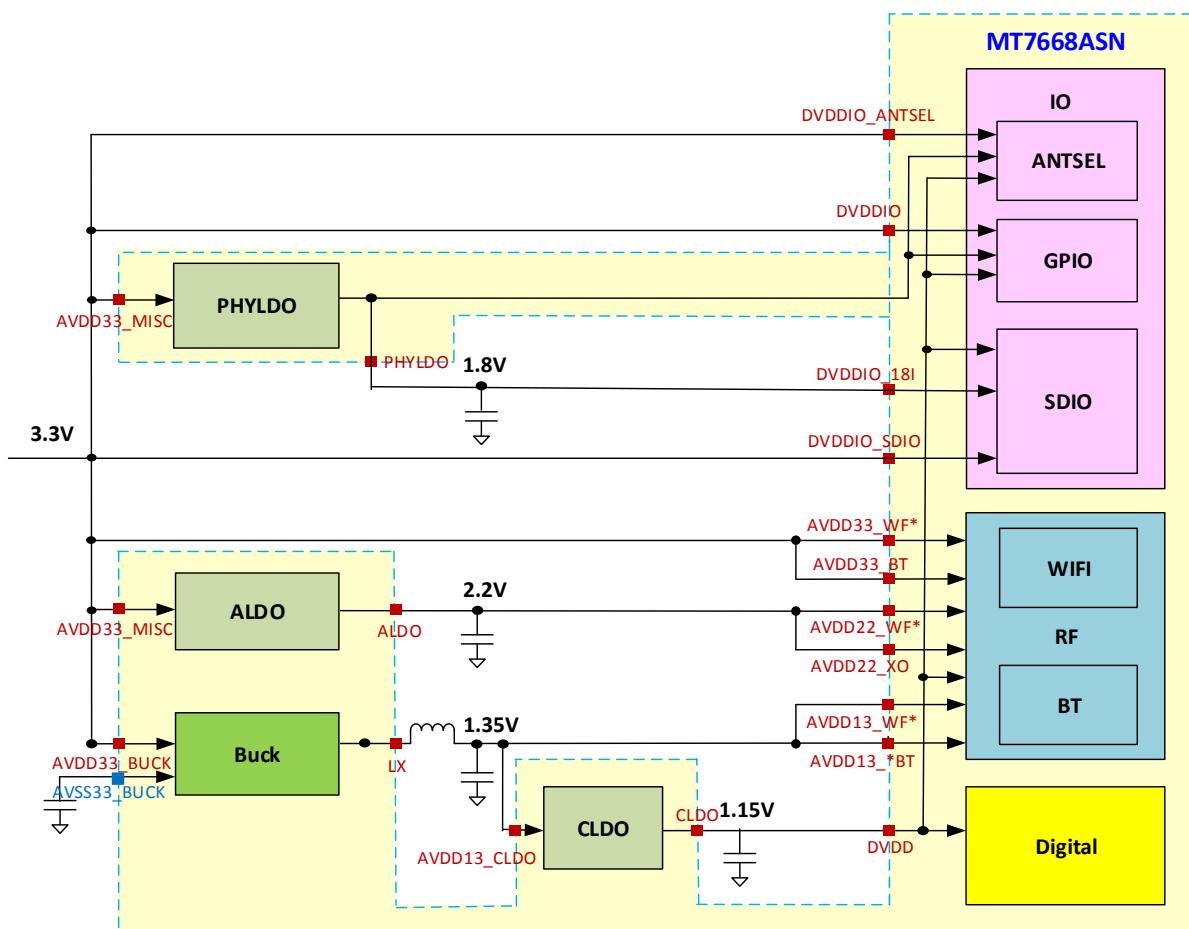


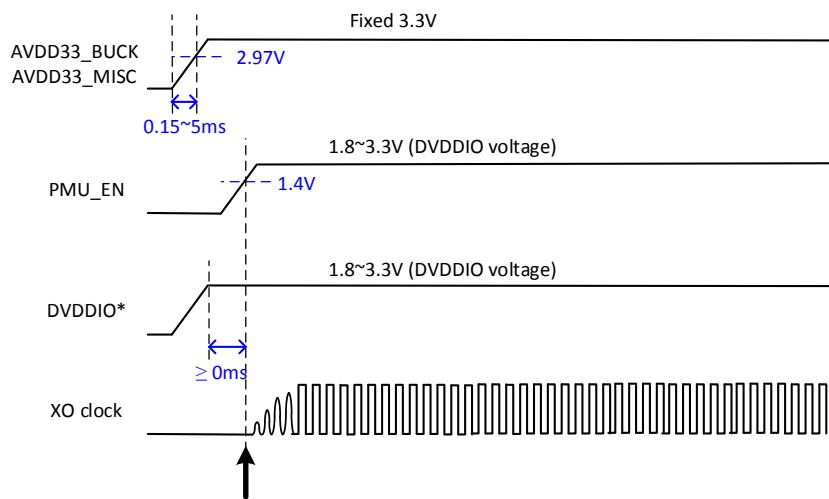
Figure 5 MT7668AEN chip power plan



**Figure 6 MT7668ASN chip power plan**

## 2.2.2 Chip power on sequence

The figure below shows the chip power on sequence.



When AVDD33 and PMU\_EN are both high,  
start chip power-on sequence.

**Figure 7 Chip power on sequence**

### 2.2.3 Digital power domain

The digital circuit is separated into AON (always-on), MCU, Wi-Fi MAC, Wi-Fi baseband, Bluetooth, and USB/PCIe power domains. Except AON, each power domain can be turned off individually for different sleep scenarios.

### 2.2.4 Clock

#### 2.2.4.1 Clock scheme

MT7668A connects to the crystal (XTAL) or the external clock source as the single clock source of the whole system. MT7668ASN XTAL oscillator support the XTAL frequency 26MHz, 40MHz, and 52MHz. MT7668AUN and MT7668AEN XTAL oscillator support 40MHz only.

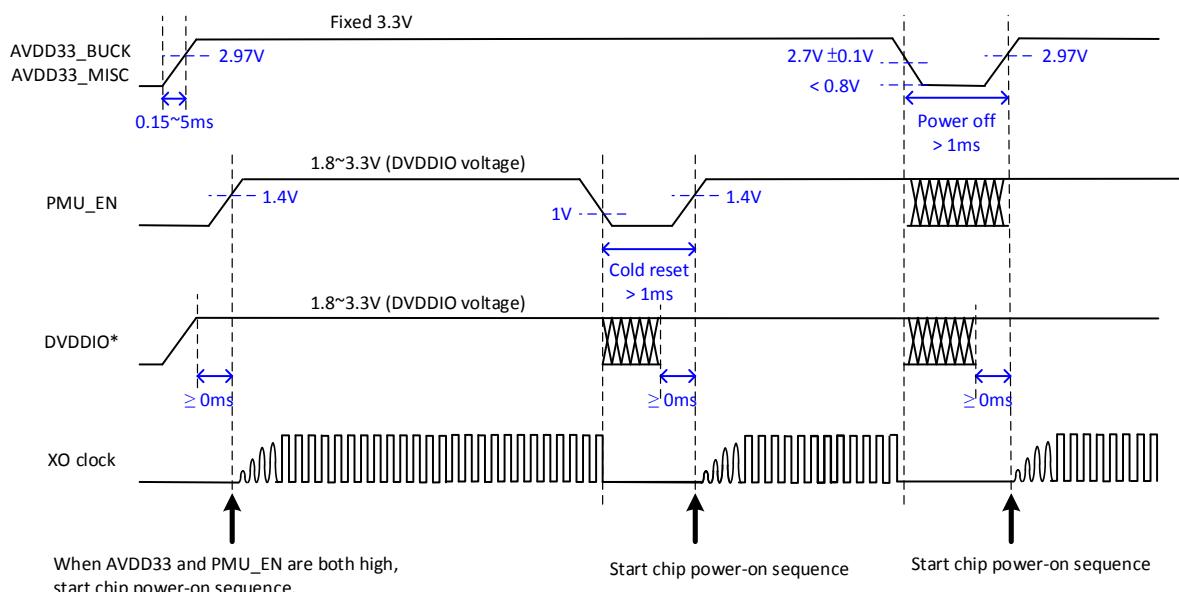
There are 3 major PLLs, MCU PLL, BT PLL, and WF PLL that generate the clocks for the digital circuit. The clocks can be gated to save power when it's not used.

### 2.2.5 Reset

#### 2.2.5.1 Global reset

MT7668A has 2 global resets as follows:

- Cold reset by AVDD33\_BUCK, AVDD33\_MISC, PMU\_EN — Whole chip reset.
- MCU WDT (watch-dog-timer) reset — Reset digital circuit, except strapping, PMU, and XTAL controller.

**Figure 8 Cold reset sequence**

## 2.3 32-bit RISC MCU subsystem

The 32-bit RISC MCU subsystem is built upon a multi-layer AHB bus fabric infrastructure. There is 736KB ROM and 192KB RAM in local instruction memory, and 448KB RAM in local data memory, with 1T access capability.

## 2.4 CR4 subsystem

MT7668A features ARM Cortex-R4 MCU to offload WiFi. There is 544KB TCM (tightly-coupled-memory) with 1T access capability.

## 2.5 Host interface subsystem

### 2.5.1 USB Interface

MT7668AUN supports USB device port which is fully compliant with the Universal Serial Bus Specification, Revision v3.0 (USB v3.0 specification). It supports high-speed and full-speed mode, suspend/resume signaling, as well as remote wake-up signaling.

MT7668AUN offers Bluetooth SIG standard HCI interface over USB. It contains the following endpoints:

- A Control Endpoint (Endpoint 0x0) for HCI commands.
- An Interrupt Endpoint (Endpoint 0x81) for HCI events.
- A Bulk IN Endpoint (Endpoint 0x82) for receiving ACL data.
- A Bulk OUT Endpoint (Endpoint 0x02) for transmitting ACL data.
- An Isochronous IN Endpoint (Endpoint 0x83) for receiving SCO voice.
- An Isochronous OUT Endpoint (Endpoint 0x03) for transmitting SCO voice.

It offers 6 OUT Endpoints (Endpoint 0x04~0x09) and 2 IN Endpoints (Endpoint 0x84~0x85) for Wi-Fi data transmission with flexible queue management.

Data aggregation is used to enhance the throughput over USB interface. Internal pull-up and pull-down resistors are integrated to indicate signaling speed capability. The USB descriptors including VID and PID can be customized. The configuration of the endpoints and the customized USB descriptors are predefined and stored in the Efuse or external flash. They are fetched and used by the USB firmware to provide the desired setting.

### 2.5.2 SDIO interface

MT7668ASN supports SDIO device which is fully compliant with the SDIO Specification Version 3.00. It supports UHS104 Card spec for DS, HS, SDR12, SDR25, SDR50, DDR50, and SDR104 (208MHz) bus speed.

The configuration is illustrated below.

- Support dual SDIO interfaces
- SDIO function 1 is used for Wi-Fi
- SDIO function 2 is used for Bluetooth
- Wi-Fi TX packet de-aggregation and W-Fi RX packet aggregation

- Wi-Fi ISR / RX enhanced read mode
- CIS (card information structure) for dual SDIO interfaces and multiple functions
- Support control register port single read / write access
- Support data port single and burst read / write access
- Embedded virtual direct DMA for WIFISYS
- Two TX channels and two RX channels

### 2.5.3 PCIe interface

MT7668AEN supports PCI Express End Point which is fully compliant with the PCI Express Base Specification Revision 2.0. It supports PCI Express Gen1 (2.5Gbps) and PCIE Express Gen2 (5.0Gbps) differential bus speed.

MT7668AEN supports PCI Express low power operations such as ASPM L1.0, ASPM L1.CLK\_PM, ASPM L1.SS (L1.1 and L1.2), and PCI PM L2 state. It also supports WAKE\_N for device wakeup host scenario, as well as remote wake-up signaling.

The PCI Express interface is only used for Wi-Fi operations. The DMA ring and the data structure are controlled by the descriptor-based PDMA engine over PCI Express interface.

## 2.6 Wi-Fi subsystem

### 2.6.1 Wi-Fi MAC

#### 2.6.1.1 Features

Wi-Fi MAC supports the following features:

- Support all date rates of 802.11a/g including 6, 9, 12, 18, 24, 36, 48, and 54Mbps
- Support short GI and all data rates of 802.11n including MCS0 to MCS7
- Support 802.11ac MCS0 to MCS9
- AMPDU/AMSDU RX (de-aggregation) and TX (aggregation) support
- TX beaformer and RX beamformee
- TX rate adaptation
- TX power control
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP hardware processing
  - GCMP hardware processing
  - SMS4-WPI (WAPI) hardware processing
- Support 2x2 and two independent 1x1 operations
- Low power beacon filtering
- Management/control frame filtering

## 2.6.2 WLAN Baseband

### 2.6.2.1 Features

Wi-Fi baseband supports the following features:

- 20/40/80 MHz channels and 80+80 MHz mode
- Dual band dual concurrent (DBDC)
  - Two Wi-Fi ports can work on two different bands (A-band and G-band) concurrently
  - Use WF0 for A-band, and WF1 for G-band for better performance
- VHT MCS0-9 BW20/40/80MHz with Nss=1~2
- BW80+80MHz with Nss=1
  - Any two non-contiguous 80 MHz channels can be used as a non-contiguous 80+80 MHz channel.
  - Works on A-band only. The throughput of 1 stream BW80+80 is equal to 2 stream BW80.
- Short Guard Interval
- Space-time block code (STBC)
- Low Density Parity check (LDPC)
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- DFS radar detection
- Beamformer (explicit/implicit)
  - Decoded BW20/40/80 up to 2x2 BF matrix apply
  - Not support BW80+80 and DBDC
- Beamformee
  - Decoded BW20/40/80 up to 4x2 MU matrix feedback
  - Decoded BW80+80 up to 4x1 MU matrix feedback
  - DBDC (20/40/80) up to 4x1 MU matrix feedback, one band only
- MU-MIMO RX (MU capable STA only, can't be AP for DL-MU-MIMO)
- Support 2x2 and two independent 1x1 operations.
- 802.11v location

## 2.6.3 WLAN RF

RF supports the following features:

- Integrated 2.4GHz/5GHz PA and LNA, and T/R switch
- Integrated 2.4GHz/5GHz Balun
- Support 2.4GHz/5GHz external PA and LNA
- Support frequency band
  - 2400-2497MHz
  - 5150-5350MHz
  - 5470-5725MHz
  - 5725-5850MHz
  - 5850-5925MHz
- Configurable PA that provides different PA modes at different power levels for power consumption optimization
- Shared RF port for Wi-Fi and Bluetooth, when Co-RX enabled.

## 2.7 Bluetooth subsystem

### 2.7.1 Feature set

MT7668A Bluetooth supports the following features:

- Bluetooth v4.2
  - LE privacy 1.2
  - Data length extension
  - LE security connection
- Bluetooth 5.0
  - BLE 2Mbps
  - Public Indoor Position (direction finding)
- Single-ended, RF port with integrated Balun and T/R switch
- Integrated high efficiency PA
- Baseband and radio BDR and EDR packet types: 1Mbps (GFSK), 2Mbps ( $\pi/4$ -DQPSK), and 3Mbps (8PSK).
- Fully functional Bluetooth baseband: AFH, forward error correction, header error control, access code correlation, CRC, whitening.
- Standard pairing, authentication, link key, and encryption operation.
- Standard power saving mechanisms: sniff mode and sniff-subrating.
- Interlaced scan for faster connection setup
- Up to 7 simultaneous active ACL connections with background inquiry and page scan
- Up to 32 BLE links
- ANT/ANT+ support
- Scatternet support
- Channel quality driven data rate control
- WB RSSI support. Monitor environment air condition to select good channel for AFH

The Bluetooth baseband subsystem of MT7668A contains a baseband processor which supports timing control, bit stream processing, encryption, frequency hopping and modulation/demodulation. The baseband processor fulfills v2.1+EDR, BT3.0+HS, v4.0 BLE, v4.1+HS and ANT/ANT+ specifications, and contains the voice codec, PCM interface controller, WLAN coexistence interface controller and a sleep mode controller. It also supports SCO over I2S, and can function as I2S master or slave. The I2S interface signals share the pins of PCM interface. MT7668A Bluetooth enhances BT and BLE encryption with AES-128.

One hardware accelerator is added to implement packet loss concealment function. The packet loss concealment (PLC) function is used to improve the voice quality in a noisy environment. A low-power scan function, deep sleep mode function and PLL idle mode function are implemented in MT7668A to reduce the power consumption in the scan mode.

## 3 Radio Characteristics

### 3.1 Wi-Fi Radio Characteristics

#### 3.1.1 Wi-Fi RF Block Diagram

MT7668A has two Wi-Fi RF ports. Port 0 is a Wi-Fi only port with WF0 circuit, while port 1 is a shared port with WF1 and Bluetooth circuit.

The front-end loss with diplexer: 2.4GHz insertion loss is 1.0dB, 5GHz insertion loss is 1.5dB.

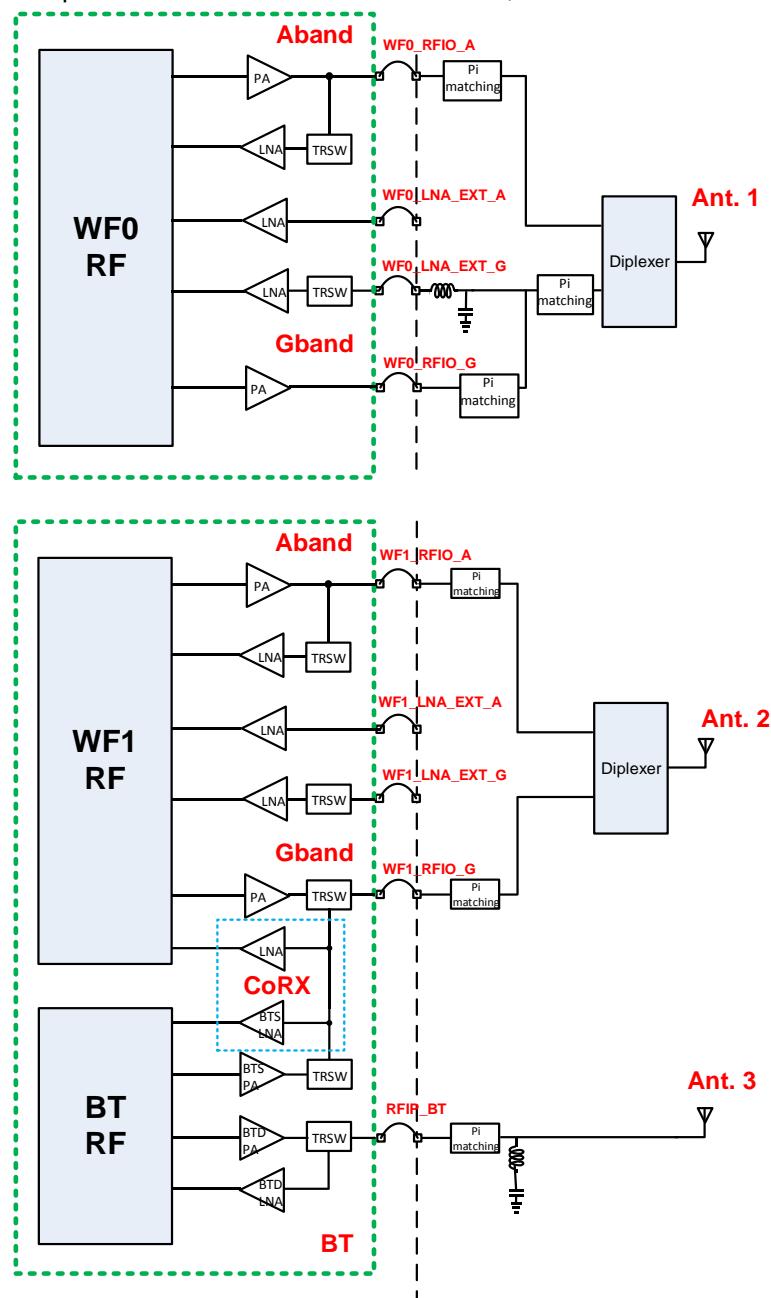


Figure 9 2.4/5GHz RF block diagram

### 3.1.2 Wi-Fi 2.4GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the front-end loss. The data of MCS15 is measured with  $N_{ss}=2$ , while the others are measured with  $N_{ss}=1$  and applicable for WF0 and WF1 in the block diagram above.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-97	-	dBm
	2 Mbps CCK	-	-94	-	dBm
	5.5 Mbps CCK	-	-92	-	dBm
	11 Mbps CCK	-	-89	-	dBm
RX sensitivity	6 Mbps OFDM	-	-94.5	-	dBm
	9 Mbps OFDM	-	-92	-	dBm
	12 Mbps OFDM	-	-91.5	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-85.5	-	dBm
	36 Mbps OFDM	-	-82.5	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
	MCS 0	-	-93.5	-	dBm
RX Sensitivity BW=20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 1	-	-90.5	-	dBm
	MCS 2	-	-88	-	dBm
	MCS 3	-	-85	-	dBm
	MCS 4	-	-81.5	-	dBm
	MCS 5	-	-77	-	dBm
	MCS 6	-	-76	-	dBm
	MCS 7	-	-74.5	-	dBm
	MCS 15	-	-74	-	dBm
	MCS 0	-	-90.5	-	dBm
	MCS 1	-	-87.5	-	dBm
RX Sensitivity BW=40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 2	-	-85	-	dBm
	MCS 3	-	-81.5	-	dBm
	MCS 4	-	-78.5	-	dBm
	MCS 5	-	-74	-	dBm
	MCS 6	-	-73	-	dBm
	MCS 7	-	-71.5	-	dBm
	MCS 15	-	-71	-	dBm
	11 Mbps CCK	-	-10	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
Maximum Receive Level	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
	1 Mbps CCK	-	43	-	dBm
	11 Mbps CCK	-	41	-	dBm
Receive Adjacent Channel Rejection	6 Mbps OFDM	-	41	-	dBm
	54 Mbps OFDM	-	27	-	dBm
	MCS 0	-	37	-	dBm
	MCS 7	-	13	-	dBm
Receive Adjacent Channel Rejection (HT20)	MCS 0	-	29	-	dBm
	MCS 7	-	8	-	dBm
Receive Adjacent Channel Rejection (HT40)	MCS 0	-	29	-	dBm
	MCS 7	-	8	-	dBm

**Table 1 2.4GHz RF receiver specification****3.1.3 Wi-Fi 2.4GHz band RF transmitter specifications**

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
Output power at 25°C and 3.3V with mask and EVM compliance	1~11 Mbps CCK	-	21	-	dBm
	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	18	-	dBm
	HT20, MCS 0	-	18	-	dBm
	HT20, MCS 7	-	17.5	-	dBm
	HT20, MCS 0	-	17	-	dBm
	HT40, MCS 7	-	16.5	-	dBm
Output power variation <sup>1</sup>	TSSI closed-loop control across all temperature range and channels and VSWR $\leq 1.5:1$ .	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3rd Harmonic	-	-45	-	dBm/MHz

Note 1: VDD33 voltage is within  $\pm 5\%$  of typical value

**Table 2 2.4GHz RF transmitter specifications****3.1.4 Wi-Fi 5GHz band RF receiver specifications**

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	GHz
RX sensitivity	6 Mbps OFDM	-	-93.5	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-84.5	-	dBm
	36 Mbps OFDM	-	-81.5	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-75.5	-	dBm
	MCS 0	-	-93	-	dBm
RX Sensitivity BW=20MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 1	-	-89.5	-	dBm
	MCS 2	-	-87	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-80.5	-	dBm
	MCS 5	-	-76	-	dBm
	MCS 6	-	-75	-	dBm
	MCS 7	-	-73.5	-	dBm
	MCS 8	-	-69	-	dBm
	MCS 0	-	-89.5	-	dBm
RX Sensitivity BW=40MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 1	-	-86.5	-	dBm
	MCS 2	-	-84	-	dBm
	MCS 3	-	-80.5	-	dBm
	MCS 4	-	-77.5	-	dBm
	MCS 5	-	-73	-	dBm
	MCS 6	-	-72	-	dBm

	MCS 7	-	-70.5	-	dBm
	MCS 8	-	-66	-	dBm
	MCS 9	-	-64.5	-	dBm
RX Sensitivity BW=80MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-86.5	-	dBm
	MCS 1	-	-83.5	-	dBm
	MCS 2	-	-80.5	-	dBm
	MCS 3	-	-77.5	-	dBm
	MCS 4	-	-74	-	dBm
	MCS 5	-	-70	-	dBm
	MCS 6	-	-68.5	-	dBm
	MCS 7	-	-67	-	dBm
	MCS 8	-	-63	-	dBm
	MCS 9	-	-61	-	dBm
RX Sensitivity BW=160MHz VHT (BW80+BW80) Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-82.5	-	dBm
	MCS 1	-	-79.5	-	dBm
	MCS 2	-	-76.5	-	dBm
	MCS 3	-	-73.5	-	dBm
	MCS 4	-	-70	-	dBm
	MCS 5	-	-66	-	dBm
	MCS 6	-	-64.5	-	dBm
	MCS 7	-	-63	-	dBm
	MCS 8	-	-59	-	dBm
	MCS 9	-	-57	-	dBm
Maximum Receive Level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection (VHT20)	MCS0	-	28	-	dBm
	MCS8	-	0	-	dBm
Receive Adjacent Channel Rejection (VHT40)	MCS 0	-	27	-	dBm
	MCS 9	-	1	-	dBm
Receive Adjacent Channel Rejection (VHT80)	MCS 0	-	31	-	dBm
	MCS 9	-	12	-	dBm

Table 3 5GHz RF receiver specifications

### 3.1.5 Wi-Fi 5GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	MHz
Output power at 25°C and 3.3V with mask and EVM compliance	6 Mbps OFDM	-	18	-	dBm
	54 Mbps OFDM	-	17	-	dBm
	HT20, MCS 0	-	17	-	dBm
	HT20, MCS 7	-	16	-	dBm
	HT40, MCS 0		16.5		
	HT40, MCS 7		15.5		
	VHT80, MCS0	-	16.5	-	dBm
	VHT80, MCS9	-	15	-	dBm
Output power variation <sup>1</sup>	TSSI closed-loop control across all temperature range and channels and VSWR $\leq 1.5:1$ .	-2	-	2	dB

Carrier suppression		-	-	-30	dBc
Harmonic Power	Output	2nd Harmonic	-	-45	dBm/MHz
		3rd Harmonic	-	-45	dBm/MHz

Note 1: VDD33 voltage is within  $\pm 5\%$  of typical value

Table 4 5GHz RF transmitter specifications

## 3.2 Bluetooth Radio Characteristics

### 3.2.1 Bluetooth RF Block Diagram

MT7668A Bluetooth RF can be dedicated port (BTD) or shared port (BTS). In BTD, Bluetooth has a dedicated Bluetooth only port. In BTS, Bluetooth share the port with WF1 circuit.

The Ant. 3 frond-end loss is about 0.8dB.

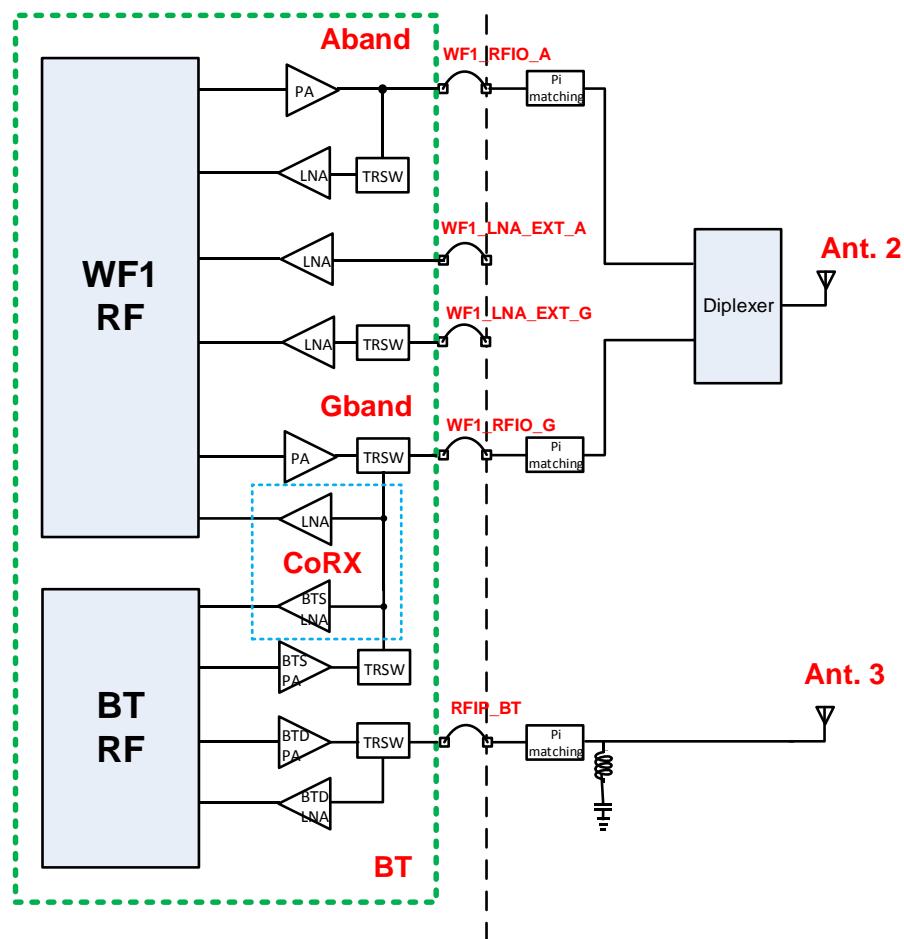


Figure 10 Wi-Fi/Bluetooth RF block diagram

### 3.2.2 Basic rate receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss. The data is measured with Bluetooth dedicated port.

PARAMETER	DESCRIPTION	PERFORMANCE			
		MIN	TYP	MAX	Unit
Frequency range		2402	-	2480	MHz

Receiver sensitivity <sup>1</sup>	BER<0.1%	-	-94.5	-70	dBm
Maximum usable signal	BER<0.1%	-20	-5	-	dBm
C/I co-channel (BER<0.1%)	Co channel selectivity	-	6	11	dB
C/I 1MHz (BER<0.1%)	Adjacent channel selectivity	-	-7	0	dB
C/I 2MHz (BER<0.1%)	2 <sup>nd</sup> adjacent channel selectivity	-	-40	-30	dB
C/I $\geq$ 3MHz (BER<0.1%)	3 <sup>rd</sup> adjacent channel selectivity	-	-43	-40	dB
C/I Image channel (BER<0.1%)	Image channel selectivity	-	-20	-9	dB
C/I Image 1MHz (BER<0.1%)	1MHz adjacent to image channel selectivity	-	-35	-20	dB
Inter-modulation		-39	-30	-	dBm
Out-of-band blocking	30MHz to 2000MHz	-10	-	-	dBm
	2000MHz to 2399MHz	-27	-	-	dBm
	2498MHz to 3000MHz	-27	-	-	dBm
	3000MHz to 12.75GHz	-10	-	-	dBm

Note 1: The receiver sensitivity is measured at the antenna port.

**Table 5 Basic rate receiver specifications**

### 3.2.3 Basic rate transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

PARAMETER	DESCRIPTION	PERFORMANCE			
		MIN	TYP	MAX	Unit
Frequency range		2402	-	2480	MHz
Output power <sup>1</sup>	At maximum power output level	-	12	-	dBm
Gain step		2	4	8	dB
Modulation characteristics	$\Delta f_1 avg$	140	157	175	KHz
	$\Delta f_2 max$ (For at least 99.9% of all $\Delta f_2 max$ )	115	145	-	KHz
	$\Delta f_1 avg / \Delta f_2 avg$	0.8	0.98	-	KHz
ICFT	Initial carrier frequency tolerance	-75	$\pm 18$	+75	KHz
Carrier frequency drift	One slot packet (DH1)	-25	$\pm 10$	+25	KHz
	Two slot packet (DH3)	-40	$\pm 10$	+40	KHz
	Five slot packet (DH5)	-40	$\pm 10$	+40	KHz
	Max drift rate	-	10	20	KHz/50 $\mu$ s
TX output spectrum	20dB bandwidth	-	922	1000	KHz
In-Band spurious emission	$\pm 2$ MHz offset	-	-38	-20	dBm
	$\pm 3$ MHz offset	-	-43	-40	dBm
	> $\pm 3$ MHz offset	-	-45	-40	dBm

Note 1: The output power is measured at the antenna port.

**Table 6 Basic rate transmitter specifications**

### 3.2.4 Enhanced data rate receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

PARAMETER	DESCRIPTION	PERFORMANCE			
		MIN	TYP	MAX	Unit
Frequency range		2402	-	2480	MHz
Receiver sensitivity (BER<0.01%) <sup>1</sup>	$\pi/4$ DQPSK	-	-95	-	dBm
	8PSK	-	-89	-	dBm
Maximum usable signal (BER<0.1%)	$\pi/4$ DQPSK	-	-5	-	dBm
	8PSK	-	-5	-	dBm
C/I co-channel (BER<0.1%)	$\pi/4$ DQPSK	-	9	13	dB

	8PSK	-	15	21	dB
C/I 1MHz (BER<0.1%)	$\pi/4$ DQPSK	-	-12	0	dB
	8PSK	-	-6	5	dB
C/I 2MHz (BER<0.1%)	$\pi/4$ DQPSK	-	-40	-30	dB
	8PSK	-	-36	-25	dB
C/I $\geq$ 3MHz (BER<0.1%)	$\pi/4$ DQPSK	-	-43	-40	dB
	8PSK	-	-40	-33	dB
C/I Image channel (BER<0.1%)	$\pi/4$ DQPSK	-	-20	-7	dB
	8PSK	-	-15	0	dB
C/I Image 1MHz (BER<0.1%)	$\pi/4$ DQPSK	-	-40	-20	dB
	8PSK	-	-30	-13	dB

Note 1: The receiver sensitivity is measured at the antenna port.

**Table 7 Enhanced data rate receiver specifications**

### 3.2.5 Enhanced data rate transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

PARAMETER	DESCRIPTION	PERFORMANCE			
		MIN	TYP	MAX	Unit
Frequency range		2402	-	2480	MHz
Maximum transmit power <sup>1</sup>	$\pi/4$ DQPSK	-	9	-	dBm
	8PSK	-	9	-	dBm
Relative transmit power	$\pi/4$ DQPSK	-	-1.5	-	dB
	8PSK	-	-1.5	-	dB
Frequency stability	maximum carrier frequency stability, $\omega_0$	$\pi/4$ DQPSK 8PSK	-10 -10	$\pm 4$ $\pm 4$	10 10 KHz
	maximum carrier frequency stability, $\omega_i$	$\pi/4$ DQPSK 8PSK	-75 -75	$\pm 18$ $\pm 18$	75 75 KHz
	maximum carrier frequency stability, $ \omega_0 + \omega_i $	$\pi/4$ DQPSK 8PSK	-75 -75	$\pm 20$ $\pm 20$	75 75 KHz
	RMS DEVM	$\pi/4$ DQPSK 8PSK	- -	8 8	20 13 %
	99% DEVM	$\pi/4$ DQPSK 8PSK	- -	11 11	- % %
	Peak DEVM	$\pi/4$ DQPSK 8PSK	- -	15 15	35 25 %
In-Band spurious emission	$\pm 1$ MHz offset	$\pi/4$ DQPSK	-	-29	-26 dB
	$\pm 1$ MHz offset	8PSK	-	-29	-26 dB
	$\pm 2$ MHz offset	$\pi/4$ DQPSK	-	-26	-20 dBm
	$\pm 2$ MHz offset	8PSK	-	-26	-20 dBm
	$\pm 3$ MHz offset	$\pi/4$ DQPSK	-	-40	-40 dBm
	$\pm 3$ MHz offset	8PSK	-	-40	-40 dBm

Note 1: The output power is measured at the antenna port.

**Table 8 Enhanced data rate transmitter specifications**

### 3.2.6 Bluetooth LE receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		2402	-	2480	MHz
Receiver Sensitivity (*)	PER < 30.8%	-	-98	-70	dBm
Max. Usable Signal	PER < 30.8%	-20	-5	-	dBm
C/I Co-channel	Co-channel selectivity (PER < 30.8%)	-	6	21	dB
C/I 1MHz	Adjacent channel selectivity (PER < 30.8%)	-	-7	15	dB
C/I 2MHz	2nd adjacent channel selectivity (PER < 30.8%)	-	-30	-17	dB
C/I $\geq$ 3MHz	3rd adjacent channel selectivity (PER < 30.8%)	-	-33	-27	dB
C/I Image channel	Image channel selectivity (PER < 30.8%)	-	-20	-9	dB
C/I Image 1MHz	1MHz adjacent to image channel selectivity (PER < 30.8%)	-	-30	-15	dB
Out-of-band Blocking	30MHz to 2000MHz	-30	-	-	dBm
	2001MHz to 2339MHz	-35	-	-	dBm
	2501MHz to 3000MHz	-35	-	-	dBm
	3001MHz to 12.75GHz	-30	-	-	dBm

*Note 1: The receiver sensitivity is measured at the antenna port.*

**Table 9 Bluetooth LE receiver specifications**

### 3.2.7 Bluetooth LE transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		2402	-	2480	MHz
Output Power (*)	At default power output level	-20	3	12	dBm
Carrier Frequency Offset and Drift	Frequency offset	-150	$\pm 10$	150	kHz
	Frequency drift	-50	$\pm 10$	50	kHz
	Max. drift rate	-20	$\pm 10$	20	Hz/us
Modulation Characteristic	$\square f_{1\text{avg}}$	225	250	275	kHz
	$\square f_{2\text{max}}$ (For at least 99% of all $\square f_{2\text{max}}$ )	185	215	-	kHz
	$\square f_{2\text{avg}}/\square f_{1\text{avg}}$	0.8	0.9	-	Hz/Hz
In-band Spurious Emission	$\pm 2\text{MHz}$ offset	-	-35	-20	dBm
	$>\pm 3\text{MHz}$ offset	-	-40	-30	dBm

*Note 1: The output power is measured at the antenna port.*

**Table 10 Bluetooth LE transmitter specifications**

### 3.3 Current Consumption

#### 3.3.1 WLAN Current Consumption

Description	Current (average)		
	MT7668AUN	MT7668ASN	Unit
Sleep mode, radio off	1.5 (USB suspend)	1.2 (SDIO bus idle)	mA
2.4GHz RX Power saving, DTIM=1	3.3	3.1	mA
2.4GHz RX Active, HT20, MCS15	144	136	mA
2.4GHz TX CCK, 11Mbps @ 21dBm	403	396	mA
2.4GHz TX HT20, MCS15 @ 17.5dBm	496	488	mA
2.4GHz TX HT20, MCS8 @ 18dBm	520	510	mA
5GHz VHT80 RX Listen, 2RX	154	149	mA
5GHz RX Active, VHT80, MCS9, NSS=2	242	232	mA
5GHz TX VHT80, MCS9, NSS=2 @ 15dBm	678	668	mA
5GHz TX VHT80, MCS0, NSS=2 @ 16.5dBm	713	700	mA

Note:

[1] All result is measured provided VDD33 is 3.3V. TX power is measured at antenna port. Temperature is 25°C.

[2] MT7668AUN host interface is USB2. MT7668ASN host interface is SDIO2.0.

[3] Duty cycle for TX/RX measurement is 100%.

[4] The chip variation is +/- 15%.

**Table 11 WLAN 2.4/5GHz Current Consumption**

#### 3.3.2 Bluetooth Current Consumption

Description	Current (average)		
	MT7668AUN	MT7668ASN	Unit
Sleep mode, radio off	1.5 (USB suspend)	1.2 (SDIO bus idle)	mA
Bluetooth TX @ 9dBm	42	41	mA
Bluetooth RX	21	20	mA
Bluetooth SCO connection, HV3 packets + sniff mode + scan (Page scan interval = 1.28sec, inquiry scan interval = 2.56s, sniff interval = 500ms)	21	20	mA
Bluetooth page scan + inquiry scan (Page scan interval = 1.28s, inquiry scan interval = 2.56s)	1.7	1.6	mA
Bluetooth page scan (Page scan interval = 1.28s)	1.6	1.5	mA

Note:

[1] All result is measured provided VDD33 is 3.3V. TX power is measured at antenna port. Temperature is 25°C.

[2] MT7668AUN host interface is USB2. MT7668ASN host interface is SDIO2.0.

[3] Duty cycle for TX/RX measurement is 100%.

[4] The chip variation is +/- 15%.

**Table 12 Bluetooth 2.4GHz Current Consumption**

## 4 Electrical Characteristics

### 4.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
VDD18	1.8V Supply Voltage	-0.3 to 3.63	V
T <sub>STG</sub>	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 13 Absolute maximum rating

### 4.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD18	1.8V Supply voltage	1.7	1.8	1.9	V
T <sub>AMBIENT</sub>	Ambient Temperature	-10	-	70	°C

Table 14 Recommended operating range

### 4.3 DC characteristics

The digital IO supports VDD33 or VDD18 application.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V <sub>IL</sub>	Input Low Voltage	Input voltage <ul style="list-style-type: none"> <li>• VDD33</li> <li>• VDD18</li> </ul>	-0.3 -0.3	-	VDD33*0.25 VDD18*0.35	V
V <sub>IH</sub>	Input High Voltage	Input voltage <ul style="list-style-type: none"> <li>• VDD33</li> <li>• VDD18</li> </ul>	VDD33*0.625 VDD18*0.65	-	VDD33+0.3 VDD18+0.3	V
V <sub>OL</sub>	Output Low Voltage	Input voltage <ul style="list-style-type: none"> <li>• VDD33</li> <li>• VDD18</li> </ul>  I <sub>OL</sub>   = 4~16 mA	-0.3 -0.3	-	0.4 0.2	V
V <sub>OH</sub>	Output High Voltage	Input voltage <ul style="list-style-type: none"> <li>• VDD33</li> <li>• VDD18</li> </ul>  I <sub>OH</sub>   = 4~16 mA	VDD33-0.4 VDD18-0.2	-	VDD33+0.3 VDD18+0.3	V
R <sub>PU</sub>	Input Pull-Up Resistance	Input voltage <ul style="list-style-type: none"> <li>• VDD33</li> <li>• VDD18</li> </ul> PU=high, PD=low	40 10	75 50	190 100	KΩ
R <sub>PD</sub>	Input Pull-Down Resistance	Input voltage <ul style="list-style-type: none"> <li>• VDD33</li> <li>• VDD18</li> </ul> PU=low, PD=high	40 10	75 50	190 100	KΩ

Table 15 DC characteristics of 3.3V application

## 4.4 XTAL oscillator

The table below lists the requirement for the XTAL.

Parameter	Value
Frequency	MT7668ASN: 26MHz, 40MHz, 52MHz MT7668AUN, MT7668AEN: 40MHz
Frequency stability	±10 ppm @ 25°C

**Table 16 XTAL oscillator requirement**

## 4.5 PMU Characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
<b>Switching regulator(BUCK)</b>					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.28	1.35	1.42	V
Output current		-	-	1000	mA
Quiescent current		-	150	200	uA
Efficiency	500~750mA load current	-	81	-	%
Over-current Shutdown	Iout=1000mA	1.2	-	5	A
<b>Core LDO (CLDO)</b>					
Input voltage		1.3	1.35	1.5	V
Output voltage		0.8	1.15	1.2	V
Output current		-	-	750	mA
Quiescent current		-	40	50	uA
<b>Analog LDO (ALDO)</b>					
Input voltage		2.97	3.3	3.63	V
Output voltage		2.09	2.2	2.31	V
Output current		-	-	100	mA
Quiescent current		-	40	55	uA
<b>PHY LDO</b>					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.7	1.8	1.9	V
Output current		-	-	60	mA
Quiescent current		-	40	50	uA

**Table 17 PMU electrical characteristic**

## 4.6 Thermal characteristics

$\Theta_{JC}$  assumes that all the heat is dissipated through the top of the package, while  $\Psi_{Jt}$  assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use  $\Psi_{Jt}$  to estimate the junction temperature.

Symbol	Description	Performance	
		Typical	Unit
$T_J$	Maximum Junction Temperature (Plastic Package)	125	°C
$\Theta_{JA}$	Junction to ambient temperature thermal resistance	17.03	°C/W
$\Theta_{JC}$	Junction to case temperature thermal resistance	6.7	°C/W
$\Psi_{Jt}$	Junction to the package thermal resistance	1.9	°C/W

Note: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3"x4.5"), 4 layer.

**Table 18 Thermal characteristics**

## 5 Package specification

### 5.1 Pin Layout

MT7668A uses QFN package of with 9mm x 9mm dimension.

	BGF_INT_B	GPIO0	UART_TXD	UART_RXD	PCM_OUT	PCM_IN	DVDDIO	DVDD	PCM_CLK	PCM_SYNC	PDET0	PDET1	AVDD13_WF1_AFE	AVDD13_RXFE_BT	RFIP_BT	AVDD33_BT	TSTRST_B	AVDD22_WF1	AVDD13_WF1_TRX
WIFI_INT_B	1																	57	GPIO1
	NC	2																56	OSC_EN
	NC	3																55	WF1_RFIO_G
AVDD18_SSUSB	4																	54	AVDD33_WF1_PA_G
SSUSB_TXN	5																	53	WF1_LNA_EXT_G
SSUSB_TXP	6																	52	WF1_LNA_EXT_A
AVDD10_SSUSB	7																	51	WF1_RFIO_A
SSUSB_RXN	8																	50	AVDD33_WF1_A_PA
SSUSB_RXP	9																	49	AVDD33_WF1_A_TX
AVDD18_USB	10																	48	AVDD33_WF0_PA_G
USB_DP	11																	47	WF0_RFIO_G
USB_DM	12																	46	WF0_LNA_EXT_G
AVDD33_USB	13																	45	WF0_LNA_EXT_A
DVDD	14																	44	WF0_RFIO_A
PMU_EN	15																	42	AVDD33_WF0_A_PA
AVDD25_V2P5NA	16																	42	AVDD33_WF0_A_TX
AVDD33_BUCK	17																	41	ANTSEL0
LX	18																	40	ANTSEL2
AVSS33_BUCK	19																	39	ANTSEL3
	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
	AVDD13_CLDO	AVDD13_CLDO	CLDO	CLDO	VREF	PHYLDO	AVDD33_MISC	ALDO	DVDDIO_ANTSEL	DVDD	ANTSEL1	AVDD13_WF0_AFE	XO_OUT	XO	AVDD22_XO	ANTSEL5	ANTSEL4	AVDD22_WF0	AVDD13_WF0_TRX

Figure 11 MT7668AUN Pin Layout

	BGF_INT_B	GPIO0	UART_TXD	UART_RXD	PCM_OUT	PCM_IN	DVDD	PCM_CLK	PCM_SYNC	PDET0	PDET1	AVDD13_WF1_AFE	AVDD13_RXFE_BT	RFIP_BT	AVDD33_BT	TSTRST_B	AVDD22_WF1	AVDD13_WF1_TRX	
WIFI_INT_B	1																57	GPIO1	
PCIE_CKRXP	2																56	OSC_EN	
PCIE_CKRXN	3																55	WF1_RFIO_G	
AVDD18_PCIE	4																54	AVDD33_WF1_PA_G	
PCIE_TXN	5																53	WF1_LNA_EXT_G	
PCIE_TXP	6																52	WF1_LNA_EXT_A	
AVDD10_PCIE	7																51	WF1_RFIO_A	
PCIE_RXN	8																50	AVDD33_WF1_A_PA	
PCIE_RXP	9																49	AVDD33_WF1_A_TX	
AVDD18_USB	10																48	AVDD33_WF0_PA_G	
USB_DP	11																47	WF0_RFIO_G	
USB_DM	12																46	WF0_LNA_EXT_G	
AVDD33_USB	13																45	WF0_LNA_EXT_A	
DVDD	14																44	WF0_RFIO_A	
PMU_EN	15																42	AVDD33_WF0_A_PA	
AVDD25_V2P5NA	16																42	AVDD33_WF0_A_TX	
AVDD33_BUCK	17																41	ANTSEL0	
LX	18																40	ANTSEL2	
AVSS33_BUCK	19																39	ANTSEL3	
	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
	AVDD13_CLDO	AVDD13_CLDO	CLDO	CLDO	VREF	PHYLDO	AVDD33_MISC	ALDO	DVDDIO_ANTSEL	DVDD	ANTSEL1	AVDD13_WF0_AFE	XO_OUT	XO	AVDD22_XO	ANTSEL5	ANTSEL4	AVDD22_WF0	AVDD13_WF0_TRX

Figure 12 MT7668AEN Pin Layout

	BGF_INT_B	GPIO0	UART_TXD	UART_RXD	PCM_OUT	PCM_IN	DVDDIO	DVDD	PCM_CLK	PCM_SYNC	PDET0	PDET1	AVDD13_WF1_AFE	AVDD13_RXFE_BT	RFIP_BT	AVDD33_BT	TSTRST_B	AVDD22_WF1	AVDD13_WF1_TRX	
WIFI_INT_B	1																		57	GPIO1
	NC	2																	56	OSC_EN
	NC	3																	55	WF1_RFIO_G
	NC	4																	54	AVDD33_WF1_PA_G
	DVDD	5																	53	WF1_LNA_EXT_G
	SDIO_DS	6																	52	WF1_LNA_EXT_A
	SDIO_DAT0	7																	51	WF1_RFIO_A
	SDIO_DAT1	8																	50	AVDD33_WF1_A_PA
	SDIO_CLK	9																	49	AVDD33_WF1_A_TX
	SDIO_DAT2	10																	48	AVDD33_WF0_PA_G
	SDIO_CMD	11																	47	WF0_RFIO_G
	SDIO_DAT3	12																	46	WF0_LNA_EXT_G
	DVDDIO_SDIO	13																	45	WF0_LNA_EXT_A
	DVDDIO_18I	14																	44	WF0_RFIO_A
	PMU_EN	15																	42	AVDD33_WF0_A_PA
	AVDD25_V2P5NA	16																	42	AVDD33_WF0_A_TX
	AVDD33_BUCK	17																	41	ANTSEL0
	LX	18																	40	ANTSEL2
	AVSS33_BUCK	19																	39	ANTSEL3
		20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
		AVDD13_CLDO	AVDD13_CLDO	CLDO	CLDO	VREF	PHYLDO	AVDD33_MISC	ALDO	DVDDIO_ANTSEL	DVDD	ANTSEL1	AVDD13_WF0_AFE	XO_OUT	XO	AVDD22_XO	ANTSEL5	ANTSEL4	AVDD22_WF0	AVDD13_WF0_TRX

Figure 13 MT7668ASN Pin Layout

## 5.2 Pin Description

The section describes the pin functionality of MT7668A chip.

QFN	Pin Name	Pin description	PU/PD	I/O	Supply domain

Reset and clocks						
60	TSTRST_B	External system reset active low, for testing	PU	Input	DVDDIO	
33	XO	Crystal input or external clock input	N/A	Input	AVDD22_XO	
34	AVDD22_XO	RF 2.2v power supply	N/A	Power		
32	XO_OUT	Clock monitor for PLL: debug purpose	N/A	Output		
UART						
73	UART_RXD	UART receive	PU/PD	Input	DVDDIO	
74	UART_TXD	UART transmit	PU/PD	Output	DVDDIO	
PCM						
68	PCM_CLK/GPIO	PCM interface clock	PU/PD	Output	DVDDIO	
71	PCM_IN/GPIO	PCM interface input data	PU/PD	In/out	DVDDIO	
72	PCM_OUT/GPIO	PCM interface output data	PU/PD	Output	DVDDIO	
67	PCM_SYNC/GPIO	PCM interface sync	PU/PD	In/out	DVDDIO	
ELNA TSSI						
66	PDET0/GPIO	External LNA TSSI input / GPIO	PU/PD	In/out	DVDDIO	
65	PDET1/GPIO	External LNA TSSI input / GPIO	PU/PD	In/out	DVDDIO	
Antenna Control						
41	ANT_SEL0/GPIO	RF switch control 0 / GPIO	N/A	Output	DVDDIO_ANTSEL	
30	ANT_SEL1/GPIO	RF switch control 1 / GPIO	N/A	Output	DVDDIO_ANTSEL	
40	ANT_SEL2/GPIO	RF switch control 2 / GPIO	N/A	Output	DVDDIO_ANTSEL	
39	ANT_SEL3/GPIO	RF switch control 3 / GPIO	N/A	Output	DVDDIO_ANTSEL	
36	ANT_SEL4/GPIO	RF switch control 4 / GPIO	N/A	Output	DVDDIO_ANTSEL	
35	ANT_SEL5/GPIO	RF switch control 5 / GPIO	N/A	Output	DVDDIO_ANTSEL	
WIFI radio interface						
43	AVDD33_WF0_A_PA	RF 3.3v power supply	N/A	Power		
48	AVDD33_WF0_G_PA	RF 3.3v power supply	N/A	Power		
50	AVDD33_WF1_A_PA	RF 3.3v power supply	N/A	Power		
54	AVDD33_WF1_G_PA	RF 3.3v power supply	N/A	Power		
42	AVDD33_WF0_A_TX	RF 3.3v power supply	N/A	Power		
49	AVDD33_WF1_A_TX	RF 3.3v power supply	N/A	Power		
37	AVDD22_WF0	RF 2.2v power supply	N/A	Power		
59	AVDD22_WF1	RF 2.2v power supply	N/A	Power		
38	AVDD13_WF0_TRX	RF 1.3v power supply	N/A	Power		
58	AVDD13_WF1_TRX	RF 1.3v power supply	N/A	Power		
31	AVDD13_WF0_AFE	RF 1.3v power supply	N/A	Power		
64	AVDD13_WF1_AFE	RF 1.3v power supply	N/A	Power		
44	WF0_A_RFIO	RF a-band RF port	N/A	In/out	AVDD33_WF0_A	

47	WF0_G_RFIO	RF g-band RF port	N/A	In/out	AVDD33_WF0_G
51	WF1_A_RFIO	RF a-band RF port	N/A	In/out	AVDD33_WF1_A
55	WF1_G_RFIO	RF g-band RF port	N/A	In/out	AVDD33_WF1_G
45	WF0_LNA_EXT_A	RF a-band RF port	N/A	In/out	AVDD33_WF0_A
46	WF0_LNA_EXT_G	RF g-band RF port	N/A	In/out	AVDD33_WF0_G
52	WF1_LNA_EXT_A	RF a-band RF port	N/A	In/out	AVDD33_WF1_A
53	WF1_LNA_EXT_G	RF g-band RF port	N/A	In/out	AVDD33_WF1_G
<b>Bluetooth radio interface</b>					
61	AVDD33_BT	RF 3.3v power supply	N/A	Power	
63	AVDD13_RXFE_BT	RF 1.35v power supply	N/A	Power	
62	RFIP_BT	Bluetooth RF port	N/A	In/out	AVDD33_BT
<b>PMU/BUCK</b>					
19	AVSS33_BUCK	BUCK ground	N/A	Ground	
18	LX	BUCK output	N/A	Output	
17	AVDD33_BUCK	BUCK power supply	N/A	Input	
16	AVDD25_V2P5NA	BUCK internal circuit output cap	N/A	Output	
20,21	AVDD13_CLDO	CLDO supply	N/A	Input	
26	AVDD33_MISC	PMU supply	N/A	Input	
22,23	CLDO	Core LDO output	N/A	Output	
27	ALDO	Analog LDO 2.2V output	N/A	Output	
25	PHYLDO	PHY LDO 1.8V output	N/A	Output	
24	VREF		N/A	Ground	
15	PMU_EN	PMU Enable	N/A	Input	
<b>Miscellaneous</b>					
56	OSC_EN/GPIO	OSC_EN: OSC enable in clock daisy chain	PU/PD	Output	DVDDIO
1	WIFI_INT_B/GPIO	WIFI_INT_B: WLAN host interrupt	PU/PD	Output	DVDDIO
76	BGF_INT_B/GPIO	BGF_INT_B: BT host interrupt	PU/PD	Output	DVDDIO
75	GPIO0	GPIO0 in/out	PU/PD	Output	DVDDIO
57	GPIO1	GPIO1 in/out	PU/PD	Output	DVDDIO
<b>IO power supplies</b>					
70	DVDDIO	Digital IO power input	N/A	Power	
28	DVDDIO_ANTSEL	Digital IO power input	N/A	Power	

**Table 19 MT7668A common pin descriptions**

USB3 interface					
4	AVDD18_SSUSB	USB 1.8V power supply	N/A	Power	

5	SSUSB_TXN	USB SS mode transmit differential pair	N/A	Analog	
6	SSUSB_TXP	USB SS mode transmit differential pair	N/A	Analog	
8	SSUSB_RXN	USB SS mode receive differential pair	N/A	Analog	
9	SSUSB_RXP	USB SS mode receive differential pair	N/A	Analog	
7	AVDD10_SSUSB	USB 1.0V power supply	N/A	Power	
<b>USB2 interface</b>					
13	AVDD33_USB	USB 3.3V power supply	N/A	Power	
12	USB_DM	USB D- signal	N/A	Analog	
11	USB_DP	USB D+ signal	N/A	Analog	
10	AVDD18_USB	USB 1.8V power supply	N/A	Power	
<b>Core power supplies</b>					
14, 29, 69	DVDD	Digital core power input	N/A	Power	

Table 20 MT7668AUN pin descriptions

<b>PCIE interface</b>					
4	AVDD18_PCIE	PCIe 1.8V power supply	N/A	Power	
5	PCIE_TXN	PCIe transmit differential pair	N/A	Analog	
6	PCIE_TXP	PCIe transmit differential pair	N/A	Analog	
8	PCIE_RXN	PCIe receive differential pair	N/A	Analog	
9	PCIE_RXP	PCIe receive differential pair	N/A	Analog	
7	AVDD10_PCIE	PCIe 1.8V power supply	N/A	Power	
2	PCIE_CKP	PCIe differential reference clock	N/A	Analog	
3	PCIE_CKN	PCIe differential reference clock	N/A	Analog	
<b>USB2 interface</b>					
13	AVDD33_USB	USB 3.3V power supply	N/A	Power	
12	USB_DM	USB D- signal	N/A	Analog	
11	USB_DP	USB D+ signal	N/A	Analog	
10	AVDD18_USB	USB 1.8V power supply	N/A	Power	
<b>Core power supplies</b>					
14, 29, 69	DVDD	Digital core power input	N/A	Power	

Table 21 MT7668AEN pin descriptions

<b>SDIO interface</b>					
9	SDIO_CLK	SDIO clock	N/A	Input	DVDDIO_SDIO
11	SDIO_CMD	SDIO command	N/A	In/Out	DVDDIO_SDIO
12	SDIO_DAT3	SDIO data bit 3	N/A	In/Out	DVDDIO_SDIO

10	SDIO_DAT2	SDIO data bit 2	N/A	In/Out	DVDDIO_SDIO
8	SDIO_DAT1	SDIO data bit 1	N/A	In/Out	DVDDIO_SDIO
7	SDIO_DAT0	SDIO data bit 0	N/A	In/Out	DVDDIO_SDIO
6	SDIO_DS	SDIO data strobe	N/A	Output	DVDDIO_SDIO
<b>SDIO and core power supplies</b>					
13	DVDDIO_SDIO	SDIO power input	N/A	Power	
14	DVDDIO_18I	SDIO 1.8V input	N/A	Power	
5, 29, 69	DVDD	Digital core power input	N/A	Power	

Table 22 MT7668ASN pin descriptions

## 5.3 Pin multiplexing

The pin multiplexing could be configured via control registers, and each pin can be configured individually. The default function of each pin is highlighted as bold font with blue background. The driving strength of all pins is programmable: 4mA, 8mA, 12mA, and 16mA. The default setting for all pins are 4mA.

		0		1		2		3	
Pin No.	Pin name	Function	Dir	Function	Dir	Function	Dir	Function	Dir
56	OSC_EN	OSC_EN	O	EXT_32K	I	BGF_INT_B	O	UART_DSN_TXD	O
76	BGF_INT_B	CLK_REQ_N	I/O	FRAME_SYNC	I	BGF_INT_B	O		
1	WIFI_INT_B	WAKE_N	I/O	EXT_INT_N	I	WIFI_INT_B	O		
73	UART_RXD	UART_RXD	I		I				
74	UART_TXD	UART_TXD	O		I/O				
68	PCM_CLK	N9_JTRST_B	I	EXT_INT_N	I	PCM_CLK	I/O	UART_CR4_DSN_TXD	O
67	PCM_SYNC	N9_JTMS	I		I	PCM_SYNC	I/O	UART_DSN_TXD	O
72	PCM_OUT	N9_JTDO	O		I	PCM_OUT	O	CR4_JTMS	I/O
71	PCM_IN	N9_JTDI	I		I/O	PCM_IN	I	CR4_JTCK	I
75	GPIO0	PERST_N	I	CR4_JTDO	O	FRAME_SYNC	I	EXT_32K	I
41	ANTSEL0	BGF_INT_B	O	LED0	I/O	UART_CTS	I	UART_TXD	O
30	ANTSEL1	WIFI_INT_B	O			UART_RTS	O	UART_RXD	I
40	ANTSEL2	UART_CR4_DSN_TXD	O			LED0	I/O		O
39	ANTSEL3	CR4_JTMS	I/O				O		I
36	ANTSEL4	CR4_JTCK	I			UART_CTS	I		O
35	ANTSEL5	UART_DSN_TXD	O		O	UART_RTS	O		I
66	PDET0	N9_JTCK	I	CR4_JTMS	I/O	BT_LED_B	I/O	LED1	I/O
65	PDET1	N9_DBGIN	I	EXT_INT_N	I	WIFI_INT_B	O		I/O
57	GPIO1	N9_DBGACKN	O	UART_DSN_TXD	O	FRAME_SYNC	I		O

		4		5		6		7 (reserved)		8	
Pin No.	Pin name	Function	Dir	Function	Dir	Function	Dir	Function	Dir	Function	Dir

56	OSC_EN	ANTSEL[10]	O		O	CR4_JTDO	O			GPIO[0]	I/O
76	BGF_INT_B			UART_CTS	I		O			GPIO[1]	I/O
1	WIFI_INT_B	ALL_INT_B	O	UART_RTS	O	UART_CTS	I			GPIO[2]	I/O
73	UART_RXD				I					GPIO[3]	I/O
74	UART_TXD				O	CR4_JTMS	I/O			GPIO[4]	I/O
68	PCM_CLK	ANTSEL[6]	O			CR4_JTCK	I			GPIO[5]	I/O
67	PCM_SYNC	ANTSEL[7]	O			CR4_JTRST_B	I			GPIO[6]	I/O
72	PCM_OUT	ANTSEL[8]	O	LED1	I/O	WIFI_INT_B	O			GPIO[7]	I/O
71	PCM_IN	ANTSEL[9]	O	LED2	I/O	CR4_JTDI	I			GPIO[8]	I/O
75	GPIO0	LED0	I/O	N9_JTCK	I	UART_CR4_DSN_TXD	O			GPIO[9]	I/O
41	ANTSEL0	ANTSEL[0]	O	EXT_32K	I					GPIO[10]	I/O
30	ANTSEL1	ANTSEL[1]	O	UART_TX	O					GPIO[11]	I/O
40	ANTSEL2	ANTSEL[2]	O	N9_JTRST_B	I		O			GPIO[12]	I/O
39	ANTSEL3	ANTSEL[3]	O	N9_JTMS	I		O			GPIO[13]	I/O
36	ANTSEL4	ANTSEL[4]	O	N9_JTDO	O		O			GPIO[14]	I/O
35	ANTSEL5	ANTSEL[5]	O	N9_JTDI	I		O			GPIO[15]	I/O
66	PDET0	PDET0	I	UART_RX	I		O			GPIO[16]	I/O
65	PDET1	PDET1	I	UART_TX	O		O			GPIO[17]	I/O
57	GPIO1	BT_LED_B	I/O	UART_RX	I		O			GPIO[18]	I/O

Table 23 Pin multiplexing

## 5.4 Bootstrap

The section describes the bootstrap function. The chip modes are sensed from the device pin during power up. After chip reset, the pull configuration are stored in a register and determine the device operation mode.

XTAL clock mode	ANTSEL1	ANTSEL0	Description	Feasibility
26MHz	Pull-up	Pull-down	Uses 26MHz XTAL.	MT7668ASN
40MHz	Pull-down <sup>(1)</sup>	Pull-up <sup>(2)</sup>	Uses 40MHz XTAL.	MT7668ASN, MT7668AUN, MT7668AEN
52MHz	Pull-up	Pull-up	Uses 52MHz XTAL.	MT7668ASN

Note 1: No external pull-down resistor is required because internal pull-down is active during power up.

Note 2: No external pull-up resistor is required because internal pull-up is active during power up.

Table 24 Bootstrap option – XTAL clock mode

BT Host mode	UART_TXD	Description
USB	Pull-down <sup>(1)</sup>	Use USB or SDIO as the host interface for Bluetooth
UART	Pull-up	Use UART as the host interface for Bluetooth

Note 1: No external pull-down resistor is required because internal pull-down is active during power up.

Table 25 Bootstrap option – BT host mode

USB3 mode	ANTSEL2	Description
Normal Super Speed mode	Pull-down <sup>(1)</sup>	USB3 is configured at 5GHz bit rate
Half Super Speed mode	Pull-up	USB3 is configured at 2.5GHz bit rate

Note 1: No external pull-down resistor is required because internal pull-down is active during power up.

**Table 26 Bootstrap option – USB3 mode**

Chip mode	PCM_OUT	Description
Normal mode	Pull-down <sup>(1)</sup>	Chip operates in normal mode.
Test mode	Pull-up	Chip operates in test mode.

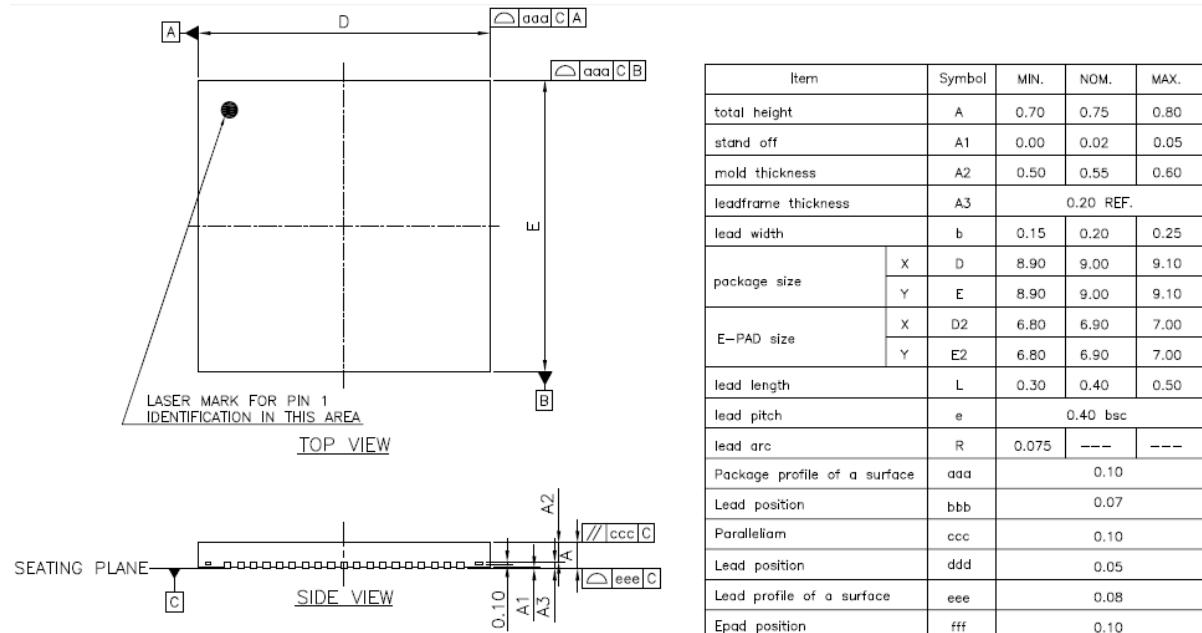
Note 1: No external pull-down resistor is required because internal pull-down is active during power up.

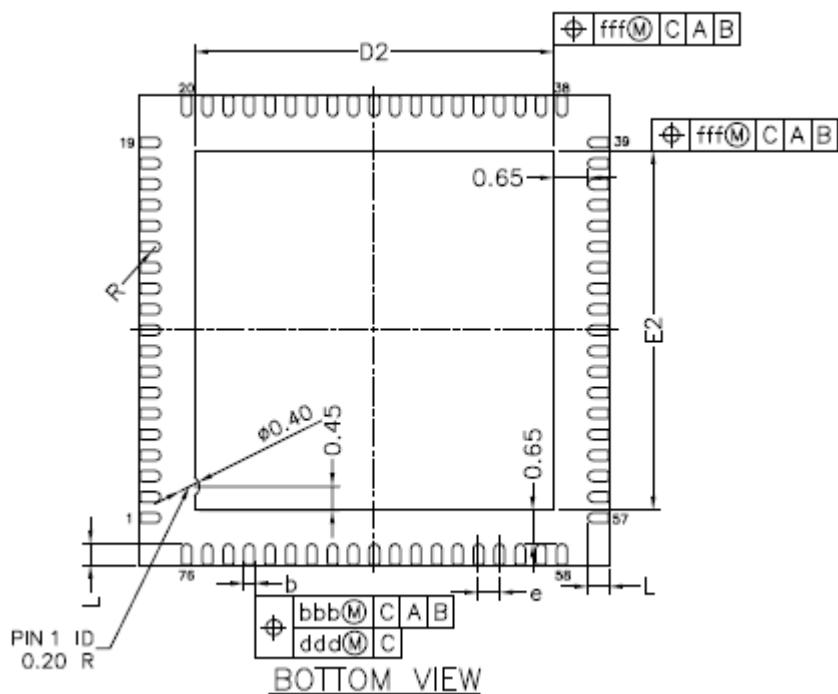
**Table 27 Bootstrap option – Chip mode**

Pins PCM\_OUT, UART\_TXD, ANTSEL2, ANTSEL1 and ANTSEL0 are used for bootstrap. The system design should follow the following guideline:

- Those pins shall not be used as input functions because the signals from other device might affect the values sensed.
- Those pins shall not be used as an open-drain function because the pull-up resistor would affect the values sensed.

## 5.5 Package information





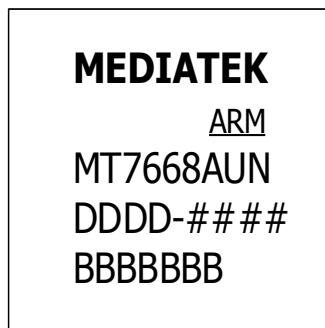
**Figure 14 Package outline drawing**

## 5.6 Ordering Information

Part number	Package	Operational temperature range
MT7668AUN	9x9x0.8 mm 76-QFN	-10~70°C
MT7668AEN	9x9x0.8 mm 76-QFN	-10~70°C
MT7668ASN	9x9x0.8 mm 76-QFN	-10~70°C

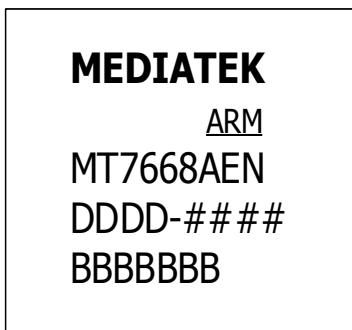
**Table 28 Ordering information**

## 5.7 Top marking



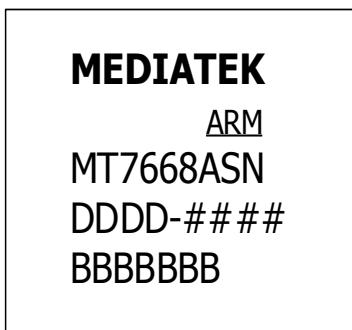
MT7668AUN : Part number  
 DDDD : Date code  
 ##### : Internal control code  
 BBBBBBB : Lot number

**Figure 15 MT7668AUN Top Marking**



MT7668AEN : Part number  
DDDD : Date code  
#### : Internal control code  
BBBBBBB : Lot number

Figure 16 MT7668AEN Top Marking



MT7668ASN : Part number  
DDDD : Date code  
#### : Internal control code  
BBBBBBB : Lot number

Figure 17 MT7668ASN Top Marking



#### ESD CAUTION

MT7668A is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7668A is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.