RTL8852AE-VR-CG

SINGLE-CHIP 802.11ax/ac/a/b/g/n 2T2R WLAN AND INTEGRATED BLUETOOTH 5 CONTROLLER WITH PCI EXPRESS /HS-UART MIXED INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.1	2020/01/10	Preliminary release.
0.2	2020/02/13	Modify PIN Assign and timing SPEC
0.3	2020/02/18	remove PCM interface
0.4	2020/03/15	Correct Part Number

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1. General Description

The Realtek RTL8852AE-VR-CG is a highly integrated single-chip that support 2-stream 802.11ax solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with Wireless LAN (WLAN) PCI Express network interface controller and HS-UART mixed interface . It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in a single chip. The RTL8852AE-VR-CG provides a complete solution for a high-performance integrated wireless and Bluetooth device.

The RTL8852AE-VR-CG baseband implements Multi-user Multiple Input, Multiple Output (MU-MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8852AE-VR-CG provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8852AE-VR-CG also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 1201Mbps for IEEE 802.11ax MIMO OFDM.

The RTL8852AE-VR-CG builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths, and Maximum-Likelihood Detection (MLD) are implemented. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8852AE-VR-CG supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8852AE-VR-CG MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac/802.11ax for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8852AE-VR-CG provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 76-pin QFN
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- Support 802.11ac/ax 2x2,Wave-2 compliant with MU-MIMO
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Maximum PHY data rate up to 286.8 Mbps using 20MHz bandwidth, 573.5Mbps using 40MHz bandwidth, and 1201Mbps using 80MHz bandwidth
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n/ac devices while operating at 802.11ax data rates

Host Interface

- Complies with PCI Express Base Specification Revision 2.1
- PCIe LTR/L1.Off state supported.
- Complies with HS-UART with configurable baud rate for Bluetooth

Standards Supported

- IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- MU/RU/SU decision path by firmware
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Support TWT function for power saving.
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8852AE-VR-CG to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications.Support BSR and queue size of Qos.
- Support MU EDCA feature.
- Support DFS, Channelinfo, PPDU state by Rx path.

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- Support S3/S4 AES/TKIP group key update
- Support Dual band concurrent.(2.4G/5G)
- FTM support distance measurement
- Support Network List Offload
- CCA on secondary through RTS/CTS handshake
- Support TCP/UDP/IP checksum offload

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins
- Two configurable LED pins
- Crystal frequency support 40MHz
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only

PHY Features

- IEEE 802.11ax MIMO OFDM
- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths

- 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7Mbps in 802.11ac, 1201Mbps in 802.11ax.
- OFDM/DSSS receive diversity with MRC using up to 2 receive paths. Switch diversity used for CCK
- Support STBC
- Support LDPC
- Hardware antenna diversity
- Maximum-Likelihood Detection (MLD)
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Controller

- Support Bluetooth 5 system (BT 5.2 Logo Compliant)
- Compatible with Bluetooth v2.1+EDR
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports Secure Simple Pairing
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

3. Application Diagrams

3.1. 11ax Dual-Band 2x2 RF Application

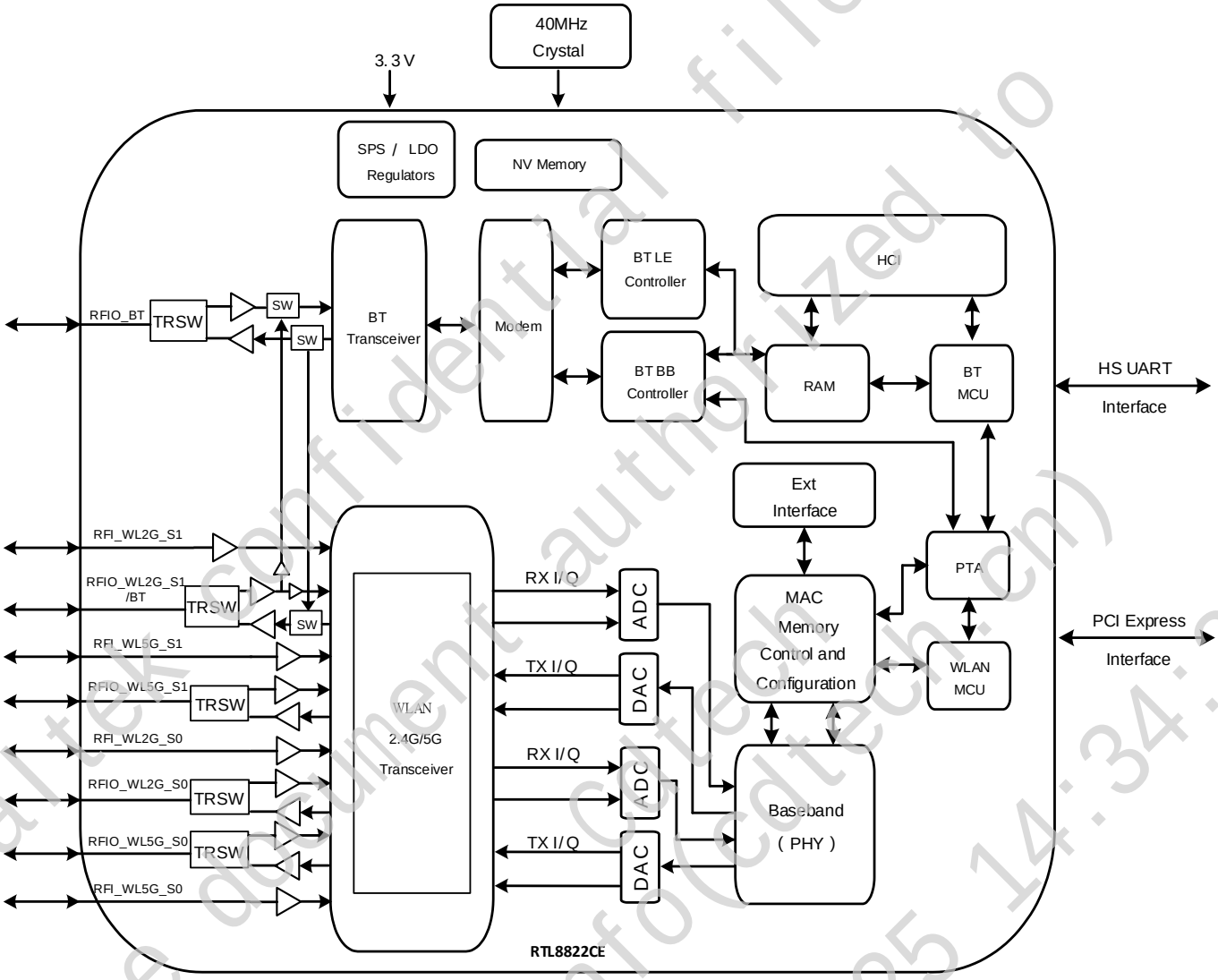


Figure 1. Dual-Band MIMO 2x2 Solution(11ax 2x2 MAC/BB/RF + PA) and Integrated Bluetooth Controller Solution -- RTL8852AE-VR-CG

4. Pin Assignments

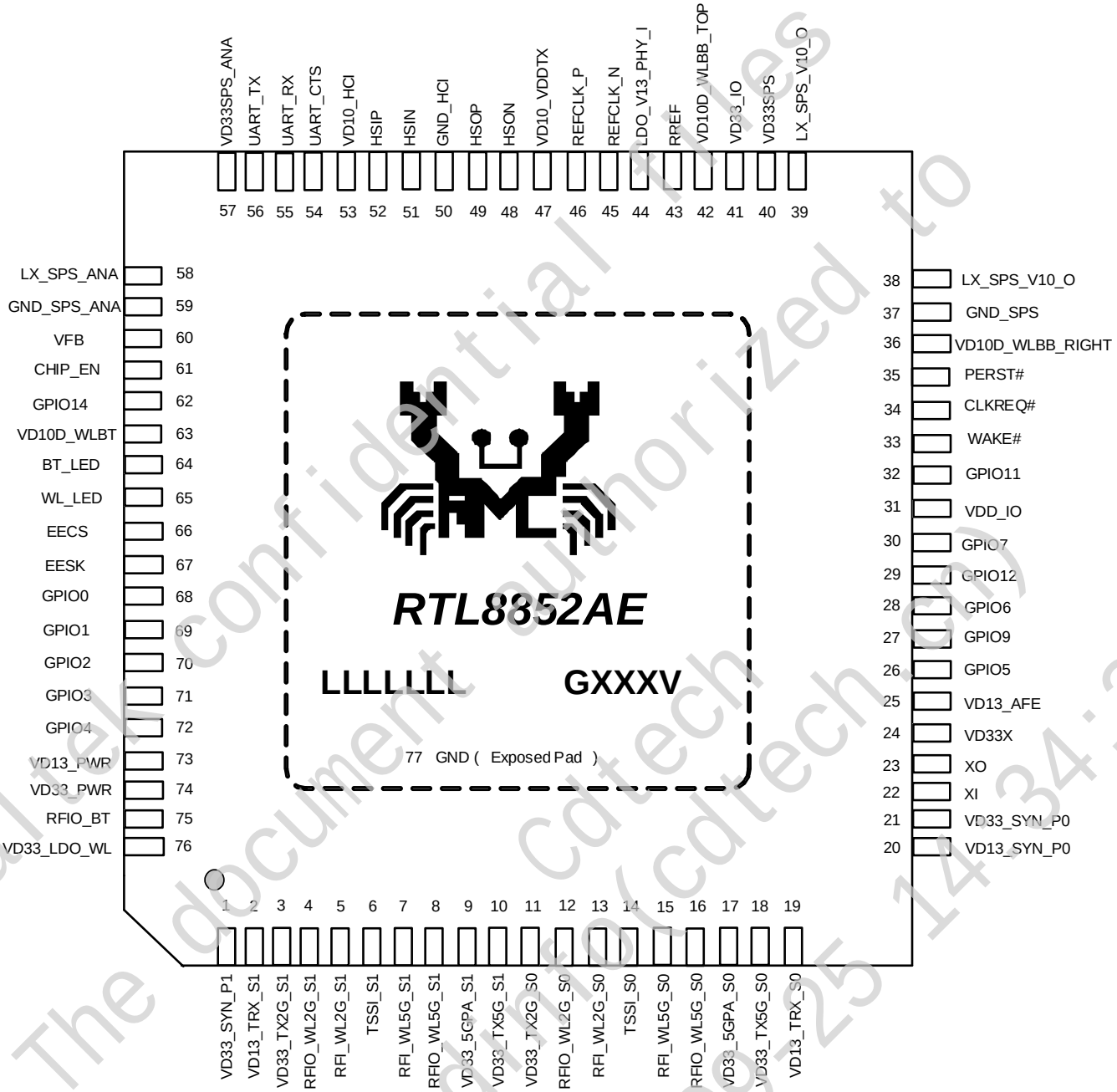


Figure 2. Pin Assignments

4.1. Package Identification & Mark Information

Green package is indicated by a ‘G’ in GXXX (Figure 2).
The version is shown in the location marked ‘V’.

5. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin
N/A:	No Bonding pin		

5.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Pin No.	Description
TEST_MODE_SEL	I	72	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode

5.2. PCI Express Transceiver Interface

Table 2. PCI Express Transceiver Interface

Symbol	Type	Pin No.	Description	Voltage
HSIN/HSIP	I	51,52	PCI Express Receive Differential Pair	
HSON/HSOP	O	48,49	PCI Express Transmit Differential Pair	
REFCLK_N/REFCLK_P	I	45,46	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm	
CLKREQ#	I/O/D	34	Reference Clock Request Signal.Also used by L1 PM substates. This signal is used by the RTL8852AE-VR-CG to request for the PCI Express reference clock.	3.3V
WAKE#	O/D	33	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks. This WAKE# can be shared with BT wake up host function via sideband signals.	3.3V
PERST#	I	35	PCI Express Reset Signal: active low. When the PERST# is asserted at power-on state, the RTL8852AE-VR-CG returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERST#.	3.3V

5.3. HS-UART Transceiver Interface

Table 3. HS-UART Transceiver Interface

Symbol	Type	Pin No..	Description
UART_CTS	I	54	High-Speed UART CTS
UART_RX	I	55	High-Speed UART Data In
UART_TX	O	56	High-Speed UART Data Out

5.4. RF Interface

Table 4. RF Interface

Symbol	Type	Pin No.	Description
RFIO_BT	I/O	76	BT RF input/output.
RFIO_WL2G_S1	I/O O	4	(1) RF input/output of path S1 WLAN 2G (2) Or RF output of path S1 WLAN 2G in external PA/FEM configuration
RFI_WL2G_S1	I	5	WLAN 2G RF input for path S1 in external LNA/FEM configuration
TSSI_S1	I	6	TSSI input from external PA/FEM
RFI_WL5G_S1	I	7	WLAN 5G RF input for path S1 in external LNA/FEM configuration
RFIO_WL5G_S1	I/O O	8	(1) WLAN 5G RF input/output for path S1 (2) Or WLAN 5G RF output for path S1 in external PA/FEM configuration
RFIO_WL2G_S0	I/O O	12	(1) RF input/output of path S0 WLAN 2G (2) Or RF output of path S0 WLAN 2G in external PA/FEM configuration
RFI_WL2G_S0	I	13	WLAN 2G RF input for path S0 in external LNA/FEM configuration
TSSI_S0	I	14	TSSI input from external PA/FEM
RFI_WL5G_S0	I	15	WLAN 5G RF input for path S0 in external LNA/FEM configuration
RFIO_WL5G_S0	I/O	16	(1) WLAN 5G RF input/output for path S0 (2) Or WLAN 5G RF output for path S0 in external PA/FEM configuration

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No.	Description
BT_LED	O	64	BT LED Pin (Active Low)
WL_LED	O	65	WL LED Pin (Active Low), shared with GPIO8

5.6. Power Management Handshake Interface

Table 6. Power Management Handshake Interface

Symbol	Type	Pin No.	Description
WL_DIS#	I	27	Shared with GPIO9.This pin can be defined as the WLAN Radio-off function with host interface remaining connected. When this pin is pulled low, WLAN function will be Radio-off. When this function is not required, external pull high is not required.
BT_DIS#	I	32	Shared with GPIO11. This pin can externally shut down the RTL8852AE-VR-CG BT function when BT_DIS# is pulled Low. When this pin is pulled low, UART interface will be also disabled. When this function is not required, external pull high is not required.
HOST_WAKE_WL	O	29	Shared with GPIO12. The Host wakes up the WLAN controller in Remote Wakeup Mode.
CHIP_EN	I	61	This Pin Can externally shut down the RTL8852AE-VR-CG (No Extra Power Switch Required). When this function is not required, external pull high is required.

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No.	Description
XI	I	22	40MHz OSC Input 40MHz crystal reference clock input
XO	O	23	40MHz Crystal reference clock output
SUS_CLK	I	66	External 32K or RTC clock input.
EESK	I	67	WLAN eFuse autoload
GPIO0	I/O	68	General Purpose Input/ Output Pin
GPIO1	I/O	69	General Purpose Input/ Output Pin
GPIO2	I/O	70	General Purpose Input/ Output Pin
GPIO3	I/O	71	General Purpose Input/ Output Pin
GPIO4	I/O	72	General Purpose Input/ Output Pin
GPIO5	I/O	26	General Purpose Input/ Output Pin
GPIO6	I/O	28	General Purpose Input/ Output Pin
GPIO7	I/O	30	General Purpose Input/ Output Pin
GPIO8	I/O	65	General Purpose Input/ Output Pin
GPIO9	I/O	27	General Purpose Input/ Output Pin
GPIO11	I/O	32	General Purpose Input/ Output Pin
GPIO12	I/O	29	General Purpose Input/ Output Pin
GPIO14	I/O	62	General Purpose Input/ Output Pin

5.8. HCI Power Pins

Table 8. HCI Power Pins

Symbol	Type	Pin No	Description
LDO_V13_PHY_I	P	44	LDO 1.3V PHY Input
GND_HCI	P	50	Ground for host interface
RREF	P	43	Precision Resistor for Bandgap
VD10_VDDTX	P/I	47	1.05V for analog circuits in interface
VD10_HCI	P	53	1.05V for HCI

5.9. Digital Power Pins

Table 9. Digital Power Pins

Symbol	Type	Pin No.	Description
VD33_IO	P	41	VDD3.3V for Digital IO (PERST#, WAKE#, CLKREQ#,WL_LED,BT_LED)
VDD_IO	P	31	VDD for GPIO[0:14] , SUS_CLK , EESK
VD10D_WLBB_TOP / VD10D_WLBB_RIGHT	P	42,36	1.05V for WLAN BB digital power
VD10D_WLBT	P	63	1.05V for WLAN and BT digital power

5.10. REGU Power Pins

Table 10. REGU Power Pins

Symbol	Type	Pin No.	Description
LX_SPS_V10_O	P	38,39	Digital Switching Regulator 1.05V Output
VD33_SPS	P	40	Digital Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
GND_SPS	P	37	Digital Switching Regulator Ground
LX_SPS_ANA	P	58	Analog Switching Regulator 1.3V Output
VD33_SPS_ANA	P	57	Analog Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
GND_SPS_ANA	P	59	Analog Switching Regulator Ground
VFB	P	60	Analog Switching Regulator Feedback

5.11. RF Power Pins

Table 11. RF Power Pins

Symbol	Type	Pin No.	Description
VD13_PWR	P	73	VDD 1.3V for RF
VD33_PWR	P	74	VDD 3.3V for RF
VD33_LDO_WL	P	76	VDD 3.3V for internal LDO input
VD33_SYN_P1	P	1	VDD 3.3V for synthesizer P1
VD13_TRX_S1	P	2	VDD 1.3V for S1 WLAN RF
VD33_TX2G_S1	P	3	VDD 3.3V for S1 2G WLAN PA
VD33_5GPA_S1	P	9	VDD 3.3V for S1 5G WLAN PA
VD33_TX5G_S1	P	10	VDD 3.3V for S1 5G WLAN PAD
VD33_TX2G_S0	P	11	VDD 3.3V for S0 2G WLAN PA
VD33_5GPA_S0	P	17	VDD 3.3V for S0 5G WLAN PA
VD33_TX5G_S0	P	18	VDD 3.3V for S0 5G WLAN PAD
VD13_TRX_S0	P	19	VDD 1.3V for S0 WLAN RF
VD13_SYN_P0	P	20	VDD 1.3V for WLAN synthesizer P0
VD33_SYN_P0	P	21	VDD 3.3V for WLAN synthesizer P0
VD33X	P	24	VDD 3.3V for crystal
VD13_AFE	P	25	VDD 1.3V for WLAN AFE

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 12. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 13. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD10	1.05V Core Supply Voltage	0.945	1.05	1.155	V
VD13	1.3V Analog Supply Voltage	1.17	1.3	1.43	V

6.2.2. Digital IO Pin DC Characteristics

Table 14. 3.3V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 15. 1.8V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	3.6	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

7. Interface Timing Specification

7.1. PCIe Bus during Power On Sequence

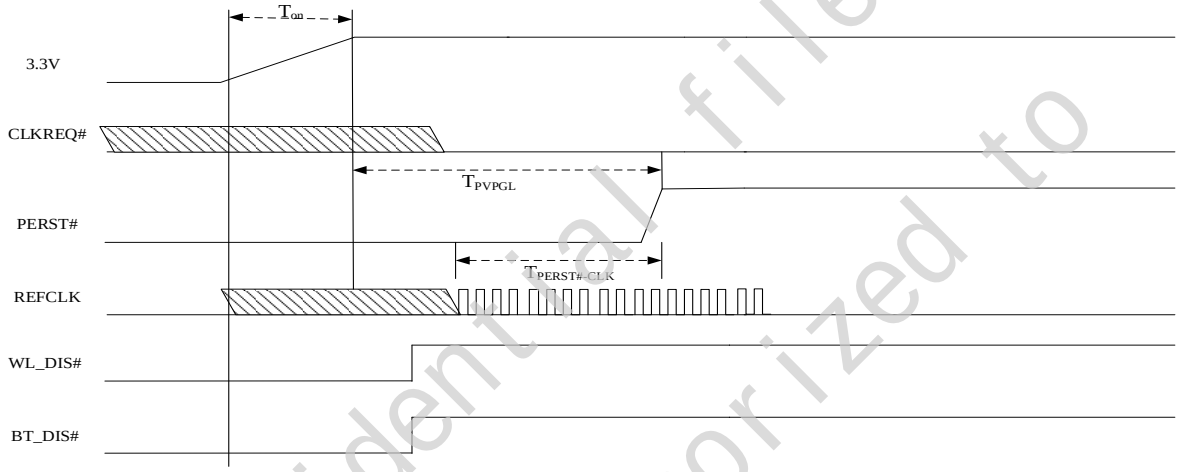


Figure 3. RTL8852AE-VR-CG PCIe Power On Sequence

Ton: The main power ramp up duration

TPVPGL: Power valid to PERST# input inactive

TPERST#-CLK: Reference clock stable before PERST# inactive

Symbol	Unit	Min	Typical	Max
Ton	ms	0.5	1.5	5
TPVPGL	ms	Implementation specific;recommended 50ms	--	--
TPERST#-CLK	us	100	--	--

Table 16. The typical timing range

7.2. PCIe PERST# Timing Sequence (if need at least twice)

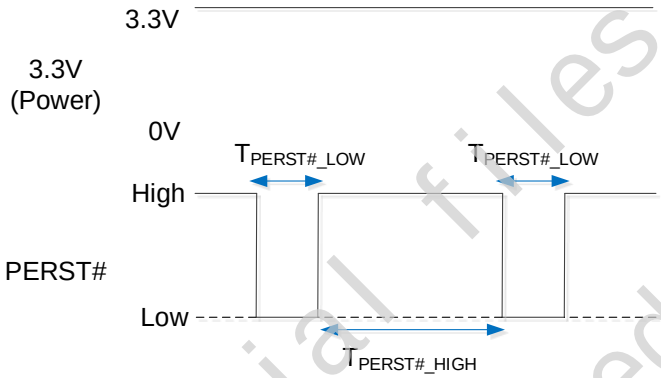


Table 17. RTL8852AE-VR-CG PCIE PERST# Timing Parameters

	Min	Typical	Max	Unit	Description
TPERST#_LOW	6	10	X	ms	PERST# low duration
TPERST#_HIGH	400	500	X	ms	PERST# high duration

7.3. Power Off Sequence

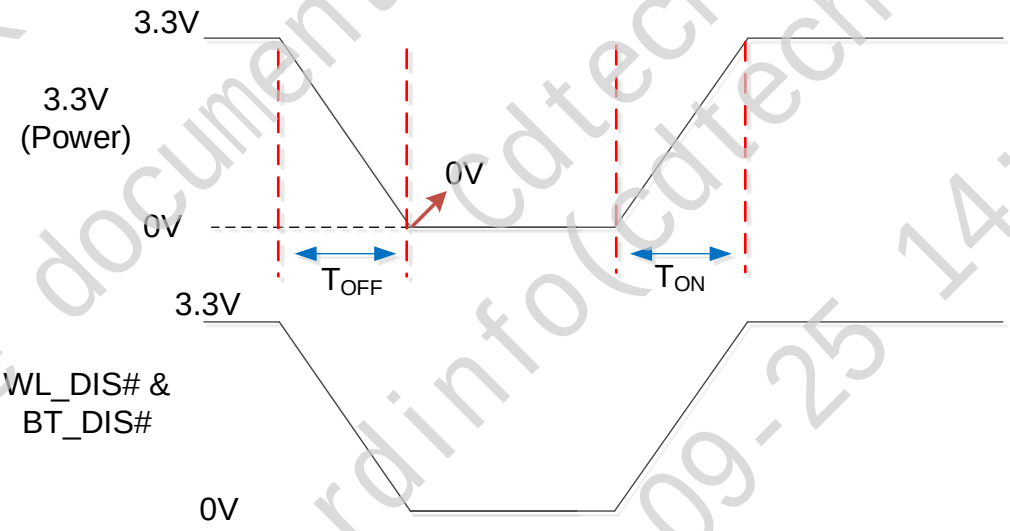


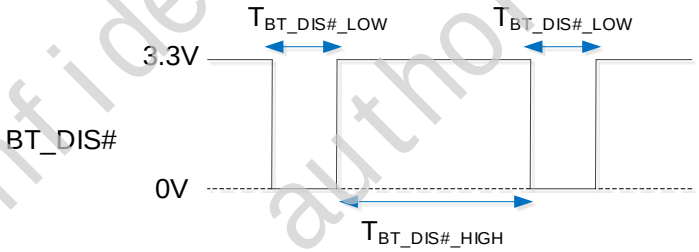
Figure 3. RTL8852AE-VR-CG Power Off Sequence of 3.3V platform

Table 18. RTL8852AE-VR-CG Power Off Timing Parameters

Symbol	Min.	Typical	Max.	Unit	Description
T_{OFF}	5	--	--	ms	Measure point start on 100% Measure point end on 0% (must be 0V)
T_{ON}	0.5	1.5	5	ms	Measure point start on 0% (must be 0V) Measure point end on 100%

Note: If BT_DIS# can't connect to the same power source with 3.3V, it need to be de-asserted before PERST# with 100ms in power on sequence.

7.4. BT_DIS Timing Sequqnece



	Min.	Typical	Max.	Unit	Description
BT_DIS#_LOW	200	--	--	ms	BT_DIS# low duration
BT_DIS#_HIGH	500	--	--	ms	BT_DIS# high duration

7.5. Interface Characteristics

The RTL8852AE-VR-CG UART interface is a 3-wire interface with RX, TX, CTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2 k baud. In order to support high and low speed baud rate, the RTL8852AE-VR-CG provides multiple UART clocks.

Table 19. UART Interface Power-On Timing Parameters

Parameter	Condition	Min.	Typical	Max.	Unit
Baud Rate error rate	Per byte (including start/stop bit)	-1.3		1.3	%

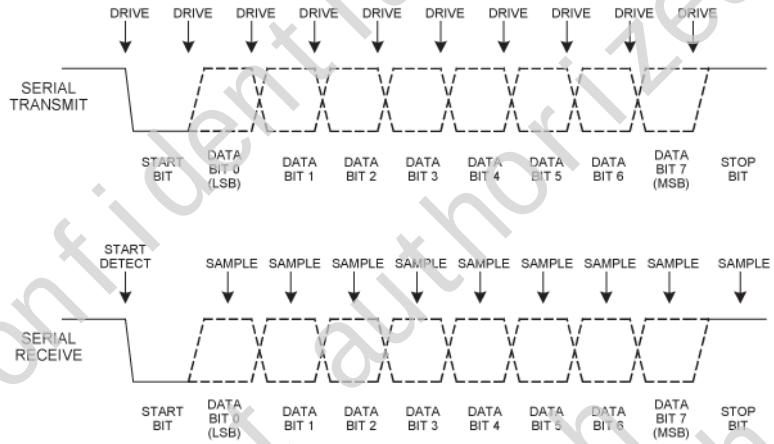


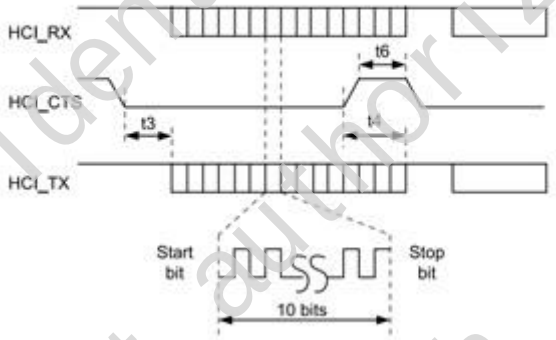
Figure 4. UART Interface Waveform

7.5.1. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8852AE-VR-CG UART interface via the VIO_HOST pin (Pin 43).

7.5.2. UART Interface Timing

The interface includes four signals, TXD/RXD/CTS. Flow control between the host and the device is byte-wise by hardware.When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.



UART Timing Diagram

UART Timing Characteristics

Parameter	Condition	Symbol	Min.	Typ	Max.	Unit
Baud rate			115.2		3000	Kbps
Baud rate accuracy per	Receive/Transmit		-3		3	%
CTS low to TX_DATA on		T3	0	2		ns
CTS high to TX_DATA off	Hardware flow	T4			1	byte
CTS High Pulse Width		T6	1			bit

* Note : HCI packet means HCI command(256 bytes), HCI event(256 bytes), ACL(1024 bytes), SCO(256 bytes)

7.5.3. UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

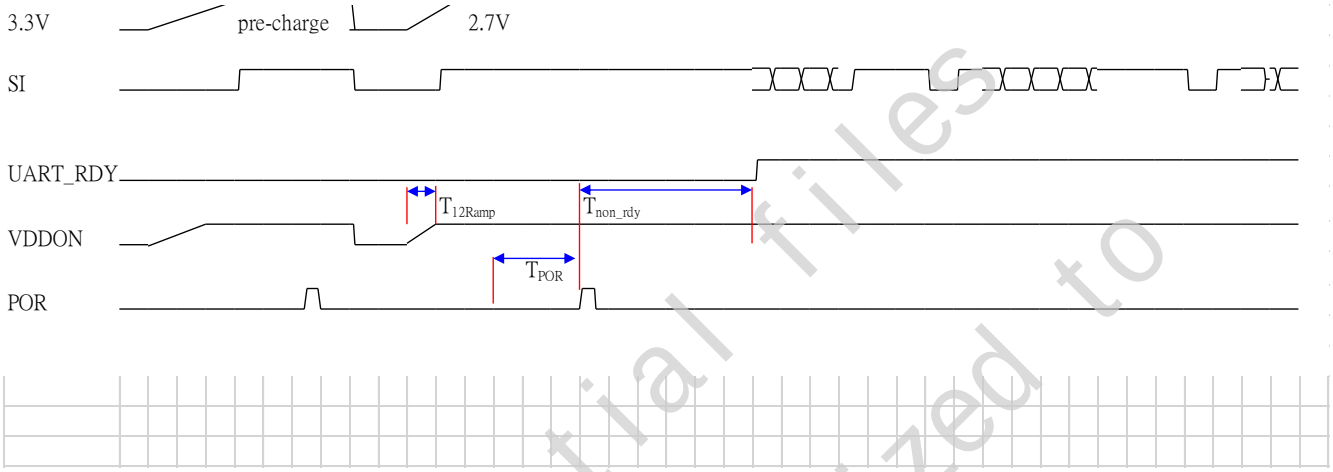


Figure 5. UART Power-On Sequence Without Hardware Flow Control

UART Hardware Flow Control Supported

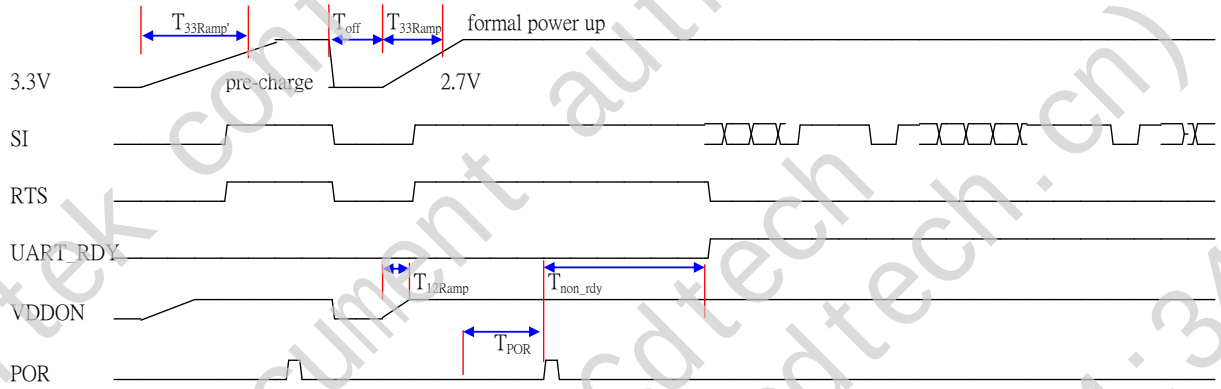


Figure 6. UART Power On Sequence With Hardware Flow Control

Table 20. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8852AE-VR-CG will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

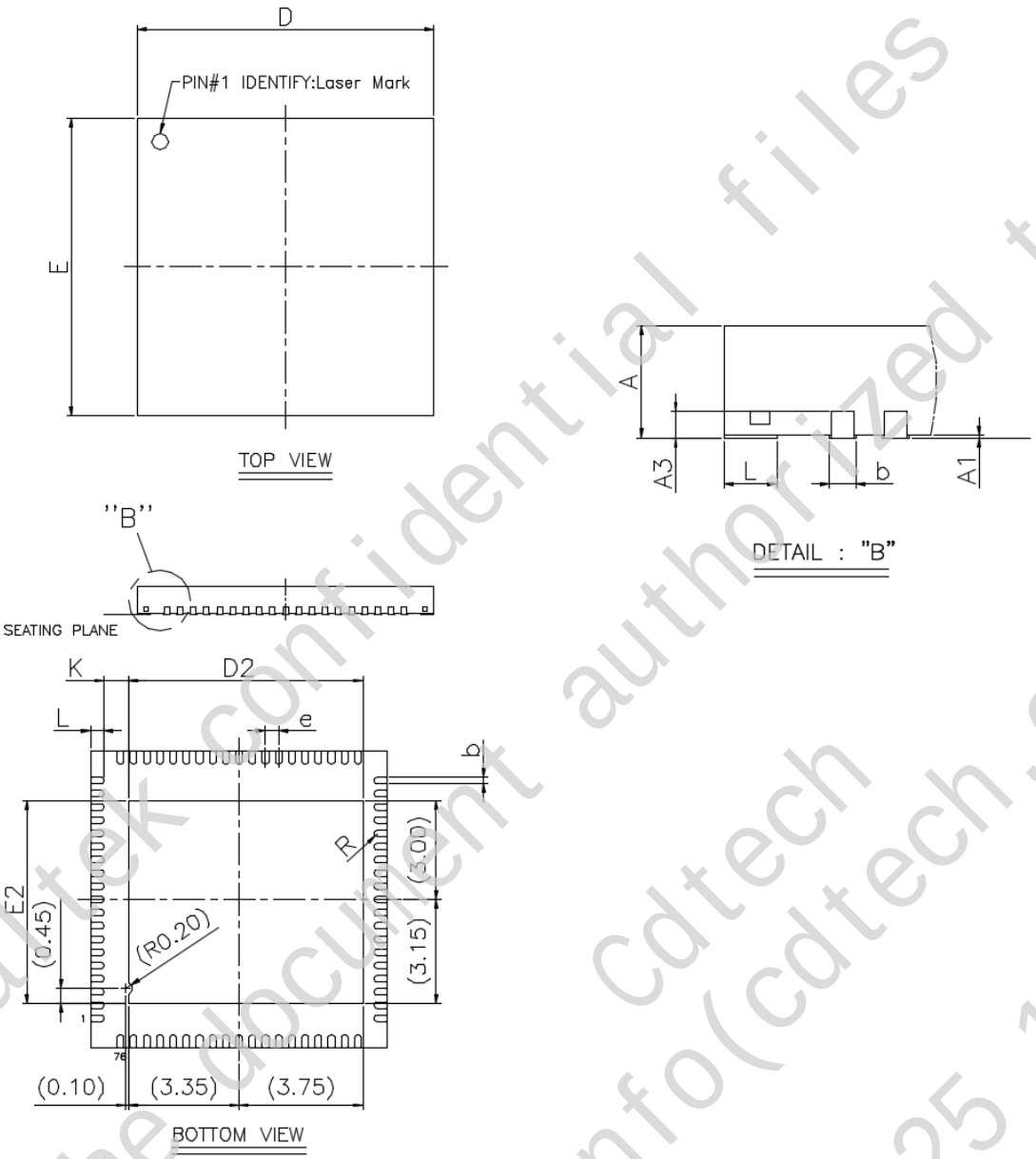
During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits included the UART.

Table 21. UART Interface Power On Timing Parameters

	Min.	Typical	Max.	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non-rdy}$	1	2	10	ms

8. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.2 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	8.90	9.00	9.10	0.350	0.354	0.358
D_2	7.00	7.10	7.20	0.276	0.280	0.283
E_2	6.05	6.15	6.25	0.238	0.242	0.246
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

9. Ordering Information

Table 22. Ordering Information

Part Number	Package	Status
RTL8852AE-VR-CG	QNF76 , 'Green' Package	To be available

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com