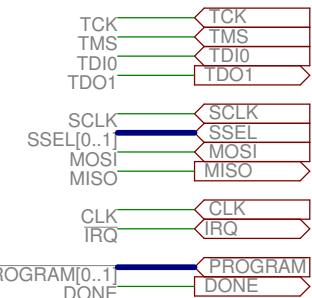
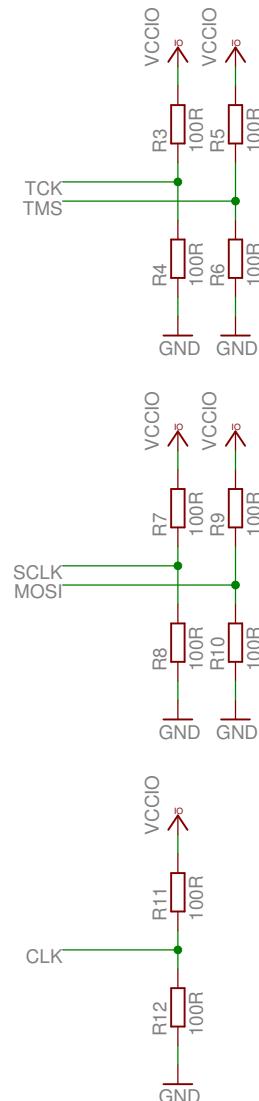


TP1	VCCINT
TP2	VCCIO
TP3	GND
TP4	NC
TP5	TCK
TP6	TMS
TP7	TDI0
TP8	TDO1
TP9	SCLK
TP10	SSEL0
TP11	SSEL1
TP12	MOSI
TP13	MISO
TP14	CLK
TP15	IRQ
TP16	PROGRAM0
TP17	PROGRAM1
TP18	DONE



## Bus Termination

TITLE: FPGA\_pin\_demo

Document Number:

REV:

0

Date: 22.07.11 14:35

Sheet: 5/5

