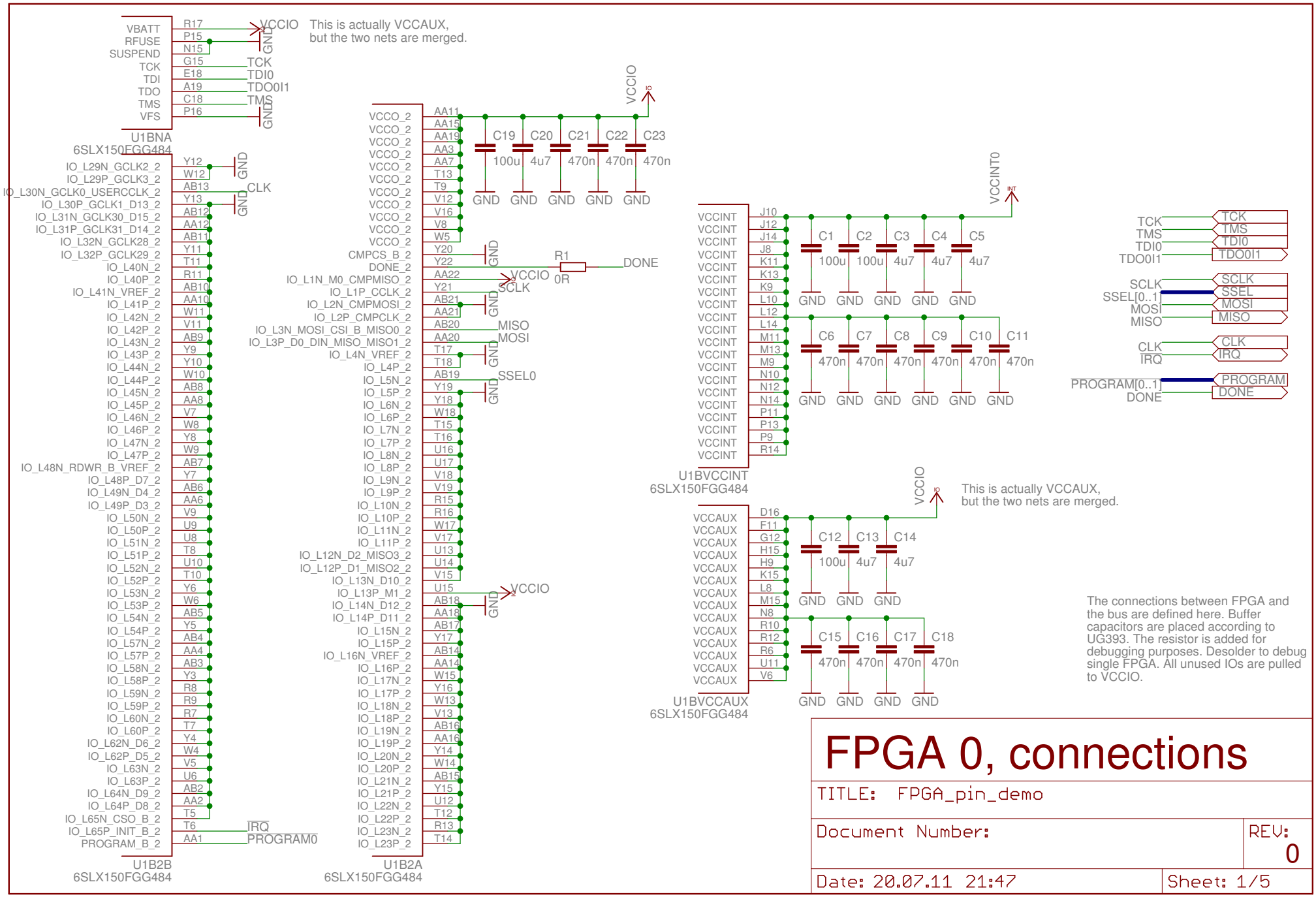
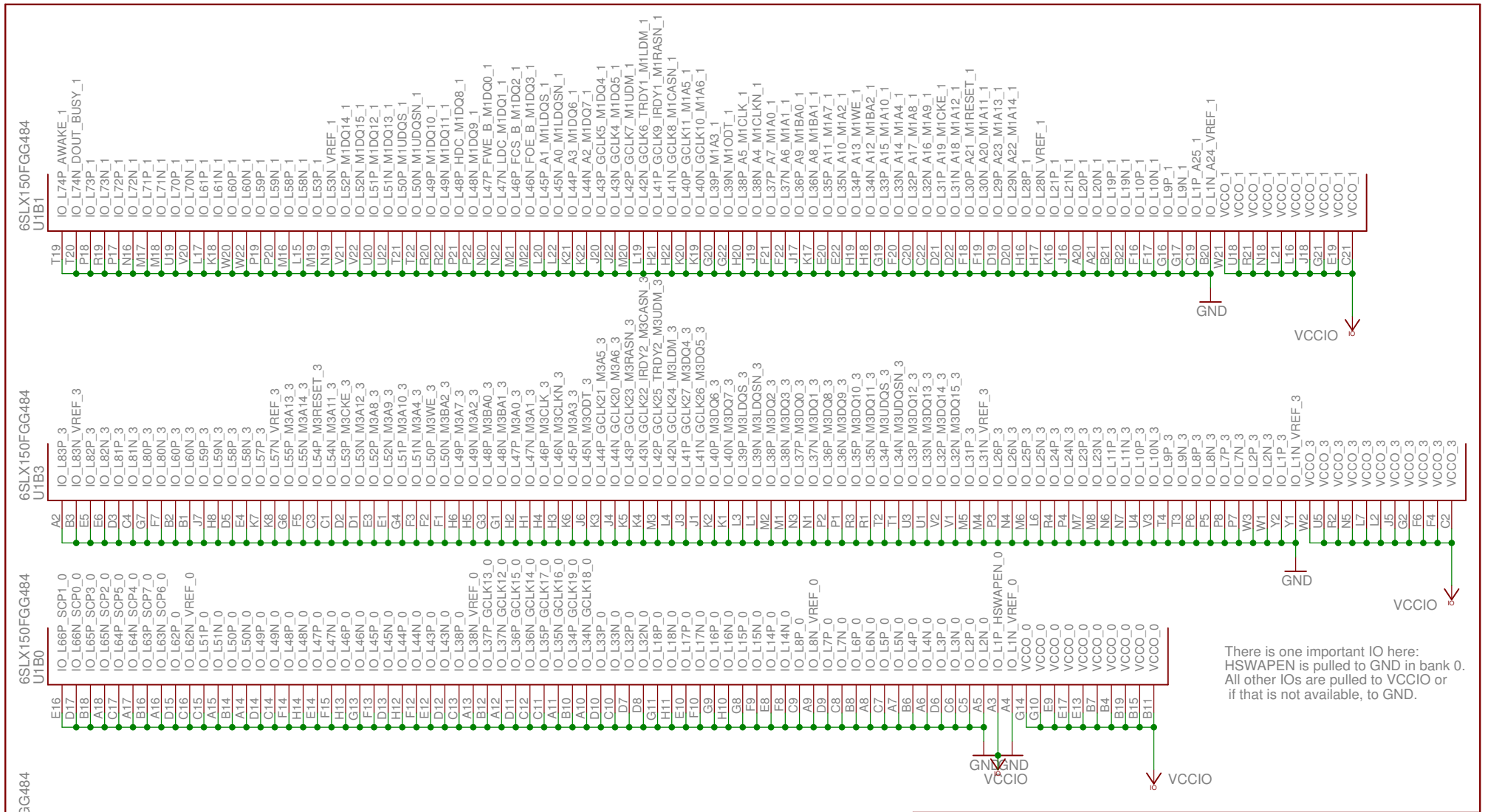

This is actually VCCAUX, but the two nets are merged.
U1BNA
6SLX150FGG484
U1B2B
6SLX150FGG484
U1B2A
6SLX150FGG484
U1BVCCINT
6SLX150FGG484
U1BVCCAUX
6SLX150FGG484
VCCIO
VCCINT0
GND
TCK
TDI0
TDO0I1
TMS
CLK
IRQ
PROGRAM0
DONE
SCLK
MISO
MOSI
SSEL0
SSEL[0..1]
PROGRAM[0..1]
PROGRAM
C19 100u
C20 4u7
C21 470n
C22 470n
C23 470n
R1 0R
C1 100u
C2 100u
C3 4u7
C4 4u7
C5 4u7
C6 470n
C7 470n
C8 470n
C9 470n
C10 470n
C11 470n
C12 100u
C13 4u7
C14 4u7
C15 470n
C16 470n
C17 470n
C18 470n
The connections between FPGA and the bus are defined here. Buffer capacitors are placed according to UG393. The resistor is added for debugging purposes. Desolder to debug single FPGA. All unused IOs are pulled to VCCIO.
FPGA 0, connections
TITLE: FPGA_pin_demo
Document Number:
REV: 0
Date: 20.07.11 21:47
Sheet: 1/5



FPGA 0, empty IOs

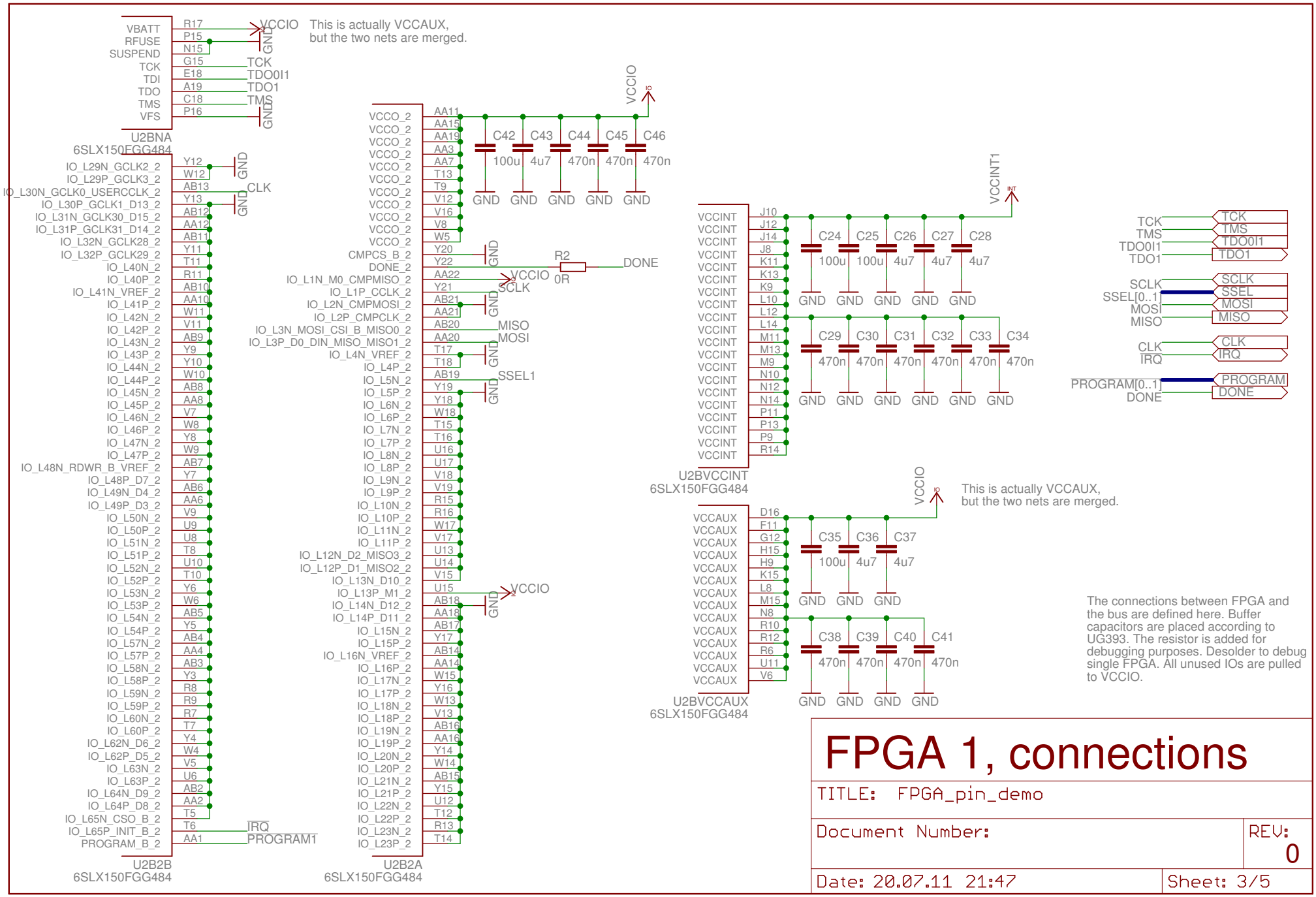
TITLE: FPGA_pin_demo

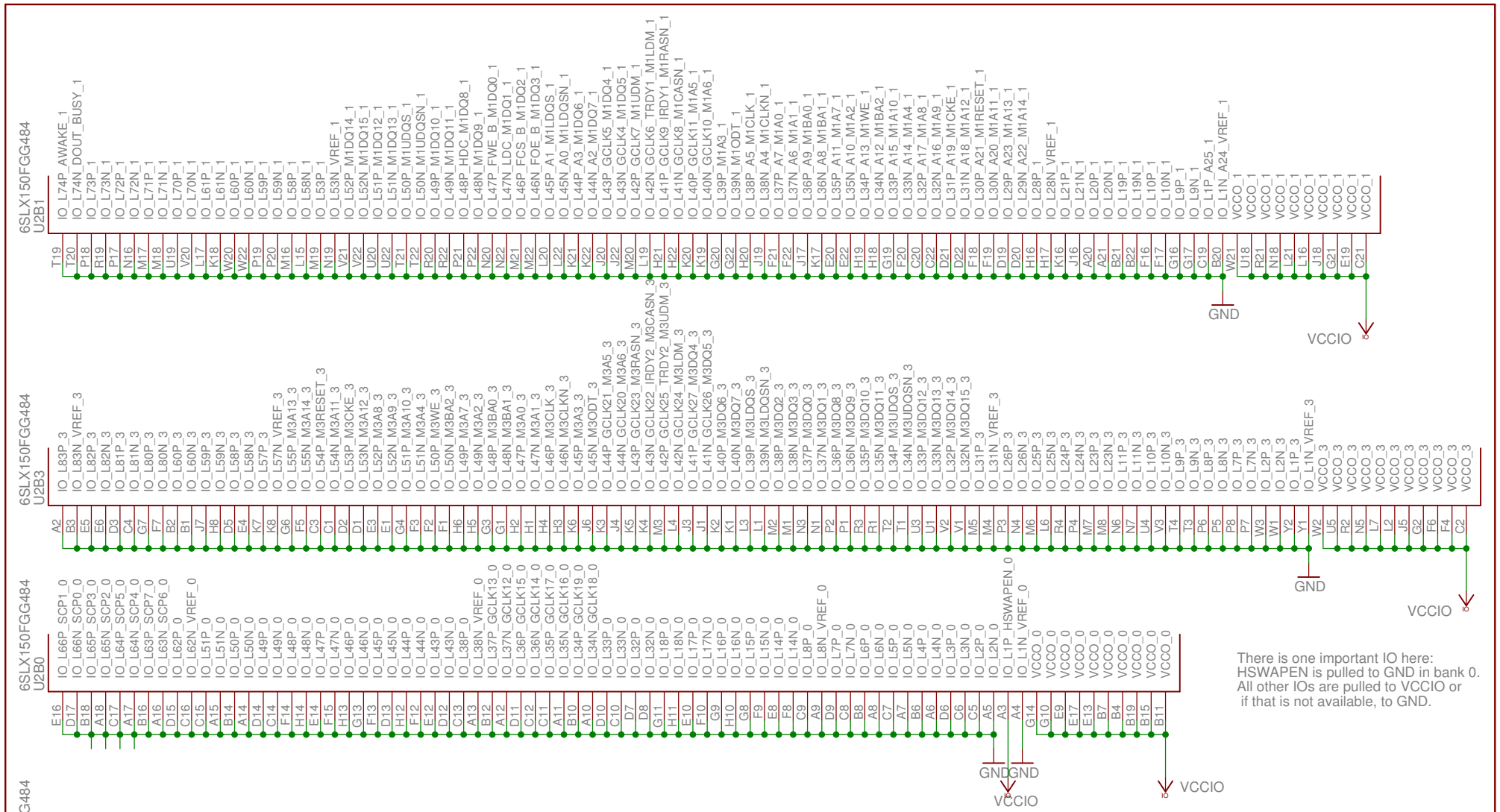
Document Number:

REV: 0

Date: 20.07.11 21:47

Sheet: 2/5


This is actually VCCAUX, but the two nets are merged.
U2BNA
6SLX150FGG484
U2B2B
6SLX150FGG484
U2B2A
6SLX150FGG484
U2BVCCINT
6SLX150FGG484
U2BVCCAUX
6SLX150FGG484
VCCIO
VCCINT1
DONE
R2
0R
TCK
TMS
TDO0I1
TDO1
SCLK
SSEL[0..1]
MOSI
MISO
CLK
IRQ
PROGRAM[0..1]
PROGRAM
PROGRAM1
SSEL1
This is actually VCCAUX, but the two nets are merged.
The connections between FPGA and the bus are defined here. Buffer capacitors are placed according to UG393. The resistor is added for debugging purposes. Desolder to debug single FPGA. All unused IOs are pulled to VCCIO.
FPGA 1, connections
TITLE: FPGA_pin_demo
Document Number:
REV: 0
Date: 20.07.11 21:47
Sheet: 3/5



FPGA 1, empty IOs

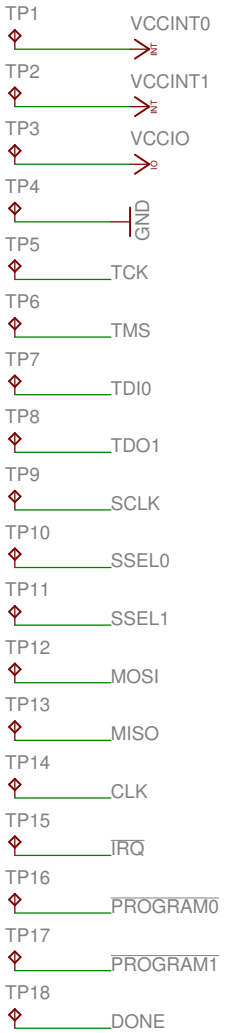
TITLE: FPGA_pin_demo

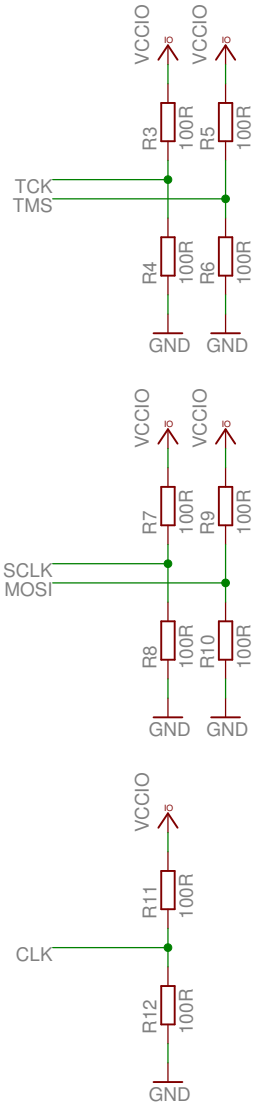
Document Number:

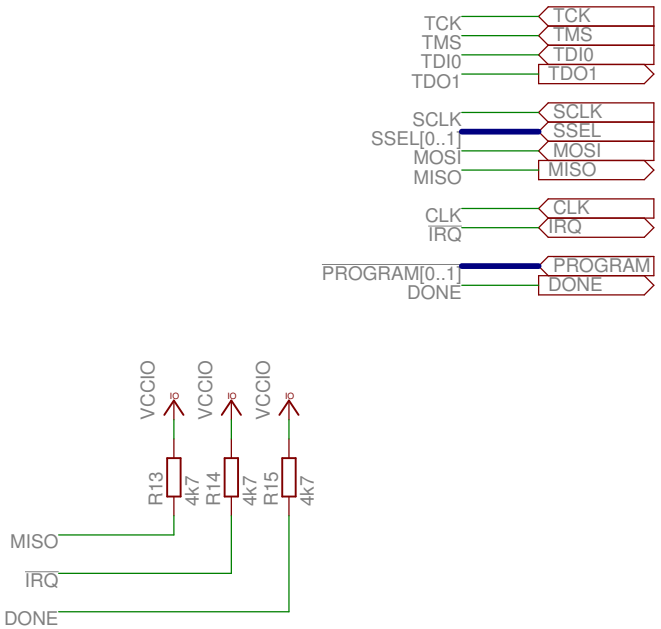
REV: 0

Date: 20.07.11 21:47

Sheet: 4/5







Bus Termination

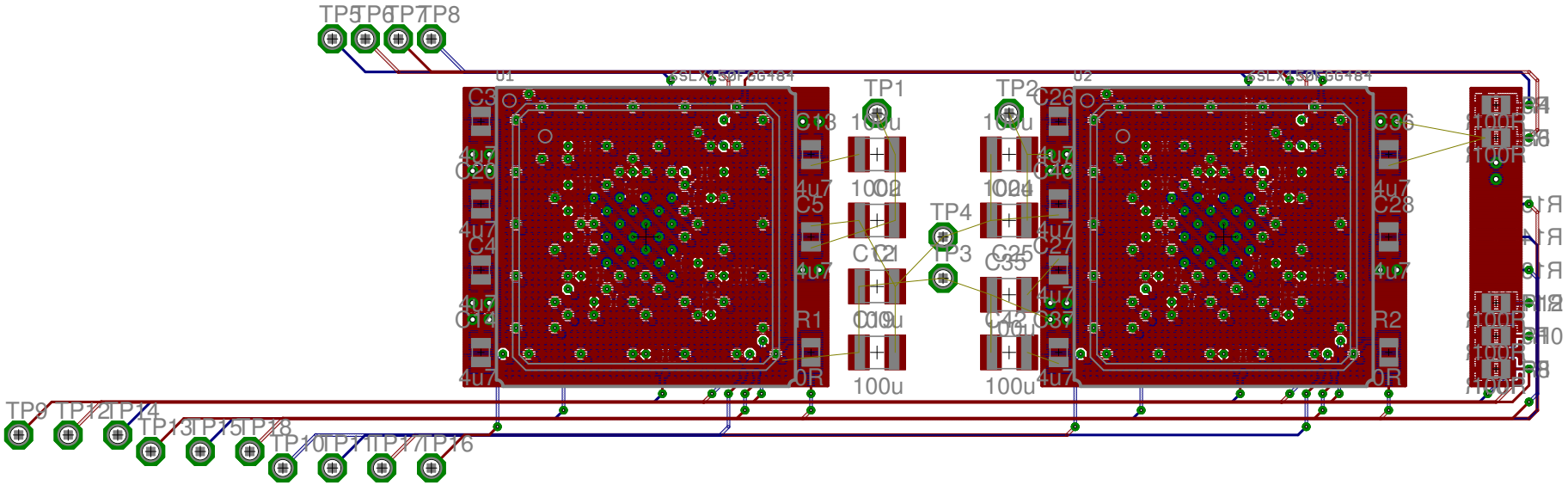
TITLE: FPGA_pin_demo

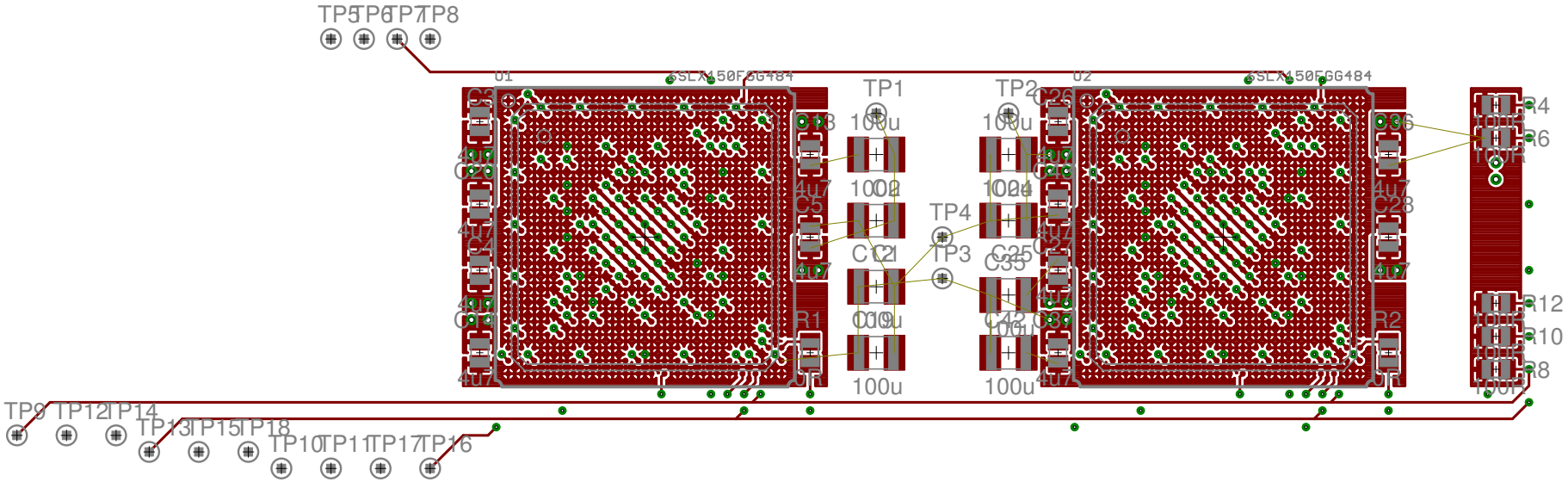
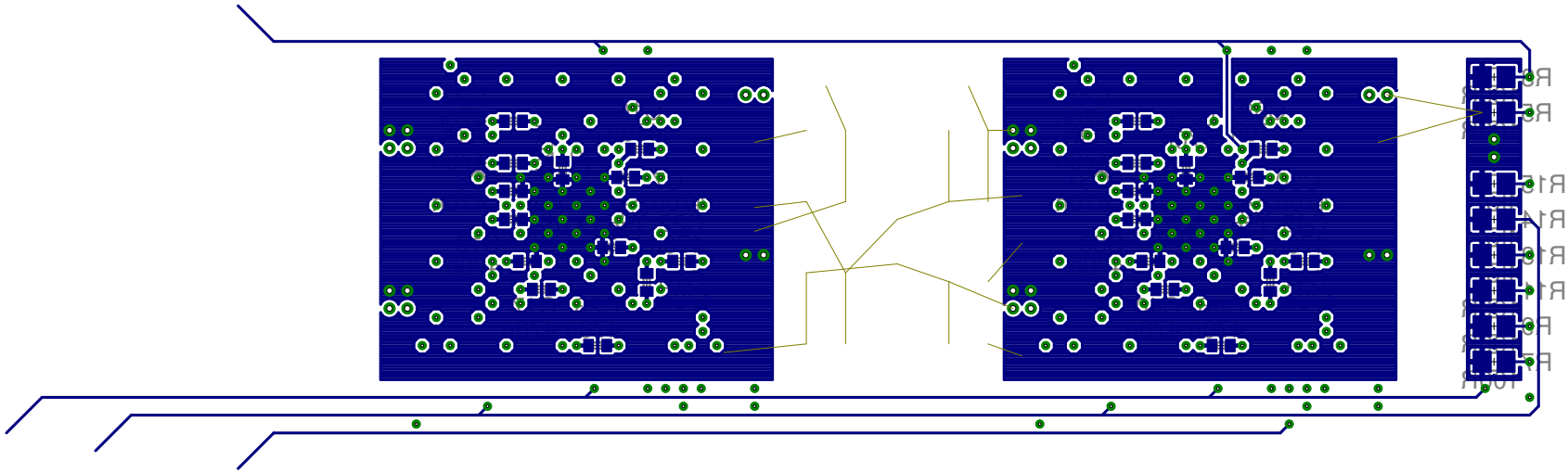
Document Number:

REV: 0

Date: 20.07.11 21:47

Sheet: 5/5


TP5
TP6
TP7
TP8
TP1
TP2
TP4
TP3
TP9
TP12
TP14
TP13
TP15
TP18
TP10
TP11
TP17
TP16
U1
U2
C3
C26
C36
C28
C5
C4
C27
C25
C35
C42
C37
R1
R2
4u7
100u
0R


TP5
TP6
TP7
TP8
U1
SLX150FGG484
U2
SLX150FGG484
TP1
TP2
TP3
TP4
100u
R1
R2
R4
R6
R8
R10
R12
TP9
TP12
TP14
TP13
TP15
TP18
TP10
TP11
TP17
TP16