SRAM-Based Programmable Counter

EE316: Computer Engineering Junior Lab
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1. Introduction

In this design, the author's were tasked with the development of an SRAM-Based Programmable Counter [1]. The designed system is expected to read and write data to and from the DE2-115 [2]

3. Results

Project Demo

4. Conclusion

The system functions as expected, but the reset button's reliability could be improved. This can be accomplished by observing the signals in Signal Tap Logic Analyzer.

2. Methods

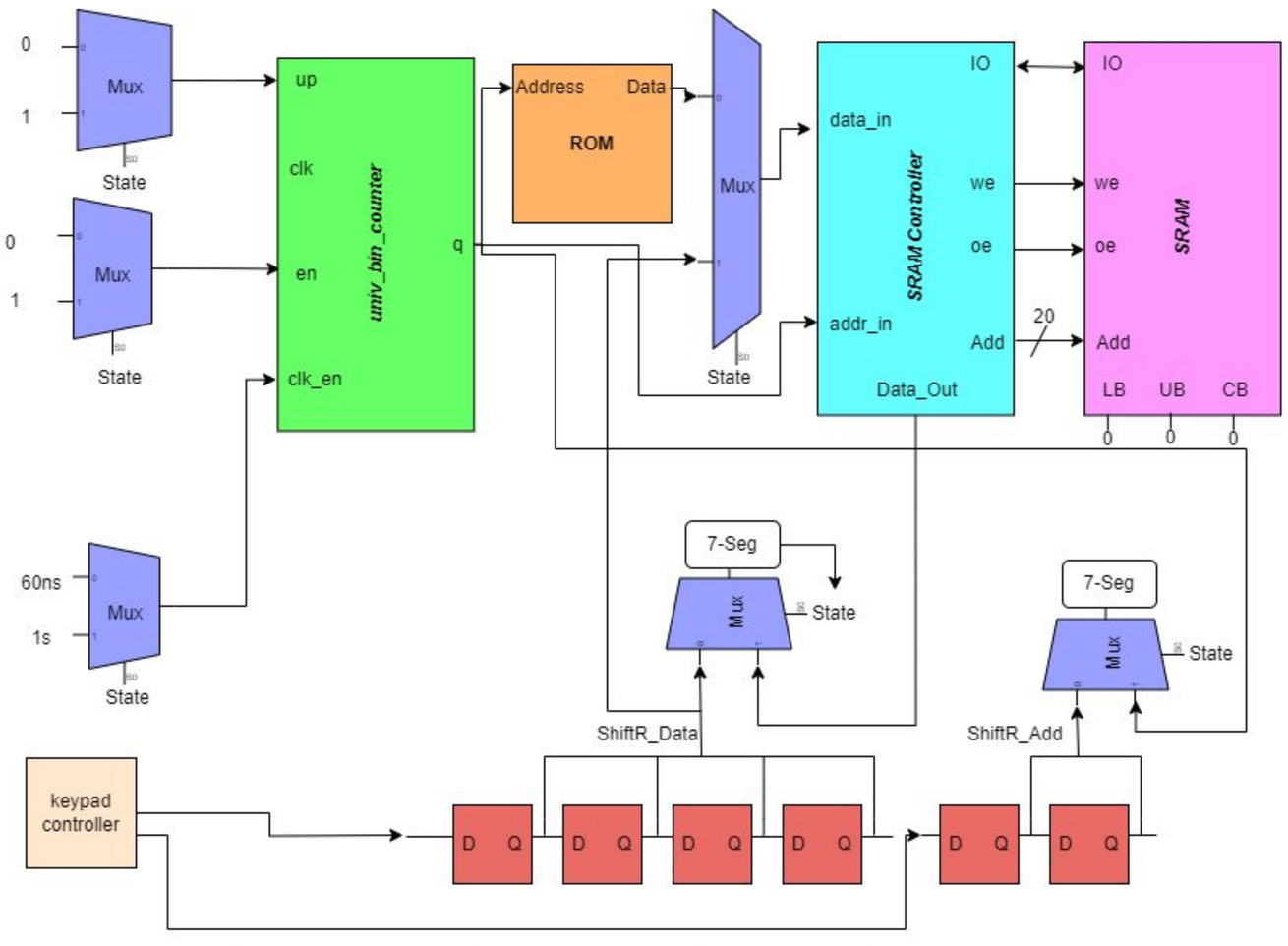

Figure 1: Functional Block Diagram of System

5. References

[1] https://github.com/olaoluwaolu/SRAM_Based_Counter
[2] "All FPGA boards - cyclone IV - altera DE2-115 development and Education Board," Terasic, https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=502 (accessed Feb. 10, 2024).