Inter-integrated Circuit (I2C) Overview

- A communication protocol used to connect low-speed devices such as microcontrollers, EEPROMS, and peripherals over short distances in embedded systems.
- Like SPI, it requires a 'Master-Slave' relationship between devices. However, I2C supports the use of multiple masters as well as slaves.
- Synchronised serial data transfer is accomplished using only 2 lines (figure 1):
    - ***Serial Clock Line (SCL)***: provides a clock signal to all devices to synchronise data transfer.
    - ***Serial Data Line (SDA)***: provides a shared data line to all devices on the bus.

Physical Bus Structure

- Master and slave bus drivers are "open drain" (figure 2):
    - they pull a line low by closing a transistor switch and grounding the bus.
    - they cannot drive a line high – preventing any potential situation where multiple devices try to pull a line high and low simultaneously.
- "Pull up" resistors tied to a voltage source are required to return a line to high once the transistor switch is opened.

Data Exchange

- Data transfer is coordinated by two special sequences* (figure 3):
    - ***'Start condition'***: SDA is brought low by master while SCL is high. This notifies all slave devices that a data transmission is about to begin.
    - ***'Stop condition'***: SDA is returned high while SCL is high. This notifies the end of the data transmission.
- Once the master has initiated the start condition, an address frame is placed on the SDA which comprises:
    - a 7-bit address which is sampled by the slaves to indicate to which device the message is being sent.
    - a R/W bit which informs the slave device of the type of data exchange, where:
        - '1' = the master is requesting data.
        - '0' = the master is sending data.
- If the slave device successfully understands the preceding address frame, it pulls the SDA low in acknowledgment and a data frame is then placed on the SDA, which comprises:
    - 1 data byte (8 bits)
- If the data is successfully R/W by the slave, it again pulls the SDA low in acknowledgement and the master initiates the 'stop' condition to end the data exchange.

**these conditions are the only times the SDA will change states while SCL is high.*

General advantages

- Minimal pin requirement (2 pins) – very beneficial to I/O constrained applications.
- 7-bit addressing and acknowledgements help ensure successful data transfer with a theoretical maximum of 128 slave devices.
- Extremely common.

General disadvantages

- Only supports half-duplex data exchange (cannot send and receive data simultaneously).
    - Slower than SPI.
- Higher complexity compared to other protocols such as SPI.
- Restricted to short distance communication.

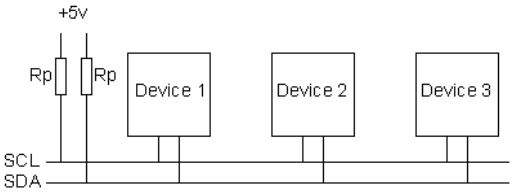

Figure 1: I2C bus

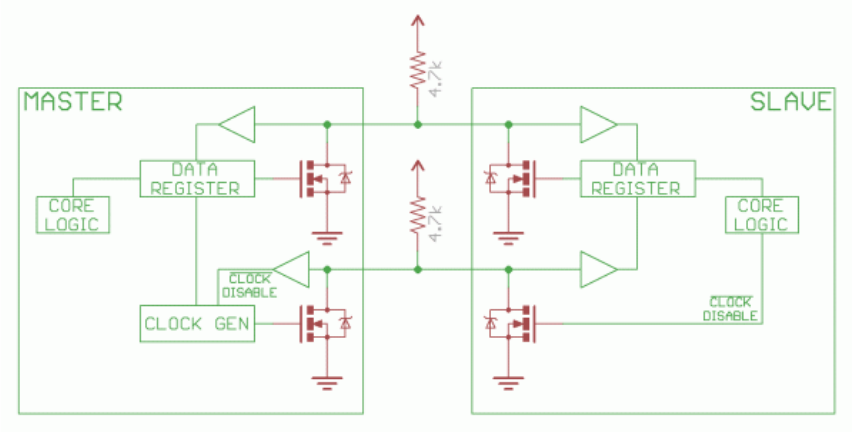

Figure 2: 'Pull up' resistors and transistor switches

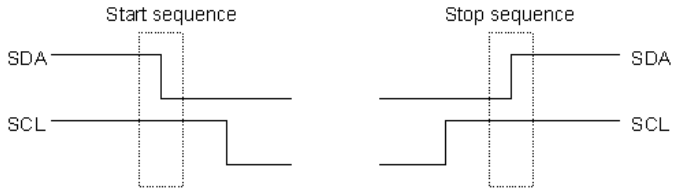

Figure 3: 'Start' and 'Stop' sequences

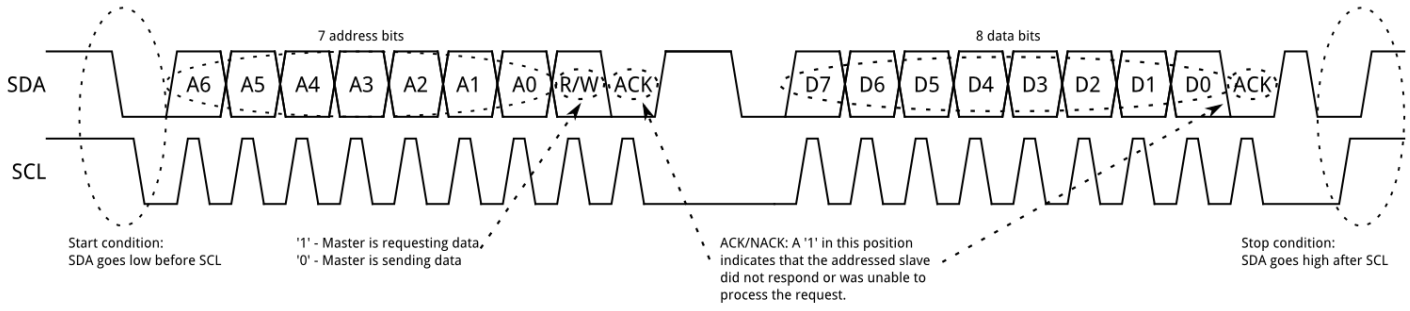

Figure 4: I2C Data Exchange: address and data frames

Sources:

https://learn.sparkfun.com/tutorials/i2c/all

https://i2c.info/

https://www.robot-electronics.co.uk/i2c-tutorial