Inter-Integrated Circuit Protocol also known as I^2C is a communication protocol it is used to connect low speed devices such as microcontrollers, D/A converters, I/O interfaces, and other similar peripherals. This protocol also requires a master-slave relationship however I^2C also supports multiple masters and slaves in a circuit. This means data is transferred bit by bit along a single wire which is the **Serial Data line (SDA line).** The SDA line is for the master and slave to send and receive data. It also uses **Serial Clock Line (SC line)** this provides a clock signal to all the devices to synchronise a data transfer.

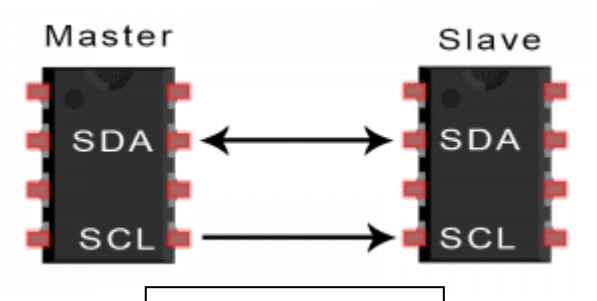

Figure.1. Master-Slave relationship for I^2C.

I^2C data is transferred like messages. Each message is broken up into frames of data, each message has its individual address frame that contains the binary address of the slave and a frame that contains the data being transmitted.

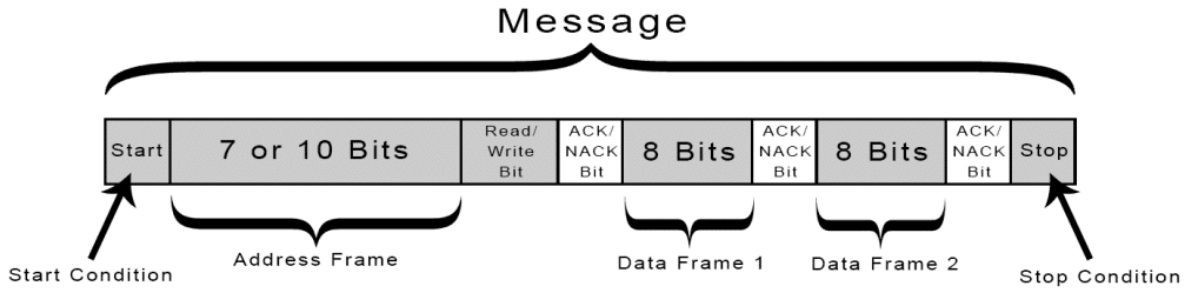

Figure.2. How I^2C works. [2]

There is a start and stop condition:

- Start Condition: The SDA line switches from high to a low voltage level just before the SC line switches from high to low voltage.
- Stop Condition: The SDA line switches from low to high voltage after the SC line switches from low to high.

In Figure.2. the **address frame** is a 7- or 10-bit sequence that is unique to each slave. This helps the master identify what slave is being talked to.

Read/Write Bit: A single bit that specifies whether the master is sending data to the slave (low voltage level) or requesting data from it (high voltage level).

ACK/NACK Bit: Each frame sent or received is followed by an acknowledge/no-acknowledge bit. If an address frame or data frame was successfully received, an ACK bit is returned to the sender from the receiving device.

Advantages of I^2C:

- Only uses 2 wires.
- Multiple masters and Slaves supported.
- Less complicated hardware.
- Well known protocol.

Disadvantages of I^2C:

- Slower data transfer than SPI.
- Data limited to 8 bits.
- More complicated than SPI.

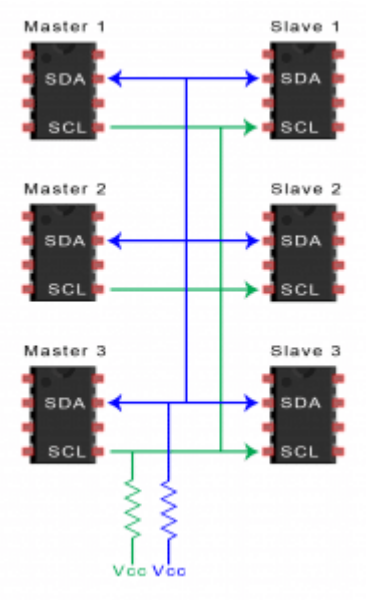

Figure.3. Multiple masters with multiple slaves [3]

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