DESCRIPTION OF I^2C

The Inter-Integrated Circuit (I^2C) is a communication protocol which allows for multiple slaves integrated with one or more masters in a microcontroller. The protocol only allowing for short distance communication within an integrated device or peripherals (slave) as it operates in half duplex mode (the amount of bandwidth is restricted). This is contrast to SPI which has a single master shifting and sampling between one or more slaves and, the SPI system allows for long distance communication over a multiple line (as, it operates in full duplex).

The I^2C is a synchronous system, which suggests that the master and each salve share the same clock frequency/sample rate. Most microcontrollers manufactured least come with one or more I^2C communication protocol as it is easy to manufacture compared to SPI or other protocols. This is because, I^2C contain lower number of logic gated and two lines/bus. The interface has a clock line and a data line which can be connected to multiple slaves/peripherals such as, accelerometer, temperature sensors or memory. The slaves/peripherals depend on the application the protocol is used for.

As the protocol is using serial communication the data stream on the data line starts with a start-bit. The start bit is sent to all the slaves connected to the master. The start-bit is followed by a control byte which is an address of the slave/peripheral the master wants to establish a communication with. This is done so that the data is not sent to the wrong device. At the rising or the falling edge of the clock (depends on how the master and slave if configured in settings), a read-write bit is copied to the data line and this is received by the slave. This tells the slave whether there is data coming in for processing or data is being requested by the master. In most I^2C microcontrollers are configured where a logic 0 signifies a write and 1 signifies a read. This may be able to be configured in the I^2C settings. The master waits for the slave/peripheral to send a as acknowledgement-bit, this is to show that the salve acknowledge the master. After the master receives the acknowledgement-bit signified by a logic 1, the address of the data to be written or read from is sent to the slave/peripheral. The data is read from or written to slave depending or earlier read-write bit request. The order that the data is sent and received by both device must be agreed both master and the slave. This may be configurable in the settings of both devices. The data can be read and written as MSB first or LSB first. After the data is read or written the slave sends an acknowledgement-bit to signify it has successfully met the request of the master. Finally, a stop-bit is sent to the slave/peripheral to signify an end in data transmission. The data request that might be sent to a slave/peripheral using a I2C could be to increase a lower the voltage to a motor in an autonomous self-driving car. This would be increase or lower the speed of the car or individual motors to turn the car.