SERIAL PERIPHERAL INTERFACE (SPI)

SPI is a synchronous interface that has a clock to keep it in sync and various data lines. The clock allows the receiver to know when to sample the bits on the data line, which is usually at a rising/falling edge.

SPI makes use of a master-slave notion. The side that generates the clock signal is known as the master, while the other is known as the slave. There can only be one master, but there can be multiple slaves. There are usually four data lines which are the SCLK (Serial clock), MOSI (Master-out slave-in, MISO (Master-in slave-out) and SS (Slave select). When data is transmitted from the master to the slave, it travels through the MOSI data line, but when data is transmitted from the slave to the master, it travels through the MISO data line.

The slave select (SS) data line activates a slave and enables the slave to send and receive data. When the SS line is at an active low is when the slave is usually activated and can then send and receive data. But when it is high, the slave is inactive at that time. SPI can also have multiple slaves, and this requires separate SS lines for each slave and multiple SS lines on the master corresponding to that on the slave, but the other data lines are shared. To communicate/activate a particular slave, its SS line must be set to a low, and the other slaves' SS line should be kept high. This prevents the other slaves from trying to send data through the same MISO line (since it is shared), causing a major issue.

There are some advantages of using an SPI. For one, it is full duplex, meaning data can be sent and receives at the same time through the MISO and MOSI (A master and slave can send and receive data simultaneously). It is very fast and is a very common interface on integrated circuits.

The disadvantages of SPI are that there are a lot of pins and this increases as the number of slaves increase. It is also very good with short distance, but not with long distance.