**Serial Peripheral Interface (SPI) overview**

- A communication protocol commonly used between integrated circuits, microcontrollers, and peripheral devices over short distances.
- Utilises a 'Master-Slave' relationship between devices, where the master (generally a microcontroller) controls one or more slaves (peripheral devices).
- Supports synchronised serial data transfer with use of 4 lines:
    - ***Serial Clock (SCLK)***: to provide clock signals to synchronise data transmission
    - ***Master Out Slave In (MOSI)***: a dedicated data line to send data from the master device to a slave.
    - ***Master In Slave Out (MISO)***: a dedicated data line to send data from a slave device to the master.
    - ***Slave Select (SS)***: A signal line used to wake and select slave device to send or receiving data. (This line is typically held high to disconnect a slave from the interface bus, and only brought low when required. This is known as 'active low'.

**Modes and Bus timings**

There are 4 possible clocking configurations the SPI protocol can synchronise data exchange (figure 1).

- Non-inverted clock polarity (SCLK is low when SS is brought low):
    - Mode 0: Data is sampled on positive edge of clock signal and shifted on negative edge.
    - Mode 1: Data is sampled on negative edge of clock signal and shifted on positive edge.
- Inverted clock polarity (SCLCK is high when SS is brought low):
    - Mode 2: Data is sampled on negative edge of clock signal and shifted on positive edge.
    - Mode 3: Data is sampled on positive edge of clock signal and shifted on negative edge.

**Multiple Slave configurations**

- SPI interfacing supports the control of multiple slave devices by a single master in 2 main configurations.
- In a more standard 'multiple slave select' arrangement (figure 2):
    - all slave devices share the SCLK, MOSI, and MISO lines.
    - each slave device has an independent SS line.
    - Slave SS lines are kept high when the device is not communicating with the master. This prevents the device reading from or writing to the MOSI and MISO lines. Only when a slave's SS line is brought low can it communicate with the master device.
- In a 'daisy-chain' arrangement (figure 3):
    - All slave devices share a single SCLCK and SS line.
    - The MOSI line is fed from the master to the first slave, whose MISO line is then fed into the next slave's MISO.
    - This repeats until the final slave's MISO line is returned to the master's MISO.
    - Data sent from the master must cascade through each preceding slave to reach its destination.

**General advantages**

- Simplistic structure.
- Typical performance is faster than other communication protocols such as UART and I2C.
- Supports full duplex data exchange (simultaneous 2-way communication between master and slaves).
- Extremely common.

**General disadvantages**

- Potentially high pin requirement (each additional slave device requires separate SS line).
- Generally restricted to small distance communication (~1M).

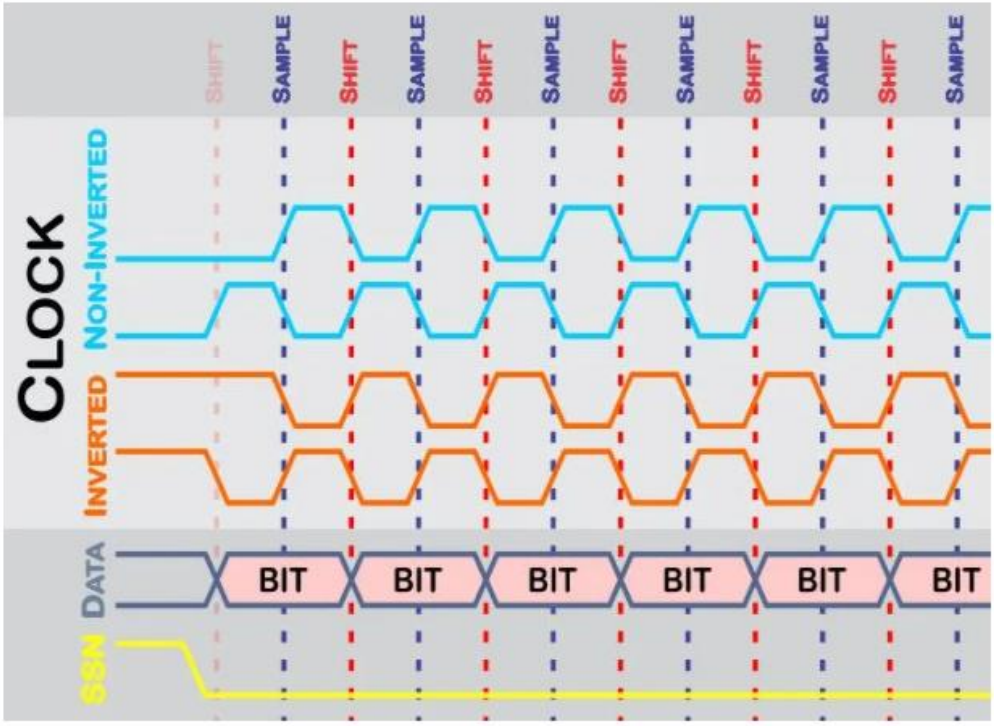


*Figure 1: Modes and bus timings*

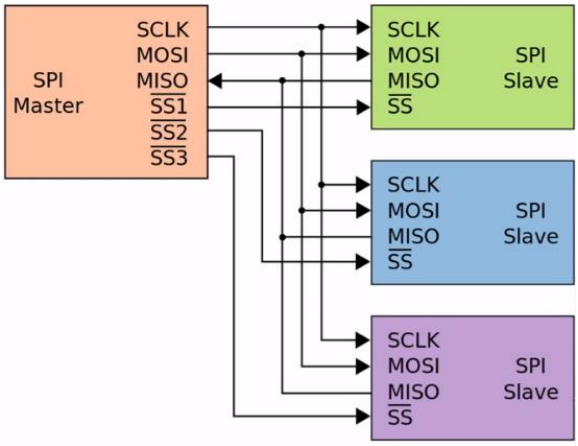


*Figure 2: 'Multiple Slave select'*

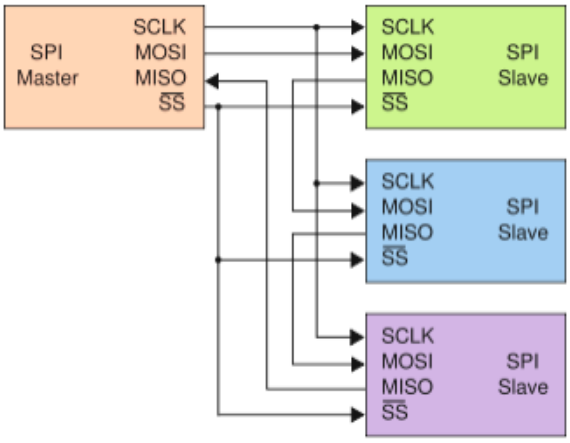


*Figure 3: 'Daisy Chain'*

Sources:

https://www.allaboutcircuits.com/technical-articles/spi-serial-peripheral-interface/

https://www.arduino.cc/en/Reference/SPI

https://learn.sparkfun.com/tutorials/serial-peripheral-interface-spi/all