

Getting Started with the Spartan-6 FPGA SP605 Embedded Kit

UG667 (v3.1) June 30, 2011



XPM 0402809-01



The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

© Copyright 2010–2011 Xilinx, Inc. XILINX, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/05/10	1.0	Initial Xilinx release.
12/21/10	2.0	Procedures have been updated in accordance with ISE® Design Suite: Embedded Edition, version 12.4.
03/15/11	3.0	Procedures have been updated in accordance with ISE Design Suite: Embedded Edition, version 13.1.
06/30/11	3.1	Replaced 13.1 with 13.x.

Table of Contents

Revision History	2
-------------------------------	---

Preface: About This Guide

Additional Documentation	5
Additional Resources	6
Conventions	6
Typographical.....	6
Online Document.....	7

Getting Started with the Spartan-6 FPGA SP605 Embedded Kit

Introduction	9
SP605 Embedded Kit Contents	9
What's Inside the Box	9
What's Available Online.....	10
Getting Started with the Benchmarking Demonstration	10
Processor System Used for the Benchmarking Demonstration.....	10
Benchmarking Demo Hardware Setup Instructions.....	12
Running the Benchmarking Demo	13
Installation and Licensing of ISE Design Suite 13.x.....	18
ISE 13.x Software Installation.....	18
Downloading and Installing Tool Licenses	25
Communicating with the SP605 USB-UART	30
Installing the USB-UART driver	30
Connecting to the SP605 UART	30
Configuring the Host Computer.....	30
Testing the USB-UART Driver Installation.....	31
Next Steps	33
Data Sheet.....	34
Tutorials	34
Reference Designs.....	34
Getting Help and Support.....	35

Appendix A: Warranty

About This Guide

This guide provides information for getting started with the Spartan®-6 FPGA SP605 Embedded Kit.

Additional Documentation

The following documents are available for download at
<http://www.xilinx.com/products/spartan6/>.

- Spartan-6 Family Overview
This overview outlines the features and product selection of the Spartan-6 family.
- Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
This data sheet contains the DC and switching characteristic specifications for the Spartan-6 family.
- Spartan-6 FPGA Packaging and Pinout Specifications
This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- Spartan-6 FPGA Configuration User Guide
This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
- Spartan-6 FPGA SelectIO Resources User Guide
This guide describes the SelectIO™ resources available in all Spartan-6 devices.
- Spartan-6 FPGA Clocking Resources User Guide
This guide describes the clocking resources available in all the Spartan-6 devices, including the DCMs and PLLs
- Spartan-6 FPGA Block RAM Resources User Guide
This guide describes the Spartan-6 device block RAM capabilities.
- Spartan-6 FPGA GTP Transceivers User Guide
This guide describes the GTP transceivers available in the Spartan-6 LXT FPGAs.
- Spartan-6 FPGA DSP48A1 Slice User Guide
This guide describes the architecture of the DSP48A1 slice in Spartan-6 FPGAs and provides configuration examples.
- Spartan-6 FPGA Memory Controller User Guide

This guide describes the Spartan-6 FPGA memory controller block, a dedicated embedded multi-port memory controller that greatly simplifies interfacing Spartan-6 FPGAs to the most popular memory standards.

- Spartan-6 FPGA PCB Designer's Guide

This guide provides information on PCB design for Spartan-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu	File → Open
	Keyboard shortcuts	Ctrl+C
<i>Italic font</i>	Variables in a syntax statement for which you must supply values	ngdbuild <i>design_name</i>
	References to other manuals	See the <i>Command Line Tools User Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus[7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>

Convention	Meaning or Use	Example
Braces { }	A list of items from which you must choose one or more	<code>lowpwr ={on off}</code>
Vertical bar	Separates items in a list of choices	<code>lowpwr ={on off}</code>
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	<code>allow block block_name loc1 loc2 ... locn;</code>

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “ Additional Resources ” for details. Refer to “ Title Formats ” in Chapter 1 for details.
<u>Blue, underlined text</u>	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Getting Started with the Spartan-6 FPGA SP605 Embedded Kit

Introduction

The Spartan®-6 FPGA Embedded Kit conveniently delivers the key components of the Xilinx® Embedded Targeted Design Platform (TDP) required for developing embedded software and hardware in a wide range of applications in Broadcast, Industrial, Medical, Aerospace and Defense markets. For software developers, a familiar Eclipse-based IDE, GNU tools, OSes, libraries and a pre-verified reference design enables them to start programming right away. Similarly, hardware designers now have immediate access to a pre-integrated MicroBlaze™ processor subsystem that includes the most commonly used peripheral IP cores, enabling them to begin at once developing their custom logic.

This Getting Started Guide identifies steps required to set up the SP605 board and run the out-of-box Benchmarking and Linux demonstrations that are designed to illustrate the flexibility and capability of a MicroBlaze processor subsystem for embedded design. If the Xilinx ISE® software has not already been installed, the user is directed through the steps to install the software, get updates, and generate a license. This guide then identifies the next steps in using the embedded software and hardware tutorials included in this kit.

SP605 Embedded Kit Contents

What's Inside the Box

- SP605 Evaluation Board with the XC6SLX45T-3FGG484 FPGA along with:
 - Power Supply
 - Two USB Type-A to Mini-B 5-pin cables
 - Ethernet Cable
 - Compact Flash card - 2 GB (with Embedded Kit demo)
- ISE Design Suite Embedded Edition: (device-locked) for Spartan-6 LX45T FPGA
- Xilinx ISE Design Suite 13.x DVD, which includes:
 - ISE Foundation with ISE Simulator
 - PlanAhead Design and Analysis Tool
 - Xilinx Platform Studio (XPS)
 - Software Development Kit (SDK)
 - ChipScope™ Pro logic analyzer

- Documentation
 - SP605, *Hardware Setup Guide*
 - UG667, *Getting Started with the Spartan-6 FPGA SP605 Embedded Kit*
 - DS667, *AXI Interface Based SP605 Embedded Kit MicroBlaze Processor Subsystem Data Sheet*
 - UG669, *AXI Interface Based ML605/SP605 MicroBlaze Processor Subsystem Hardware Tutorial*
 - UG670, *AXI Interface Based ML605/SP605 MicroBlaze Processor Subsystem Software Tutorial*
- Reference Designs and Demonstrations
 - Base MicroBlaze Processor Subsystem
 - Benchmarking Demonstration
- Reference designs, demonstrations, documentation, and applications delivered on USB Flash drive to get started quickly

What's Available Online

- License for ISE Design Suite 13.x Embedded Edition
 - <http://www.xilinx.com/getproduct>
 - <http://www.xilinx.com/tools/faq.htm>
- Embedded Kit home page with Documentation and Reference Designs
 - <http://www.xilinx.com/s6embkit>
- Technical Support
 - <http://www.xilinx.com/support/>

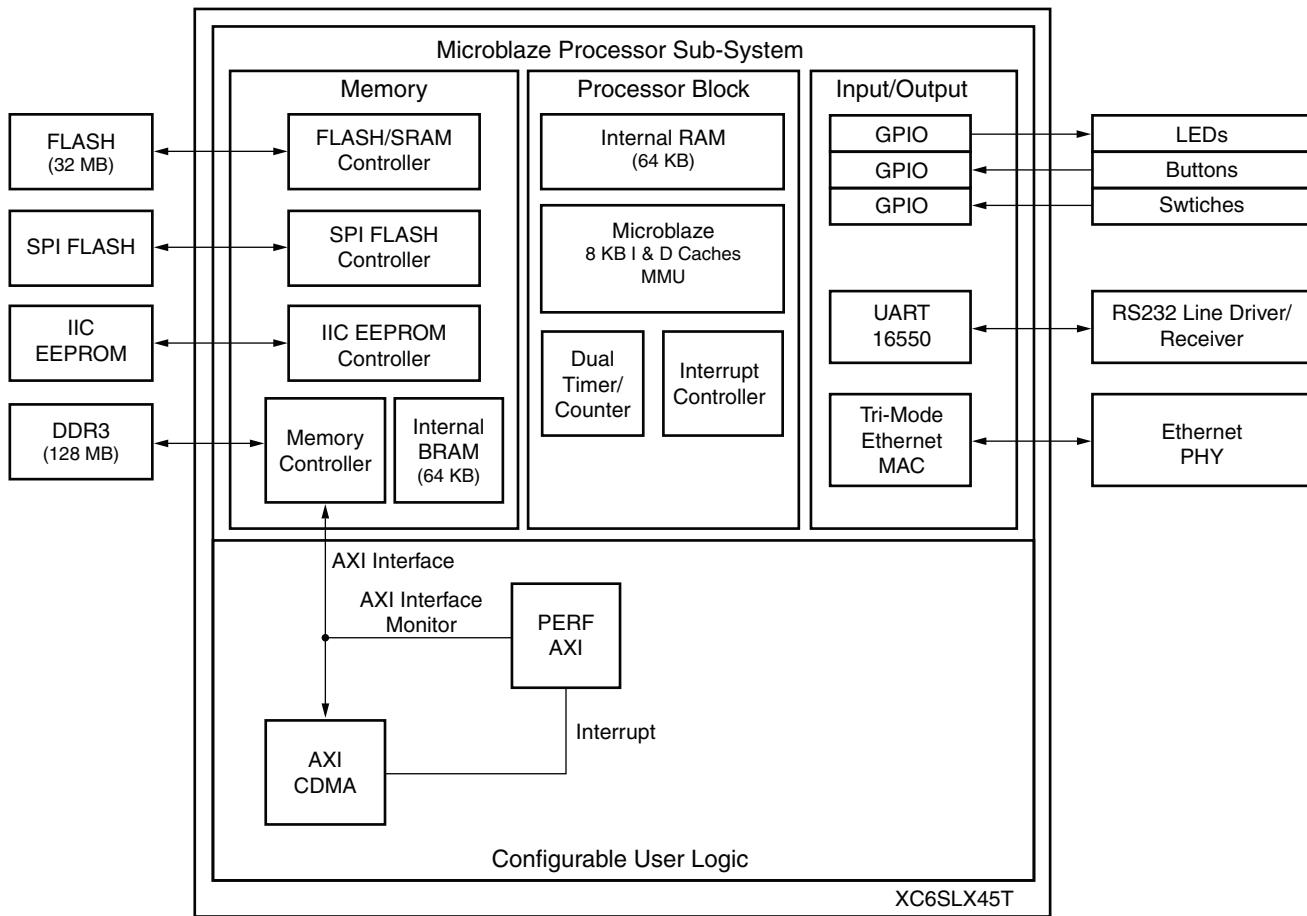
Getting Started with the Benchmarking Demonstration

This Spartan-6 Embedded Kit comes with a benchmarking demo available on the provided Compact Flash card. This demo can be run before installing any additional tools to get an overview of the features of the SP605 Evaluation Board using a MicroBlaze Processor Subsystem in the Spartan-6 LX45T FPGA.

Processor System Used for the Benchmarking Demonstration

The provided benchmarking demo uses a pre-built Spartan-6 FPGA design ([Figure 1](#)) with the following features:

- MicroBlaze soft processor
- External DDR3 SDRAM Memory Interface
- External Flash Memory Interface
- On-chip Memory (Block RAM)
- Tri-Mode Ethernet MAC (evaluation license)
- UART (connected from SP605 board via the USB-UART connector)
- Interrupt Controller (Intc) and Timer
- GPIO (LEDs, Buttons, Switches)



UG667_01_022511

Figure 1: Spartan-6 FPGA Benchmarking Demo System

Benchmarking Demo Hardware Setup Instructions

1. Connect the SP605 board to an Ethernet port on a computer via an Ethernet Cable.
2. Set the IP address of the PC to **192.168.1.100**. Return the IP address of the PC back to its original setting after running the demo.
- Note:** The demo uses a hard-coded MAC address and a fixed IP address of **192.168.1.10** and does not connect to the regular LAN network using DHCP. Do not connect more than one board to the same network segment.
3. Confirm that the SP605 jumper settings are set as identified in [Table 1](#).

Table 1: SP605 Jumper Settings

Jumper REFDES	Function	Default
FMC JTAG Bypass		
J19	Exclude FMC LPC connector J2	Jump 1-2
SFP Module		
J22	SFP Full BW	Jump 1-2
J44	SFP Enabled	Jump 1-2
SPI Memory Select		
J46	SPI Select SPI X4 Memory U32	Jump 1-2
System ACE CF Error LED		
J60	System ACE CF Error LED DS18 Enabled	Jump 1-2

Note: If the Embedded Kit design files were downloaded online, copy the entire folder - “<Zip File>/ CompactFlash_Demo_Image/” onto the Compact Flash card root directory using a CF card reader.

4. Insert the Compact Flash card into the board as shown in [Figure 2](#).
5. Set the System ACE DIP switches shown in [Figure 2](#) to the settings listed in [Table 2](#).



Figure 2: Compact Flash Card Installation and DIP Switch Settings

Table 2: Benchmarking Demo System ACE DIP Switch Settings

DIP Switch	Switch Position
1	Off
2	Off
3	Off
4	On

The pre-built Benchmarking Demo provided with this kit is now ready to be run. Follow the next set of instructions to run the demo.

Running the Benchmarking Demo

1. If the SP605 board is not already powered on, plug in the power adapter to local AC power. Plug the 12V power cable into the board connector on J18. Turn on the power by switching the SW2 to the “ON” position.
2. Open a web browser on the host computer and set the URL to **192.168.1.10**. The web page shown in [Figure 3](#) should be displayed. The Web page uses Javascript, so the browser must have Javascript enabled

Note: If the browser is an Internet Explorer browser, the Adobe SVG viewer plugin or a similar plugin that enables viewing of SVG files must be installed to view the graph.

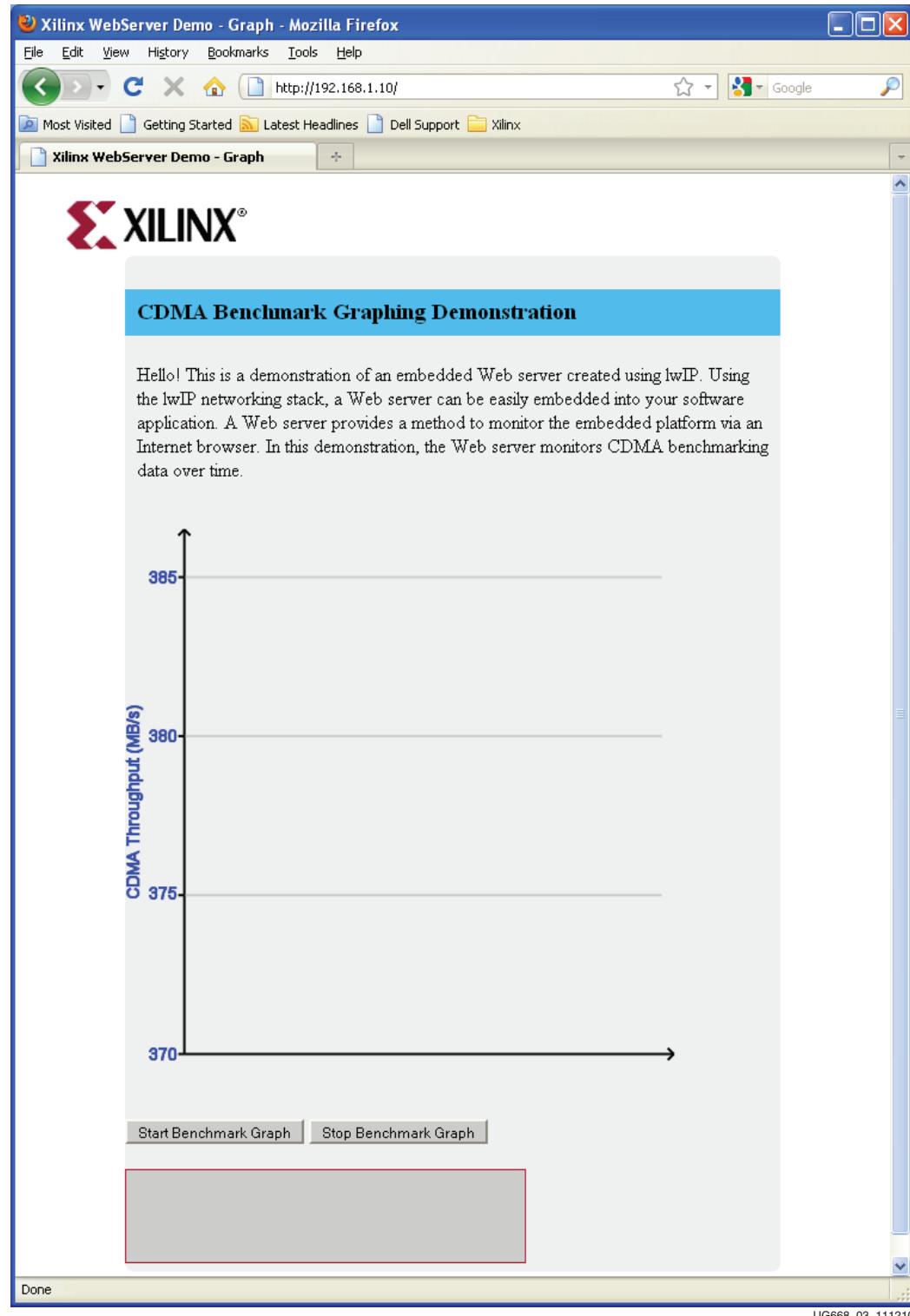


Figure 3: Initial Benchmarking Demonstration Web Page

3. In the benchmarking demonstration Web page, click **Start Benchmark Graph** to start requesting benchmarking data. Data collected from the Web server appears in the text box below the buttons and the graph begins to show. An example of the page with benchmarking data is shown in [Figure 4](#).

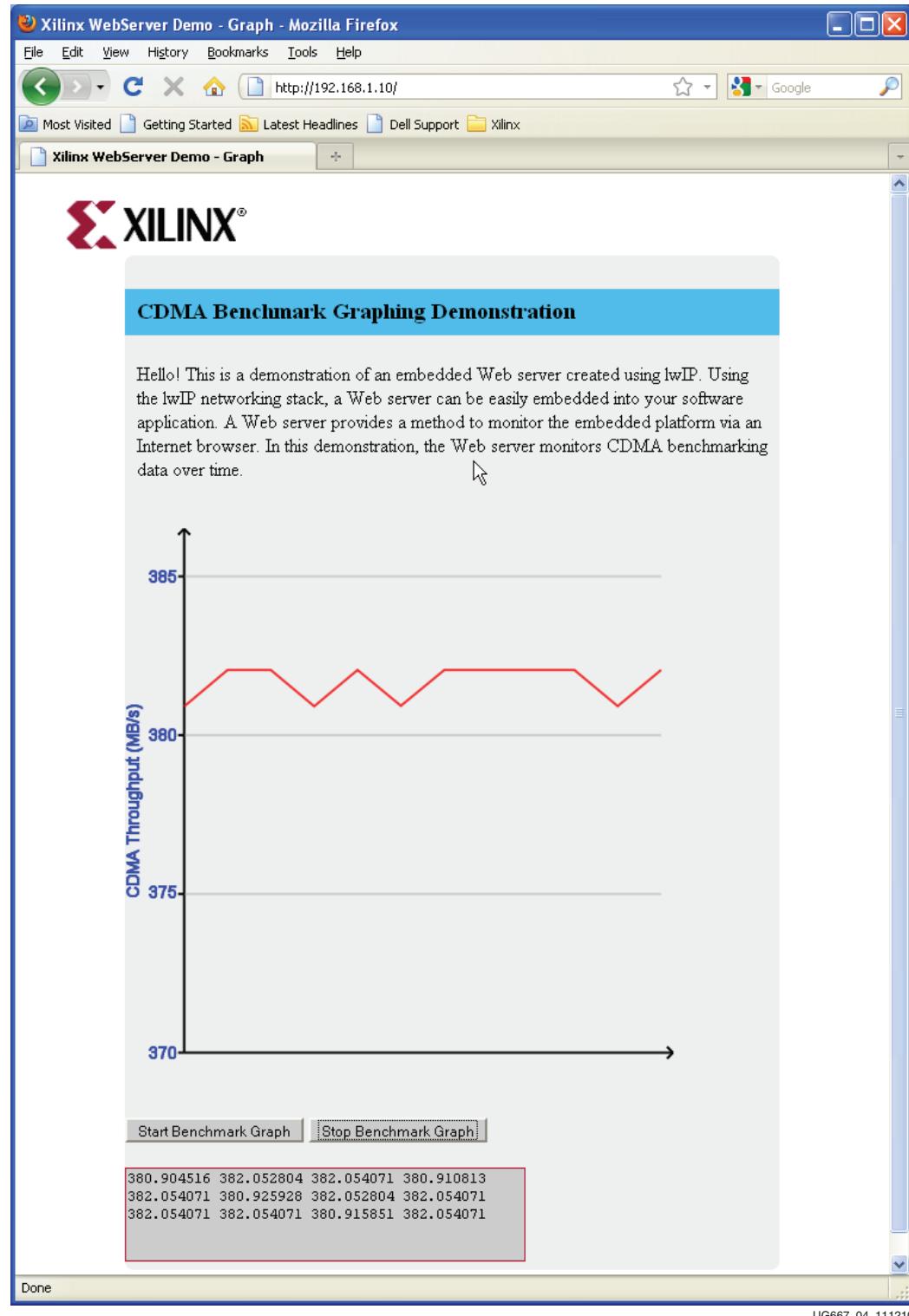


Figure 4: Benchmarking Demonstration Web Page with Data Plotted

The Web browser receives one CDMA throughput result at a time. Javascript is used to convert the throughput result into coordinates and update the graph. The graph updates every time a new data point is received. The graph holds a maximum of 12 data points at a time. After the maximum has been reached, the oldest data point is dropped and the newest data point is added.

4. In the benchmarking demonstration Web page, click **Stop Benchmark Graph** to stop requesting CDMA throughput data. After this button is clicked, any pending requests complete and then no additional data is requested
5. Repeat [step 3](#) and [step 4](#) as desired.

At this point in the tutorial the Benchmarking demo using the SP605 board with Spartan-6 LX45T FPGA and the MicroBlaze soft processor has been completed. Because a fully configured MicroBlaze Processor Subsystem has been provided, the user can start developing embedded software. In addition, because an FPGA is being used, the processor subsystem can be fully customized. In order to do this, the ISE Design Suite 13.x tools and the USB-UART driver must be installed on the computer. The [Installation and Licensing of ISE Design Suite 13.x, page 18](#) section of this document identifies these steps.

Installation and Licensing of ISE Design Suite 13.x

This SP605 Embedded Kit comes with entitlement to a full seat of the ISE Design Suite: Embedded Edition that is device locked to a Spartan-6 LX45T. This software can be installed from the DVD or the Web installer can be downloaded from <http://www.xilinx.com/support/download/index.htm>.

ISE 13.x Software Installation

1. Run the ISE Design Suite 13.x Installer:
 - a. Option 1: Insert the ISE Design Suite 13.x DVD included in this kit into your computer
 - If the Installer does not start automatically, run the “xsetup” executable from the DVD
 - b. Option 2: Run the Web Installer that you can download from <http://www.xilinx.com/support/download/index.htm>

You will be prompted with a Welcome dialog (Figure 5), two License agreements (Figure 6 and Figure 7), a selection of which tool edition to install (Figure 8), installation options (Figure 9), and an opportunity to select where you would like to install the software (Figure 10).

Note: It is recommended that you accept the two license agreements, install the ISE Design Suite: Embedded Edition, and accept the default install location.

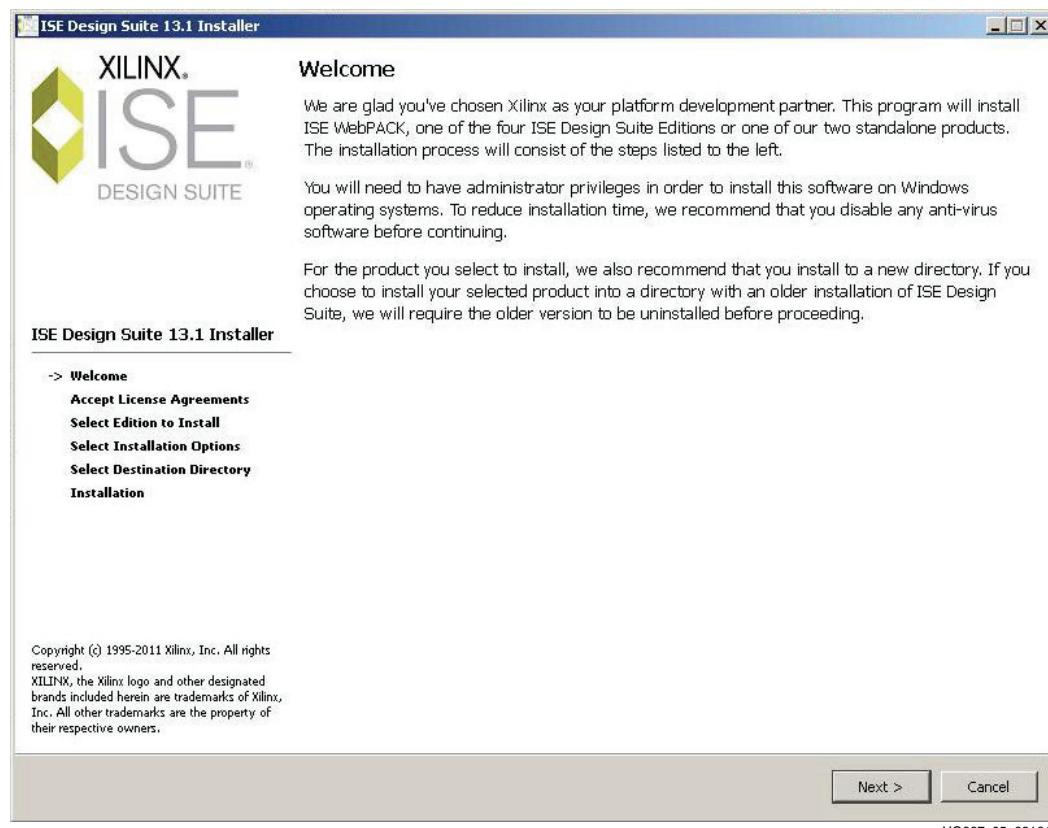


Figure 5: ISE Design Suite Install Welcome Screen

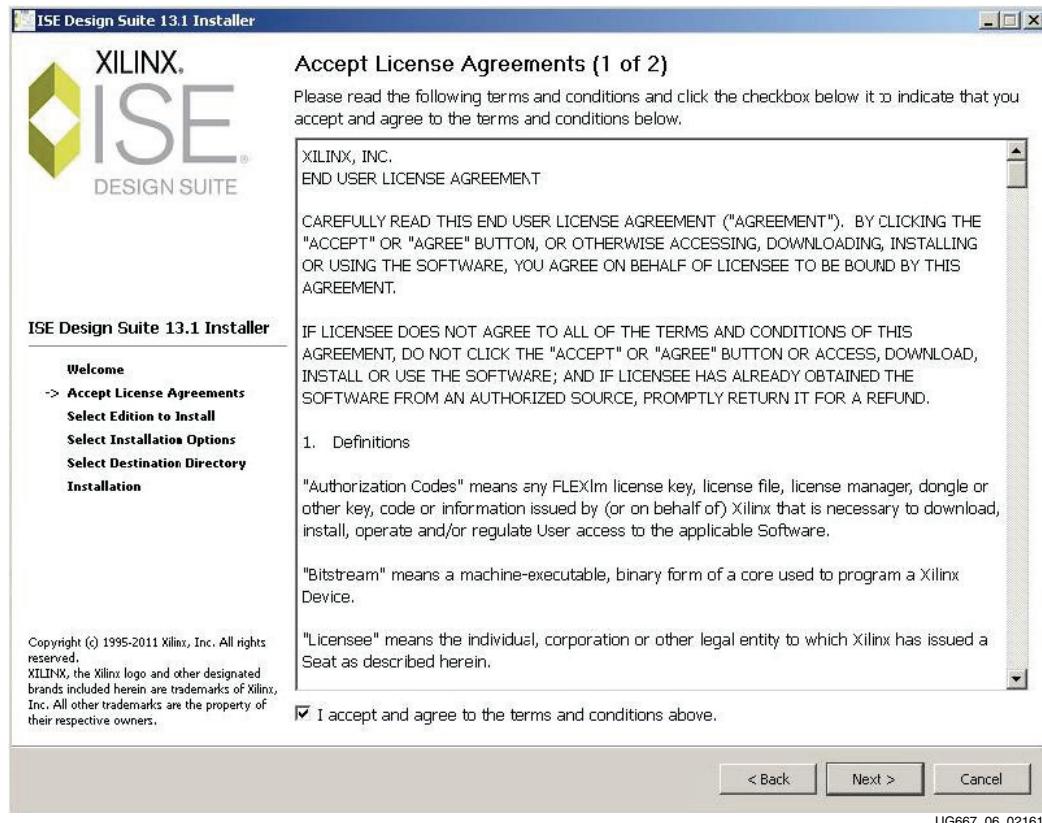


Figure 6: ISE Design Suite Third-Party Usage License Agreement

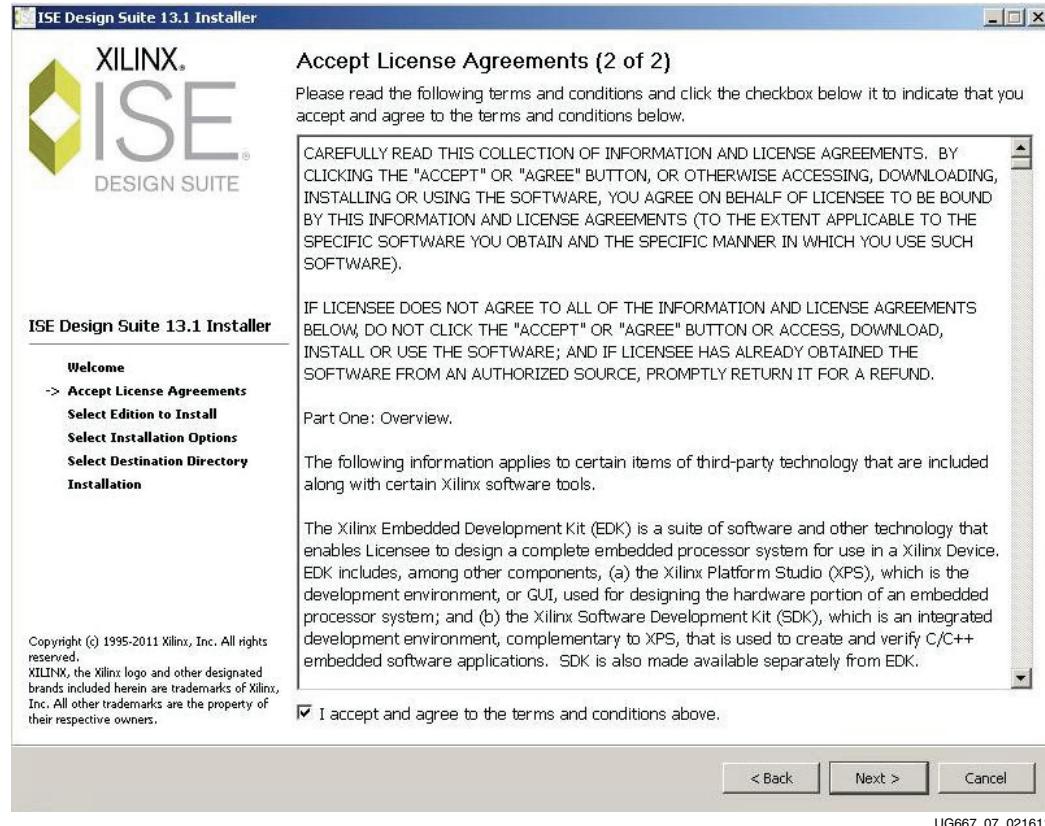


Figure 7: ISE Design Suite End-User License Agreement

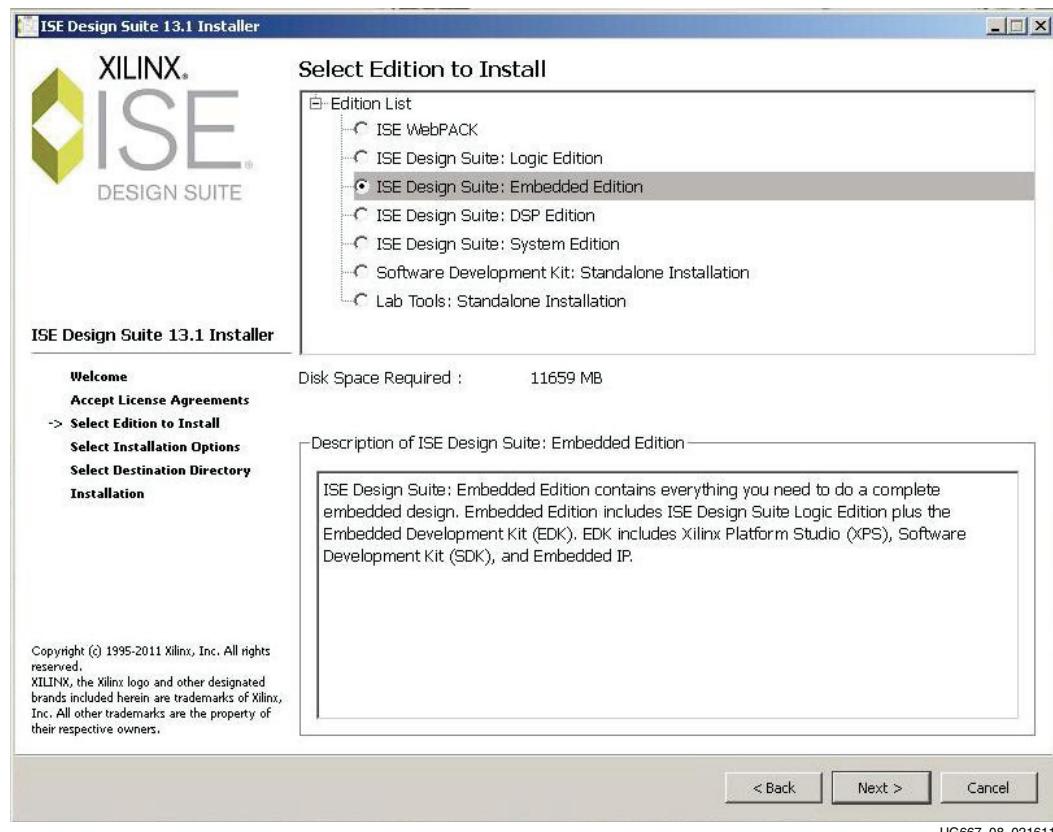


Figure 8: ISE Design Suite Edition Selection

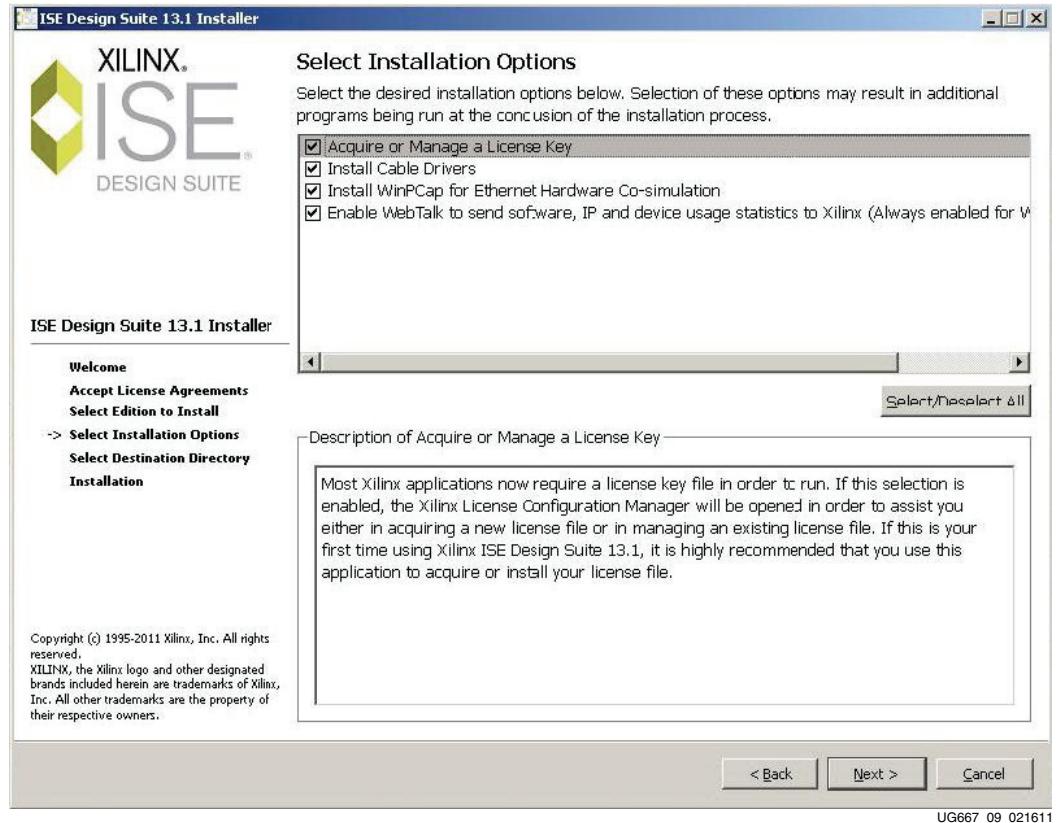


Figure 9: Installation Options

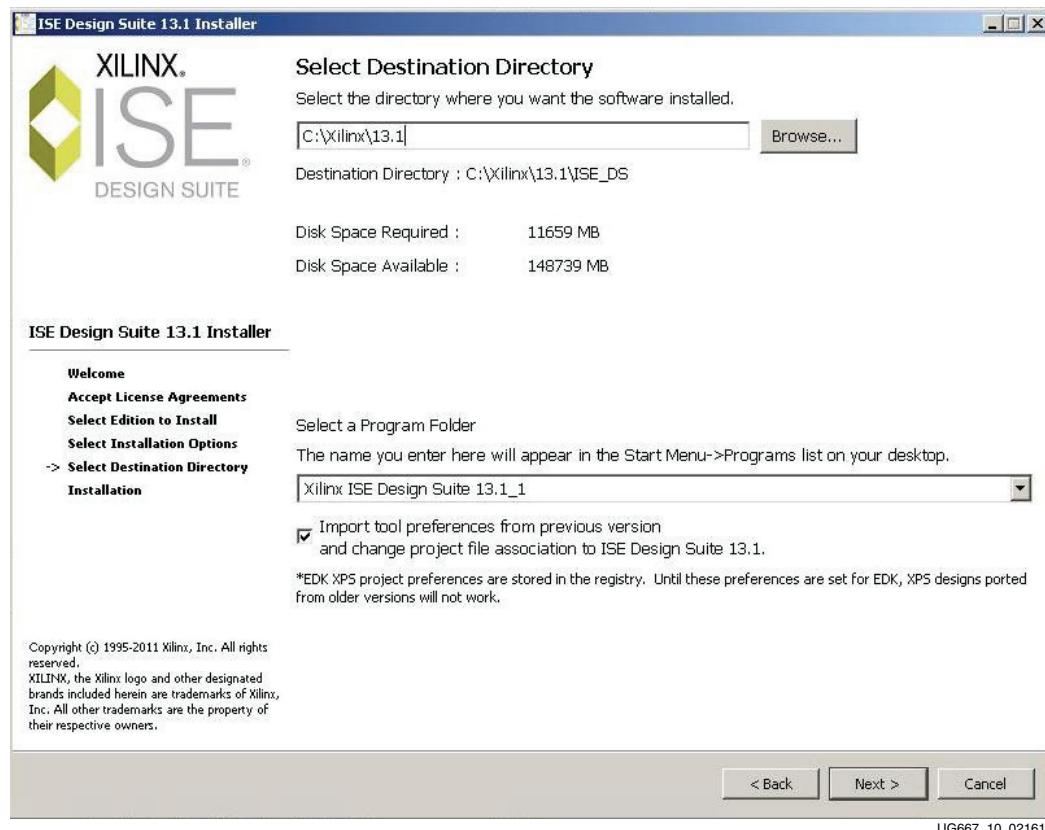


Figure 10: ISE Design Suite Destination Directory

2. The installer summarizes the installation settings. Click **Install** to start the installation.
Note: The DVD installation might take about one hour. The Web installation might take about three to ten hours based on Internet download speeds.
3. When the installation has completed, the window shown in [Figure 11](#) is displayed. Click **Finish**.

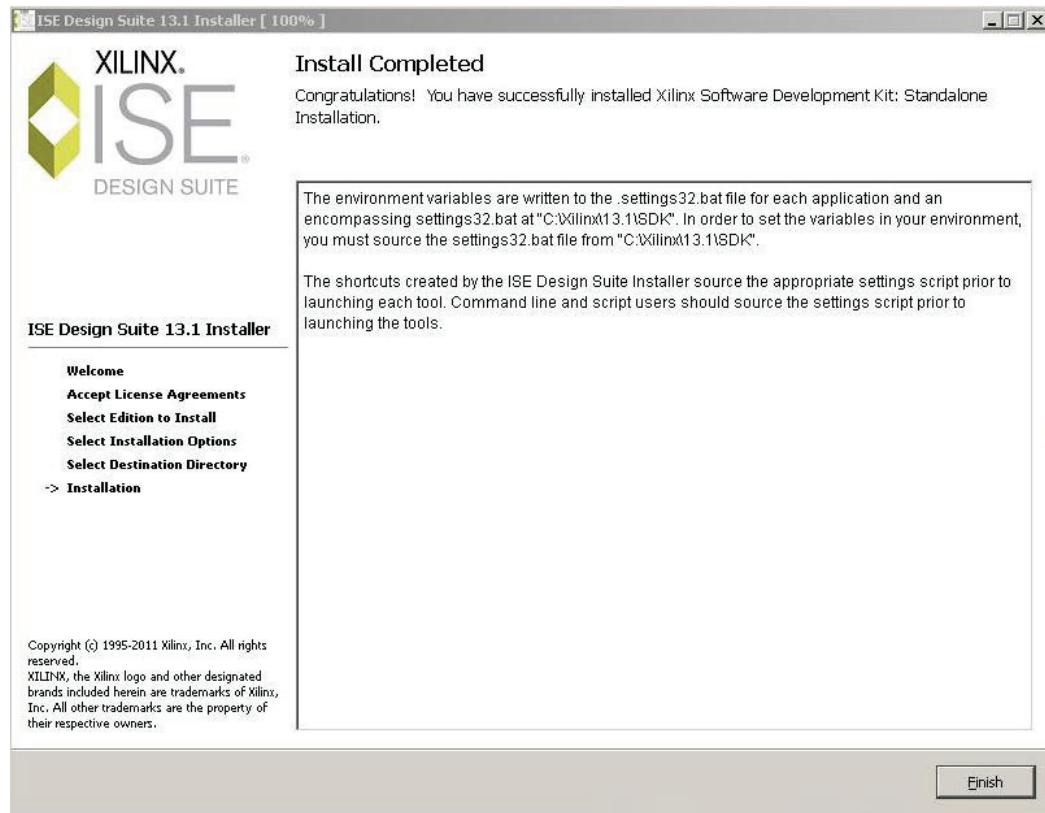


Figure 11: Installation Completed

4. Click **Close** to exit the Xilinx License Configuration Manager. The license for the software will be acquired in [Downloading and Installing Tool Licenses, page 25](#).
5. Exit the installation.
6. Reboot the computer.

Downloading and Installing Tool Licenses

1. Visit the Xilinx software registration and entitlement site at
<http://www.xilinx.com/getproduct>.
2. This launches your Web browser and takes you to the Xilinx product download and licensing site ([Figure 12](#)).

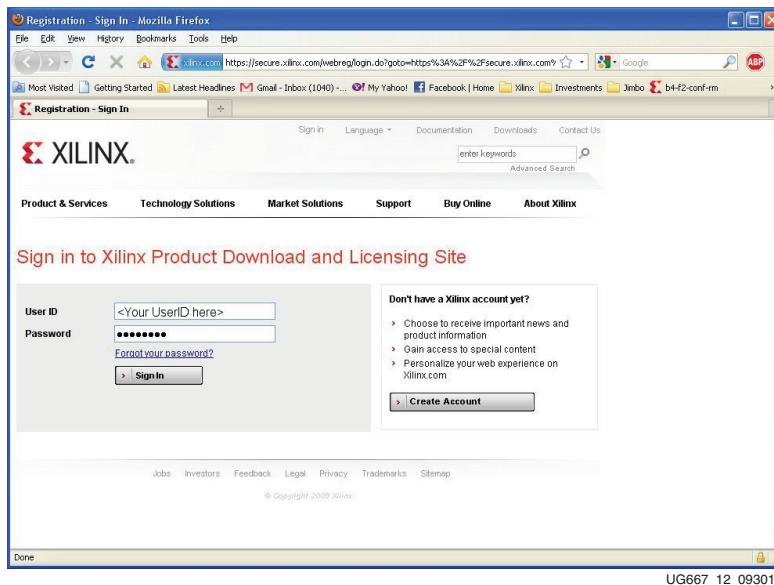


Figure 12: Sign In to Xilinx Product Download and Licensing Site

3. Log in if you already have an existing account or create an account if needed.
Note: Your user name and password are provided in an e-mail sent when you ordered the kit. If you do not have this e-mail, or have lost this e-mail, please contact Xilinx customer support. They will be able to provide you with the support to access your account
<http://www.xilinx.com/support/techsup/tappinfo.htm>.
4. After logging in, you may be requested to verify your shipping address. Click **Next** after the shipping address has been verified or updated.

5. Check the product **ISE Design Suite Embedded Spartan-6 LX45T Device Locked Edition** and click on **Generate Node-Locked License** as shown in [Figure 13](#).

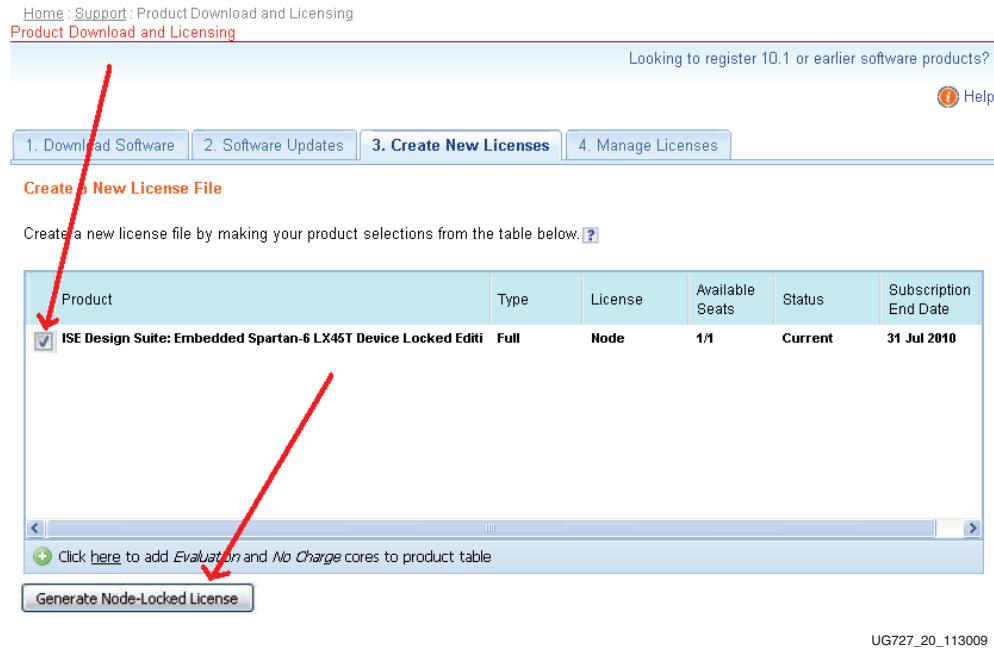


Figure 13: Xilinx Entitlement Center

6. Follow the instructions to generate the license by providing your Host OS information and Host ID (Disk Serial number or Ethernet MAC address) as shown in [Figure 14](#) and click **Next**.

Note: Laptop users can select their Disk ID or Wireless Ethernet card HostID. Laptops on docking stations have three Ethernet HostIDs to choose from. If you select a docking station HostID, then you only have a license when you are docked. It is best to avoid the HostID of your RJ45 Ethernet connection on Laptop computers, as some Ethernet adapters power down when not plugged into the network. If you do select an Ethernet adapter, it is best to select your wireless card.

Generate Node License
Fields marked with an asterisk * are required.

1 PRODUCT SELECTION

Product Selections *	Product	Type	Available Seats	Subscription End Date	Requested Seats
<input checked="" type="checkbox"/>	ISE Design Suite: Embedded Spartan-6 Full	1/1	1	31-Jul-2010	1

2 SYSTEM INFORMATION

License	Node
Host ID * ?	<Your Host> Windows 32-bit - Disk - 06356ab

3 COMMENTS

Comments ?	Spartan-6 FPGA Embedded Kit Device Locked License
------------	---

Next **Reset** **Cancel**

UG667_14_093010

Figure 14: Selecting Your Host ID

7. Review your license request as show in [Figure 15](#) and click **Next**.

Generate Node License

4 REVIEW LICENSE REQUEST

Product Selections			
Product	Subscription End Date	Available Seats	Requested Seats
ISE Design Suite: Embedded Spartan-6 LX45T Device	31-Jul-2010	1/1	1

License	Node
Host ID	566356ab

Previous **Next** **Cancel**

UG667_15_093010

Figure 15: Reviewing Your License Request

8. The generated license is e-mailed to you in an E-mail similar to the one shown in Figure 16.

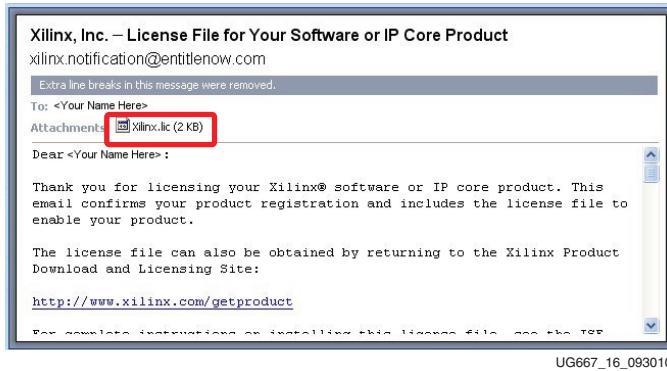


Figure 16: Xilinx License Notification E-mail

9. Start the Xilinx License Manager (**Start → Programs → ISE Design Suite 13.x → Manage Xilinx Licenses**) and click on **Copy License** to install the license on your computer (see Figure 17).

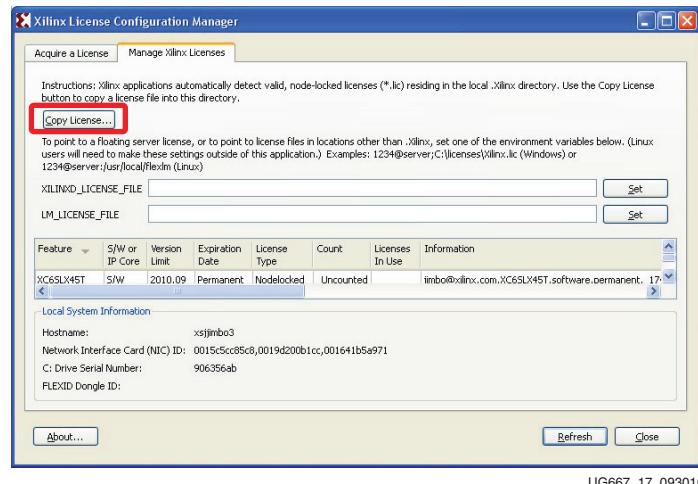


Figure 17: Manage Xilinx License Tab

10. Navigate to the location where the Xilinx.lic file was saved and select it. See Figure 18.

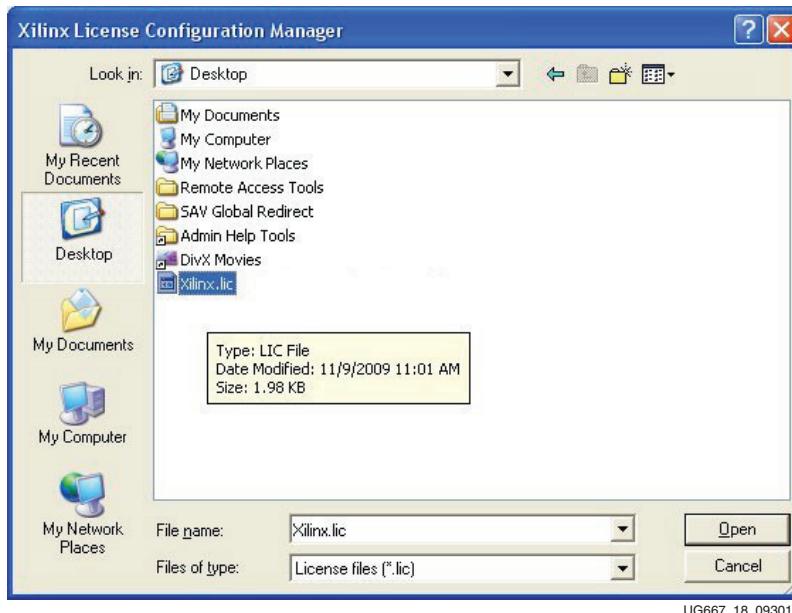


Figure 18: Select the xilinx.lic File

11. The ISE software license has now been successfully installed. Click **OK** on the Success Dialog (Figure 19) and close the Xilinx License Configuration Manager.

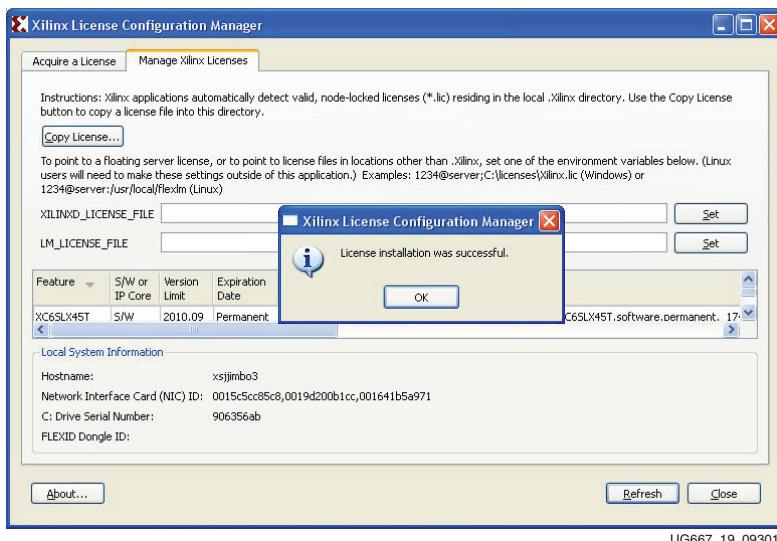


Figure 19: License Installation Successful

At this point in the tutorial The ISE Design Suite 13.x tools have been installed and the licenses set up for the Embedded Edition of the tools. You are now ready to use Xilinx ISE Design Suite 13.x Embedded Edition to create or modify your custom Embedded Systems using the MicroBlaze soft processor.

For detailed information on licensing & installation, please refer the following guide:
http://www.xilinx.com/support/documentation/sw_manuals/xilinx12/irn.pdf.

Communicating with the SP605 USB-UART

Installing the USB-UART driver

1. Execute the installer for the Silicon Labs USB-UART Virtual COM Port (VCP) driver from the `Drivers_and_Tools` folder on the USB drive shipped with your SP605 Embedded Kit.

`Drivers_and_Tools\CP210x_VCP_Win2K_XP_S2K3.exe`

2. Follow the installer instructions. Restart the computer when instructed to do so.

Connecting to the SP605 UART

1. Connect a USB Type-A to Mini-B 5-pin cable between the SP605 USB-UART connector (J23) and the host computer.
2. Power on the SP605 Evaluation Board if it is not already powered on.

Configuring the Host Computer

1. Right-click on **My Computer** and select **Properties**. Select the **Hardware** tab. Click on **Device Manager**.
2. Expand the **Ports (COM & LPT)** entry as shown in [Figure 20](#). This shows the COM port assigned to the Silicon Labs CP210x USB to UART bridge. This is the COM port to use in the serial communications program.

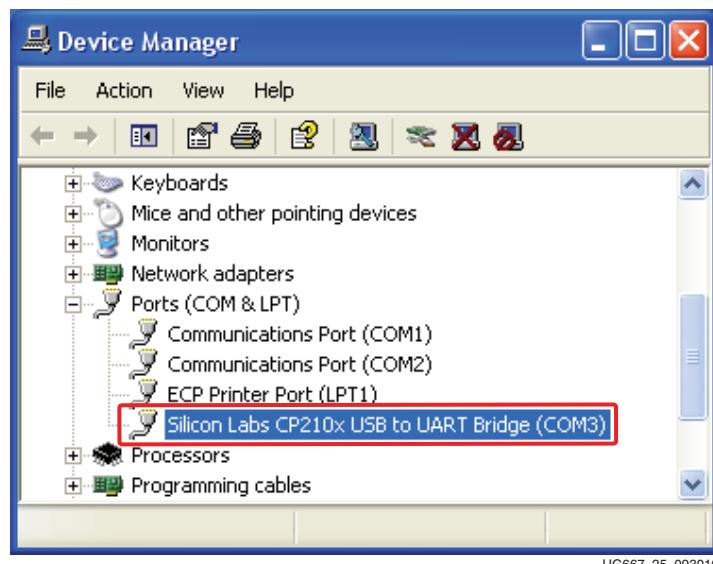
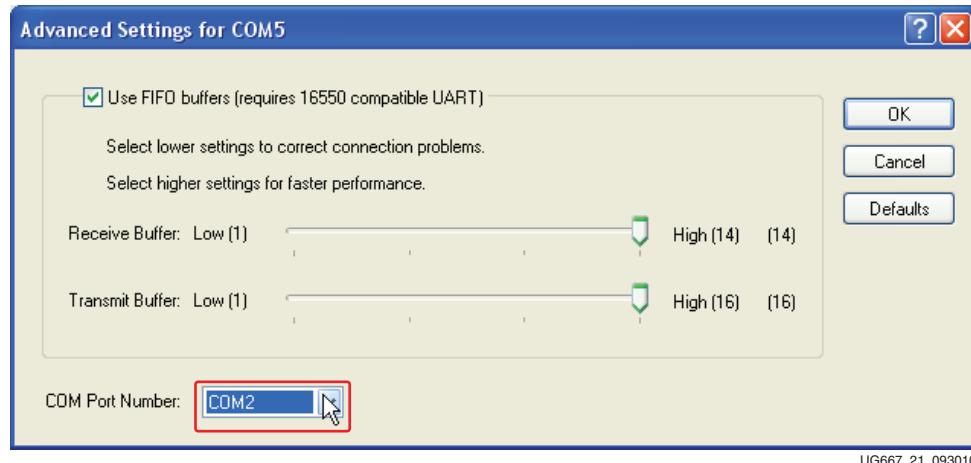


Figure 20: Silicon Labs USB to UART Bridge Properties

Note: If the Silicon Labs CP210x USB to UART bridge does not appear in the Ports list, a reboot of the computer might be required. After rebooting, repeat step 5 and step 6.

3. If using TeraTerm as the serial communications utility program, right-click on the **Silicon Labs CP210x USB to UART bridge** and select **Properties**.
 - a. Click on the **Port Settings** tab and then click **Advanced**.
 - b. Set the COM port to an open COM port setting from COM1 to COM4. Note that the COM port setting for your system may not be the one shown in [Figure 21](#).



UG667_21_093010

Figure 21: Setting the COM port for the Silicon Labs USB to UART Bridge Driver

4. Click **OK** to exit all open windows.

Testing the USB-UART Driver Installation

5. Start a serial communication program like HyperTerminal or TeraTerm on the Host PC with the following settings:
 - Baud Rate: **9600**
 - Data Bits: **8**
 - Parity: **None**
 - Stop Bits: **1**
 - Flow Control: **None**
6. Set the SystemACE DIP switches shown in [Figure 2](#) and listed in [Table 2](#).

7. Press the SYS ACE RESET button (SW9) shown in [Figure 22](#) to re-load the Benchmarking Demo. Make sure the Compact FLASH card is still inserted.

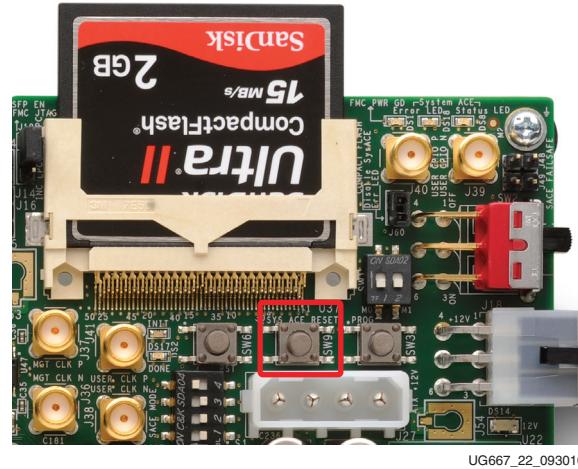


Figure 22: SP605 SYSACE RESET Button

8. After a lapse of 1 to 5 seconds, the output shown in [Figure 23](#) should be displayed on the serial communication window.

```
*****
**      Xilinx Embedded Kit Web server Demo      **
*****
Initializing MFS at 0x4013C4A4
Done.
Located index.html
Starting XILKERNEL.
initialize LWIP
create network_thread

-----lwIP Socket Mode Demo Application -----
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1

Server   Port Connect With...
http server    80 Point your web browser to http://192.168.1.10
auto-negotiated link speed: 1000
```

UG667_23_111210

Figure 23: Serial Communication Window Output

The Silicon Labs USB-UART Virtual COM Port (VCP) driver has now been installed.

Next Steps

Now that you have run through an FPGA-based Embedded Processor demo and installed the ISE Design Suite Embedded Edition, you are ready to create custom embedded systems for the Spartan-6 LX45T FPGA.

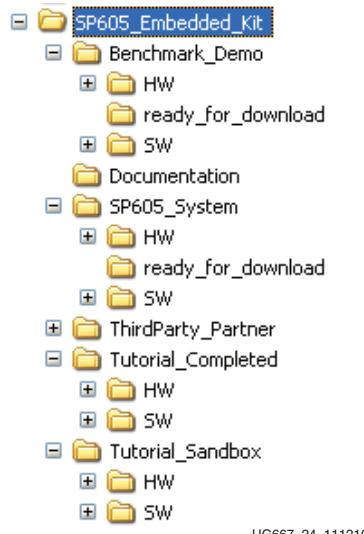
The following section provides pointers to various tutorials and reference designs that will help you become familiar with the Embedded Hardware and Software tools needed to customize MicroBlaze designs.

All material below can be found in the USB Stick provided with this Embedded Kit or under the Reference Designs section from the Spartan-6 Embedded Kit home page:
<http://www.xilinx.com/s6embkit>

Figure 24 is a snapshot of the directory structure you will find in the SP605_EMBEDDED_Kit folder on the USB stick included in the Embedded Kit or the zip file from the Embedded Kit web page. It is recommended that you copy the contents of the USB stick to a working area on your host computer.

Caution! Ensure that there are no spaces in the path name of the working area on your host computer.

The SP605_EMBEDDED_Kit directories and their content are explained in [Table 3](#).



UG667_24_111210

Figure 24: SP605 Embedded Kit Directory Structure

Table 3: SP605 Embedded Kit Directory Structure Contents

Directory	Purpose
Documentation	Includes the data sheet, tutorials, and other supporting documentation provided with this Embedded Kit.
SP605_System	Base MicroBlaze Processor Subsystem including the software applications and platforms.
Tutorial_Completed	Final state of files after the Hardware and Software Tutorials have been completed.
Tutorial_Sandbox	Working directory to use for executing the Hardware and Software Tutorials. Perform the tutorials in this directory.

Table 3: SP605 Embedded Kit Directory Structure Contents (Cont'd)

Directory	Purpose
Benchmark_Demo	Base MicroBlaze Processor System with the cores for CDMA benchmarking. Source files for the benchmarking demo are included here.
ThirdParty_Partner	Includes demos from third party partners.

Data Sheet

DS667 AXI Interface Based SP605 Embedded Kit MicroBlaze Processor Subsystem Data Sheet

- Documentation\ds667_SP605_MicroBlaze_Processor_SubSystem_datasheet.pdf
- Detailed data sheet documentation of the MicroBlaze Processor Subsystem including block diagram, address map, and system configuration.

Tutorials

UG670 AXI Interface Based ML605/SP605 MicroBlaze Processor Subsystem Software Tutorial

- Documentation\ug670_SP605_software_tutorial.pdf
- This tutorial guides the user through the steps to start software development using Xilinx SDK (Eclipse IDE) and the MicroBlaze Processor Subsystem.
- This shows the user how to create stand-alone (no OS) programs from simple Hello World designs to a more complex Board Test program.
- This also describes the software for the benchmarking demonstration that is included with the kit.

UG669 AXI Interface Based ML605/SP605 MicroBlaze Processor Subsystem Hardware Tutorial

- Documentation\ug669_SP605_hardware_tutorial.pdf
- This tutorial guides the user through the steps to open the MicroBlaze Processor Subsystem using Platform Studio and add the cores necessary for measuring CDMA throughput to recreate the out-of-the-box embedded kit demo.

Reference Designs

MicroBlaze Processor Subsystem

- SP605_System
 - This is the base MicroBlaze Processor Subsystem including the software applications and platforms.

MicroBlaze Processor Subsystem with Benchmarking Demo

- Benchmark_Demo
 - This is the MicroBlaze Processor Subsystem with the benchmarking cores that were run as the power-on demo. Source files for the demo including the software application and platform are included here.

Getting Help and Support

For questions regarding products within your Product Entitlement Account, send an e-mail message to your regional Customer Service Representative:

- Canada, USA and South America - isscs_cases@xilinx.com
- Europe, Middle East, and Africa - eucases@xilinx.com
- Asia Pacific including Japan - apaccase@xilinx.com

For technical support including the installation and use of your product license file you may contact Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

- Software, IP and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training - Select instructor-led classes and recorded e-learning options

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes: (i) engineering samples or beta versions of Development Systems (which are provided "AS-IS" without warranty); (ii) design defects or errors known as "errata"; (iii) Development Systems procured through unauthorized third parties; and (iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

THE WARRANTIES SET FORTH HEREIN ARE EXCLUSIVE. XILINX DISCLAIMS ALL OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT, AND ANY WARRANTY THAT MAY ARISE FROM COURSE OF DEALING, COURSE OF PERFORMANCE, OR USAGE OF TRADE. (2008.10)



Do not throw Xilinx products marked with the "crossed out wheelie bin" in the trash. Directive 2002/96/EC on waste electrical and electronic equipment (WEEE) requires the separate collection of WEEE. Your cooperation is essential in ensuring the proper management of WEEE and the protection of the environment and human health from potential effects arising from the presence of hazardous substances in WEEE. Return the marked products to Xilinx for proper disposal. Further information and instructions for free-of-charge return available at: <http://www.xilinx.com/ehs/weee.htm>.

