WebPHY

DATABUS v1.1

May 2013 **Product Specification**

Introduction

WebPHY-*DATABUS*™ provides a drop-in web interface IP core for command and control of FPGA applications. An on-FPGA web page can be customized by the user to create buttons, text boxes and other HTML/Javascript objects enabling a built-in FPGA GUI, tailored to the user's application. The core can also be controlled by web-clients from non-browser, custom software applications. The core implements HTTP/TCP/IP/ ARP/MAC layers and features a built-in PHY allowing direct connection of FPGA's LVDS I/O to Ethernet equipment using only resistors, capacitors and a RJ-45 mag-jack. The core can be accessed via LAN or over the internet when connected to a router with properly configured port address translation.

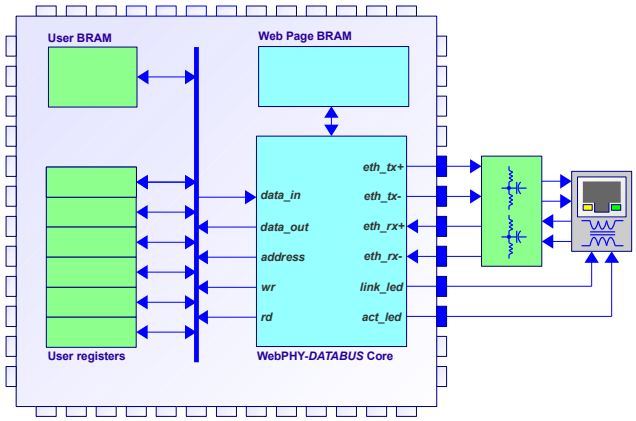

Fig. 1 – WebPHY-DATABUS connects to web page BRAM, user's data bus, and directly to Ethernet, enabling web control of user applications.

Features

- Drop-in IP core – no CPU or software TCP stack required
- User customizable web-page GUI
- Compatible with Firefox, Internet Explorer, Chrome, Safari and Dolphin web browsers and IPhone, IPAD, Android, and Windows platforms
- De-layered and co-optimized stack implementation for ultra-small footprint
- Available for Xilinx and Altera FPGAs

Applications

- Internet/LAN control and monitoring of FPGAs
- Host-FPGA Interface
- FPGA Graphical User Interface
- Low-cost applications

IP Core Facts Table				
Provided with Core				
Documentation	User Manual			
Design Files	NGC File			
Example Design	Example register/mux/BRAM bus			
Resources				
FPGA	FFs	LUTs	Block RAMs	f_{clk}
Spartan3 XC3S400	1,379 (19%)	1,692 (23%)	3 RAMB16s (18%)	80 MHz

Overview

The WebPHY-*DATABUS*™ FPGA Core implements a web-server which receives data for the user via a web-client such as a PC running Firefox, and responds with user data, in accordance with the request-response model of the HTTP protocol. Together with the rest of the stack layers, this enables a reliable data link between a host such as a PC and the user's FPGA using a standard web browser. All layers from HTTP down to the PHY are implemented in the core. A 10Base-T PHY is built into the core requiring only resistors, capacitors, a mag-jack, and FPGA LVDS I/O to connect directly to Ethernet equipment such as PC NIC cards and Ethernet switches. This capitalizes on the mandatory requirement in 1000Base-T Ethernet specifications for auto-negotiation down to 10Base-T, and guarantees interoperability with virtually any NIC or switch. MII and GMII versions of the core are also available for use with external 100/1000Base-T PHYs.

User data bus timing

DATABUS acts as a bus master, driving data, address and wr for writes, and driving rd and reading data for reads. A read acknowledgment is used to allow for latency in the user's read-back logic.

TCP/IP Support

A light-weight TCP/IP stack is implemented to support the DATABUS/HTTP application. Packets sent from the core to the client are retransmitted in the event of acknowledgment timeout from the web-client. Incoming packets from the web-client which fail Ethernet CRC or TCP check-sum are discarded. This provides the reliability mechanism offered by TCP/Ethernet while consuming minimal FPGA resources.

Web Interface

The web page uses Javascript and HTML code to read data from and write data to the user's address space. The user can customize the web page to add buttons and other HTML/JavaScript objects to read or write specific data and addresses for specific user functions. All that is required is that the web page send commands to the core using the two specified ASCII read and write string formats shown in the following examples:

```
wr 0x00 0x1234
rd 0x00 0x02
```

The web page is stored in FPGA block memory and has a maximum size of 64K Bytes. Gzip compression can be used to improve space efficiency. The page shipped with the core, shown below, uses Gzip compression and requires approximately 1.7K Bytes of BRAM:

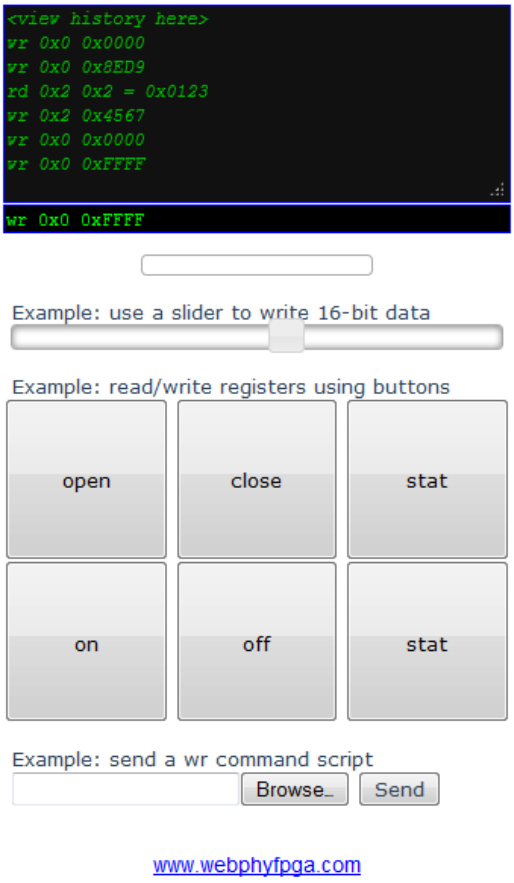

Fig. 2- Example web page shipped with core can be customized by user