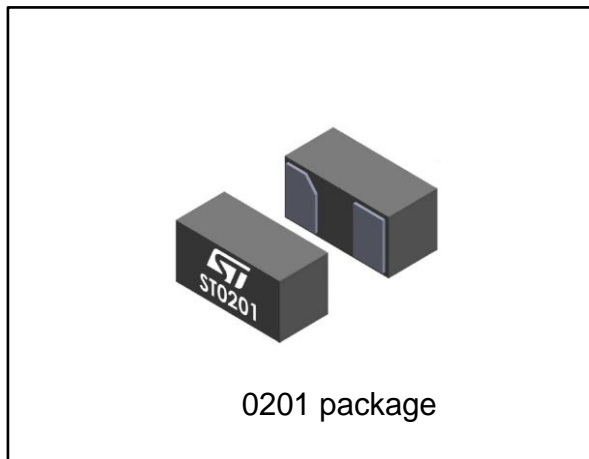


Low clamping single line unidirectional ESD

Datasheet - production data



Features

- Low clamping voltage:
 - -3 V / +9 V (IEC 61000-4-2 contact discharge at 30 ns)
- Unidirectional device
- Low leakage current
- 0201 package
- ECOPACK®2 compliant component

Complies with the following standards

- IEC 61000-4-2, level 4 (exceed level 4)
 - ±30 kV (air discharge)
 - ±30 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

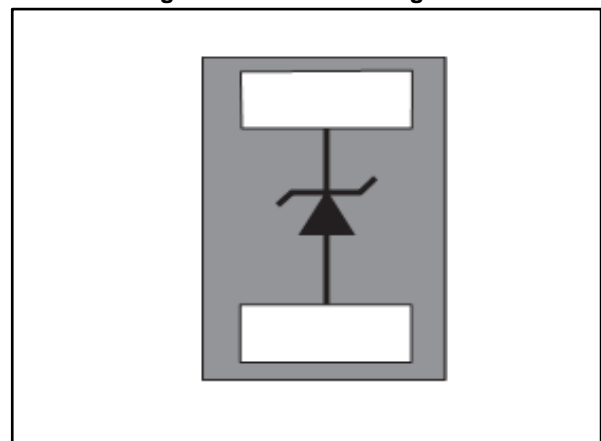
- Smartphones, mobile phones and accessories
- Tablet, PC, netbooks and notebooks
- Portable multimedia devices and accessories
- Digital cameras and camcorders
- Communication and highly integrated systems

Description

The ESDA5-1F4 is a unidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

Figure 1: Functional diagram

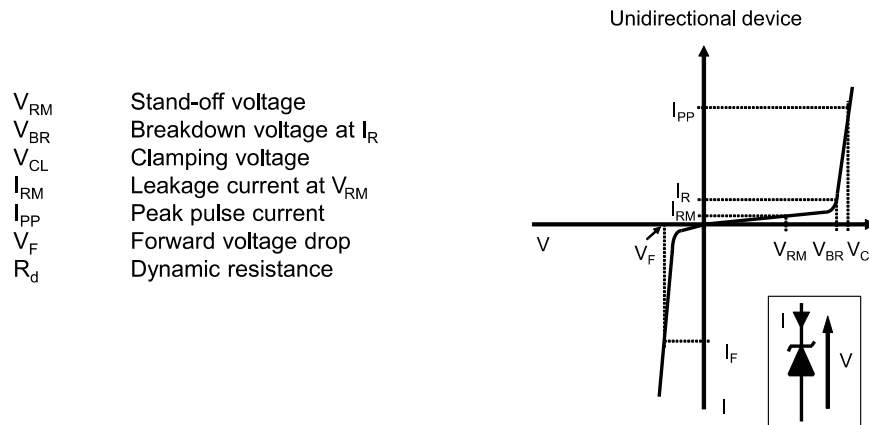


1 Characteristics

Table 1: Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC61000-4-2 contact discharge	± 30	kV
		IEC61000-4-2 air discharge	± 30	
P_{pp}	Peak pulse power (8/20 μ s)		110	W
I_{pp}	Peak pulse current (8/20 μ s)		11	A
T_j	Operating junction temperature range		-55 to +150	$^{\circ}\text{C}$
T_{stg}	Storage junction temperature range		-65 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 2: Electrical characteristics (definitions)

Table 2: Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage	$I_R = 1\text{ mA}$	5.8			V
V_{RM}	Reverse working voltage				5.5	V
I_{RM}	Leakage current	$V_{RM} = 5.5\text{ V}$			100	nA
V_{CL}	Clamping voltage	IEC 61000-4-2, +8 kV contact measured at 30 ns		9.0		V
		IEC 61000-4-2, -8 kV contact measured at 30 ns		-3.0		V
R_d	Dynamic resistance, pulse duration 100 ns ⁽¹⁾	Direct		0.17		Ω
		Forward		0.14		
C_{LINE}	Line capacitance	$V_{LINE} = 0\text{ V}$, $F = 1\text{ MHz}$, $V_{OSC} = 30\text{ mV}$		110		pF

Notes:

⁽¹⁾More information are available in ST application note: AN4022

1.1 Characteristics (curves)

Figure 3: Variation of leakage current versus junction temperature (typical values)

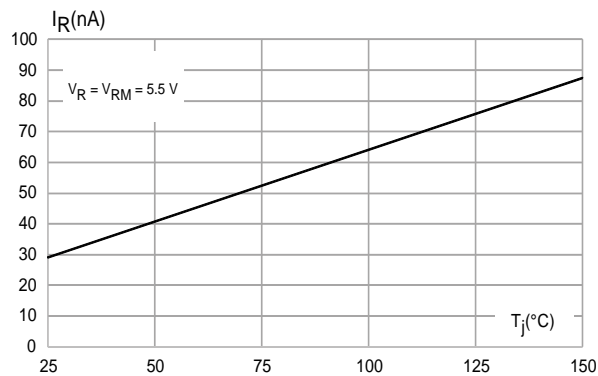


Figure 4: Junction capacitance versus frequency (typical values)

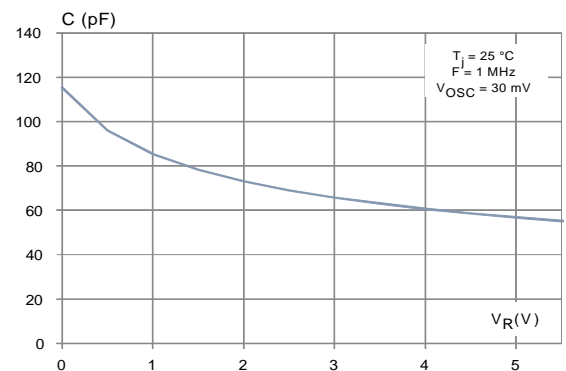


Figure 5: ESD response to IEC61000-4-2 (+8 kV contact discharge)

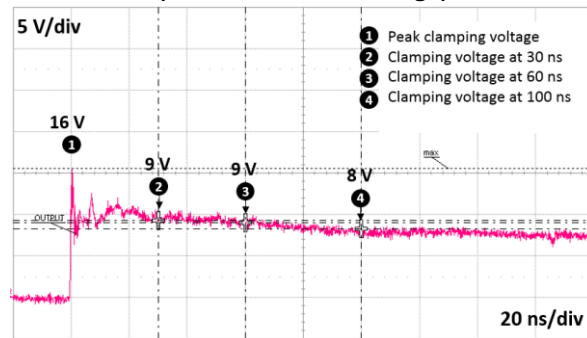


Figure 6: ESD response to IEC61000-4-2 (-8 kV contact discharge).

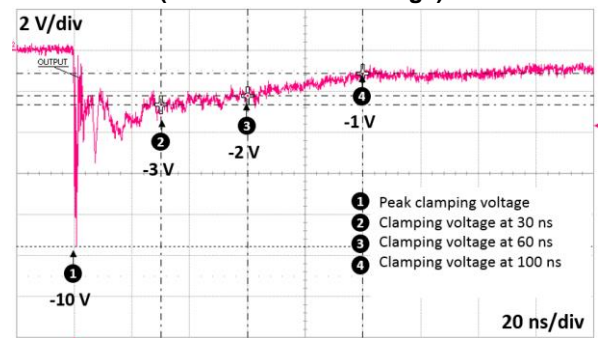


Figure 7: Dynamic resistance (TLP conditions)

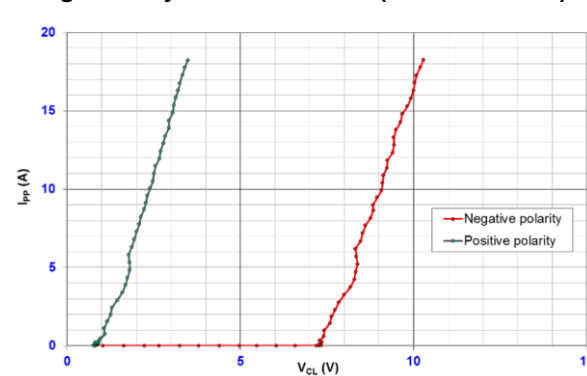
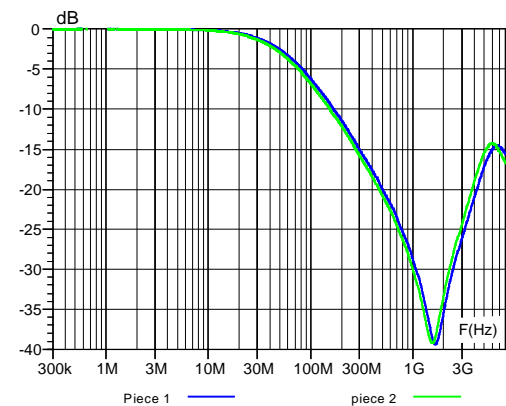


Figure 8: S21 attenuation measurement result



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 0201 package information

Figure 9: 0201 package outline

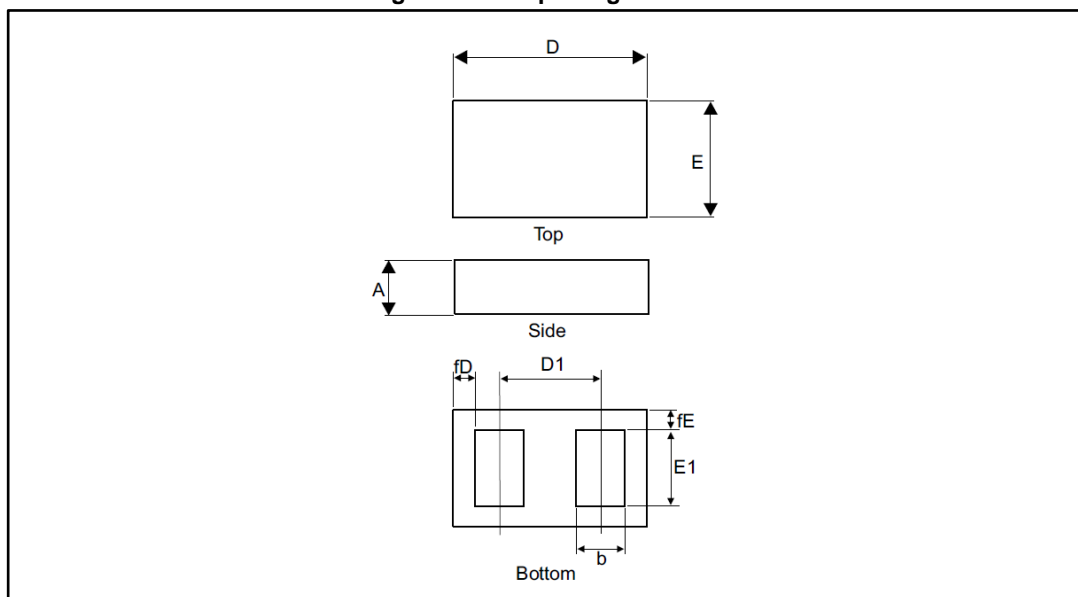
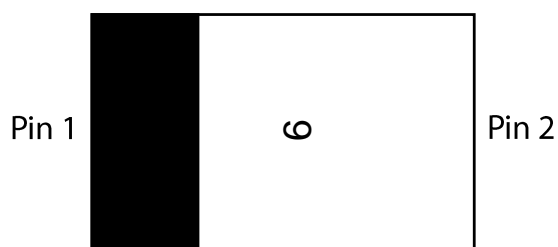


Table 3: 0201 package mechanical data

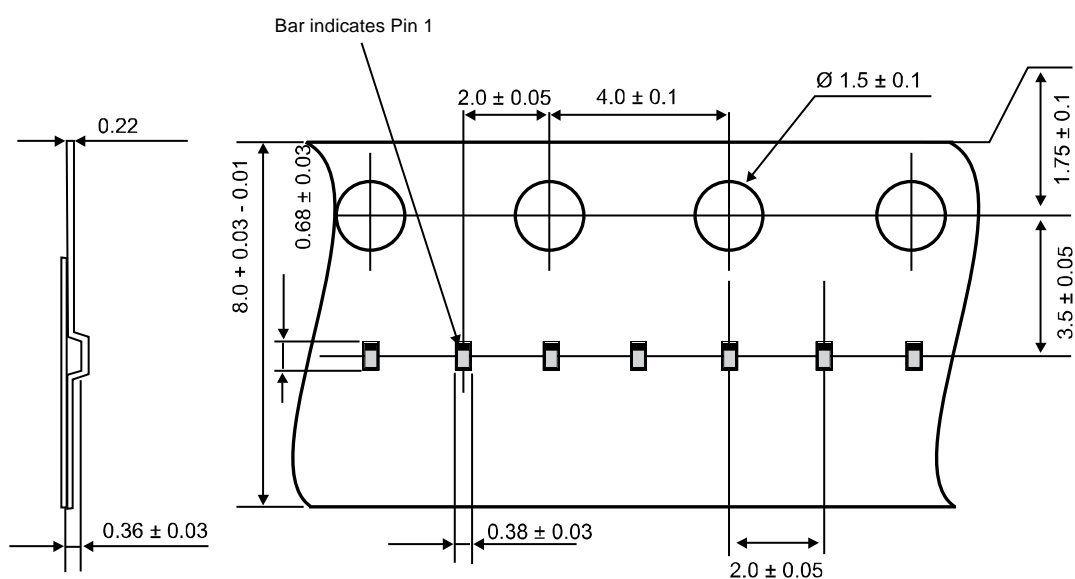
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.280	0.300	0.320	0.011	0.0118	0.0126
b	0.125	0.140	0.155	0.0049	0.0055	0.0061
D	0.570	0.600	0.630	0.0224	0.0236	0.0248
D1		0.350			0.0138	
E	0.270	0.300	0.330	0.0106	0.0118	0.0130
E1	0.175	0.190	0.205	0.0069	0.0075	0.0081
fD	0.110	0.125	0.140	0.0043	0.0049	0.0055
fE	0.040	0.055	0.070	0.0016	0.0022	0.0028

Figure 10: Marking



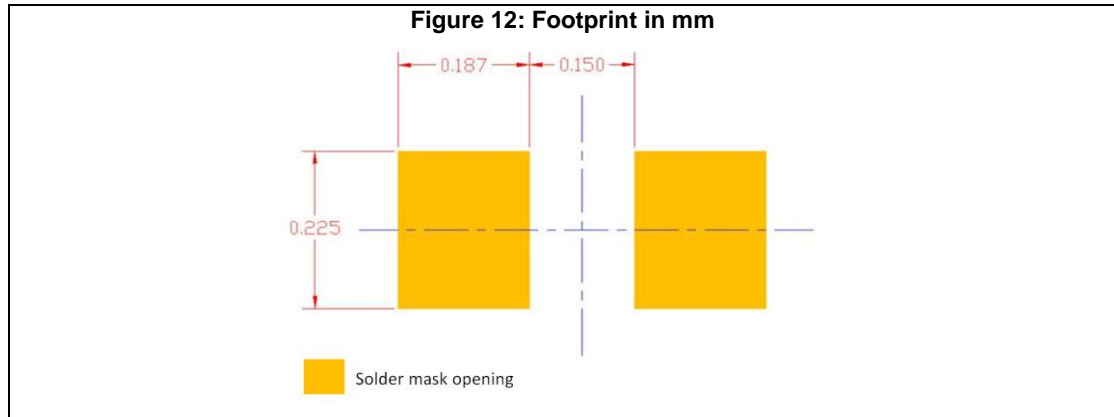
Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 11: Tape and reel specification (in mm)



3 Recommendation on PCB assembly

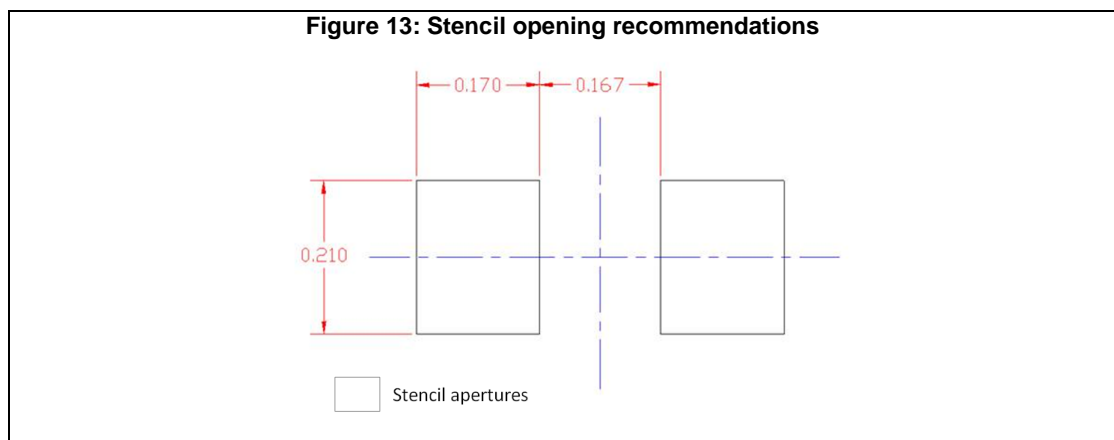
3.1 Footprint



1. SMD footprint design is recommended.

3.2 Stencil opening design

1. Recommended design reference
 - a. Stencil opening thickness: 75 μm / 3 mils



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-38 μm .

3.4 Placement

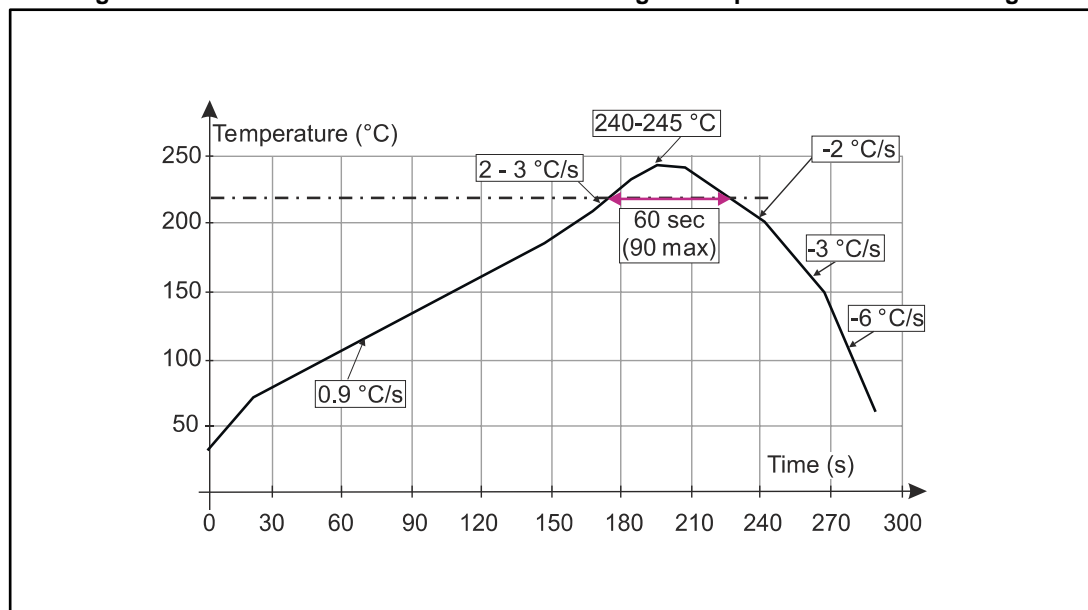
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.6 Reflow profile

Figure 14: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 15: Ordering information scheme

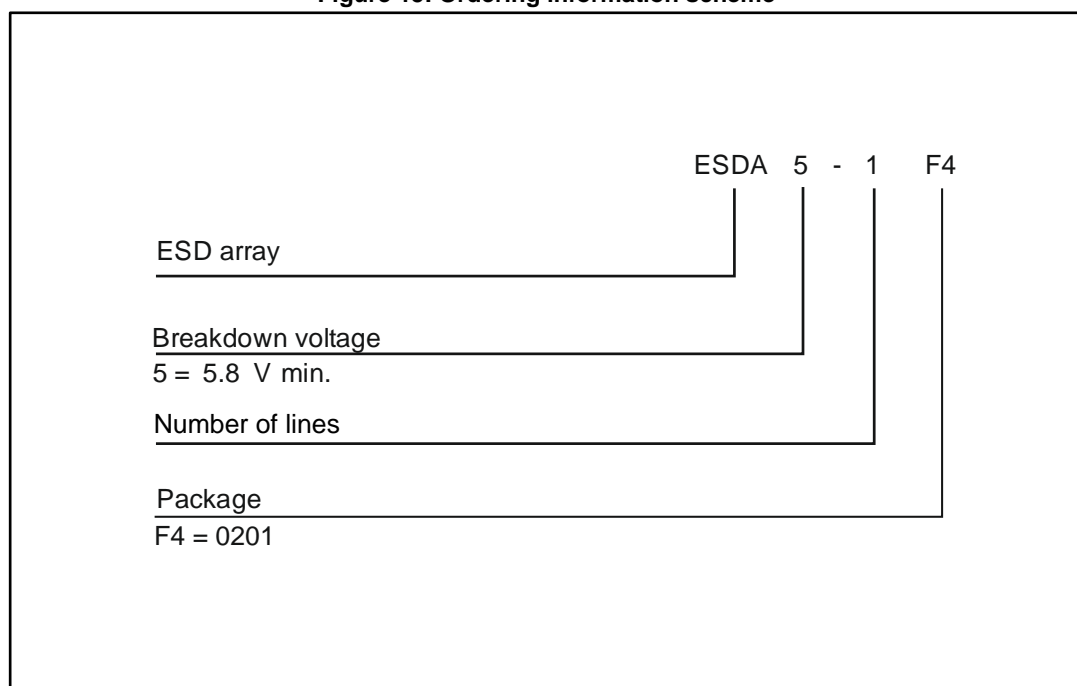


Table 4: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDA5-1F4	6	ST0201	0.116 mg	15000	Tape and reel

5 Revision history

Table 5: Document revision history

Date	Revision	Changes
02-May-2017	1	Initial release.

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