HETEROGENEOUS INTEGRATION ROADMAP

2021 Edition

Chapter 22: Interconnects for 2D and 3D Architectures

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Chapter 22: Interconnects for 2D and 3D Architectures

Executive Summary

With increasing interest in on-package Heterogeneous Integration (HI), there is a need to describe package architectures and their interconnect capabilities in a simple and consistent manner. This chapter has two primary objectives: to (a) define and proliferate a new standardized nomenclature for package architectures covering and clearly demarcating both 2D and 3D[1] constructions, and to (b) define and proliferate key metrics driving the evolution of the physical interconnects in these architectures.

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1. Introduction

Moore's Law has paced the growth of the microelectronics industry for the last 50 years by providing a template for silicon scaling and homogeneous SoC (System on Chip) integration of different IP. Moving forward, HI, enabled by changes in the physical, electrical, thermal and thermo-mechanical attributes of packages and micro-systems increasingly complements Moore's Law to provide improved functionality [1, 2]. Current and new advanced package architectures are major enablers in sustaining and enhancing growth in the micro-electronics industry [3-13]. These architectures enable novel heterogeneous SiP (System in Package) configurations for cost-performance optimized micro-electronics systems. A number of products that use advanced HI have been announced in recent years attesting to the importance of this field [14-19].

Historically, the primary purpose of the package for homogenous integration was to provide mechanical protection for the die, space transformation for silicon features, form-factor scaling, low-parasitic power-delivery, efficient power removal, and low loss, high bandwidth signaling. Innovations in packaging for homogeneous SoCs focused on enabling silicon size scaling, power, performance, and latency while maximizing performance opportunities made possible by Moore's Law. During the period where the primary focus was homogeneous integration, MCPs (Multi-Chip Packages) were used primarily for improved time-to-market and for critical HI needs (e.g., DRAM integration).

Industry trends today show an increasing need for HI driven by a need to add diverse functionality (often realized with different IP on silicon nodes from multiple different suppliers), improved silicon yield resiliency, and the continued need for rapid time to market. 2D and 3D package architectures are ideal heterogeneous integration platforms because they provide short, power-efficient, high-bandwidth connections between components in compact form factors. Today's heterogeneous packaging technologies:

- Deliver power-efficient, high-bandwidth on-package IO links using various communication protocols
- Enable a diversity of off-package IO protocols
- Deliver noise isolation for single-ended and differential on-package and off-package signaling
- Manage increasing cooling demands
- Support complex power delivery architectures
- Meet diverse application functionality, form factor and weight constraints ranging from high-performance servers to flexible, wearable electronics
- Meet a broad spectrum of reliability requirements for different market segments and applications
- Provide cost effective, high-precision and quick-turn assembly to meet fast production ramps

In this respect they differ from packaging for homogeneous integration in terms of increased complexity and the increased focus on on-package bandwidth. Developing products using advanced packaging requires an integrated approach involving collaboration with product architects, system architects, process engineers, materials engineers, and reliability engineers, and a detailed understanding of the fundamental thermal, mechanical, electrical and materials characteristics of the various architectures.

2. Scope

This roadmap chapter has a two-fold purpose:

- Define and proliferate a standardized nomenclature for package architectures covering, and clearly demarcating, both 2D and 3D constructions. Currently there are a number of intermediate definitions between 2D and 3D constructions, referred to as 2.xD architectures. Experts in this road-mapping effort,

[1] Scope of this chapter is restricted to electrical interconnects between one or more semiconductor devices.

representing a wide spectrum of industry, academia, and consultants, agree that the current nomenclature (e.g., 2.1D, 2.3D, 2.5D architectures) does not have a common rational basis and that there is a need to provide a comprehensive classification framework based on a common set of assumptions. The objective of this chapter is to drive clarity and provide a nomenclature framework that will house different architectures.

- Define and proliferate key metrics driving the evolution of the physical interconnects in these architectures. This chapter will list their current values (based on the state of the art) and projections for the next generations.

The chapter is organized into 4 primary areas:

- Converged Nomenclature Framework for 2D and 3D Architectures
- Key Metrics:[2]
  - Design Attributes
  - Electrical Attributes including Signal Integrity and Power Delivery
- Difficult Challenges
- Discussion

3. Converged Nomenclature Framework for 2D and 3D Architectures

a) A 2D architecture is defined as an architecture where two or more active silicon devices are placed side-by-side on a package and are interconnected on the package. If the interconnect is "enhanced", i.e., has higher interconnect density than mainstream organic packages, and is accomplished using an organic medium, the architecture is further sub-categorized as a 2DO (2D Organic) architecture; and similarly, if the enhanced architecture uses an inorganic medium (e.g., a silicon/glass/ceramic interposer or bridge), the architecture is further sub-categorized as a 2DS architecture. Architectures that include enhancements over and above traditional 2D architectures (typically 2 or more die flip-chip attached on a traditional organic package) are variously referred to as 2.x architectures to emphasize their specialness. These nomenclatures do not have any particular technical basis. It is proposed here that they all be broadly categorized as 2D enhanced architectures.

b) A 3D architecture is defined as an architecture where two or more active silicon devices are stacked and interconnected without the agency of the package.

The ideas described by this nomenclature[3] are schematically shown in Figure 1.

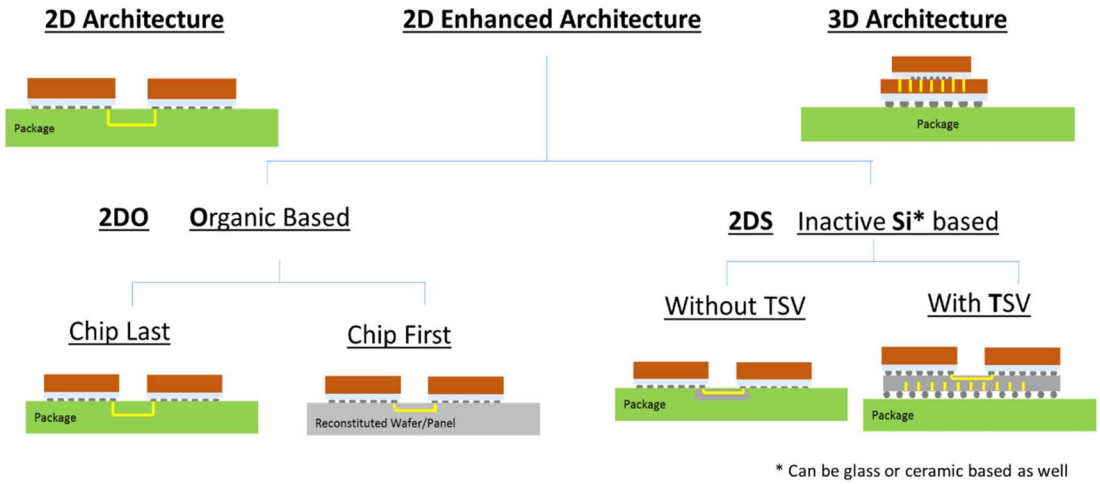


Figure 1: Schematic describing the Converged Nomenclature Framework for 2D and 3D Architectures. Note that the difference between the 2D and 2DO Chip Last schematic in this figure is in the interconnect density in the die-die links. The latter has increased interconnect density enabled by finer lines and spaces along with reduced-sized vias and via pads. In the 2DS images, the grey color is used for silicon (or glass)

[2] Other key attributes such as thermal and process attributes are covered in different chapters in this roadmap.

[3] Figure 1 only describes a nomenclature and technology equivalence is not intended or implied.

4. Interconnect Nomenclature

Package interconnects can be classified as:

a) **Die-Die Interconnects**: Interconnects between stacked die for vertical connectivity between multiple dies in a 3-D stack. These may be further sub-categorized using the process these interconnects are created with, which can lead to different physical attributes, such as Die-Die interconnects created using a:
- Wafer-to-Wafer attach process
- Die-to-Wafer attach process
- Die-Die attach process

The roadmap for these interconnects is described in Section 5.1.1.

b) **On-package Die-Die Interconnects**: i.e., 2D and Enhanced-2D Interconnects: Interconnects between die (and/or die stacks/pre-packaged die) within the package for lateral connectivity. The roadmap for these interconnects is described in Section 5.1.1.

c) **Die-to-Package Interconnects**: Interconnects between the die and the package (Figure 2), typically known as the first level interconnect (FLI).

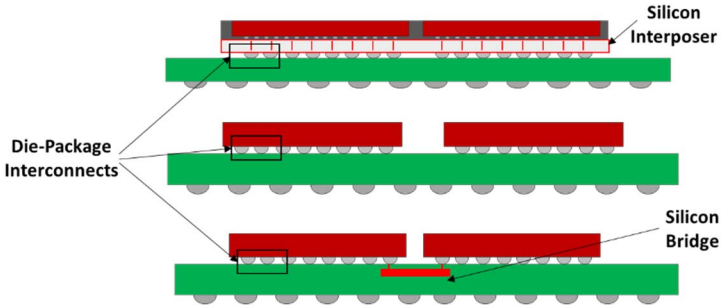


Figure 2: Schematic showing the die-package interconnects.[4]

The schematic in Figure 2 only shows area-array interconnects. Wire-bond interconnects are also an important die-to-package interconnect. Three types of wire bonding technologies, Au, Cu and Ag wire-based technologies, are widely used today. The finest in-line wire-bond pitch currently seen in high-volume manufacturing (HVM) remains at 40µm inline pitch and has been that way for the last few years. Wire-bonders are capable of supporting a minimum inline pitch of 35µm or 40µm staggered (dual row) pitch in HVM (Au, Cu, or Ag wire). Process advances in recent years have brought Cu-wire bonding capabilities just about on par with Au-wire bonding capabilities. Additionally, current bonders have successfully demonstrated 30µm inline pitch capability to provide an envelope covering potential near term demand. Table 1 shows the best-judged 5-year roadmap from leading wire-bond experts. For additional details on wire-bonding technology, including discussions on multi-tier stacking that allows for considerable innovations on heterogeneous integration, the reader is referred to the chapter on Single and Multi-Chip Integration in this roadmap [20].

Another key metric is the flip-chip pitch for area-array interconnects. Table 1 shows a 5-year roadmap for the traditional flip-chip pitch. Given that the pace of change is flat, it is reasonable to assume that the flip-chip pitch will stay at a minimum bound of 90µm (this does not cover the fine-pitch scaling available in enhanced 2D and 3D architectures).

Table 1: Die-Package Interconnect Pitch Roadmap

Year of Production	2018	2019	2020	2021	2022	2023	2024
Au Wire bond – single in-line (µm)	40	35	35	33	30	30	30
Cu wire – single in-line (µm)	40	35	35	33	30	30	30
Flip chip array, low end & consumer (µm)	150	150	130	130	130	130	130
Flip chip – cost performance (µm)	110	110	110	100	100	100	90
Flip chip – high performance (µm)	110	100	100	90	90	90	90

d) **Within-Package Interconnects**: Interconnects within the package that enable lateral connections between two or more die. Roadmap projections of within-package interconnects are not discussed in this chapter. The reader is referred to the chapter on package substrate technologies (Chapter 8).

[4] Note that the values discussed in this section do not include the case where the organic substrate is scaled to accept fine-pitch die stacks such as HBM @ 55µm, with and without EMIB. Since instances such as these are more relevant to die-die interconnects, they are discussed in Section 5.1.1.

e) **Package-to-Board Interconnects**: Interconnects between the package and the next level, which is typically the motherboard, are referred to as second-level interconnects (SLI). SLI connections are either socketed or ball grid array (BGA) and may be combined with on-package cabling[5]. The 2015 ITRS roadmap projections for socket pin counts are reproduced below [21] in Table 2a[6]. Figure 3 shows a trend graph based on how sockets have evolved. This exponential pin-count growth is expected for the near term, as shown in Figure 3. However, the effect of heterogeneous integration on the pin-count growth is yet to be comprehended for the long term. The 2015 ITRS projections are reasonable extrapolations for the cost-performance segment (minor changes are shown in Table 2b). For the high-performance segments, the projections look reasonable until ~2021 but seem to be under-projecting significantly after that. This is likely because the pin-count increase trend in the 2015 projections was assumed to be linear. Table 2b shows an updated projection for the high-performance segment using a combination of exponential and polynomial fits.

Table 2a: Socket pin count projections from 2015 ITRS. [21]

	2019	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*	*2029*	*2030*
Low-end, Low-cost package	550	550	550	600	600	600	600	600	650	650	650	650
Memory (MCP)	260	280	280	280	280	280	280	280	280	280	280	280
Cost-performance	3200	3300	3400	3500	3600	3700	3800	3900	4000	4100	4200	4300
Harsh	693	728	764	803	843	860	877	894	911	928	945	962
High performance	5394	5651	5934	6231	6543	6855	7167	7479	7791	8103	8415	8727

Table 2b: Updated projections for socket pin count in the Cost-Performance and High-Performance segments.

	2019	2020	2021	2022	2025	2028	2031	2034
Cost performance	3200	3300	3400	3500	3800	4100	4400	4700
High performance	5125	5694	6302	6946	9105	11601	14434	17604

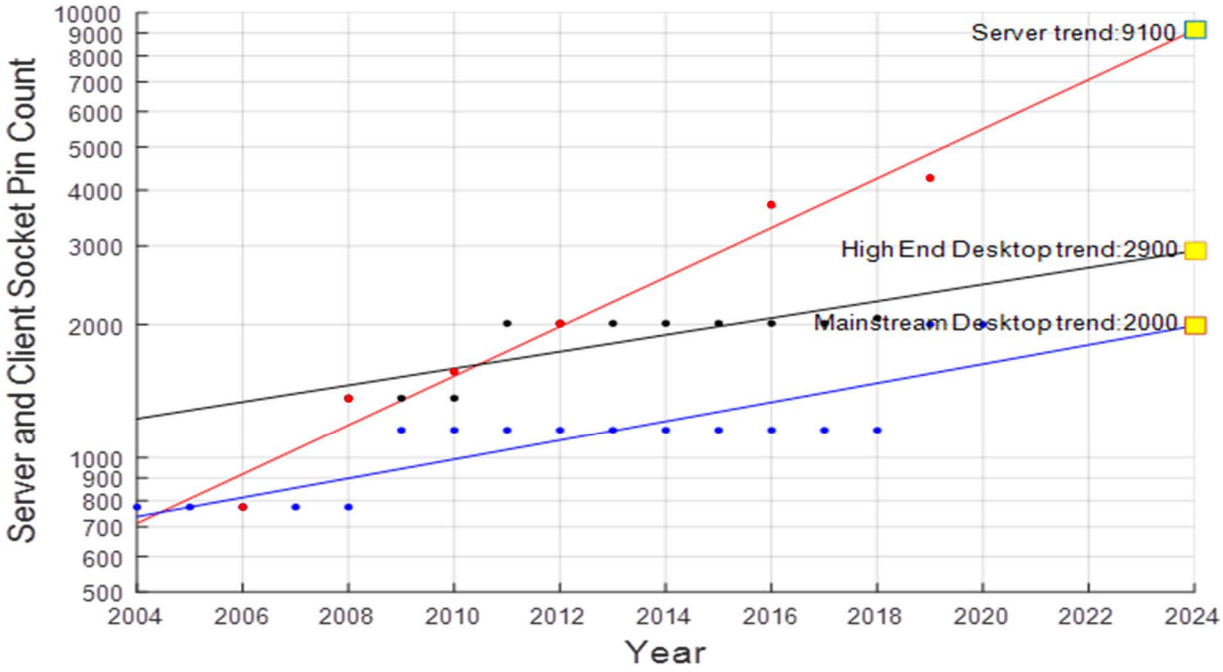


Figure 3: Near term trend graph based on actual pin count evolution. (Source: Intel)

[5] This chapter does not address on-package cabling solutions or provide a roadmap since this class of solutions is still maturing.

[6] The ball count for Mobile packages has been removed from this table. The 2015 projections show a flat trend, and this trend needs additional study in light of the current evolution of mobile products.

As described in [22], off-package bandwidth, electrical lane speeds and ASIC IO continue to scale steadily. In addition to pin-count changes, socket constructions that minimize signaling losses should be developed. 2015 ITRS projections for BGA[7] pitch continue to be valid.

f) **POP (Package-on-Package) Interconnects**: The PoP construction [23] allows for packages to be placed on top of other packages using peripheral package interconnects, also referred to as VI (Vertical Interconnects). It is typically used to stack memory packages on logic to create compact form factors. One such typical construction is shown in Figure 4.

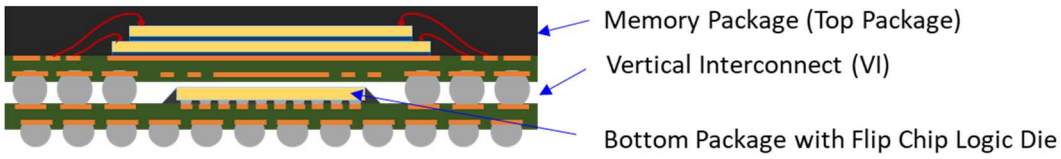


Figure 4: Typical Package-on-Package Architecture.

The VI pitch and the overall height of the package are two key characteristics for this architecture. Currently there is no methodology to project a roadmap for these architectures and in lieu of such a roadmap, the state-of-the-art pitches and package heights, along with their projected changes, are listed in Table 3.

Table 3: State-of-the-Art Pitches and Package Heights and their projected targets for PoP Architectures (Source: TechSearch International)

PoP Architectures	VI Pitch (mm)	Maximum Bottom Package Height (mm)
Bare Die PoP	0.5	0.75
Bare Die PoP with 2-Step solder resist (SR) + solder on pad (SOP)	0.4	0.75
TMV (**T**hrough **M**old **V**ia) PoP	0.4	0.78
Exposed Die TMV PoP	0.35 → 0.27	0.69
Interposer PoP	0.27 → 0.20	0.67
FOWLP PoP	0.30 → 0.20	0.50 → 0.30

5. Key Metrics

5.1 Design Attributes[8]

The physical attributes and signaling speeds needed to enable generation-over-generation BW doubling are described in this section.

5.1.1 Peripheral Interconnects for 2D and Enhanced-2D Architectures (see Figure 1)

A key role of packaging is to provide physical interconnects.[9] Two design metrics that describe capability of these interconnects are linear escape density and areal escape density. These two metrics are shown in Figure 5A. Note that these two can be combined into a single metric by multiplying the two (Figure 5B). The same metric has also been described by other researchers [24]. Tables 4-6 show possible ways of physical-interconnect scaling instead of mere signaling-speed scaling to achieve raw bandwidth doubling generation over generation. Such scaling can achieve aggressive bandwidth targets while keeping the signaling speeds relatively low, so that it is feasible to achieve a very low raw bit error rate (BER) such as 10^{-18}. This avoids the complicated error-correction circuits and minimizes the I/O latency. It is important to emphasize that the physical IO dimensions listed are not bounding parameters and depend on specific business and technical demands i.e., the same bandwidth doubling can be achieved through more- or less-aggressive choices of the physical IO dimensions.

[7] The focus in BGA interconnects and more broadly in other solder joints is on low-temperature solders to provide additional options within the reflow hierarchy and opportunities for reduced power usage during manufacturing (hence greater environmental friendliness). There is extensive literature in this area in recent years; however it is not covered in this chapter.

[8] 2D to 3D packaging architectures provide the physical construction architecture to enable signaling and power delivery. To the first order, these physical constructions are agnostic to the IO protocols for which they are used. Hence all attributes described here are independent of the IO protocol.

[9] These interconnects must be designed to minimize power dissipation and signal distortion in addition to provide effective interconnects [25-27].

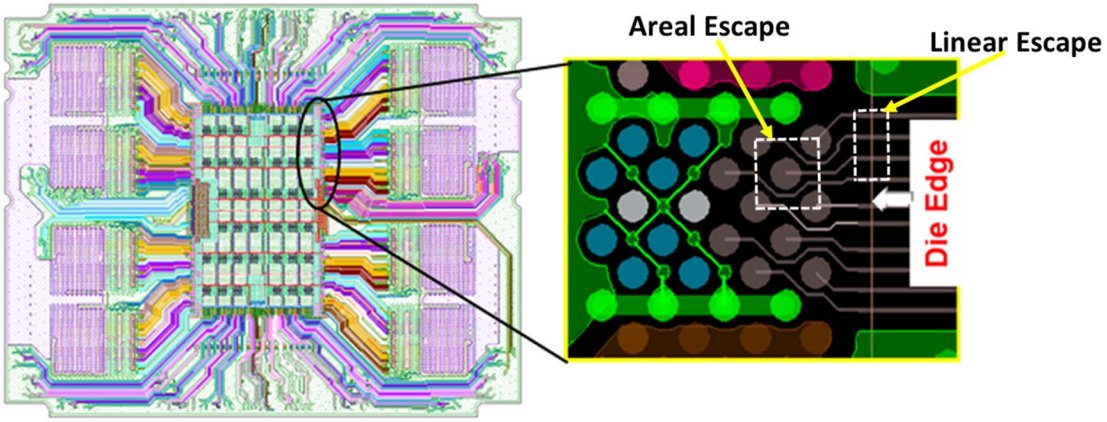
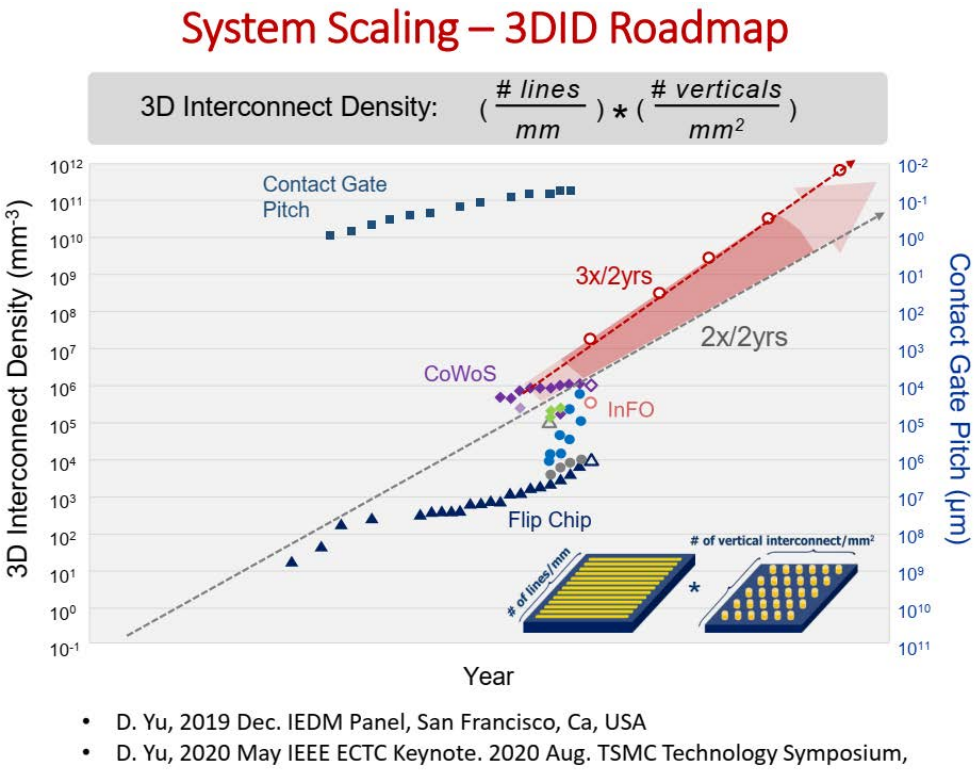


Figure 5A: Two Key Physical Design Attributes: IO/mm of die edge (Linear Escape Density) and (b) IO/mm² of die (Areal Escape Density). Note that the term IO here refers to physical bumps and wires.



- D. Yu, 2019 Dec. IEDM Panel, San Francisco, Ca, USA
- D. Yu, 2020 May IEEE ECTC Keynote. 2020 Aug. TSMC Technology Symposium,

Figure 5B: Two Key Physical Design Attributes: IO/mm of die edge (Linear Escape Density) and IO/mm² of die edge (Areal Escape Density) are multiplied to create a single 3D Interconnect Density (3DID). Note that the term IO here refers to physical bumps and wires. (Ack: TSMC)[10]

[10] Acronyms CoWoS and InFO are well known in the industry.

Table 4: Physical IO Scaling Roadmap 2D and Enhanced-2D Architectures that use Solder-based Interconnects.

Generation Number[11] →		1	2	3	4	5
Raw Linear Bandwidth Density (GBps/mm)[12,13,14]		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	50	40	35	30
	Linear Escape Density (IO/mm)[15]	500	667	1000	1500	2000
	Areal Escape Density (IO/mm^2)	331	400	625	816	1111
Signaling Speed (Gbps)[16]		2	3	4	5.33	8

Table 5: Physical IO Scaling Roadmap for 2D and Enhanced-2D Architectures that use both solder and hybrid interconnects.

Generation Number →		1	2	3	4	5
Raw Linear Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)[17]	55	40	30	20	10
	Linear Escape Density (IO/mm)	500	667	1000	2000	4000
	Areal Escape Density (IO/mm^2)	331	625	1111	2500	10000
Signaling Speed (Gbps)		2	3	4	4	4

5.1.2 Area Interconnects for 3D Architectures (see Figure 1)

Table 6: Physical IO Scaling Roadmap for 3D architectures that use both solder and hybrid interconnects.

Generation Number →		1	2	3	4	5
Raw Areal Bandwidth Density (GBps/mm^2)[18]		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)[19]	40	30	20	15	10
	Areal Escape Density (IO/mm^2)	625	1111	2500	4444	10000
Signaling Speed (Gbps)[20]		1.6	1.8	1.6	1.8	1.6

5.2 Signal Integrity Attributes

5.2.1 Signal Integrity Attributes for 2D and Enhanced 2D Architectures

The short and high-density interconnects described in Section 5.1.1 become more and more RC-dominated with the generational scaling. The interconnect inductance is expected to have a secondary effect on the channel performance. Table 7 shows the reduction of channel length with bump pitch scaling. This does compensate the larger per-unit-length RC of denser routing interconnects, so that the total channel RC loss does not increase from generation to generation.

Table 7: Channel Signaling Characteristics for 2D and Enhanced-2D Architectures

Generation Number →		1	2	3	4	5
Linear Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Channel Performance	Channel Length (mm)	<2	<1.7	<1.4	<1.1	<0.8
	Bump-to-Bump Channel RC (ps)	<10	<10	<10	<10	<10

[11] At present there is no universal understanding/agreement of the required time gap between generations. The TWG judgment is that it will be a minimum of 2 years, and from a planning perspective we recommend a maximum of 3 years, to ensure that the interconnect roadmap is competitive. Both these numbers reflect the leading edge, and mainstream implementations will depend on both economic and technical factors.

[12] Per mm of die edge.

[13] Starting value of 125 GBps/mm is estimated raw bandwidth possible in an AIB-style implementation.

[14] Raw Bandwidth is essentially the product of # of connections and signaling speed per connection. Achieved bandwidth will be lower since not all connections are used for data transmission. The starting point of 125 GBps/mm is a judged value.

[15] Since multiple silicon back-end layers or package layers can be used to route the bumps, specific geometrical features of the layers are not described.

[16] Representative example showing how the BW goals are reached. These speeds are not unique.

[17] Starting value of 55µm is based on the most common current implementation, i.e., HBM.

[18] Per mm^2 of die area.

[19] Starting value of 40 µm bump pitch based on known implementations in HBM and WIO2. .

[20] Note that previous versions of this chapter had shown a range of signaling speeds. The range has been removed to simplify the table.

5.2.2 Area Interconnects

The signal integrity performance of the extremely short area vertical interconnects is dominated by their capacitance. Their resistance and inductance are expected to have a secondary impact on the channel performance with generational scaling. Table 8 shows the scaling of bump capacitance with bump pitch reduction. The improved capacitance is an important enabler to avoid the need for stronger driver design.

Table 8: Channel Signaling Characteristics for 3D Architectures

Generation Number →	1	2	3	4	5
Areal Bandwidth Density (GBps/mm^2)	125	250	500	1000	2000
Bump Capacitance (fF)	<30	<22	<15	<10	<7

5.3 Power Delivery Attributes: Area Interconnects for 2D and 3D Architectures

The main changes in Table 9 from previous versions are in the MIM density and the VR power density. The table has been updated to reflect recent advances in the MIM and VR technology. Table 9 reflects projected demand, and packaging engineers will be challenged and will need to explore new materials and architectures to deliver capacitance and current-carrying capabilities.

Table 9: Power delivery Attributes for 2D, Enhanced-2D and 3D Architectures.
It should be noted that power delivery attributes are agnostic to the architecture.

Generation Number →		1	2	3	4	5
Core Power Density (W/mm^2)		5	8	12	18	25
	On-die MIM Capacitance Density (nF/mm^2)	50	100	200	400	750
	Silicon Trench Capacitance Density (nF/mm^2)	300	500	1000	1750	3000
	VR Power Density (W/mm^2)	0.4	0.6	1	1.5	2.5
	Ceramic Cap Density (μF/mm^2)[21]	40	50	70	100	150
	Bump Current-Carrying Capability (A/mm^2)	6	9	14	20	30

6. Review of Different Packaging Architectures:

In this section, we tabulate the various examples seen in literature with their corresponding architecture type, interconnection materials used, tightest pitches observed and the required processes and equipment to enable them. In addition, we list the resulting applications, reliability concerns and any additional challenges resulting from the same. This is a broad overview intended to offer perspective on all the interconnect examples; see Table 10.

7. Difficult Challenges

The high IO/mm values listed in Tables 4 and 5 are achieved using silicon back-end technologies to create thin, closely spaced wires (Figure 6). This roadmap projects the need for increasing density, i.e., reduced line pitch. When combined with increasing signal speeds, there will be greater concerns about signal quality due to increased crosstalk, caused by the reduced line spacing. The packaging community will be challenged to develop solutions that minimize impact to signal integrity and provide physical links with improved power efficiency.[22]

[21] Errata: Ceramic cap density values in the 2020 version of this chapter had an error i.e., an extra "0" was included in Gens 4 and 5

[22] Power efficiency (measured in pJ/bit) is a sum of Tx, Rx and link power efficiency. The die-die links need to provide reducing RC (Table 6) to ensure improved power efficiency.

Table 10. Examples of applications from literature as a function of the different packaging architecture and process/material attributes. [28, 29]

Architecture Type (2D/2D Enhanced/3D)	**Packaging Materials**	**Tightest Pitch[23]**	**Typical Interconnection Process**	**Typical Equipment**	**Typical Applications**	**Key Concerns (Partial List)**	**Challenges (Partial List)**	**Advantages (Partial List)**
2D [30]	Wire-Bonding	25µm	Wire-bonding	Wire-Bonder	Automotive, LCD drivers, Sensors, ASICs, Controllers	- Oxidation of Cu bonds - Wire-bond lift-off due to CTE mismatch	- Limitations with bonding temperatures - Corrosion / bond integrity	- Low cost-of-ownership - Flexible process - Easy to test / re-work wire-bonds
2D & 2D Enhanced [31]	Micro-bumps, C4s, TSVs, and passive Si Interposer	20 µm	TCB / mass-reflow processes	Thermo-compression bonding tools	CPUs, GPUs, FPGA, Network servers, Gaming Console Servers	- Warpage issues due to large package size	- Interposer testing - Handling thinned wafers	- Packaging enables high performance - Multifunction heterogeneous integration e.g. ASIC + HBM
3D Die-to-Die, Die-to-Wafer [32]	Micro-bumps, TSVs, Cu-Cu Bonding	5 µm	F2F or F2B Direct Cu-Cu bonding interconnection	Custom bonding equipment	AI, HPC, AR/VR, 5G applications	- Ensuring known good dies (KGD) - Test coverage limited during wafer probing	- High cost of ownership - Misalignment / FM particles during die placement	- Pitch Scalability
3D Wafer-to-Wafer [33]	Solder Bumps, Cu-Cu Bonding	0.9 µm	F2F or F2B Direct Cu-Cu bonding interconnection	Custom bonding equipment	AI, HPC, AR/VR, 5G applications	- Ensuring known good dies/stacks - Test coverage limited during wafer probing	High cost of ownership - Misalignment / FM particles during die placement	High 3D interconnect density with ultra-low bonding latency

[23] Reference envelope values. Values listed in Table in this chapter represent the broader mainstream envelopes.

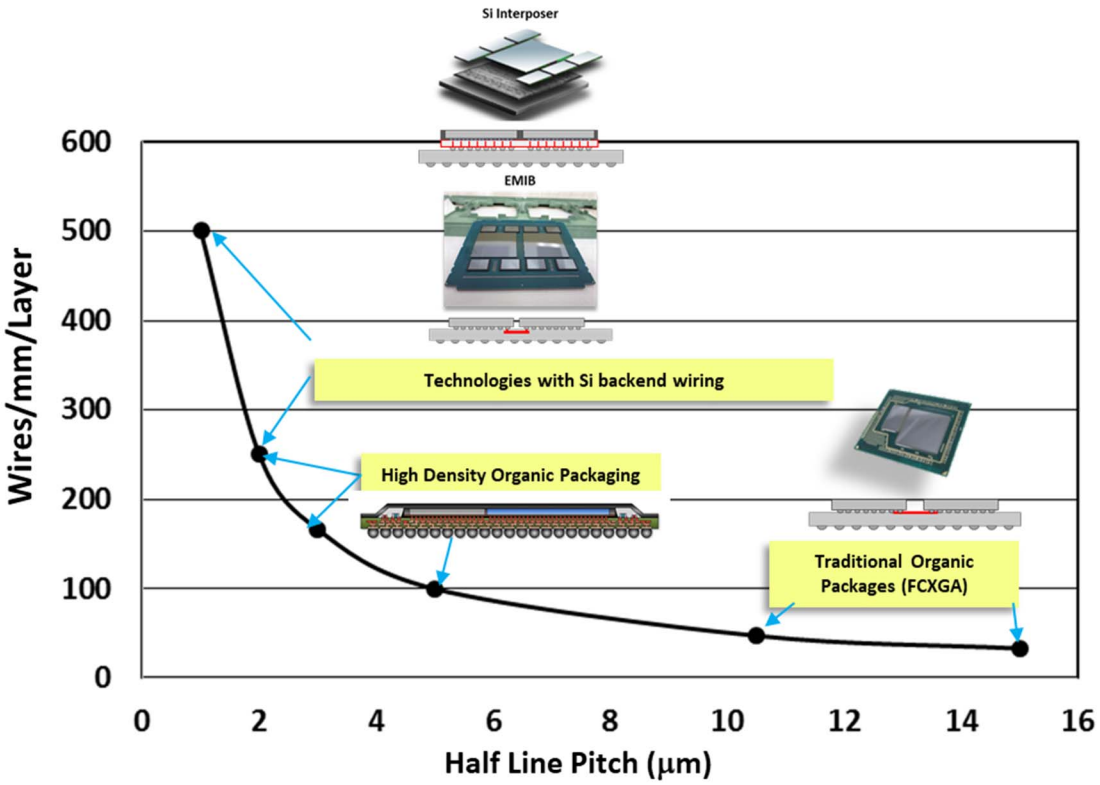


Figure 6: Technologies for different wiring features. L is the width of the line in µm, S is the minimum space between lines in µm; half line pitch is (L+S)/2. Technologies that use silicon backend wiring can achieve wiring densities of greater than 1000 with L & S ≤ 0.5µm.

There will be greater need to enable novel assembly technologies for ultra-fine pitch enhanced-2D and 3D architectures using both solder and non-solder-based approaches. A number of researchers have demonstrated the reduced bump pitches described in Table 4 and there is a fairly good understanding of the technologies needed to transition from solder-based interconnects to solderless interconnects [10-12, 28-33]. Key challenges for stacked-die architectures will continue to be in fine pitch sort/test, thermal management, power-delivery network development, design process co-design, in-line process control and equipment readiness for high volume.

8. Discussion

The primary driver for advanced 2D and 3D packaging technologies is the need for increased interconnect densities to support HI and deliver increasing bandwidth in a power-efficient manner while enabling efficient power delivery. An increasing number of innovative packaging architectures deliver significantly improved HI envelopes. In these HI architectures, physical interconnects (i.e., wires, bumps) and link RC characteristics are completely under the control of packaging technologists and it is relatively easy to establish a non-unique scaling roadmap. Already a number of power efficient, high bandwidth IO links that take advantage of advanced packaging have been defined to further spur the proliferation of heterogeneous integration [34-44]. We anticipate that moving forward, this chapter will spur discussion among product architects and will help develop further clarity on various use cases that will drive the pace of technology innovation. Delivering higher interconnect densities will challenge packaging engineers to develop novel materials, assembly processes and metrologies to develop cost-effective technology solutions that meet the performance demands of future HI architectures. Even though it is not the focus of this chapter, it is also important to note that the ability to integrate the right thermal features will define the physical envelope (i.e., form factor and number of die or die stacks that can be integrated on the package) and the warpage characteristics that will ensure manufacturability [45].

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Key Contributors

Ravi Mahajan (Chair)	Raja Swaminathan	Subramanian Iyer	Kemal Aygun
Jan Vardaman	Zhiguo Qian	Kaladhar Radhakrishnan	Srikant Nekkanty
Rozalia Beica	Tom DeBonis	Dishit Parekh	Vidya Jayaram
Kanad Ghose	John Hunt	Adeel A. Bajwa	Paul Franzon
Debendra Mallik	Kaushik Mysore	Peter Ramm	Steffen Kroehnert
Venky Sundaram	Markus Wimplinger	Thom Gregorich	Sam Karikalan
Dave Armstrong	Chintan Buch	Vaibhav Agrawal	Michael Alfano
Gamal Refai-Ahmed	SB Park	Takafumi Fukushima	Ivy Qin

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