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PDN Resonance Calculator for Chip, Package and Board

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Biographies

Larry D. Smith is a signal and power integrity principle engineer at Qualcomm Corporation concentrating on power distribution methodology. Prior to joining Qualcomm in 2011, he worked at Altera Corporation from 2005 to 2011 specializing in PDN design and SSN noise and at Sun Microsystems from 1996 to 2005, where he did development work in the field of signal and power integrity. Before his work at Altera and Sun, he worked at IBM in the areas of reliability, characterization, failure analysis, power supply and analog circuit design, packaging and signal integrity. Mr. Smith received the BSEE degree from Rose-Hulman Institute of Technology and the MS degree in material science from the University of Vermont.

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Shishuang Sun is a senior member of technical staff engineer at Altera Corporation. His research interests include signal integrity in high-speed digital systems, on-chip and system-level power distribution network design and modeling, and jitter and timing impact from on-chip PDN noise. He received a PhD degree in electrical engineering from Missouri University of Science and Technology (formerly the University of Missouri-Rolla). He has authored more than a dozen journal and conference papers. He received paper awards from DesignCon 2010.

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Sunitha Chandra serves as a Member of Technical staff at Altera focused in the area of Signal and Power Integrity. Prior to her work at Altera she worked at Nvidia during 2004-2011 as a senior signal integrity engineer. She received her Masters degree in Electrical Engineering from Missouri University of Science and Technology (formerly the University of Missouri-Rolla). Her interests include PDN analysis, system level channel optimization and timing analysis for serial and parallel interfaces.

Abstract

Power Distribution Networks (PDNs) are important for performance but are costly. A spreadsheet method to manage the resistance, inductance and capacitance (RLC) properties of the die package and PCB is demonstrated. The resonant frequency and peak height are calculated using closed-form electromagnetic (EM) extraction and on-die capacitance (ODC) estimates. The switch factor is calculated from the PDN current, operating frequency, and ODC, and used to drive time-domain simulation. The SPICE simulation compares the PDN impedance with the target impedance and shows the first dip and burst transient responses. Model-to-hardware correlation is achieved using clock gating techniques to produce power transients at any frequency and generate impedance plots.

Introduction

The PDN is important for product performance and is also expensive. A method for determining the dominant parts of the PDN and estimated performance early in the design process is highly desirable. Usually the dominant impedance peak occurs at a frequency determined by ODC and the inductance found in the package and PCB. There may be on-package decoupling (OPD) that sits on top of the die/package resonance and splits the impedance peak up into two peaks: one between the die and package and the other between the OPD and PCB. The components that make up a typical PDN along with the frequency bands that they dominate are illustrated in Figure 1.

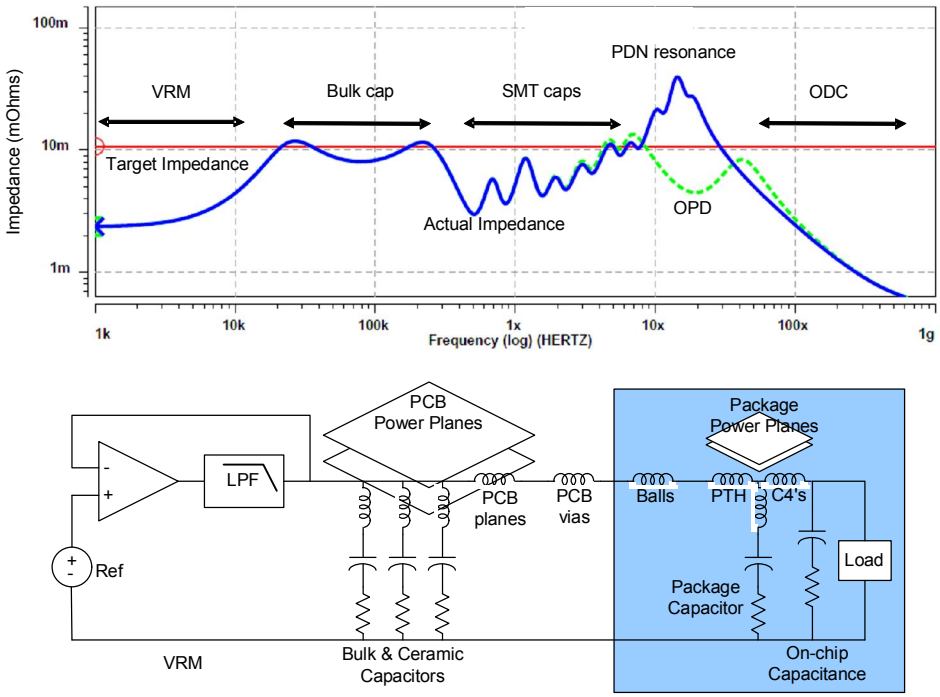


Figure 1: Components that make up a typical PDN. Upper graph shows approximate frequency ranges where components are effective.

Previous work has demonstrated the issues caused by PDN impedance peaks [1]. Measured data has classified noise signatures into 1st dip, burst and periodic burst transients. Methods have been developed to measure the PDN response to clock edge and dynamic current and correlate these with simulation results.

This paper develops techniques to estimate the impedance peaks with a simple spread sheet and generate SPICE simulation to match the noise signature classifications mentioned above. Figures of merit are defined which are an indication of the goodness or badness of a PDN. This provides a simple and effective method to manage many diverse PDN types across a product line. It is not intended to be a replacement for accurate EM modeling of intricate structures but does provide a way to identify the portions of a PDN that are expected to dominate performance well before die, package or PCB artwork is available.

The essence of the PDN Resonance Calculator is to reduce the PDN geometries and materials to equivalent RLC components that estimate the dominant impedance peak. An extension of this methodology allows for a package capacitor to break up the resonance into two peaks. EM extraction is accomplished by separating geometries and materials into vertical and horizontal structures that are represented by twin lead transmission lines and parallel plates with closed form solutions for resistance and inductance. An equivalent circuit topology is defined which enables a SPICE template to be generated and populated with circuit parameters by simply pushing a button on a spread sheet. SPICE simulation runs quickly to give near instantaneous performance expectations for the PDN. Product parameters such as the number of balls, vias, power plane stackup, die capacitance, discrete capacitor properties, etc are quickly changed to evaluate performance and optimize the cost of the PDN. This paper describes and summarizes the methodology for developing and using the PDN Resonance Calculator and compares predictions to measured results.

Series and Parallel Circuits

From a practical standpoint, the resonant peak for the PDN is estimated from knowledge of capacitance, inductance and resistance. After reducing the PDN structures to these three elements, closed form equations are used to predict important PDN parameters such as the resonant frequency, height of the resonant peak and q-factor. Properties of series and parallel RLC circuits are reviewed below.

Figure 2 shows the RLC elements of an example PDN. The same components with the same parameters are combined together in series and parallel. The series circuit can be observed from the balls on a package (outside looking in) and the parallel circuit is seen by on-die circuits (inside looking out).

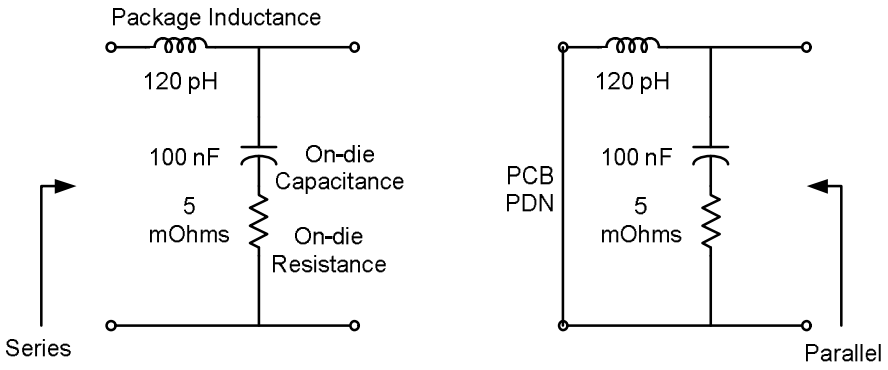


Figure 2: Series and parallel RLC circuits made from same component values.

The impedance profiles are shown in figure 3. Capacitance always presents itself as a -20 dB per decade slope and inductance always presents itself as a +20 dB per decade slope on log-log scales. Resistance is identified as the bottoming out of the series circuit and as the final value of the parallel circuit at high frequency where the capacitive reactance becomes small.

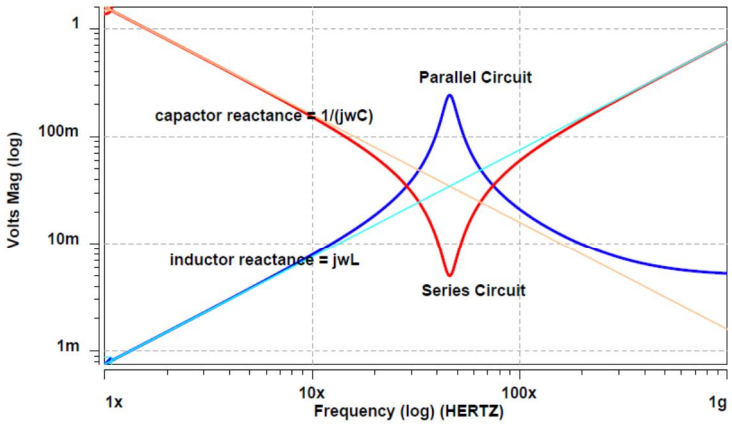


Figure 3: SPICE simulation of a parallel and series RLC circuit in the frequency domain.

The resonant frequency, reactance at resonance, q-factor, and resonant peak are calculated or estimated as follows:

1) Resonant frequency $$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

2) Reactance at resonance $$X = \sqrt{\frac{L}{C}}$$

3) q-factor $$q\ factor = \frac{X}{R} = \frac{\sqrt{L/C}}{R}$$

4) Estimate of impedance peak $$Z_{peak} \doteq X \bullet q\ factor = \frac{X^2}{R} = \frac{L/C}{R}$$

The first three quantities are derived from circuit theory but there is not an easy closed form formula to calculate the height of the peak. The precise peak height as well as the phase depends on how much of the resistance is associated with the inductor and how much is associated with the capacitor. But from visual inspection of figure 3, which was simulated with all of the resistance associated with the capacitor, the distance from the parallel peak to the reactance crossing is the same as the distance from the series dip on a log scale. This is the basis for the fourth equation above. The higher the q-factor, the better this estimate is. The estimate is less accurate as the q-factor approaches 1 (resistance is equal to reactance at resonance). But as long as there is an important resonant peak, this formula can be used to estimate the height of the peak to within reasonable accuracy. Assuming that the RLC parameters are correctly estimated, these equations give many of the important properties of PDN resonance.

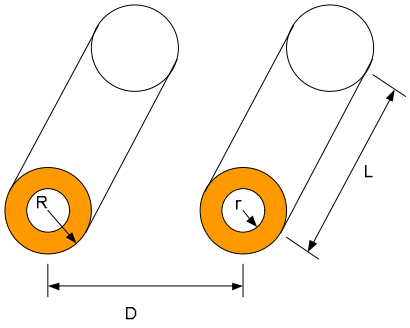
Estimation of Capacitance, Inductance and Resistance

A previous paper discusses the measurement of ODC and ODR [2]. Briefly summarizing, the ODC and ODR are measured in the frequency domain using a VNA. In the time domain, a known impulse of charge is consumed from the PDN and the 1st dip and PDN response is observed with an oscilloscope. ODC and ODR can also be estimated from SPICE or other simulation of all the circuit blocks attached to the PDN. Once the ODC and ODR have been found from one of these three methods, a capacitance density (capacitance per area) is established for the type of circuits under consideration. The capacitance density is used to estimate the capacitance for other similar circuits in that technology node within some confidence factor. Capacitance density of the next technology node must be projected based on experience with previous technology nodes and insight into the changes that come with next generation technology. Historically, the capacitance density for the PDN has approximately doubled for the past several generations but this may vary from circuit type to circuit type and may or may not continue into the next generation.

Inductance and resistance are associated with package and PCB structures and is estimated from geometries and materials. Structures are classified into two types: vertical where the cross section is cylindrical in nature and horizontal where the structures are planer in nature. Examples of vertical structures are vias, balls, and bumps. Examples of horizontal structures include power planes and power traces. Closed form formulas are used to estimate loop inductance and loop resistance both at DC and at resonant frequency due to skin effect. The simple geometries and closed form formulas are not as accurate as field solver results but they are often good enough to give reasonable predictions and to focus attention on the structures that dominate the PDN properties at resonance.

The basis for vertical structure calculation is the twin lead transmission line as discussed in Kraus [3] and shown in Figure 4. The loop inductance per unit length of this structure is $0.4\mu_r \ln(D/R)$

μH/m where μ_r is the relative permeability (usually 1 unless magnetic materials are involved), D is the center to center spacing between conductors and R is the outside radius of the conductor. Current is assumed to be on the surface of the conductor. The DC loop resistance per unit length is $2/[(\pi R^2 - \pi r^2)\times\sigma]$ where r is the inside diameter and σ is the conductivity of the material. Skin effect causes the inside diameter to change as a function of frequency. The skin depth is $1/\sqrt{f\pi\mu\sigma}$ where f is the frequency where the skin depth is to be calculated, μ is the permeability. The cross sectional area is calculated for a high frequency where skin effect is completely engaged (i.e. 100MHz). After the resonant frequency has been determined, the skin effect resistance is calculated from $R_1 = R_0\sqrt{f_1/f_0}$ where R_0 is the resistance at high frequency f_0 and R_1 is the resistance at resonant frequency f_1. The maximum of the DC resistance or the skin effect resistance is selected because the frequency ratio formula may predict a resistance that is less than the DC resistance if f_1 is too low. From these simple formulas, the per-unit-length loop inductance and resistance are calculated for the twin lead structure. It is then a matter of multiplying by the length and accounting for multiple pairs in parallel to determine the inductance and resistance of vertical PDN structures.



$$Loop\ Inductance = 0.4\mu_r \ln\frac{D}{R}$$

$$Loop\ Resistance = \frac{2}{area \bullet \sigma}$$

$$R_1 = R_0\sqrt{f_1/f_0}$$

$$skin\ depth = \frac{1}{\sqrt{f\pi\mu\sigma}}$$

Vertical	PCB vias	Package Balls	Package L1-L2 micro vias	Package PTH vias	Units
Material	copper	solder	copper	copper	
Pitch	1.00	1.000	0.320	1.000	mm
Diameter (OD)	0.253	0.500	0.125	0.200	mm
Diameter (ID)	0.203	0.000	0.000	0.100	mm
Cross Sectional Area	0.0181	0.1963	0.0123	0.0236	mm^2
Conductivity	5.80E+007	5.20E+006	5.80E+007	5.80E+007	1/(ohm-m)
Skin Depth @ 100MHz	0.0066	0.022	0.007	0.0066	mm
Cross Sect. Area @ 100 MHz	0.00512	0.03314	0.00246	0.00402	mm^2
Per Unit Length (mm)					
Loop Inductance	827	555	653	921	pH/mm
Loop Resistance @ DC	1.903	1.959	2.810	1.463	mOhm/mm
Loop Resistance @ 100MHz	6.736	11.606	14.029	8.588	mOhm/mm
1 Loop					
Length	108.00				mils
Length	2.734	0.500	0.105	0.800	mm
1 Loop Inductance	2260	277	69	737	pH
1 Loop Resistance @ DC	5.20	0.98	0.30	1.17	mohm
1 Loop Resistance @ 100MHz	18.42	5.80	1.47	6.87	mohm
Pairs					
number of pairs	31	31	62	31	
checkerboard factor	1.1	1.2	1.1	1.2	
Loop Inductance	66	7.5	1.0	19.8	pH
Loop Resistance @ DC	0.168	0.032	0.005	0.038	mOhm
Loop Resistance @ resonance	0.175	0.055	0.007	0.065	mOhm

Figure 4: Vertical structures such as vias and balls are represented by twin lead transmission line formulas. The table shows example calculations for the geometries and materials of PCB vias and Package balls, micro vias and PTH vias.

The most efficient arrangement of multiple pairs is a checkerboard pattern that takes advantage of mutual inductance between pairs in order to minimize loop inductance. In a checkerboard pattern, each Vdd pin looks out four directions (north, south, east and west) and sees a Vss pin for return current. Similarly, each Vss looks out four directions and sees a Vdd pin for return current. Total loop inductance is minimized in this way. With 2 pair arranged in a 2x2 array, less inductance is expected than what is predicted by two pairs of twin lead transmission line in parallel. Similarly, a 4x4 array with 8 pairs of Vdd and Vss arranged in a checkerboard pattern will have less inductance than predicted by 8

twin lead transmission lines in parallel. This inductance reduction is called the checkerboard reduction factor.

Figure 5 shows Vdd and Vss pins arranged as 1 pair (1x2), 2 pair (2x2), 4.5 pair (3x3), 8 pair (4x4), 12.5 pair (5x5), and 18 pair (6x6). The loop inductance is extracted for each pattern and normalized to the ñper pairò value for each configuration. A single pair has the inductance predicted by the twin lead formula. By adding more pair into the mix, the normalized inductance per pair is reduced. With enough pairs in the checkerboard pattern, the normalized inductance reaches an asymptote and flattens out to a quantity known as the ñchecker board factor.ò All pin configurations will have a checkerboard factor for inductance but its specific value depends on a lot of factors such as the number of pair, the ratio of diameter to pitch, the frequency, the exact configuration of the pins, etc. If the pattern is not a checkerboard but some of the Vdd pins are clumped together and some of the Vss pins are clumped together, the factor can be more than 1. This indicates that the specific pin configuration has normalized inductance per pair is greater than that of the twin lead transmission line. Sometimes clumping of similar pins is necessary for layout considerations but results in less inductance improvement than might be expected from the pin count. The checker board factor is essentially a fudge factor that accounts for the pin configuration as inductance is estimated for a number of cylindrical structures in parallel.

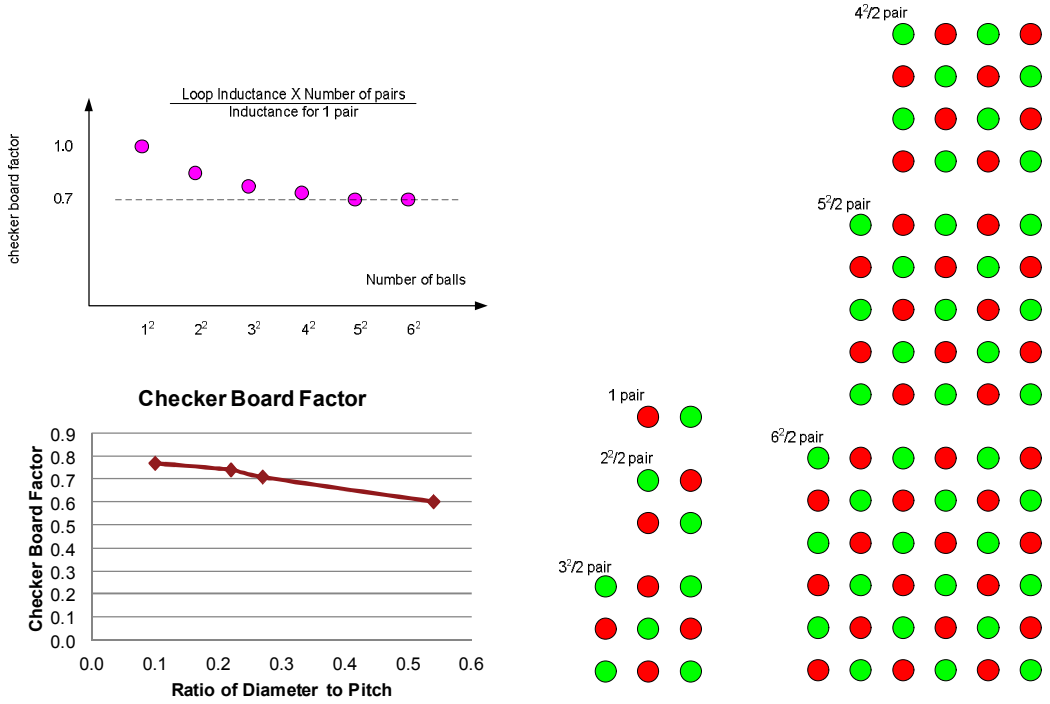
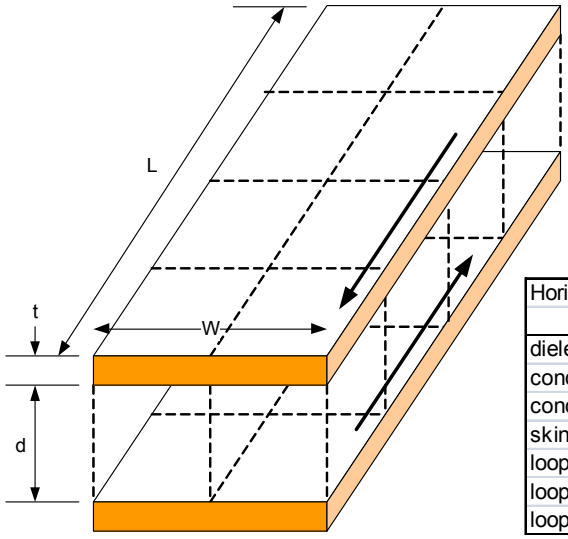


Figure 5: Vdd and Vss pins arranged in checkerboard pattern. The inductance per unit length is reduced by a factor that is related to the number of twin lead pairs and the ratio of diameter to pitch for the pattern.

Like vertical structures, horizontal structures also have inductance and resistance that must be estimated. Kraus [3] discusses these in terms of field cells and curvilinear squares. Figure 6 shows the cross section of power plane material including two conducting planes separated by a dielectric. To find the resistance between the ends of a block of material, it is necessary to know the cross sectional area and the length. The resistance between end plates is $\rho L / area = L / (\sigma wt) = (1/\sigma t) / (L/W)$ where ρ is the resistivity of the material in ohm-m, σ is the conductivity in 1/ohm-m, l, w and t are the length, width and thickness of the material in appropriate units. As suggested in the formula, the terms can be broken into a portion that is a property of the material $(1/\sigma t)$ and a portion that is related to the design (L/W). The reciprocal of conductivity times thickness has units of ohms and is known as ñsheet resistanceò and is often discussed in terms of ñohms per squareò because each square of material with equal length and width has this resistance. The conductor thickness will be reduced by skin effect above some frequency. The conductor will effectively be $1/\sqrt{f\pi\mu\sigma}$ thick as discussed above in the section on vertical resistance. The length divided by the width is the ñnumber of squaresò of material and is a conceptually convenient quantity that can be estimated simply by looking at the design. Horizontal plane resistance is known as ñspreading resistanceò and is the product of the sheet resistance and the number of squares.



Horizontal (planer)	package shape	Units
dielectric thickness	0.035	mm
conductor thickness	36	uM
conductivity	5.80E+07	1/(ohm-m)
skin depth @ 100MHz	0.0066	mm
loop inductance per square	42	pH
loop resistance per square - DC	0.97	mOhms
loop resistance per square - 100 MHz	5.218	mOhms

Figure 6: Cross section of power plane material segmented up into squares. Sheet resistance and inductance are calculated from the conductor thickness and dielectric thickness respectively.

Resistance of irregular structures such as a sheet of material contacted by two cylinders, each with a diameter, can be estimated by the using curvilinear squares. The pattern of current flow is drawn on the sheet and marked off into squares. The resistance of irregular shapes is estimated by multiplying the sheet resistance by the number of squares in series and dividing by the number of squares in parallel.

Loop resistance is important for power planes where current goes down a horizontal power structure and returns on a ground structure. If the structures are symmetrical, the loop resistance is twice

that of the power structure. The ground structure may possibly be much wider than the power structure and so the return path may have fewer squares of conductive material. The wider ground path may be carrying return current for a different PDN. So the loop resistance of power plane is estimated by the resistance of the power path multiplied by a factor between 1 and 2 depending on ground return path considerations.

Inductance is estimated by similar considerations. Loop inductance is essentially a representation of the energy stored in a magnetic field due to a loop of current. Current travels in a direction on the power plane and returns on the ground plane which causes a magnetic field between the planes. At high frequency, currents are on the conductor surface and the magnetic field is contained in the dielectric between the conducting planes. Similar to the curvilinear square concept for resistance, the ñsheet inductanceò of power plane material is described in terms of squares and is proportional to the dielectric thickness[3]. The sheet inductance per square of a sandwich of metal-dielectric-metal is $\mu_0 d$ where μ_0 is the permeability of free space and d is the dielectric thickness. Horizontal plane inductance is known as ñspreading inductanceò and is the product of the sheet inductance and the number of squares. The inductance as well as the resistance is estimated by multiplying material property values (sheet inductance or sheet resistance) by the number of squares of material present in the layout.

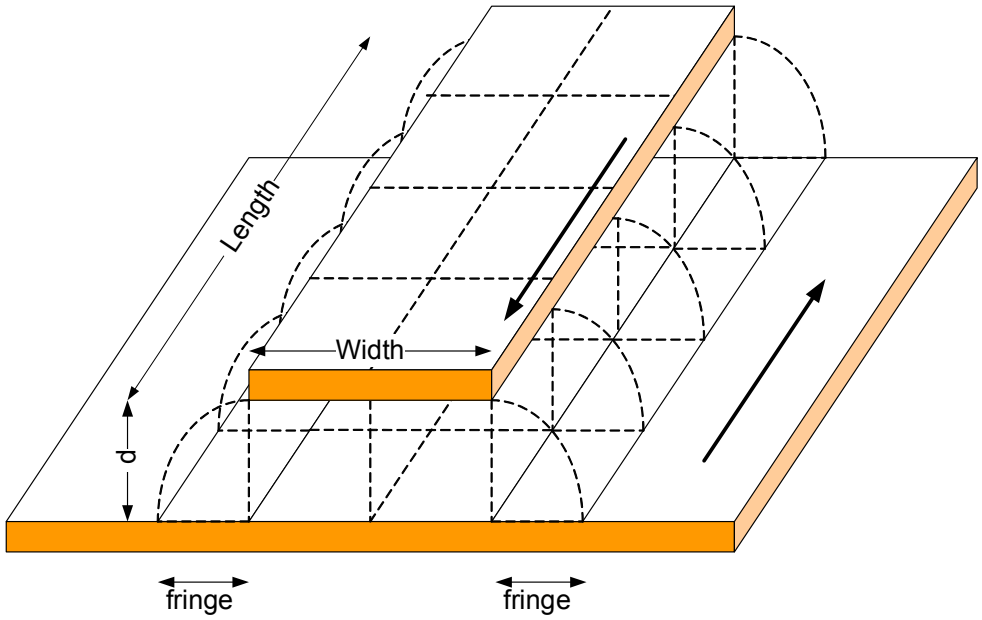


Figure 7: Fringing fields at the edge of power planes. For EM purposes, the width of plane is effectively 2.8 times the dielectric thickness wider than the physical dimension of the power trace.

Similar to the DC return current, the high frequency return current for inductance purposes is not exactly underneath the power structure. Figure 7 shows fringing fields at the edge of power planes as the electric and magnetic fields diverge outward from the top surface. At DC and audio frequencies, current will expand out to cover the whole ground plane because inductance is not important. At

frequencies where skin effect is important (above approximately 1MHz), the return current will stay close to the power current. Fringe fields will extend out approximately 1.4 dielectric thicknesses on each side and the width of the power structure is effectively extended. For broad power planes this is not too important but for narrow power traces it is. With a 50 µm dielectric, a 5mm power trace is 100 times wider than the dielectric thickness and the addition of 2.8 more thicknesses makes the effective width 102.8% of the actual width. But a 500 µm wide trace is effectively 128% of its width and a 100 µm trace is effectively 240% of its width. The sheet inductance method over estimates spreading inductance for narrow power traces but can be mitigated by making the effective width 2.8 x dielectric thickness wider than the actual width.

PDN Resonance Calculator

The PDN Resonance Calculator is broken down into several sections including target impedance calculation, die, package and PCB properties, figures of merit and spice parameters. These sections are considered in the next several paragraphs.

The target impedance is the starting point for PDN design [xxx]. It is the reference impedance to judge the goodness or badness of the actual impedance. If the actual impedance exceeds the target impedance there will be noise and performance consequences. The PDN is probably more expensive than it needs to be if the actual impedance is far below the target impedance. The target impedance is a simple Ohms law calculation

$$Z_{\text{target}} = \frac{Vdd \times tolerance}{I_{\max} - I_{\min}} = \frac{Vdd \times tolerance}{I_{\max} \times \%_{transient}} = \frac{0.85V \times 5\%}{12A \times 50\%} = 7.1m\Omega$$

The tolerance refers to the voltage excursions that can be tolerated by the on-die circuits and have them still work within specification. The transient current is the minimum current minus the maximum current and can also be expressed as a percentage of the maximum current. If either the tolerance or the transient current is a function of frequency, then target impedance is also a function of frequency. Tolerance and transient current are easily understood concepts but are often illusive when trying to quantify them for a given design. Leakage current contributes to damping but is not part of the transient current calculation. Dynamic current, which comes with the clock, is the only current involved with the target impedance calculation which is shown in Table xxx.

Voltage	volts	0.85
Leakage current per channel or bank	amps	3.0
Dynamic AVG current per channel or bank*	amps	12.0
AC calculations		
AC Tolerance	%	5
transient (% of dynamic)	%	50
AC Target impedance	mOhms	7.1

The amount of on-die capacitance required, the average clock edge current [2] and the switch factor are calculated by some surprisingly simple formulas. The average clock edge current (charge per clock cycle) is calculated from the time averaged current that would be measured from the bench power supply and the clock frequency: $q_{cycle} = I_{bench} / f_{clock}$. Some clock edges will draw more current than others but on the average, the time integral of current associated with a clock edge is q_{cycle} with units of nCoulombs. This is the amount of charge that is responsible for the average 1st dip in the PDN voltage waveform [1]. The amount of load capacitance that must have switched in order to draw that amount of charge is: $C_{switched} = q_{cycle} / Vdd$. The depth of the 1st dip (V_{dip}) is calculated from the $q_{cycle} = CV = ODC_{nonswitching} \times V_{dip}$ relationship. From this equation, the amount of non-switching ODC required to be present on-die to keep the 1st dip from dropping more than a given percentage of the power supply is calculated: $ODC_{nonswitching} = Vdd \times Tol_{1^{st}\ dip} / q_{cycle}$. The capacitance required on-die to keep the PDN voltage noise within the 1st dip tolerance is: $ODC = C_{switched} + ODC_{nonswitched}$. Note that this quantity has been calculated simply from knowledge of the dynamic current consumed at a clock frequency and the depth of the 1st dip that will be tolerated by the circuits.

Another useful quantity is the switch factor which is the ratio of the switched and the non-switched capacitance expressed as a percentage. This is roughly interpreted as the percentage of gates that switch during an average clock cycle. As discussed above, some clock cycles will have more switching activity than others but average quantities can be used to establish the minimum requirements for a PDN. In this case, the switch factor is expressed as a percentage of the actual capacitance rather than the calculated required capacitance. This is going to be a useful quantity when the time domain load is developed for SPICE simulation below. The Die ODC and ODR are found from measurements and previous experience as discussed above.

clock frequency	MHz	533
charge per cycle	nCoul/cycle	18.8
load capactiance that switched	nF	17.1
1st dip tolerance	%	10
ODC required to stay within tolerance	nF	188
switch factor	%	5.7
Die		
ODC (on-die capacitance)	nF	300
ODR (on-die resistance)	mOhm	2.5

In the example above, a 533 MHz clock has caused 12A to be consumed from a bench power supply, so the charge per cycle is 18.8 nCoul. Given the 0.85V Vdd, the average load capacitance switched was 17.1nF. 188 nF of ODC is required to keep the depth of the 1st dip less than 10% of Vdd. For the scenario, 5.7% of the total ODC (300nF) was switching.

Package		
number of Vcc/Vss ball pairs		66
Inductance	pH	15.4
resistance @ DC	mOhm	0.327
resistance @ resonance	mOhm	0.462

The next section of the PDN Resonance calculator has to with the package inductance and resistance. The number of package balls is an input which is referred back an electromagnetic extraction page where the closed form formulas described above are used to calculate the vertical and horizontal parameters from geometries and materials. The inductance, DC and skin effect resistance are summed up and reported back in this section in the purple shaded cells.

PCB		
via length	mils	80
via inductance	pH	23.1
via resistance @ DC	mOhm	0.058
via resistance @ resonance	mOhm	0.120
plane dielectric thickness	mils	3
plane squares		0.25
plane inductance	pH	23.1
plane resistance @ DC	mOhm	0.242
plane resistance @ resonance	mOhm	0.759
number of PCB caps		50
average mounted cap inductance	pH	600
cap inductance	pH	12.0
cap resistance	mOhm	0.20

PCB inductance and resistance parameters are calculated similar to the package. PCB inputs are needed including the via length from the top surface of the board to the power planes and the plane properties such as dielectric thickness and number of squares. This information goes back to EM calculation page and the extracted parameters are returned in the purple cells. The board capacitors may contribute significant inductance and damping resistance to the PDN so the final four rows of this section are used for this purpose.

Total Inductance	pH	74
Total Resistance at DC	mOhm	3.1
Total Resistance at resonance	mOhm	4.0

The inputs and sub calculations of the PDN Resonance Calculator are now complete. Resistance and inductance from the die, package and PCB are summed up and reported. These together with the ODC contain all of the RLC information needed to calculate the properties of the PDN resonance.

PDN Figures of Merit

The resonant frequency together with five figures of merit are calculated.

1) Resonant Peak

2) PDN Ratio

3) Q-factor

4) 1st dip as percentage of Vdd

5) DC IR drop as percentage of Vdd

Resonant frequency	MHz	34
Resonant peak	mOhm	61
PDN Ratio (self aggression)		11.0
Q factor (noise accumulation)	Q	3.9
1st dip (clock edge noise as % of Vdd)	%	5.7
DC IR drop (as % of Vdd)	%	3.7

The resonant frequency is useful information but not considered to be a figure of merit. The first three figures of merit are related but have subtle differences. The height of the **resonant peak** determines the susceptibility to external aggression. External aggression can come from single ended IO, other PDNs, PCB activity, cavity resonances within the package and any other unidentified external source that is not related to the PDN under evaluation. Any of these external sources are capable of coupling energy to the PDN and it is most vulnerable at its resonant frequency, even if it meets target impedance. For example, a Phase Lock Loop PDN may have a very high target impedance (possibly 10 ohms) because it draws very little transient current. But any PDN that is above about 1 ohm is susceptible to external aggression, particularly if it has a high q-factor.

The **PDN ratio** compares the actual impedance to the target impedance and indicates how susceptible the PDN is to self aggression. Current or power transients generated in the PDN under evaluation are responsible for self aggression. Many successful products have an actual impedance peak that is up to 3 times the target impedance which is a bit of a paradox and is probably due to errors in the target impedance calculation. Circuit designers often claim that their circuits will fail if the power supply exceeds some tolerance (i.e. 5%) but the circuits actually have more margin than expected. The current transient may also be overestimated. Many times, performance and product cost targets can only be simultaneously met if the PDN impedance is allowed to exceed the target impedance (PDN ratio) by some amount. This amount can only be estimated after careful characterization of products, possibly over several generations.

The **q-factor** indicates the sharpness of the peak and the ability of the PDN to pick up energy over several clock cycles. PDNs with a q-factor less than 2 are considered to be pretty safe. With a higher q-factor, the PDN may pick up noise from an aggressor cycle after cycle by superimposing energy from one cycle onto another.

The **1st dip** that comes from the clock edge current (charge) being consumed from the ODC is compared to Vdd voltage and expressed as a percentage. This percentage is highly related to the voltage tolerance used in the target impedance calculation. It is essentially the tolerance for the GHz frequency

band. As shown above, the 1st dip tolerance may be used to calculate the necessary ODC to for the average q_{cycle}. Or, the 1st dip as a percentage of Vdd (high frequency voltage noise) can be calculated from the available ODC. This essentially makes the target impedance a function of frequency if the high frequency voltage tolerance is different than that of a different frequency band.

Finally, the **DC IR drop** is listed as a figure of merit for the PDN. For power consumption and efficiency purposes, the voltage tolerance at DC may be different than other frequency bands which further defines the target impedance as a function of frequency.

The PDN resonance calculator spread sheet is useful as a stand alone tool to evaluate figures of merit. It is even more useful when used to drive spice simulation to graphically demonstrate the frequency and time domain PDN performance. The next section develops the time domain load.

Time Domain Load Circuit

PDN simulation often involves ideal SPICE current sources with a piecewise linear time profile to draw current transients from the PDN. One problem with this type of load circuit is that it draws the same amount of current no matter what the PDN voltage is. In real life, CMOS circuits draw current that is proportional to PDN voltage, similar to a resistor. CMOS provides PDN damping in a way that an ideal current source does not. An improvement over the current source is a time dependent resistor. It will draw current that is proportional to PDN voltage and also provide damping. Piecewise linear time domain resistors can be made in SPICE to serve as the PDN load. A resistor value that will draw the nominal current at the nominal voltage is easily calculated from Ohmôs law. Current transients are drawn from the PDN by giving the resistor piecewise linear values as a function of time.

A further improvement is to use switched capacitors to mimic the CMOS load current similar to a real CMOS device. Each logic circuit is loaded by diffusion capacitance, wiring channel capacitance and the fan out capacitance of the next FET gates. In one clock cycle, the charge consumed by the load is the capacitance times the PDN voltage, $q = C_{load}V$. Average Current is the charge per cycle multiplied by the frequency, $I = q \times freq = C_{load}V \times freq$. Power is $freq \times C_{load}V^2$. It is desirable to build a time domain load circuit that has all of the properties of CMOS circuits including the relationship to the clock, PDN voltage, current (power) consumed and damping. Figure 8 shows such a circuit.

each cycle charge is supplied by input current eventually, I is amount of charge per s, divided by freq ==> amount of charge per cycle

I = Q/t = C*V / R_t
R_t is diff from T = 1/freq

now I is related with V
P = V*I= V*(C*V*f)

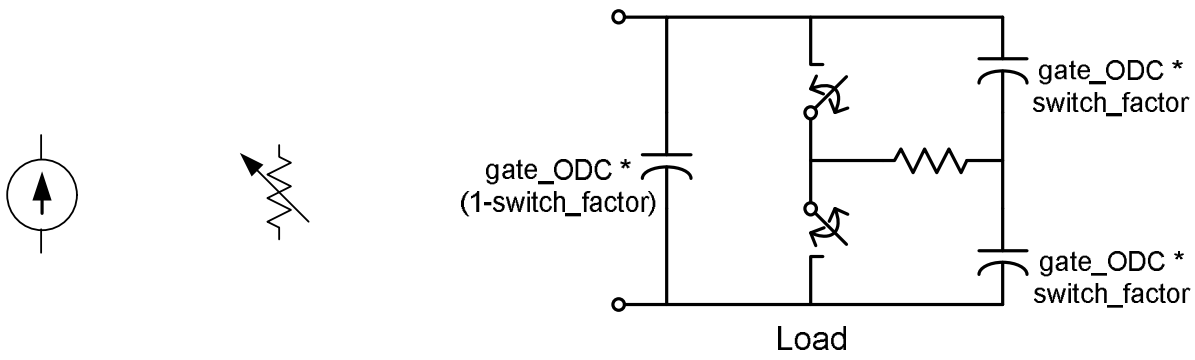


Figure 8: Three types of time domain loads for PDN circuit: constant current source, time varying resistor and switched capacitor circuit. The current source is constant no matter what the PDN voltage and provides no damping. The time varying resistor provides damping but determination of resistor value is difficult. Switched capacitor load draws correct current with PDN voltage, provides damping and is easily correlated to actual CMOS circuit operation.

Much of the on-die capacitance resides in the CMOS gates and wiring channels. In any given clock cycle, most of the gates do not switch but some of them do. This circuit takes a portion of the ODC and places it in the load position. For this analysis, the upper and lower (Vdd and Vss) capacitance is equal. It can be argued that routing wires in adjacent wiring channels are equally likely to be high or low and that the following PFET and NFET gate capacitances are nearly equal and therefore the load capacitance is approximately symmetrical between Vdd and Vss. The switches can be thought of as a single pole double throw switch where only one switch is closed at a time. The switches are zero ohms with all of the resistance being placed in the output branch. The switch factor is calculated in the PDN Resonance Calculator spread sheet and is the proportion of ODC that is switched on each clock cycle.

The circuit only draws PDN current when a non-zero amount of ODC is placed in the load position. As discussed above, the switch factor is calculated from the charge per cycle $q_{cycle} = I / freq$; the amount of capacitance required to draw that charge given the PDN voltage $C_{swiched} = q_{cycle} / V$; and by then taking the ratio to find $switch\ factor = c_{switched} / ODC$ and expressing it as a percentage. For every nF of capacitance taken from the ODC, one nF is given to both the Vdd and Vss capacitor. For resonance purposes, the total amount of PDN ODC is not changed because one or the other of the switches is always closed. Current (power) transients are accomplished by changing the switch factor as a function of time. If the switch factor is determined to be 10% in order to draw the prescribed dynamic current from the PDN, a 50% current reduction is generated by changing the switch factor to 5%. An 80% current transient is generated by changing the switch factor from 10% to 2%. The switched capacitor time domain load circuit accurately accounts for the clock edge currents, current transients, ODC, PDN current as a function of voltage and PDN damping. It should be emphasized that the clock edge current calculated from DC current and frequency is correct on the average but does not represent the minimum or maximum clock edge current. Much more sophisticated analysis is required to obtain minimum and maximum clock edge current.

q= I*T = I/freq

Figure 9 demonstrates the current paths when the output node of the time domain load switches from low-to-high (left side) and then when it switches from high-to-low (right side). On each edge, current is drawn from the ODC to charge up one of the capacitors. Also, one of the two capacitors is discharged on each edge. The resistor carries 2x current on each edge and 1x current is drawn from the ODC during each rise and fall of the output node. The 1x current drawn from the ODC represents the clock edge current drawn from the PDN of a real CMOS circuit during a clock cycle. Therefore, this time domain load is switched at half clock frequency in order to draw impulses of charge from the PDN, once per real clock cycle. The resistor sets the time constant and needs to be changed along with the switch factor and amount of load capacitance when simulating a power transient. It is calculated so that the RC time constant is 20% of the clock cycle. This changes the shape and determines the height of the current impulse (but not the charge or area under the curve) and is an important consideration when compared with the ESR for the ODC.

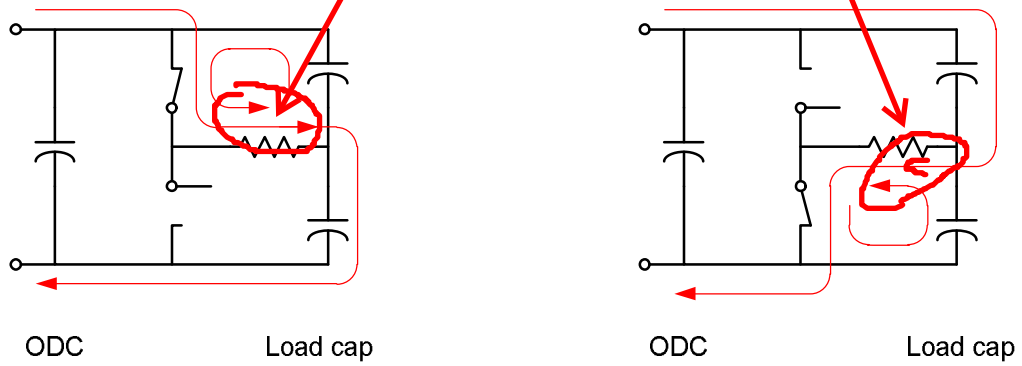


Figure 9: Current paths for switched capacitor time domain load circuit for the rising and falling edge of the output node. Current is drawn from the PDN (on-die capacitance) each time the circuit switches high or low.

Figure 10 shows voltage and current waveforms associated with the time domain load. The top panel (red) shows the output node voltage of the switching circuit together with the PDN voltage with some non-zero attachment of the ODC to an ideal voltage source. The instantaneous PDN voltage has an effect on the voltage and current waveforms as it must. The second panel (blue) shows the current through the resistor and is both positive and negative as current flows to the right and to the left. The third panel (green) is the current consumed from the ODC. Note that it is always positive and is half as much (20amps peak rather than 40 amps peak) as compared to the resistor current. The resistor is set to a value that insures the completion of charge transfer during the clock period. During the runtime of this simulation, the switch factor was changed several times. There was no switching activity for the 1st 10 nSec. The switch factor was 10% between 1nSec and 20nSec, switch to 5% from 20nSec to 30 nSec, and then alternates between 10% and 5% for the final 20nSec. This dramatically changes the clock edge current and causes current (power) transients to stimulate the PDN at 1/10 the clock frequency (5 clock cycles of high load current followed by 5 clock cycles of low load current). The bottom panel shows the resistor current together with the ODC current for easy comparison.

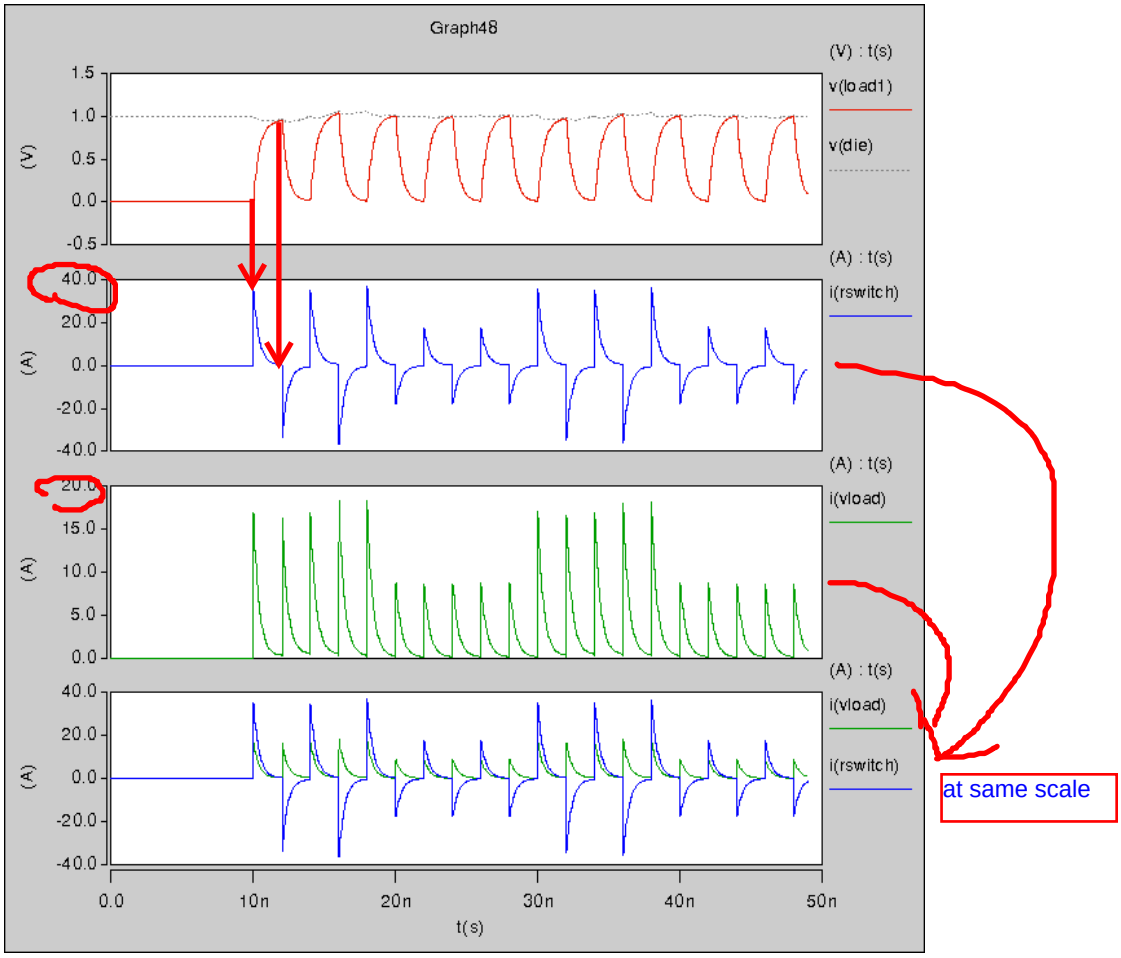


Figure 10: Voltage and current waveforms for switched capacitor time domain load. Red is output voltage. Blue is resistor current. Green is ODC current. Switch factor is used to produce current (power) transients at sub rate of clock to stimulate PDN resonances.

It is now time to combine the spread sheet calculations with Spice simulation. Figure 11 shows a complete PDN Resonance Calculator for a core PDN on an experimental chip that was measured in the lab. The left side has all the sections described above for die capacitance resonating with package/PCB inductance. It is for a 0.85V power supply at that consumes 1.1A leakage current and 27.2A dynamic current when the clock runs at 266 MHz. With a voltage tolerance of 5% and transient current of 50% of dynamic current, the target impedance is 3.1 mOhms. With the estimated die, package and PCB parameters, the switch factor is 7.9% for full power operation. Total capacitance, inductance and resistance are 1203nF, 385pH and 11.2mOhm respectively and produce a resonant peak at 6.6MHz. These parameters create some high figures of merit with an impedance peak of 22.7mOhms and PDN ratio of 7.3. Note that a socket has been included for lab purposes and dominates the resistance and contributes significant inductance. With the FPGA soldered to the board (no socket), the impedance peak would have been 31.9mOhms PDN ratio of 10.2 at the 8.1MHz resonant frequency. The socket more than doubles the series DC IR drop resistance and contributes greatly to the damping of the low frequency resonance.

On-package capacitors can help the situation. OPD parameters are shown on the right side of Figure xxx. With 4 similar package capacitors, the tall peak is split into two peaks, one at 3.7MHz and the other at 17.7 MHz. PDN ratios are respectable at 3.4 and 5.1.

Voltage	volts	0.85	
Leakage current per channel or bank	amps	1.1	
Dynamic AVG current per channel or bank*	amps	27.2	
AC calculations			
AC Tolerance	%	5	
Dynamic current per package net	amps	27.2	
transient (% of dynamic)	%	50	
AC Target impedance	mOhms	3.1	
clock frequency	MHz	266	
charge per cycle	nCoul/cycle	102.3	
load capactiance that switched	nF	120.3	
1st dip tolerance	%	10	
ODC required to stay within tolerance	nF	1203	
switch factor	%	7.9	
ODC	nF	1518	
Extrinsic ODC			
ODC ESR calculated	mOhm	1.0	
intentional ODR			
number of Vcc/Vss ball pairs		36	socket
Package Inductance	pH	16	131
Package resistance @ DC	mOhm	0.583	4.45
Package resistance @ resonance	mOhm	0.623	5.99
PCB via length	mils	116.1	
PCB via inductance	pH	168	
PCB via resistance @ resonance	mOhm	0.13	
PCB plane dielectric thickness	mils	3	
PCB plane squares		0.25	
PCB plane inductance	pH	23	
PCB plane resistance @ resonance	mOhm	0.33	
number of PCB caps		13	
average mounted cap inductance	pH	600	
PCB cap inductance	pH	46	
PCB cap resistance	mOhm	3.10	
Total Inductance	pH	385	
Total Resistance at resonance	mOhm	11.2	
Resonant frequency	MHz	6.6	
Resonant peak	mOhm	22.7	
Ratio (Z to Z_target)		7.3	
Q factor = sqrt(L/C)/R	Q	1.4	
1st dip as percent of Vcc	%	7.9	

OPD (On-Package) Capacitance (nF)	nF	2615
OPD ESL	pH	28
OPD ESR	mOhm	1.34
L1 (lower package)	pH	9
R1 @ non-OPD resonance	mOhm	0.084
R1 @ 1st OPD resonance	mOhm	0.063
L2 (upper package)	pH	8
R2 @ non-OPD resonance	mOhm	0.540
R2 @ 1st OPD resonance	mOhm	0.528
R2 @ 2nd OPD resonance	mOhm	0.571
L3 (OPD path)	pH	49
R3 @ 1st OPD resonance	mOhm	1.137
R3 @ 2nd OPD resonance	mOhm	2.598
PCB via resistance @ 1st resonance	mOhm	0.127
PCB plane resistance @ 1st resonance	mOhm	0.250
Total Inductance @ 1st resonance	pH	453
Total resistance @ 1nd resonance	mOhm	10.467
Total inductance @ 2nd resonance	pH	84
Total resistance @ 2nd resonance	mOhm	5.509
1st resonant frequency	MHz	3.7
1st resonant peak	mOhm	10
1st peak ratio		3.4
1st peak Q		1.0
2nd peak frequency	MHz	17.7
2nd peak resonant peak	mOhm	16
2nd peak ratio		5.1
2nd peak Q		1.7
1st dip from q=CV	V	0.067

Figure 11: Complete PDN Resonance calculator for PDN with package capacitor. A subset of these parameters are fed into a SPICE template file for the circuit topology of Figure 12 and produces the simulated results shown in Figures 13 and 14.

Spice Simulation

The switched capacitor time domain load circuit is used to stimulate the circuit topology shown in Figure 12. The circuit is divided into three major sections: die, package and PCB. The parameters for each of the circuit elements are calculated in the PDN Resonance Calculator spread sheet and fed into a Spice template for this topology. The die is separated into 3 capacitor types: gate, diffusion and metal. There is also a resistor from power to ground to consume leakage current. The package has four capacitors along with a star pattern of resistors and inductors to carry current. The PCB has via and

plane inductance as well as discrete capacitors. The voltage regulator module (VRM) is represented by an inductance that delivers current from the ideal voltage source with an appropriate time constant.

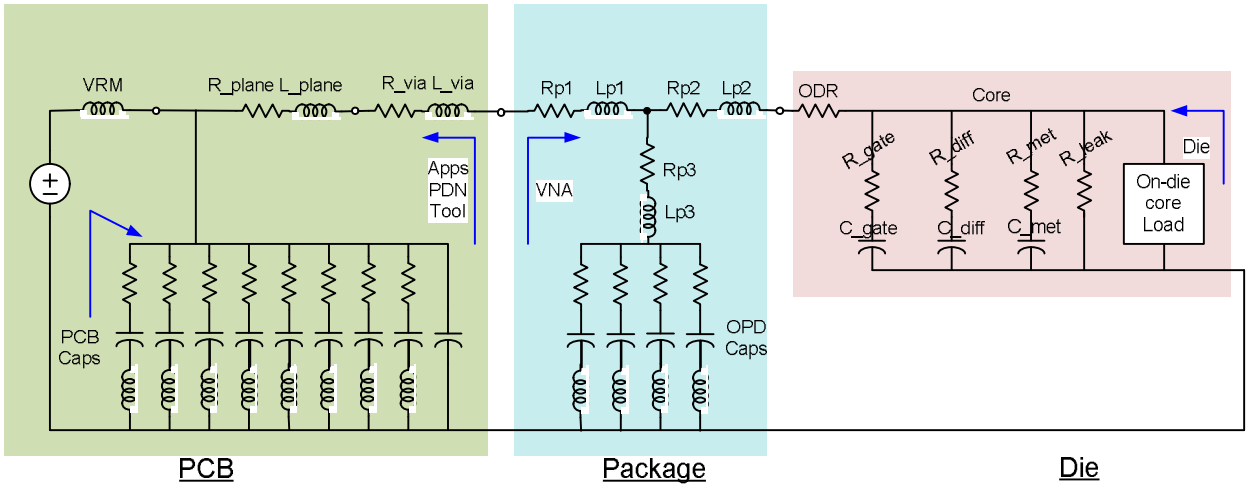


Figure 12: Circuit topology for PDN with package capacitor. Circuit parameter values are calculated in PDN Resonance Calculator for SPICE simulation.

This circuit is simulated to deliver the Spice results shown in Figure 13. The simulation seeks to bring out the several classifications of waveform signatures discussed in [1] including the 1st dip, burst and periodic burst transients. The top left panel gives the impedance compared to the target impedance. The four package capacitors sit on top of the major impedance peak that would have existed between the die capacitance and package/PCB inductance. The impedance peak is separated into two minor impedance peaks, one at 3.7 MHz and another at 17.7 MHz which compare favorably to the peak magnitude and frequencies calculated in the spread sheet. The bottom left panel shows the first dip PDN response when an impulse of current is consumed from the PDN by the die circuits when they are given a single clock edge. With one transition of the switched capacitor load, clock edge current is consumed from the PDN in about 1 nSec. The die voltage immediately drops to a level predicted by $q_{cycle} = CV = ODC_{nonswitching} \times V_{dip}$. The PDN then rings out in a damped sinusoid associated with the higher frequency peak. If the simulation had been allowed to run long enough, ringing at the lower frequency would also be evident.

For the right panel of Figure 13, the switched capacitor time domain load circuit has a load capacitance, frequency and switch factor and that was calculated by the PDN Resonance Calculator. Transients occur in a pattern that is meant to demonstrate the burst transient. Charge impulses are drawn from the PDN at the 266MHz clock frequency. Leakage plus dynamic current is initially about 25A until a 50% dynamic current transient occurs about 1.3 uSec into the run (switch factor changes and some of the load capacitance is moved back into ODC). The current abruptly drops to about 12A as seen on the bottom right panel. The burst transients are repeated twice. The top right panel shows the power supply voltage as seen by the CMOS circuits. The dashed lines show the desired 0.85 +-5% volts. The thick orange line is the result of many 1st dips at the 266 MHz rate. It is thicker when 25A

dynamic current is being drawn and thinner when 12A is being drawn. The damped sinusoid from the high frequency resonance is not visible on this time scale. The damped sinusoid observed as an envelope on the 1st dip noise is from the lower frequency resonant peak. DC IR drop causes the average voltage to sag especially at high current and is the reason why the load circuit does not draw the full 28.3A. The nominal voltage may be boosted up to compensate and bring the average voltage closer to 0.85V. As seen on the front edge of the graph, a fast transient from 0% to 100% load current will pull the circuit voltage down to less than 0.63V. This is essentially the step response of the entire PDN circuit.

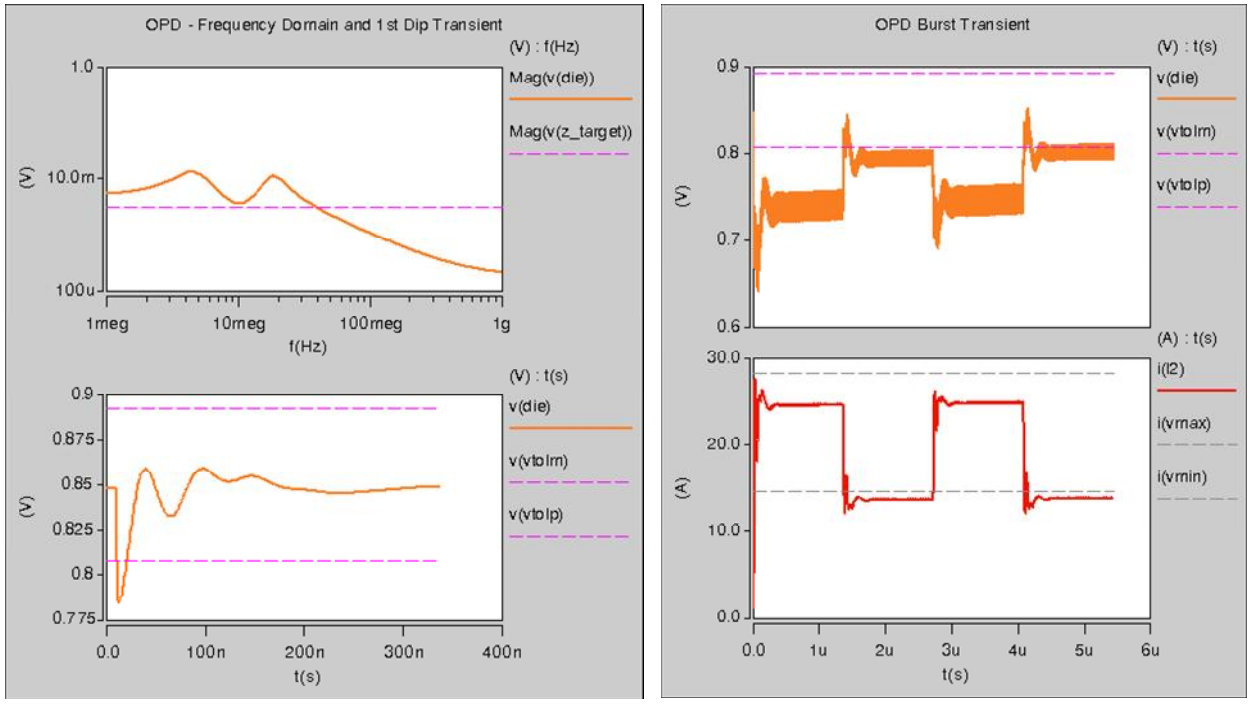


Figure 13: SPICE simulation results for PDN with package capacitor. Top left is frequency domain impedance compared to target impedance. Bottom left is 1st dip due to current impulse from one clock edge. Top left is PDN voltage seen by the die circuits as the switched capacitor load circuit draws current (power) transients with changes in switch factor. Bottom right is current through the die bumps for burst transient. Die voltage has thick waveform due to many current impulses being drawn from ODC but bump current is smoothed due to filtering action of ODC. DC voltage has sagged due to IR drop and reduced the PDN current.

As illustrated above, there are two peak frequencies where the PDN is the weakest, 3.7 MHz and 17.7 MHz. The most stressful thing that can be done to the PDN is to draw periodic burst transients at those frequencies. Figure 14 demonstrates this. In the left panel, the PDN is allowed to stabilize and then 50% current transients are drawn at the 3.7 MHz rate. The bottom trace shows the current alternating between approximately 12A and 25A which causes the PDN to have about 200mV p-p swing. The right side shows the same thing when similar current transients are taken at the 17.7 MHz rate. Note that both the 3.7MHz and 17.7 MHz current transients are far below the fundamental clock frequency of 266 MHz.

The simulations above take about 10 seconds CPU time running HSPICE on a 2.67 GHz laptop computer with 4GB RAM. The spread sheet calculations are instantaneous. Because of the assumptions and approximations made, these results will not be as accurate as sophisticated tools available in the industry, but it is possible to evaluate several different PDN scenarios in a 5 minute time period while sitting at your laptop. With this simple analysis, it is possible to locate the weak spots in a PDN and understand the nature of the current and power transients produced by CMOS loads.

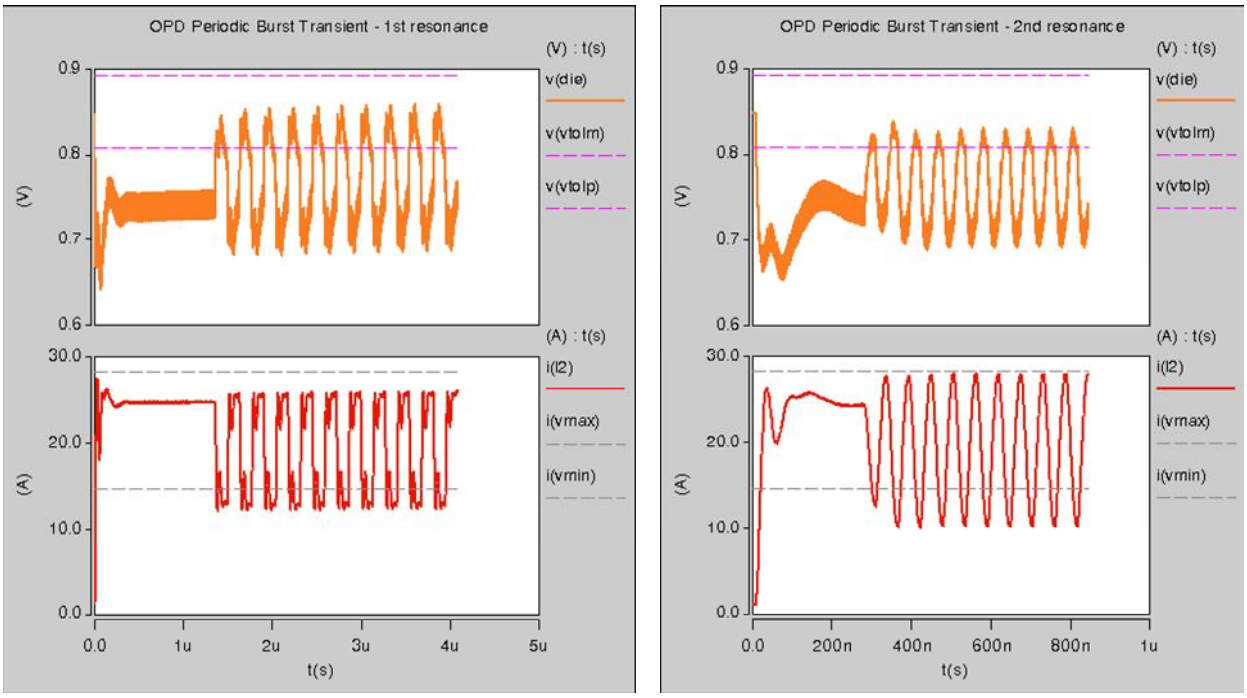


Figure 14: Periodic burst transients. The switch factor is changed at the lower resonant frequency (left side) and then the higher resonant frequency (right side) to stimulate PDN resonances.

Model to Hardware Correlation

Model to hardware correlation for the 1st dip is shown in Figure 15. Package and PCB sense lines have access to bump level metal for both Vcc and Vss. The signals are measured and subtracted at the scope and shown in the top trace of the right hand graph. The left hand graph is the simulated first dip. The predicted and measured values from the PDN Resonance Calculator spread sheet, Spice simulation and lab measurements are compared in the table below.

	PDN Resonance Calculator	Spice Simulation	Lab Measurements	Units
Depth of 1st dip	67.4	63.2	63.6	mV
Resonant Frequency	17.745	17.39	17.45	MHz

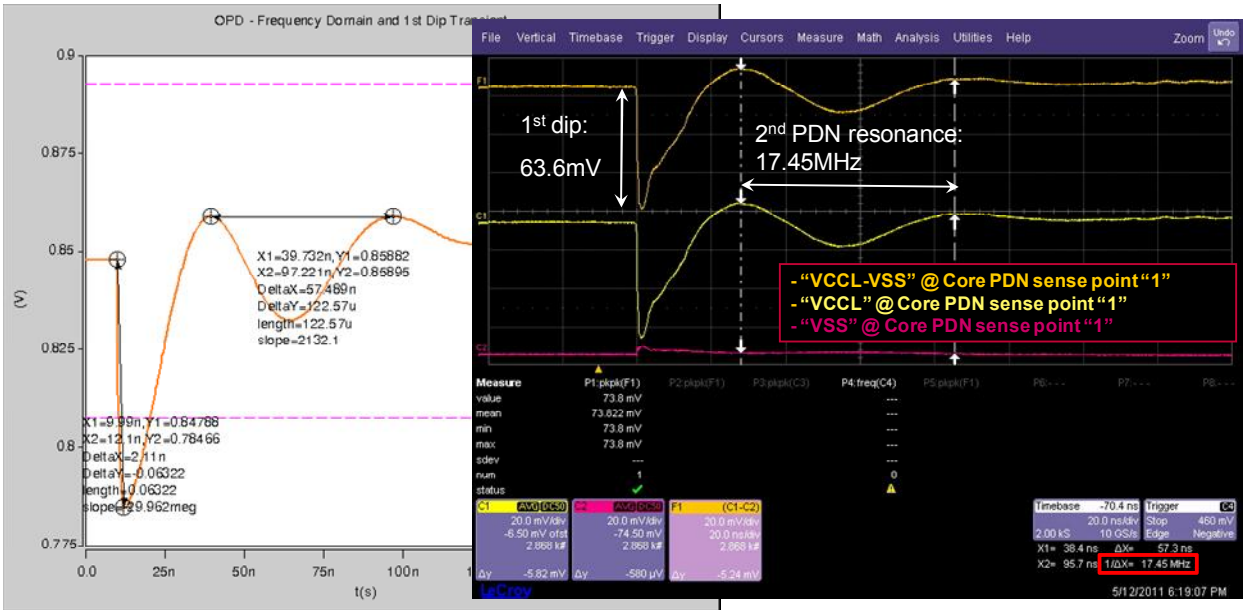


Figure 15: Model to hardware correlation for 1st dip.

Model to hardware correlation for the periodic burst transient at approximately 17MHz is shown in figure xxx. In this case, there was 100% transient current. Spice simulation predicts 261mV p-p but 243mV was measured. The circuit was stimulated slightly below the ~17.5MHz resonance because of clock granularity issues.

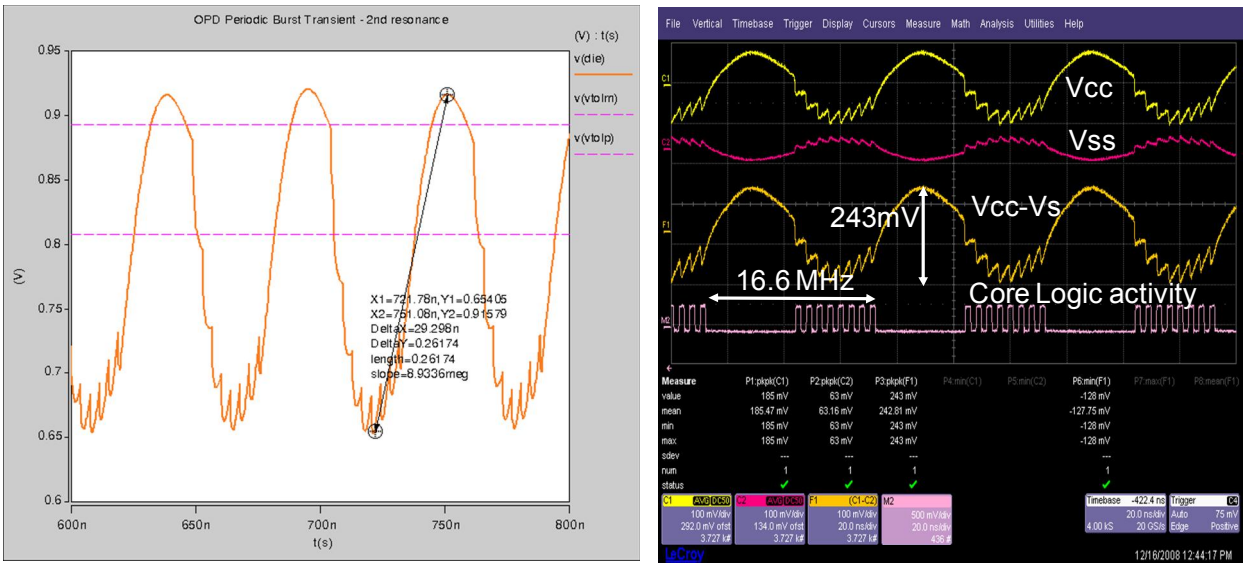


Figure 16: Model to hardware correlation for periodic burst transient.

Conclusions

A PDN Resonance Calculator has been developed to predict the PDN resonant peaks. Spread sheet calculations are based upon simple closed form formulas for series and parallel resonant circuits involving inductance, capacitance and resistance. Die capacitance is estimated from previous measurements in a given technology node or projections to the next node. Inductance and resistance of packaging and PCB structures are based upon twin lead transmission line and parallel plate structures. Calculations are made for geometries and materials for power planes, balls, vias, bumps, etc. Structures that dominate the PDN impedance peaks are easily identified. PDN figures of merit include the impedance peak, ratio of impedance to target impedance, q-factor, depth of 1st dip and DC IR drop. Spice parameters and a circuit topology are generated to match spread calculations. A switched capacitor time domain load was developed to apply the stimulus prescribed by the PDN Resonance Calculator. Simulations include frequency domain impedance compared to target impedance, and time domain 1st dip, burst and periodic burst transients. Lab measurements have been made and good model to hardware correlation achieved.

[1] S. Sun, L. D. Smith, P. Boyle, B. Krsnik, "On-Chip PDN Noise Characterization and Modeling,ò Santa Clara, CA, DesignCon 2010.

[2] L. D. Smith, S. Sun, M. Sarmiento, Z. Li, K. Chandrasekar, ñOn-Die Capacitance Measurements in the Frequency and Time Domains,ò Santa Clara, CA, DesignCon 2011

[3] John D. Kraus, Electromagnetics, Fourth Edition, McGrawī Hill, (1992).

[4] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol.22, No.3, P284, August 1999.