Voltage drop analysis using RedHawk is possible at different stages of the design flow. Use from the start of the design cycle can identify and fix power grid problems in the design when changes are inexpensive and when they do not affect a project's schedule. This also reduces the possibility of changes required in the later part of the design process when final static and dynamic voltage drop are performed for sign-off.

I. RedHawk flow for use in different stages of design cycle

RedHawk can be used as soon as any form of power routing is available. It can be used anywhere in the design flow starting from the floorplanning stage through initial and final cell placement stages. This allows for early feedback on the power grid integrity and identifies gross errors earlier. During the final stages of the design, RedHawk can be used for sign-off verification and localized fixing.

Table 1.1 shows different RedHawk settings required for these stages.

INPUT DATA	CASE 1 P/G routing; No cell placement	CASE 2 P/G routing; Initial cell placement; No SPEF; No STA	CASE 3 P/G routing; Initial cell placement; No STA	CASE 4 P/G routing; Cell placement, SPEF and STA available
Frequency	Frequency assigned to all instances GSR keyword: FREQUENCY	Instance frequency traced from clock roots GSR keyword: CLOCK_ROOTS	Instance frequency traced from clock roots GSR keyword: CLOCK_ROOTS	Instance frequency from PrimeTime report GSR keyword: STA_FILE
Input Slew	Constant slew assigned to all instances GSR keyword: INPUT_TRANSITION	Constant slew assigned to all instances GSR keyword: INPUT_TRANSITION	Constant slew assigned to all instances GSR keyword: INPUT_TRANSITION	Instance slew from PrimeTime report GSR keyword: STA_FILE
Signal loading	Instance loading computed based on interconnect and gate capacitance ratios GSR keyword: INTERCONNECT_GATE_CAP_RATIO	Instance loading computed based on Steiner tree wire length estimations GSR keyword: STEINER_TREE_CAP	Instance loading from SPEF file GSR keyword: CELL_RC_FILE	Instance loading from SPEF file GSR keyword: CELL_RC_FILE
LIB	User assigned LIB properties of block (Optional) GSR keyword: ADD_LEF_CELL_FOR_POWER, CUSTOM_LIBS_FILE	Cell library data from LIB files GSR keyword: LIB_FILES	Cell library data from LIB files GSR keyword: LIB_FILES	Cell library data from LIB files GSR keyword: LIB_FILES

Power calculation	Assign block power GSR keyword: BLOCK_POWER_FOR_SCALING	Assign/Calculate block/instance power GSR keyword: BLOCK_POWER_FOR_SCALING INSTANCE_POWER_FILE	Assign/Calculate block/instance power GSR keyword: BLOCK_POWER_FOR_SCALING INSTANCE_POWER_FILE	Assign/Calculate block/instance power GSR keyword: BLOCK_POWER_FOR_SCALING INSTANCE_POWER_FILE
Pad sources	Use PCELL/PAD/PLOC or DEF power/ground pins GSR keyword: ADD_PAD_LOC_FROM_TOP_DEF PAD_CELLS	Use PCELL/PAD/PLOC or DEF power/ground pins GSR keyword: ADD_PAD_LOC_FROM_TOP_DEF PAD_CELLS	Use PCELL/PAD/PLOC or DEF power/ground pins GSR keyword: ADD_PAD_LOC_FROM_TOP_DEF PAD_CELLS	Use PCELL/PAD/PLOC or DEF power/ground pins GSR keyword: ADD_PAD_LOC_FROM_TOP_DEF PAD_CELLS
APL characterization	Use LIB based profiles	Use design-independent APL library	Use design-independent APL library	Use design-dependent APL library
Current Distribution	Current distribution at pins (including boundary and area pins) of block	Current distribution at cell level	Current distribution at cell level	Current distribution at cell level
Timing Window	Instance switching within ½ clock period GSR keyword: FREQUENCY	Instance switching within ½ clock period GSR keyword: FREQUENCY, CLOCK_ROOTS	Instance switching within ½ clock period GSR keyword: FREQUENCY, CLOCK_ROOTS	Instance switching in TW from PrimeTime report GSR keyword: STA_FILE

Table 1 : RedHawk settings for different stages of design cycle

II. Illustration of RedHawk usage through a design cycle

RedHawk analysis for the cases described in the Table 1 is shown here on a test design.

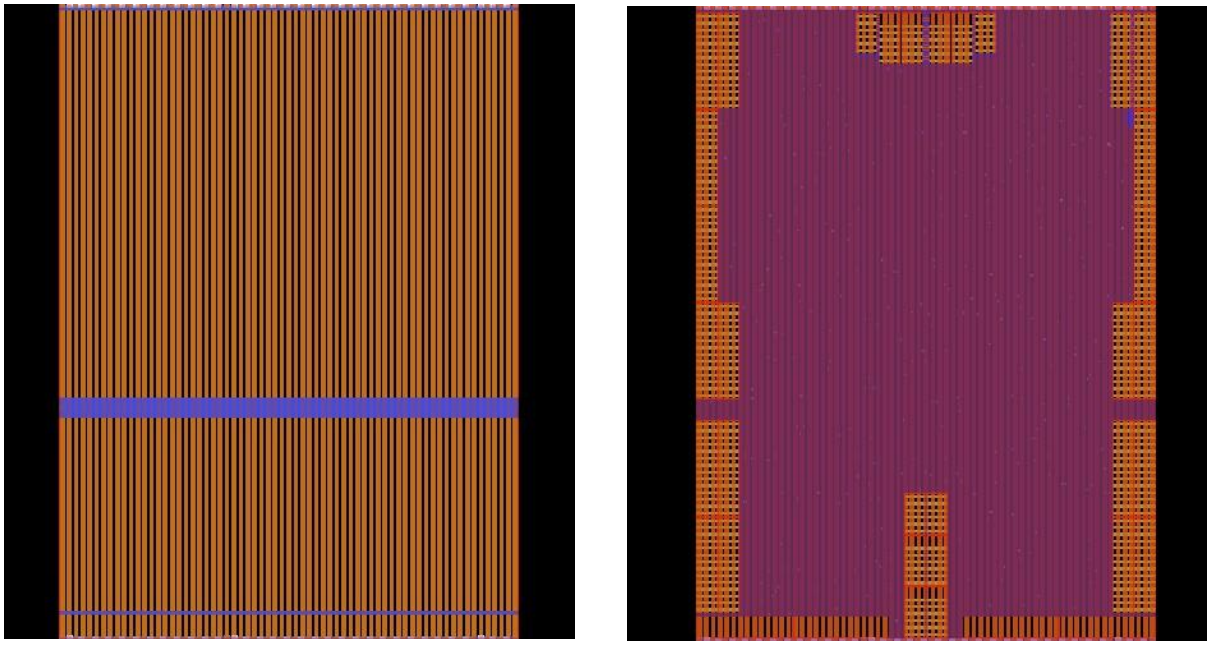

Figure 1. Layout view for case 1 (left) and case 2, 3, 4 (right)

Figure 1 shows a design that has power routing but no cell placement. The current distribution depends on the pin definitions in the design LEF. The PIN section of a block's LEF should contain all information of the power routes in the design. RedHawk will assign current sinks at via locations at the pins geometries and distribute the assigned power for the block among these current sinks.

In this particular case, the LEF view has vias only in select vertical Metal6 and horizontal Metal1 pins. The pin and via definitions in this LEF are **incomplete** and are not representative of the design power routes. This voltage drop from this model is **for illustration purpose only** since the current draw happens only in few areas of the design.

For case 2, 3, 4, cell placement is available which allows for a more realistic distribution of current based on every cell's power and location.

Increased level of accuracy can be obtained as more design information is available such as signal parasitic loading and instance frequency and slew information. Figures 2, 3 and Table 2 compare the voltage drop maps for the different cases.

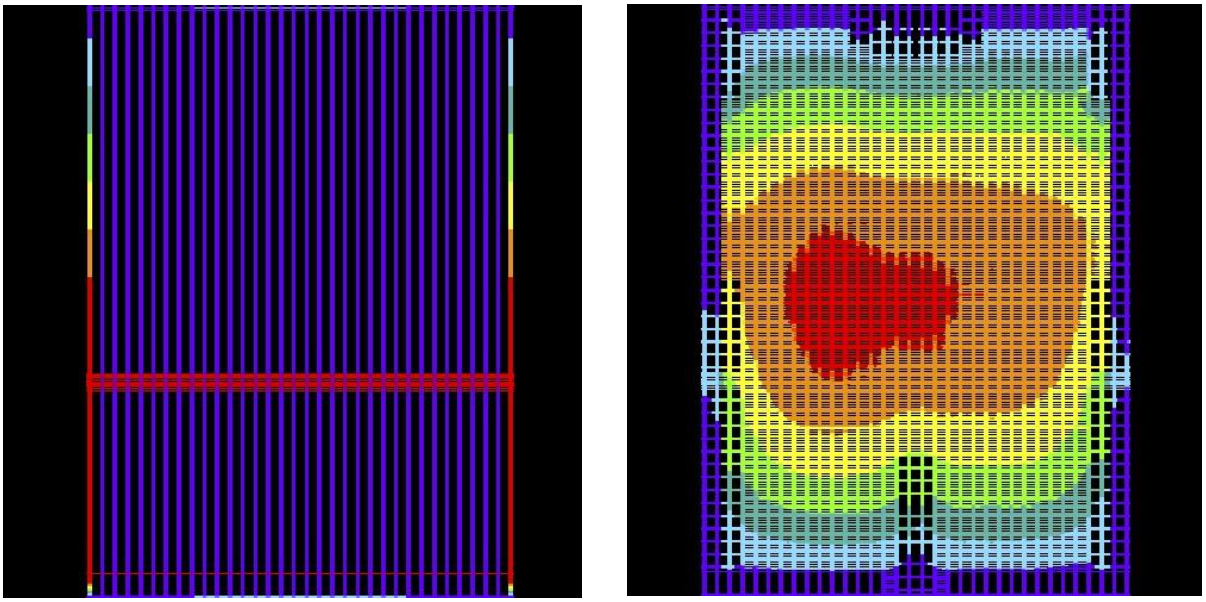

Figure 2. Static IR drop map on VDD network for case 1 (left) and case 2 (right)

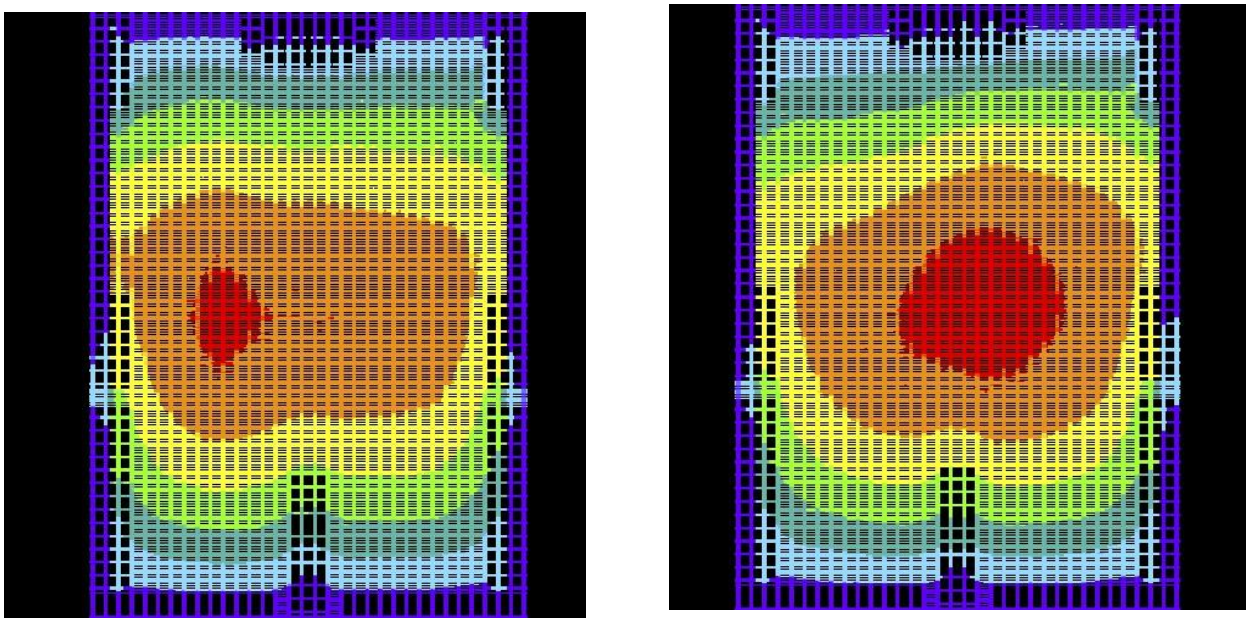

Figure 3. Static IR drop on VDD network for case 3 (left) and case 4 (right)

	CASE 1	CASE 2	CASE 3	CASE 4
Worst VDD drop	13.400mV	1.540 mV	1.537 mV	1.626mV
Worst VSS rise	6.500 mV	1.550 mV	1.550 mV	1.638 mV

Table 2 Comparison of voltage drops. Case 1 numbers reflect incompleteness of the LEF view.

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