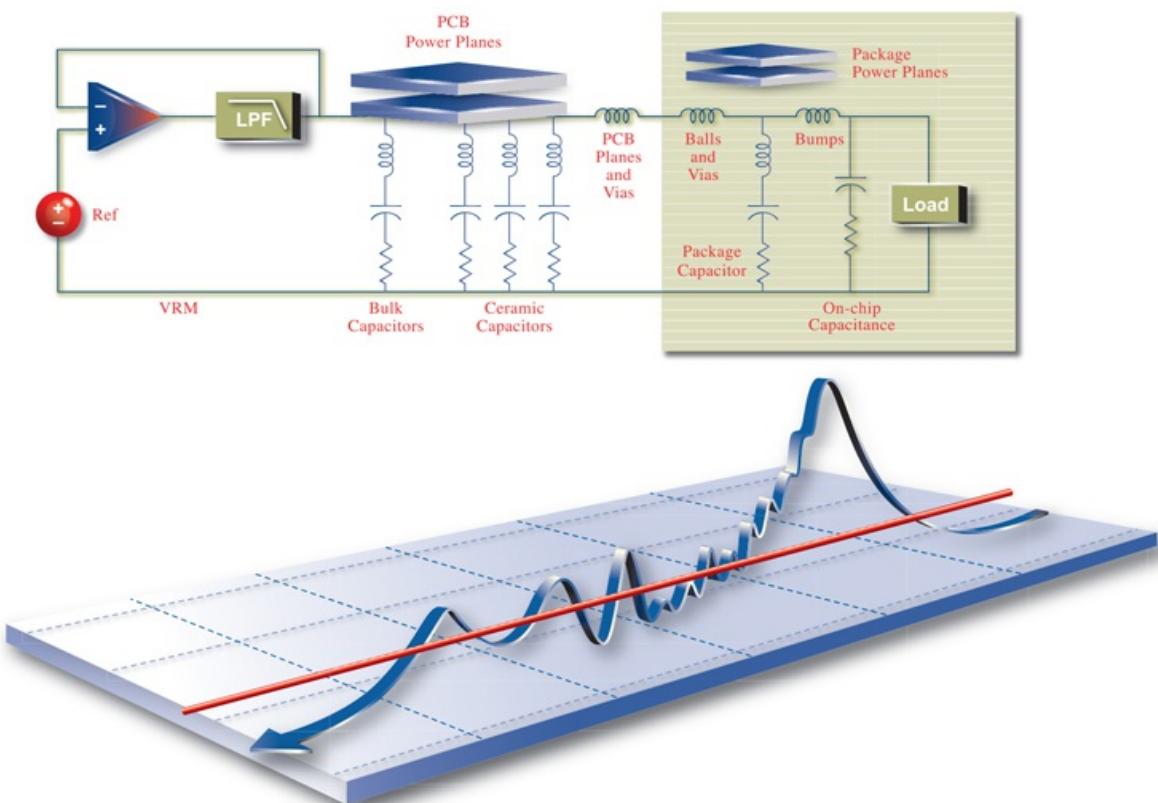


# Principles of Power Integrity for PDN Design

Robust and Cost Effective Design for High Speed Digital Products

SIMPLIFIED



Larry D. Smith • Eric Bogatin

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# **Principles of Power Integrity for PDN Design— Simplified**

**Robust and Cost Effective Design for  
High Speed Digital Products**

Larry D. Smith  
Eric Bogatin



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*The creation of this book took more than the 5,000 person-hours of writing, simulating, and editing and more than 500 hours of conference calls. We could not have done this without the unfailing support and confidence from our wives, Susan and Marty, who kept the faith and gave us encouragement even during the long hours of writing, rewriting, and more rewriting.*

*Larry would also like to dedicate this book to his father, who was his undergrad Professor of Electrical Engineering.*

# **Contents at a glance**

**Preface**

**Acknowledgments**

**About the Authors**

**Chapter 1** Engineering the Power Delivery Network

**Chapter 2** Essential Principles of Impedance for PDN  
Design

**Chapter 3** Measuring Low Impedance

**Chapter 4** Inductance and PDN Design

**Chapter 5** Practical Multi-Layer Ceramic Chip  
Capacitor Integration

**Chapter 6** Properties of Planes and Capacitors

**Chapter 7** Taming Signal Integrity Problems When  
Signals Change Return Planes

**Chapter 8** The PDN Ecology

**Chapter 9** Transient Currents and PDN Voltage Noise

**Chapter 10** Putting It All Together: A Practical  
Approach to PDN Design

**Index**

# **Contents**

## **Preface**

## **Acknowledgments**

## **About the Authors**

## **Chapter 1 Engineering the Power Delivery Network**

**1.1 What Is the Power Delivery Network (PDN) and Why Should I Care?**

**1.2 Engineering the PDN**

**1.3 “Working” or “Robust” PDN Design**

**1.4 Sculpting the PDN Impedance Profile**

**1.5 The Bottom Line**

**Reference**

## **Chapter 2 Essential Principles of Impedance for PDN Design**

**2.1 Why Do We Care About Impedance?**

**2.2 Impedance in the Frequency Domain**

**2.3 Calculating or Simulating Impedance**

**2.4 Real Circuit Components vs. Ideal Circuit Elements**

**2.5 The Series RLC Circuit**

**2.6 The Parallel RLC Circuit**

**2.7 The Resonant Properties of a Series and Parallel RLC Circuit**

**2.8 Examples of RLC Circuits and Real Capacitors**

**2.9 The PDN as Viewed by the Chip or by the**

## Board

2.10 Transient Response

2.11 Advanced Topic: The Impedance Matrix

2.12 The Bottom Line

References

## **Chapter 3 Measuring Low Impedance**

3.1 Why Do We Care About Measuring Low Impedance?

3.2 Measurements Based on the V/I Definition of Impedance

3.3 Measuring Impedance Based on the Reflection of Signals

3.4 Measuring Impedance with a VNA

3.5 Example: Measuring the Impedance of Two Leads in a DIP

3.6 Example: Measuring the Impedance of a Small Wire Loop

3.7 Limitations of VNA Impedance Measurements at Low Frequency

3.8 The Four-Point Kelvin Resistance Measurement Technique

3.9 The Two-Port Low Impedance Measurement Technique

3.10 Example: Measuring the Impedance of a 1-inch Diameter Copper Loop

3.11 Accounting for Fixture Artifacts

3.12 Example: Measured Inductance of a Via

3.13 Example: Small MLCC Capacitor on a Board

3.14 Advanced Topic: Measuring On-Die Capacitance

## 3.15 The Bottom Line

### References

## **Chapter 4 Inductance and PDN Design**

### 4.1 Why Do We Care About Inductance in PDN Design?

### 4.2 A Brief Review of Capacitance to Put Inductance in Perspective

### 4.3 What Is Inductance? Essential Principles of Magnetic Fields and Inductance

### 4.4 Impedance of an Inductor

### 4.5 The Quasi-Static Approximation for Inductance

### 4.6 Magnetic Field Density, B

### 4.7 Inductance and Energy in the Magnetic Field

### 4.8 Maxwell's Equations and Loop Inductance

### 4.9 Internal and External Inductance and Skin Depth

### 4.10 Loop and Partial, Self- and Mutual Inductance

### 4.11 Uniform Round Conductors

### 4.12 Approximations for the Loop Inductance of Round Loops

### 4.13 Loop Inductance of Wide Conductors Close Together

### 4.14 Approximations for the Loop Inductance of Any Uniform Transmission Line

### 4.15 A Simple Rule of Thumb for Loop Inductance

### 4.16 Advanced Topic: Extracting Loop Inductance from the S-parameters

4.17 The Bottom Line

References

## **Chapter 5 Practical Multi-Layer Ceramic Chip**

### **Capacitor Integration**

5.1 Why Use Capacitors?

5.2 Equivalent Circuit Models for Real Capacitors

5.3 Combining Multiple Identical Capacitors in Parallel

5.4 The Parallel Resonance Frequency Between Two Different Capacitors

5.5 The Peak Impedance at the PRF

5.6 Engineering the Capacitance of a Capacitor

5.7 Capacitor Temperature and Voltage Stability

5.8 How Much Capacitance Is Enough?

5.9 The ESR of Real Capacitors: First- and Second-Order Models

5.10 Estimating the ESR of Capacitors from Spec Sheets

5.11 Controlled ESR Capacitors

5.12 Mounting Inductance of a Capacitor

5.13 Using Vendor-Supplied S-parameter Capacitor Models

5.14 How to Analyze Vendor-Supplied S-parameter Models

5.15 Advanced Topics: A Higher Bandwidth Capacitor Model

5.16 The Bottom Line

References

# **Chapter 6 Properties of Planes and Capacitors**

6.1 The Key Role of Planes

6.2 Low-Frequency Property of Planes: Parallel Plate Capacitance

6.3 Low-Frequency Property of Planes: Fringe Field Capacitance

6.4 Low-Frequency Property of Planes: Fringe Field Capacitance in Power Puddles

6.5 Loop Inductance of Long, Narrow Cavities

6.6 Spreading Inductance in Wide Cavities

6.7 Extracting Spreading Inductance from a 3D Field Solver

6.8 Lumped-Circuit Series and Parallel Self-Resonant Frequency

6.9 Exploring the Features of the Series LC Resonance

6.10 Spreading Inductance and Source Contact Location

6.11 Spreading Inductance Between Two Contact Points

6.12 The Interactions of a Capacitor and Cavities

6.13 The Role of Spreading Inductance: When Does Capacitor Location Matter?

6.14 Saturating the Spreading Inductance

6.15 Cavity Modal Resonances and Transmission Line Properties

6.16 Input Impedance of a Transmission Line and Modal Resonances

6.17 Modal Resonances and Attenuation

6.18 Cavity Modes in Two Dimensions

6.19 Advanced Topic: Using Transfer Impedance  
to Probe Spreading Inductance

6.20 The Bottom Line

References

## **Chapter 7 Taming Signal Integrity Problems When Signals Change Return Planes**

7.1 Signal Integrity and Planes

7.2 Why the Peak Impedances Matter

7.3 Reducing Cavity Noise through Lower  
Impedance and Higher Damping

7.4 Suppressing Cavity Resonances with  
Shorting Vias

7.5 Suppressing Cavity Resonances with Many  
DC Blocking Capacitors

7.6 Estimating the Number of DC Blocking  
Capacitors to Suppress Cavity Resonances

7.7 Determining How Many DC Blocking  
Capacitors Are Needed to Carry Return  
Current

7.8 Cavity Impedance with a Suboptimal  
Number of DC Blocking Capacitors

7.9 Spreading Inductance and Capacitor  
Mounting Inductance

7.10 Using Damping to Suppress Parallel  
Resonant Peaks Created by a Few Capacitors

7.11 Cavity Losses and Impedance Peak  
Reduction

7.12 Using Multiple Capacitor Values to  
Suppress Impedance Peak

7.13 Using Controlled ESR Capacitors to Reduce  
Peak Impedance Heights

7.14 Summary of the Most Important Design Principles for Managing Return Planes

7.15 Advanced Topic: Modeling Planes with Transmission Line Circuits

7.16 The Bottom Line

References

## **Chapter 8 The PDN Ecology**

8.1 Putting the Elements Together: The PDN Ecology and the Frequency Domain

8.2 At the High-Frequency End: The On-Die Decoupling Capacitance

8.3 The Package PDN

8.4 The Bandini Mountain

8.5 Estimating the Typical Bandini Mountain Frequency

8.6 Intrinsic Damping of the Bandini Mountain

8.7 The Power Ground Planes with Multiple Via Pair Contacts

8.8 Looking from the Chip Through the Package into the PCB Cavity

8.9 Role of the Cavity: Small Boards, Large Boards, and “Power Puddles”

8.10 At the Low Frequency: The VRM and Its Bulk Capacitor

8.11 Bulk Capacitors: How Much Capacitance Is Enough?

8.12 Optimizing the Bulk Capacitor and VRM

8.13 Building the PDN Ecosystem: The VRM, Bulk Capacitor, Cavity, Package, and On-Die Capacitance

8.14 The Fundamental Limits to the Peak

## Impedance

8.15 Using One Value MLCC Capacitor on the Board-General Features

8.16 Optimizing the Single MLCC Capacitance Value

8.17 Using Three Different Values of MLCC Capacitors on the Board

8.18 Optimizing the Values of Three Capacitors

8.19 The Frequency Domain Target Impedance Method (FDTIM) for Selecting Capacitor Values and the Minimum Number of Capacitors

8.20 Selecting Capacitor Values with the FDTIM

8.21 When the On-Die Capacitance Is Large and Package Lead Inductance Is Small

8.22 An Alternative Decoupling Strategy Using Controlled ESR Capacitors

8.23 On-Package Decoupling (OPD) Capacitors

8.24 Advanced Section: Impact of Multiple Chips on the Board Sharing the Same Rail

8.25 The Bottom Line

References

## **Chapter 9 Transient Currents and PDN Voltage Noise**

9.1 What's So Important About the Transient Current?

9.2 A Flat Impedance Profile, a Transient Current, and a Target Impedance

9.3 Estimating the Transient Current to Calculate the Target Impedance with a Flat Impedance Profile

9.4 The Actual PDN Current Profile Through a Die

9.5 Clock-Edge Current When Capacitance Is Referenced to Both Vss and Vdd

9.6 Measurement Example: Embedded Controller Processor

9.7 The Real Origin of PDN Noise—How Clock-Edge Current Drives PDN Noise

9.8 Equations That Govern a PDN Impedance Peak

9.9 The Most Important Current Waveforms That Characterize the PDN

9.10 PDN Response to an Impulse of Dynamic Current

9.11 PDN Response to a Step Change in Dynamic Current

9.12 PDN Response to a Square Wave of Dynamic Current at Resonance

9.13 Target Impedance and the Transient and AC Steady-State Responses

9.14 Impact of Reactive Elements, q-Factor, and Peak Impedances on PDN Voltage Noise

9.15 Rogue Waves

9.16 A Robust Design Strategy in the Presence of Rogue Waves

9.17 Clock-Edge Current Impulses from Switched Capacitor Loads

9.18 Transient Current Waveforms Composed of a Series of Clock Impulses

9.19 Advanced Section: Applying Clock Gating, Clock Swallowing, and Power Gating to Real CMOS Situations

[9.20 Advanced Section: Power Gating](#)

[9.21 The Bottom Line](#)

[References](#)

## **Chapter 10 Putting It All Together: A Practical Approach to PDN Design**

[10.1 Reiterating Our Goal in PDN Design](#)

[10.2 Summary of the Most Important Power Integrity Principles](#)

[10.3 Introducing a Spreadsheet to Explore Design Space](#)

[10.4 Lines 1–12: PDN Input Voltage, Current, and Target Impedance Parameters](#)

[10.5 Lines 13–24: 0th Dip \(Clock-Edge\) Noise and On-Die Parameters](#)

[10.6 Extracting the Mounting Inductance and Resistance](#)

[10.7 Analyzing Typical Board and Package Geometries for Inductance](#)

[10.8 The Three Loops of the PDN Resonance Calculator \(PRC\) Spreadsheet](#)

[10.9 The Performance Figures of Merit](#)

[10.10 Significance of Damping and q-factors](#)

[10.11 Using a Switched Capacitor Load Model to Stimulate the PDN](#)

[10.12 Impulse, Step, and Resonance Response for Three-Peak PDN: Correlation to Transient Simulation](#)

[10.13 Individual q-factors in Both the Frequency and Time Domains](#)

[10.14 Rise Time and Stimulation of Impedance Peak](#)

## 10.15 Improvements for a Three-Peak PDN:

Reduced Loop Inductance of the Bandini  
Mountain and Selective MLCC Capacitor  
Values

## 10.16 Improvements for a Three-Peak PDN: A Better SMPS Model

## 10.17 Improvements for a Three-Peak PDN: On- Package Decoupling (OPD) Capacitors

## 10.18 Transient Response of the PDN: Before and After Improvement

## 10.19 Re-examining Transient Current Assumptions

## 10.20 Practical Limitations: Risk, Performance, and Cost Tradeoffs

## 10.21 Reverse Engineering the PDN Features from Measurements

## 10.22 Simulation-to-Measurement Correlation

## 10.23 Summary of the Simulated and Measured PDN Impedance and Voltage Features

## 10.24 The Bottom Line

## References

# Index

# Preface

## THE FOCUS OF THIS BOOK

Power integrity is a confusing topic in the electronics industry—partly because it is not well-defined and can encompass a wide range of problems, each with their own set of root causes and solutions. There is universal agreement that the field of power integrity includes everything from the voltage regulator module (VRM) to the on-die core power rails and on-die capacitance.

Between the VRM and die are interconnects on the package and board, which often carry discrete capacitors with their associated mounting inductance. The power distribution network (PDN) refers to all interconnects (usually inductive), the intentional energy storage devices (usually capacitive), and loss mechanisms (damping) between the VRM and the on-die Vdd-Vss power rails.

Power integrity is all about the quality of the power seen by the circuits on the die. What about noise created on the board power and ground planes by signals passing through cavities? Is this a signal integrity problem or a power integrity problem? Is the voltage noise generated by I/O switching currents and seen by the on-die Vcc and Vss rails a power integrity or signal integrity problem? Current that comes in through the common package lead inductance, which is ultimately connected to the VRM, generates this noise, which is sometimes referred to as switching noise or ground bounce.

This gray area between signal and power integrity has a profound impact on solutions that are offered for “power integrity” problems. Adding decoupling

capacitors on the board often provide a solution for reducing Vdd core noise but seldom improve the cavity noise induced by high bandwidth signals. In general, board-level capacitors offer little or no improvement to return-plane bounce noise. In some cases, the parallel resonances they create can actually increase the cavity-to-signal cross talk.

The first step to solving a problem is to clearly identify the problem and then correctly identify its root cause. A well-defined problem is often only a few steps away from a solution. Efficient solutions to problems are developed based on the actual root cause.

This book focuses on the specific power integrity problems related to noise on the Vdd rail, which powers the on-die core logic and enables it to perform functions. The gates powered by the on-die Vdd rail switch signals that communicate to other gates on the same die, and do not necessarily travel off die as I/O. Transient current caused by core activity causes noise on the Vdd rail, which is sometimes referred to as “self-aggression.” The principles, analysis methods, and recommended best design practices to minimize this problem can also apply to other signal integrity, power integrity, and EMI problems; however, the focus in this book is on self-aggression of the Vdd rail.

## **OTHER POWER INTEGRITY OR SIGNAL INTEGRITY PROBLEMS AND SOLUTIONS**

The term “power integrity” paints with too broad a brush to address all problems with general design recommendations. Instead, we need clear identification of the specific problem we are trying to solve, along with best design practices for each specific problem.

Some peripheral problems in a complete system design are sometimes categorized as power integrity:

- Noise on the Vcc-Vss rails from I/O switching, ground bounce, and switching noise: self-aggression by the Vcc rails
- Noise on the VRM output from its changing load impedance: self-aggression by the VRM
- Signal distortion as it travels through return path discontinuities: self-aggression by signals paths
- Noise from the power rails and VRM transferring onto and polluting the board-level PDN interconnects
- Cross talk between the voltage noise on the package and board-level PDN interconnects from all sources, coupling onto a Vdd rail
- Cross talk between the voltage noise on the package and board-level PDN interconnects from all sources, coupling to an I/O power rail
- Cross talk between the voltage noise on the package and board-level PDN interconnects and a signal which couples to the PDN

Each of these problems has a very different root cause and a different set of best design practices to reduce their impact. These topics are sometimes lumped under the signal integrity umbrella and sometimes the power integrity umbrella.

To avoid the possible confusion of assuming all power integrity problems are the same—and hence one set of solutions apply to all problems—engineers and designers should get in the habit of carefully articulating which problem is being addressed rather than using the general heading of power integrity or signal integrity.

A wealth of PDN design recommendations are offered in publications, at conferences, or by your favorite uncle. Blindly following any of them is dangerous. Unfortunately, many recommendations are either wrong or contradictory. This is partly because they are

oriented toward only one of the specific problems listed above, but incorrectly generalized as the cure for all power integrity problems.

Be specific about the problem, the root cause, and the recommended best design practices.

## MEETING THE CHALLENGE OF ROBUST PDN DESIGN

A poorly designed PDN can result in the product failing, usually at the worst possible time. PDN failures are difficult to diagnose because they are hard to reproduce. Sometimes they result from a very specific combination of microcode running a specific set of problems. This makes it difficult to “test in the quality” of a PDN. A robust PDN must be designed in.

Some PDNs may actually be robust with no additional considerations on the board other than a low impedance VRM. Other PDNs may require very specific combinations of capacitor values mounted in very specific positions, and then only run restricted microcode to be robust.

Every PDN is unique and has its own story. Each has its own combination of performance requirements, chip features, microcode, and design constraints on cost, performance, risk, and schedule. This makes it difficult to efficiently design a robust PDN by just following someone else’s best design principles. That’s where a solid design methodology plays an important role.

A common answer to many questions in any engineering field, including power integrity, is “...it depends.” The only way to answer “...it depends” questions is by clearly defining the problem and then putting in the numbers and performing analysis of the specific problem, the root cause, and the various solution options.

The most efficient design process for the PDN (and most aspects of high-performance product design) so that there is a high probability of “getting it right the first time” is based on four elements:

- Start with the established best design practices.
- Understand the essential principles of how signals interact with interconnects—basically the principles of applied Maxwell’s Equations.
- Identify the common problems to avoid and their root causes.
- Leverage analysis tools to efficiently explore design space and find the appropriate cost-performance-risk-schedule tradeoffs for each specific product’s details and constraints.

The goal for many projects is to find an acceptable design that meets the performance objectives at acceptable cost, risk, and schedule.

This book is designed to be a handbook for the practicing power integrity engineer to establish a firm foundation in the principles of power integrity, identify the root cause of the common problems found in PDN design, follow the best design practices, and perform engineering trade-off analysis to balance cost, performance, schedule, and risk.

## **WHO THIS BOOK IS REALLY FOR**

As with all books in the Prentice Hall “Simplified” series, *Principles of Power Integrity for PDN Design—Simplified* minimizes the mathematical formalism to reveal the important engineering principles behind power integrity. If you are looking for detailed mathematical derivations and complicated numerical simulations, look elsewhere.

This is not to say that mathematical rigor is not

important—every student of electrical engineering should have studied this in college. As a practicing engineer, being able to apply these principles to solve real problems is often more important than deriving every detail from Maxwell’s Equations.

This book is based on a specific design methodology for high-performance systems. The starting place is to use established best design principles. Unfortunately, every design is custom, they each have their own story. They each have their own set of performance goals and cost, risk, and schedule constraints. This means you cannot blindly follow every design guideline, but must use your engineering judgement.

This does not mean grab your 3D full-wave simulator and simulate everything. This would be an incredibly inefficient process with no guarantee of successfully converging on an acceptable solution.

The basis of engineering judgement is understanding the essential principles—which are really applied Maxwell’s Equations—identifying the problems to avoid and their root cause, and leveraging analysis tools to efficiently explore design space to find an acceptable answer. This book is a guideline for applying this methodology to designing robust PDN systems.

As two experts in the signal and power integrity fields, with more than 70 years of engineering experience between us, we have distilled into this book what we consider to be the most important engineering principles upon which power integrity engineering is based.

Our experience is based on having personally worked on many designs, helping many engineers, and having to rescue many failed designs. We’ve seen the consequence of carrying around misconceptions based on a recommendation from the person you sat next to on

your last airplane flight who has a nephew who once built a board that worked so must have done it correctly.

Engineers involved in the design process must become their own expert and not rely on what the last expert they talked to said about a product that has nothing to do with the one they are currently working on.

Enough mathematics is included to accelerate a practicing engineer up the learning curve to immediately perform trade-off analysis and identify what is important—and equally of value—what is not important.

Equations are used as a shorthand to clarify which terms are important and how they combine to influence the result. They are used to restate the principle with more detail. They are the first line of attack when “putting in the numbers.”

Where possible, we show examples of simple simulations to illustrate the analytical approximations. Where appropriate, measurements from test vehicles and real systems are introduced to provide an anchor to reality that these principles actually work, as long as they are applied with good engineering judgement.

***If PDN design is in your future, you'll find this book essential to your success.***

## **FIVE FEATURES THAT MAKE THIS BOOK EASY TO NAVIGATE**

To engineer a more efficient process for using this book, we've incorporated five valuable features.

As with all books in the Prentice Hall Simplified series, we've tried hard to take the complexity of real-world problems and break them down to their simplest form to identify the essential principles and how they apply. Approximations are included as a way of

quantifying the principles and applying them to specific problem examples. They are a first step to help calibrate our engineering judgement so we can make sense of simulation results.

Where possible, the results of an analysis are shown graphically in figures. The figures with their extended captions tell a story in parallel with the text and equations.

In each section, we've pulled out what we consider to be some of the most important conclusions or observations as TIPS. These reinforce the section's essences and make it easy when skimming the book to pick up or recall the highlights.

At the end of each chapter we've added "The Bottom Line" as a quick 10-point summary of the chapter's most important points. After reading the chapter, the 10 points should be obvious and expected.

Finally, the PDN resonance calculator spreadsheet used extensively in the last chapter is available on the book's companion web site at [informit.com/title/9780132735551](http://informit.com/title/9780132735551) and on the [www.beTheSignal.com](http://www.beTheSignal.com) web site. Additional supplemental information on power integrity is available on these two web resource sites.

## OUTLINE FOR THIS BOOK

*Principles of Power Integrity for PDN Design—Simplified* is organized as a training manual for the power integrity engineer to learn the strategies, tactics, essential principles, and skills for successful PDN design.

Chapter 1, "Engineering the Power Delivery Network," provides a brief perspective on what the PDN is and why engineering a low impedance is so important. We introduce the idea of the impedance profile as an

important design feature and indicator of PDN performance. We also introduce the most important figure of merit to describe the PDN design goal—the target impedance. Our goal is to engineer a PDN impedance profile below the target impedance with acceptable cost, risk, and meet performance and schedule targets.

Chapter 2, “Essential Principles of Impedance for PDN Design,” provides a thorough review of impedance, which is the fundamental basis of evaluating a robust PDN. In particular, the properties of series and parallel RLC circuits are reviewed. These circuits determine the fundamental features of the PDN impedance profile. Simulation of the impedance profile of a collection of components is introduced as an essential skill. We show how any free version of a SPICE simulator can be used as an impedance analyzer.

Chapter 3, “Measuring Low Impedance,” introduces measurement techniques for low impedance. Typical PDN target impedances range from  $1 \Omega$  to lower than  $1 \text{ m}\Omega$ . Special techniques are used to measure the very low impedance of components and the entire PDN ecology.

Chapter 4, “Inductance and PDN Design,” covers the essence of inductance, what it is, how it is affected by physical design, and how to estimate the loop inductance from physical design features. Engineering low loop inductance in the PDN interconnects is an important way to reduce peak impedances. When inductance cannot be eliminated, it is important to know how much there is so that its impact can be evaluated.

Chapter 5, “Practical Multi-Layer Ceramic Chip Capacitor Integration,” reviews the properties of capacitors and how they behave individually and

together. They are the primary component used to sculpt the impedance profile and manage the peaks. The five general tactics to reducing peak impedances from combinations of capacitors are introduced. In particular, the critical step of engineering low mounting inductance is introduced.

Chapter 6, “Properties of Planes and Capacitors,” introduces the properties of critically important power and ground planes in the PDN interconnect, and how the capacitors interact with the planes. The most important property of the planes—the spreading inductance—is explored in detail. In addition, we show that the plane cavity resonances are not important at all for the quality of power seen by die circuits.

Chapter 7, “Taming Signal Integrity Problems When Signals Change Return Planes,” explores another function of PDN interconnects: to provide a low impedance for the signal return currents. Switching noise, a form of ground bounce, is a problem that results in noise on the planes when signals pass through them. This is the realm of signal integrity and is separate and distinct from power integrity. Because the root cause of switching noise is different from PDN noise on the core Vdd rails, the solutions are very different. We are careful to distinguish this important signal integrity problem from power integrity.

Chapter 8, “The PDN Ecology,” addresses the most important PDN feature: the peak impedance created by the on-die capacitance and the package lead inductance, and what can be done at the board level to reduce this peak. We show how to leverage all the design principles introduced up to this point to overcome the limitations created by this peak.

Chapter 9, “Transient Currents and PDN Voltage Noise,” describes the features of the current drawn by

CMOS circuitry, and how this current spectrum interacts with the PDN impedance profile. Three important transient current waveforms are introduced: a clock-edge impulse, a step transient current, and a repetitive square wave of current. These waveforms interact with different PDN features. Most importantly, we show how the three elements—impedance profile, transient current, and stimulated voltages—all interact. Knowing any two elements enables us to evaluate the third.

Chapter 10, “Putting It All Together: A Practical Approach to PDN Design,” brings together all the principles and processes to illustrate how to design the specific features in the PDN to meet the performance goals. In particular, a simple spreadsheet-based analysis technique is introduced, which dramatically speeds up the process of creating a first-pass design. We walk through a few design scenarios and show an example of the power of the principles introduced in this book. From measured data, PDN parameters are developed that match measured performance incredibly well.

*Larry Smith and Eric Bogatin*

January, 2017

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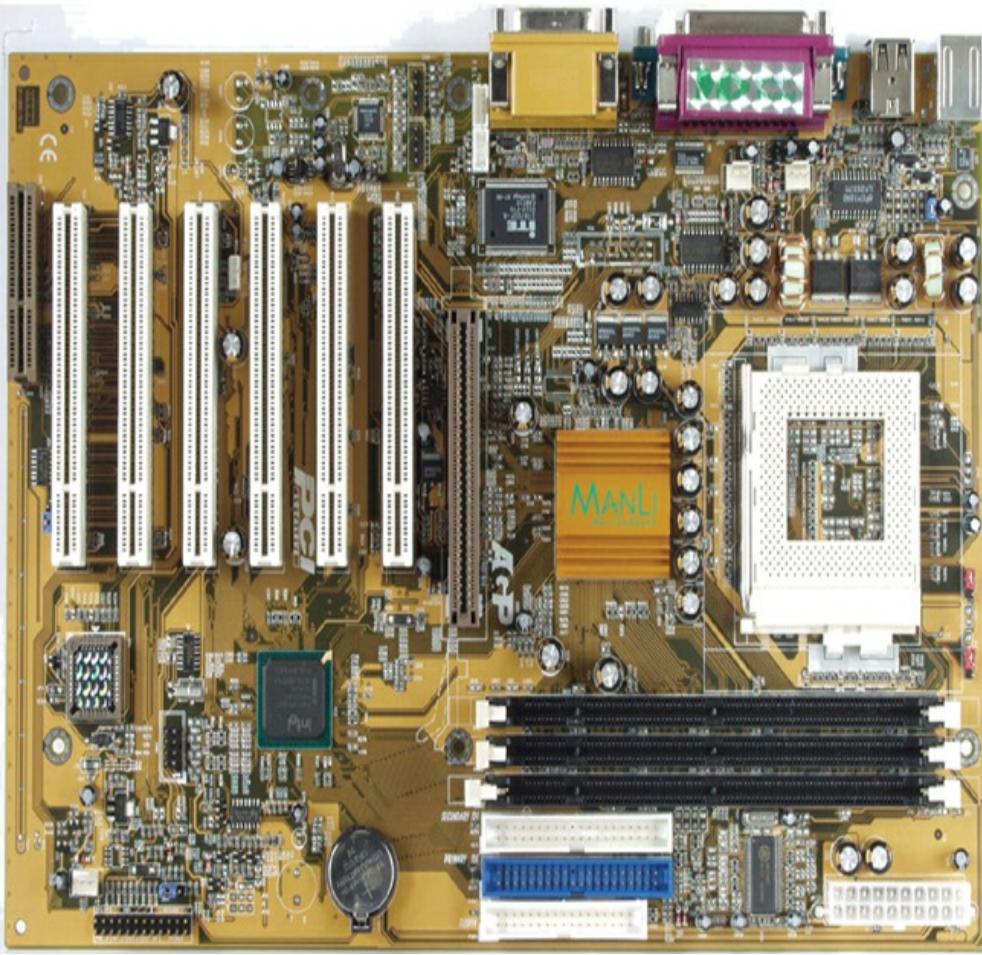
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# **Chapter 1. Engineering the Power Delivery Network**

## **1.1 WHAT IS THE POWER DELIVERY NETWORK (PDN) AND WHY SHOULD I CARE?**

The power delivery network consists of all the interconnects in the power supply path from the voltage regulator modules (VRMs) to the circuits on the die. Generally, these include the power and ground planes in the boards, cables, connectors, and all the capacitors associated with the power supply. Figure 1.1 is an example of a typical computer board with multiple VRMs and paths delivering the power and ground to the pads of all the active devices.



**Figure 1.1** A typical computer motherboard with multiple VRMs and active devices. The PDN includes all the interconnects from the pads of the VRMs to the circuits on the die.

The purpose of the PDN is to

- Distribute low-noise DC voltage and power to the active devices doing all the work.
- Provide a low-noise return path for all the signals.
- Mitigate electromagnetic interference (EMI) problems without contributing to radiated emissions.

In this book, we focus on the first role of the PDN: to distribute a DC voltage and power to all the active devices requiring power and to keep the noise below an acceptable level. Unsuccessful noise control on the PDN will contribute to contraction of the eye of any signal. The amplitude of the eye in the vertical direction collapses from voltage noise. The time of the signal

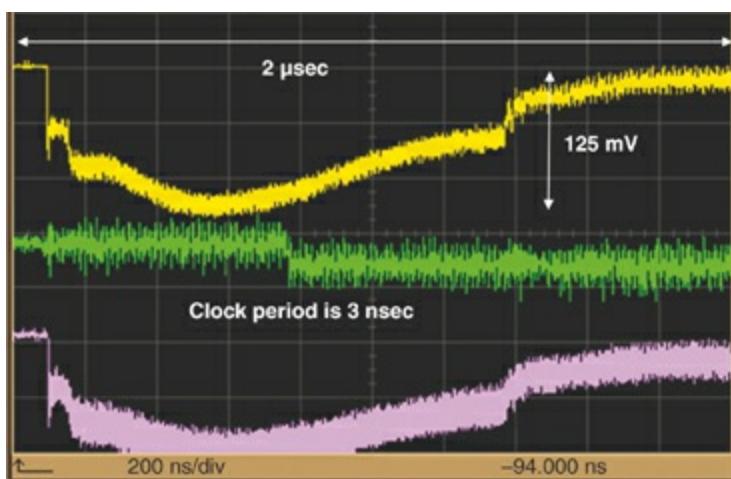
crossing a reference spreads out in the horizontal direction creating jitter and reduction of the eye opening. Internal core circuits might suffer setup and hold-time errors, leading to functional failures.

**Tip**

The consequence of not correctly designing the PDN is increased bit error ratios from enhanced vertical noise and jitter on both I/O circuits and internal-to-the-chip circuits. Excessive horizontal noise in core circuits might lead to setup and hold-time violations.

Depending on the circuit of the switching gates, the PDN noise will add to the signal coming from the transmitter (TX). This can also appear as noise on the voltage reference at the receiver (RX). In both cases, the PDN noise will reduce the noise margin available from other sources.

Figure 1.2 shows an example of the measured voltage noise between the core power and ground (Vdd and Vss) rails on a microprocessor die at three different on-die locations and two different voltage rails. In this example, the voltage noise is 125 mV. In many circuits, a large fraction of this voltage noise will appear superimposed on the signal at the RX.

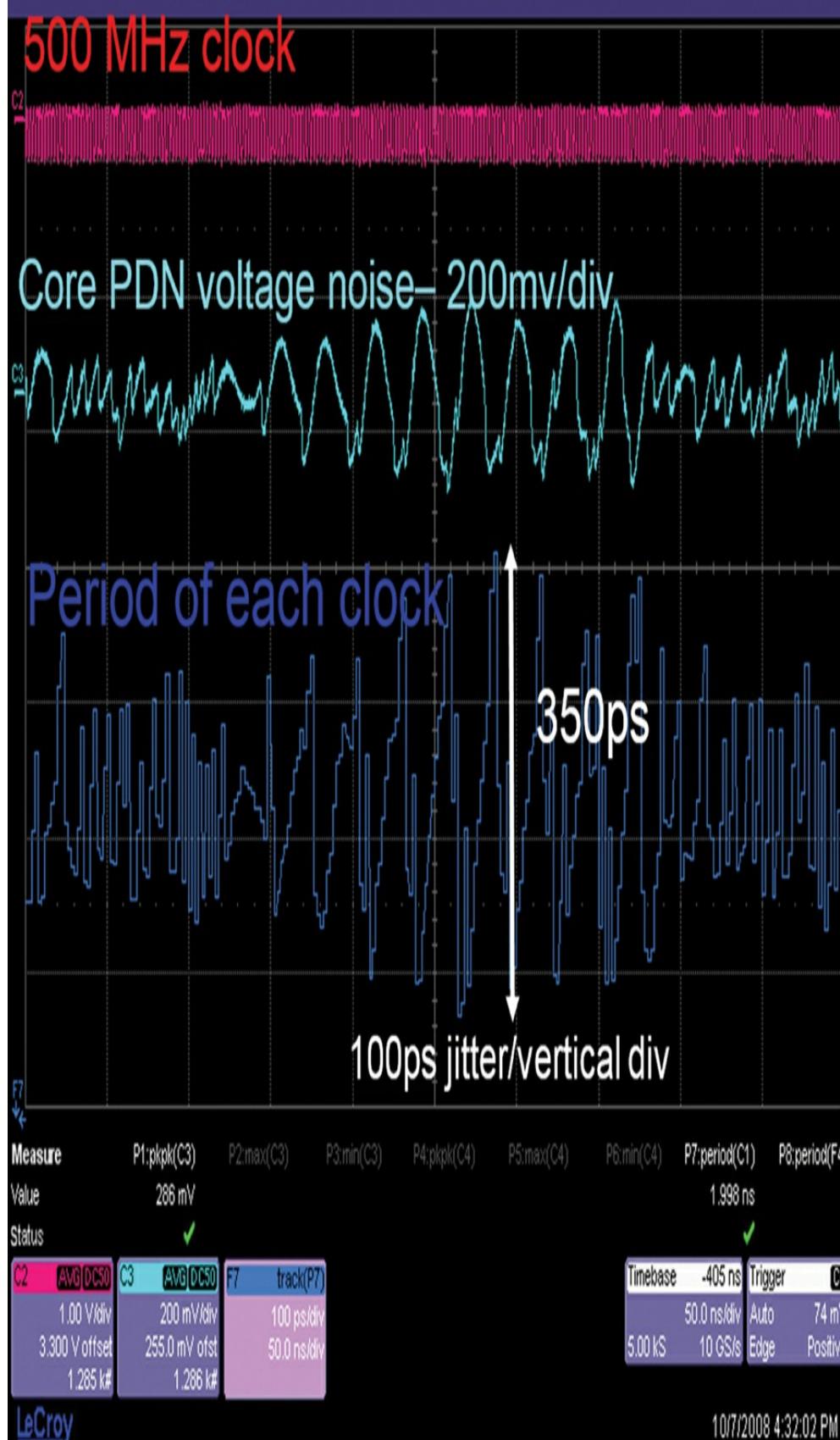


**Figure 1.2** Example of the noise between the Vdd and Vss rails in a microprocessor running at 300 MHz clock, measured at three different locations. More than 125 mV of noise is present.

Even if this noise by itself is not enough to cause a bit failure, it will contribute to eye closure, and with the other noise sources might result in a failure.

Voltage noise on the power rails of the chips also affects timing. The propagation delay, the time from which an input voltage transition propagates through the sequence of gates contributing to an output voltage transition, depends on the instantaneous voltage level between the In CMOS technology, the higher the drain-to-source voltage, the larger the electric fields in the channels and the shorter the propagation delay. Likewise, the lower the Vdd to Vss voltage, the longer the propagation delay.

This means that voltage noise on the Vdd to Vss rails on die directly contributes to timing variations in the output signals called jitter. A higher voltage on the Vdd rail “pulls in” a clock edge, whereas a lower rail voltage “pushes out” a clock edge. Figure 1.3 is an example of the measured jitter induced on a high-end FPGA test chip from voltage noise on the PDN.



**Figure 1.3** Measured jitter on a clock signal in the presence of Vdd to Vss voltage noise.

In this example, a clock distribution net shares the Vdd rail with a number of other gates. These gates were

switching with a pseudo-random bit sequence (PRBS), drawing large currents from the PDN and generating large transient voltage noise. This voltage noise, as applied to the clock distribution network gates, caused timing variations in the clock signal. The period jitter measurement, the period of time from one clock edge to the next clock edge, appears as the period of each clock. This measurement demonstrates the direct correlation between the voltage noise on the die and the jitter on the clock.

In this example, the sensitivity of the jitter from PDN noise is about 1 ps of jitter per mV of voltage noise. A 100 mV peak-to-peak PDN noise would contribute to 100 ps peak-to-peak jitter. In a 2 GHz clocked system, the period is only 500 psec. The jitter from the PDN noise alone would consume the entire timing budget.

**Tip**

In this example, the jitter sensitivity to PDN noise is about 1 ps/mV. This is a rough estimate of the sensitivity to expect in many devices.

## 1.2 ENGINEERING THE PDN

To meet both voltage noise and the timing budgets, the voltage noise on the PDN must be kept below some specified value. Depending on the system details, this voltage noise limit is roughly about  $\pm 5\%$  of the supply voltage. In typical CMOS-based digital systems with single-ended signals, the total noise margin for the receiver is about 15% of the signal swing. Unless there is a compelling reason not to do so, we usually partition this budget equally between the three dominate sources of noise: reflection noise, crosstalk, and PDN noise. This is the origin of the typical specification being 5% PDN noise allowed.

In some applications, such as analog-to-digital converters (ADCs) or phase locked loops (PLLs), performance is very sensitive to voltage noise and the PDN noise must be kept below 1%. The voltage noise must be kept below the limits from DC all the way up to the bandwidth of the signals, which might be as high as 5 GHz to 10 GHz.

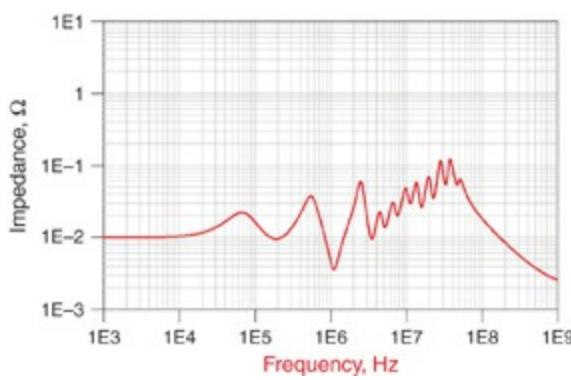
As with all signal integrity problems, the first step in eliminating them is to identify the root cause. At low frequency, the voltage noise across the PDN is usually due to the voltage noise from the VRM and so the first step in PDN design is selecting a VRM with low enough voltage noise under a suitable load current.

However, even with the world's most stable VRM, voltage noise still exists on the pads of the die. This arises from the voltage drop across the impedance of the entire PDN from transient power currents through the gates on the die. Between the pads of the VRM and the pads on the die are all the interconnects associated with the PDN. We refer to this entire network as the *PDN ecology*.

**Tip**

The PDN ecology is the entire series of interconnects from the pads on the die to the pads of the VRM. These all interact to create the impedance profile applied to the die and influence PDN noise.

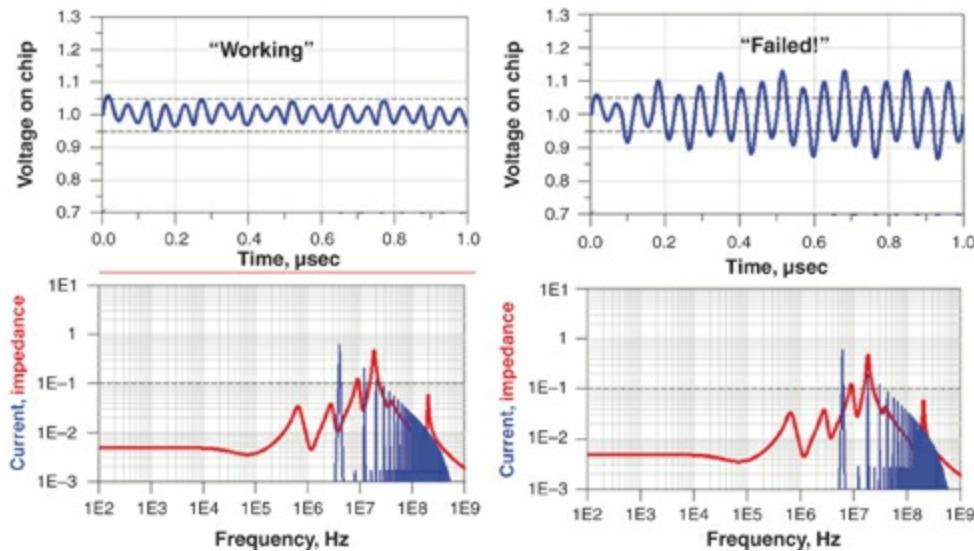
As applied to the pads of the die, these interconnects contribute to an impedance profile. Figure 1.4 shows a typical example.



**Figure 1.4** Example of an impedance profile of the entire PDN ecology, as applied to the pads of the die.

Any transient currents through this impedance profile generates voltage noise on the pads of the chip, independent of the VRM stability.

For example, **Figure 1.5** shows the transient current spectrum drawn by the core power rail for a device when executing a specific microcode. Superimposed on the current spectrum is the impedance profile through which this current flows. The combination of the current amplitude and impedance at each frequency generates a voltage noise spectrum. This noise spectrum, when viewed in the time domain, results in a transient voltage noise.



**Figure 1.5 Left Side:** PDN impedance profile and transient current spectrum result in acceptable voltage noise. **Right Side:** Slight change in current spectrum gives unacceptable voltage noise.

The left side of [Figure 1.5](#) shows the transient current spectrum, PDN impedance profile, and resulting voltage noise on the power rail. This combination of current spectral peaks and impedance peaks results in acceptable noise. On the right is the same impedance profile, but with slightly different microcode algorithm driving the same gates at a slightly different frequency. A current spectral peak ended up overlapping a larger impedance peak and generating a rail voltage noise above the acceptable limit.

The actual voltage noise generated by the transient current through the impedance profile depends on the overlap of the current frequency components and the peaks in the impedance profile. If the voltage noise is below a specified level, PDN induced errors will not occur. If the microcode changes resulting current amplitude peaks and frequency component changes, their overlap with impedance peaks might create more voltage noise and product failure.

**Tip**

The noise on the PDN depends as much on the impedance profile applied to the die as the spectrum of the transient current through the die. Microcode details and gate utilization have a strong impact on the PDN noise generated.

### 1.3 “WORKING” OR “ROBUST” PDN DESIGN

The variability in performance due to the specific microcode driving the switching of on-die gates makes testing a product for adequate PDN design difficult. A product might work just fine at boot up, or when running a specific software test suite if the combination of current spectral peaks and impedance peaks results in less than the specified transient noise. The product design may “pass” this test and be stamped as “working.”

However, if another software suite were to run that drives more gates and causes them to switch at a different dominant loop frequency, which coincidentally overlaps a peak in the PDN impedance profile, larger instantaneous voltage drops might result and the same product could fail.

Although having the product boot up, run a test suite and apparently work is encouraging, it does not guarantee “robust” operation. Products often “work” in evaluation but have field failures when driven by a broad range of customer software.

A robust PDN design means that any software code may run and generate the maximum transient current at any arbitrary frequency with any time domain signature. The resulting worst-case voltage generated by this current through the impedance profile is always less than an amount that would cause a failure.

The combination of the worst-case transient current and the voltage noise specification work together to set a limit for the maximum allowable PDN impedance such that the voltage noise will never exceed the specification.

This **maximum allowable PDN impedance** with guaranteed performance is referred to as the **target impedance** in PDN design, and we derive it with [1]

$$Z_{\text{target}} = \frac{\Delta V_{\text{noise}}}{I_{\text{max-transient}}} \quad (1.1)$$

where

$Z_{\text{target}}$  = the maximum allowable PDN impedance at any frequency

$\Delta V_{\text{noise}}$  = the maximum specified voltage rail noise to meet performance requirements

$I_{\text{max-transient}}$  = the worst-case transient current under

any possible operation

For example, if the noise spec is set as  $\pm 50$  mV and the worst-case transient current is 1 A, the target impedance is

$$Z_{\text{target}} = \frac{\Delta V_{\text{noise}}}{I_{\text{max-transient}}} = \frac{0.05\text{V}}{1\text{A}} = 50 \text{m}\Omega \quad (1.2)$$

If either  $\Delta V_{\text{noise}}$  or  $I_{\text{max-transient}}$  is a function of frequency, then  $Z_{\text{target}}$  is a function of frequency.

In principle, the combination of the entire spectral distribution of currents and the entire impedance profile is what creates the worst-case peak voltage noise. Unfortunately, this can only be determined with a transient simulation including the details of the transient current waveform and the impedance profile of the entire PDN. In practice, the target impedance is a useful approximation as a figure of merit to help focus the design of the PDN on a good starting place.

**Tip**

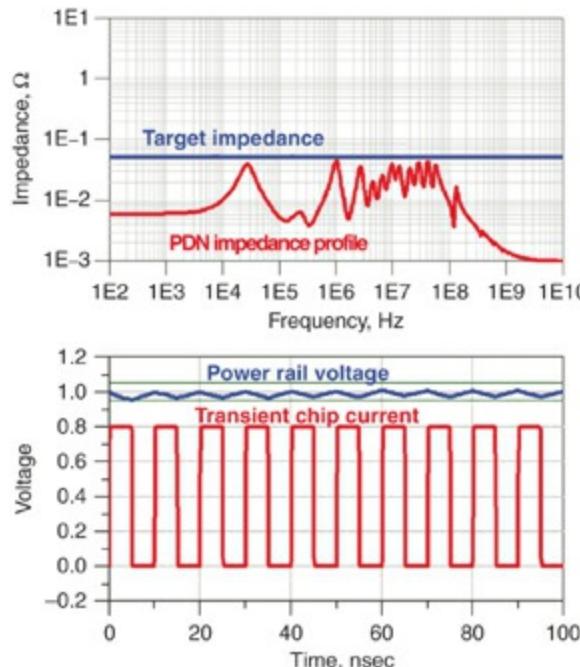
The target impedance is a useful figure of merit for the PDN. It is a good approximation of a design goal for a robust PDN design. The final evaluation of robust PDN design would come from a transient simulation of the entire PDN and the transient current waveforms.

A fully robust PDN is defined by this target impedance. If the impedance of the entire PDN ecology, as applied to the pads of the die, is below the target impedance at all frequencies, the maximum worst-case rail collapse noise generated by the transient current flowing through the PDN impedance will not exceed the noise spec except in a very rare rogue wave situation. Figure 1.6 shows an example of the impedance profile below the target impedance of  $50 \text{m}\Omega$  at all frequencies and an example of the resulting rail voltage noise with a

high current load.

**Tip**

The target impedance is the most important metric when evaluating PDN performance. The farther the PDN impedance is above the target impedance, the greater the risk of a failure.

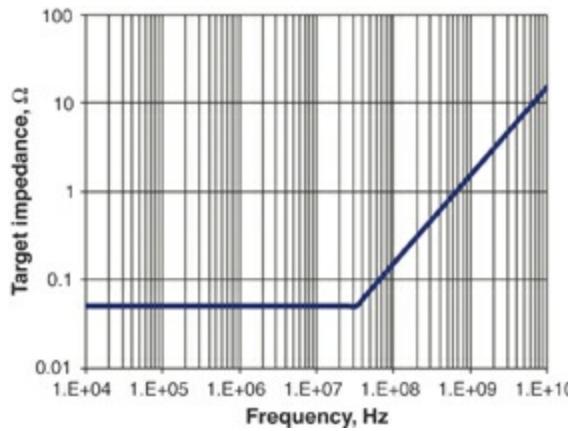


**Figure 1.6 Top:** The impedance profile of the PDN ecology engineered to be below the target impedance from DC up to a very high bandwidth. **Bottom:** The resulting Vdd rail noise under large transient current load showing the noise is always below the 5% spec limit. The square wave trace is the transient current as driven by a clock. It is plotted on a relative scale.

In practice, the maximum, worst-case transient current through the die will not be flat at all frequencies. The maximum current amplitude generally drops off at the high-frequency end, related to how quickly the maximum number of switching gates can be turned on. The precise details depend on the chip architecture, the number of bits in the pipeline, and the nature of the microcode. The effective rise time could be from the rise time of the clock edge to 100 clock cycles.

For example, if the clock frequency is 2 GHz, with a 0.5 ns clock period, and the maximum number of

switching gates requires 20 cycles to build up, the shortest rise time for the turn on of the worst-case transient current would be  $0.5 \text{ ns} \times 20 \text{ cycles} = 10 \text{ ns}$ . The amplitude of the maximum transient current frequency components will begin to roll off above about  $0.35/10 \text{ ns} = 35 \text{ MHz}$ . Above 35 MHz, the worst-case transient current spectrum would drop off at  $-20 \text{ dB/decade}$  and the resulting target impedance would increase with frequency. The target impedance, in this example, assuming a 50 mV rail voltage noise spec and worst-case current amplitude of 1 A, is shown in Figure 1.7.



**Figure 1.7** Target impedance when the transient current turns on in 20 clock cycles to a maximum of 1 A.

The consequence of this behavior is that the target impedance spec is relaxed at higher frequency. Estimating where this knee frequency begins is often difficult unless we know the details of the transient current and worst-case microcode.

This analysis points out that, in practice, accurately calculating the transient currents and the precise requirements for the target impedance of the PDN is extremely difficult. One must always apply engineering judgment in translating the information available into the requirements for a cost-effective design.

The process to engineer the PDN is to

- Establish a best guess for the target impedance based on what is known about the functioning and applications of the chips.
- Make engineering decisions to try to meet this impedance profile where possible.
- Balance the trade-offs between the cost of implementing the PDN impedance compared to the target impedance, and the risk of a field failure.

A rough measure of the risk of a failure of circuits to run at rated performance is the ratio of the actual PDN impedance to the target impedance, termed the *PDN ratio*:

$$\text{PDN ratio} = \frac{\text{Actual PDN Impedance}}{\text{Target Impedance}} \quad (1.3)$$

A ratio of less than 1 indicates low risk of a PDN-related failure. As this ratio increases, the risk increases as well. From practical experience, a ratio of 2 might still offer an acceptable risk, but a ratio of 10 will almost surely result in unacceptable risk. Even though many microcodes run at rated performance, some are likely to stimulate the PDN resonance and generate product stability issues.

Generally, achieving a lower impedance PDN, and consequently a lower risk ratio, costs more either due to more components required, tighter assembly design rules impacting yield, more layers in the board or package, increased area for die capacitance, or the use of more expensive materials. The balance between cost and risk is often a question of how much risk you are comfortable with. By paying more for added design margin, you can always “buy insurance” and reduce the risk. This is the fundamental trade-off in PDN design.

**Tip**

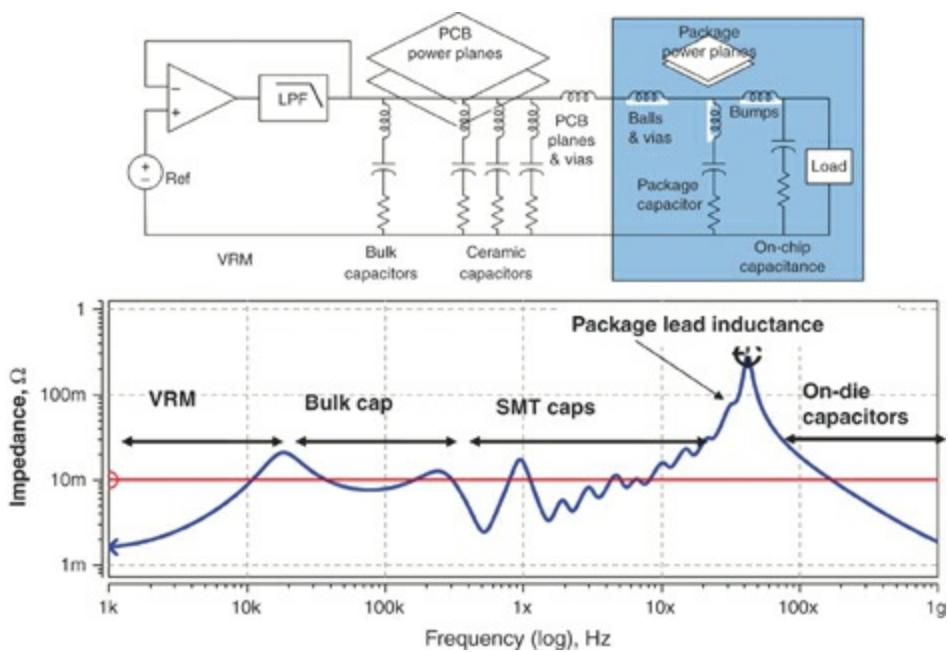
An important metric of risk in PDN design is the PDN ratio, which is the ratio of the peak impedance to the target impedance. A PDN ratio of 2 or lower is a low risk whereas a PDN ratio of 10 or more is a high risk.

In consumer applications, often strongly cost driven, engineering for a higher risk ratio with a lower cost design might be a better balance. However, in avionic systems, for example, paying extra for a risk ratio less than 1 might be the cost-effective solution. Different applications have a different balance between cost and risk ratio.

## **1.4 SCULPTING THE PDN IMPEDANCE PROFILE**

The goal in PDN design is to engineer an acceptable impedance profile from DC to the highest frequency component of any power rail currents. All the elements of the PDN should be engineered together to sculpt the impedance profile of the entire ecology. Although many elements interact, assigning some features of the PDN impedance profile to specific features in the PDN design is possible.

Figure 1.8 shows a simplified schematic of the entire PDN ecology. This includes the on-die capacitance, the possibility of on-package capacitors, the package lead inductance, the circuit board vias, the power and ground planes in the circuit board, decoupling capacitor, bulk capacitors, and VRM.



**Figure 1.8 Top:** Simplified schematic of the PDN

ecology showing the major elements. **Bottom:**

Resulting impedance profile identifying how specific design features contribute to specific impedance features.

On the horizontal scale “x” is MHz.

Isolating functions of some PDN elements enables us to optimize parts of the PDN independent of the others, as long as we always pay attention to the interfaces where the impedance of one element interacts with the impedance of another. This is why so much of PDN design is about the interfaces between the parts.

In the journey ahead, we explore each of these elements that make up the PDN and how they interact to result in a robust and cost-effective PDN design. Ultimately, the power integrity engineer is responsible for finding an acceptable balance between cost, risk, performance, and schedule. The more we know about the details of the specific PDN elements, the more quickly we can reach an acceptable solution.

## 1.5 THE BOTTOM LINE

1. The PDN consists of all the interconnects from the pads on the die to the VRM and all of the components in between.

2. The purpose of the PDN is to provide a clean, low-noise voltage and ground supply to the devices and a low impedance return path for signals, and to mitigate EMC problems.
3. The typical noise spec on the PDN of 5% tolerance is based on an allocation of 1/3 the noise budget to each of the main sources of noise: reflection noise, cross talk, and PDN.
4. Voltage noise on the PDN is a result of transient power currents passing through the impedance of the PDN. The amount of noise is due to the combination of the impedance profile and the transient current spectrum.
5. Noise on the PDN can contribute to jitter. A typical value of the sensitivity is 1 psec/mV of noise. This number varies depending on the chip design and device technology node.
6. The impedance profile, as applied to the chip pads, is the most important metric for the quality and performance of the PDN. This is from DC to the highest frequency components of the switching signals.
7. The target impedance is a measure of the maximum impedance, which will keep the worst-case voltage noise below the acceptable spec.
8. The PDN ratio is the ratio of the actual PDN peak impedance to the target impedance. It is a good metric of risk. A PDN ratio greater than 10 is a high-risk design.
9. Sculpting the impedance profile requires optimizing both the individual elements of the PDN and their interactions. The entire PDN ecology must be optimized to reduce the peak values.

10. If you care about PDN design, this book is for you.

## REFERENCES

- [1] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 284–291, 1999.

# **Chapter 2. Essential Principles of Impedance for PDN Design**

## **2.1 WHY DO WE CARE ABOUT IMPEDANCE?**

Ultimately, a PDN is acceptable if it provides a voltage to the chips that is within the specified range: an average value with some AC ripple. Unfortunately, whether this voltage stays at an acceptable level is based on not only the PDN design but also on the behavior of the various chips in the system: what functions they perform and the frequency spectrum of current they draw.

The voltage measured at a location on the circuit board might be acceptable while running a particular section of code. However, no guarantee exists that running other microcode will produce acceptable results. Voltage measured on the pads of a chip often has more noise than is found on the board.

This makes testing for an acceptable power distribution network design difficult. However, to a first approximation, the voltage noise is created by the spectrum of current drawn by the various chips flowing through the impedance of the power distribution network of interconnects.

If we know the worst-case current draw by the chips, based on gate utilization or simulation, for example, and know the impedance of the power distribution by measurement, simulation, or calculation, then we can calculate the expected noise under worst-case but realistic conditions.

Even if we cannot create every current waveform expected to be drawn by an end user in a test environment, evaluating the acceptability of a PDN design based on its impedance behavior may be

possible. Impedance can become a surrogate measure of the acceptability of a PDN design.

**Tip**

If you don't know the specific spectrum of the power supply current from the die, you might use the impedance profile of the PDN as a surrogate measure of the acceptability of the PDN design.

If impedance is the measure of the quality of a robust PDN, then PDN design can be reduced to designing against a target impedance value. This makes impedance the most important design metric for PDN performance. Understanding the details of impedance and how component selection and physical design affects impedance becomes the important aspect of PDN design. We start this process with a discussion about impedance and the impedance properties of capacitors.

Impedance is a fundamental electrical quantity in electrical design in general and is the most important and essential principle in PDN design.

## 2.2 IMPEDANCE IN THE FREQUENCY DOMAIN

Impedance always refers to the ratio of the voltage to the current through any device:

$$Z = \frac{V}{I} \quad (2.1)$$

$$Z_{11} = V_{11}/I_{11}$$

where

Z = the impedance between two terminals of the device

V = the voltage between the terminals of the device

I = the current going into one terminal and out into the other through the device

This basic fundamental definition applies in both the time and frequency domains and can be extended to

include multi-terminal elements; for example, voltage across two planes at different locations [1]. This is the basis of transfer impedance described at the end of this chapter.

Although impedance is well defined in both the time and frequency domains, the impedance definition for an ideal circuit element, such as a capacitor or inductor, has a much simpler description in the frequency domain.

**Tip**

Impedance is equally well defined in the time and frequency domains. It is simpler and easier to use in the frequency domain, which is why this domain is so often used to display and analyze the impedance of the PDN.

For example, in the time domain, the current through an ideal capacitor is

$$I = C \frac{dV}{dt} \quad (2.2)$$

where

$I$  = current through the capacitor

$C$  = the capacitance of the capacitor

$V$  = the voltage across the capacitor

Using the definition of the impedance, the impedance of a capacitor in the time domain is

$$Z = \frac{V}{C \frac{dV}{dt}} \quad (2.3)$$

This is consistent with what we expect: the larger the  $dV/dt$ , the larger the current through the capacitor and the lower its impedance. The impedance of an ideal capacitor depends on the slope of the voltage waveform

across the capacitor. Although this expression is absolutely correct, using it in any real application is awkward because the impedance depends in a complicated way on the actual shape of the voltage waveform across the capacitor.

When we switch to the frequency domain, where the only waveforms allowed are sine waves, the impedance of the capacitor takes a simpler form:

$$Z = \frac{-j}{\omega C} \quad (2.4)$$

where

$Z$  = the impedance of the ideal capacitor

$C$  = the capacitance of the ideal capacitor

$j$  = the square root of  $-1$

$\omega$  = the angular frequency =  $2 \times \pi \times f$

Likewise, the impedance of an ideal inductor has a simpler form in the frequency domain compared to the time domain:

$$Z = j\omega L \quad (2.5)$$

where

$Z$  = the impedance of the ideal inductor

$L$  = the inductance of the ideal inductor

$j$  = the square root of  $-1$

$\omega$  = the angular frequency =  $2 \times \pi \times f$

Because impedance has a simpler form in the frequency domain, for many problems, we can get the answer more quickly by working in the frequency domain. This motivates us to leave the time domain and work in the frequency domain. Analyzing problems related to impedance in the frequency domain is a common practice.

**Tip**

Although performance is often evaluated in the time domain, we can sometimes get to an answer faster by taking a shortcut through the frequency domain. This is the most important reason to consider frequency domain analysis.

The “j” term in the impedance means the impedance is complex—it has two values at any frequency. These are represented as a magnitude and a phase or as a real and imaginary part. In many cases, the magnitude and phase are the most common representation for the complex impedance.

When impedance is described in the frequency domain as a real and imaginary component, the imaginary component is referred to as the reactance. In circuits constructed with combinations of resistance (R), inductance (L), and capacitance (C) elements, the reactance is dominated by the L and C values. For example, when an R and C element are combined in series, the impedance is

$$Z = R + \frac{-j}{\omega C} \quad (2.6)$$

The reactance is the imaginary term, which by convention, is represented by the letter X:

$$X_C = \frac{-1}{\omega C} \quad (2.7)$$

In the case of a single ideal C element, the reactance drops off inversely with frequency. This is a drop of a factor of 10 in magnitude with a factor of 10 increase in frequency. Because a factor of 10 in magnitude of impedance is -20 dB, we refer to the drop in reactance over frequency as a -20 dB drop per decade of frequency. This is typical of a circuit with a single capacitor element.

Likewise, the reactance of a single inductor is

$$X_L = \omega L \quad (2.8)$$

This is an increase in reactance of 20 dB per decade of frequency.

**Tip**

In the frequency domain, the impedance of a capacitor or inductor changes at the rate of 20 dB per decade of frequency. On a log-log scale, this is a straight line with slope of +1 for an inductor and -1 for a capacitor. This is why we often plot log impedance vertically with log frequency on the horizontal axis.

## 2.3 CALCULATING OR SIMULATING IMPEDANCE

Although we can calculate impedance in the frequency domain with pencil and paper for a single element, it gets exponentially more tedious with each additional element in the circuit.

Luckily, we can calculate the impedance of any collection of ideal, linear, time-invariant circuit elements using SPICE or a SPICE-like simulator. These simulators are generally easy to use, free, and run on all the popular operating systems. They also have graphical inputs and displays, making them universally valuable.

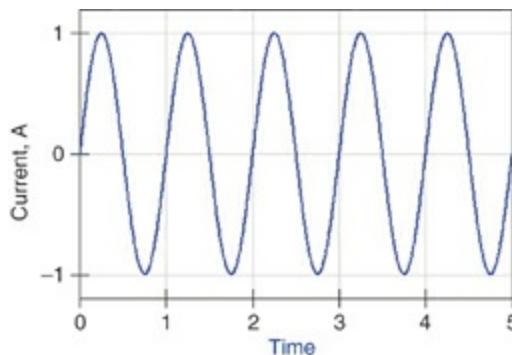
In particular, QUCS (Quite Universal Circuit Simulator) [2] is a free, open source, powerful, and simple-to-use circuit simulator that you can use as an impedance calculator or analyzer. Some of the examples created in this book use QUCS. Other examples use one of the highest end circuit simulation tools, Advanced System Design (ADS) [3], available from Keysight Technologies, formerly Agilent Technologies. The results are identical.

### Tip

An essential tool to simulate impedance is a SPICE-compatible circuit simulator. The easiest to use free version is QUCS, whereas the highest end version is probably Keysight's ADS. These tools can be used to simulate the impedance profiles of any circuit combinations.

The secret to building an impedance analyzer for any circuit in SPICE is a constant current AC source. In SPICE, a constant current source is an ideal source that will *always* output a constant current, no matter what load is attached. It keeps the current constant by outputting whatever voltage is necessary to drive that fixed current.

In the AC mode, the constant current source outputs a sine wave of current with an amplitude that is always constant, independent of the load. Figure 2.1 shows this current waveform.



**Figure 2.1** Sine wave of constant current amplitude.

To output this constant amplitude of AC *current*, the sine wave *voltage* amplitude output from the source must be a specific value. In the frequency domain, all waveforms are sine waves. The frequency, amplitude, and phase properties of any sine wave completely describe everything about it.

The sine wave output voltage of the AC constant current source is always related to the sine wave current through it by

$$V(\omega) = Z(\omega) \times I(\omega) \quad (2.9)$$

where

$V(\omega)$  = the amplitude and phase of the sine wave voltage at each frequency

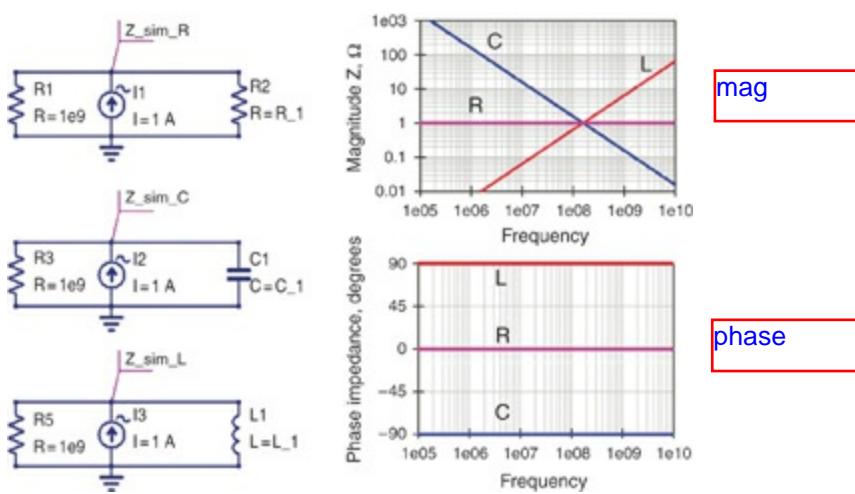
$I(\omega)$  = the amplitude and phase of the sine wave current at each frequency

$Z(\omega)$  = the magnitude and phase of the impedance of the load at each frequency

All of these quantities are complex. The simulated complex voltage, based on this load attached to this current source, is numerically the complex impedance of the load. The amplitude of the simulated voltage is the magnitude of the impedance, and the phase of the simulated voltage is the phase of the impedance of the load.

This simple relationship says that if we use a 1-amp amplitude constant current sine wave source with a zero-degree phase, the output voltage amplitude in volts is numerically the impedance in Ohms. Just as important, the phase of the simulated voltage is numerically the phase of the impedance.

By simulating the output voltage amplitude and phase from the constant current source, we can simulate the complex impedance of the load attached to the constant current source at any frequency. Figure 2.2 illustrates the circuit for a simple impedance analyzer and the resulting impedance plots for a few ideal elements.



**Figure 2.2** Circuit model to simulate an impedance analyzer in QUCS and examples of the simulated impedance of three common ideal circuit elements.

In the impedance analyzer circuit, the 1-G $\Omega$  resistor on the left side of the constant current source is present to keep the simulator from blowing up. Many simulators require a DC path to ground to each node. This resistor provides a DC path to the output of the constant current source even when the output is open or has a capacitive load. It limits the highest impedance we can simulate to 1 G $\Omega$ , perfectly adequate for all PDN applications.

Note the patterns of the magnitude of the impedance for an ideal capacitor and ideal inductor on a log-log scale. The impedance drops as frequency increases for an ideal capacitor and increases with frequency for an ideal inductor. This change in the magnitude of impedance is 20 dB per decade of frequency.

When plotting impedance against frequency, a log-log scale is always the most useful format because it immediately shows when a circuit behaves “capacitive” and when it behaves “inductive.”

The impedance of an ideal capacitor *decreases* with frequency, whereas the phase of the impedance of an ideal capacitor remains constant at –90 degrees. The impedance of an ideal inductor *increases* with

frequency, whereas the phase of the impedance of an ideal inductor remains constant at +90 degrees. Of course, the magnitude of the impedance of an ideal resistor is constant, and the phase of its impedance is constant at 0 degrees.

The phase of the impedance is closely connected to the shape of the impedance profile. The underlying root cause of this is based on the Kramers-Kronig relationship. Essentially, this concept says that for any complex function in the frequency domain to describe a real-world effect in the time domain and not violate causality—that is, for the response to *always* occur after the stimulus—a specific connection must exist between the real and imaginary parts of the complex function.

Kramers-Kronig says, to know the real part of the impedance is to know the imaginary part. The real and imaginary parts are constrained by this relationship when describing the impedance of a physical structure. The impact of this relationship is that the shape of the magnitude of the impedance curve is related to the phase of the impedance. To know the shape of the impedance curve is to know the phase. Look for this behavior in impedance and phase plots.

In all circuits, when the magnitude of the impedance drops by -20 dB per decade, such as with a capacitor, the phase will be close to -90 degrees. When the magnitude of the impedance increases by 20 dB per decade, the phase will be close to +90 degree. When the impedance curve is flat with frequency, the phase will be close to 0 degrees. This means that if we pay careful attention to the shape of the impedance curve when it's plotted on a log-log scale, we can infer what the phase is doing as well.

**Tip**

To know the magnitude of the impedance is to know the phase of the impedance. When the magnitude drops with frequency, the phase will be near  $-90^\circ$  degrees. When the magnitude of the impedance increases with frequency, the phase will be near  $+90^\circ$  degrees. This is fundamental to the nature of real, causal physical systems.

Because we can infer its shape, we will not always show the phase of the impedance, but focus on the magnitude of the impedance, usually plotted on a log-log scale.

Never confuse the values of the capacitance and inductance of ideal capacitor and inductor elements with their impedance. For ideal circuit elements, the value of the capacitance of an ideal capacitor is *always constant* with changing frequency, by definition. Likewise, the value of the inductance of an ideal inductor is *always constant* with frequency, by definition, as is the value of the resistance of an ideal resistor. The impedance of the L and C elements may vary with frequency, but their capacitance and inductance values are constant.

**Tip**

Never forget—the capacitance of an ideal capacitor is constant with frequency, but its impedance varies with frequency. Likewise for an inductor.

We can automatically calculate all of these features by using any simple circuit simulator. All versions of SPICE are able to simulate the impedance of any circuit with this approach.

## 2.4 REAL CIRCUIT COMPONENTS VS. IDEAL CIRCUIT ELEMENTS

We can simulate the impedance of any circuit constructed from combinations of ideal circuit elements

with the QUCS impedance analyzer circuit.

Being aware of the distinction between *ideal* circuit elements and *real* circuit components [4] is important. Ideal circuit elements have well-defined properties and are used in circuit simulations. Real circuit components are real physical structures that have measurable impedances including parasitic effects. It is unfortunate that we use the same term, *capacitor*, for an ideal circuit element and for a real physical structure, even though their behaviors and properties can be very different.

Although we may call a structure a real capacitor, its measured impedance will not even be close to the behavior of an ideal capacitor in some frequency bands.

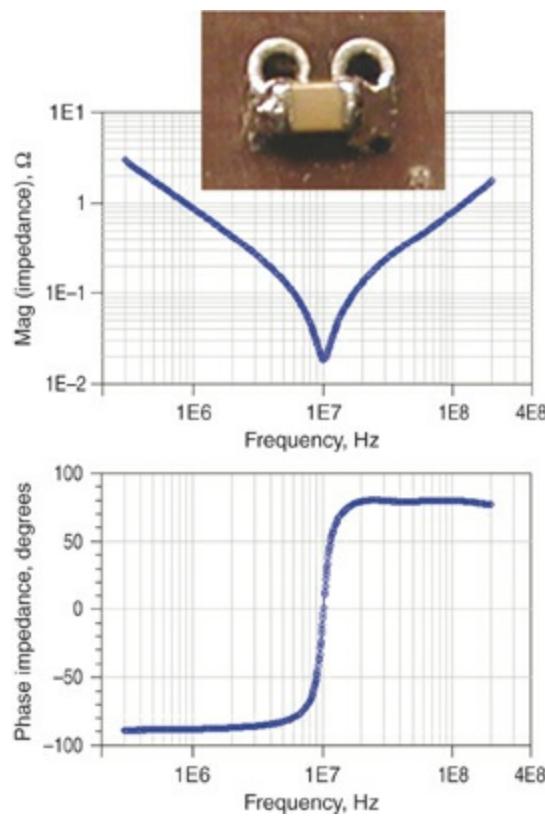
**Tip**

A real circuit component is going to behave somewhat like an ideal component with the addition of parasitic effects, based on its physical design, material properties, and Maxwell's Equations. An ideal circuit element is an ideal representation of a non-ideal physical device.

In special situations, incorporating the measured impedance of a real component in a circuit simulation might be possible using some form of a behavioral model, such as a description in terms of S-parameters. It takes a special simulator tool to allow an S-parameter behavioral model to be incorporated in a circuit simulation with traditional RLC and T elements. And even then, using behavioral models is a little dangerous if you are not completely aware of the specific details of the measurement setup or how the S-parameters were created.

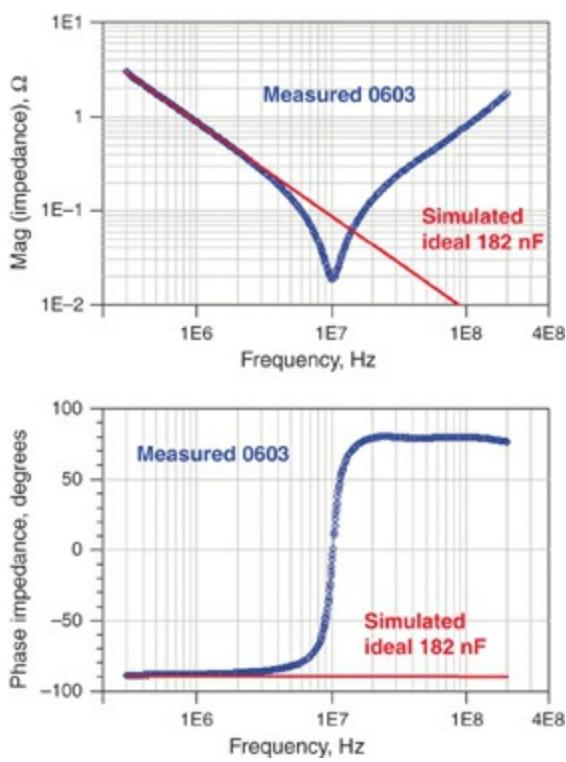
We can measure the impedance of a real capacitor with a network analyzer using two-port techniques, discussed in [Chapter 3](#), “Measuring Low Impedance.” [Figure 2.3](#) shows the measured impedance of an 0603

multilayer ceramic chip (MLCC) capacitor.



**Figure 2.3** Measured impedance profile of an o603 MLCC capacitor attached to a four-layer test board, measured with a two-port VNA. Inset picture of a typical o603 capacitor. Sample courtesy of X2Y attenuators.

At low frequency, the impedance of this real capacitor matches that of a 182 nF ideal capacitor. Figure 2.4 compares the measured impedance of the real capacitor and the simulated impedance of an ideal capacitor. The agreement is excellent up to about 3 MHz, in this example.



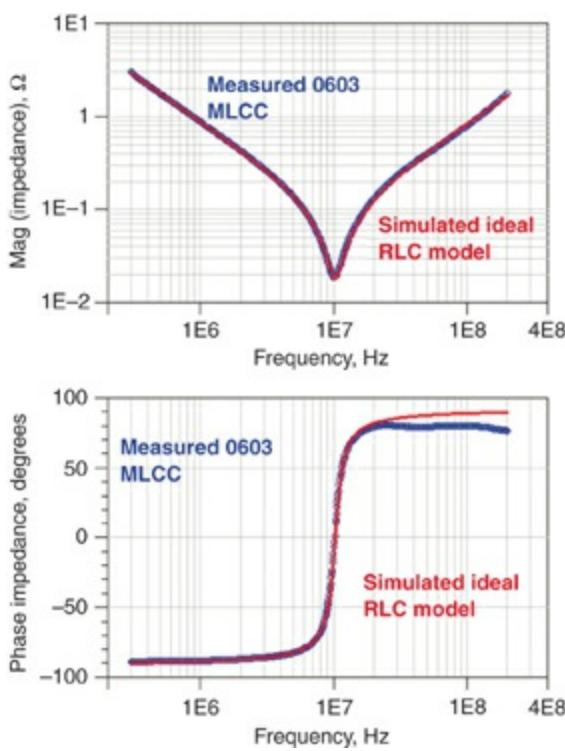
**Figure 2.4** Measured impedance of a real MLCC capacitor and the simulated impedance of an ideal 182 nF capacitor.

However, a higher bandwidth model that describes this real capacitor's impedance behavior is a series RLC circuit. Figure 2.5 shows the agreement in the magnitude and phase of the measured impedance of this real capacitor and the simulated impedance of an ideal RLC series circuit. The values used in this simulated circuit were

$$R = 18 \text{ m}\Omega$$

$$C = 182 \text{ nF}$$

$$L = 1.3 \text{ nH}$$



**Figure 2.5** Comparing the measured impedance of a 0603 MLCC capacitor and an ideal series RLC circuit.

Note that although the impedance changes with frequency, the values of the R, L, and C ideal elements are constant with frequency. This example illustrates that we can approximate well the measured impedance of real structures by the simulated impedance of combinations of ideal circuit elements. From insight and experience, we can combine several ideal elements in a proper topology and choose parameter values to closely approximate the non-ideal parasitic effects of real physical components. In this example, the agreement of this simple model and the actual measured performance is as high as the bandwidth of the measurement, 200 MHz. The bandwidth of the model might be higher than 200 MHz; we just can't tell from this measurement.

#### Tip

It is remarkable that the measured impedance of real, sometimes complicated structures can be accurately approximated by relatively simple combinations of ideal circuit elements to very high bandwidth.

Often times, the only way of knowing how good the model is, or how high a bandwidth it matches the measured performance, is through measurement. This is why the next chapter focuses on measurement techniques.

Most structures associated with the PDN can be described by two simple RLC circuits and their combinations: a series combination of R, L, and C elements, and a parallel combination of R, L, and C elements.

The terms *series* and *parallel* refer to how the L and C elements are connected together as viewed from the measurement or simulation source. The R element can be connected either in series or in parallel with one of the reactive elements.

Understanding the properties of these circuits will make understanding the performance of the PDN much easier.

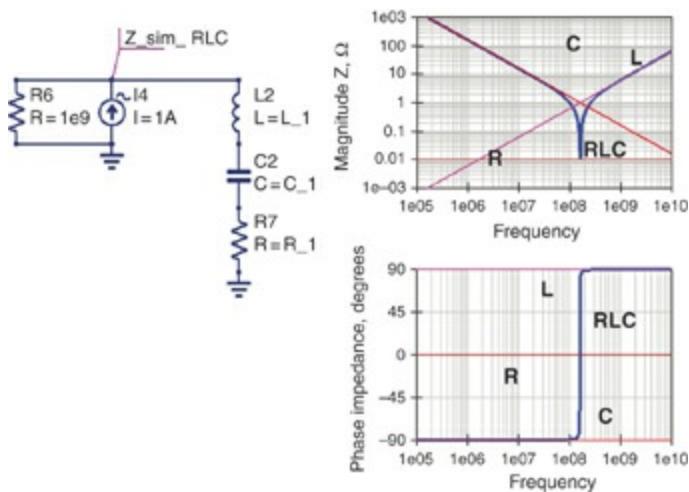
## 2.5 THE SERIES RLC CIRCUIT

The example shown in [Figure 2.5](#) also illustrates why the series RLC circuit is so important: It is an excellent model for the behavior of real capacitors. We calculate impedance of a series RLC circuit with a little algebra by adding up the impedance of each element [5]. We represent this series impedance with

$$Z_{RLC} = R + j \left( \omega L - \frac{1}{\omega C} \right) \quad (2.10)$$

We can also simulate this impedance using the impedance analyzer circuit in SPICE. The simulated impedance of a combination of ideal R, L, and C elements is shown in [Figure 2.6](#), which compares the simulated impedance of the series RLC circuit with the impedances of the individual RLC elements in

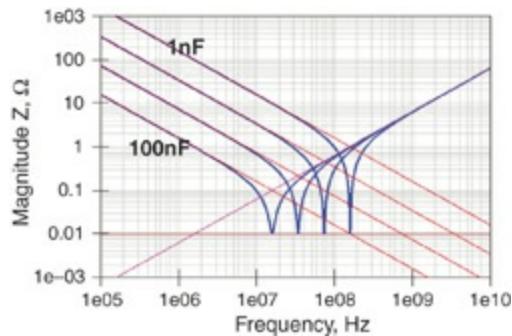
magnitude and phase.



**Figure 2.6** Simulated impedance profile of the series RLC circuit. The circuit element values are  $R = 0.01 \Omega$ ,  $L = 1 \text{ nH}$ , and  $C = 1 \text{ nF}$ .

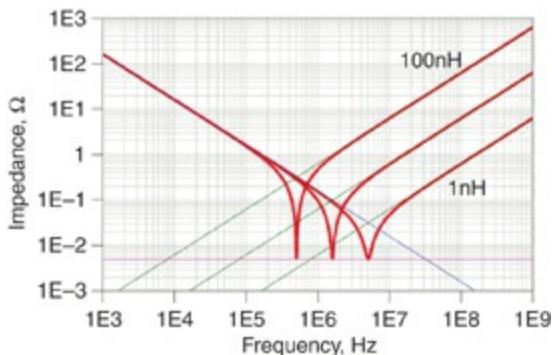
Three important features exist in the impedance profile of the series RLC model including frequency bands where the device behaves as capacitance, resistance, and inductance.

At the lowest frequency, the impedance of the RLC circuit is dominated by the impedance of the ideal capacitor. Even the phase of the impedance of the RLC circuit is  $-90$  degrees, the same as the ideal capacitor, consistent with the Kramers-Kronig relationship. The capacitance will only affect the low-frequency impedance, as illustrated in [Figure 2.7](#). As the capacitance change, the impedance of the series RLC circuit is only affected at the lower frequency end.



**Figure 2.7** Impedance profile of the RLC circuit as the capacitance is changed from 1 nF to 100 nF in four steps. Only the impedance at low frequency is affected.  $L = 1 \text{ nH}$ .

At the higher frequency end, the impedance of the series RLC circuit is dominated by the impedance of the ideal inductor, and the phase of the RLC circuit is +90 degrees, the same as an ideal inductor. The only way of changing the impedance of the RLC circuit at the high-frequency end is by changing the inductance (see [Figure 2.8](#)).



**Figure 2.8** Impedance profile of RLC circuit as the value of  $L$  is changed from 1 nH to 100 nH in three steps. As the  $L$  changes, only the impedance on the high-frequency side is affected.  $C=1 \mu\text{F}$ .

At the frequency where the inductive and capacitive reactances cross, their series combination of impedance goes to zero and the impedance of the series RLC circuit is dominated by the impedance of the ideal resistor element. We can calculate the angular frequency at which the magnitude of the capacitive and inductive reactances cross and are equal from

$w^2L$  and  $1/(w^2C)$  cancels out  
 $Z_{\{RLC\}} = R$

$$|X_C| = |X_L| = \frac{1}{\omega C} = \omega L \quad (2.11)$$

and

$$\omega = \sqrt{\frac{1}{LC}} \quad (2.12)$$

The frequency at which the minimum impedance occurs is called the self or **series resonance frequency (SRF)**, which we derive with

$$SRF = \frac{\omega}{2\pi} = \frac{1}{2\pi} \frac{1}{\sqrt{LC}} \quad (2.13)$$

where

$SRF$  = the self or series resonant frequency in Hz

$\omega$  = the angular frequency in radians/sec

$L$  = the inductance in H

$C$  = the capacitance in F

In a more convenient set of units, the SRF is

$$SRF = \frac{159}{\sqrt{LC}} \text{ MHz} \quad (2.14)$$

where

$SRF$  = the self-resonant frequency in MHz

$L$  = the inductance in nH

$C$  = the capacitance in nF

For example, in the earlier RLC circuit,  $L = 1 \text{ nH}$ ,  $C = 1 \text{ nF}$ , and the SRF is calculated as  $SRF = 159 \text{ MHz}$ . This is exactly the frequency of the minimum impedance.

At this resonant frequency, we get the capacitive and inductive reactances alone with

$$|X_C| = |X_L| = \frac{1}{\omega C} = \omega L = \sqrt{\frac{1}{LC}} \times L = \sqrt{\frac{L}{C}} = Z_0 \quad (2.15)$$

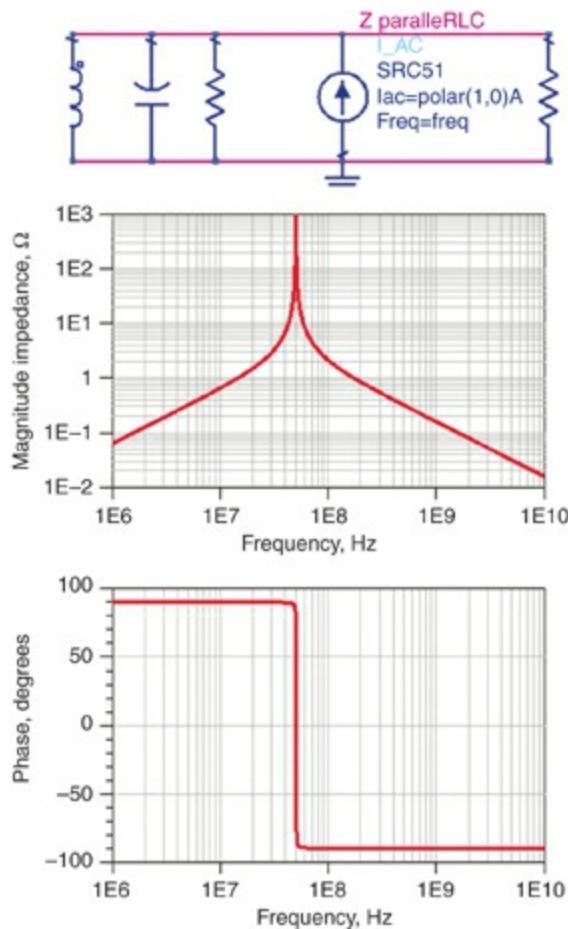
This impedance is often referred to as the **characteristic impedance** of the RLC circuit. It is in no way the same as the characteristic impedance of a transmission line, but is an impedance “characteristic” of the RLC circuit and is equivalent to the impedance of the L and C elements at the resonant frequency.

**Tip**

In a series RLC circuit, the low-frequency impedance is determined only by the capacitor whereas the high-frequency impedance is determined only by the inductor.

## 2.6 THE PARALLEL RLC CIRCUIT

An equally useful ideal circuit model is the parallel RLC circuit. In this case, the three ideal circuit elements are connected in parallel, as shown in Figure 2.9.



**Figure 2.9** Parallel RLC circuit and the impedance behavior with  $R = 1\text{k }\Omega$ ,  $L = 10\text{ nH}$ , and  $C = 1\text{ nF}$ .

At low frequency, the impedance is dominated by the

parallel inductor. It acts as a short at DC with increasing impedance at higher frequency. At high frequency, the impedance is dominated by the impedance of the capacitor, which decreases at higher frequency. The peak impedance occurs when the parallel impedance of the L and C is a maximum and the circuit's impedance is limited by the impedance of the resistor element.

The peak in impedance is referred to as a parallel resonant peak. When the inductive and capacitive reactances are equal, their parallel impedance is a maximum. If the parallel resistor were not there, the parallel resonant peak impedance of just the C and L elements would be infinite. The resistor acts to damp out this parallel resonant peak. Just as in the case of the series resonant frequency, the parallel resonant frequency (PRF) is the frequency at which the inductor's reactance matches the capacitor's reactance:

$$\boxed{\text{PRF} = \frac{1}{2\pi} \frac{1}{\sqrt{LC}}} \quad (2.16)$$

where

PRF = the parallel resonant frequency in Hz

L = the inductance in H

C = the capacitance in F

In a more convenient set of units, the PRF is

$$\text{PRF} = \frac{159}{\sqrt{LC}} \text{ MHz} \quad (2.17)$$

where

PRF = the parallel resonant frequency in MHz

L = the inductance in nH

C = the capacitance in nF

For example, in the earlier parallel RLC circuit, L = 10

nH, C = 1 nF, and the PRF is calculated as PRF = 50.3 MHz. This is exactly the frequency of the peak impedance.

**Tip**

Peaks in an impedance profile are almost always created by parallel RLC circuits. You can leverage your understanding of the features that influence the peak impedance to engineer lower peaks.

## 2.7 THE RESONANT PROPERTIES OF A SERIES AND PARALLEL RLC CIRCUIT

In a series or parallel RLC circuit, three features describe the impedance properties:

- The resonant frequency
- The min or max impedance at the resonance
- The broadness of the dip or peak

The dip or peak in impedance occurs at the series resonant or parallel resonant frequency, related to the L and C values and calculated with

$$\text{SRF} = \text{PRF} = \frac{159}{\sqrt{LC}} \text{ MHz} \quad (2.18)$$

where

L = the inductance in nH

C = the capacitance in nF

The value of the inductive or capacitive reactance at the SRF or PRF is the characteristic impedance of the circuit,  $Z_0$ , calculated with

$$Z_0 = |X_C| = |X_L| = \frac{1}{\omega C} = \omega L \quad \text{at the SRF or PRF} \quad (2.19)$$

where

$Z_0$  = the characteristic impedance of the RLC circuit,

not to be confused with the characteristic impedance of a transmission line.

The characteristic impedance of the RLC circuit is in no way related to the concept of the characteristic impedance of a uniform transmission line. It is just an impedance “characteristic” of the RLC circuit.

Solving for omega:

$$\omega^2 = \frac{1}{LC} \Rightarrow \omega = \frac{1}{\sqrt{LC}} \quad (2.20)$$

$$\frac{1}{\omega C} = \frac{1}{\sqrt{\frac{1}{LC} C}} = \sqrt{\frac{L}{C}} = Z_0 \quad (2.21)$$

and,

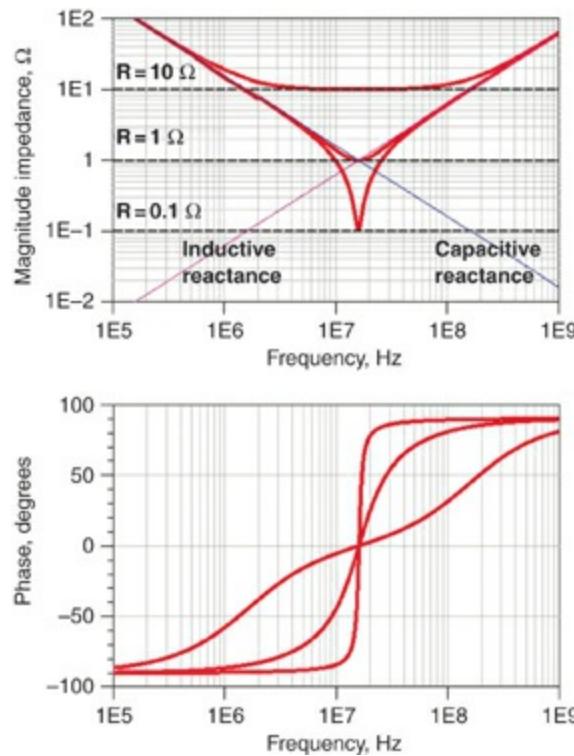
$$\omega L = \sqrt{\frac{1}{LC}} \times L = \sqrt{\frac{L}{C}} = Z_0 \quad (2.22)$$

The **resistive element** strongly influences the impedance of the parallel or series circuit at the resonant frequency. In the absence of damping, the peak value or the minimum value approaches infinity or zero. Q factor  
The damping provided by the resistance of the resistor element brings these peaks away from the extremes.

In a series RLC circuit, the minimum value of the impedance is literally the resistance. At the SRF, the capacitive and inductive reactances cancel out and the resulting series impedance is just the R value. In a parallel RLC circuit, the maximum value of the impedance is the parallel resistance. At the PRF, the capacitive and inductive reactances cancel out and the resulting parallel impedance is, once again, just the R value.

At frequencies away from the SRF, the impedance profile is only dependent on the C value at low

frequency or the L value at high frequency. The impedance behavior around the resonant frequency also changes slightly due to the resistance. As the minimum impedance value rises with larger R, the dip at the SRF becomes shallower. It looks like the dip is broadening out. Figure 2.10 shows an example of the impedance profile for three different resistance values.



**Figure 2.10** Impedance profile of a series RLC circuit with three different values of  $R_{\text{series}}$  with  $L = 10 \text{ nH}$  and  $C = 10 \text{ nF}$ .

As the series resistance increases, the depth of the dip decreases but the impedance on the outer extremes is mostly unaffected. This example also illustrates the relationship between the shape of the impedance profile and the phase, as a consequence of the Kramers-Kronig relationship. The larger the frequency span over which the impedance is flat and nearly constant, similar to the behavior of an ideal resistor, the closer the phase is to 0 degrees, the phase of the impedance of an ideal resistor.

The shape of the impedance curve depends very much on not just the value of  $R_{\text{series}}$  but also on the L and C

values. A metric that describes the relative amount of resistance and its influence in the RLC resonant circuit is the q-factor or “quality” of the circuit. Sometimes the quality of a resonance circuit is identified with the letter  $Q$ . In this book, we prefer to use q-factor, so as not to confuse the q-factor with the charge stored in a capacitor, for example, for which we reserve the letter  $Q$ .

In resonant circuits, the **q-factor** is defined as

$$\text{q-factor} = 2\pi \times \frac{\text{Peak energy stored in each cycle}}{\text{Total energy dissipated per cycle}} \quad (2.23)$$

It is also the ratio of the characteristic impedance of the circuit to the damping resistance and the ratio of the resonant frequency to the frequency span of the full-width of the dip at half its minimum or maximum value. In an RLC series circuit, the q-factor is

$$\text{q-factor} = \frac{1}{R_{\text{series}}} \sqrt{\frac{L}{C}} = \frac{Z_0}{R_{\text{series}}} \quad (2.24)$$

For example, in the preceding circuit, with  $L = 10 \text{ nH}$  and  $C = 10 \text{ nF}$ , the q-factor is

$$\text{q-factor} = \frac{1}{R_{\text{series}}} \sqrt{\frac{10 \text{ nH}}{10 \text{ nF}}} = \frac{1 \Omega}{R_{\text{series}} [\Omega]} \quad (2.25)$$

When  $R_{\text{series}} = 1 \Omega$ , the q-factor is 1. In Figure 2.10, the three different values of resistance used in the simulation corresponded to values of the q-factor of 10, 1, and 0.1.

The q-factor is a relative measure of the damping in the system. In a high q-factor system, only a small fraction of the energy stored at the peak frequency is lost each cycle. The system continues ringing in the time domain for a long time, and the impedance curve shows a sharp and narrow dip. In a low q-factor system, a large fraction of the energy stored is dissipated each cycle, the

system quickly stops ringing, and the dip in the impedance curve is broad. Note that in this context we discuss the series RLC circuit, which has an impedance dip with a q-factor. In this case, the time domain ringing is for current. The q-factor concept applies equally well for parallel RLC circuits that have an impedance peak. In this case, the time domain ringing applies to voltage.

As a rough measure of the ringing, a q-factor of 1/2 is critically damped and has a perfect balance between the fastest settling time with no ringing. Higher q-factor values show more ringing, and lower q-factor values have a sluggish response.

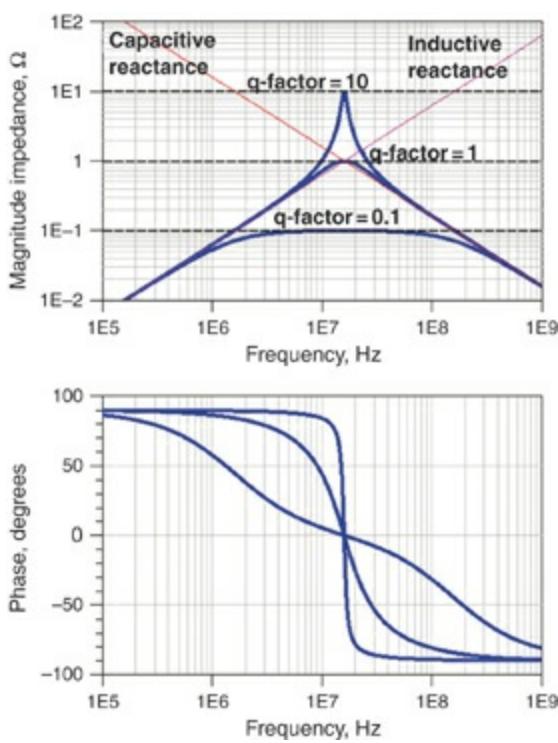
The characteristic impedance of the series RLC circuit is where the capacitive and inductive reactances cross, and practically, it's a useful parameter for an RLC circuit because it immediately shouts out the value of  $R_{\text{series}}$  that provides a q-factor value on the order of 1.

We can also see that the minimum impedance of the dip in a series RLC circuit, the resistance  $R_{\text{series}}$ , is related to the q-factor by

$$Z_{\min} = R_{\text{series}} = \frac{1}{\text{q-factor}} Z_0 \quad (2.26)$$

The q-factor of a series RLC circuit is a measure of the depth of the impedance dip compared to the characteristic impedance of the series RLC circuit. In a high q-factor circuit, the minimum impedance is very small compared to the characteristic impedance. The appearance of the resonant dip is pointed and sharp for high q-factor circuits.

Exactly the same analysis applies to peaks in a parallel RLC circuit. [Figure 2.11](#) shows the impedance curves for the same RLC elements in parallel, with q-factor values corresponding to 0.1, 1, and 10.



**Figure 2.11** Impedance profile of parallel RLC circuit with  $L = 10 \text{ nH}$ ,  $C = 10 \text{ nF}$ , and three different q-factor values.

The value of the impedance peak at the parallel resonance is roughly related to the q-factor of the circuit and the characteristic impedance of the circuit, calculated with

$$Z_{\text{peak}} \sim \text{q-factor} \times Z_0 = \frac{R_{\text{parallel}}}{Z_0} \times Z_0 = R_{\text{parallel}} \quad (2.27)$$

For this equation, the resistance is in parallel with L and C. If the resistor had been in series with either the capacitor or inductor of the parallel resonant circuit, the equation would have been

$$Z_{\text{peak}} \sim \text{q-factor} \times Z_0 = \frac{Z_0}{R_{\text{series}}} \times Z_0 = \frac{1}{R_{\text{series}}} \frac{L}{C} \quad (2.28)$$

For the L and C of the preceding circuit, the characteristic impedance is  $1 \Omega$ . For the three different values of q-factors, the peak impedances are  $10$ ,  $1$ , and  $0.1 \Omega$ .

**Tip**

An important way of reducing peak impedances in parallel RLC circuits is increasing the damping, which decreases the q-factor of the circuit. We can accomplish this by increasing the series resistance or decreasing the parallel resistance.

To reduce the PDN impedance peak heights at resonant frequencies we engineer q-factor values close to 1. That is, to get the R close to the characteristic impedance of the RLC circuit, we engineer either a higher R, a lower L, or a higher C. In this and later chapters we show how these values become important design goals.

**Tip**

Two of the important figures of merit for a series or parallel RLC circuit are the characteristic impedance and q-factor. The peak impedance in a parallel circuit is related to  $Z_0 \times \text{q-factor}$  and the minimum impedance in a series circuit is related to  $Z_0 / \text{q-factor}$ .

## 2.8 EXAMPLES OF RLC CIRCUITS AND REAL CAPACITORS

In any parallel or series RLC circuit, there are four important figures of merit, the resonant frequency, characteristic impedance, q-factor, and maximum or minimum impedance for the parallel or series circuit, respectively. These describe the properties of these circuits and are valuable to always keep in mind:

$$\text{SRF} = \text{PRF} = \frac{1}{2\pi\sqrt{LC}} = \frac{159 \text{ MHz}}{\sqrt{LC}} \quad (2.29)$$

$$Z_0 = \sqrt{\frac{L}{C}} \quad (2.30)$$

$$\text{q-factor} = \frac{1}{R_{\text{series}}} \sqrt{\frac{L}{C}} = \frac{Z_0}{R_{\text{series}}} \quad (2.31)$$

$$Z_{\min} = R_{\text{series}} = \frac{1}{\text{q-factor}} Z_0, \quad (2.32)$$

or

$$Z_{\max} \sim \text{q-factor} \times Z_0 = \frac{Z_0}{R_{\text{series}}} \times Z_0 = \frac{1}{R_{\text{series}}} \frac{L}{C} \quad (2.33)$$

where

SRF = the series resonant frequency, in MHz

$Z_0$  = the characteristic impedance of the circuit, in  $\Omega$

q-factor = the Quality factor of the circuit

$Z_{\min}$  = the lowest impedance in the series RLC circuit

$Z_{\max}$  = the maximum impedance in the parallel circuit

$R_{\text{series}}$  = the resistance of the series resistor element in  $\Omega$

C = the capacitance of the capacitor element in nF

L = the inductance of the inductive element in nH

**Tip**

Every RLC circuit has four important figures of merit that describe their properties and important features. The first step in analyzing any RLC circuit is calculation of these four figures of merit.

**Example 1:** A large tantalum capacitor. This is modeled as a series RLC circuit with typical values of

$$C = 1000 \mu F = 10^6 nF$$

$$L = 8 nH$$

$$R = 0.05 \Omega$$

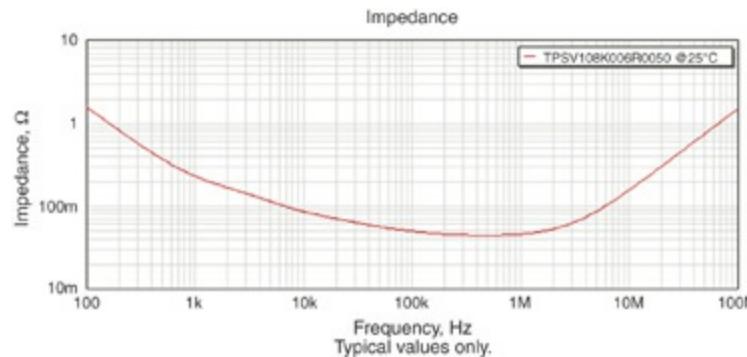
$$\text{SRF} = \frac{159 \text{ MHz}}{\sqrt{LC}} = \frac{159 \text{ MHz}}{\sqrt{8 \times 10^6}} = 56 \text{ kHz} \quad (2.34)$$

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{8}{10^6}} = 0.003 \Omega \quad (2.35)$$

$$\text{q-factor} = \frac{Z_0}{R} = \frac{0.003}{0.05} = 0.06 \quad (2.36)$$

$$Z_{\min} = R_{\text{series}} = 0.05 \Omega \quad (2.37)$$

In this example we see that the very large tantalum capacitor has a low q-factor and we expect a flat impedance profile. The impedance profile offered by AVX for a similar capacitor but with lower L and higher SRF is shown in Figure 2.12 to be very broad and flat.



**Figure 2.12** Suggested impedance profile for the tantalum capacitor in the example, provided by AVX Corp.

**Example 2:** A typical large MLCC (multilayer ceramic chip) capacitor in a 1206 body using X5R dielectric material

$$C = 10 \mu F = 10,000 \text{ nF}$$

$$L = 3 \text{ nH}$$

$$R_{\text{series}} = 0.003 \Omega$$

$$\text{SRF} = \frac{159 \text{ MHz}}{\sqrt{LC}} = \frac{159 \text{ MHz}}{\sqrt{3 \times 10^4}} = 0.9 \text{ MHz} \quad (2.38)$$

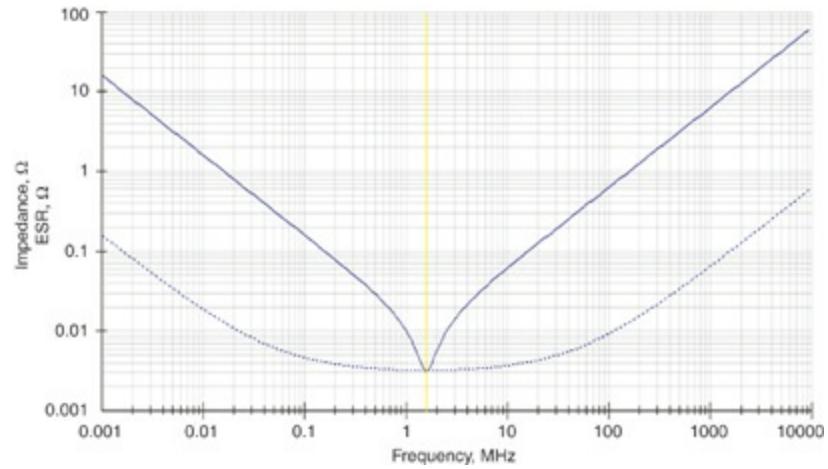
$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{3}{10^4}} = 0.017 \Omega \quad (2.39)$$

$$\text{q-factor} = \frac{Z_0}{R_{\text{series}}} = \frac{0.017}{0.003} = 5.7 \quad (2.40)$$

$$Z_{\min} = R_{\text{series}} = 0.003 \Omega \quad (2.41)$$

For this large value MLCC capacitor the q-factor is relatively large so we expect a sharp resonance. This is

due to the very low series R. The impedance profile provided by AVX is shown in [Figure 2.13](#). Their value of L is 1 nH, much more aggressive than may typically be achieved for this size capacitor when it is mounted on board and attached with vias. This accounts for the slightly higher SRF calculated by AVX compared to our earlier estimate.



**Figure 2.13** Impedance profile for 1206 10  $\mu\text{F}$  MLCC capacitor provided by AVX using an  $L = 1 \text{ nH}$ .

**Example 3:** A small value MLCC capacitor, 0402 body, X7R dielectric type

$$C = 1 \text{ nF}$$

$$L = 1 \text{ nH}$$

$$R_{\text{series}} = 0.16 \Omega$$

$$\text{SRF} = \frac{159 \text{ MHz}}{\sqrt{LC}} = \frac{159 \text{ MHz}}{\sqrt{1 \times 1}} = 159 \text{ MHz} \quad (2.42)$$

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{1}{1}} = 1 \Omega \quad (2.43)$$

$$\text{q-factor} = \frac{Z_0}{R_{\text{series}}} = \frac{1}{0.16} = 6 \quad (2.44)$$

$$Z_{\min} = R_{\text{series}} = 0.16 \Omega \quad (2.45)$$

For the small value capacitor the resistance element is

about 50 times larger than the large capacitor's due primarily to fewer conductor plates in parallel. However, the higher characteristic impedance results in a q-factor value that is still comparable.

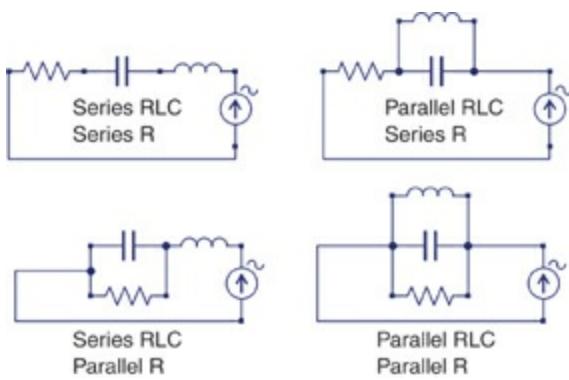
## **2.9 THE PDN AS VIEWED BY THE CHIP OR BY THE BOARD**

The terms *parallel* and *series* refer to the circuit topology of the L and C elements. Their connection topology determines whether the impedance will be a minimum or a maximum at the resonant frequency. A parallel circuit has the impedance measured for a parallel inductor and capacitor. The loss element (resistor) can either be in parallel or series with a parallel resonant circuit. It is often expressed as ESR (equivalent series resistance) even when the inductor and capacitor are in parallel. A series circuit has the impedance measured for an inductor and capacitor in series.

**Tip**

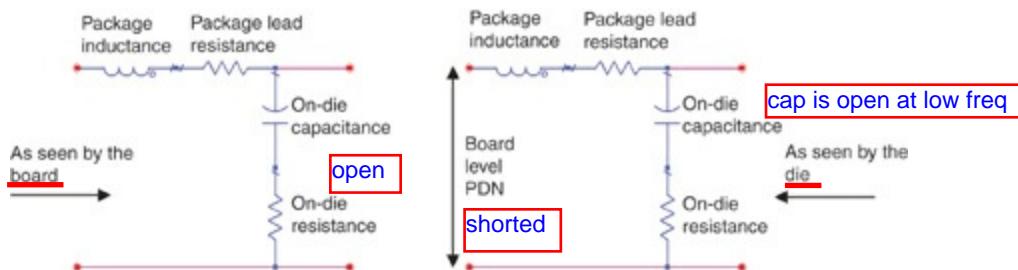
When L and C are measured in parallel the impedance is a maximum. When L and C are measured in series the impedance is a minimum.

The first step to determine which type of circuit we have and whether to expect a peak or dip in impedance is to identify where in the circuit the measurement or simulation is being performed. From this perspective, we identify the circuit topology of the L and C elements. Finally, we identify whether the resistance term is in series or parallel with the L or C and the source. Figure 2.14 shows the four combinations of series and parallel LC and series or parallel resistance.



**Figure 2.14** Four different circuit topologies identifying the simulation source location, the combination of the L and C elements, and the combination of the resistor damping term.

A typical PDN circuit appears differently depending on the perspective from where we look [6]. As viewed from the chip side looking into a low impedance board, the PDN looks like a parallel LC circuit with series resistance. When viewed from the board looking into the chip, the circuit looks like a series LC circuit, with a series resistance. Figure 2.15 illustrates these two perspectives for the same circuit.



**Figure 2.15** The same circuit describing the on-die capacitance and package lead inductance viewed from two different perspectives. From the board, the impedance will have a dip. From the die, the impedance will have a peak.

When viewed from the board, looking through the package to the chip, the package lead inductance is in series with the on-die capacitance. The impedance looking into the chip appears as a series RLC circuit with a low impedance dip. At the high-frequency end the impedance continues to increase with frequency dominated by the package lead inductance.

### Tip

This means we can only see the low-frequency impedance of the on-die environment from the board. The high-frequency properties of the die's local PDN environment are blocked from the board view by the package lead inductance and the low impedance of the on-die capacitance.

From the die's perspective, looking into the rest of the low-impedance board-level PDN, the on-die capacitance is in parallel with the package lead inductance resulting in a peak impedance. At high frequency the impedance decreases with frequency dominated by on-die capacitance and ultimately limited by the on-die metallization.

At low frequency the chip sees its impedance shorted by the package lead inductance connected to the low impedance board. The board-level impedance, including the VRM, has an impedance decreasing toward lower frequency. From the die's perspective the low-frequency impedance is ultimately limited by the series resistance of the package leads and the resistance of the rest of the board path. //

There are two contributions to the series resistance in the package and die. The on-die metallization of the PDN rails is a resistance in series with the on-die capacitance. The lead resistance of the package leads and the vias to the circuit board is a resistance in series with the package lead inductance. The equivalent series resistance of the four elements when in series, as viewed from the board, is just the sum of the on-die metallization and the package lead resistance. The series impedance of the four circuit elements is independent of their order in the series circuit.

ESR The equivalent series resistance of the parallel circuit as viewed by the die is slightly more complicated. At low frequency, the chip sees a high impedance from the on-

reason why pkge inductance, but not board inductance :

- pkge inductance is much bigger (due to narrow line) and much closer to on die cap, hence create an more dominant LC circuit

- board/PCB use wide planes, so inductance is low cmp to pkge

Fig. 2.15  
Right figure

Figure 2.15

die capacitance shorted to the board environment by the low impedance of the package leads. The impedance is dominated by the package lead resistance at low frequency in series with the rest of the circuit board. At high frequency the impedance from the on-die capacitance is low and the impedance the chip sees is dominated by the series resistance of the on-die metallization.

Fig 2.15 Right figure,  
when freq is high,  
cap is shorted, so  
die resistance  
dominates

Near resonance, the current flows in a loop through the parallel L and C combination including both the package lead resistance and on-die resistance. These losses add, and this circuit near resonance looks like a parallel RLC circuit with the equivalent resistance as the series combination of the lead resistance and on-die metallization resistance.

**Tip**

The same circuit and interconnect structures look like a parallel RLC circuit with a peak impedance when viewed from the chip side and as a series RLC circuit with a minimum impedance when viewed from the board side.

seen from board side

The same figures of merit for series and parallel RLC circuits apply to this special case of the two views of the PDN, provided we replace the R by the series combination of the package lead and on-die metallization resistances. This is the equivalent series loop resistance.

For a small die, typical values might be

$$C_{\text{die}} = 50 \text{ nF}$$

$$L_{\text{package}} = 0.5 \text{ nH}$$

$$R_{\text{leads}} = 0.01 \Omega$$

$$R_{\text{metallization}} = 0.005 \Omega$$

$$R_{\text{equivalent}} = 0.015 \Omega$$

We expect these figures of merit to be:

$$\text{SRF} = \text{PRF} = \frac{1}{2\pi} \frac{1}{\sqrt{\text{LC}}} = \frac{159 \text{ MHz}}{\sqrt{0.5 \times 50}} = 31.8 \text{ MHz} \quad (2.46)$$

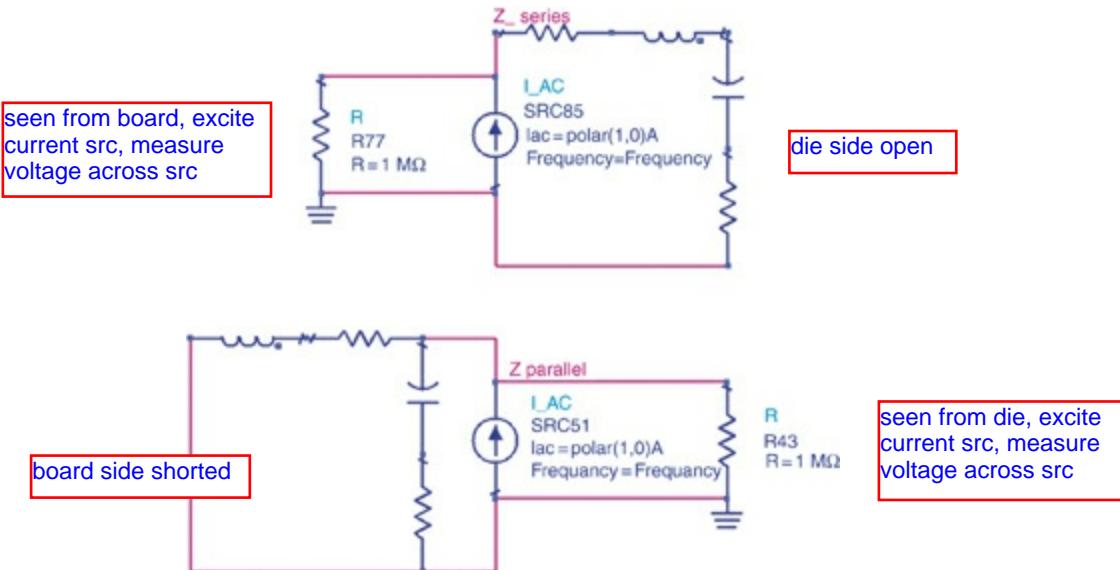
$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{0.5}{50}} = 0.1 \Omega \quad (2.47)$$

$$\text{q-factor} = \frac{1}{R_{\text{series}}} \sqrt{\frac{L}{C}} = \frac{Z_0}{R_{\text{series}}} = \frac{0.1}{0.015} = 6.7 \quad (2.48)$$

$$Z_{\min} = R_{\text{series}} = \frac{1}{\text{q-factor}} Z_0 = \frac{1}{6.7} 0.1 = 0.015 \Omega \quad (2.49)$$

$$Z_{\text{peak}} \sim \text{q-factor} \times Z_0 = \frac{Z_0}{R_{\text{series}}} \times Z_0 = \frac{1}{R_{\text{series}}} \times \frac{L}{C} = \frac{1}{0.015} \times \frac{0.5}{50} = 0.67 \Omega \quad (2.50)$$

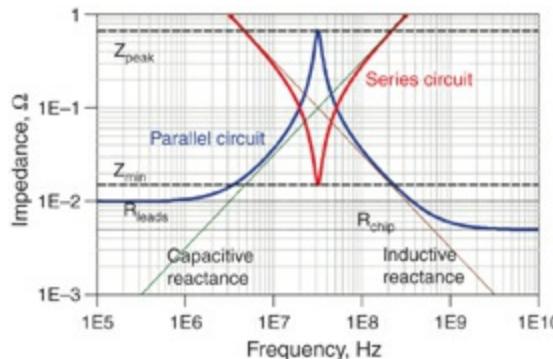
Note the q-factors for these circuits are high, suggesting a peaked response. We can simulate two cases using the circuit shown in [Figure 2.16](#). The impedance profiles of these two circuits are very different, even though they are composed of the same elements.



**Figure 2.16** Circuit topology for the PDN, viewed from two different sides, appearing as a parallel or series circuit.

The simulated impedances of the circuits of [Figure 2.16](#), with the element values defined above, are shown in [Figure 2.17](#). From the impedance profile we can

compare the figures of merit with the estimates. The agreement is excellent.



**Figure 2.17** Impedance of the parallel and series RLC circuits with the impedance of just the L and C elements, and the min and peak impedances, using  $C = 50 \text{ nF}$ ,  $L = 0.1 \text{ nH}$ ,  $R_{\text{chip}} = 0.005 \Omega$ , and  $R_{\text{leads}} = 0.01 \Omega$ . Note the excellent agreement of the min and max values with the figure of merit estimates.

This circuit is important to consider when measuring the PDN. How the impedance measurement is hooked up influences the impedance profile and exactly what is measured.

## 2.10 TRANSIENT RESPONSE

The impedance profile of a circuit is a direct indicator of the voltage noise that would appear across it if a current were to flow through it [7]. When a frequency component of the current flows through the impedance, the voltage generated at that frequency is related to the current amplitude and the impedance.

$$V_{\text{noise}}(f) = I(f) \times Z(f) \quad (2.51)$$

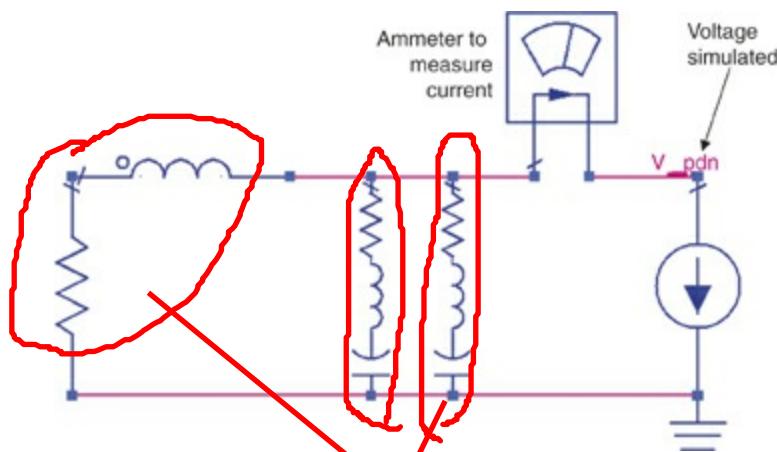
Note that when we do a frequency domain analysis we are evaluating *only* the steady-state time-invariant response. We are effectively assuming each frequency component of the current has been on forever and the voltage response is the steady-state response. This is often the desired response; however, there are a few cases, often referred to as rogue waves, as explored in

Chapter 9, where the transient response reveals new behavior not apparent in the frequency domain.

**Tip**

The frequency domain response is a good first-order estimate and can assist in quick estimates of the voltage response of the PDN. However, it is not the complete response, especially when the current source has complicated behavior. This is why analyzing a transient response is also important.

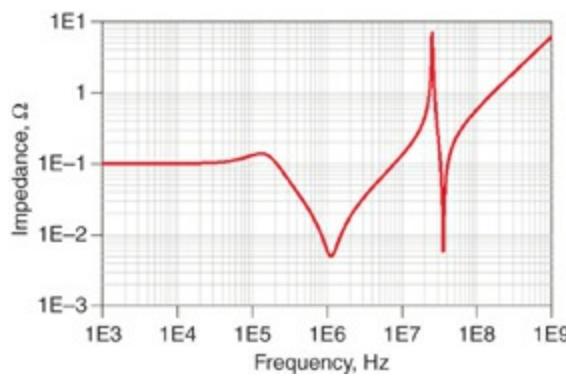
Although analytically calculating the transient voltage across a complex impedance profile for an arbitrary current waveform is difficult, simulating the voltage noise associated with an arbitrary impedance profile is easy. Figure 2.18 shows an example of a SPICE circuit to simulate the transient voltage noise generated from a transient current source.



**Figure 2.18** Typical circuit model to simulate the voltage generated across a combination of RLC circuits as transient current flows. The ammeter is there to display the transient current.

In this example, the R and L elements on the left edge of the circuit model have been added to emulate the impedance profile of a voltage regulator module (VRM). The two series RLC circuits have been added to emulate real decoupling capacitors. As a prelude to simulating the transient response, we first look at the impedance profile of this circuit in the frequency domain. It is

shown in Figure 2.19.



**Figure 2.19** Impedance profile for the circuit in the earlier example, with the VRM model added. Note the parallel resonance at about 25 MHz.

When frequency components of the current at the PRF of 25 MHz flow through the circuit they see a larger impedance and generate a larger voltage across the circuit.

In the time domain, the noise generated by the PRF appears as ringing at the PRF frequency. In the transient simulation the magnitude of the ringing depends on how much amplitude exists in the current waveform at the PRF.

The bandwidth of the current waveform reveals the highest expected sine wave frequency and is roughly related to the current rise time by

$$BW = \frac{0.35}{RT} \quad (2.52)$$

where

BW = the bandwidth of the signal, in GHz

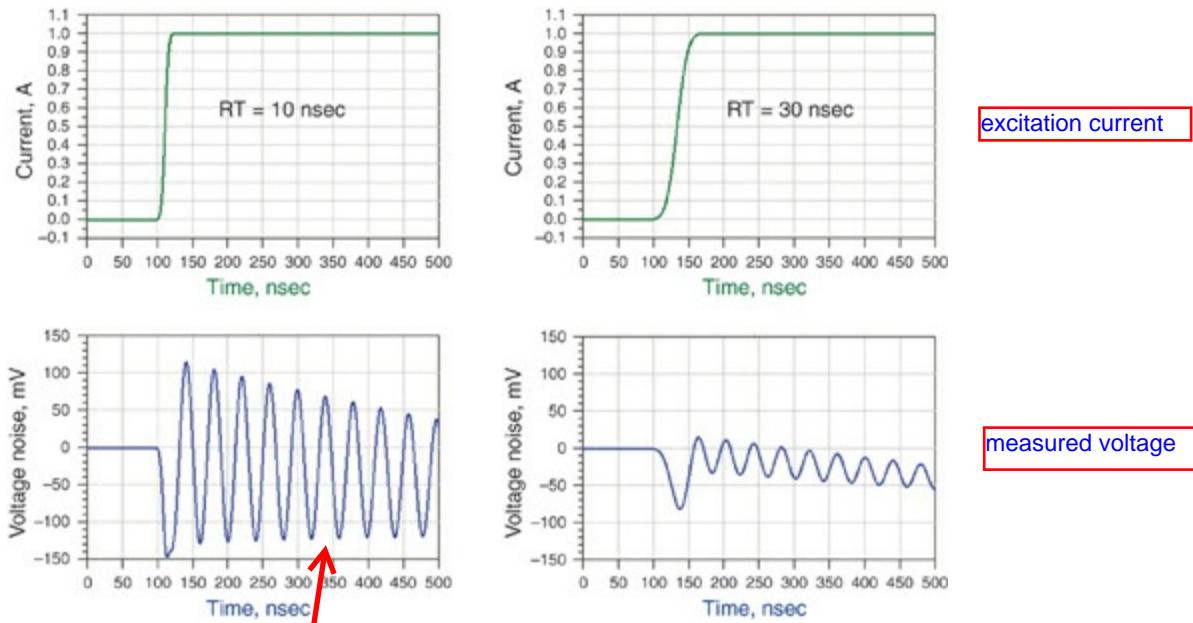
RT = the 10–90 rise time of the waveform, in nsec

For example, a current waveform rise time of 10 nsec gives a bandwidth of

$$BW = \frac{0.35}{10} = 0.035 \text{ GHz} = 35 \text{ MHz} \quad (2.53)$$

For a 10 nsec rise time current step we expect to see frequency components up to 35 MHz but not much beyond. If this current step were to pass through the circuit of Figure 2.18 with its PRF at 25 MHz, we expect to see ringing at 25 MHz from the high impedance.

If we increase the rise time of the current step to 30 nsec, the bandwidth decreases to about 10 MHz. The amplitude of the current component at 25 MHz is less and the voltage noise we expect to see is reduced. This example is shown in Figure 2.20, where we show the transient current waveform with a 10 nsec and 30 nsec rise time and the resulting transient voltage noise across the circuit of Figure 2.18.



**Figure 2.20** Simulated transient current with a step response using two different rise times and the resulting voltage noise generated across the circuit of Figure 2.18.

Note that even though the current waveform is a smooth Gaussian edge, the voltage generated across the circuit shows very large ringing at the PRF where the impedance has peaks.

The PRF of this circuit is 25 MHz. The period of the ringing is 40 nsec in both of these plots and corresponds to the PRF. Even though the rise time changed, the

ringing frequency did not. The ringing frequency is intrinsic to the circuit and related to the PRF, not the current waveform.

**Tip**

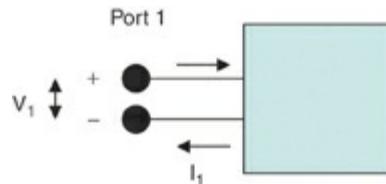
Ringing voltage noise measured on a PDN is often an indication of peaks in the impedance profile. The magnitude of the ringing is related to the peak height and the energy content in the current waveform at the ringing frequency. This is why parallel resonances are so important in PDN design.

The amplitude of the ringing depends on the relative energy in the current step at the ringing frequency. The longer the rise time, the less energy at 25 MHz and the lower the amplitude of the noise.

This is why parallel resonances are an important principle in PDN design. The frequency components of the current and the peak impedance at the PRF determine the amplitude of the noise for the PDN.

## 2.11 ADVANCED TOPIC: THE IMPEDANCE MATRIX

Impedance is fundamentally defined as the ratio of the voltage to the current. It is trivial to see this when applied to a two-terminal component. A generalized circuit with two terminals is shown in Figure 2.21.



**Figure 2.21** A generalized circuit with two terminals.

It doesn't matter what the circuit looks like inside the box. The circuit could be a single R, L, or C element, or it could be 25 elements connected together in a complex network, as long as there were only the two connections to the outside world as shown.

The impedance of the circuit is defined by the properties at its terminals, in this case labeled as port 1. The basic fundamental definition of impedance is based on the ratio of the voltage appearing across the terminals,  $V_1$  to the current going in and coming out,  $I_1$  as

$$Z = \frac{V_1}{I_1} \quad (2.54)$$

where

$V_1$  = the voltage between the terminals at port 1

$I_1$  = the current into and out of port 1

When there is just one pair of terminals the definition of the impedance of the circuit is trivial. When there are multiple pairs the impedance can still be defined but takes on a more complex meaning and contains much more information about the behavior of the circuit. As the number of pairs of terminals grows, the complexity of the circuit grows exponentially. To simplify the description of the various impedances and to more efficiently leverage the information buried in these impedances, a matrix formalism is adopted [8]. This is a compact, efficient way of describing multiple pairs of terminals.

**Tip**

The principles of impedance, while initially defined for a two-terminal device, can be extended to many more terminals. The matrix formalism is important to minimize the complexity as the number of terminals increases.

In this formalism, each pair of terminals is called a port. At each port there are two terminals between which the voltage is defined. Voltage is always a difference in potential between two points. The current

is defined as the current going into one of the terminals and returning out the other terminal.

In an n-port circuit, there are n voltages and n currents. The impedance, as a ratio of a voltage to a current, can be defined for any combination of voltage and current. To keep track of each different ratio, a matrix is used to store the impedance values. Each element in the matrix corresponds to a different ratio. The rows are the ports at which the voltage is selected and the columns are the ports at which the currents are selected. In this way, the impedance matrix is defined as

$$Z_{jk} = \frac{V_j}{I_k} \quad (2.55)$$

where

$V_j$  = the voltage on port j

$I_k$  = the current going into port k

This formalism applies to a linear, passive, time-invariant system. This means that the circuit elements inside the box do not change. No new connections are being created and the circuit is fixed. During any period of time in which a sine wave signal is applied, the impedance of every matrix element is constant. This is the case for all passive interconnect circuits.

A linear network requires that a single sine wave going in at frequency f results in a response at only that sine wave frequency. No harmonics are generated and linear superposition applies. This means that the impedance of any element is completely independent of the voltage or current associated with any terminal. This is the case for all interconnect structures except some ferrites.

The impedance matrix defines how all the combinations of voltages and currents are linked

together:

$$V_j = \sum_k Z_{jk} \times I_k \quad (2.56)$$

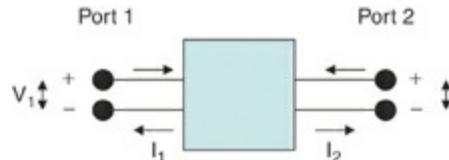
**Tip**

Each impedance matrix element relates the ratio of the voltage generated on a port to the current through a port.

In the frequency domain the voltages and currents are complex so the impedance matrix is complex and generally varies with frequency. Each impedance matrix element is complex and frequency dependent. Writing this explicitly is useful to remind us of this complex nature:

$$\tilde{V}_j(\omega) = \tilde{Z}_{jk}(\omega) \times \tilde{I}_k(\omega) \quad (2.57)$$

A simple example illustrates the power of the impedance matrix. [Figure 2.22](#) shows a two-port generalized circuit.



**Figure 2.22** Generalized two-port circuit with the voltages and currents at each port defined.

This circuit has two voltages and two currents. Four combinations of voltage and current can be combined in a ratio as an impedance. Each one has a separate and significant meaning.

The combination of all the impedance matrix elements can be grouped in a simple  $2 \times 2$  matrix:

$$Z = \begin{vmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{vmatrix} \quad (2.58)$$

This matrix defines the relationship between the combination of voltages on each node and the currents going into each node. Using matrix formalism the connection between the voltages on each node and the currents into each node is

$$\begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = \begin{vmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{vmatrix} \times \begin{vmatrix} I_1 \\ I_2 \end{vmatrix} \quad (2.59)$$

We write the equations defined by this matrix as

$$\begin{aligned} V_1 &= Z_{11} \times I_1 + Z_{12} \times I_2 \\ V_2 &= Z_{21} \times I_1 + Z_{22} \times I_2 \end{aligned} \quad (2.60)$$

These equations further refine the definition of the impedance matrix elements. A specific impedance matrix element can be isolated from the others by setting all the currents except the current into one port to zero. For example, to obtain a diagonal element set all the other currents = 0 except the diagonal port. We calculate these as

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \quad \text{and} \quad Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0} \quad (2.61)$$

The diagonal elements are called the “self” impedances. These represent the impedances seen at one port as the ratio of the voltage on that port to the current into that port when there is no current into any other port.

#### Tip

The diagonal elements of the impedance matrix are the self-impedances. When all the currents into other ports are 0 and left open, the self-impedance is the same as the two-terminal impedance.

We extract the off-diagonal elements, referred to as the *mutual* or *transfer* impedances or *transimpedances*,

in the same way by setting the currents into all other ports to 0. This is easily implemented by keeping the ports with zero current as open circuits with nothing connected. When  $I_1 = 0$ , the voltage on port 1 converts to

$$V_1 = 0 + Z_{12} \times I_2 \quad (2.62)$$

From this relationship, we calculate one of the off-diagonal elements as

$$Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} \quad (2.63)$$

In the same way, we calculate the second off-diagonal or transfer impedance as

$$Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} \quad (2.64)$$

The term *transfer impedance* is also used to describe the shielding effectiveness of conductors such as cable shields and enclosures. In this application, transfer impedance is the ratio of the voltage generated on one side of the conductor when there is a current on the other side. It is a measure of the transfer of energy from an outside surface to an inside surface.

The term *transimpedance* also relates to a device that converts a current into a voltage. A simple resistor does this and has a transimpedance that is the ratio of the voltage to the current equal to its resistance. A transimpedance amplifier, using an operational amp with a resistor in its feedback loop, has a transimpedance, which may start out very high but drop off with frequency as the gain-bandwidth of the amplifier is exceeded.

When used to describe the off-diagonal elements of

the impedance matrix, transfer impedance and transimpedance also relate to a current in one region creating a voltage in another.

The transfer impedances in the impedance matrix describe the coupling between a current going into one port and creating a voltage on another port. If the transfer impedance between two ports were zero, a current into one port would create 0 V on the second port. There would be no coupling at all.

In the opposite extreme, if the two ports were so tightly coupled they were literally connected together, a current into one port would create the same voltage on both ports. The transfer impedance would be the same as the self-impedances of each port. These are the two extremes of transfer impedance. A value of 0 Ω means no coupling between the ports and a value equal to the self-impedances of both ports means the ports are 100% coupled together.

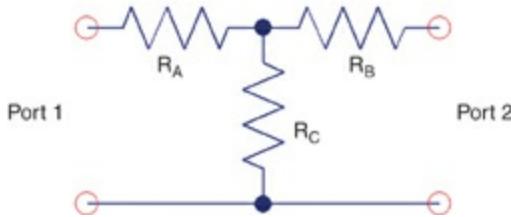
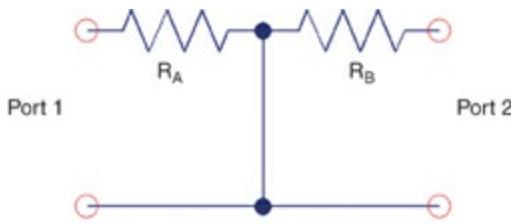
The concept of transfer impedance is very subtle and confusing because of the intuition we have of impedance. A transfer impedance does not connect between two ports. It is not the impedance between the two ports as would be measured by an ohmmeter between the ports. Rather, it describes the relationship between a current into one port and the voltage appearing on another port. It is a measure of the coupling.

**Tip**

A transfer impedance does not connect between two ports. It is not the impedance between the two ports as would be measured by an ohmmeter between the ports. Rather, it describes the relationship between a current into one port and the voltage appearing on another port. It is a measure of the coupling.

The two circuit examples, shown in [Figure 2.23](#),

illustrate the properties of the impedance matrix elements.



**Figure 2.23** Two different two-port circuits with very different transfer impedances.

In the top circuit, the center ends of the resistors are connected to the return path with a zero Ohm path. Using the definition of the self-impedance, the self-impedances of each port are just the resistances:

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} = R_A \quad \text{and} \quad Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0} = R_B \quad (2.65)$$

The transfer impedances for this circuit are each 0. When the current into port 1 is  $I_1 = 0$ , there is an open circuit at port 1. No current flows through the resistor at port 1 and there cannot be any voltage drop across it. No matter what the current into node 2, the voltage generated on node 1 is  $V_1 = 0$ :

$$Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} = \left. \frac{0}{I_2} \right|_{I_1=0} = 0 \quad (2.66)$$

Likewise, the other transfer impedance = 0:

$$Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} = \left. \frac{0}{I_1} \right|_{I_2=0} = 0 \quad (2.67)$$

In this circuit, the impedance matrix is

$$Z = \begin{vmatrix} R_A & 0 \\ 0 & R_B \end{vmatrix} \quad (2.68)$$

This matrix describes a circuit with no coupling between the ports.

In the bottom circuit, we see that the diagonal impedance elements are

$$Z_{11} = R_A + R_C \quad \text{and} \quad Z_{22} = R_B + R_C \quad (2.69)$$

The transfer impedance terms are more interesting in this circuit. When the current into port 1 is 0, port 1 is an open circuit. In this case current flowing into port 2,  $I_2$  generates a voltage across the resistor C. This voltage appears at port 1. The transfer impedance terms are

$$Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} = R_C \quad \text{and} \quad Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} = R_C \quad (2.70)$$

The resulting impedance matrix for this circuit is:

$$Z = \begin{vmatrix} R_A + R_C & R_C \\ R_C & R_B + R_C \end{vmatrix} \quad (2.71)$$

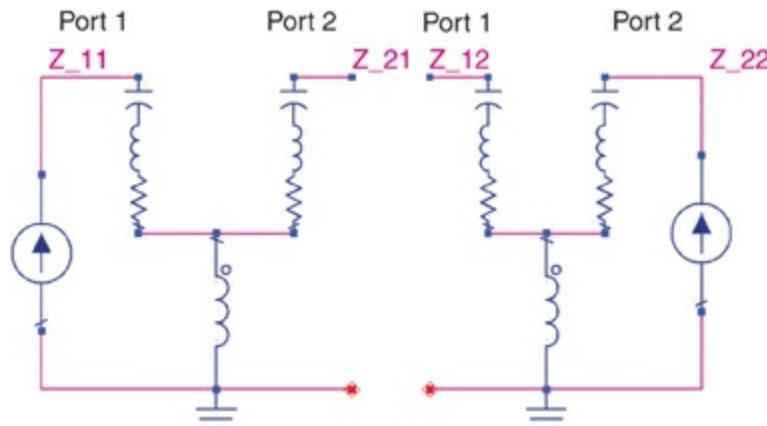
The transfer impedances describe the amount of coupling between the ports. The larger the transfer impedance, the larger the coupling. The limit is when the transfer impedance is equal to the self-impedance. As  $R_C$  increases and  $R_A$  and  $R_B$  stay the same, the transfer impedance approaches the limit of being equal to the self-impedances.

#### Tip

The transfer impedances describe the amount of coupling between the ports. The larger the transfer impedance, the larger the coupling, until the transfer impedance is the same as the self-impedance.

These examples use resistive elements to illustrate the impedance matrix. In general each element is complex and varies with frequency. When the circuit between the two ports inside the box is a complicated circuit, extracting the impedance matrix elements may only be possible by simulation.

Using the principles outlined earlier in this chapter, we can simulate each element of the impedance matrix for any arbitrary circuit. For example, we can easily simulate the impedance matrix elements for two RLC circuits with a common lead inductance using the circuits shown in [Figure 2.24](#). Recall that to set a current into one port to be 0, it is only necessary to keep that port open.



**Figure 2.24** Two two-port circuits used in the simulation of the four impedance matrix elements. Each circuit is identical. The AC current source is used to force current into each port separately, while keeping the other port open.

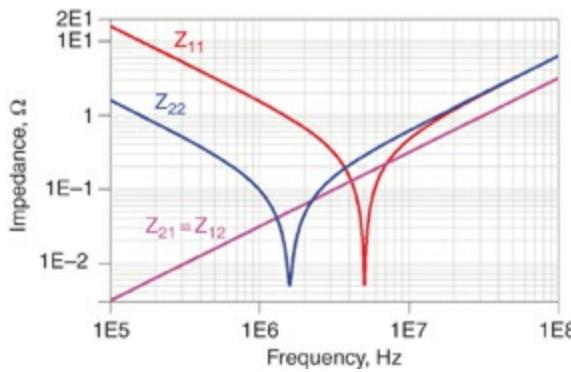
In the circuit on the left, a current is forced into port 1 and the voltage on port 1 and port 2 is simulated. The ratio of the voltage on port 1 to the current into port 1 is the self-impedance,  $Z_{11}$ , and the ratio of the voltage on port 2 to the current forced into port 1 is the transfer impedance,  $Z_{21}$ . When the current forced into port 1 is a 1-amp amplitude, the voltages on the other ports are numerically the impedances:

$$Z_{11} = \frac{V_1}{I_1} \Big|_{I_2=0} \quad \text{and} \quad Z_{21} = \frac{V_2}{I_2} \Big|_{I_2=0} \quad (2.72)$$

Likewise, in the circuit on the right, current is forced into port 2 while the open circuit sets the current into port 1 = 0. The simulated voltages on ports 1 and 2 are numerically the impedances we get with

$$Z_{22} = \frac{V_2}{I_2} \Big|_{I_1=0} \quad \text{and} \quad Z_{12} = \frac{V_1}{I_1} \Big|_{I_1=0} \quad (2.73)$$

In this way, we can simulate the impedance matrix elements of any circuit with any version of SPICE. In this example, the two RLC circuits have the same value of L and R, being 5 nH and 0.005 Ω, respectively. The C of the capacitor attached to port 1 is 1000 nF and 100 nF for the capacitor on port 2. The common lead inductance is 5 nH. The simulated impedance matrix elements are shown in Figure 2.25.



**Figure 2.25** Simulated impedance matrix elements for the circuit shown in Figure 2.24.

The self-impedances are each due to the RLC circuit, with the common lead inductance in series in each circuit. Although each circuit has a different capacitance, the equivalent inductance of each circuit is the same, and the self-impedance at the high-frequency limit for each port is the same.

The **transfer impedance** is the ratio of the voltage generated on one port when current is forced into the

other port. In this example, the voltage generated in the other port is due to the current flowing through the common lead inductance of 5 nH. The transfer impedance, from either side, is the impedance associated with the 5 nH inductor. In the simulated response, we see that both  $Z_{12}$  and  $Z_{21}$  are that of a 5 nH inductor.

The impedance matrix formalism presented in this chapter applies to all circuits. Later chapters expand on this concept to describe not just lumped circuit elements but also distributed elements and the waveguide cavities defined by power and ground planes.

## 2.12 THE BOTTOM LINE

1. The voltage noise on the PDN is related to the combination of the current spectrum from the die and the impedance profile of the PDN.
2. Impedance is always V/I in both the frequency and time domains. For circuit elements that contain C or L elements, impedance has a simpler form in the frequency domain where currents and voltages are always sine waves.
3. Do not confuse real circuit elements, which are the only thing that can be measured, with ideal circuit elements, which are the only thing that can be simulated.
4. The impedance of many complicated, real structures can be described by simple combinations of ideal RLC circuit elements.
5. The two most important circuit configurations to understand are the series RLC and parallel RLC circuits. These are powerful models for real PDN elements.
6. Every RLC circuit has four important figures of merit: the series or parallel resonant frequency,

the characteristic impedance, the q-factor, and the min or max impedance. These should always be the first quantities estimated for every RLC circuit.

7. The most important features of the impedance profile of the PDN are the peaks caused by the parallel resonances. These are related to  $Z_0 * q$ -factor, the characteristic impedance of the RLC circuit and the q-factor of the circuit.
8. The ringing frequency of a circuit when stimulated with a transient current is determined by the peak impedance frequency in the PDN.
9. The impedance matrix is a powerful extension of the concept of impedance to include multi-terminal circuits. In this environment, each pair of terminals is called a port.
10. In the impedance matrix, the diagonal elements (called the self-impedance) relate to the impedance seen at each port. The off-diagonal elements (called the transfer impedance) relate to the coupling between each port. A small value of transfer impedance means very little coupling.

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# **Chapter 3. Measuring Low Impedance**

## **3.1 WHY DO WE CARE ABOUT MEASURING LOW IMPEDANCE?**

The design of a robust power distribution network is really about designing to a target impedance profile across a wide frequency range, from DC to the bandwidth of the highest frequency signals. Among different applications, this target impedance may range from higher than  $1\ \Omega$  to a value in some applications to lower than  $1\ m\Omega$ .

Simulation is a critical part of the analysis process for the design of each PDN element and the entire ecology. Measurement of system components and correlation back to simulation is just as important.

Measurements not only verify that a manufactured component meets the performance spec but also verify the accuracy of the simulation tool and the process of translating a physical design into the simulation environment. Measurements are a final test that the entire PDN ecology is acceptably close to meeting the target impedance. If it is not, measurement can be an important tool to speed up the debug process. The challenge is to measure the impedance of structures as low as  $1\ m\Omega$  and low impedances up to frequencies exceeding 1 GHz.

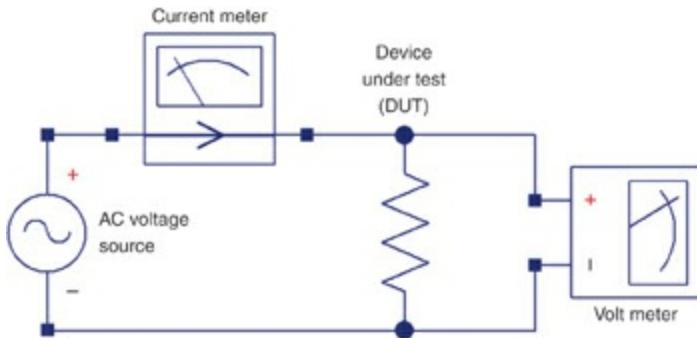
## **3.2 MEASUREMENTS BASED ON THE V/I DEFINITION OF IMPEDANCE**

One fundamental definition of the impedance of a two-terminal device is the ratio of the voltage across it to the current through it. This is the basis of an impedance analyzer in a circuit simulation and for measuring the impedance of a component at low frequency.

**Tip**

One fundamental definition of impedance is based on the ratio of the voltage across and the current through a device under test (DUT). This is only one definition of impedance; the next section introduces another one.

In principle, we apply a sine wave voltage at one frequency across a device under test (DUT) and measure the amplitude and phase of the current through it, as illustrated in Figure 3.1.



**Figure 3.1** Calculate impedance by measuring the voltage across and current through a DUT.

We calculate impedance from

$$Z(f) = \frac{V(f)}{I(f)} \quad (3.1)$$

where

$Z(f)$  = the impedance of the DUT

$V(f)$  = the voltage measured across it, as a complex voltage

$I(f)$  = the current through the DUT, as a complex current

This is the measurement basis for many low-end impedance analyzers. A sine wave voltage source drives a signal across the DUT and the current through it is measured. The ratio of the voltage across it to the current through it, together with the phase, is the impedance of the DUT.

This approach has an upper frequency limit based on the highest practical frequency to directly measure the current through the DUT. At frequencies above 100 MHz measuring impedance based on another definition of impedance is often more cost effective.

### **3.3 MEASURING IMPEDANCE BASED ON THE REFLECTION OF SIGNALS**

A completely different definition of impedance leverages an important property of propagating waves reflected at an interface. This definition is based on one of the most essential principles of signal integrity that signals are dynamic, being both a propagating voltage wave and a current loop. You can do nothing to prevent them from propagating down an interconnect in a specific direction.

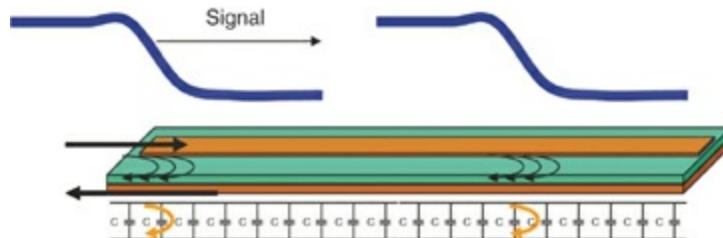
After a voltage is applied across the two conductors that make up a transmission line, involving a signal and return path, the voltage difference travels down the transmission line at the speed of electromagnetic propagation in the material surrounding the conductors. In addition to the voltage wave front, a propagating current wave front exists that has two directions associated with it.

#### **Tip**

The most important principle in signal integrity is that signals are dynamic and constantly propagate down a transmission line. The signal is the voltage difference between the signal and return conductors. The current propagates as a current-loop wave front with both a direction of propagation and a direction of circulation.

The current wave front propagates in the same direction as the voltage and has a direction of circulation. A positive voltage signal, propagating from the left to the right, is a current loop flowing between the signal and return path propagating from left to right and circulating in the clockwise direction. A negative

voltage signal is a current wave propagating from left to right, flowing from the return to the signal conductor, circulating in the counterclockwise direction. Figure 3.2 illustrates this.



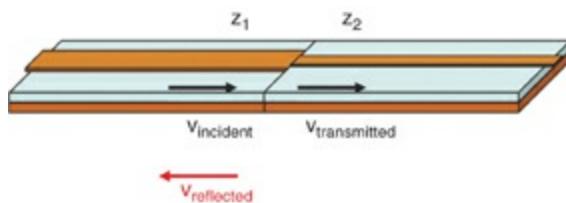
**Figure 3.2** A propagating signal showing the voltage and current waves at two locations down a transmission line.

As this wave propagates, it reacts to the instantaneous impedance each step along the way. If the instantaneous impedance is constant, the voltage and current waves propagate undistorted. If the instantaneous impedance changes for any reason, a reflected wave is created and the transmitted wave is distorted.

**Tip**

All signals are dynamic and *always* propagate down a transmission line at the speed of light in the medium. Whenever they encounter a change in the instantaneous impedance, they reflect. This concept is the basis for the second method of measuring impedance.

Figure 3.3 illustrates a simple case of two different interconnects each with a different instantaneous impedance. When the signal propagating from left to right reaches the interface, it sees the change in instantaneous impedance. A reflected signal is created propagating from right to left and traveling back to the source. This is a dynamic process.



**Figure 3.3** A reflected signal is created whenever a signal encounters a change in the instantaneous impedance.

The reflected signal is related to the incident signal and the impedances on both sides of the interface. Using the definition of the impedance in both regions as  $V/I$  and based on the boundary conditions at the interface, we derive the reflection coefficient from

$$\rho = \text{rho} = \frac{V_r}{V_i} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad (3.2)$$

where

$\rho$  = the reflection coefficient

$V_i$  = the incident voltage propagating on side 1 from left to right

$V_r$  = the reflected voltage propagating on side 1 from right to left

$Z_1$  = the instantaneous impedance in region 1

$Z_2$  = the instantaneous impedance in region 2

This relationship applies in both the time domain and the frequency domain. In the time domain, the voltage at any instant of time along every part of the propagating wave front obeys this relationship.

In the frequency domain, all signals are sine waves and every sine wave has a frequency, amplitude, and phase. Voltage signals in the frequency domain are described with complex numbers. This means that ratios of voltages, the reflection coefficient, and impedances are all complex.

If the source impedance  $Z_1$  is well known, we can

calculate the second impedance ( $Z_2$ ), which caused the reflection, from the reflection coefficient. With a little algebra after rearranging the terms, we find the second impedance to be

$$Z_2 = Z_1 \frac{1+\rho}{1-\rho} \quad (3.3)$$

where

$\rho$  = the reflection coefficient

$Z_1$  = the instantaneous impedance in region 1

$Z_2$  = the instantaneous impedance in region 2

If the source impedance is set to  $50 \Omega$  and a propagating wave reflects from its terminals, we extract the input impedance of any two-terminal DUT from the reflection coefficient as

$$Z_{\text{DUT}} = 50\Omega \frac{1+\rho}{1-\rho} \quad (3.4)$$

This relationship represents a reflection method of defining impedance that is different from, but equivalent to, the ratio of voltage and current. The impedance is the “input” impedance of the device under test. If the DUT is a simple discrete component, such as an ideal resistor or capacitor, the input impedance is just the impedance of the element.

**Tip**

In the frequency domain, the impedance based on the reflected signal is the total integrated input impedance looking into the DUT. It depends in a complicated way on the impedance distribution along the entire distributed interconnect.

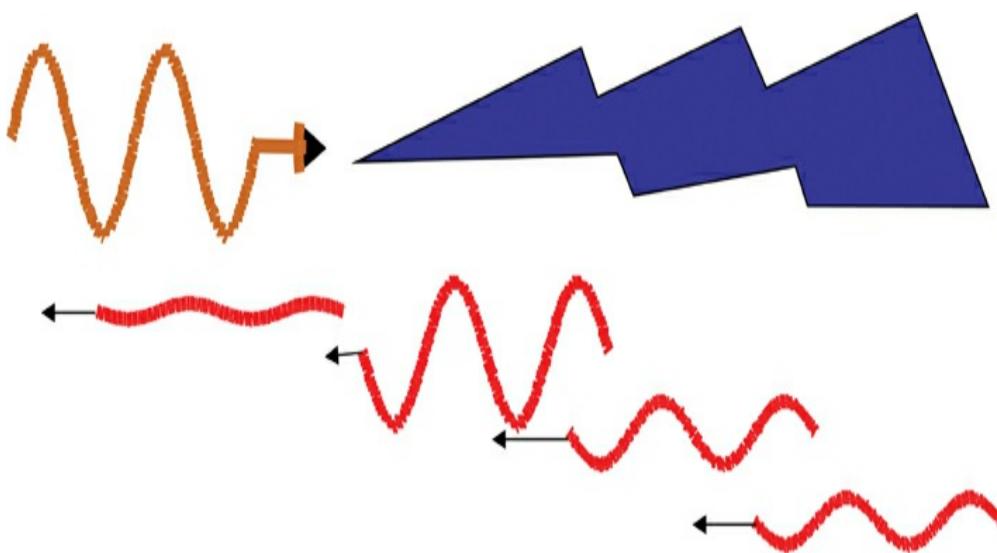
If the DUT is an extended object, such as an ideal resistor at the end of a fixture as shown in [Figure 3.4](#), opportunity exists for the incident signal to reflect off

the front of the fixture. The signal propagates through the fixture to the actual device under test and reflects from each and every discontinuity along the way with multiple bounces back and forth.



**Figure 3.4** Example of a discrete component at the end of an extended fixture. The incident wave reflects from multiple locations along the distributed fixture as well as from the DUT.

When the incident signal is a single sine wave, the reflected signal is the combination of each and every reflected sine wave from each and every interface including all the multiple bounces back and forth. The net reflected signal propagating back to the source is the sum of every sine wave, each with a different amplitude and a different phase and all with the same frequency, as illustrated in Figure 3.5.



**Figure 3.5** The reflected signal is the combination of all the reflected sine waves from every discontinuity and their multiple bounces. The lightning bolt represents an interconnect structure with widely varying impedance discontinuities distributed down its length that cause multiple reflections.

Remarkably, when a collection of sine waves with the same frequency but with arbitrary amplitudes and phases are added together, the resulting waveform is also a sine wave with the same frequency. The amplitude and phase of the reflected sine wave has information about the total net integrated impedance looking into the DUT from the  $50 \Omega$  source impedance. This alternative definition of input impedance is more general than the ratio of  $V/I$ , and is the basis of a measurement technique that applies to all structures up to very high frequency.

#### Tip

An alternative definition of the input impedance of a DUT is based on how much voltage from a known impedance reflects from the DUT. The reflection coefficient is a complex number and is a measure of the total integrated input impedance of the entire DUT at each frequency.

We measure the input impedance of a DUT by sending a propagating incident sine wave signal into the

DUT from a well-controlled impedance and measuring the reflected sine wave's amplitude and phase. From the known source impedance and the measured reflection coefficient, we extract the impedance of the DUT. This input impedance is the total input impedance looking in from the front of the connection and includes any fixture plus the DUT.

The instrument that routinely performs this sort of measurement is a vector network analyzer (VNA).

### 3.4 MEASURING IMPEDANCE WITH A VNA

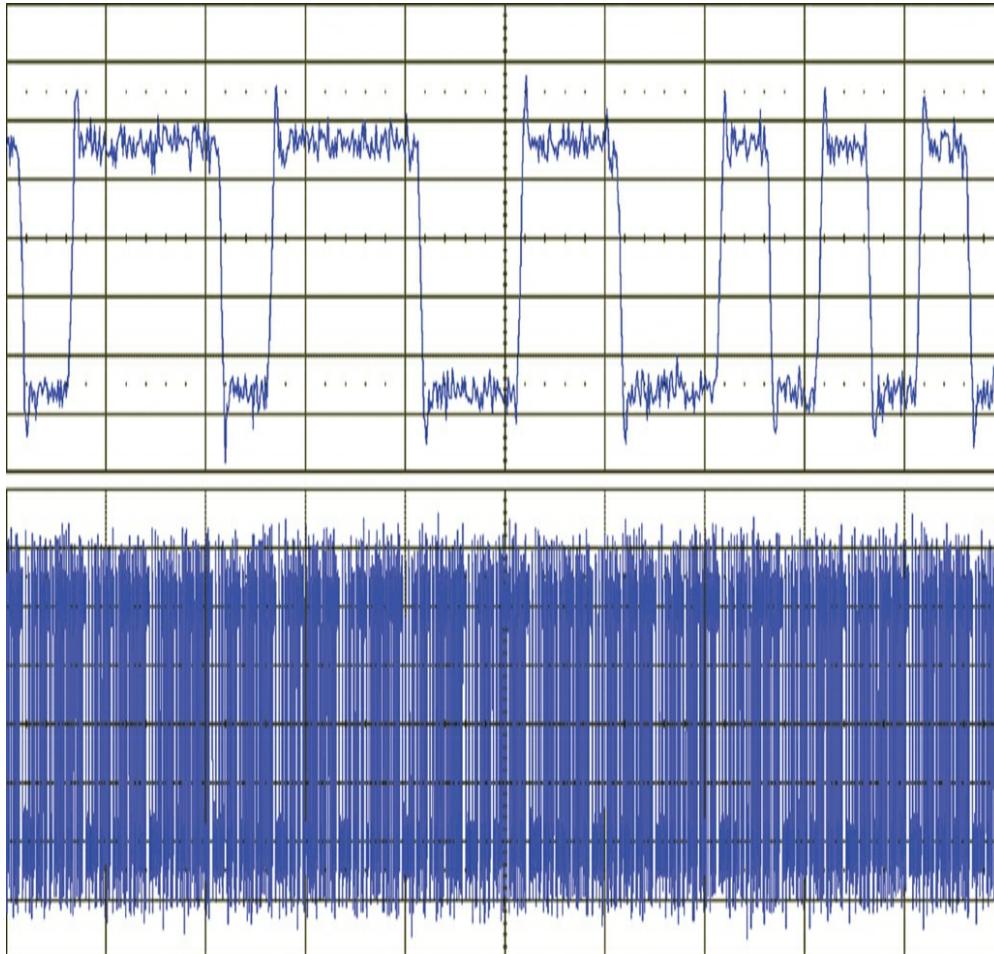
The term *vector* in vector network analyzer refers to the feature that the instrument measures the phase of the waves as well as the amplitudes. To do this, it must separate the incident and reflected signals, both propagating in the same interconnect, though in opposite directions [1].

The source impedance of a network analyzer is typically  $50 \Omega$ . A calibration is usually performed to the end of the coax cable connected to it. VNAs have been in use for more than 50 years and a detailed formalism has been developed to describe what they measure.

The connections between the VNA and DUT are referred to as *ports*. The electronics of the VNA transmit a sine wave to each port and simultaneously measure any sine wave traveling back from the DUT into the VNA port. The impedance of each port as seen by the DUT is calibrated to be a precision  $50 \Omega$ . This includes the source termination and the precision coax cable.

Being able to distinguish between the waves traveling out of and into the VNA is different from a common oscilloscope, which just measures the voltage between two adjacent conductors. It cannot distinguish the direction of propagation of the measured voltages. Figure 3.6 shows the measured voltage between a signal

and return conductor in a functioning circuit board. This snapshot of the transient voltage between these terminals on the board has no information about the direction in which the signals are traveling on the interconnect.



**Figure 3.6** Example of the measured voltage between two conductors in a functioning circuit. It provides no information about the direction these signals are traveling.

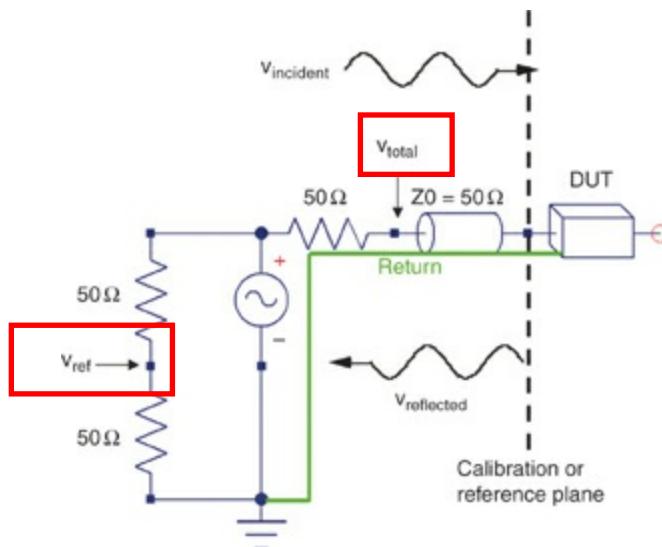
If your training as an engineer has only exposed you to using scopes to view signals, you have not been able to see that the voltages are really propagating. Many scope signals are the combination of two waves propagating in opposite directions and are measured simultaneously as the total voltage at the probed location. This is especially true if the probed point is in the middle of an interconnect.

### Tip

An oscilloscope only measures the total voltage between a signal and return path, not the direction of propagation of the signals. Further analysis must be used to interpret the voltage signals on a scope and sort out the signals propagating in each direction on the interconnect.

A VNA is designed to separately measure the amplitude and phase of the waves propagating in the two directions at each port.

A sine wave can come out of any VNA port. A portion of the sine wave enters a DUT and another portion scatters off the DUT propagating back to the source. The VNA measures the incident wave coming out of the VNA into the DUT and the scattered wave propagating back from the DUT. The ratio of the sine wave scattered back from the DUT to the wave going into the DUT is called a Scattering parameter, or *S-parameter* for short. [Figure 3.7](#) shows a schematic representation of one port of a VNA. This is also the same SPICE circuit that is used to simulate a VNA measurement.



**Figure 3.7** Schematic of a VNA port showing the sine wave generator, the  $50\Omega$  source impedance, and the internal electronics that measure the reflected amplitude and phase. The reference plane is the boundary of the port. Shown explicitly is the return path for the port and the input to the DUT.

In this circuit, the source creates a sine wave. This voltage passes through a precision  $50 \Omega$  resistor into a precision  $50 \Omega$  coax cable where it propagates. We know exactly what the incident voltage is that begins to propagate into the  $50 \Omega$  cable. It is exactly half the voltage from the sine wave source because it is based on the voltage divider of the  $50 \Omega$  series resistance and the  $50 \Omega$  transmission line.

In practice, we measure this incident voltage indirectly by measuring the voltage across another voltage divider labeled in the circuit shown in Figure 3.7 as  $V_{ref}$ . This voltage is exactly the same as the incident voltage propagating out of the VNA from the transmission line coming out of port 1. This is the wave that is incident into the DUT.

Due to the impedance change looking into the DUT compared to the  $50 \Omega$  source impedance of the port, a net reflected wave propagates back into the VNA. This single net wave, which might be the superposition of multiple sine waves all propagating back to the VNA, will pass by the internal measurement point labeled as  $V_{total}$ . We measure the magnitude and phase of the total voltage at this point with a sophisticated, precision voltmeter.

Like any oscilloscope, the voltmeter at this location cannot separate the incident voltage wave propagating from left to right from the reflected voltage wave propagating from right to left, both in the same coax cable. Only the total voltage is measured. The total voltage is the sum of  $V_{incident} + V_{reflected}$ . Because  $V_{incident}$  is measured independently in the pure resistive voltage divider, we can easily extract the reflected voltage from

$$V_{reflected} = V_{total} - V_{ref} \quad (3.5)$$

Any reflected wave that propagates back into port 1 of

the VNA will be terminated by the  $50 \Omega$  source resistor and will never go back to the DUT.

We calculate the reflection coefficient from the measured  $V_{\text{total}}$  and  $V_{\text{ref}}$ , which is equivalent to  $V_{\text{incident}}$ . Because the phase of both waves is also measured, the reflection coefficient is complex.

S-parameters of a DUT consist of every combination of the ratio of the sine wave coming out from each DUT port to the sine wave going into each DUT port. To keep track of all the combinations of signals coming out and going in the ports of the DUT, each port is labeled by an index number and subscripts on each S-parameter are used to identify the coming out port and the going in port.

The definition of an S-parameter is

$$S_{jk} = \frac{\text{sine wave out from port } j}{\text{sine wave into port } k} \quad (3.6)$$

The reflection coefficient  $S_{11}$  is the ratio of the reflected signal from port 1 to the incident signal going into port 1. This S-parameter is often referred to as the *return loss*. The *insertion loss* is the magnitude of the ratio of the sine wave coming out of port 2 of the DUT to the sine wave going into port 1 of the DUT. Insertion loss is the magnitude of  $S_{21}$ , usually in units of dB.

**Tip**

S-parameters have become the de facto standard to describe the high-frequency properties of interconnects. Effort spent understanding S-parameters is well worth the investment.

In the formalism of S-parameters,  $S_{11}$  is exactly the same as the reflection coefficient. Because the source impedance of the port of a VNA is a precision  $50 \Omega$ , the reflected S-parameter,  $S_{11}$ , is related to the DUT input

impedance as

$$S_{11} = \frac{Z_{\text{DUT}} - 50}{Z_{\text{DUT}} + 50} \quad (3.7)$$

After we apply a little algebra and rearrange the terms, the input impedance of the DUT based on the definition of the reflected signal is

$$Z_{\text{DUT}} = 50\Omega \frac{1+S_{11}}{1-S_{11}} \quad (3.8)$$

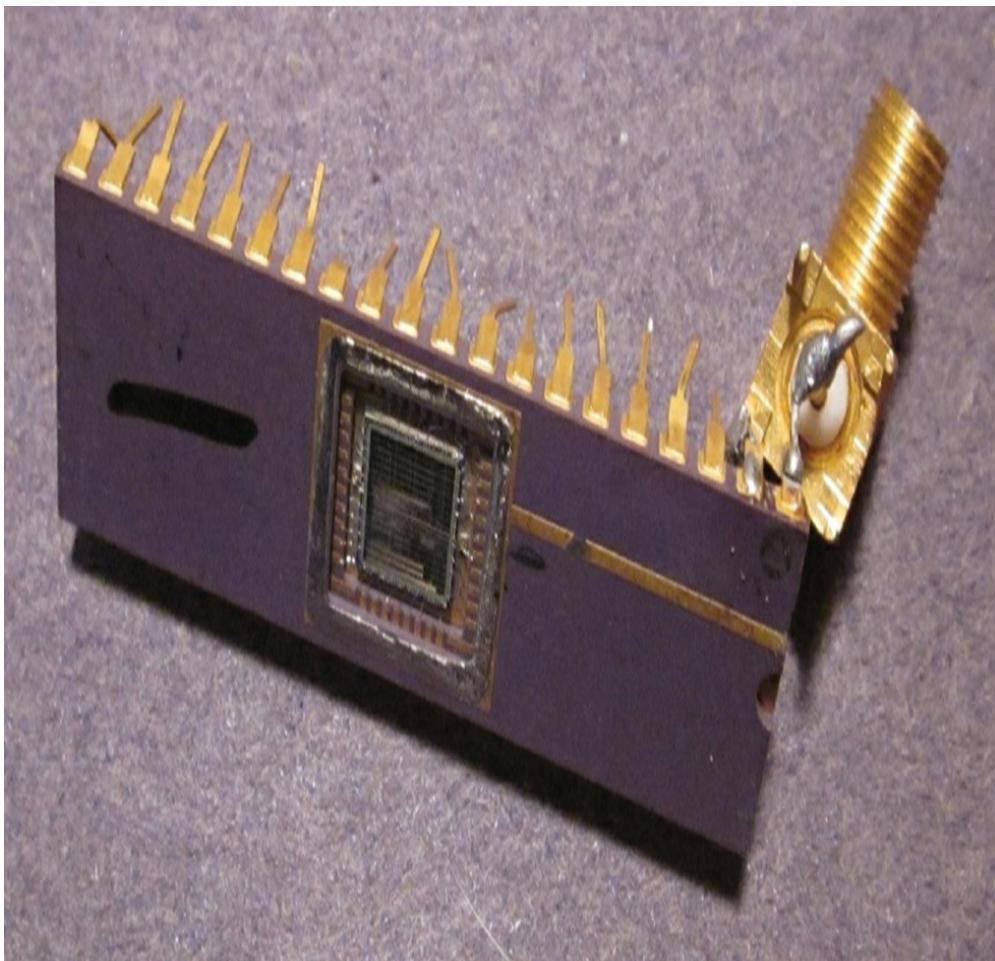
This is the basis for measuring the impedance of any DUT to as high a frequency as the VNA is capable, which may be above 50 GHz. A little algebra converts the measured, complex  $S_{11}$  into the complex impedance.

**Tip**

An alternative definition of the input impedance of a device under test (DUT) is based on  $S_{11}$ . No assumptions or models are used to convert the  $S_{11}$  of a device into the input impedance, just a little complex algebra. This alternative definition of impedance is completely equivalent to the V/I definition of impedance in the frequency domain. It just opens up new ways of measuring impedance.

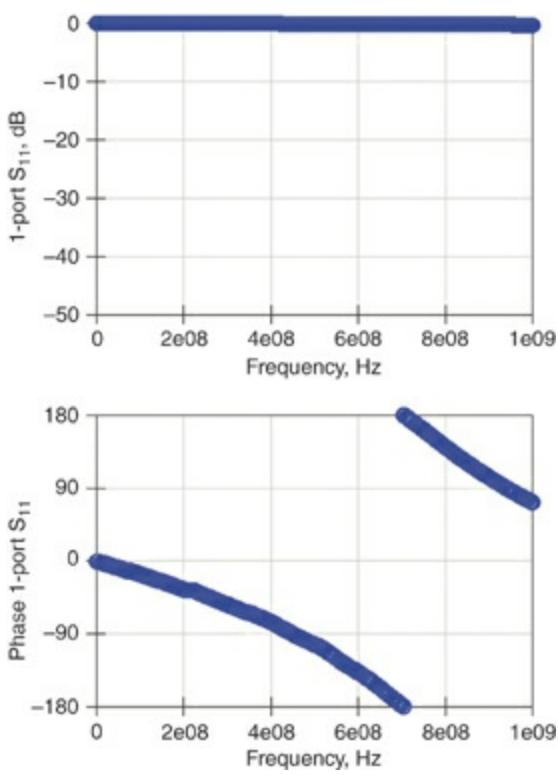
### 3.5 EXAMPLE: MEASURING THE IMPEDANCE OF TWO LEADS IN A DIP

To show an example of using a VNA to measure impedance, we soldered an old-style ceramic DIP (dual in-line package) to an SMA (SubMiniture version A) connector as the fixture to interface to a VNA. This test structure is shown in [Figure 3.8](#). We chose two adjacent leads as the signal and return connections.



**Figure 3.8** A simple ceramic DIP as a DUT using two adjacent leads as a signal and return path, soldered to an SMA fixture.

The VNA sends a sine wave into the pair of leads. It measures the reflected sine wave at each frequency stepped through by the VNA. The S-parameter  $S_{11}$  is measured at each VNA frequency. Figure 3.9 shows the measured  $S_{11}$  from this DUT. The bonding shelf of the package is open and the pins are not connected to anything for this measurement. The input impedance seen looking into the SMA connector is initially open at low frequency.



**Figure 3.9** Measured S<sub>11</sub> of a ceramic DIP looking into a pair of adjacent leads.

We convert the measured S<sub>11</sub> values over the entire range of the measurement from 10 MHz to 1 GHz into the input impedance using complex algebra, frequency by frequency. We calculate the input impedance from

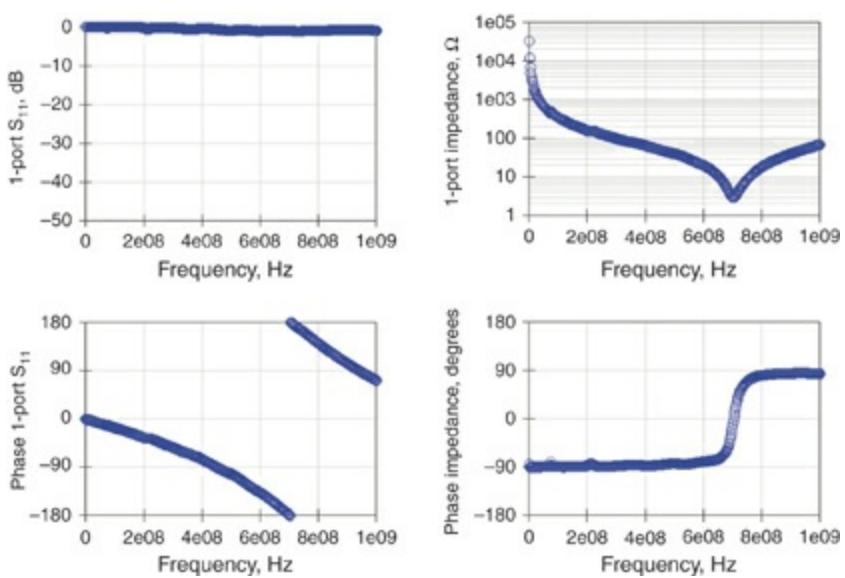
$$Z_{DUT}(f) = 50\Omega \frac{1 + S_{11}(f)}{1 - S_{11}(f)} \quad (3.9)$$

where

Z<sub>DUT</sub>(f) = the complex input impedance of the DUT at each frequency

S<sub>11</sub>(f) = the complex measured S-parameter at each frequency

We can perform these calculations in any SPICE simulation tool and even in Excel. Figure 3.10 shows the comparison between the measured S<sub>11</sub> and the converted input impedance.



**Figure 3.10** Measured  $S_{11}$  and converted input impedance, for the ceramic DIP example on a linear frequency scale from 10 MHz to 1 GHz.

Note that the magnitude and phase of the extracted impedance at each frequency is directly related to the magnitude and phase of  $S_{11}$  at that same frequency, but in a very complicated way. Looking at the phase of  $S_{11}$ , for example, and predicting the phase of the input impedance is exceedingly difficult. Note that because the magnitude of  $S_{11}$  is virtually constant at 0 dB, all the impedance information is really contained in the phase of  $S_{11}$ .

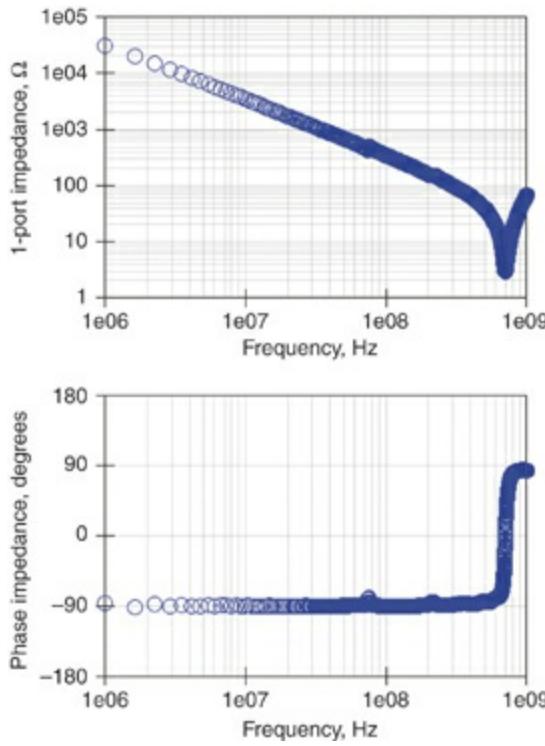
#### Tip

Even though the return loss and the impedance are both complex numbers each with a magnitude and phase, the phase of the return loss and the phase of the impedance are not in any way the same. The phase of the impedance arises from a complicated combination of the magnitude and phase of the return loss at each frequency. Do not confuse the phase of the  $S_{11}$  with the phase of the impedance.

Whenever we view an impedance over frequency plot, interpreting the data is almost always easier by plotting both the impedance and frequency on a log-log scale. The impedance of an ideal capacitor is a straight line with slope of  $-1$  and an ideal inductor is a straight line

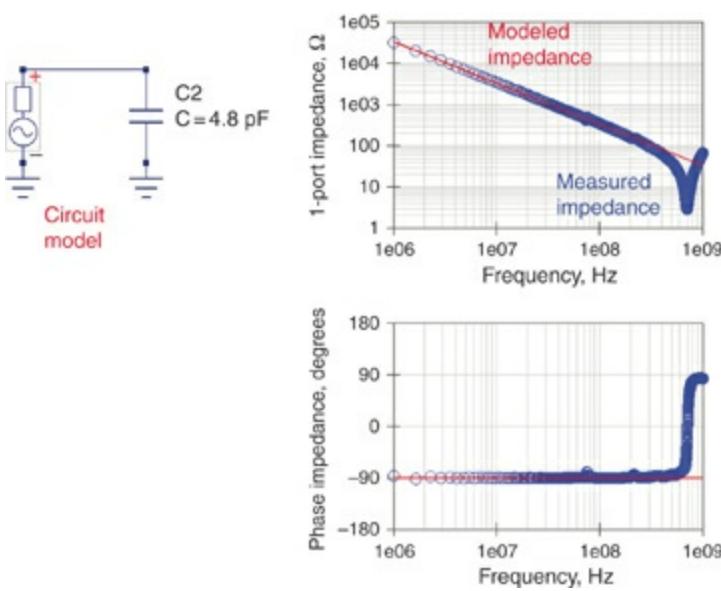
with a slope of +1 on log-log scales.

An impedance plot reveals capacitive and inductive natures at a glance on a log-log scale. Figure 3.11 shows the measured impedance on a log-log plot for the magnitude and linear-log plot for the phase.



**Figure 3.11** Measured package lead impedance on a log-log scale.

It's obvious in this impedance plot that the package leads look capacitive at low frequency, and then around 800 MHz, switch to look inductive. This initial behavior offers a clue on how to model the package leads as a simple capacitor at low frequency. In a simulation environment such as QUCS or Keysight's Advanced Design System (ADS), we can compare the measured impedance data with the predicted impedance of a simple model. The simplest model to use is a single ideal capacitor. Figure 3.12 compares the measured impedance with the simulated impedance of a 4.8 pF capacitor.



**Figure 3.12** Comparison of simple capacitor model and measured impedance of two leads in a ceramic DIP.

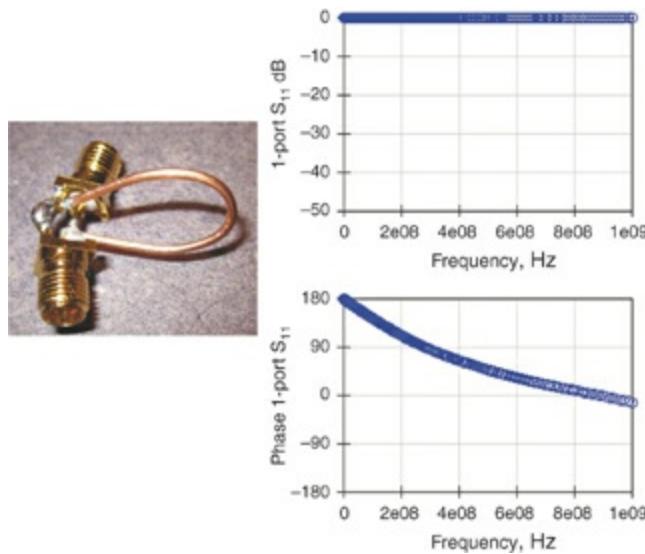
Using a VNA, we can measure the impedance of any DUT from the return loss and bring it into a simulation environment for further analysis. This process of taking the measured S-parameters of a DUT and fitting an ideal circuit topology-based model to extract the model parameters is sometimes referred to as *measurement-based modeling*. It is also sometimes referred to as *hacking the interconnect*.

In effect, we are looking “under the hood” to develop a scalable model that describes the measurements of the interconnect, which we can then modify or “hack” to explore what-if questions. This is a powerful technique to identify the root cause of interconnect behavior.

### 3.6 EXAMPLE: MEASURING THE IMPEDANCE OF A SMALL WIRE LOOP

We can apply this technique of using a VNA to measure the high-frequency impedance of any DUT to a variety of components. Figure 3.13 shows a small wire loop about 1 inch in diameter measured with a one-port VNA, together with the measured  $S_{11}$  magnitude and phase. The wire loop is connected between the signal and reference terminals of the VNA port. Only one of the

two connectors is attached to the VNA port for this measurement.



**Figure 3.13** Measured return loss of 1-inch diameter copper loop. Although two SMAs are soldered to the end of the loop, only one of them was connected to the VNA.

Using the definition of the impedance in terms of the return loss, we can extract the measured impedance of this wire loop. As an engineer, keeping Bogatin's Rule #9 in mind is important.

**Tip**

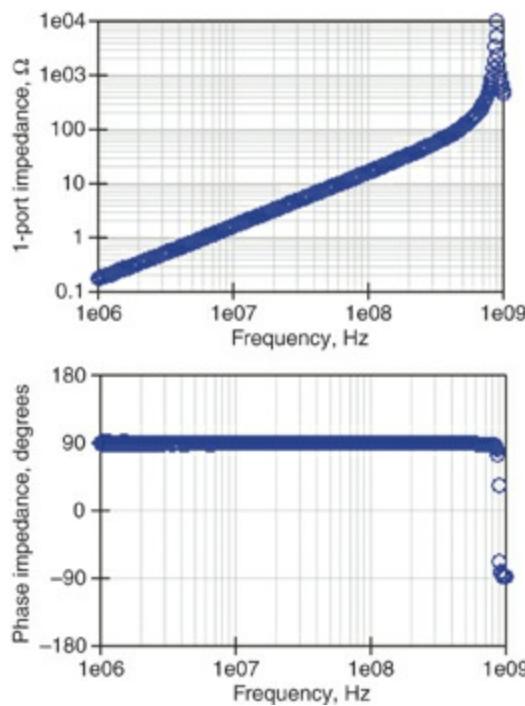
Always remember Bogatin's Rule #9: "Never perform a measurement or simulation without first anticipating the result. If you find something unexpected, either your intuition is wrong or something is wrong about how you think the measurement or simulation is set up. Either way, investigating the difference will be important. On the other hand, if you see what you expect, then you get a nice warm feeling in knowing that you are beginning to understand the real world. It is an important confidence builder."

Before converting the measured return loss into the impedance, anticipate what to expect. We would expect this loop to look like an inductor at low frequency. At frequencies where the physical dimensions are on the order of 1/10 of a wavelength, the model should break down. For the roughly 1-inch diameter loop, with a circumference of about 3 inches, the frequency when

this is 1/10 of a wavelength is

$$f = \frac{c}{\lambda} = \frac{12 \text{ in/sec}}{10 \times 3 \text{ in}} = 0.4 \text{ GHz} \quad (3.10)$$

At frequencies below 400 MHz, the impedance of this loop should look like an inductor. The impedance should start out low and increase with frequency. Likewise, the resistance should be very low and maybe increase with frequency slightly due to skin depth. Figure 3.14 is the measured impedance extracted from the return loss of this copper loop.



**Figure 3.14** Measured impedance converted from the measured return loss for the copper loop.

The measured impedance looks like an ideal inductor. If we assume the model for this structure is an ideal inductor in series with an ideal resistor, we would predict the impedance to be

$$Z = R + j\omega L \quad (3.11)$$

where

$Z$  = the impedance of the DUT

$R$  = the series resistance of the copper loop

$$\omega = 2\pi \times \text{frequency}$$

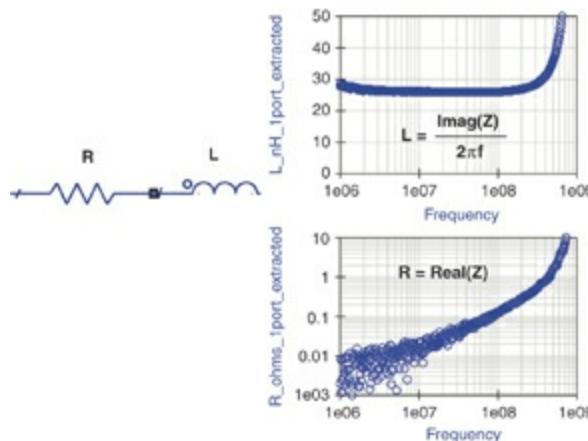
$L$  = the loop inductance

We extract the values of the  $R$  and  $L$  at each frequency from the real and imaginary components of the impedance as

$$R = \text{real}(Z) \quad (3.12)$$

$$L = \frac{\text{imag}(Z)}{\omega} \quad (3.13)$$

We extract these terms from the measured impedance at each frequency using simple algebra. [Figure 3.15](#) shows the values of the  $R$  and  $L$  for this copper loop.



**Figure 3.15** Extracted  $R$  and  $L$  values for this copper loop measured with a one-port network analyzer.

At frequencies above about 400 MHz we see the inductance begin to dramatically increase as we expected from distributed effects. Three questions immediately arise when we look at this data:

1. How much of this inductance is the loop and how much is from the uncalibrated SMA fixture?
2. Is the resistance increasing with frequency due to skin depth effects?
3. Why is the data so noisy below about  $0.1 \Omega$ ?

Although a one-port VNA is a powerful tool for measuring the impedance of a DUT to high frequency, it

has some limitations and introduces artifacts when applied to measuring low impedance.

### 3.7 LIMITATIONS OF VNA IMPEDANCE MEASUREMENTS AT LOW FREQUENCY

The first practical problem in using a VNA to measure low impedance is related to the signal-to-noise ratio of the reflected signal. If the impedance of the DUT is  $1\ \Omega$ , the magnitude of  $S_{11}$  is

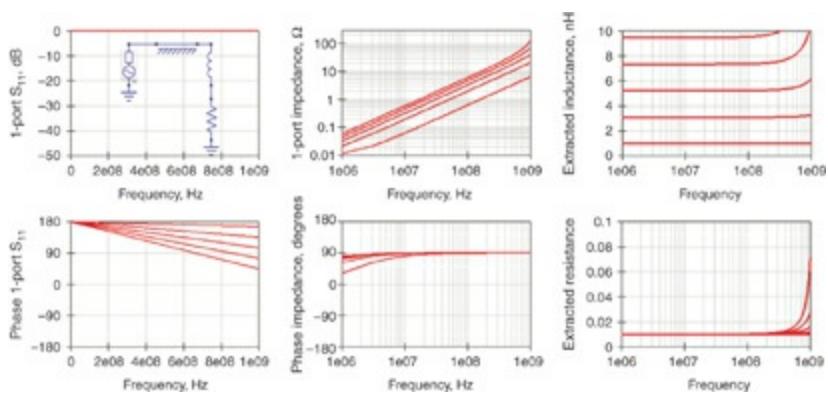
$$S_{11} = \frac{1 - 50}{1 + 50} = \frac{-49}{51} = -0.96 \quad (3.14)$$

Though this is only about 4% greater than  $-1$ , it is an easy value for a typical VNA to distinguish from  $-1$ . But suppose the input impedance of the DUT is  $0.1\ \Omega$ . The reflection coefficient will be

$$S_{11} = \frac{0.1 - 50}{0.1 + 50} = \frac{-49.9}{50.1} = -0.996 \quad (3.15)$$

Measuring the reflected signal as  $-0.996$  rather than  $-1$  is a challenge and will be sensitive to a small amount of noise. In dB, this is  $-0.035$  dB, a very tiny amount of dB, often times in the reproducibility noise limit of a calibration process. Even so, the resistance measurement at  $0.1\ \Omega$  is pretty consistent. The  $S_{11}$  measurement has really fallen apart when the resistance is below  $0.1\ \Omega$ .

The second problem is an artifact from the fixture connecting to the DUT. Even if a perfect lossless transmission line is used to connect the calibrated ends of the VNA to the end of the DUT of interest, the phase delay of the transmission line fixture will add an artifact to the measured phase and distort the extracted impedance. We can easily simulate this with a simple circuit, as shown in Figure 3.16.



**Figure 3.16** Simulated  $S_{11}$  of an ideal RL circuit with a series transmission line acting as a fixture. Four different transmission line lengths from 0 to 1 inch have a dramatic effect on the extracted impedance and L and R values. The circuit model of the fixture plus the DUT is shown in the upper left-hand panel.

In this example, we increased the length of the transmission line from 0 to 1 inch with 0.25-inch increments. The ideal R was  $0.01 \Omega$  and the ideal L was  $1 \text{ nH}$ . An artificial phase is added to  $S_{11}$  when the length of the fixture increases as modeled by the ideal transmission line. This ripples down to impact the phase of the impedance, affecting both the extracted inductance and the resistance. The extracted inductance increases with fixture length and begins to show frequency dependence at the high-frequency end. The series resistance also appears to have frequency dependence to it.

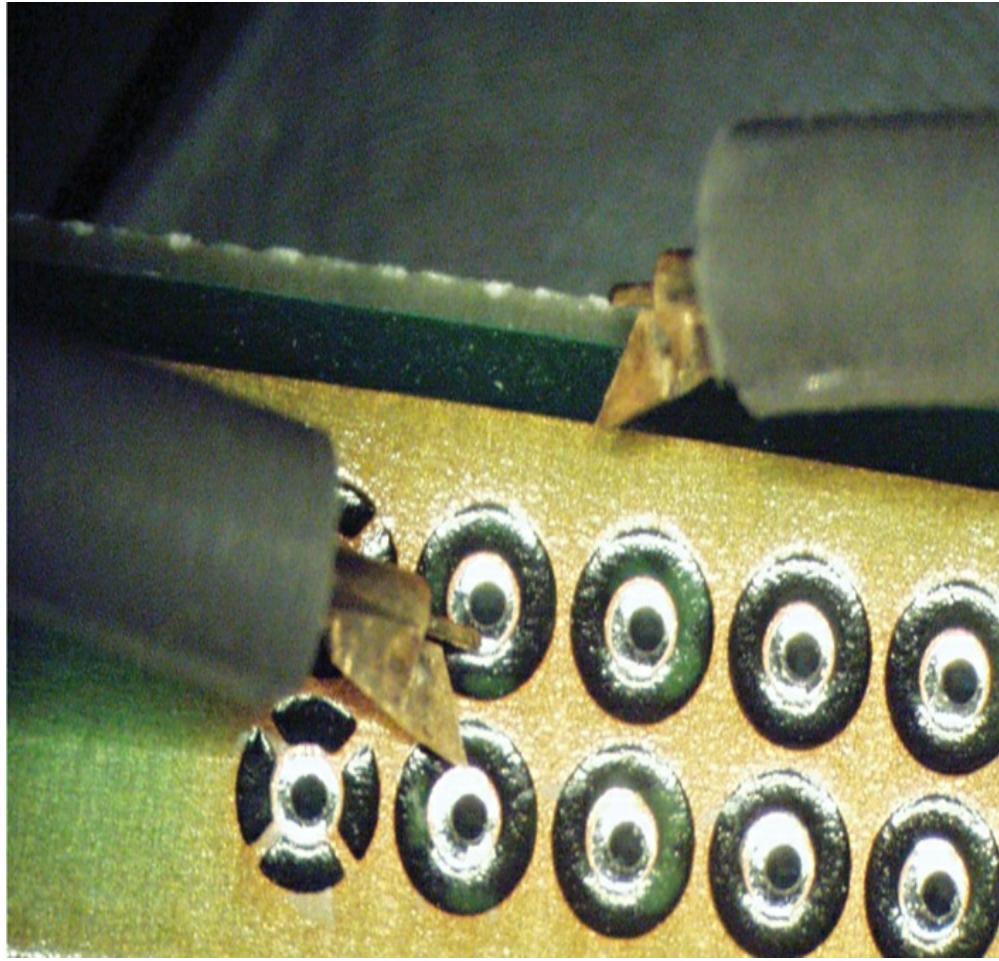
The one-port VNA measurement is viewing not just the DUT but also the fixture. The higher extracted inductance is due to the additional series inductance in the transmission line fixture.

This means that when performing a one-port impedance measurement, accurately separating the inductance of the DUT from the inductance of the total measurement is impossible. Even short fixtures of a fraction of an inch will swamp low inductance DUT measurements. If the fixture properties are accurately known, the possibility exists to “de-embed” the DUT

from the fixture plus DUT measurement. However, the larger the contribution from the fixture, the more difficult is the de-embedding process.

This suggests that the way to perform one-port impedance measurements is to use a minimum-length fixture such as a microprobe, which is calibrated to the probe tip.

Figure 3.17 shows an example of a microprobe probing the pads of a simple via structure.



**Figure 3.17** Close-up of a microprobe probing the pads of a via pair. The VNA is calibrated right to the tips of the microprobe. Photo courtesy of GigaTest Labs.

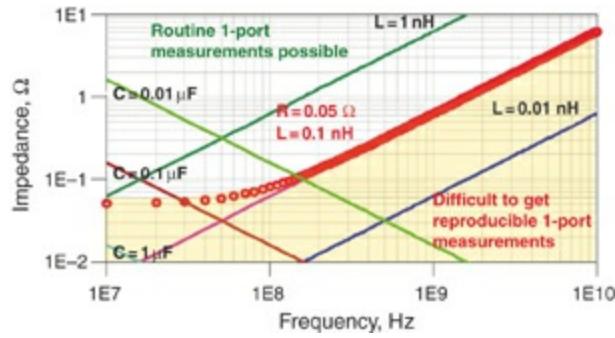
The VNA is calibrated right to the ends of the probe tip, effectively eliminating any fixture length in the measurement. Although this dramatically reduces the fixture artifact from the measurement, it introduces contact resistance.

The third problem with one-port impedance measurements is the contact impedance of the probe. The contact of the probe to the DUT is a “dry” contact. Depending on the metallization, this can vary from  $0.05 \Omega$  for gold-to-gold contacts and up to  $2 \Omega$  for an oxidized solder or copper pad surface.

Even though the probe features are calibrated out of the measurement, small changes in the distortion of the probe tip or where it comes down to probe the DUT will affect the residual loop inductance of the probe tip that has been calibrated out.

For example, the typical inductance of a small loop is about  $20 \text{ pH/mil}$  of length. If the probe distorts or scrubs along the pad only 5 mils, the probe tip’s residual loop inductance will change by as much as  $5 \text{ mils} \times 20 \text{ pH/mil} = 100 \text{ pH}$  over and above what may have been calibrated out.

For most microprobe tips, the noise floor for an impedance measurement is limited to about  $0.05 \Omega$  and  $0.1 \text{ nH}$  in the best case. [Figure 3.18](#) maps out this impedance range.



**Figure 3.18** Range of reproducible probe measurements identified as the circles corresponding to an  $R = 0.05 \Omega$  and  $L = 0.1 \text{ nH}$ .

The reproducibility of the probe contact impedance sets the fundamental floor for a one-port VNA impedance measurement. Above 100 MHz, this limits capacitance measurements to  $< 0.01 \mu\text{F}$  and inductance

measurements to  $> 0.1$  nH. This is a significant limitation for PDN component characterization because on-die capacitance can be  $0.001\ \mu\text{F}$  and a via inductance can be  $0.01\ \text{nH}$ .

This is also a limitation for physical one-port measurements in a lab with real probes. The simulated  $S_{11}$  can still be used to extract the input impedance of a DUT even for very low impedances if it includes only the DUT without any fixture.

**Tip**

A one-port VNA measurement can be converted to impedance, but for impedances below about  $0.1\ \Omega$ , three artifacts—including S/N ratio, fixture transmission line phase, and contact resistance—contribute to incorrect interpretation of the measured values. A different technique is needed for typical PDN impedance measurements.

Making PDN measurements, which are typically very low impedance, requires a different technique. The two-port VNA technique derives from the four-point Kelvin low resistance measurement method and exceeds the limitations of the one-port VNA technique.

### **3.8 THE FOUR-POINT KELVIN RESISTANCE MEASUREMENT TECHNIQUE**

Contact resistance arises whenever two metals are brought into dry contact. A series resistance exists at the interface between any two metal surfaces. In the absence of oxide or intermetallic layers, contact resistance is created due to the very tiny area where two surfaces actually touch. The current constricts in passing through this narrow contact region, increasing the resistance. We generally call this sort of resistance *constricting or spreading resistance*. It decreases as the actual contact area increases, such as when the contact pressure increases. In gold-to-gold surfaces, the contact

resistance is on the order of  $20\text{ m}\Omega$  for a 100 gram weight of force.

In the presence of oxides, this contact resistance can dramatically increase to more than  $100\text{ m}\Omega$ . In the case of solder, aluminum and copper surfaces that readily oxidize, the contact resistance can be as high as  $2\text{ }\Omega$  or more.

Contact resistance plays a dominant role in measuring series resistance of a conductor structure with resistances less than  $1\text{ }\Omega$ . The way around this artifact is by using a technique originally developed by William Thomson, a brilliant physicist whose career spanned more than 50 years until his death in 1907.

Thompson was a professor of natural philosophy at the University of Glasgow, Scotland. Among his early accomplishments was the analysis of the first transatlantic cable, for which he invented the concept of transmission lines. He was first to derive and introduce the Telegrapher's Equations. For his efforts in fixing the transatlantic cable, he was given a knighthood and early on became known as Sir William Thomson.

He was the first UK scientist appointed by the Queen of England to the House of Lords and took on the title of Lord Kelvin in honor of the River Kelvin, which ran near his university. Since then he has been known as Lord Kelvin. The Kelvin temperature scale is named after him, in tribute to his discovery of a limit to the lowest temperature possible.

Among his other investigations in electricity, he developed a simple technique to overcome contact resistance and measure the low intrinsic resistance of metal conductors.

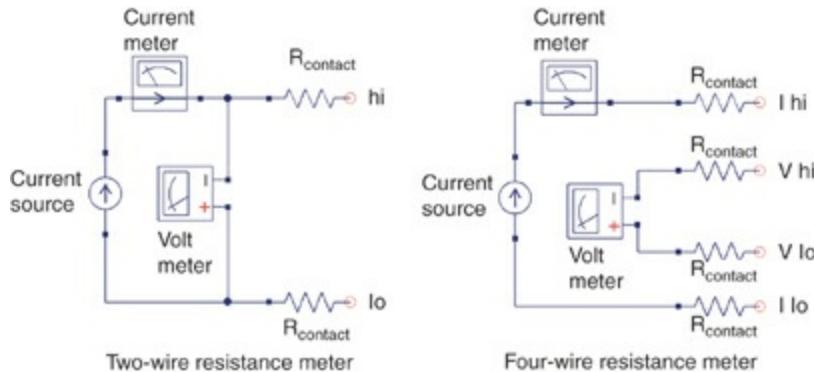
In traditional two-wire resistance measurements, a current source forces some current through the leads in

contact with the DUT. The current through the leads,  $I$ , and the voltage drop across the leads,  $V$ , are measured. The impedance of the DUT is calculated as the ratio of  $V/I$ . In series with the two leads that contact the DUT is the series contact resistance of the leads. This approach is usually referred to as a two-wire measurement.

#### Tip

In conventional two-wire resistance measurements, the same two leads that force the current are also used to measure the voltage. This means that what is really measured are the resistance of the DUT plus the series contact resistances. Lord Kelvin found a way around this problem.

In Lord Kelvin's approach, the voltage leads are separated from the current leads to make their own contact to the DUT. Four leads connect to the DUT. This technique is usually referred to as a four-wire or Kelvin measurement. The current through the device is still measured, which also flows through the series contact resistance, but in the Kelvin technique, independent leads measure the voltage across the DUT. Although there is contact resistance in the voltage leads, the voltmeter is usually such a high impedance that the contact resistance does not affect the voltage measurement. [Figure 3.19](#) outlines these two configurations.



**Figure 3.19** Configuration of traditional two-wire resistance measurement and the Kelvin four-wire method.

The essence of the Kelvin technique is to use independent leads for the current measurement and the voltage measurement. This is the basis of measuring both low impedance at DC and low impedance at high frequency.

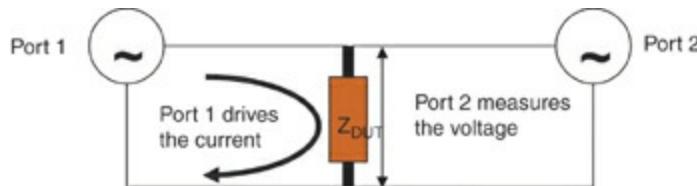
**Tip**

To get around the contact resistance (or impedance) effects, two separated leads force the current and two additional leads measure the voltage. This separates the impedance of the DUT from the impedance of the fixture connected to it.

### 3.9 THE TWO-PORT LOW IMPEDANCE MEASUREMENT TECHNIQUE

As illustrated early in this chapter, we can measure impedance using a one-port network analyzer. Even though it is one-port, really two wires connect to the DUT: the signal conductor and the return conductor. This technique is sensitive to contact impedance in the probes and fixture and is only accurate for impedances above the  $0.1 \Omega$  level. Overcoming this limitation is possible if two ports of the VNA are used [2].

In the two-port technique, one port drives a current loop into the DUT. This generates a voltage drop across the DUT. The second port measures the voltage generated across the DUT. Two independent contacts are required to the DUT so that the contact paths are *not* shared by the two probes. Figure 3.20 shows an illustration of the two-port technique.



**Figure 3.20** Illustration of a two-port low impedance VNA measurement with both ports connected independently to the same two terminal DUT.

Looking in from port 1 we see the low impedance of the DUT with the  $50 \Omega$  of port 2 in parallel. The DUT shunting port 2 dominates if it is a much lower impedance than port 2. This is the usual case with PDN DUT measurements. When the incident signal from port 1 encounters the DUT, it sees a very low impedance and the reflection coefficient is nearly  $-1$ .

A positive going signal  $V_{\text{incident}}$  approaches the DUT with a current loop circulating in the clockwise direction, propagating down the  $50 \Omega$  cable. The magnitude of the incident current loop is  $V_{\text{incident}}/50 \Omega$ . A negative going signal  $V_{\text{reflected}}$  comes back from the DUT with a current loop propagating toward port 1, also circulating in the clockwise direction. The magnitude of the current loop of the reflected signal is  $V_{\text{reflected}}/50 \Omega$ . The net current through the DUT is the sum of these two current loops at the DUT.

When the impedance of the DUT is very low, the reflection coefficient is nearly  $-1$ . The magnitude of the reflected voltage is the same as that of the incident voltage but opposite polarity (180-degree phase change). The reflected current loop circulating in the clockwise direction is the same magnitude as the incident current loop. The net current loop through the DUT is the sum of the incident and reflected current loops, both circulating in the clockwise direction. The voltage at the DUT essentially drops to zero and the net current through the DUT is twice the incident current when the DUT is much less than  $50 \Omega$  impedance. This is the expected behavior of a shorted transmission line.

The net current generates a small voltage across the DUT determined by its impedance times twice the current out of port 1. This small voltage across the DUT is launched into the right-hand transmission line and propagates to port 2 where the receiver of port 2

measures it. The definition of  $S_{21}$  is the ratio of the voltage out of port 2 of the DUT divided by the incident voltage into port 1 of the DUT. This is given by

$$S_{21} = \frac{V_{\text{transmitted}}}{V_{\text{incident}}} = \frac{Z_{\text{DUT}} \times 2 \times \frac{V_{\text{incident}}}{50 \Omega}}{V_{\text{incident}}} = \frac{Z_{\text{DUT}}}{25 \Omega} \quad (3.16)$$

Remarkably, the measured  $S_{21}$  is simply the impedance of the DUT divided by  $25 \Omega$  when the impedance of the DUT is very low. This is based on  $50 \Omega$  port impedances. A measure of  $S_{21}$  is a direct measure of the impedance of the DUT. We get the impedance of the DUT simply by

$$Z_{\text{DUT}} = 25 \Omega \times S_{21} \quad (3.17)$$

**Tip**

In the two-port measurement the DUT impedance magnitude is directly proportional to the  $S_{21}$  value when the impedance of the DUT is very small. The phase of  $S_{21}$  is the same as the phase of the impedance. This is a remarkably simple relationship.

Note that  $S_{21}$  is expressed as a complex number, not as dB. To get the impedance when  $S_{21}$  is expressed in dB we first convert it into a magnitude then scale it. We convert the magnitude of  $S_{21}$  in dB to impedance by

$$Z_{\text{DUT}} = 25 \Omega \times S_{21} = 25 \Omega \times 10^{\frac{S_{21}(\text{dB})}{20}} \quad (3.18)$$

For example, if the  $S_{21}$  measurement is  $-20$  dB, the impedance in  $\Omega$  is  $Z = 25 \times 10^{(-20/20)} = 2.5 \Omega$ . When  $S_{21}$  is  $-40$  dB, the impedance is  $0.25 \Omega$ . When  $S_{21}$  is  $-60$  dB the impedance is  $25 \text{ m}\Omega$ . The full dynamic range of a VNA is required to measure impedances in the  $\text{m}\Omega$  range. The preceding formula is a first-order approximation and should not be used if  $S_{21}$  is larger than about  $-20$  dB, which would mean that the DUT

violates the assumption that it is much less than  $50\ \Omega$ .

We can also express impedance in dB because the dB scale just represents the log of the ratio of two quantities, which are powers. Two sources of confusion are “What do we take as the reference value?” and “Do we consider an impedance as a voltage or a power?”

When impedance is reported in dB, it behaves like an amplitude or magnitude rather than a power because it is directly proportional to one of the S-parameters, which by definition is a magnitude. This means that when converting impedance in dB back into impedance in Ohms we use a factor of 20 *not* 10:

$$Z[\text{dB}] = 20 \times \log\left(\frac{Z[\Omega]}{1\Omega}\right) \quad \text{and} \quad Z[\Omega] = 10^{\frac{Z[\text{dB}]}{20}} \quad (3.19)$$

where

$Z[\text{dB}]$  is the impedance in dB

$Z[\Omega]$  is the impedance in  $\Omega$

By convention, when we describe an impedance in dB we use  $1\ \Omega$  as the reference value. When we use  $1\ \text{mW}$  as the reference scale for measuring power, we identify the units as dBm to identify the reference as  $1\ \text{mW}$ . Likewise, dBu is a dB scale with the reference to which other powers are compared, as  $1\ \mu\text{W}$ .

In the same way, we identify the  $\Omega$  values in dB using the units of  $\text{dB}\Omega$ . Using this scale would certainly reduce the confusion but, unfortunately, the industry has not adopted this convention. Instead we just refer to impedance in dB.

**Tip**

If you want to minimize the confusion when you see impedance measured in dB, think of the units as  $\text{dB}\Omega$  and remember that impedance behaves like an amplitude.

For example,

0 dB of impedance is  $1 \Omega$

-20 dB of impedance is  $0.1 \Omega$

-60 dB of impedance is  $1 \text{ m}\Omega$

When  $S_{21}$  is described in terms of dB and the first-order approximation applies, the impedance of the DUT also described in dB is approximately

$$Z_{\text{DUT}}[\text{dB}] = (25\Omega)_{\text{in dB}} + S_{21}[\text{dB}] = 28\text{dB} + S_{21}[\text{dB}] \quad (3.20)$$

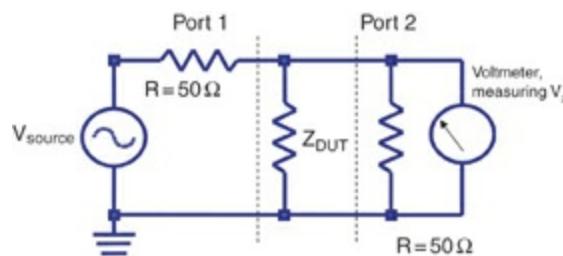
where

$$28 \text{ dB} = 20 \times \log(25\Omega)$$

If the measured  $S_{21}$  is -40 dB, the value of the impedance in dB is  $28 \text{ dB} + -40 \text{ dB} = -12 \text{ dB}$ . The value of the impedance in  $\Omega$  is  $10^{(-12 \text{ dB}/20)} = 0.25 \Omega$ .

If the measured  $S_{21}$  is -60 dB, the value of the impedance in dB is  $28 \text{ dB} + -60 \text{ dB} = -32 \text{ dB}$ . The value of the impedance in  $\Omega$  is  $10^{(-32 \text{ dB}/20)} = 0.025 \Omega$ .

Returning to the discussion on impedance and  $S_{21}$ , the simple formula that  $Z = 25 \Omega \times S_{21}$  is based on the assumption that the impedance of the DUT is very low. The general case without this assumption is derived with a little more algebra and applies for any DUT impedance. Figure 3.21 shows the circuit for impedance extraction. It is essentially the VNA with zero-length transmission lines connecting to the DUT.



**Figure 3.21** Schematic illustrating how the voltage measured at port 2 is related to the impedance of the DUT.

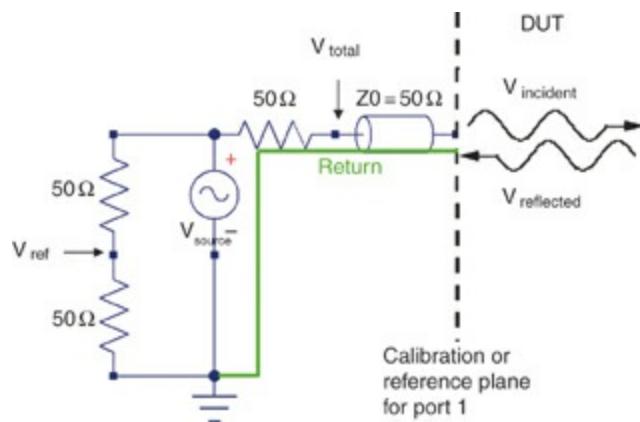
Figure 3.21 shows the equivalent lumped circuit model for two ports of a VNA connected across the same terminals of a shunted DUT. Because it is a lumped circuit model, there are no propagating waves, just voltage and currents at each node.

In this circuit we evaluate the voltage  $V_2$  measured at port 2 in terms of the voltage from the source and the impedance of the DUT. This is simple circuit theory. The voltage measured at port 2 is

$$V_2 = V_{\text{source}} \frac{\frac{50\Omega Z_{\text{DUT}}}{50\Omega + Z_{\text{DUT}}}}{\frac{50\Omega + Z_{\text{DUT}}}{50\Omega + Z_{\text{DUT}}}} = V_{\text{source}} \frac{Z_{\text{DUT}}}{50\Omega + 2Z_{\text{DUT}}} \quad (3.21)$$

Now that the voltage measured at port 2 is established in terms of the impedance of the DUT, we can include transmission line effects and translate this into  $S_{21}$ .  $S_{21}$  is the ratio of the signal  $V_2$  entering port 2 divided by the signal that is incident to port 1 of the DUT. To determine the voltage wave incident to port 1 we have to return to the model of the VNA that describes the waves into and out of the port.

The incident voltage to the DUT is the voltage coming out of port 1 of the VNA into port 1 of the DUT. This is probably the most confusing aspect of VNA circuit analysis. The actual voltage incident to the DUT, coming out of port 1, is independent of the impedance of the DUT, and depends only on the source voltage and the voltage divider of the source series resistance and the internal transmission line of the VNA. This is illustrated in Figure 3.22.



**Figure 3.22** Schematic of the internals of port 1 of a VNA showing how the voltage out of port 1, incident to the DUT, is related to the source voltage, the internal source impedance, and the transmission line from the source to the DUT. Also at port 1 is the reflected wave from the DUT. Both of these waves propagate in the transmission line internal to port 1. Their sum is measured as  $V_{\text{total}}$  by the internal voltmeter of port 1.

The incident voltage to the DUT, traveling from the left to the right is the result of the source voltage going through the voltage divider of the source resistance and transmission line impedance. The difference between the lumped element circuit with zero transmission line length and VNA port circuit is that the transmission line enables imagining the incident wave arising from the source voltage and the source impedance. The voltage incident to the DUT is

$$V_{\text{incident}} = \frac{50\Omega}{50\Omega + 50\Omega} V_{\text{source}} = \frac{1}{2} V_{\text{source}} \quad (3.22)$$

Using this relationship to convert the source voltage into the incident voltage, the Eqn 2.21 relationship for  $V_2$  is

$$V_2 = V_{\text{source}} \frac{Z_{\text{DUT}}}{50\Omega + 2Z_{\text{DUT}}} = 2 \times V_{\text{incident}} \frac{Z_{\text{DUT}}}{50\Omega + 2Z_{\text{DUT}}} = V_{\text{incident}} \frac{Z_{\text{DUT}}}{25\Omega + Z_{\text{DUT}}} \quad (3.23)$$

The reader may find it helpful to verify that the  $V_2$  voltage is correct for both the lumped element and transmission line circuit representations by checking

the solutions for several DUT impedances including zero,  $25 \Omega$ , and infinite impedance.

The definition of  $S_{21}$  is that  $S_{21} = V_2/V_{\text{incident}}$ . This relationship is converted into

$$S_{21} = \frac{V_2}{V_{\text{incident}}} = \frac{Z_{\text{DUT}}}{25\Omega + Z_{\text{DUT}}} \quad (3.24)$$

With a little rearranging, the impedance of the DUT is related to the  $S_{21}$  measurement as

$$Z_{\text{DUT}} = 25\Omega \frac{S_{21}}{1 - S_{21}} \quad (3.25)$$

This is an exact relationship and is valid for any values of the impedance of the DUT. When the DUT impedance is very small,  $S_{21}$  is very small and it reduces to the preceding approximation that  $Z_{\text{DUT}} = 25 \Omega \times S_{21}$ .

One caution: The  $S_{21}$  measurement suffers from numerical problems when the DUT impedance gets really large, similar to the way the  $S_{11}$  measurement suffers when the impedance gets really small. This happens when measuring small capacitors at low frequency or large inductors at high frequency. For PDN measurements we are most concerned with impedances that are very small compared to  $25 \Omega$ .

Note that  $S_{21}$  is complex and therefore the DUT impedance is complex as well. This is all handled in the complex algebra of this expression.

**Tip**

In the two-port Kelvin VNA measurement, the impedance of the device is related to the measured  $S_{21}$  in a simple relationship, which is exact and valid across the entire range of impedances from high to low. Always keep in mind that  $S_{21}$  and the impedance are both complex numbers and each varies with frequency.

This simple relationship is a key that unlocks the

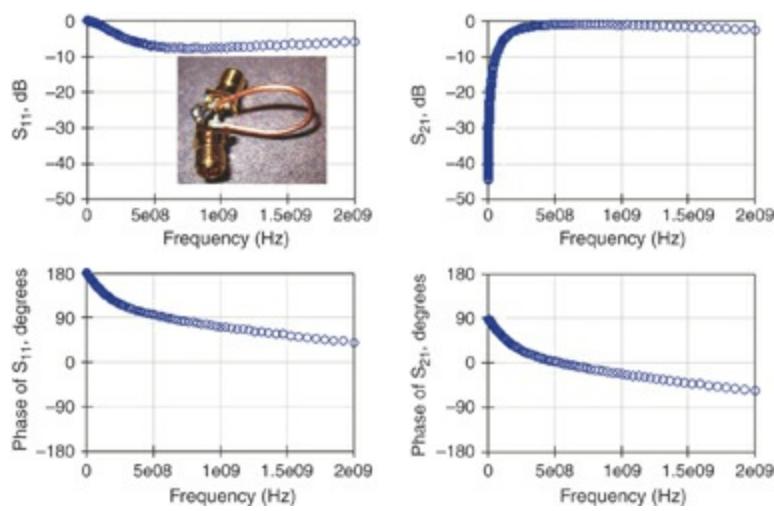
power of the Kelvin four-wire technique to enable measurement of impedances lower than  $1\text{ m}\Omega$  to frequencies greater than  $1\text{ GHz}$  [3]. By using a VNA set up for higher power, averaging, and a narrow pass band filter, a noise floor of  $-90\text{ dB}$  in  $S_{21}$  is routinely possible. This corresponds to an impedance of

$$Z_{\text{DUT}} = 25\Omega \frac{S_{21}}{1 - S_{21}} \approx 25\Omega \times S_{21} = 25 \times 3.16 \times 10^{-5} = 0.75\text{ m}\Omega \quad (3.26)$$

You can use *any* two-port VNA to measure low impedances using this relationship. It's just a matter of paying careful attention to the port connections to the DUT and avoiding the important measurement artifact described in section [3.11](#).

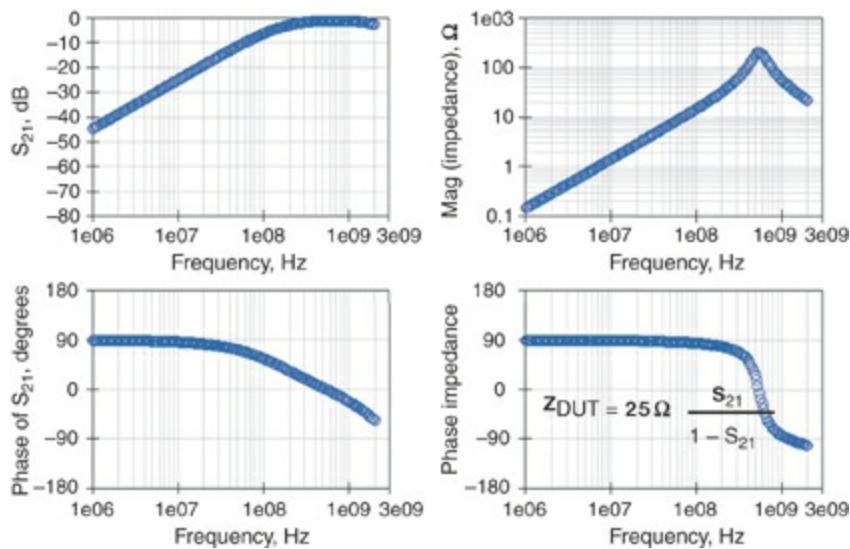
### **3.10 EXAMPLE: MEASURING THE IMPEDANCE OF A 1-INCH DIAMETER COPPER LOOP**

We also configured the 1-inch diameter copper loop measured with a one-port VNA in the example in [section 3.6](#) for a two-port measurement. We attached SMA connectors to the two ends of the loop with the signal pins of both SMAs to one end of the loop and the return pins of both SMAs to the other end of the loop. We took the two-port measurements over the same frequency range as the one-port measurements. [Figure 3.23](#) shows the DUT and its two-port measurements.



**Figure 3.23** Measured two-port S-parameters of the short copper loop shown in the inset picture.

The  $S_{11}$  measurement has little accurate information because it is a one-port measurement of a low impedance DUT. The  $S_{21}$  term does have accurate information about the DUT impedance. Using the Eqn 3.25 we convert the measured  $S_{21}$  into the impedance of the DUT. Figure 3.24 shows the measured  $S_{21}$  of the DUT and the calculated impedance, both plotted on a log-log scale.

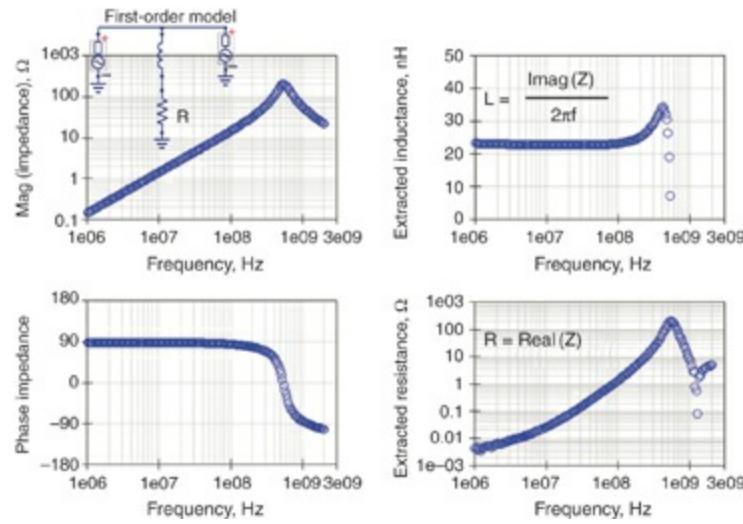


**Figure 3.24** Measured  $S_{21}$  and converted impedance of the short copper loop.

This extracted impedance is not based on any assumptions, models, or fitting. It is calculated directly from the two-port measurement of  $S_{21}$ . Below 1  $\Omega$  a common pattern exists between the magnitude and

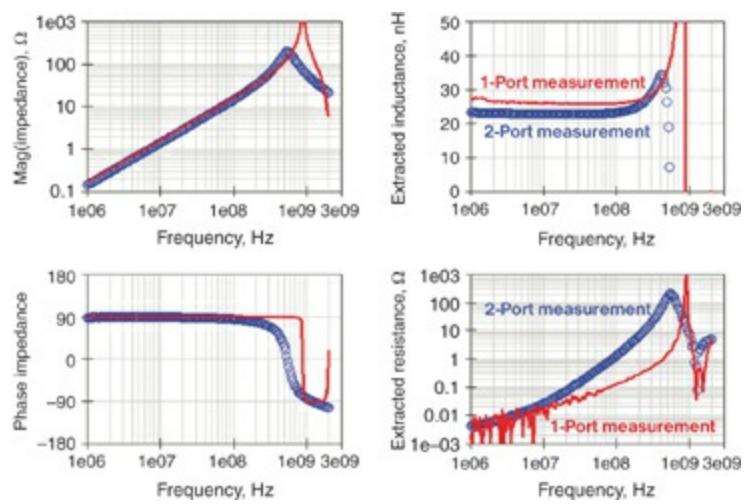
phase of  $S_{21}$  and the impedance. In this low range the DUT impedance is approximately  $25 \Omega \times S_{21}$ . This simple relationship breaks down above  $10 \Omega$ .

Impedance increasing linearly on a log-log scale is an indication of a series inductor. We now assume a simple series R and L model for the DUT and interpret the real part of the impedance as the resistance R and the imaginary part of the impedance as related to the inductance L. [Figure 3.25](#) shows the extracted values of R and L plotted using a simple series RL circuit for interpreting the impedance.



**Figure 3.25** Extracted R and L from the measured impedance of the wire loop based on a simple RL circuit model.

How well do the R and L values extracted from two-port measurements match the R and L values extracted from one-port measurements? To make this comparison, the second port needs to be disconnected and not loaded by a  $50\Omega$  termination. [Figure 3.26](#) superimposes the extracted R and L values for the one-port and two-port measurements.



**Figure 3.26** Comparing the impedance and extracted L and R values of the wire loop from one-port (solid line) and two-port (circles) measured data.

The inductance extracted from the two-port measurement shows a lower value compared to the one-port measurement. This is because the inductance in the one-port measurement has the contribution of the series inductance of the short SMA fixture. The 5 nH difference in inductance is the series inductance of the SMA fixture.

#### Tip

The inductance of the short SMA connector creates a significant difference in the extracted inductance between the one-port and two-port measurements. This fixture effect is eliminated in the two-port technique, but another subtle artifact exists in the two-port technique to consider.

The extracted resistance is also subtly different between the one-port and two-port measurements. At low frequency, when the resistance is very small, the one-port measurement shows considerably more noise. The two-port resistance is about 8 mΩ at 10 MHz. The series resistance increases with frequency in both cases. Is this an indication of skin depth or some other effect? We answer this important question in the next section.

## 3.11 ACCOUNTING FOR FIXTURE ARTIFACTS

An important way to interpret the measured data from any DUT is by building an equivalent circuit model that includes the effects expected and comparing the predictions of the simulated model with the measured result. This is the process of “hacking.” Good agreement between the measured behavior and simulated model builds confidence that the behavior is consistent with the model.

Even when excellent agreement exists between measured and simulated responses, the only accurate conclusion is that the model is consistent with the measurement. Good agreement still does not prove the model is the correct explanation for the real world, only that it is consistent with it. There could always be another effect going on that has the same frequency dependence.

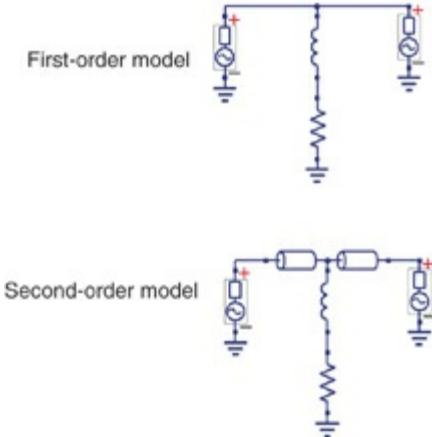
**Tip**

Good agreement between the predictions of a model and the measurements can't prove the model is correct, only that it is consistent with the real DUT. You can never do too many consistency checks. The more you pass, the higher your confidence that the model represents what is going on “under the hood” in the DUT.

Another interpretation of the resistance increasing with frequency, in addition to a skin depth effect, is that the simple series RL model is incomplete for what is being measured. We interpreted the wire loop in terms of a single RL circuit. From this model we interpreted the two-port impedance measurement in terms of R and L values. Although this is a good approximation, we can improve the model. One improvement is to add the effect of the SMAs on each port by modeling them as short transmission lines.

The second-order model adds identical, uniform, lossless transmission lines on either side of the RL

circuit to connect the ports of the VNA. The interconnect structures from the reference plane of the VNA to the DUT are generally called the *fixture*. Figure 3.27 shows the first-order RL circuit element model and the second-order model including the fixture.



**Figure 3.27** First-order and second-order circuit models used to simulate the expected two-port S-parameters for the wire loop.

This second-order model has four parameters:

$R$  = the series resistance of the wire loop, constant with frequency

$L$  = the loop inductance of the wire loop, constant with frequency

$Z_0$  = the characteristic impedance of the SMA feed transmission line fixture

$TD$  = the time delay of the SMA feed transmission line fixture

The most important action of the fixture is to introduce a phase shift in  $S_{21}$  that is more than the DUT alone. This shifts some of the imaginary part of the extracted DUT impedance into the real part because the phase of the fixture is increasing with frequency.

One way of optimizing parameter values for the fixture and DUT is to vary these parameters until good agreement exists between the simulated model and the measured results. This is how we “hack” an interconnect

model from measurements. At low frequency the transmission line elements of the fixture do not affect the simulations so we can extract the R and L values of the DUT from the low-frequency response.

We can also extract the impedance and TD of the SMA fixture. We initially approximate the characteristic impedance as  $50 \Omega$  and adjust the time delay of the fixture until the simulated model's impedance matches the measured impedance. In a simple, manual process the parameters of the second-order model are extracted as a best fit to the measured data. An optimizer routine could also perform this extraction with a little more accuracy. The final values of each parameter are

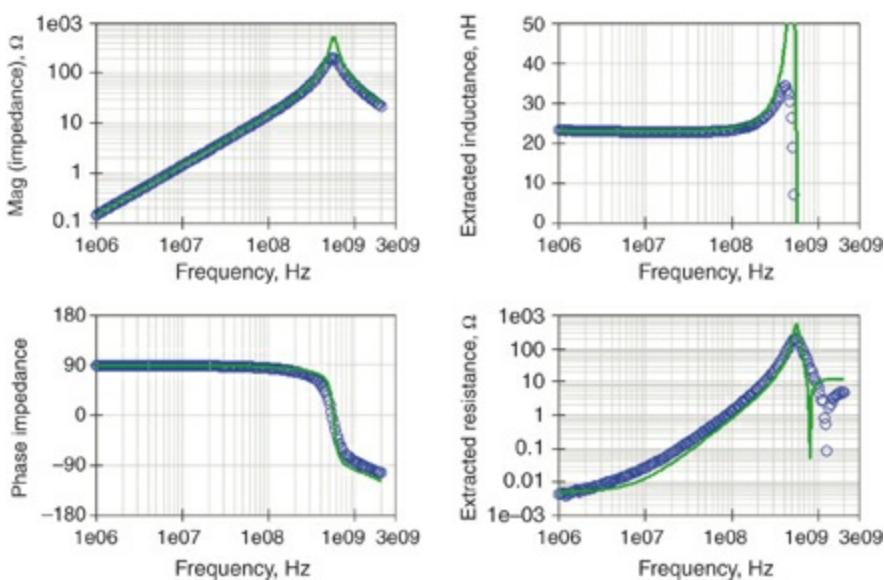
$$R = 0.005 \Omega$$

$$L = 23 \text{ nH}$$

$$Z_0 = 50 \Omega$$

$$TD = 42 \text{ ps}$$

Figure 3.28 shows the final agreement between the measured two-port impedance, extracted R and L values, and the predictions of the model. The extracted R and L values are based on interpreting the measured or simulated two-port S-parameters as a simple R-L series model.



**Figure 3.28** Comparing the measured data (circles) with the simulation of the second-order model (solid line) for the wire loop.

The agreement between the measured impedance and the simulated impedance is excellent. A simple RL model would have predicted the impedance to increase linearly. We see that the introduction of the transmission line fixtures of the SMA launches explains the peak and drop-off around 600 MHz.

When the transmission line models for the SMA fixture are added to the model, the simulated real part of the impedance (which we naively interpreted as the series resistance of the wire loop) shows a strong frequency dependence. The model uses an ideal R element that is absolutely constant with frequency. Yet, the presence of the transmission line fixtures makes the simulated real part of the impedance look frequency dependent.

#### Tip

The fixture to the DUT adds a phase to the  $S_{21}$  measurement that shifts some of the imaginary impedance into real impedance, acting as if there were a series resistance increasing with frequency. This is an artifact of the fixture and is the chief artifact to watch out for in these low impedance two-port impedance measurements.

A simple explanation exists for why the short SMA fixture leads appear as a real part of the impedance and increase with frequency. The transmission line segments on each end add a negative phase shift to  $S_{21}$ , which increases with frequency. Because the impedance and  $S_{21}$  are virtually the same, a negative phase shift is added to the impedance. The inductance of the loop has an impedance phase of nearly 90 degrees and the negative phase shift from the short transmission line fixture shifts this phase toward zero. This increases the real part of the impedance, which we interpreted—incorrectly—as a resistive element.

The increasing real part of the impedance with frequency is not created by a resistor but by a phase shift in the impedance. No need exists to invoke a “skin depth” effect to explain the increasing real part of the impedance with frequency. We recognize that the real part of the impedance extracted from the two-port S-parameters is not contributed by just the R element but is a function of the entire circuit in which the R element is embedded.

All that was needed to get good agreement between the measured and simulated impedance of the model was a simple series RL circuit with the fixture included. If we still did not have adequate agreement after the inclusion of the fixture model, we could have included a small shunt capacitor to account for the coupling from one half the loop to the other half, especially at higher frequency.

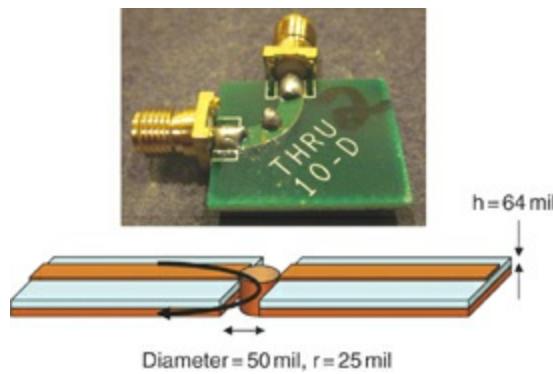
In this specific loop example there was no need for a model more complicated than a simple RL circuit up to about 300 MHz where the distributed effects began.

**Tip**

As a general rule, starting with the simplest model possible and building complexity as needed to match higher frequency effects is always a good practice. It is astonishing how well very simple models match the measured behavior of real structures up to very high frequency.

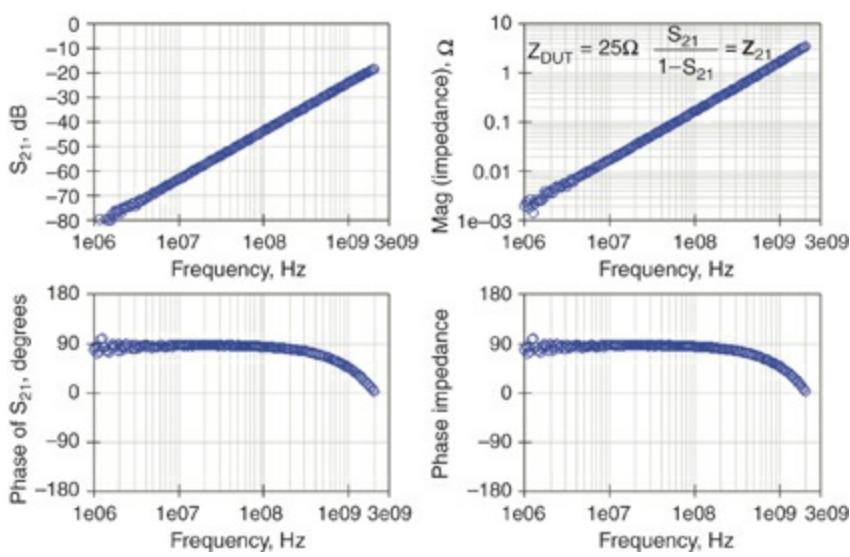
### 3.12 EXAMPLE: MEASURED INDUCTANCE OF A VIA

We constructed a simple test vehicle to extract the total inductance of a via used to short between the signal line and the return path in a microstrip. [Figure 3.29](#) shows a closeup of the short circuit board and an illustration of the structure.



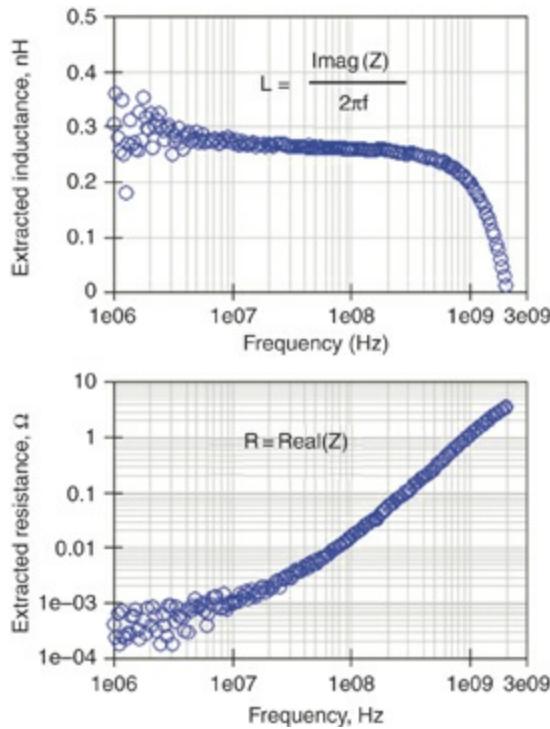
**Figure 3.29** A simple test fixture to measure the inductance of a via.

This two-layer board has a through-connected  $50\text{-}\Omega$  microstrip trace connecting two SMA connectors. A 50 mil diameter hole was drilled in the middle of the signal trace and a 50 mil diameter wire inserted. It was soldered between the top signal line and the bottom return plane, shorting the signal line. This is the via structure that we will measure with the two-port technique. The microstrip and SMAs act as the fixture to interface with the VNA. [Figure 3.30](#) shows the two-port S-parameters and the converted impedance.



**Figure 3.30** Measured two-port impedance of the via in the middle of the transmission line and its extracted impedance.

Using a simple model to describe the via as a series RL circuit, we can interpret the real part of the measured impedance in terms of the R value and the imaginary part as related to the L. We convert the impedance into R and L values, which are shown in Figure 3.31.



**Figure 3.31** Extracted R and L values based on interpreting the measured impedance in terms of a simple RL model.

We see again an inductance that drops off with frequency and a resistance that increases with frequency. Is this real? As we noted earlier, we might account for the frequency dependence of the R and the drop off in inductance with frequency by using a more complex model that includes the model for the fixture. It is exactly the same R L model topology as used in sections 3.6 and 3.10 for the wire loop, just with different parameter values. For this via in the middle of the uniform transmission line, the parameters that give the best agreement with the measured data are

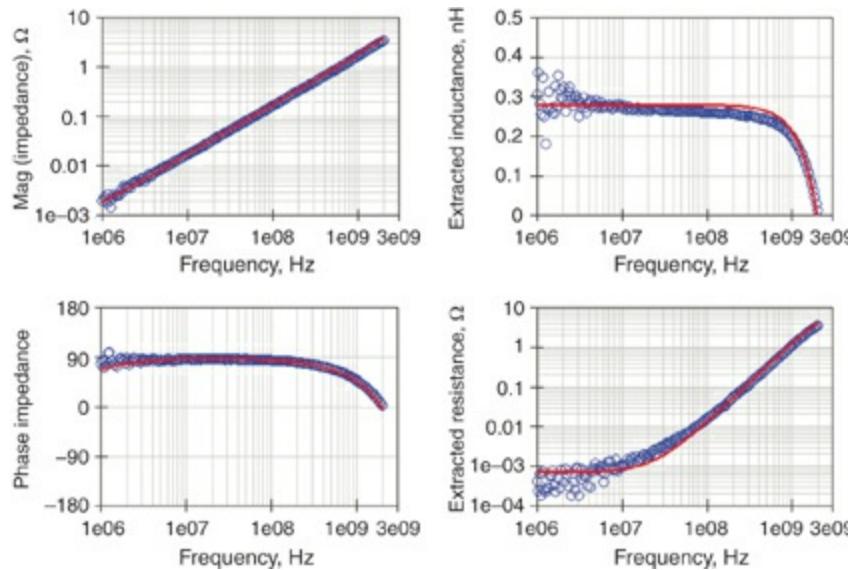
$$R = 0.0007 \Omega$$

$$L = 0.28 \text{ nH}$$

$$Z_0 = 50 \Omega$$

$$TD = 210 \text{ ps}$$

The agreement between simulated and measured impedance is excellent using these values in the second-order model across the whole bandwidth of the measurement. Figure 3.32 shows the resulting real part of the impedance and the equivalent single element inductance.



**Figure 3.32** Measured impedance (circles) and simulated impedance from the second-order model (solid line) for the two-port measurements of the single shorting via.

What looks like frequency-dependent inductance and resistance of the via is really a measurement artifact introduced by the phase shift in the fixture.

Interpretation of the measurement must include the fixture leading to the DUT. We can reproduce the precise measured data across the full 2 GHz bandwidth when correct interpretation of the measurement includes the ideal model of a transmission line feed to an ideal L and R.

Analyzing the measured values of the physical structures to see whether they are reasonable is instructive. From the geometry of the via, we can estimate the expected DC resistance and the total inductance.

The DC series resistance and partial self-inductance of a short cylinder are approximately

$$R = \rho \frac{Len}{\pi r^2} \quad \text{and} \quad L_{\text{total}} = 5 \times Len \left\{ \ln \left( \frac{2 \times Len}{r} \right) - 0.75 \right\} \quad (3.27)$$

where

R = the series resistance in  $\Omega$

$\rho$  = the bulk resistivity of copper =  $0.7 \times 10^{-6} \Omega\text{-inches}$

Len = the length of the via = 0.064 inches

r = radius of the via = 0.025 inches

L<sub>total</sub> = the total inductance of the via, in nH

Because the return path of the via is relatively far away, we approximate the total inductance of the via as the partial self-inductance of the via. Using these values for the physical features of the via, the DC series resistance and total inductance are estimated as

$$R = 0.7 \times 10^{-6} \frac{0.064}{\pi \times 0.025^2} = 0.02 \text{ m}\Omega$$

(3.28)

and

$$L_{\text{total}} = 5 \times 0.064 \left\{ \ln \left( \frac{2 \times 0.064}{0.025} \right) - 0.75 \right\} = 0.29 \text{ nH}$$

The series resistance extracted from the measurement is about 0.7 mΩ, about 35 times higher than the predicted resistance of 0.02 mΩ. This is probably related to a combination of the noise floor of the VNA and some skin depth resistance. At 10 MHz, the skin depth in copper is about 0.8 mils. The cross-sectional area through which current flows is not the geometrical area, 0.002 inches<sup>2</sup>, but the area of the annulus of the circumference × the skin depth or  $2\pi r \times 0.0008$  inches = 0.00013 inches<sup>2</sup>. The resistance at 10 MHz is  $0.002/0.00013 = 15$  times higher. This is within a factor of two of what was extracted. The actual resistance, increasing with the square root of frequency, is masked by the artifact of the fixture causing the apparent resistance to increase by the square of the frequency.

The predicted total inductance of the via, 0.29 nH, based on the partial self-inductance of a straight rod, is very close to the extracted value of 0.28 nH. We see that these measured values are reasonable for this structure.

Both the wire loop and the via examples illustrate that although two-ports enable measurements of smaller impedances at higher frequencies compared to one-port measurements, they still require some care in interpreting the results. The impact on the phase shift from the fixture connecting the DUT to the SMA at high frequency requires special attention. When the fixture is simply modeled, separating out the intrinsic low impedance properties of the DUT and the fixture is possible.

**Tip**

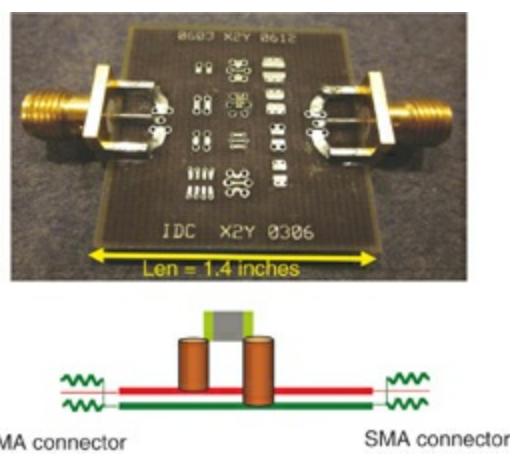
Although two-ports eliminate the artifacts of one-port measurements, they still require care in interpreting the results, especially at high frequency, due to the phase shift from the fixture connecting the DUT to the SMAconnectors to the VNA.

### 3.13 EXAMPLE: SMALL MLCC CAPACITOR ON A BOARD

Measuring the properties of a discrete component all by itself is often difficult. Some sort of connection is required between the DUT and the SMAs of the VNA connections. In the case of a capacitor, measuring the intrinsic properties of a capacitor independent of how it is mounted onto the fixture is impossible. The same capacitor will have completely different impedance profiles depending on the structure of the fixture to which it is attached. Given this limitation, measuring the impedance profile of any simple discrete capacitor element and its specific mounting inductance is straightforward.

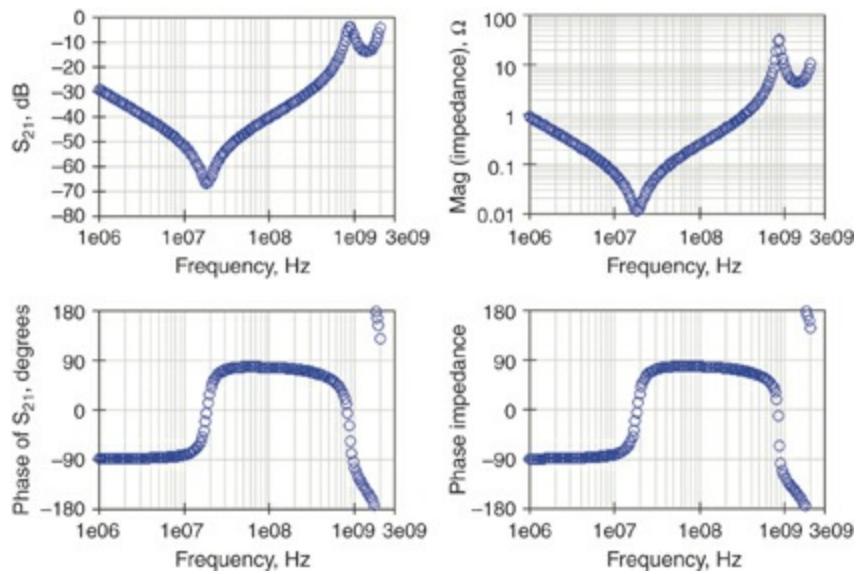
One commonly used fixture is a four-layer board with planes feeding from the edge of the board where SMAs are connected to the central region of the board where discrete capacitors are mounted.

An example of such a board, provided by X2Y Attenuators, is designed for two-port measurements with various mounting pad configurations. By moving the capacitor to different pads, we can easily measure the impact on impedance from different pads or different capacitors. [Figure 3.33](#) shows the board and a schematic of the cross section showing the capacitor vias and internal planes.



**Figure 3.33** Example of a fixture board to measure the impedance properties of a surface mount–attached capacitor, and a rough schematic of the internal configuration, courtesy of X2Y Attenuators.

An X2Y capacitor is mounted to the pads on the fixture board and the two-port S-parameters are measured. **Figure 3.34** shows the measured  $S_{21}$  and converted impedance, as viewed from the SMA connectors of the fixture board.



**Figure 3.34** Measured  $S_{21}$  and converted impedance of the capacitor-evaluation-fixture board.

The impedance matches the profile of a simple RLC circuit. Virtually all commonly used capacitors show this simple behavior. By adjusting the R, L, and C values in the model, we can find a combination that simulates an impedance profile nearly identical to the measured

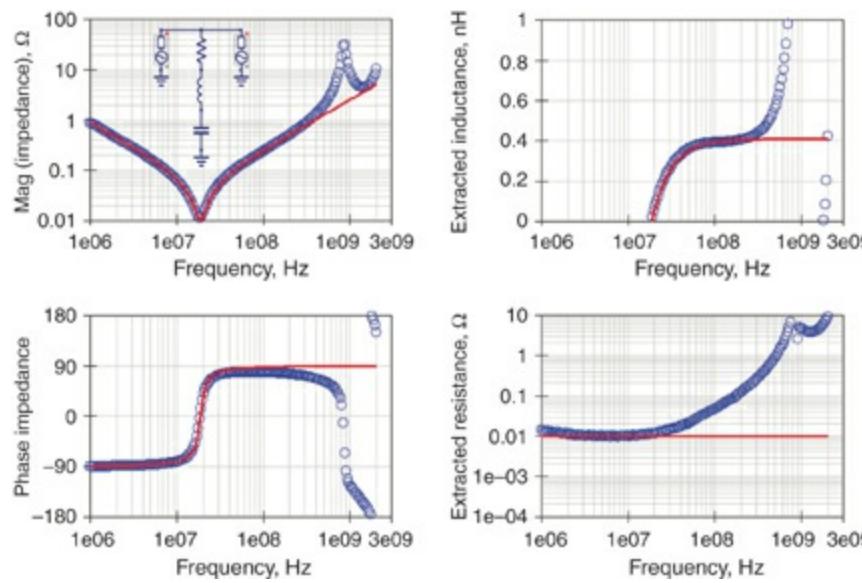
values.

Using the following values, the agreement is excellent, as shown in Figure 3.35.

$$R = 0.01 \Omega$$

$$C = 175 \text{ nF}$$

$$L = 0.41 \text{ nH}$$



**Figure 3.35** Measured impedance (circles) and simulated impedance (solid line) of a simple RLC model shown in the upper left-hand panel and the extracted L and R based on the real part of the impedance and the imaginary part of the impedance.

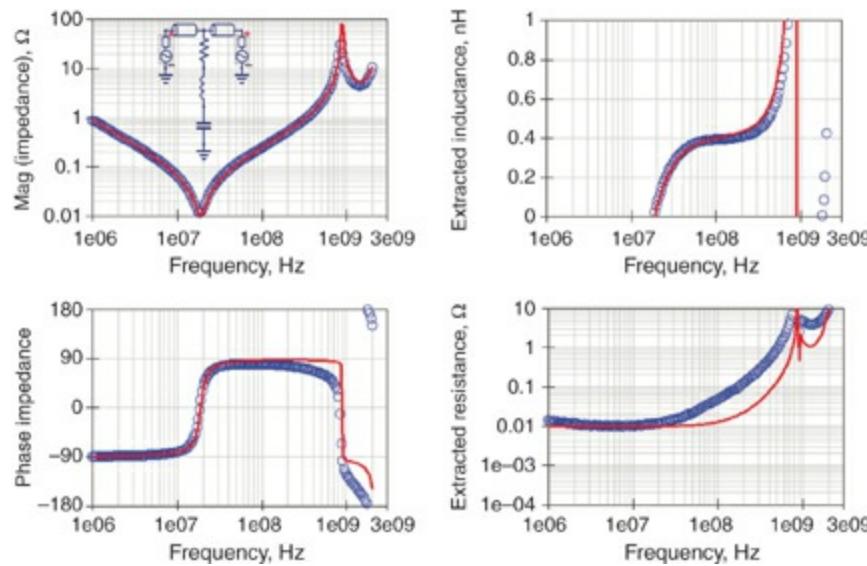
That such a simple model works so well to describe this real component is remarkable. However, this model only matches the measured response up to about 400 MHz. As we have seen before, the finite size of the fixture begins to play a role at high frequency and must be included in the model. The simplest model for the fixture on either end is a short, uniform transmission line.

#### Tip

Remarkably, the measured impedance profile of real capacitors mounted to boards in various ways matches the behavior of a simple RLC circuit to very high frequency. Complicated structures can have simple models.

In this capacitor fixture board, the length of interconnect from the beginning of the SMA to the center of the board where the capacitor is mounted is about 0.7 inches on each side. Once again, simple transmission lines are chosen to represent the fixture. The length is hardcoded into the transmission line model leaving the characteristic impedance as the only parameter to fit the measured data. Through a few trials, a value of  $3.5 \Omega$  was found to give very good agreement. This is a reasonable value because the connection between the SMA and the capacitor mount is a wide plane.

When the transmission line fixture model is added on either side of the RLC model, we see the agreement, as shown in [Figure 3.36](#), is very good.



**Figure 3.36** Comparison of measured and simulated response, including the transmission line model for the fixture and the simple RLC circuit model for the capacitor mounted to the fixture board.

This simple model of an RLC series circuit to describe the capacitor and two uniform transmission lines to describe the fixture for the capacitor are very good approximations. Evaluating whether the residual discrepancy between the measured and modeled impedance is a real feature of the capacitor or related to

fixture parasitics not accounted for by this simple model is difficult. This is why you should always design fixtures to introduce the minimum artifacts in the measurements as possible.

**Tip**

Because of the artifact introduced by the fixture length affecting the real part of the extracted impedance, always design fixtures with as short a length as possible and to look as close to a  $50\text{-}\Omega$  transmission line as possible.

The possibility exists that the real part of the impedance increasing from 40 MHz to 800 MHz is a real feature of the capacitor, perhaps related to the dissipation factor of the ceramic, the number of capacitor plates engaged at high frequency, or the series resistance of the capacitor and mounting conductors. These features are not included in the simple RLC model.

The value of the C extracted from the model is the bulk capacitance of the capacitor. This unit was specified as 220 nF. The value extracted is 175 nF. This is about 25% low, not unexpected.

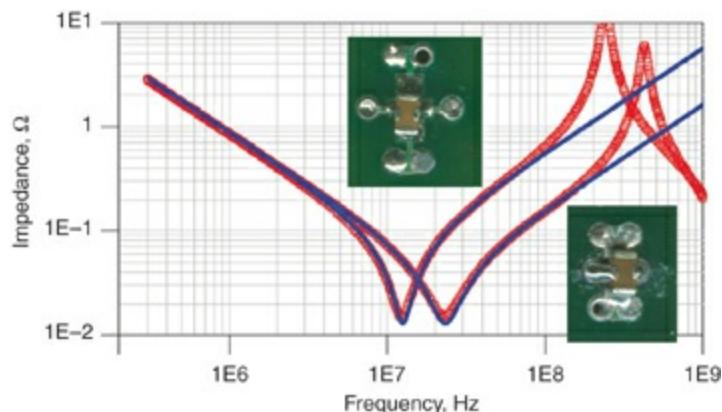
The R extracted was  $0.01\ \Omega$ . This is usually referred to as the equivalent series resistance (ESR). The ESR is an important property of capacitors that plays a dominant role in damping parallel resonances.

The value of the  $L = 0.41\text{ nH}$  is referred to as the equivalent series inductance (ESL). This value is not intrinsic to the capacitor, but related to how it is mounted to the board. It is the most important design term of any capacitor because it fundamentally sets the limit on the minimum number of capacitors required for the PDN. The goal when integrating capacitors into a system is to design as low an ESL as possible. In this case, the relatively low value of ESL is due to the special

design of the X2Y capacitor, enabling a low mounting inductance and the nearly via-in-pad mounting to the test board.

We can measure almost any value of ESL for a capacitor depending on how it is mounted to the board, the specific stackup of the board under the capacitor, and how much spreading inductance exists between the capacitor and port locations. It is not intrinsic to the capacitor.

We can use this two-port technique to explore different capacitor mounting techniques and empirically determine the total mounted inductance. For example, [Figure 3.37](#) shows the measured impedance profile for two similar capacitors mounted with different surface trace lengths to a multilayer fixture board. The ESL for the two cases was measured as 0.2 nH and 0.9 nH.



**Figure 3.37** Measured (circles) and simulated (line) impedance for two capacitors with slightly different mounting geometry resulting in dramatically different ESL. SMAs, not shown in the closeups, were used as part of the two-port measurement fixture for these capacitors.

The impedance at the high-frequency end shows a large difference in the ESL of the two different mounting techniques. With close to via-in-pad mounting, the ESL extracted from the measurement is 0.2 nH. When surface traces just 20 mils long connect the capacitor pads to vias, the ESL dramatically

increases to 0.9 nH. This example shows how important the small details of capacitor mount design are to achieving low ESL.

**Tip**

Using these low impedance measurement techniques we can explore the mounting inductance of capacitors. It is remarkable how small features have a large impact on the mounting inductance.

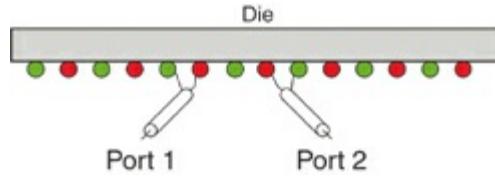
### **3.14 ADVANCED TOPIC: MEASURING ON-DIE CAPACITANCE**

The two-port method for measuring low impedance is not limited to very low impedance. This method is also well suited to measure the large dynamic range associated with the impedance of on-die capacitance, one of the most important PDN properties [4].

This section examines the two-port measurements of on-die capacitance for three configurations: from the perspective of the bumps of a bare die, from a single pair of package balls, and from two pairs of package balls. In each case, we must interpret the measurement to include some uncalibrated extension of the measurement fixture. By using two different ball or bump pairs for the two ports, we can measure deeper into the DUT and eliminate some of the impedance that is in series with the device that we really want to measure. However, the two-ball-pair measurement is sometimes degraded by insertion loss or transimpedance effects. We begin by probing the bumps of a bare die.

Figure 3.38 illustrates the measurement configuration for probing the Vdd and Vss rails of a die from the C4 bumps. The die is biased up by the VNA and the two probe points are relatively close together. The VNA is calibrated right to the tips of the microprobes.

The residual, uncalibrated or nonreproducible circuit component of the tips can be roughly approximated as a transmission line element with an impedance of  $50 \Omega$  and a TD of about 1 ps. This corresponds to variations in the tip placement and distortion of about 10 mils.

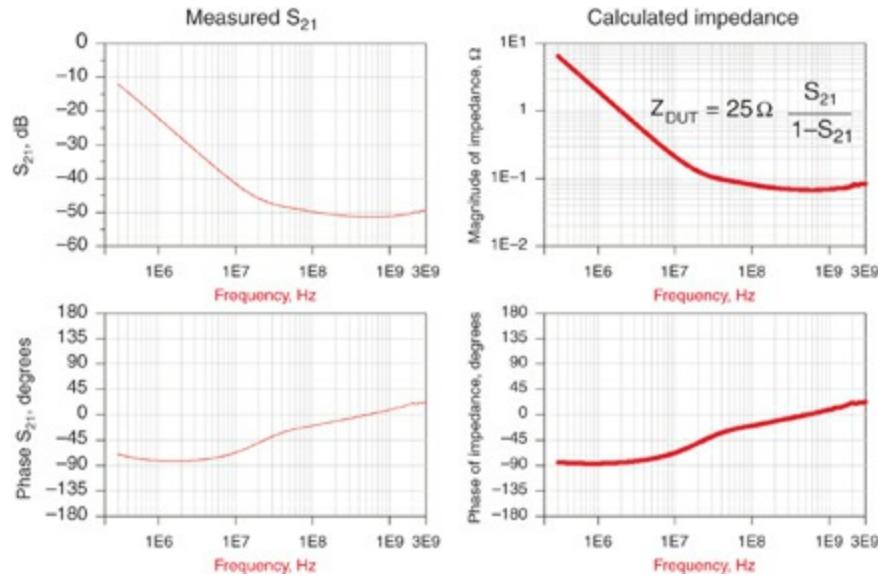


**Figure 3.38** Probing configuration for the Vdd and Vss power rails measured from die bumps.

We measure the two-port S-parameters with a VNA from 300 kHz to 3 GHz. From  $S_{21}$ , we extract the impedance using

$$Z_{\text{DUT}} = 25 \Omega \frac{S_{21}}{1 - S_{21}} \quad (3.29)$$

**Figure 3.39** shows the measured  $S_{21}$  and the calculated  $Z_{\text{DUT}}$ .

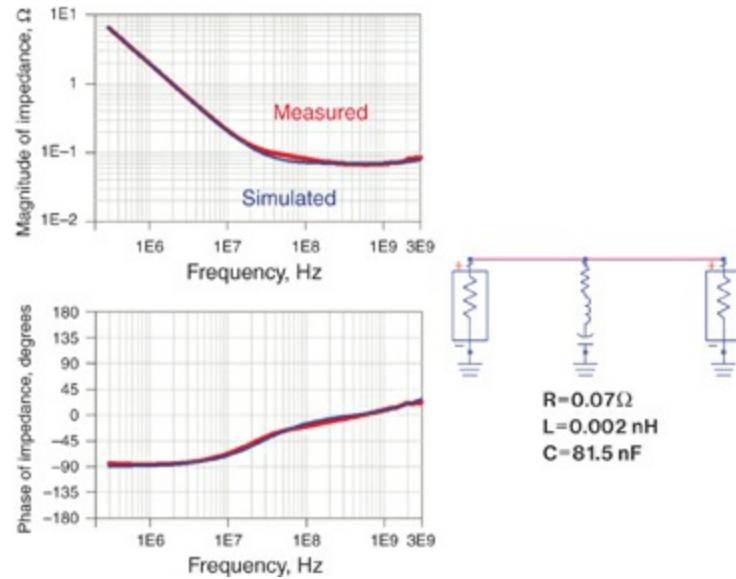


**Figure 3.39** Measured  $S_{21}$  from two separate solder bump pairs on-die and the resulting transfer impedance from calculation.

We extract the impedance looking onto the die's solder bumps in two ways. First, we perform simulation

on a simple series RLC circuit model. RLC parameters are optimized for a best fit with the measured  $S_{21}$  data. The C value is selected to match the impedance behavior at low frequency. The R value is adjusted to match the performance near the lowest impedance and the L value is adjusted to match the impedance at high frequency.

Figure 3.40 compares the measured impedance with the simulated impedance of the RLC model using the best-fit values.



**Figure 3.40** Comparing the measured impedance of the power rail of the bare die and the simulated impedance, based on the simple RLC circuit on the right.

It is remarkable that so simple a model matches the measured impedance profile of the on-die PDN so well. From the simulated model, the on-die capacitance is extracted as 81.5 nF for this die and power rail. The very low value of L, only 2 pH, is related to the very low spreading inductance looking into the power-ground grid towards the on-die capacitance. This is a direct benefit of the very thin dielectric between the Vdd and Vss grid on die and its small size.

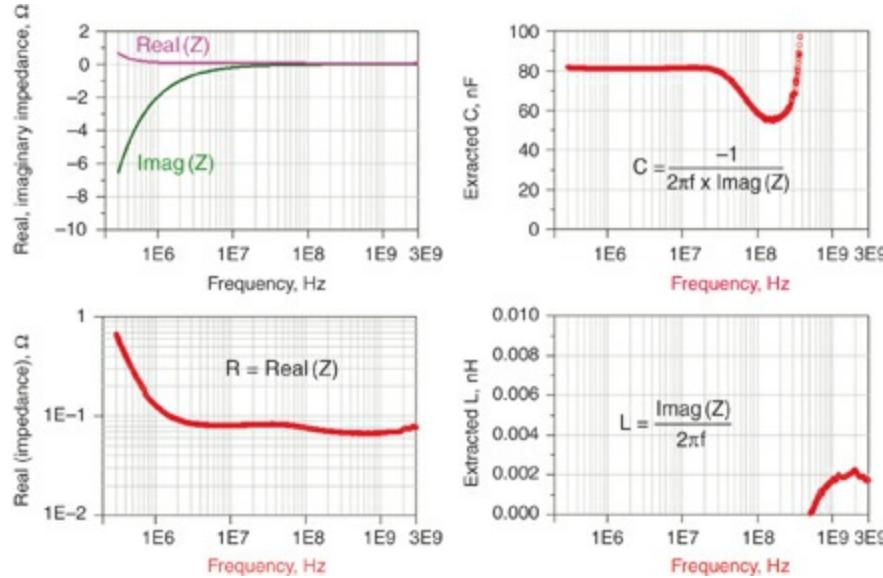
An alternative way of extracting the impedance profile is by assuming a series RLC topology and calculating the C and L values from the imaginary component of the

impedance. The real part of the impedance is interpreted as R. This gives a reactive and resistive estimate for the PDN impedance at every measured frequency point.

Figure 3.41 shows the converted impedance from the  $S_{21}$  measurement with the C, L, and R values extracted.

**Tip**

We can extract the measured impedance profile in two ways by assuming an RLC circuit topology. The first method involves circuit simulation and curve fitting with optimized parameter values; the second method involves interpreting the real part of the impedance as R and the imaginary part as C or L and making calculations at each frequency point.



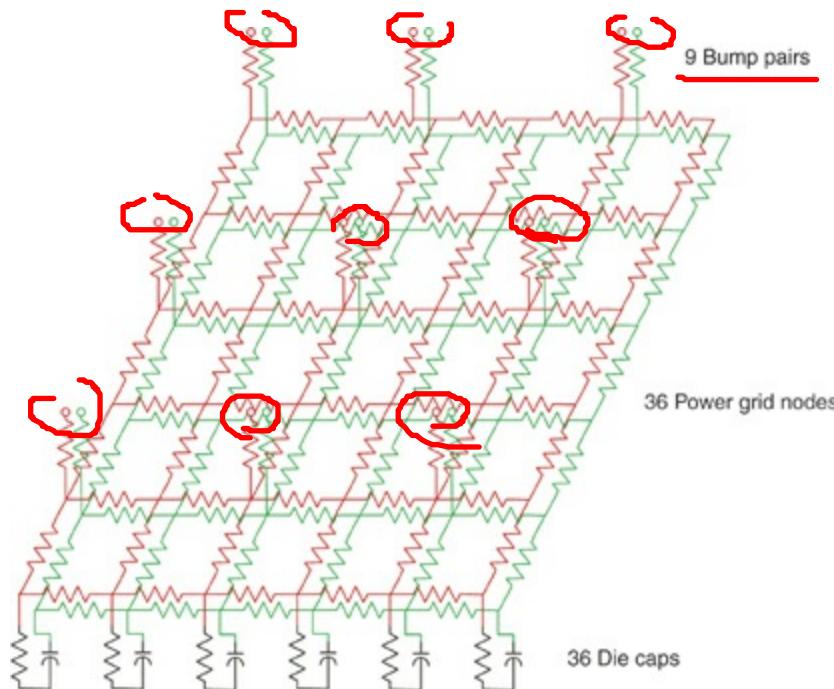
**Figure 3.41** Real and imaginary components of the impedance and the extracted R, L, and C values calculated at each frequency point.

The best calculated C value is 81 nF at low frequency as expected from simulation and curve fitting. C starts to vary above 40 MHz. This is because the impedance is no longer determined just by capacitance but also inductance.

The inductance reaches 2 pH above 1 GHz. This is close to the noise floor of this measurement. The frequency variation in L is because the imaginary part of the impedance is due to more than just L.

The resistance shows some frequency dependence. At low frequency, this could be due to a contribution from the dielectric loss of the SiO<sub>2</sub> on-die insulation or a contribution from the leakage current. At high frequency, the slight drop in resistance may be due to the onset of fixture effects.

The R value of 70 mΩ, obtained in both approaches, is from a combination of spreading resistance of the Vdd and Vss on-die grid and the shunt resistance of the on-die capacitance. [Figure 3.42](#) illustrates the inherent 3-D nature of the on-die distributed capacitance and resistance [5].



**Figure 3.42** Illustration of the distributed on-die capacitance, its shunt resistance, and the spreading resistance of the power and ground rails. This network is probed at various solder bump locations.

At high frequency, above about 100 MHz in this measured example, the impedance is mostly resistive. The resistor elements that contribute to this behavior are identified in the approximate circuit network. At high frequency the distributed capacitance has such a low impedance compared to its associated shunt resistance that the circuit network from bump to bump

at high freq, cap almost shorted

is nearly resistive.

When measured between two pairs of solder bumps, the transfer impedance can be interpreted directly in terms of the insertion loss  $S_{21}$ . The voltage at port 2 is related to the resistive divider network of the  $50\text{-}\Omega$  source impedance of port 1, the equivalent series and shunt resistance of the circuit network and the  $50\text{-}\Omega$  impedance of port 2. For the specific probed solder bumps, the voltage divider network results in  $-50$  dB attenuation of the VNA signal from port 1 to port 2.

If port 2 were to move farther from port 1, more shunted conductance would exist between the power and ground grids and more series resistance, both resulting in lower voltage measured at port 2 and more attenuation. The transfer impedance drops and appears as a lower resistance. Interpreting the transfer impedance and the extracted, equivalent resistance as the series-damping-resistance of the on-die power grid is incorrect. It is a composite value of the combination of shunt and series resistance. Its value is inherently a 3-D planar effect.

This is a general problem that occurs often in two-port PDN measurements of distributed structures. We must use two ports and the insertion loss,  $S_{21}$ , to interpret impedance because a single port and  $S_{11}$  does not work well for low impedance measurements at high frequency. But the two-port measurement is really an insertion loss measurement and gives a  $Z_{21}$  value, which is really a transfer impedance. Some amount of attenuation will always exist over the space of the two-port measurement. This is sometimes called spatial attenuation and should not be interpreted as low impedance. Insertion loss, also known as transimpedance and spatial attenuation, should be considered in the interpretation of all PDN two-port

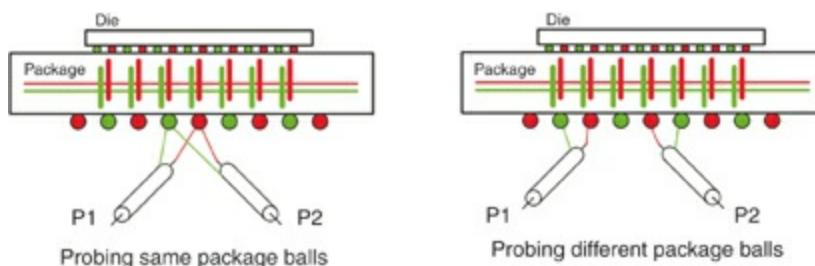
measurements of distributed planar structures [4][6].

**Tip**

Interpreting the measured transfer impedance of a distributed structure is tricky, especially when both series and shunt impedances are involved. In the absence of matching the measured transfer impedance at a few points to a simulated transfer impedance using a 3-D distributed model, only a rough hand-waving interpretation is possible.

From a PDN resonance standpoint, this equivalent on-die distributed resistance is a good thing because it helps damp the peak impedances at the parallel resonances. Unfortunately for the PDN resonances, this resistance is shorted out by the much lower resistance of the package metal layers. The package metal layers are connected to the die through the many C4 bumps distributed over its surface and provide another layer of interconnect to combine the distributed on-die capacitance.

We now move from the die bumps to the package balls. When the die is measured looking through the package, the impedance must be interpreted based on the composite structure. [Figure 3.43](#) illustrates two ways of probing the die through the package.

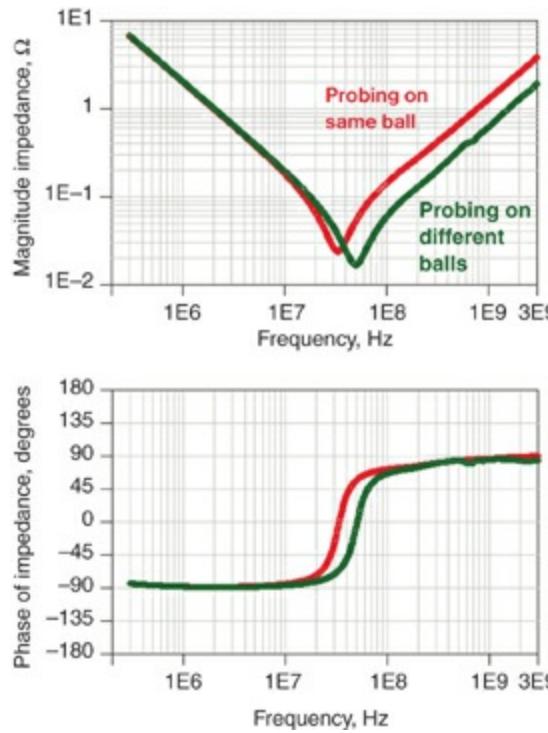


**Figure 3.43** Two ways of probing the chip's PDN from the package solder balls through a single ball pair or two ball pairs. In both cases, the die PDN has the package PDN impedance as part of it.

When the probes from port 1 and port 2 touch the same ball pair on the package and look into the die, the package solder balls and initial package via inductance

are included in the DUT and are part of the series impedance path. When the two probes of the VNA contact two different pairs of package solder balls, some of the package PDN is part of the impedance path to the die and is considered to be an uncalibrated portion of the fixture. The DUT begins at the package power planes where port 1 and port 2 meet up for the first time. The inductance and resistance of the single ball pair has been removed from the measurement. This is good because the measurement is made closer to the on-die capacitance but it also requires careful interpretation.

We measured the two-port S-parameters for both probe configurations and the impedance calculated. Figure 3.44 shows the measured impedance in these two cases.



**Figure 3.44** Measured impedance of the on-die PDN using the two-port technique, probing through the package with two different ball pair connections.

At low frequency, the impedance is determined by the on-die capacitance and is the same whether measured from the die bumps or from the package balls. Interpreting the impedance at higher frequency in terms

of the inductance and resistance of the structure is more complicated.

As viewed from the package balls, the high-frequency impedance is related to the composite structure of both the package and the die. The package planes have higher inductance but lower resistance. The die has low inductance but higher resistance associated with the on-die power grid. The package and die interconnects are in parallel because PDN current can be delivered to the circuit load and the on-die capacitance through either path. This is further complicated by the location of the probes.

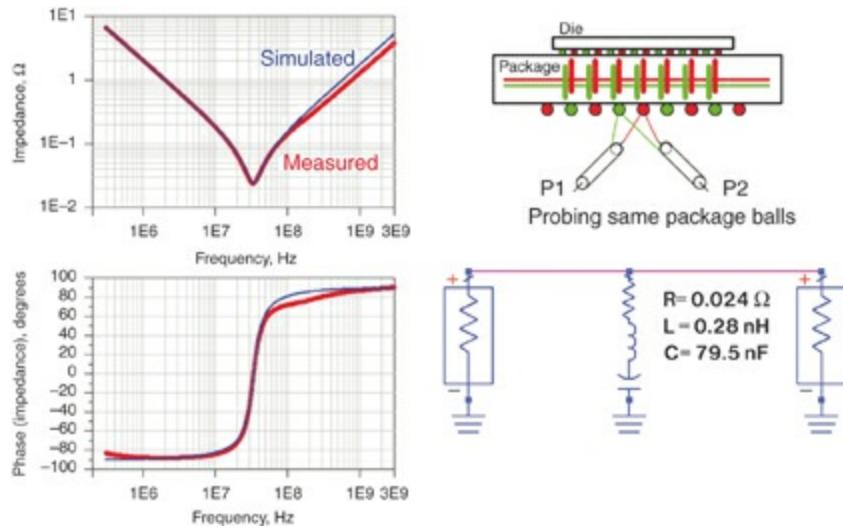
This composite structure is inherently a multi-layered 3-D planar interconnected grid and can be best interpreted by a 3-D field solver. However, we can gain a few glimmers of insight by inspecting the measured results more closely.

When the probes are on the same solder ball pair, the impedance is sensitive to the inductance and resistance of the package solder balls and vias. The DUT includes a single path to the package planes and the impedance of the ball pair might dominate the high-frequency portion of the measurement.

When the probes are on different solder ball pairs, the impedance is less sensitive to the single ball pair and more sensitive to the multi-layer planar composite structure. The two ball pairs are essentially a fixture to the DUT, which now begins at the package power planes. As demonstrated in [sections 3.7](#) and [3.11](#), the fixture introduces phase change to the measurement. Choices made for the port selection of the two ball pairs and their relative positions have a large effect on the measurement outcome.

Based on the shape of the impedance curve, seeing a good match to a simple series RLC circuit model for the

measured impedance would not be surprising. [Figure 3.45](#) shows the case of probing on the same balls, the match between the RLC model, and the measured impedance.



**Figure 3.45** Comparing the measured impedance profile of the package with two ports on the same solder ball pair and the simulated impedance of a simple RLC circuit.

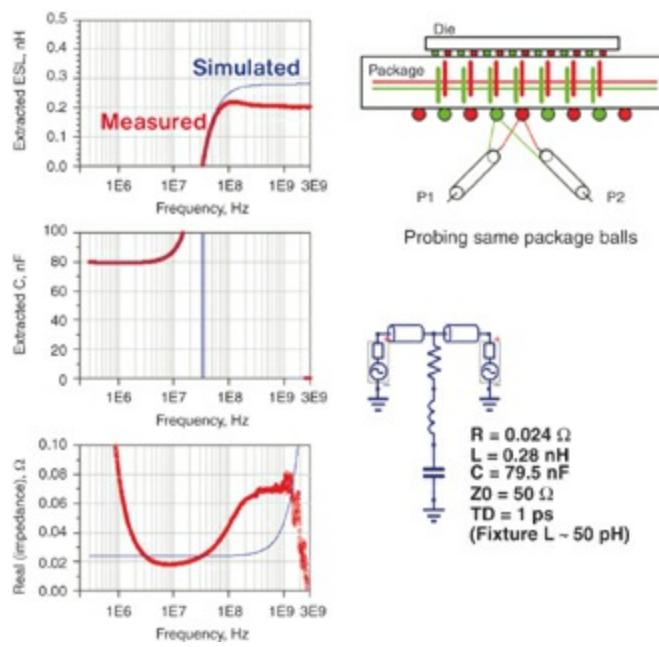
The agreement at low frequency is excellent. For this specific die in this package, the on-chip capacitance for this rail is 79.5 nF. This is close to the 80.5 nF measured from the die bumps in the on-die capacitance example shown in [Figure 3.41](#) for a similar but physically different die.

The match between the measured and simulated impedance near the self-resonant frequency using a value of 24 m $\Omega$  and 0.28 nH is also excellent. Above about 100 MHz the measured inductance decreases with frequency. This suggests that the simple RLC model might not be sufficient to describe the low resistance of the package planes shorting the higher resistance and lower inductance of the on-die grid.

More current might possibly be traveling through the low inductance and high resistance of the die. Or, it might be that current at high frequency does not travel

as far to find low impedance capacitance as it did at the series resonant frequency. When the current passes through less interconnect on-die to find the capacitance, it passes through fewer on-die shunt resistors. Both of these effects result in an increase in ESR with frequency.

Assuming a series RLC circuit model, we calculate the equivalent C and L values from the measured imaginary part of the impedance. The real part of the impedance has information about the resistive part of the impedance. [Figure 3.46](#) shows the calculated R, L, and C values from the measured impedance at each frequency point, together with the simulation results for an RLC circuit with optimum parameters.



**Figure 3.46** Extracted R, L, and C values at each frequency point from the measured impedance compared to the simulated results using the circuit parameters shown.

The extracted capacitance from both the measured impedance and the simulated model are in good agreement at low frequency. However, the extracted inductance from measurement shows a drop off with frequency. This is consistent with the inductance

decreasing with frequency, possibly related to the shunting of the inductance by the die or the shorter current path through the on-die grid.

The real part of the measured impedance shows a frequency dependence at low frequency. This is consistent with the possible dielectric loss from the insulation on-die.

Plotted on the same graphs are the simulated R, L, and C elements of the optimized circuit model but with the addition of the fixture model to represent the residual uncalibrated contribution of the probes. The fixture is modeled as a transmission line with a 1 ps electrical length. This gives an indication of the impact of the fixture in shifting the phase of the imaginary part of the impedance into the real part.

In this measurement, the probes could contribute an artifact to the extracted resistance at the high-frequency limit around 1 GHz. This example demonstrates that the increase in resistance starting at 10 MHz is not due to a fixture artifact and neither the inductance nor capacitance are very sensitive to the fixture.

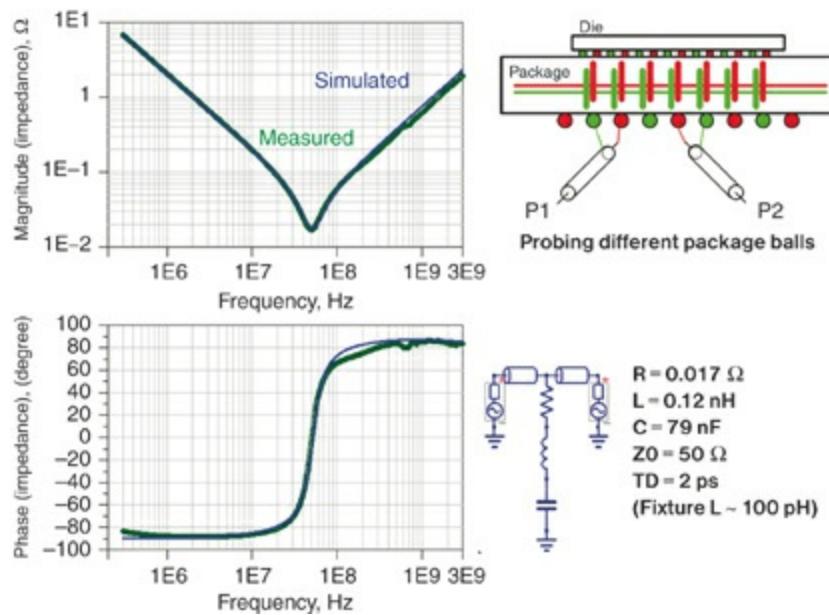
**Tip**

By introducing a short transmission line model for the fixture, we can estimate the impact on the extracted R, L, and C values to determine whether the fixture could account for the observed behavior.

This simple model including a short transmission line as the fixture suggests that the resistive behavior above 1 GHz might be due to the microprobes shifting the phase in the negative direction. If the probes were shorter by 2 psec than when calibrated, the resistance would have dropped at 1 GHz as it appears to do in the measured impedance. This could be due to a difference in probe tip scrub between the calibration and DUT

measurement conditions.

In the second package measurement, the probes contacted different solder balls. This eliminates the series inductance of the solder balls and initial vias into the package power and ground planes and some of the package spreading inductance and resistance. It is a more sensitive measurement of the package cavity shunted by the low-inductance high-resistance distributed-capacitance of the on-die power distribution grid. [Figure 3.47](#) shows the impedance calculated from measurement at each frequency point compared to the simulated impedance of an RLC circuit.

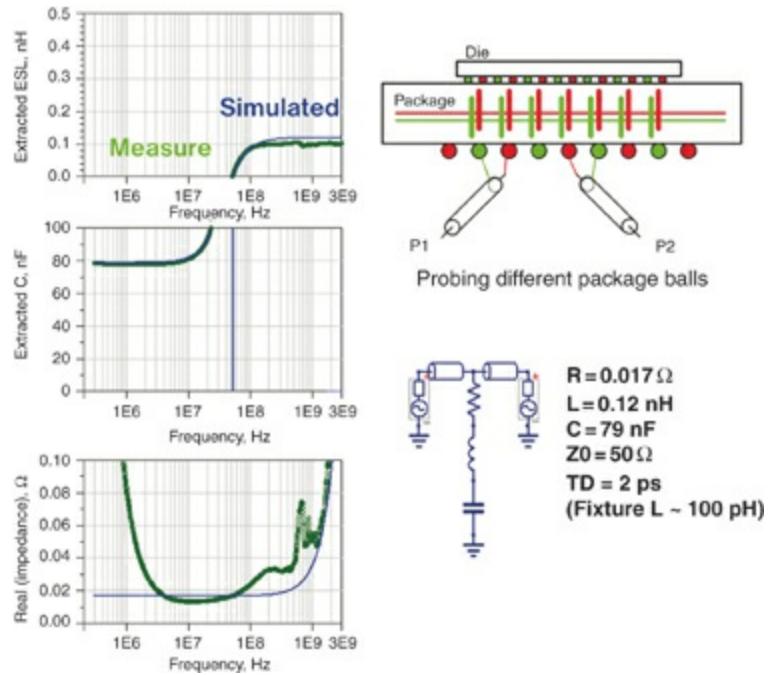


**Figure 3.47** Measured impedance of the package from two different solder ball pairs and the simulated impedance of a simple RLC circuit.

The low-frequency impedance is related to the on-die capacitance, whether measured from the die bumps or through the package. The SRF is related to the on-die capacitance and the effective inductance at that frequency. When measured from a single pair of package solder balls, the effective inductance at the SRF was 0.28 nH. When measured from two pairs of solder balls, the effective inductance was 0.12 nH.

The 0.16 nH difference is from the solder balls, initial

vias into the package's planes, and some spreading of inductance in the package planes. We gain further insight into the inductance and resistance by looking at the extracted L and R from the real and imaginary parts of the impedance, as shown in Figure 3.48.



**Figure 3.48** Extracted R, L, and C elements from the measured impedance, compared to values extracted from the simulated circuit model.

Inductance measured from the two pair of package solder balls does not vary as much with frequency as when probed from a single solder ball pair. The resistance is lower but shows an increase with frequency.

This is consistent with the lower inductance but higher resistance power grid of the die shunting the package cavity. The distance between the probe points increases the attenuation due to spreading inductance and resistance between the probed locations compared with the values when probed from the same solder ball pair.

The 160 pH of inductance contributed by each probe path through the solder balls and vias, into the package power planes, act as additional fixture inductance. In the

simulation of Figures 3.47 and 3.48, the fixture TD was increased to 2 psec corresponding to a total inductance on each end of the probes to the PDN of 100 pH. The 2 psec corresponds to the actual fixture path plus the residual non-reproducibility of the probe tip shape between calibration and DUT measurement, which we assume to be -1 psec.

The impact of this tiny value of fixture delay is to add phase to the imaginary part of the impedance and shift it into the real part, giving the appearance of frequency-dependent resistance at the high-frequency limit. This matches the measured real part of the impedance above 1 GHz. This further supports that any real part of the impedance above 1 GHz is masked by fixture artifacts and cannot be interpreted as an actual resistance. The glitches around 600 MHz might be measurement artifacts.

The behavior of the multi-layer composite structure of the distributed capacitance and low inductance and high resistance grid of the die, shunting the higher inductance and low resistance of the package, and the precise current distribution as a function of frequency make modeling this structure tricky.

In the frequency range below 100 MHz, typically where parallel resonances are found between the on-die capacitance and the package lead inductance, the ESR of the resonant loop might be dominated by the low resistance of the package. Above 500 MHz the ESR seen by the on-die circuitry is dominated by the higher distributed resistance of the on-die power grid as current comes from the on-die capacitance.

This is significant because not as much damping exists for the 100 MHz resonance as might have been expected from the on-die resistance measurement from the bumps. The die circuits have to go through

significant series and shunt resistance to get to the on-die capacitance that supports switching activity.

These measurements suggest that accurate representation of the impedance seen by the die above 1 GHz can only come from 3D models that take into account the distribution of connections between the die and package. This includes the low inductance and high resistance on-die and the high inductance and low resistance on-package forming a shunt, parallel path to the circuits.

Earlier in this section near [Figure 3.42](#) for on-die measurements from bump positions, we demonstrated the insertion-loss mechanism also known as transimpedance and spatial attenuation. This mechanism degrades the two-port measurement by making impedances appear smaller than they really are. A similar situation arises when selecting package balls to measure over the top of a bump array that ultimately accesses on-die capacitance. As we place port 1 and port 2 probes further away from each other, the VNA power injected by port 1 is attenuated over space and a smaller amount of signal is received at port 2. When package balls are involved we have inductive filtering and attenuation as well as resistive filtering.

At the printed circuit board level of assembly, a similar situation exists when the two ports are spaced widely apart accessing power planes at different locations. This time the attenuation comes from discrete capacitors mounted in the space between the ports rather than on-die capacitance underneath die bumps or package balls. The signal from port 1 is attenuated as it progresses across the space of the PCB and is finally measured at port 2. A temptation exists to claim low impedance or low inductance based on this kind of measurement and several products have done so. But it

is really the insertion loss associated with a two-port measurement. The PDN cannot deliver power or voltage at this artificially low impedance; it is an artifact of the measurement.

In this section, we highlighted two major problems in the interpretation of two-port measurements. We discussed them in the context of on-die capacitance but they are really general problems that must be considered whenever two-port measurements are used.

**Tip**

The two-port measurement is an insertion loss measurement. Uncalibrated extensions of the probes contribute a phase change that can easily change the DUT from a real to an imaginary impedance and vice versa. Also, spatial attenuation between the probes can make the impedance measurement artificially low and the DUT appear to have reduced inductance or impedance.

We must carefully interpret two-port measurements to guard against these two problems.

### 3.15 THE BOTTOM LINE

1. One popular definition of impedance is the ratio of the voltage across a device to the current through it. This is a universal definition and is always correct. However, it is not the only definition.
2. A second equally correct definition of impedance, applied specifically in the frequency domain, relates to the reflection coefficient of a sine wave from one port to the input of a DUT. This general definition applies to discrete as well as distributed structures up to very high frequencies.
3. Impedance is measured to very high frequency with a one-port VNA using the definition based on the reflection coefficient. However, accuracy of this technique is limited to impedances above about 0.1

$\Omega$ .

4. Remarkably, simple models of a few ideal circuit elements can be combined together to match the measured impedance of real physical structures. This makes characterization of complex systems in terms of a few ideal circuit elements straightforward.
5. To get around the accuracy and DUT impedance limitations of one-port VNA measurements, we use two-port VNA measurements. This is similar to four-lead Kelvin measurements where one port forces the current into the DUT and the other port measures the voltage response. We can measure very low impedances to very high frequency with this technique.
6. To first order the impedance of a device is  $25 \Omega \times S_{21}$  in a two-port measurement, where the low impedance DUT is in shunt with port 1 and port 2.
7. One important artifact to avoid in two-port low impedance measurements is the phase shift introduced by the time delay of the fixture. We can de-embed this from the measurement or include it in the circuit topology used to model the DUT.
8. Another important artifact of two-port measurements is impedance or inductance appearing smaller than it really is. This is because the two-port measurement is really an insertion loss measurement. If the two ports are spatially separated across the DUT, attenuation might impact the interpretation of the measurement.
9. We can use the two-port technique to measure the mounting inductance of discrete capacitors and extract their capacitance, equivalent series resistance, and equivalent series inductance.

10. We can also use the two-port technique to measure the on-die capacitance. The extracted impedance can be fit to an RLC circuit model through simulation, or the imaginary part of the impedance can be fit to a simple LC model and the capacitance extracted with simple algebra from the imaginary component for each measured frequency point.
11. Interpreting the two-port impedance profile of a die through a package can be tricky because it depends on the distributed nature of the spreading resistance, shunt resistance, and spreading inductance of the package and power grid on the die. Interpreting the details of the impedance profile in terms of a 3-D simulation of the combined power distribution networks is best.

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# Chapter 4. Inductance and PDN Design

## 4.1 WHY DO WE CARE ABOUT INDUCTANCE IN PDN DESIGN?

The goal for the power distribution design is to meet a target impedance profile. We can simulate impedance with the right models for the components and interconnects of the PDN, and model all interconnects as transmission line segments, which can themselves be approximated as L and C elements at low enough frequency. The L, or inductance, of a signal conductor and its return path conductor is a fundamental electrical description that applies to all interconnects. We can also approximate other discrete components with L and C elements.

Inductive properties dominate impedance of real interconnects, especially at high frequency. Even at low frequency, the interaction of the effective inductance of the VRM and the capacitance of the bulk capacitors determines a parallel resonance peak in the PDN. At intermediate frequencies, parallel resonances and their associated peaks arise from capacitive and inductive properties of real capacitor elements. The loop inductance of the interconnect structures including capacitors, planes, and vias dominate the impedance at high frequency.

Reducing the inductance of the PDN is one of the most important steps in reducing impedance at high frequency and peak impedances throughout the frequency range. Engineering lower inductance is the key to balancing performance and cost. This is especially true when there is no incremental cost to designing lower inductance structures. Knowledge of inductance is an essential ingredient to cost-effective design.

**Tip**

Inductance is arguably the most important electrical property of a PDN element. Higher values will increase the peak impedance in parallel resonances and is the dominant term that sets the lowest impedance at high frequency. Reducing the inductance of PDN elements by design is one of the most important ways of improving performance, sometimes with little cost.

A significant problem for design engineers is that inductance is one of the most confusing topics in signal integrity and yet one of the most important. It is confusing because it is complicated and many of the terms associated with inductance are misunderstood and incorrectly used in the industry, messing up our intuition.

Many good text books are available on inductance [1]–[5]. This chapter focuses on building strong engineering intuition and a solid foundation in mastering inductance.

## 4.2 A BRIEF REVIEW OF CAPACITANCE TO PUT INDUCTANCE IN PERSPECTIVE

Understanding inductance is much simpler if we first rethink capacitance. Just as every signal and return-path conductor-pair has inductance associated with it, each pair of conductors also has an associated capacitance.

The basic definition of capacitance is that it relates the charge separation between two conductors to a voltage difference between the conductors, as

$$C = \frac{Q}{V} \quad \text{and} \quad Q = CV \tag{4.1}$$

where

$C$  = the capacitance between the conductors, in F

$Q$  = the charge on each conductor in Coulombs

$V$  = the voltage between the conductors, in volts

Capacitance is not a measure of the difference in charge on a pair of conductors. If the equal and opposite charges on two conductors doubles, the capacitance stays the same. Of course, the voltage between them doubles. The ratio of the charge to the voltage stays the same.

Capacitance is a measure of the efficiency of storing charge between conductors at the cost of voltage. A pair of conductors with a high capacitance means we can dump excess charge on each conductor with a small voltage increase. The conductors are efficient at storing charge with little voltage cost. Likewise, a small capacitance means a small capacity to store charge at the cost of voltage. Not much excess charge can be added to the conductors before the voltage is increased a lot.

**Tip**

Capacitance is a direct measure of the efficiency of a pair of conductors for storing charge at the cost of voltage. A large capacitance means conductors are good at storing charge at little cost of voltage.

In this respect, the capacitance between two conductors is about the geometry of the conductors and the distribution of dielectric materials around the conductors. It is not about the voltage between the conductors but the ratio of charge to voltage.

The two important physical design features that influence capacitance are the overlap area of the two conductors and the spacing between them. An additional factor influencing capacitance is the dielectric constant of the material between the plates. If no voltage difference exists between the two conductors, there is no excess charge difference. They still have the same capacitance as they would if there were enough charge

to increase their voltage to 1 kV.

Distinguishing between the terms *capacitance*, *charge*, and *voltage* is important. Capacitance depends only on the geometry of the conductors and the dielectric materials. It is constant no matter what voltage is applied across the capacitor. Charge and voltage are external properties of the capacitor. They can have any value without affecting the capacitance.

The impedance of a capacitor is related to the ratio of the voltage across it to the current through it. To derive the current through a capacitor, we take the derivative of both sides of Equation 4.1 and arrive at:

$$I = \frac{dQ}{dt} = C \frac{dV}{dt} \quad (4.2)$$

Taking the ratio of the voltage to the current, we end up with the impedance of a capacitor in the time domain:

$$Z = \frac{V}{I} = \frac{V}{C \frac{dV}{dt}} \quad (4.3)$$

This is a perfectly correct relationship; it's just complicated. The impedance of a capacitor in the time domain depends on the precise waveform of voltage across the capacitor. In the time domain, the impedance of a capacitor is not intrinsic to the capacitor itself.

In the frequency domain, the impedance has a simpler form. In the frequency domain, currents and voltages are sine waves, described in the time domain as

$$\begin{aligned} \tilde{I} &= I_0 \exp(j\omega t) \quad \text{with} \quad \frac{d\tilde{I}}{dt} = j\omega \tilde{I} \\ \tilde{V} &= V_0 \exp(j\omega t) \quad \text{with} \quad \frac{d\tilde{V}}{dt} = j\omega \tilde{V} \end{aligned} \quad (4.4)$$

where

The squiggles over the terms denote complex numbers

$I_o$  = the amplitude of the current

$V_o$  = the amplitude of the voltage

$\omega$  = the angular frequency in radians/sec

This transforms the impedance in the frequency domain to

$$\tilde{Z} = \frac{\tilde{V}}{\tilde{I}} = \frac{V}{C \frac{dV}{dt}} = \frac{\tilde{V}}{C j \omega \tilde{V}} = \frac{1}{j \omega C} = \frac{-j}{\omega C} \quad (4.5)$$

In the frequency domain, the impedance of an ideal capacitor has a very simple form and is also extrinsic, depending on the frequency of the applied voltage.

**Tip**

The impedance of a capacitor in the time domain is just as valid as the impedance in the frequency domain. However, it is much more complicated in the time domain and depends on the specific voltage waveform across the capacitor. In the frequency domain, the impedance of a capacitor is just as valid, but it has a much simpler form.

## 4.3 WHAT IS INDUCTANCE? ESSENTIAL PRINCIPLES OF MAGNETIC FIELDS AND INDUCTANCE

Loop inductance is defined from the fundamental relationship of magnetic flux to current, as

$$L_{loop} = \frac{\Psi_{loop}}{I} = \frac{1}{I} \iint_{closed \text{ area}} \bar{B}(x, y) \bullet d\bar{a} \quad (4.6)$$

where

$\Psi_{loop}$  = the total number of magnetic flux lines passing through the loop

$I$  = the current in the loop

$B(x,y)$  = the magnetic field density everywhere on the surface of the loop area

$da$  = a small piece of loop area

and the integral is over the entire loop's surface area.

This definition of inductance is confusing because it is shrouded behind a surface integral of the non-uniform magnetic field density over an area. The magnetic field density distribution depends strongly on the specific size and shape of the loop and the current in it.

This complicated definition, coupled with the confusing and obtuse descriptions of inductance offered in the literature, some of which are just wrong, make inductance the most important and at the same time, most poorly understood term in signal and power integrity.

There is a simple way of thinking about inductance by using the description of capacitance in the previous section as the launching point. Just as capacitance is a measure of the efficiency of two conductors for storing charge at the price of voltage, inductance is a measure of the efficiency of a conductor loop in storing magnetic field lines at the cost of the current in the loop.

**Tip**

The fundamental definition of inductance is that it is the efficiency of conductors to create magnetic field lines at the cost of current. Inductance is not a measure of the total number of magnetic field lines; it is a measure of the efficiency of the conductors to create magnetic field lines.

To use this definition of loop inductance, we must understand not only the properties of magnetic field lines but also how the current distribution in a conductor creates magnetic field lines. We can

summarize the complicated mathematics of how currents generate magnetic field lines and how magnetic field lines contribute to inductance in six essential principles of magnetic fields. Understanding these essential principles can help to minimize confusion:

1. In nature, magnetic field lines only appear as closed rings.
2. Any current creates concentric rings of magnetic field lines around it that have a specific direction of circulation around the current.
3. Magnetic field lines do not interact with dielectric materials.
4. The total number of rings of magnetic field lines that surround a conductor is directly proportional to the current through the conductor.
5. If the number of field line rings around a conductor changes, for whatever reason, a voltage will be generated across the conductor.
6. Energy is stored in the magnetic field lines. The higher the number of field lines, the more energy in the magnetic field.

**Tip**

A secure understanding of the preceding six principles of inductance is an essential skill for designing physical structures with controlled inductance.

Because magnetic field lines appear only as rings, they can be individually counted. In SI units, the International System of Units, the number of rings of magnetic field lines is counted in units of Webers of field lines. In cgs units, we use units of Maxwells to count the number of rings of magnetic field lines, with

$$1 \text{ Weber} = 10^8 \text{ Maxwells} \quad (4.7)$$

where

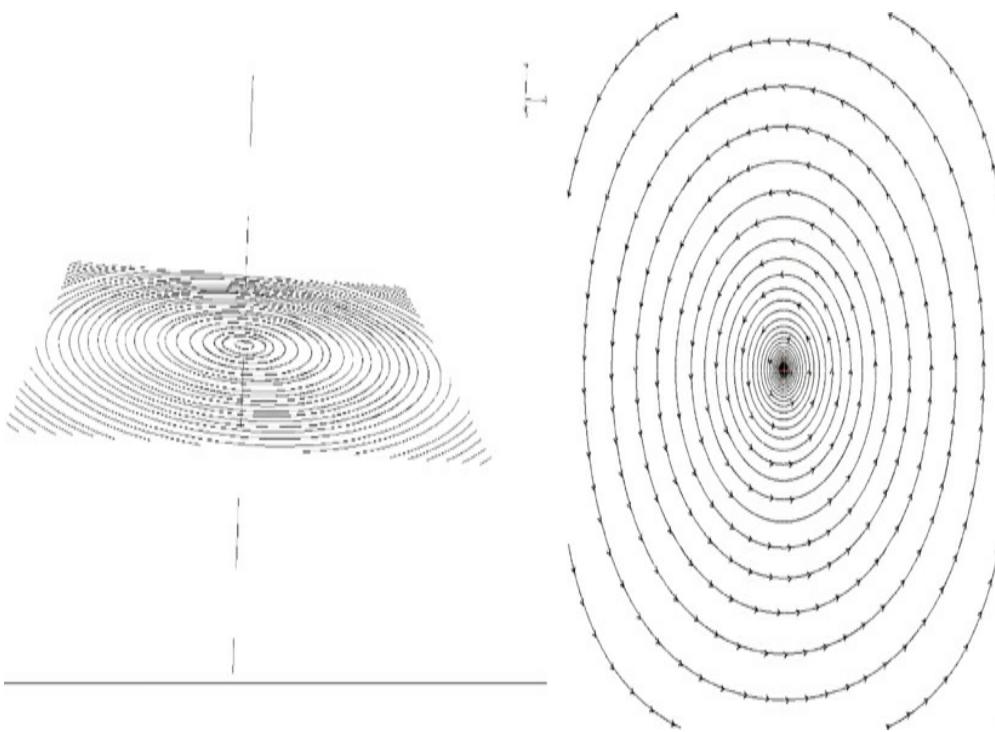
Weber = units of a quantity of rings of magnetic field lines in SI units

Maxwells = units of a quantity of rings of magnetic field lines in cgs units

Regardless of units, the number of magnetic field line rings around a conductor is directly proportional to the current through the conductor.

This is analogous with capacitors. With capacitors, we count charge in SI-units of Coulombs, and the amount of excess charge between the conductors is directly proportional to the voltage between the conductors.

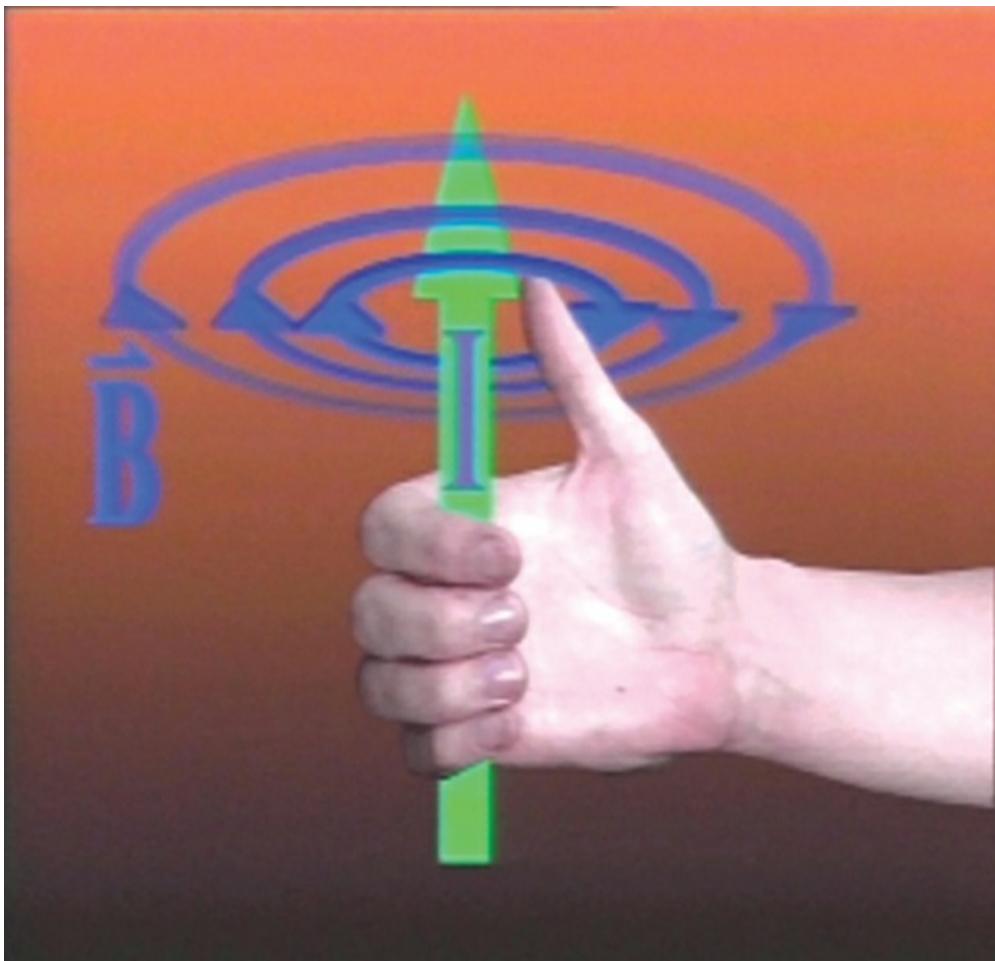
The magnetic field lines around a long uniform wire carrying a current are in the shape of concentric rings, as shown in Figure 4.1.



**Figure 4.1** Two views of the rings of magnetic field lines around a long straight wire carrying a current. In the left view, the wire is nearly straight up and the field lines are shown as centric circles around the wire. In the right view, the wire and current through it are coming out of the paper. The magnetic field lines are concentric circles around the current, decreasing in density the farther from the current. These rings are distributed up and down the length of the current carrying wire.

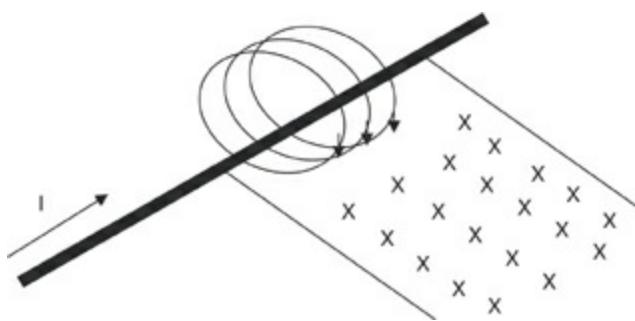
These rings of magnetic field lines appear up and down the length of the wire. At every slice perpendicular to the wire, the field lines will appear as concentric rings.

The field line rings behave as if they have a direction of circulation. The direction in which they circulate is defined by the “right-hand rule”: The thumb of your right-hand points in the direction of the positive current and your fingers curl in the direction of circulation of the magnetic field lines. This concept is illustrated in Figure 4.2.



**Figure 4.2** Direction of circulation of the rings of magnetic field lines around a wire is given by the “right-hand rule”: The thumb of your right-hand points in the direction of the current, fingers curl in the direction of circulation.

We sometimes use the Greek letter psi,  $\Psi$ , to designate the number of field line rings around a conductor, also referred to as the *flux of field lines*. Because each and every magnetic field line surrounding a conductor is part of a ring, we can count the number of rings surrounding the conductor from any position around the conductor. All we have to do is count the rings that pass through a plane that extends from the conductor to the edge of space. The total number of rings that pass through an imaginary plane adjacent to the current is the flux of field lines. This is illustrated in Figure 4.3.



**Figure 4.3** We can count the total number of field line rings surrounding the current by counting the flux of lines that pass through an area adjacent to the conductor. The crosses are the tails of the arrows showing the direction of the magnetic field lines as they pass through the plane adjacent to the wire.

The total number of field line rings surrounding the conductor is the total flux of field lines passing through this area, counting from the center of the conductor to infinity.

**Tip**

The flux of field lines is the same as the number of field line rings surrounding a conductor.

The fundamental definition of inductance is based on the number of field line rings that completely surround the conductor per amp of current through the conductor:

$$L = \frac{\Psi}{I} \quad \text{and} \quad \Psi = LI \quad (4.8)$$

where

$L$  = inductance in Webers/Amp = Henrys

$\Psi$  = the flux of field line rings around a conductor in Webers

$I$  = current through the conductors in Amps

Although capacitance is a measure of the efficiency of storing excess charge for a given voltage, inductance is a measure of the efficiency of generating rings of

magnetic field lines at the cost of the current. The more rings of magnetic field lines that are generated per Amp of current, the greater the efficiency of generating field line rings and the higher the inductance of the conductor configuration.

A conductor configuration that has a high efficiency at generating many Webers of field line rings for a small amount of current has a large inductance. A conductor design that has a low efficiency at generating field line rings has a small inductance.

Inductance is not about the number of field line rings around the conductor. If there is 1  $\mu$ A or 1 MA of current through the conductor, the number of rings of magnetic field lines dramatically changes, but the inductance of the conductor does not. Even if there is no current through a conductor, it still has the same inductance.

**Tip**

Inductance is a property of the geometry of the conductor and not about the current through the conductor.

If the flux of field lines is measured in units of Webers of field line rings and the current through the conductor is in units of amps, then inductance, as a measure of the total number of field lines per amp of current, has units of Webers/Amp. In SI units, these have the special name of Henrys. Because many applications in signal integrity involve tiny inductances, a more convenient set of units is the nanoHenry abbreviated as nH, or even picoHenry abbreviated as pH.

Inductance is rarely measured in cgs units. This is partly because multiple sets of cgs units exist. In ElectroMagnetic Units (EMU) cgs units, inductance is described by the abHenry, and current is described by the abAmp. The conversion is

$$1 \text{ Amp} = 0.1 \text{ abAmp}$$

(4.9)

$$1 \text{ Henry} = 1 \text{ Weber/Amp} = 10^8 \text{ Maxwells}/0.1 \text{ abAmp} = 10^9 \text{ abHenrys} \quad (4.10)$$

We introduce abHenrys here only for completeness and they will not be discussed again. Inductance is confusing enough without adding another set of units that are hardly ever used.

If the current doubles, the number of rings of magnetic field lines around the conductor doubles but the inductance stays the same. Inductance is an intrinsic property of the conductors and only depends on the geometry of the conductors. Because magnetic field lines do not interact with dielectrics, the distribution of dielectric materials around conductors will in no way influence the number of magnetic field lines and will not affect the inductance of the signal and return path conductors.

Technically, this is not quite true. There is a slight impact on magnetic field lines from dielectrics. These properties are described as diamagnetic or paramagnetic properties, depending on whether the dielectric material decreases or increases the number of field line rings. In all insulating dielectrics, except those considered as ferrites, the impact of the dielectric on the magnetic field is much less than 0.01%. On a practical basis, dielectric materials are transparent to magnetic field lines and they do not interact with magnetic fields at all.

**Tip**

On a practical basis, dielectric materials, with the exception of ferrites, are transparent to magnetic field lines and they do not interact with magnetic fields at all.

One interesting dielectric material is ferrite, a ceramic

composed of iron oxide and typically one or two other metal oxides such as zinc, nickel, manganese, or strontium. These materials have a high permeability and dramatically increase the inductance of any conductor they are wrapped around. The condition for highest inductance is that the rings of magnetic field lines from the enclosed current be wholly contained in the high permeability ferrite. The ferrite must completely surround the current.

This property makes them ideal for increasing the inductance (and impedance) seen by common currents on cables. In this application they are often called “common mode chokes” because they help decrease the common currents flowing on external cables connecting to the power line or to peripheral devices, thereby decreasing radiated emissions from products.

Ferrite materials are also used in discrete inductor elements where higher inductance in a small volume is needed with the added advantage of high-frequency loss.

Where lower inductance is required, ferrites are never used.

With only three exceptions, magnetic fields do not interact with the conductive material through which the current travels. These three exceptions are the ferromagnetic metals: iron, nickel, and cobalt, or alloys containing them. These metals and alloys can be high permeability and increase the inductance of conductors composed of them. However, only the internal self-inductance is affected by the permeability of the conductor. See [section 4.9](#) for more details.

With the exceptions noted previously, only the geometry of the signal and return path conductors influence the inductance of the pair of conductors. As we will show in detail, only three general geometry features influence inductance:

- 1. Length:** Shorter length, lower inductance
- 2. Cross-sectional area:** The more the current spreads out, the lower the inductance
- 3. Distance between signal and return conductors:** The closer the spacing, the lower the inductance

## 4.4 IMPEDANCE OF AN INDUCTOR

The electrical properties of inductors are based on the definition of inductance and one more principle: If the number of rings of magnetic field lines around a conductor changes, a voltage is generated. This is Faraday's Law of Induction, one of Maxwell's Equations, usually written as

$$V = \oint E \cdot d\vec{l} = -\frac{d}{dt} \iint_{\text{closed area}} \bar{B} \cdot d\vec{a} \quad (4.11)$$

In words this says, a voltage, which is the line integral of the  $E$  field dotted along the line segment of a path, is created by the rate of change of the total number of magnetic field lines enclosed by the path.

In our simplified perspective, the following terms describe this relationship, which Figure 4.4 illustrates:

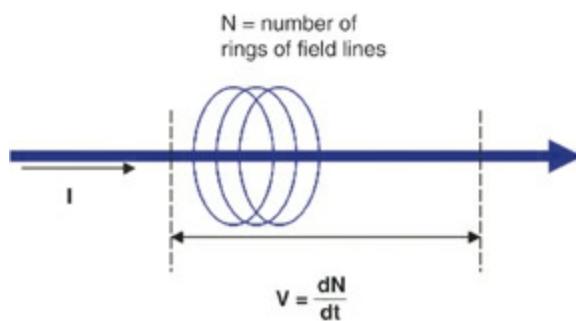
$$\Delta V = \frac{d\Psi}{dt} \quad (4.12)$$

where

$\Delta V$  = the voltage difference generated between the ends of a conductor

$d\Psi$  = the small change in the number of rings of magnetic field lines around the conductor

$dt$  = the small time interval in which the number of rings are changing



**Figure 4.4** A voltage difference is induced between the ends of a conductor when the number of field line rings around it changes, for any reason.

One way the number of rings of magnetic field lines around a conductor can change is if the current through the conductor changes. If the current increases, the number of rings around it increases. How fast the number of rings change determines the voltage generated across the ends of the loop. Another way of considering this property is a voltage applied across the conductor drives a changing current, which changes the number of field line rings.

From this expression and the definition of inductance, we derive the I-V properties of an inductor as

$$\begin{aligned} \Psi &= LI \\ \Delta V &= \frac{d\Psi}{dt} = L \frac{dI}{dt} \quad \text{or} \quad \Delta V = L \frac{dI}{dt} \end{aligned} \tag{4.13}$$

This is the familiar definition of an inductor. The voltage across an inductor is instantaneous with the current change through it. We can interpret this in two equivalent ways. A voltage generates across the inductor when the current through it changes. This voltage generated from the changing current is also sometimes referred to as the *back emf* (electromotive force).

For the second interpretation, a changing current through the inductor is generated by applying a voltage difference across its ends, neglecting the resistive properties of the conductor. This is an alternative way of considering the relationship between the voltage across

the conductor and the changing current in it. The two effects happen simultaneously.

In Chapter 9, where we discuss the role of interconnect structures influencing the currents through the PDN, we will see this description of a voltage difference driving a changing current is a useful perspective.

**Tip**

Although the common interpretation of the definition of inductance is that it's a changing current that generates the voltage across the conductor, reinterpreting this as a voltage drop across the conductor drives a changing current through the conductor can help to interpret the role of chip-attach inductance.

In the time domain, the impedance of an inductor,  $Z$ , is still based on the definition of impedance:

$$Z = \frac{V}{I} = \frac{L \frac{dI}{dt}}{I} \quad (4.14)$$

Although this is a perfectly correct description of the impedance of an inductor and matches our expectations, it is a complicated format and illustrates that in the time domain, the impedance of an inductor depends on the precise shape of the current waveform through it. As with a capacitor, the description of the inductor's impedance is much simpler in the frequency domain.

In the frequency domain, with all signals as sine waves, described in an exponential form, the relationship between the voltage across an inductor and a changing current is

$$\tilde{V}(\omega) = L \frac{d\tilde{I}(\omega)}{dt} = j\omega L \tilde{I}(\omega) \quad (4.15)$$

where the tilde over the  $V$  and the  $I$  denotes complex elements.

We derive the impedance of an inductor in the frequency domain by

$$\tilde{Z}(\omega) = \frac{\tilde{V}(\omega)}{\tilde{I}(\omega)} = \frac{j\omega L \tilde{I}(\omega)}{\tilde{I}(\omega)} = j\omega L \quad (4.16)$$

This relationship illustrates the general problem caused by an inductor: Its impedance increases with frequency. At a higher frequency, an interconnect's impedance will often be dominated by its conductors' inductance. This is why minimizing inductance is a significant part of PDN design.

Generally, an interconnect's inductance is constant with frequency. A slight frequency dependence might exist due to current redistribution. This effect causes the inductance to decrease slightly with frequency. Don't confuse the inductance with its impedance.

**Tip**

The inductance of an inductor is mostly constant with frequency. An inductor's impedance always increases with frequency. This is why minimizing inductance is such a significant part of PDN design.

## 4.5 THE QUASI-STATIC APPROXIMATION FOR INDUCTANCE

The very nature of the complex behavior of magnetic fields and currents complicates the connection between physical design and inductance.

A change in the electric or magnetic fields in one region of space propagates at the speed of light to all other regions of space. This is, after all, the nature of electromagnetic radiation. To describe these effects requires all four of Maxwell's Equations, their time and spatial variation, and accounts for the propagation of fields in free space.

However, if we make a simplifying assumption, we

can dramatically reduce the complexity of Maxwell's Equations to a more easily managed level. If we restrict attention to a region in space in which the time for propagation is short compared to the period of a cycle, the phase of the radiation is the same everywhere over the problem area and we can ignore the propagation effects.

The phase being constant over the region of space of interest does not mean the fields are the same everywhere. It means the field distribution is static over space.

This is often called the *quasi-static approximation*. When we lift the quasi-static restriction, we refer to the solution of the problem as a full-wave solution, which includes propagation effects and arbitrary sizes of conductors. In a full-wave solution, the physical size of the problem area can be unrestricted.

**Tip**

The quasi-static approximation assumes there is no time-varying change in the magnetic field strength over the region of the space around the problem, or that the wavelength of the highest frequency components of the changing field is very long compared to the largest physical extent of the device. This approximation dramatically simplifies the calculation of magnetic fields.

With the flexibility of dealing with any size problem comes a much higher level of complexity in a full-wave solution: We require more complex tools to deal with practical problems and need more time to arrive at a solution. The advantage of using a quasi-static solution is a shorter time to an answer, with the restriction that the problem size must be small compared to a wavelength of the highest frequency of interest.

We can describe the condition for a valid quasi-static solution in three equivalent ways:

1. When the variation in the phase of the time-varying fields is very small over the problem area (less than 1/20 a cycle)
2. When the physical size of the problem area is small compared with the wavelength of the shortest wave (less than 1/20 a wavelength)
3. When the time delay across the problem area is short compared to the period of oscillation of the field (less than 1/20 the period)

As a rule of thumb, the condition for a valid quasi-static approximation for an interconnect structure is that the physical size of the structure is less than 1/20 the wavelength of the highest frequency of interest; or the time delay through the structure is shorter than 1/20 the period; or the phase delay through the structure is less than  $360/20 = 18$  degrees. If you are worried about whether this should be 1/10 or 1/20, you should not use a quasi-static approximation, but a full-wave solution.

The following equation describes the condition for 1/20 a wave to be the size of the largest structure dimension for which a quasi-static solution can apply

$$\text{Len} < \frac{v}{f} \times \frac{1}{20} \quad (4.17)$$

where

$\text{Len}$  = the length of the object, in meters

$v$  = the speed of light in the medium surrounding the object in m/sec

$f$  = the frequency at which the fields are changing in Hz

In air, the speed of light is about 12 inches/nsec, so the limit on the length being shorter than 1/20 the wave length is about

$$\text{Len[inches]} < \frac{v[\text{inches/nsec}]}{f[\text{GHz}]} \times \frac{1}{20} = \frac{12}{f} \times \frac{1}{20} = \frac{0.6}{f[\text{GHz}]} \quad (4.18)$$

Likewise, based on a physical length of a structure in air, the highest frequency for which the quasi-static approximation would apply is roughly

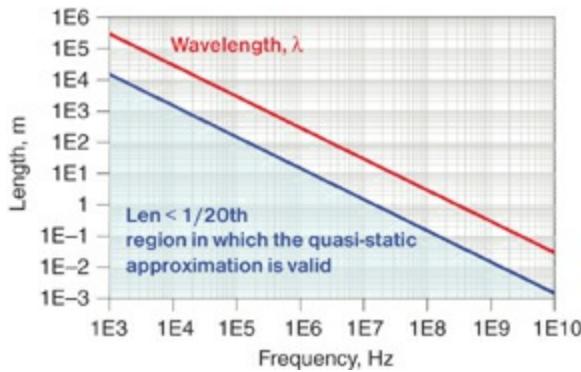
$$f[\text{GHz}] < \frac{0.6}{\text{Len[inches]}} \quad (4.19)$$

For example, if the physical size of a structure is 1 inch, the quasi-static model would apply up to about 0.6 GHz.

**Tip**

As a general rule of thumb, in air the quasi-static approximation should apply up to about 0.6 GHz for a structure that is roughly 1 inch in extent. The frequency limit scales inversely with physical length.

Figure 4.5 shows this relationship compared with the wavelength of the light for the case of the structures surrounded by air, with a dielectric constant  $D_k$  of 1 and a speed of light of 12 inches/nsec = 30 cm/nsec = 0.3 m/sec.



**Figure 4.5** Quasi-static approximation is valid when the physical length of the structure < 1/20 a wavelength, when the structure is surrounded by air.

From the graph, we see that at 1 GHz, we can approximate physical structures as large as 0.01 m or 1 cm as lumped circuit elements and the quasi-static

approximation will be valid. This means that modeling discrete capacitors as lumped RLC elements using the quasi-static approximation is still valid, even above 1 GHz.

When the structure is embedded in a dielectric material like FR4, the speed slows down by a factor of 2 and the highest frequency for the quasi-static model to apply decreases by a factor of 2:

$$f[\text{GHz}] < \frac{0.3}{\text{Len}[\text{inches}]} \quad (4.20)$$

A typical circuit board that might be 12 inches or 30 cm on a side begins to show full-wave effects at frequencies above about 30 MHz. This is why the electrical properties of the power and ground planes in a board, above about 30 MHz, must include the full-wave and propagation effects. This is ultimately the origin of resonances in the power and ground cavities.

**Tip**

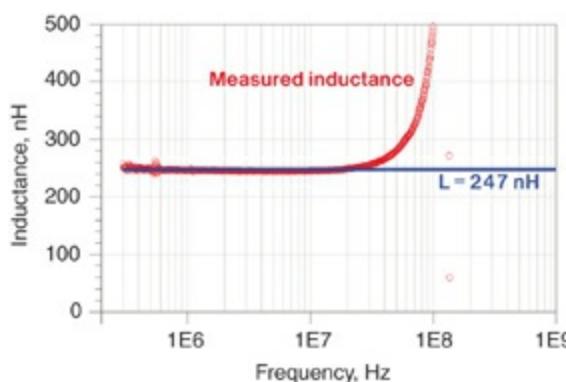
Although we can approximate discrete capacitors with a quasi-static approximation at 1 GHz and above, large boards require a full-wave solution at frequencies above about 30 MHz. The full-wave analysis is needed to predict the resonances in power and ground plane cavities.

As an example of the validity of the quasi-static approximation, [Figure 4.6](#) shows a simple circular loop of 18-gauge, 49 mil OD copper wire, about 10 cm in diameter, surrounded by air. It has a circumference of about 0.3 m or 12 inches. As predicated from the graph in [Figure 4.5](#), we expect full-wave effects to begin to play a role at a frequency of about  $0.6/12 \text{ inches} = 50 \text{ MHz}$ .



**Figure 4.6** Close up of 10 cm diameter loop of 18-gauge wire set up for measurement with the two-port technique.

Its impedance was measured using a VNA and the two-port technique described in the [Chapter 3](#). From the impedance, we extracted the inductance and plotted it as a function of frequency in [Figure 4.7](#).



**Figure 4.7** Measured inductance for 10 cm diameter loop of wire, compared to the inductance of an ideal inductor. The real inductor matches the ideal inductor up to about 40 MHz to better than 10% and up to 60 MHz to better than 20%, beyond which full-wave effects affect the extracted inductance.

We expect the inductance of the loop of wire to be constant with frequency until the full-wave effects make the lumped circuit model an inaccurate approximation for this structure. The condition for the physical size less than  $1/20$  a wave is for frequencies below about 50 MHz. In this specific example, the lumped circuit model is accurate to better than 10% up to 40 MHz and better than 20% up to 60 MHz.

After we introduce the approximation for the inductance of a circular loop later in this chapter, we compare the loop's measured inductance with the calculated loop inductance. These values will be surprisingly close.

## 4.6 MAGNETIC FIELD DENSITY, $\mathbf{B}$

In the quasi-static approximation, magnetic field lines around a current are in the form of closed rings whether the current is constant or changing. We describe the field lines themselves in terms of the flux of field lines. However, referring to the magnetic field line density, rather than the field lines themselves, is more common. The magnetic field line density is the number of magnetic field lines, or the flux of field lines, that pass

through a small area, per unit area. The letter  $B$  is usually used to denote the magnetic field density and it is defined as

$$B = \frac{d\Psi}{da} \quad (4.21)$$

where

$B$  = the field density in Webers/m<sup>2</sup>

$d\Psi$  = the small number of Webers of field lines, or flux, that passes through the small area

$da$  = the small area through which the field lines are passing

In the limit as  $da$  becomes vanishingly small, the magnetic field density is defined at every point in space.

In SI units, the magnetic field line density is Webers of field lines/m<sup>2</sup>. This has the special name of Tesla, as a unit of magnetic field density. In cgs units, the magnetic field density is Maxwells of field lines per cm<sup>2</sup>. This has the special name of Gauss.

The connection between the magnetic field density units of Tesla and Gauss is

$$1 \text{ Tesla} = 1 \text{ Weber/m}^2 = 10^8 \text{ Maxwells}/(10^4 \text{ cm}^2) = 10^4 \text{ Gauss} \quad (4.22)$$

Referring to  $B$  as the magnetic field is misleading and a major source of confusion. It is a field density, a measure of the number of field lines that pass through a narrow area of space per unit area. We choose the region of space,  $da$ , to be so small that the density of flux lines passing through this region is constant over the area.

**Tip**

Referring to  $B$  as the magnetic field is misleading and a major source of confusion. It is not really the magnetic field, but the density of magnetic field lines that pass through a small area. The field density is not the same as the number of field lines.

For example, we often refer to the Earth's magnetic field as 0.5 Gauss, or  $5 \times 10^{-5}$  Teslas or  $5 \times 10^{-5}$  Webers/m<sup>2</sup>, or 50  $\mu$ Tesla. To be correct, and less confusing, we should refer to the Earth's magnetic field *density* near the equator to be 0.5 Gauss or 50  $\mu$ Tesla. The Sun's magnetic field density is more complicated than the Earth's. The overall dipole component is on the order of 1 Gauss, but at sunspots, can be as large as 5,000 Gauss.

As coronal mass ejections (CMEs) spread outward from the Sun, the CME plasma can carry magnetic field lines with it, which can have field densities on the order of 1 Gauss. When the charged particles in the CME plasma hit the Earth, the Earth's magnetic field deflects them to the poles. However, if the entrapped solar magnetic field density is on the order of 1 Gauss and oriented opposite to the Earth's magnetic field, the trapped solar magnetic fields can cancel the Earth's field and let the charged particles through. These are occasions of larger auroras and, if they are large enough CMEs, can disrupt power grids.

Table 4.1 summarizes the various units introduced so far.

Quantity	SI Units	cgs Units
Number of magnetic field lines (flux)	Webers	Maxwells
Current	Amps	abAmps
Inductance	Webers/Amp = Henry	Maxwells/abAmp = AbHenry
Magnetic field density	Webers/m <sup>2</sup> = Tesla	Maxwells/cm <sup>2</sup> = Gauss

**Table 4.1** Summary of the Units Used for Various Magnetic Quantities

Inductance is not about the magnetic field density. If a region of space exists where the magnetic field density happens to be larger than another region, this is not an indication of a potentially higher inductance. It is only the *total* number of field lines per amp surrounding a conductor that determines the inductance of the conductor.

**Tip**

Inductance is not about the magnetic field density. If a region of space exists where the magnetic field density happens to be larger than another region, this is not an indication of a potentially higher inductance. It is only the *total* number of field lines per amp surrounding a conductor that determines the inductance of the conductor.

From the field density  $B$  everywhere in space, we can calculate the total number of field lines surrounding the conductor by integrating the field density over an area that extends in the half plane from the conductor to infinity. This will count all the field line rings surrounding the conductor.

$$\Psi = \oint_{\text{area}} \bar{B} \bullet d\bar{a} \quad (4.23)$$

where

$B$  = the magnetic field density in Webers/m<sup>2</sup>

$da$  = a small area over which the field density is constant

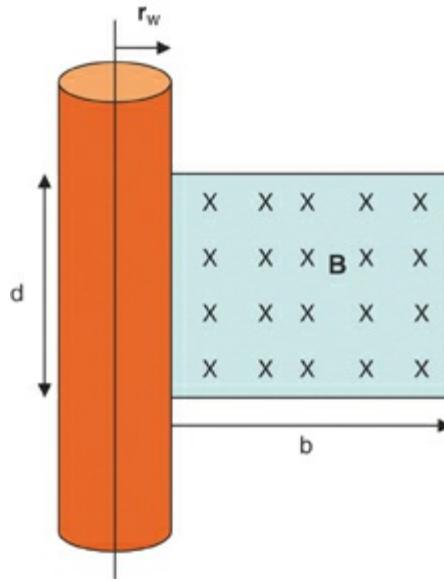
$\Psi$  = the total flux of field lines passing through the total area

The operator inside the integral is a dot product between the two vectors.

The arrows denote that the dot product includes the vector direction of the flux density and the normal (perpendicular) to the surface of the area in integrating the number of field lines that pass through the area. From this definition of the flux, we can define the inductance more traditionally as

$$L = \frac{\Psi}{I} = \frac{1}{I} \iint_{\text{area}} \bar{B} \cdot d\bar{a} \quad (4.24)$$

This relationship illustrates that counting the number of rings of magnetic field lines around a conductor is really the same as integrating the magnetic field density in the half space from one side of the conductor to infinity, as illustrated in Figure 4.8.



**Figure 4.8** Counting field lines is about integrating the  $B$  field density from the edge of the wire to some distance  $b$ , typically infinity. When the integration starts from the outside edge of the conductor, it is just the “external” inductance.

Conceptually, thinking of inductance as the number

of field line rings per amp of current completely surrounding the conductor is easy. The integral of the field line density merely does the counting for us. Knowing the magnetic field line density in space allows us to perform this integral and calculate the inductance for any arrangement of currents.

**Tip**

Inductance, as a total number of field lines per amp of current through the conductor, is the integral of the magnetic field density. One way of integrating the field density is to count the number of field line rings.

## 4.7 INDUCTANCE AND ENERGY IN THE MAGNETIC FIELD

We can also think of inductance as related to the efficiency of storing energy in the magnetic field around a current carrying loop. Current flowing through a collection of conductors creates some distribution of magnetic field lines. The resulting field lines store energy. The higher the field line density  $B$  the higher the energy density. We derive the energy density stored in the magnetic field with

$$e = \frac{1}{2} \mu_0 B^2 \quad (4.25)$$

where

$e$  = energy density in the magnetic field, in joules/m<sup>3</sup>

$B$  = the magnetic field density in Webers/m<sup>2</sup>

$\mu_0 = 4 \times \pi \times 10^{-7}$  H/m = 1.257 nH/mm = 32 nH/inch  
= 32 pH/mil

Note that the number of rings of magnetic field lines  $\Psi$  do not store the energy density; the field line density  $B$  stores the energy density. This suggests that the field lines themselves are not what store energy, but how

tightly packed they are. A single magnetic field line does not have energy by itself. Energy is stored in how close together the field lines are packed. It is as if the field lines create a pressure. The tighter they are bunched, the higher their pressure and the more energy is stored in compressing them.

**Tip**

Although energy is stored in the magnetic field around a conductor, it is as if the energy is stored in the pressure of compressing magnetic fields and increasing their density. The higher the density of field lines, the higher the energy density.

We can calculate the total energy in the space containing the magnetic field lines by integrating the energy density and the B field density, over all space around the current loop:

$$U = \iiint_{\text{volume}} \frac{1}{2} \mu_0 B^2 dv \quad (4.26)$$

where

$U$  = the total energy stored in the magnetic fields around the current loop in joules

$B$  = the magnetic field density in Webers/m<sup>2</sup>

$\mu_0 = 4 \times \pi \times 10^{-7}$  H/m = 1.257 nH/mm = 32 nH/inch  
= 32 pH/mil

$dv$  is the small volume element in which the B field density is constant

Because the magnetic fields are also related to the inductance of the current loop and the current in the loop, we can calculate the total energy stored in the magnetic field in terms of the inductance of the loop and the current:

$$U = \frac{1}{2} LI^2 \quad (4.27)$$

From this, we can relate the loop inductance to the energy stored in the magnetic field around it as

$$L = \frac{2U}{I^2} \quad (4.28)$$

where

$U$  = the total energy stored in the magnetic fields around the current loop in joules

$L$  = the total loop inductance of the current loop

$I$  = the current in the current loop

This suggests another way of thinking about inductance: as the efficiency of creating energy stored in the magnetic field per amp squared. A higher inductance for a conductor loop means a higher efficiency of storing energy. A low inductance means a lower efficiency of storing energy.

**Tip**

An alternative way of thinking about inductance is as the efficiency of creating energy stored in the magnetic field per amp of current. A higher inductance for a conductor loop means a higher efficiency of storing energy at the cost of current.

The loop inductance of a current loop is a property of the entire loop, related to the total number of rings of magnetic field lines completely surrounding the conductors. The energy stored in the magnetic field is a property of the entire space around the conductors.

We can easily imagine the energy distributed in the space around a current carrying loop in terms of the energy density in the magnetic field—the compression of the magnetic field lines. In regions of space where the field density is higher and the field lines are packed close together, the energy density is higher.

In the same way, it is as if the inductance were

distributed in the space around the current carrying conductors. When we integrate the “inductance density” over all space, we get the total loop inductance of the current loop. Relating the energy stored in the magnetic field and the total loop inductance, we get

$$L = \frac{2U}{I^2} = \iiint_{\text{volume}} \frac{\mu_0}{I^2} B^2 dv \quad (4.29)$$

and

$$\frac{dL}{dv} = \frac{\mu_0}{I^2} B^2 \quad (4.30)$$

where

$dL/dv$  = the “inductance density” in the space around a current loop

$B$  = the magnetic field density in Webers/m<sup>2</sup>

$\mu_0 = 4 \times \pi \times 10^{-7}$  H/m = 1.257 nH/mm = 32 nH/inch  
= 32 pH/mil

$I$  = the current in the current loop creating the magnetic field lines

The “inductance density” is a measure of the square of the (B field density per amp). The higher the B field density per amp, the more efficiently the magnetic field density is created, and the higher the inductance density.

In this way, we can think of an inductance density arising from the magnetic field density. It is not strictly the magnetic field density, but is the efficiency of creating the magnetic field density per amp of current.

**Tip**

The inductance density in the space around a conductor is related to the square of the magnetic field density. This concept is important when trying to engineer physical structures with lower inductance. Try to reduce the inductance density around the conductor.

This view of inductance is useful when considering design alternatives. Conductor configurations that create high magnetic field densities will also create high inductance densities. Two design features can help reduce the inductance of a collection of current-carrying conductors. For a fixed current:

- Reduce the magnetic field density around the conductors by making the conductors larger, perpendicular to the current flow
- Bring the signal and return current in close proximity so that a smaller volume of space around the conductors has any appreciable magnetic field density

These two goals translate to the same three design principles illustrated earlier to reduce loop inductance:

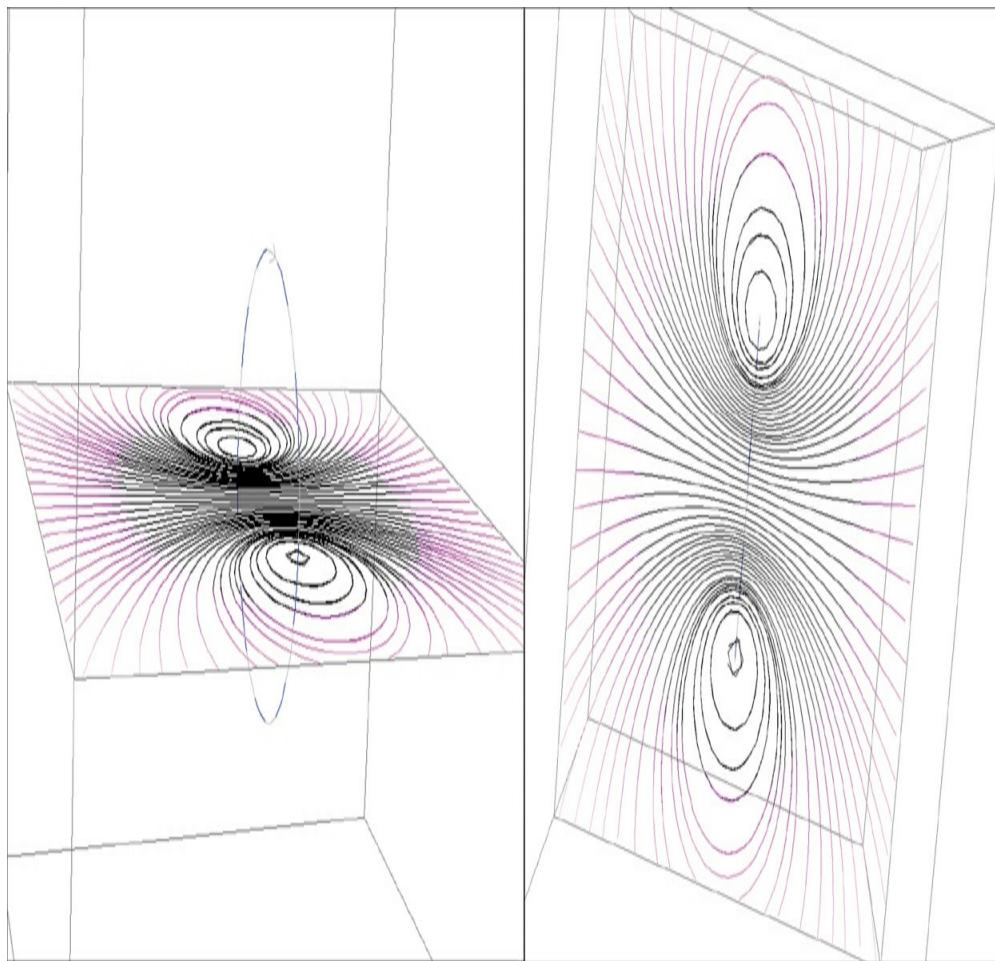
- 1. Increase the width of the conductors:** This reduces the magnetic field density.
- 2. Decrease the length of the conductors:** This reduces the volume over which the magnetic field density is integrated.
- 3. Bring the signal and return conductors into close proximity:** This causes the magnetic field density far from the current loop to drop to near zero, reducing the volume over which the field density is integrated.

Although the total inductance is what matters, if the possibility exists to keep the inductance density low over the entire region around the current loop, the total

inductance will be low as well.

## 4.8 MAXWELL'S EQUATIONS AND LOOP INDUCTANCE

One sort of geometry exists for which the inductance of a conductor is unambiguous and straightforward to calculate. When the conductor is in the shape of a closed loop of current, every single field line that goes around the loop of current also goes through the closed area of the loop (see [Figure 4.9](#)).



**Figure 4.9** Two different views of the magnetic field lines around a closed loop of current showing only those field lines on a slice through the center of the loop.

To uniquely count all the rings of magnetic field lines that completely surround the conductor, we need only to count the field lines that pass through the area enclosed by the current loop. In the special case when the conductor is in the shape of a closed loop, we call

the inductance associated with the entire loop, the loop inductance.

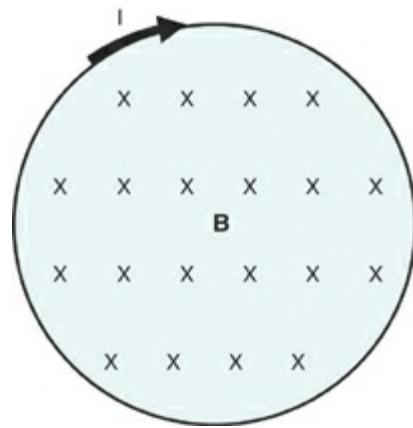
**Tip**

Loop inductance is the total number of field line rings per amp that pass through the closed current loop. We can calculate it by integrating the magnetic field density over the closed loop.

The loop inductance is the total number of rings of magnetic field lines that completely surround the conductor that makes up the loop. Counting these field lines is equivalent to integrating the magnetic field density, which may vary across the surface of the loop:

$$L_{\text{loop}} = \frac{\Psi_{\text{loop}}}{I} = \frac{1}{I} \iint_{\text{closed area}} \bar{B}(x, y) \cdot d\bar{a} \quad (4.31)$$

This is illustrated in Figure 4.10.



**Figure 4.10** We calculate the loop inductance of a closed loop of current by integrating the magnetic field density over the surface enclosed by the loop of the current. This is equivalent to counting all the rings of magnetic field lines that pass through the loop and that also completely surround the entire conductor.

If we can calculate the magnetic field density across the surface enclosed by the loop, normalized by the current, we can calculate that loop's inductance. The field density cannot vary arbitrarily over space. Its spatial variation must obey two of Maxwell's Equations.

The first describes the rule that magnetic field lines must be closed rings, because no sources or sinks exist on which magnetic field lines can terminate:

$$\vec{\nabla} \cdot \vec{B} = 0 \quad (4.32)$$

The second of Maxwell's Equations the B field density must obey is

$$\vec{\nabla} \times \vec{B} = \mu_0 \vec{J} \quad (4.33)$$

where

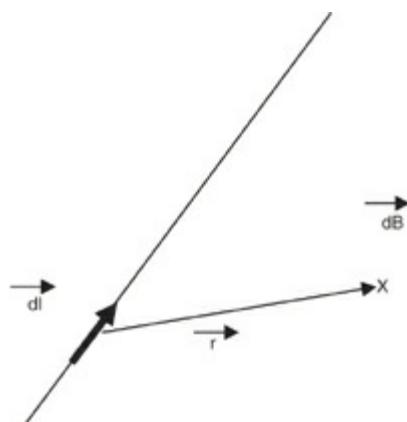
$J$  = the current density in amps/m<sup>2</sup>

$\mu_0$  = the permeability of free space, =  $4 \times \pi \times 10^{-7}$

H/m = 32 nH/inch = 32 pH/mil

This describes how to calculate the magnetic field density in space, as generated by currents. From these expressions, we can calculate the magnetic field density anywhere in space from an arbitrary collection of currents. Solving these equations is often a challenge, except for simple geometries, and this is another reason why calculating inductance is difficult.

A commonly used technique to apply Maxwell's Equations to calculate the magnetic field density anywhere in space is to use the Biot-Savart relationship. This describes the small contribution of magnetic field density created in space by a small current element, with current I, and of length, dl. Figure 4.11 illustrates this relationship.



**Figure 4.11** The Biot-Savart relationship describes the generation of a small amount of magnetic field density,  $d\vec{B}$ , at the location marked by the  $x$ , from a small current element.

The Biot-Savart relationship is

$$d\vec{B} = \frac{\mu_0}{4\pi} I \frac{d\vec{l} \times \vec{r}}{|r|^3} \quad (4.34)$$

where

$d\vec{B}$  = the small amount of magnetic field density created at a point in space,  $r$  from the current

$I$  = the current in the small section of the conductor,  
 $dl$

$dl$  = the small vector length of current generating the small magnetic field density

$r$  = the vector distance from the small current element to the point where the  $B$  field density is generated

and the operator in this relationship is the cross product between the  $dl$  and  $r$  vectors.

To calculate the magnetic field density at a point in space, we need to integrate the magnetic field density created by all the current elements at one point. To map out the magnetic field density everywhere in space surrounding the conductors, we move this point in space around.

To calculate the loop inductance of a conductor

configuration, we need to integrate this calculated magnetic field density over the enclosed loop area. This process is a double integral. First, integrate over all the currents to get the magnetic field density at one point in space, and then integrate the field density over the area enclosed by the current loop. This is why calculating the inductance is generally so difficult. Although some simplifications exist, in general, it requires calculating two complicated integrals.

As a practicing engineer, doing an inductance integral at least once in your life is important, just to see how to do it. Luckily, there is never a reason to do one again. Instead, four options are available to calculate the inductance of a collection of conductors, in any configuration.

1. Use a closed-form analytical approximation.
2. When the geometry is a uniform transmission line, use a 2D static or quasi-static field solver that provides either the high-frequency or the frequency-dependent inductance.
3. Use a 3D quasi-static field solver that calculates the DC, the high-frequency, or the frequency-dependent inductance.
4. Use a full-wave field solver that always takes the frequency-dependent inductance into account.

**Tip**

In general, calculating loop inductance for any shaped loop is difficult because it involves a double integral, which can be complicated. Instead, we can use approximations for specific geometries or field solvers to calculate loop inductance.

## 4.9 INTERNAL AND EXTERNAL INDUCTANCE AND SKIN DEPTH

Yet another complication is that the total inductance of

a conductor depends on the precise current distribution in the conductor. If the current distribution changes with frequency, the magnetic field density pattern will change and the inductance will be frequency dependent. It has nothing to do with the propagating wave nature of the current, as long as the structure is within the quasi-static approximation size restriction, but is related to the currents inside the conductor interacting with the magnetic field lines inside the conductor, as well as the material properties of the conductors.

We separate the magnetic field lines into external magnetic fields, which circulate outside the conductor, and internal magnetic field lines, which circulate inside the conductor, and interact with the material properties of the conductor. External field lines contribute to external inductance and internal field lines contribute to the internal inductance of the conductor.

The external field lines are generally independent of the current distribution inside the conductor. External inductance will not vary with frequency. External inductance is independent of the composition of the conductor. External inductance only depends on the geometry of the conductor.

However, internal inductance generally is frequency dependent and is sensitive to the material properties of the conductor. At DC, the current distribution in a conductor is generally uniform throughout the conductor cross section. Internal field lines will circulate around the current inside the conductor.

**Tip**

The inductance of any conductor is composed of internal inductance contributed by magnetic field lines that circulate inside the conductor and external inductance, composed of field lines outside the conductor. External inductance is the high-frequency inductance of a conductor.

The total internal inductance for a length, Len, of round wire, due to a uniform DC current distribution is the number of rings of magnetic field lines inside the conductor per amp of current. Surprisingly, internal inductance is independent of the diameter of the wire. The larger the diameter, the lower the current density and the lower the density of the rings of magnetic field lines. The total number of internal field lines, the integral of the B field density internal to the conductor per amp of current, inside the conductor is the same independent of conductor diameter.

With a little algebra, using Ampere's Law, we can calculate the total internal inductance of a round conductor at DC exactly, assuming a metal with a relative permeability of  $\mu_r$ , as

$$L_{\text{internal}} = \text{Len} \frac{\mu_r \mu_0}{8\pi} = \mu_r \times \text{Len} \times 50 \text{nH/m} = \mu_r \times 1.28 \text{nH/inch} \times \text{Len} \quad (4.35)$$

Relative permeability is a measure of the effective amplification of magnetic field lines by a material. When rings of magnetic field lines are fully contained inside a conductor, the number of field line rings is increased by a factor equal to the relative permeability, compared to the number of field line rings that would be there if the relative permeability were 1. When the field line rings are not fully enclosed inside the higher permeability material, the amplification factor is closer to 1 and generally difficult to calculate analytically.

The relative permeability of most metals is 1, and the internal inductance of a conductor is independent of the conductor composition. For example, copper, silver, aluminum, tin, and lead all have a permeability of 1. For these conductors, the internal inductance is independent of the conductor's composition.

The exceptions are the three ferromagnetic metals,

and alloys or compounds that contain them. These ferromagnetic metals are iron, nickel, and cobalt. When nickel is plated, its permeability can be between 1 and 40 depending on the plating conditions. It generally decreases above about 1 GHz and approaches 1 at higher frequencies.

**Tip**

With the exception of the three ferromagnetic materials, iron, nickel, and cobalt, the magnetic permeability of all interconnect metals is 1. The permeability of a ferromagnetic material will increase the number of rings of magnetic field lines that circulate *inside* the conductor.

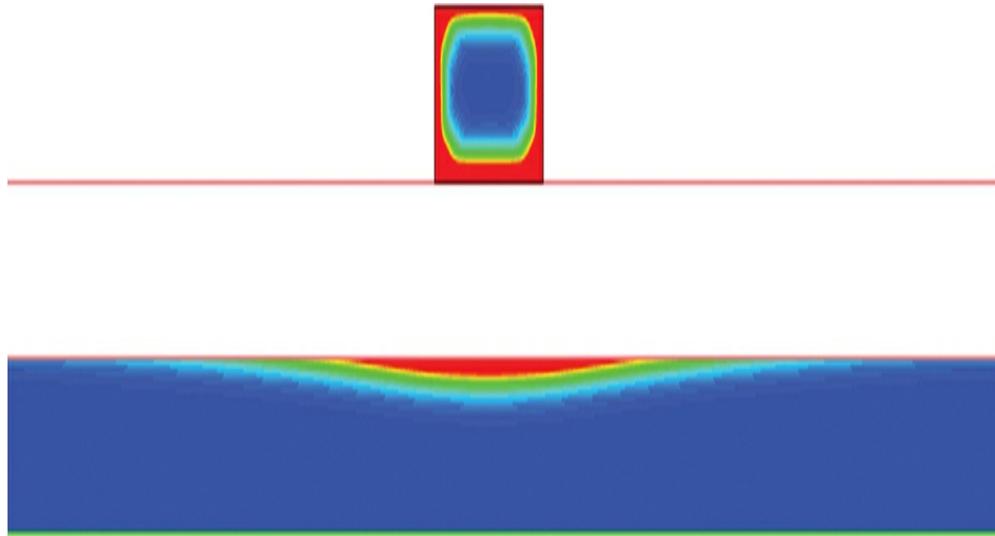
A popular lead frame metal, alloy 42, is composed of 42% nickel and the rest iron. Its thermal coefficient of expansion is engineered to match that of glass and is used in glass-ceramic hermetic packages. It is also stiffer than copper. For very small and delicate lead frames, it has better mechanical strength for handling and assembly operations. However, its bulk resistivity is about 50 times higher than copper, and its relative permeability is about 200.

This means that at DC, the internal inductance of an alloy 42 lead frame will be as much as 200 times that of a copper lead frame. This sounds like it could be a huge problem, but the inductance at DC is not nearly as important as the inductance at 100 MHz. At higher frequency, the currents will flow mostly in the outer surface of the conductor and there will be no internal magnetic field lines to be affected by the higher permeability of the conductor. The inductance of the lead frame will be mostly external inductance, which is independent of the permeability.

As frequency increases, the current in all conductors redistributes toward the outer surface of the conductor.

**Figure 4.12** shows an example of the simulated current distribution at 100 MHz in a microstrip transmission line. With no current in the center of the conductor, no closed field line rings will be inside the conductor, and no internal inductance. As less and less current flows inside the conductor, the internal inductance decreases and the permeability of the conductor material has less and less influence. In alloy 42 lead frames, the internal inductance is negligible above about 10 MHz.

The external inductance, in contrast, is unaffected by the composition of the conductor. It just depends on the geometry of the conductor.



**Figure 4.12** Current density at 100 MHz in a 1.4 mil thick copper microstrip transmission line. At higher frequency, current redistributes to the outer surface of conductors. The uniform color is lower current density.

The effective thickness in which most of the current travels in a conductor is the *skin depth*. This is also the effective depth in the conductor into which the magnetic field lines penetrate, where they are affected by the permeability properties of the conductor. We calculate the skin depth of a conductor as

$$\delta = \frac{1}{\sqrt{\pi \mu_r \mu_0 \sigma f}} \quad (4.36)$$

where

$\delta$  = the skin depth in meters

$\mu_r$  = the relative permeability of the conductor

$\mu_0 = 4 \times \pi \times 10^{-7}$  H/m

$\sigma$  = the conductivity of the conductor in  $1/\Omega\text{-m}$

$f$  = the frequency in Hz

In a more useful set of units, and for the specific case of copper, the skin depth is

$$\delta = \frac{1}{\sqrt{\pi \mu_r \mu_0 \sigma f}} = 2.1 \times \frac{1}{\sqrt{f[\text{GHz}]}} \mu\text{m} \quad (4.37)$$

where

$\delta$  = the skin depth in  $\mu\text{m}$

$f$  = the frequency in GHz

At 1 GHz, the skin depth of copper is 2.1  $\mu\text{m}$ . At 10 MHz, it is 21  $\mu\text{m}$ , which is slightly under 1 mil. This suggests that for typical circuit board traces, with a geometrical thickness of 17  $\mu\text{m}$ , the current is mostly on the outer surface at frequencies above 100 MHz and the inductance of the traces is all external inductance.

**Tip**

Skin depth is the effective thickness in which current flows in a conductor. At 1 GHz, it is 2.1  $\mu\text{m}$  in copper and decreases inversely with the square root of frequency. This causes inductance to be slightly frequency dependent.

In thick copper wires, which can be many mils in diameter, the current is mostly on the outer surface at frequencies above about 1 MHz and all the inductance is external inductance. The high-frequency inductance is a good approximation to the conductor's inductance when the skin depth is significantly less than the geometrical thickness. For wires, this is above about 1 MHz. For

circuit board traces, this is above about 100 MHz.

In the case of alloy 42 lead frames, the skin depth is affected by both its conductivity and its permeability. The permeability is 200 times that of copper, and the conductivity is 1/50 that of copper. The product is 4 times higher than copper. This means the skin depth for alloy 42 is half that of copper. At 10 MHz, it is about 10  $\mu\text{m}$ .

The typical lead frame thickness is about 3 mils, which is 75  $\mu\text{m}$ . This means that at 10 MHz and above, most of the current is in the outer 10  $\mu\text{m}$  of the conductor. There is very little penetration of magnetic field lines into the conductor and few internal field lines to be affected by the high permeability of the alloy 42 leads. Its inductance is almost all external inductance. Above about 10 MHz, the inductance of an alloy 42 lead frame is the same as for a copper lead frame.

However, the resistance of the alloy 42 lead frame is much higher than for a copper lead frame. This is due to the 50 times higher resistivity and the cross section through which current is traveling is half that of the copper lead frame. This makes the resistance 100 times higher than a copper lead frame. A common practice to compensate for this higher resistance is to plate silver on the outside of the lead frame. This makes for robust soldering and, with a silver plating thickness of 20  $\mu\text{m}$ , makes the resistance of alloy 42 lead frames comparable to copper lead frames above 10 MHz.

When the relative permeability is 1, the difference between the DC inductance and the high-frequency inductance is just the internal inductance. For example, the 18-gauge wire in the [Figure 4.6](#) loop example had a total loop inductance of about 247 nH. This is the external, or high-frequency inductance, as the typical frequency range measured was  $> 1$  MHz. At 1 MHz the

skin depth is about 3 mil, which is about 10% of the radius. All the current is within about 10% of the outer surface at the lowest frequency, and the internal inductance decreases even more at higher frequency.

The loop circumference in [Figure 4.6](#) was about  $3.5 \text{ inches} \times 3.1416 = 11 \text{ inches}$ . Its internal self-inductance was about  $1.28 \text{ nH/inch} \times 11 \text{ inches} = 14 \text{ nH}$ . This is < 6% of the total loop inductance. If we could have measured its loop inductance at 1 Hz, for example, the loop inductance would have measured as about 14 nH higher than 247 nH due to this internal self-inductance.

**Tip**

The typical difference between the DC inductance and high-frequency inductance of a conductor is the amount of internal self-inductance, which is typically less than 10% of the high-frequency inductance.

When solving this as an analytical approximation, we usually state inductance as either the DC inductance, where the currents are assumed to flow uniformly inside the conductor, or as the high-frequency inductance, where the currents are assumed to flow on the outer surface of the conductors. The high-frequency inductance of a conductor is its external inductance.

## 4.10 LOOP AND PARTIAL, SELF- AND MUTUAL INDUCTANCE

We calculate loop inductance, the efficiency of a closed loop of current for generating rings of magnetic field lines, per amp of current, by taking the integral of the magnetic field density enclosed by the current loop. We can measure and simulate this unambiguous quality of the current loop. Although signal and return path segments make up the loop, we make no distinction about the contributions to the loop inductance from any

specific section. Loop inductance is a property of the entire loop. Make a change to any feature of the loop, and the entire loop inductance changes.

To separate the contributions to the loop inductance from specific segments of the loop, we need to use partial self- and partial mutual inductances. These terms have a precise mathematical foundation and offer some conceptual advantages over just total loop inductance.

In the view of partial inductance, any segment of a loop has some inductance associated with it. Partial inductance is defined just like any inductance: a ratio of the number of rings of magnetic field lines per amp of current. However, we distinguish around which conductor segment we are counting field line rings and in which segment the current flows that creates these field line rings.

**Tip**

Partial inductance is another way of looking at loop inductance, which identifies the contribution to the loop inductance from each part of the loop. Sometimes thinking of the partial inductances of a loop can add insight on how to engineer loop design features to affect the loop inductance.

*Self*-field lines are the field line rings around a conductor from current in that conductor. The self-inductance of a segment is the ratio of the number of self-magnetic field lines around that segment per amp of current through that segment. The region of space over which we count the rings of self-field lines is bounded by infinite planes normal to the endcaps of the conductor. To distinguish this inductance, which is for only part of the loop, from the entire loop's inductance, this self-inductance has the special label of *partial* self-inductance.

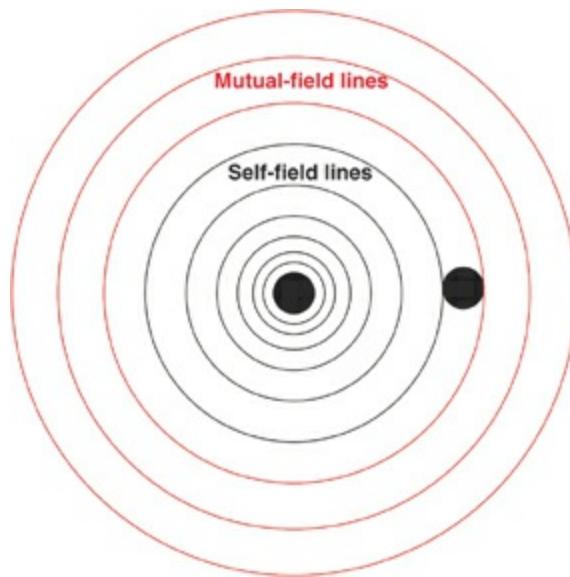
In addition to the length, the chief factor that

influences the partial self-inductance of a conductor is its width. The wider the conductor, the more the current can spread out, and the lower its partial self-inductance.

Rings of magnetic field lines from one segment of a loop that also go around another segment of the loop are *mutual* field lines. The *partial* mutual inductance between two parts of a loop is the ratio of the number of rings of magnetic field lines around one segment from the current in another segment, per amp of current in the other segment.

In addition to the length, the chief design feature that influences the partial mutual inductance between two conductors is their separation. Increase their separation and there will be fewer mutual-field lines around a conductor from currents in the other conductor, and the partial mutual inductance will decrease.

Figure 4.13 illustrates these two types of magnetic field lines.



**Figure 4.13** Magnetic field lines surrounding a current in a conductor with an adjacent conductor nearby. All the field lines are self-field lines to the central current. Some of the rings of magnetic field lines also go around the adjacent conductor and are mutual-field lines.

The loop inductance of a closed loop of current is the total number of field line rings around the entire

current path. If we decompose a loop into two segments, a signal path and a return path, we can calculate the loop inductance of the entire loop from the partial self- and partial mutual inductances of the two segments.

The total number of rings of magnetic field lines around just the signal path is its self-field lines minus the mutual-field lines from the return path. The subtraction is because the direction of circulation of the mutual-field lines from the return current, around the signal path, are in the opposite direction. The total number of field lines around the return path are its self-field lines of the return path minus the mutual-field lines from the current in the signal path. The total inductance of the signal and return paths, which is the loop inductance of the complete path, is the sum of these two total inductances derived by

$$L_{\text{loop}} = (L_{\text{self-signal}} - L_{\text{mutual}}) + (L_{\text{self-return}} - L_{\text{mutual}}) = L_{\text{self-signal}} + L_{\text{self-return}} - 2L_{\text{mutual}} \quad (4.38)$$

If the signal and return path conductors are identical, their self-inductances are the same and the loop inductance is just

$$L_{\text{loop}} = L_{\text{self-signal}} + L_{\text{self-return}} - 2L_{\text{mutual}} = 2 \times (L_{\text{self}} - L_{\text{mutual}}) \quad (4.39)$$

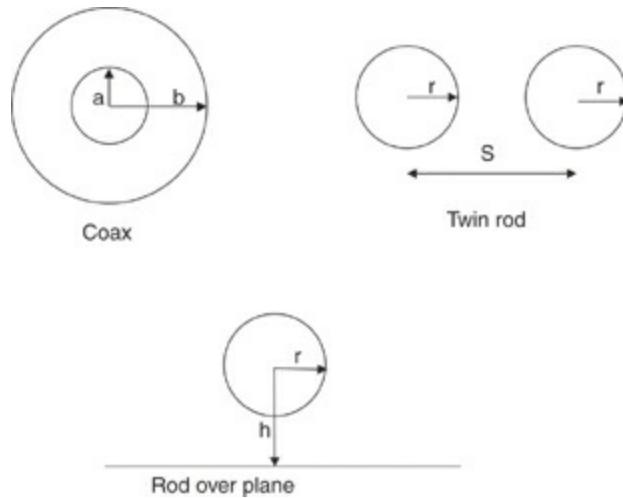
If the goal is to reduce the loop inductance of a signal and return path loop, then in addition to decreasing the length of the conductors, the other two important design features are implementing wider conductors to achieve smaller partial self-inductance of each conductor, and bringing the conductors closer together to achieve larger partial mutual inductance between the conductors. As we look at analytical approximations for the loop inductance of many geometrical configurations, these three design guidelines appear over and over again.

**Tip**

Using partial inductance, we can identify specific features in the signal path and the return path to affect the loop inductance of the entire loop. We can achieve lower loop inductance with shorter conductors, wider conductors, and bringing the signal and return paths closer together.

## 4.11 UNIFORM ROUND CONDUCTORS

Only three geometries exist for which Maxwell's Equations can be solved exactly and the capacitance and inductance per length of structures calculated with exact analytical equations: coax, two round rods, and a rod over a plane [5]. Every other structure has an inductance that is calculated either by an approximation or in a complicated and unwieldy form. Figure 4.14 shows these three special geometries.



**Figure 4.14** Examples of the three geometries for which exact expressions exist for the loop inductance per length of the conductors.

In a coax cable, we derive the loop inductance per length of a current traveling down the center conductor and looping back through the shield as

$$L_{\text{Len}} = \frac{\mu_0}{2\pi} \ln\left(\frac{b}{a}\right) \quad (4.40)$$

where

$L_{\text{Len}}$  = loop inductance per length, nH/inch or

nH/mm

a = outer radius of inner conductor

b = inner radius of outer conductor

$$\mu_0 = 4\pi \times 10^{-7} \text{ H/m} = 32 \text{ nH/inch} = 32 \text{ pH/mil}$$

This relationship illustrates how design features affect inductance. If the return conductor is pulled farther away, b increases and the loop inductance increases, though weakly with a natural log function. For example, in a coax cable with the outer radius of 5 mm and inner radius of 2 mm, the loop inductance per length is

$$L_{Len} = \frac{\mu_0}{2\pi} \ln\left(\frac{b}{a}\right) = \frac{32}{2\pi} \ln\left(\frac{5}{2}\right) = 4.7 \text{ nH/inch} \quad (4.41)$$

For two parallel, round rods, we get the loop inductance per length with

$$L_{Len} = \frac{\mu_0}{\pi} \cosh^{-1}\left(\frac{s}{2r}\right) = \frac{\mu_0}{\pi} \ln\left(\left(\frac{s}{2r}\right) + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \quad (4.42)$$

In the special case when the separation between the rods is much larger than the radius of the rods,  $s \gg r$ , we can approximate this with

$$L_{Len} = \frac{\mu_0}{\pi} \ln\left(\frac{s}{r}\right) = \frac{32}{\pi} \ln\left(\frac{s}{r}\right) = 10 \times \ln\left(\frac{s}{r}\right) \text{ pH/mil} \quad (4.43)$$

where

$L_{Len}$  = loop inductance per length, nH/inch or  
nH/mm

r = radius of each rod, in mils

s = center-to-center pitch of the two rods, in mils

$$\mu_0 = 4\pi \times 10^{-7} \text{ H/m} = 32 \text{ nH/inch} = 32 \text{ pH/mil}$$

For example, the typical dimensions of a pair of vias under a BGA package might be  $r = 5$  mils and  $s = 40$

mils. The loop inductance per length of the via pair would be

$$L_{Len} = \frac{\mu_0}{\pi} \ln \left( \left( \frac{s}{2r} \right) + \sqrt{\left( \frac{s}{2r} \right)^2 - 1} \right) = \frac{\mu_0}{\pi} \ln \left( \left( \frac{40}{10} \right) + \sqrt{\left( \frac{40}{10} \right)^2 - 1} \right) = 21 \text{ pH/mil} \quad (4.44)$$

The approximation also predicts

$$L_{Len} = 10 \times \ln \left( \frac{s}{r} \right) = 10 \times \ln \left( \frac{40}{5} \right) = 21 \text{ pH/mil} \quad (4.45)$$

For a board about 64 mils thick and vias spanning from one side to the other, the loop inductance for the via pair is about  $64 \text{ mils} \times 21 \text{ pH/mil} = 1.3 \text{ nH}$ . This is a good approximation for the typical loop inductance of vias in a board.

The rod over plane geometry is similar to the twin rod geometry. Using the principle of the method of images, the magnetic field distribution for the twin rod is identical to the rod over plane with the height above the plane,  $h$ , equal to half the separation,  $s$ .

For the rod over plane example, we are only counting the magnetic field lines in the upper region of the space. This means the loop inductance of the rod over plane is half the loop inductance of the equivalent twin rods case. We get the loop inductance per length for the rod over plane geometry with

$$L_{Len} = \frac{\mu_0}{2\pi} \ln \left( \left( \frac{h}{r} \right) + \sqrt{\left( \frac{h}{r} \right)^2 - 1} \right) \quad (4.46)$$

where

$L_{Len}$  = loop inductance per length, nH/inch or  
nH/mm

$r$  = radius of each rod, in mils

$h$  = height of the center of the rod over the plane, in

mils

$$\mu_0 = 4 \pi \times 10^{-7} \text{ H/m} = 32 \text{ nH/inch} = 32 \text{ pH/mil}$$

For example, if a 24 AWG engineering change wire with a diameter of 10 mils (or radius of 5 mils) is routed over the top surface of a board with an internal plane located 20 mils from the center of the wire, the loop inductance per inch for current flowing through it and returning in the plane is

$$L_{\text{len}} = \frac{\mu_0}{2\pi} \ln \left( \left( \frac{h}{r} \right) + \sqrt{\left( \frac{h}{r} \right)^2 - 1} \right) = \frac{32}{2\pi} \ln \left( \left( \frac{20}{5} \right) + \sqrt{\left( \frac{20}{5} \right)^2 - 1} \right) = 10.5 \text{ nH/inch} \quad (4.47)$$

The loop inductance of a 1-inch length of engineering change wire, routed over the surface of a board with a plane close to the board's surface, is 1 inch  $\times$  10 nH/inch = 10 nH. This also illustrates that the closer the wire can be positioned to the plane, the lower its loop inductance. However, because it is the ratio of the height between the center of the rod and the plane to the radius of the wire, if we decrease both the wire radius and distance to the plane, no net change occurs in the loop inductance. Rather, keeping the length short is the most important factor to minimize the loop inductance of a wire.

**Tip**

The only three structures for which we can calculate the inductance calculated exactly are coax, twin rods, and rod over plane. For all other structures, the loop inductance—however complicated the equation might be—is still just an approximation.

## 4.12 APPROXIMATIONS FOR THE LOOP INDUCTANCE OF ROUND LOOPS

A few simple approximations can provide some rough estimates to the loop inductance of a collection of conductors [6]. To calculate the inductance of a loop, we

need to know the value of the magnetic field density everywhere within the loop area and then integrate this value over the surface of the loop.

If the magnetic field density were constant over the loop area, the loop inductance would be proportional to the area of the loop. In general, the magnetic field density is not constant over the loop, but varies in a complex way. Contrary to popular belief, this means that the total flux of field lines—the total number of rings of magnetic field lines that surround the entire current loop—will not be exactly proportional to the area.

For the case of the simplest geometry, a circular loop with radius  $a$  and a wire of radius  $WR$ , we approximate the high-frequency loop inductance as

$$L_{\text{loop}} = \mu_0 a \left( \ln\left(\frac{8a}{WR}\right) - 2 \right) \quad (4.48)$$

where

$L_{\text{loop}}$  = the loop inductance of a round loop in H

$a$  = the radius of the loop in m or inches

$WR$  = the wire radius in m or inches

$$\begin{aligned} \mu_0 &= 4 \times \pi \times 10^{-7} \text{ H/m} = 1.257 \text{ nH/mm} = 32 \text{ nH/inch} \\ &= 32 \text{ pH/mil} \end{aligned}$$

For example, for a wire with a 10 mil radius, which is roughly 24-gauge AWG wire wrapped in a loop with a loop radius of 1 inch (roughly the size of your thumb and index finger touching in a circle), the loop inductance is

$$L_{\text{loop}} = 32 \text{ nH/inch} \times 1 \times \left( \ln\left(\frac{8 \times 1}{0.01}\right) - 2 \right) = 150 \text{ nH} \quad (4.49)$$

In the measured example presented after [Figure 4.7](#), the parameters were

$$a = 1.75 \text{ inches}$$

$$WR = 0.0245 \text{ inches}$$

$$\begin{aligned}\mu_0 &= 4 \times \pi \times 10^{-7} \text{ H/m} = 1.257 \text{ nH/mm} = 32 \text{ nH/inch} \\ &= 32 \text{ pH/mil}\end{aligned}$$

The predicted loop inductance of this 3.5-inch diameter loop is

$$L_{\text{loop}} = 32 \text{ nH/inch} \times 1.75 \times \left( \ln\left(\frac{8 \times 1.75}{0.0245}\right) - 2 \right) = 245 \text{ nH} \quad (4.50)$$

Note that the measured high-frequency loop inductance was 247 nH. This illustrates the accuracy of this simple approximation.

Also note that the dielectric constant ( $Dk$ ) of the material around the conductor does not play any role at all in the loop inductance of the conductor. Because magnetic fields do not interact with dielectric materials, the loop inductance of a collection of current paths is completely independent of the dielectric properties of the materials surrounding the conductors. It depends only on the geometry of the conductors.

From the form of this approximation, we see immediately that for a round loop of wire, the loop inductance is not proportional to the area of the loop,  $a^2$ , nor is it proportional to the circumference  $a$ , but is proportional to  $a \times \ln(a)$ . Although thinking of the loop inductance of a round loop to be directly proportional to the loop area is not correct, it is convenient to imagine that a smaller area would result in less loop inductance.

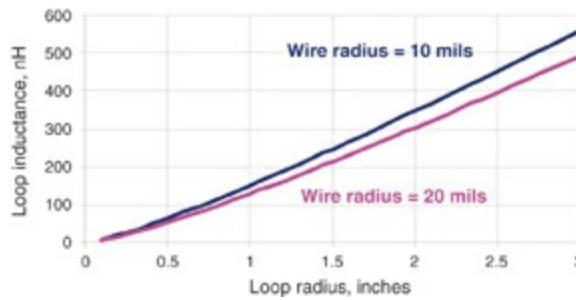
**Tip**

Contrary to popular belief, the loop inductance of a round loop is not proportional to the area of the loop but to the diameter  $\times \ln(\text{diameter})$ . It is true that a larger area will increase the loop inductance, just not proportionately.

This relationship also identifies the other physical

design feature that affects loop inductance: the diameter of the conductor. The more the current can spread out in the conductor because of a larger wire radius (WR), the lower the loop inductance. Of course, in this specific geometry the loop inductance depends on the natural log of the wire radius, which is a soft dependence. An increase in the wire radius allows the current to spread out more and the loop inductance decreases.

This is illustrated in [Figure 4.15](#), which shows the loop inductance plotted for a wire radius of 10 and 20 mils.

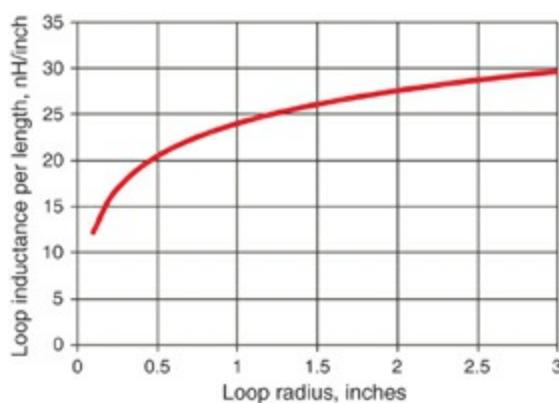


**Figure 4.15** Loop inductance of round wire with changing wire radius and two different wire radii.

The loop inductance does not scale with the perimeter of the loop. For a wire radius of 10 mils, we roughly estimate the loop inductance per length of the perimeter by taking the loop inductance and normalizing it to the circumference of the loop. [Equation 4.51](#) describes this:

$$L_{\text{loop}}/\text{Len} = \frac{L_{\text{loop}}}{2\pi a} = \frac{\mu_0}{2\pi} \left( \ln\left(\frac{8a}{\text{WR}}\right) - 2 \right) \quad (4.51)$$

For the special case of a wire 10 mils in radius, the loop inductance per length is shown in [Figure 4.16](#).



**Figure 4.16** Loop inductance per length for a round wire loop with wire radius of 10 mils.

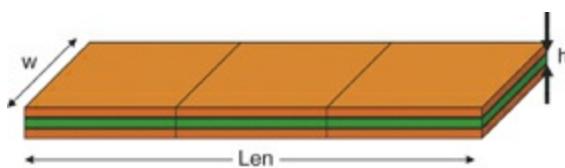
In this specific case of a wire radius of 10 mils, we see that over the range of about a half-inch loop radius to 2-inch loop radius, the loop inductance per length is about 25 nH/inch of circumference. This is one of the origins of the simple rule of thumb that without knowing anything else about the conductors except that they are roughly in a loop, the loop inductance is about 25 nH/inch or 1 nH/mm of circumference. This is a useful general rule of thumb to estimate loop inductance.

**Tip**

Based on the approximation for a circular loop of wire, the loop inductance per length is roughly about 25 nH/inch of circumference. This is 1 nH/mm. If you don't know anything about the structure other than it is roughly circular, and the wire diameter is small, a good approximation of the loop inductance is 25 nH/inch of circumference.

## 4.13 LOOP INDUCTANCE OF WIDE CONDUCTORS CLOSE TOGETHER

When two wide conductors are broadside coupled and close together—for example, two planes with a thin dielectric between them—the loop inductance has a simple form. Figure 4.17 illustrates this geometry.



**Figure 4.17** Cross section for a current loop with wide conductors and thin dielectric between them.

We approximate the loop inductance in this configuration with

$$L_{\text{loop}} = \mu_0 \times h \times \frac{\text{Len}}{w} = (32 \text{ pH/mil} \times h) \times \frac{\text{Len}}{w} = L_{\text{sq}} \times n \quad (4.52)$$

where

$L_{\text{loop}}$  = loop inductance in nH

$\mu_0$  = permeability of free space =  $4\pi \times 10^{-7}$  H/m = 32

nH/inch = 32 pH/mil

Len = length of the conductors

w = width of the traces

h = dielectric thickness between the conductors in mils

$L_{\text{sq}}$  = the **sheet inductance in pH/square**

n = the number of squares down the length of the conductor

This relationship is derived from the capacitance of a pair of parallel plate conductors and is often referred to as the *parallel plate approximation for loop inductance*. Its accuracy is the same as the accuracy of calculating the capacitance of two parallel plates, which ignores the fringe fields off the edges. The larger the aspect ratio, that is, the wider the conductors compared to the dielectric thickness, the better the accuracy of this approximation.

This relationship clearly illustrates the three design principles for reducing inductance. This shows that the loop inductance scales directly with length and spacing between conductors and inversely with the width. The

shorter the conductor length the lower the loop inductance. The wider the current can spread out in the conductors, the lower the loop inductance. Finally, the closer together we can bring the two conductors, the lower the loop inductance. In this special geometry each of the terms are first-order terms.

#### Tip

The approximation for the loop inductance of two parallel plates illustrates the three general design principles for reducing loop inductance: make them shorter, wider, and closer together.

In a typical planar circuit board, all loops constructed from metal on two adjacent layers will have the same dielectric spacing,  $h$ . We can pull this term out separately. What remains in the loop inductance is the ratio of the length of the traces to their width. This is a measure of the number of squares that can fit down the length of the traces.

If we double both the length and the width of the traces, the ratio stays the same and the loop inductance of the two different configurations are the same. This is rather startling. It says any conductor pair constructed from the same sheet will have the same loop inductance if in the shape of a square. All squares have the same ratio of length to width, 1. This assumes the current flows uniformly from one edge of the square to the other.

The inductance of one square has the special name *inductance per square* or *sheet inductance*. The sheet inductance of a pair of planes is an intrinsic property of the two planes and the dielectric thickness between them. It is the loop inductance of one square taken from the sheet of planes:

$$L_{sq} = \mu_0 \times h \times \frac{Len}{w} = \mu_0 \times h \times 1 = (32 \text{ pH/mil} \times h) \quad (4.53)$$

Len/w : ratio determines L, Len or w alone does NOT  
1.26 pH/um x h

where

$L_{sq}$  = the sheet inductance in nH/square

$\mu_0$  = permeability of free space =  $4\pi \times 10^{-7}$  H/m = 32

nH/inch = 32 pH/mil

$h$  = dielectric thickness between the conductors in mils

The sheet inductance of a pair of planes depends only on the dielectric thickness between the planes. It is a direct metric of the inductance per square of any shape conductor pair cut out of the planes. This is one reason why thinner dielectric between power and ground planes is so important; it results in lower loop inductance for any structure cut out of this plane pair.

For example, the thinnest PCB dielectric layer in commercial production that is not at a premium price is 2.7 mils. The sheet inductance of two planes separated by 2.7 mils is

$$L_{sq} = 32 \text{ pH/mil} \times h = 32 \text{ pH/mil} \times 2.7 \text{ mils} = 86 \text{ pH/sq} \quad (4.54)$$

Every square cut from these two planes, regardless of their dimension, will have 86 pH of loop inductance. We refer to the 86 pH as the sheet inductance in units of pH/square. The units of "squares" is considered dimensionless and is often omitted, but should be added for clarity.

We can easily estimate the loop inductance of a pair of traces cut from this plane pair from the sheet inductance and the number of squares down the length of the traces.

If the traces are 1000 mils long and 100 mils wide, a total of  $n = 1000 \text{ mils}/100 \text{ mils}$  or 10 squares can be fit along the traces. Each square has a sheet inductance of 86 pH, so the total loop inductance of the 1000 mil long

and 100 mil wide pair of traces is  $86 \text{ pH/sq} \times 10 \text{ sq} =$   
860 pH.

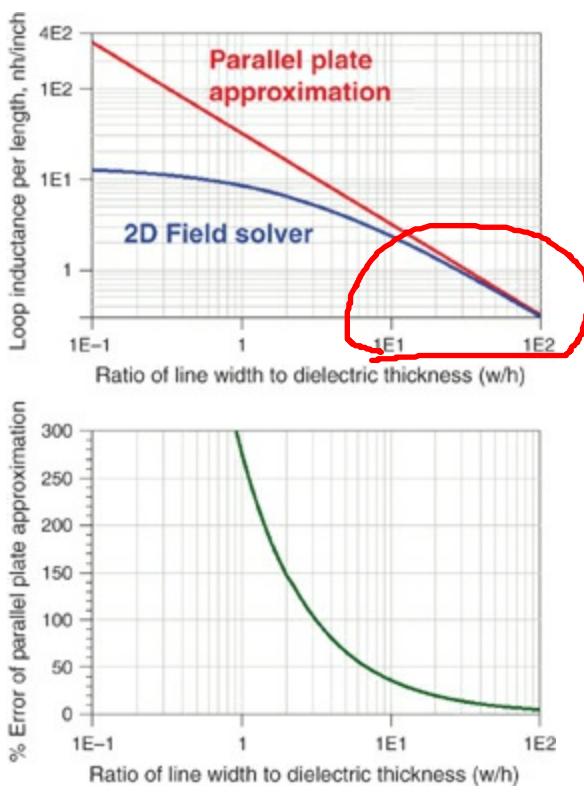
The concept of sheet inductance and the number of squares along a conductor pair is a powerful way of quickly estimating loop inductance for sections of power and ground planes or power traces over wide ground planes.

**Tip**

The concept of sheet inductance and the number of squares along a conductor pair is a powerful way of quickly estimating loop inductance for sections of power and ground planes or power traces over wide ground planes.

From the sheet inductance, we estimate the loop inductance by counting squares along the trace. Long and narrow traces have many squares and a high loop inductance. Short, wide traces have fewer squares and a lower loop inductance.

In this geometry, there is significant cancellation of the self-magnetic field lines around one conductor from the mutual field lines from the other conductor. The estimate above for the sheet inductance of a pair of planes is based on the parallel plate approximation, which assumes the width is much larger than the dielectric thickness. When the width is less than 10 times the dielectric thickness, this assumption is no longer reasonable and the parallel plate sheet inductance must be modified. Figure 4.18 shows the parallel plate loop inductance per length compared to the results from a 2D field solver, as the line width to dielectric thickness is varied.



**Figure 4.18** The parallel plate approximation for loop inductance of a narrow trace over a plane, compared to the results from a 2D field solver, simulated with Keysight's ADS.

Generally, as the line width to dielectric thickness decreases, the loop inductance does not increase as fast as would be expected in the parallel plate approximation. As a rough rule of thumb, when the aspect ratio is 10 to 1, the error in the parallel plate approximation for the loop inductance is about 30%. When the aspect ratio is 1 to 1, the error is 300%.

#### Tip

You should not use the parallel plate approximation for the loop inductance of a trace over a plane if the aspect ratio of line width to dielectric thickness is smaller than 10 to 1.

#### Tip

When the line width = the dielectric thickness, the loop inductance per inch is about 10 nH/inch. This is a good rule of thumb to remember.

As the line width decreases, the loop inductance increases, but not linearly with the width. When the conductor width becomes comparable to the dielectric spacing to the return plane, the conductor begins to look more and more like a round conductor. The external magnetic field lines also turn more circular as the line width decreases.

As we saw in [Figure 4.14](#) for a circular rod over a return plane, the loop inductance varies with the inverse of the log of the rod diameter. This is a slower function than increasing with the inverse of the line width. In [Figure 4.18](#), we see that for narrower aspect ratios, when the line width is small compared with the dielectric spacing to the return, the inductance increases with a softer dependence that can approximate the inverse of the log of the line width. The result is that for small aspect ratio, narrow conductors, the loop inductance is lower than expected from the parallel plate approximation.

We can also see this by considering the properties of fringe field capacitance. The narrower the trace, the larger the capacitance compared to the parallel plate electric field lines. This is due to the fringe electric field lines that extend from the edges of the narrow trace to the return plane. To account for the higher capacitance using the parallel plate approximation, it is as if the trace were a little wider than the geometrical width.

Likewise, the loop inductance from the 2D field solver is lower than the parallel plate approximation. To use the parallel plate approximation to account for the lower loop inductance, it is as if the line width were a little wider.

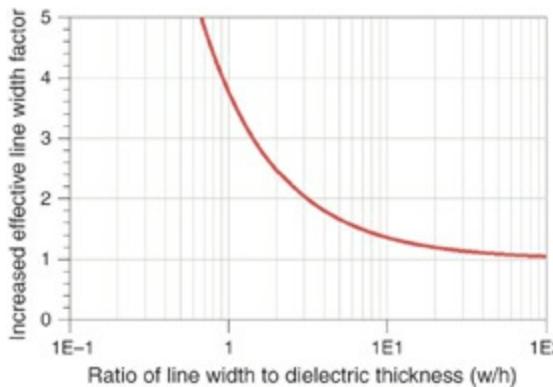
The parallel plate approximation is in the form of

$$L_{\text{loop}} = \mu_0 \times h \times \frac{Len}{w} \quad (4.55)$$

We can describe an effective or equivalent line width based on the loop inductance from a 2D field solver as

$$w_{\text{eff}} = \mu_0 \times h \times \frac{\text{Len}}{L_{\text{loop}}[2D]} \quad (4.56)$$

As we change the line width, the 2D field solver calculates the loop inductance and the equivalent line width. Figure 4.19 shows the ratio of the effective line width to the geometrical line width as the aspect ratio of the actual line width to dielectric thickness changes. This is a rough measure of how much the line acts wider than the geometric line width for narrower aspect lines over planes.



**Figure 4.19** Increased effective line width for the parallel plate approximation to account for the loop inductance based on a 2D field solver, simulated with Keysight's ADS.

#### 4.14 APPROXIMATIONS FOR THE LOOP INDUCTANCE OF ANY UNIFORM TRANSMISSION LINE

When the loop is constructed from a length of uniform transmission line and composed of the signal and its return path, typically with one or two planes, a simple way exists for estimating the loop inductance from the characteristic impedance of the transmission line and its time delay.

A uniform transmission line is a structure that has a constant cross section down its length. Over its total

length, there is a total capacitance and a total loop inductance. If the cross section is constant down its length, every equal length section of the transmission line has the same capacitance and the same loop inductance.

Applying simple transmission line analysis, we derive the two terms that characterize the transmission line, its characteristic impedance ( $Z_0$ ) and time delay (TD), in terms of the total L and C of the transmission line as

$$Z_0 = \sqrt{\frac{L}{C}} \quad \text{and} \quad TD = \sqrt{LC} \quad (4.57)$$

With a little algebra, we rearrange these to relate the total loop inductance in terms of the characteristic impedance and time delay as

$$L = TD \times Z_0 \quad (4.58)$$

where

$L$  = the total loop inductance of the transmission line  
in nH

$TD$  = the time delay of the transmission line in nsec

$Z_0$  = the characteristic impedance of the transmission line in  $\Omega$

For example, if the line impedance is  $50 \Omega$  and the time delay is  $1\text{n sec}$ , or roughly 6 inches in length for an FR4 interconnect, the loop inductance of this transmission line is

$$L = TD \times Z_0 = 1\text{n sec} \times 50\Omega = 50\text{nH} \quad (4.59)$$

This relationship applies to *every* uniform transmission line, regardless of its size, shape, or cross-sectional area, provided it is uniform down its length. This identifies a very important relationship. Every

physical feature that increases the characteristic impedance of a transmission line also increases the loop inductance of the structure.

**Tip**

Every uniform transmission line with the same dielectric material and the same characteristic impedance has exactly the same inductance per length, independent of the cross section.

**Tip**

Every feature in a transmission line that increases its characteristic impedance also increases its inductance per length.

Bringing the signal and return conductors closer together decreases the characteristic impedance and the loop inductance. Making the conductors wider decreases the characteristic impedance and the loop inductance. Finally, decreasing the length of the transmission line decreases the time delay and the loop inductance.

Relating the loop inductance and physical length of the interconnect is often convenient. From the length and effective  $Dk_{eff}$ , we evaluate the time delay as

$$TD = \frac{Len}{v} = \frac{Len}{c} \sqrt{Dk_{eff}} \quad (4.60)$$

where

$TD$  = the time delay in nsec

$Len$  = the physical length of the transmission line in inches

$v$  = velocity of a signal in inch/nsec

$c$  = the speed of light in air, 11.8 inch/nsec  $\sim 12$  inches/nsec

$Dk_{eff}$  = the effective dielectric constant, which includes any contributions from air above the trace, for example

In general, the loop inductance per length of any uniform transmission line structure is

$$L_{\text{len}} = \frac{L}{\text{Len}} = \frac{\sqrt{Dk_{\text{eff}}}}{c} \times Z_0 \quad (4.61)$$

In the special case of interconnects in FR4, with a  $Dk_{\text{eff}} \sim 4$ , we can approximate the total loop inductance per length as

$$L_{\text{len}} [\text{nH/inch}] = \frac{\sqrt{Dk_{\text{eff}}}}{c} \times Z_0 = \frac{\sqrt{4}}{12} \times Z_0 = \frac{1}{6} \times Z_0 \quad (4.62)$$

In the special case of  $50 \Omega$  lines in FR4, the loop inductance per length is about

$$L_{\text{len}} [\text{nH/inch}] = \frac{1}{6} \times Z_0 = \frac{1}{6} \times 50 = 8.3 \text{nH/inch} \quad (4.63)$$

A uniform,  $50 \Omega$  transmission line in FR4, regardless of its specific cross section, has a loop inductance per length of  $8.3 \text{ nH/inch}$ . This is a simple rule of thumb to remember.

#### Tip

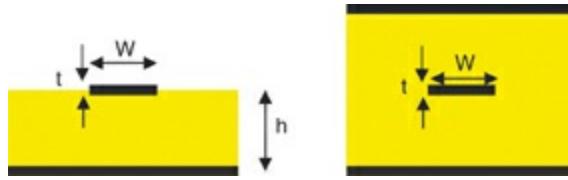
As a good rule of thumb, every  $50 \Omega$  line in FR4, regardless of its specific features, has a loop inductance per length of about  $8.3 \text{ nH/inch}$ .

For example, a  $50 \Omega$  embedded microstrip transmission line with a width of 10 mils has a dielectric thickness of about 5 mils. Such a line 2 inches long has a loop inductance of  $2 \times 8.3 = 16.6 \text{ nH}$ . This is the loop inductance of the signal and its return path in the plane directly beneath the signal line. The loop inductance for this structure estimated from sheet inductance is

$$L_{\text{loop}} = \mu_0 \times h \times \frac{\text{Len}}{w} = \left( 32 \text{ pH/mil} \times 5 \text{ mils} \times \frac{2000 \text{ mils}}{10 \text{ mils}} \right) = 32 \text{ nH} \quad (4.64)$$

This is a factor of 2 too high, because the aspect ratio is not very large. The parallel plate approximation, the basis of the sheet inductance calculation, is an overestimate of the loop inductance for this low-aspect ratio interconnect.

We can use a number of simple approximations for the characteristic impedance of microstrip and stripline structures to roughly approximate their characteristic impedance from cross-section information. [Figure 4.20](#) illustrates these cross-section geometries.



**Figure 4.20** Cross sections for microstrip and stripline transmission lines.

A popular IPC approximation for the characteristic impedance of a microstrip is

$$Z_0 = \frac{87}{\sqrt{Dk + 1.4}} \ln \left( \frac{6 \times h}{(0.8w + t)} \right) \quad (4.65)$$

From which the loop inductance per length for an FR4 microstrip is approximately

$$L_{len} = \frac{\sqrt{Dk}}{c} \times Z_0 = \frac{87}{12} \frac{\sqrt{Dk}}{\sqrt{Dk + 1.4}} \ln \left( \frac{6 \times h}{(0.8w + t)} \right) = 6.24 \text{nH/inch} \times \ln \left( \frac{6 \times h}{(0.8w + t)} \right) \quad (4.66)$$

For stripline, the characteristic impedance is roughly

$$Z_0 = \frac{60}{\sqrt{Dk}} \ln \left( \frac{1.9 \times (2h + t)}{(0.8w + t)} \right) \quad (4.67)$$

from which the loop inductance per length is approximately

$$L_{len} = \frac{\sqrt{Dk}}{c} \times \frac{60}{\sqrt{Dk}} \ln \left( \frac{1.9 \times (2h + t)}{(0.8w + t)} \right) = 5 \text{nH/inch} \times \ln \left( \frac{1.9 \times (2h + t)}{(0.8w + t)} \right) \quad (4.68)$$

where

$Z_0$  = the characteristic impedance in  $\Omega$

$Dk$  = the dielectric constant of the bulk laminate material

$c$  = speed of light in air, 11.8 inches/nsec

$h$  = the dielectric thickness between the signal and return plane in mils

$w$  = the line width of the signal conductor in mils

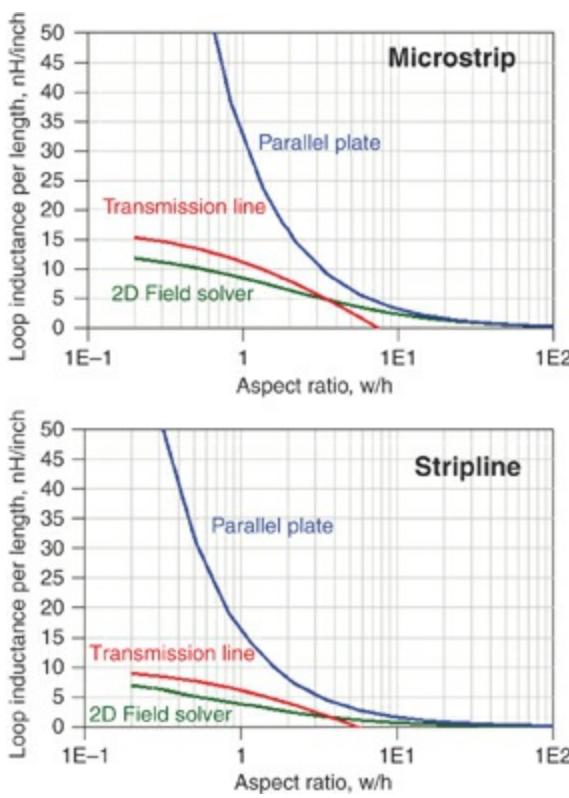
$t$  = the thickness of the signal conductor in mils

Of course, if the signal line is offset from the center in the stripline, or the shape of the conductor is not rectangular, or if more accurate values are needed, you should not use these approximations. A 2D field solver would be the right tool. These relationships are for rough estimates of the characteristic impedance from which you can estimate the loop inductance.

**Tip**

You can use any approximation for the characteristic impedance of a transmission line to estimate the loop inductance per length of the structure. If an accurate estimate of the loop inductance per length of a long, narrow, uniform trace is required, you should use a 2D field solver.

As an example of the accuracy of these two approximations, [Figure 4.21](#) compares the loop inductance per length for microstrip and stripline structures using a 2D field solver, the parallel plate approximation, and the transmission line approximations from [Equations 4.65](#) and [4.66](#).



**Figure 4.21** Comparing calculated loop inductance per length of microstrip and stripline structures using the parallel plate approximation, the transmission line approximation, and a 2D field solver. This is with a  $Dk = 4$  and trace thickness of 0.7 mils. Simulated with Keysight's ADS.

Whereas the transmission line approximations are reasonable for aspect ratios less than about 3, the parallel plate approximation is reasonable for aspect ratios greater than 3.

**Tip**

Whereas the transmission line approximations are reasonable for aspect ratios less than about 3, the parallel plate approximation is reasonable for aspect ratios greater than 3.

The relationship between the loop inductance and characteristic impedance applies to *all* uniform transmission lines geometries. This is especially useful when using a 2D field solver to calculate the characteristic impedance.

#### 4.15 A SIMPLE RULE OF THUMB FOR LOOP

## INDUCTANCE

An important principle that applies in many everyday practical design situations is that

“Sometimes an OK answer NOW! is better than a good answer later.”

Although we offered a number of approximations earlier to estimate the loop inductance of a pair of conductors, sometimes just having a quick estimate to use immediately is valuable as a way of estimating an order of magnitude. Two different estimates hint at a simple rough approximation that we can use for the total inductance per length of a conductor and scale to the loop inductance of any length loop.

We showed in the example in [Figure 4.16](#) that for a circular loop of 24-gauge wire, the loop inductance per inch is about 25 nH/inch of circumference for 0.5 to 3 inch radius loops.

The partial self-inductance of a straight wire, is approximately

$$L_{\text{self}} = 5 \times Len \times \left\{ \ln\left(\frac{2 \times Len}{r}\right) - 0.75 \right\} \quad (4.69)$$

where

$L_{\text{self}}$  = the partial self-inductance of the round rod, in nH

$Len$  = the length of the rod in inches

$R$  = the radius of the rod in inches

In the specific case of 30-gauge wire approximately 10 mil in diameter, 1-inch long, the partial self-inductance is about

$$L_{\text{self}} = 5 \times Len \times \left\{ \ln\left(\frac{2 \times Len}{r}\right) - 0.75 \right\} = 5 \times 1 \times \left\{ \ln\left(\frac{2 \times 1}{0.01}\right) - 0.75 \right\} = 23 \text{ nH} \quad (4.70)$$

Although partial self-inductance does not scale precisely with length, for the special case of 30-gauge wire, 1-inch-long, the approximate partial self-inductance is about 25 nH/inch. This would be roughly the total inductance of the rod, if the return conductor were far away.

Both of these rough estimates suggest the same simple rule of thumb for the loop inductance of a conductor as

$$L_{\text{loop}} \approx 25 \text{nH/inch} \times \text{Len} = 1 \text{nH/mm} \times \text{Len} \quad (4.71)$$

Of course, the inductance of a loop depends on the cross section, length, and shape of the conductors; but as a rough number, the loop inductance per length of a narrow conductor with its return far away, such as a via, can be approximated as about 25 nH/inch of length of circumference, which has the simple form, 1 nH/mm.

When you need a quick estimate of the loop inductance of narrow conductors, 25 nH/inch or 1 nH/mm is a good starting place. When you need a more accurate value, especially for wide conductors close together, use one of the better approximations discussed in [section 4.14](#).

**Tip**

When you need a quick estimate of the loop inductance of narrow conductors, 25 nH/inch or 1 nH/mm is a good starting place.

When you need a more accurate value, especially for wide conductors close together, use one of the better approximations discussed in [section 4.14](#).

## 4.16 ADVANCED TOPIC: EXTRACTING LOOP INDUCTANCE FROM THE S-PARAMETERS CALCULATED WITH A 3D FIELD SOLVER

Although approximations are powerful tools to explore design space and the impact of design decisions on

performance to quickly get to an answer, sometimes the higher accuracy, and in particular the higher confidence, of a 3D field solver result is important.

For geometry that can be any arbitrary size and shape with possible complications of coupling to odd-shaped plane or fringe field-dominated structures (such as via clearance holes), the only tool that has a chance of giving a reasonable answer is a 3D field solver, which solves for the electromagnetic fields using Maxwell's Equations and the boundary conditions of the conductors and dielectrics. As is often said about super heroes, with incredible power comes the possibility of incredible harm. You can almost always get an answer from a 3D field solver. The challenge is getting an answer that is relevant for solving the problem you have and confidence in the result.

**Tip**

With incredible power comes the possibility of incredible harm.  
You can almost always get an answer from a 3D field solver. The challenge is getting an accurate answer that is relevant for solving the problem you have and confidence in the result.

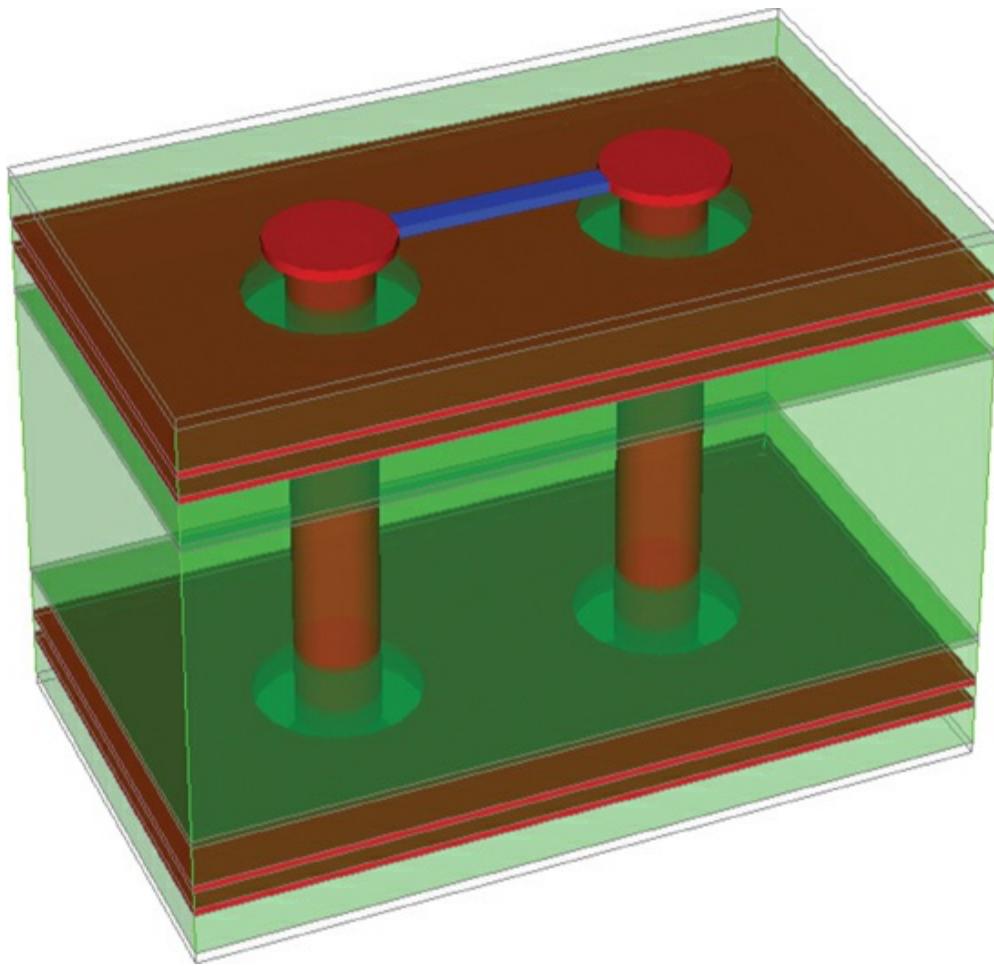
You can only achieve this through considerable effort learning, not just how to drive the tool but how to integrate it into your design flow and partition your design into bite-sized pieces your field solver can handle.

The most common output of a 3D field solver is in the form of S-parameters, based on the “ports” assigned to the problem. The ports are the signal-return connections into which either electromagnetic waves are injected or voltage sources are placed, and the scattered waves from these ports then calculated. The S-parameters calculated at the selected frequencies contain all the important information about the

properties of the structure.

In the special case of small structures for the PDN, you can use the S-parameters calculated and extract the effective loop inductance of the structure being simulated. The example used to illustrate this process is a simple structure modeling a power-ground via pair that connects the BGA solder balls on the bottom of a package to the decoupling capacitor on the bottom of the board. This would be the configuration typical of a capacitor mounted between the vias under a BGA.

Figure 4.22 shows the 3D geometry model as brought into Simbeor, a 3D field solver from Simberian Inc [7].



**Figure 4.22** Example of a pair of power and ground vias under a BGA as represented in Simbeor, a 3D field solver tool. The bar between the two via pads is the designated port on top. A comparable port is between the two vias on the bottom, which is hidden in this figure.

This particular problem is set up as a two-port

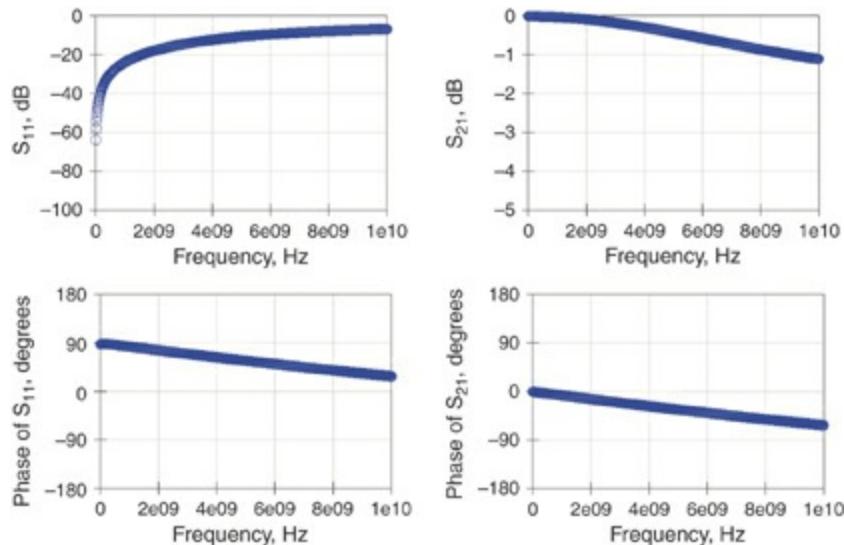
problem. The port on the top of the board, port 1, connects between the pads of the power ball to the ground ball of the BGA. Port 2 is the connection between the two vias on the bottom of the board where the decoupling capacitor would be mounted. This example is for an eight-layer board with a total thickness of 62 mils. The vias are 10 mils in diameter on a 40 mil pitch.

Using the approximation for the loop inductance of a twin rod geometry, we expect the loop inductance per linear length of these vias to be roughly:

$$L_{\text{Len}} = \frac{\mu_0}{\pi} \ln \left( \left( \frac{s}{2r} \right) + \sqrt{\left( \frac{s}{2r} \right)^2 - 1} \right) = \frac{\mu_0}{\pi} \ln \left( \left( \frac{40}{10} \right) + \sqrt{\left( \frac{40}{10} \right)^2 - 1} \right) = 21 \text{ pH/mil} \quad (4.72)$$

In a board 62 mils thick, the expected loop inductance is  $21 \text{ pH/mil} \times 62 \text{ mils} = 1.30 \text{ nH}$ .

The output from the 3D field solver is a two-port S-parameter file. [Figure 4.23](#) shows the return and insertion loss for this simulation.



**Figure 4.23** S-parameter values simulated for this two-port via pair from the top of the board to the bottom of the board, using Simbeor.

We could directly use this S-parameter file in a circuit simulation of the PDN by adding an ideal capacitor and

series resistor element to simulate the presence of a decoupling capacitor on the bottom of the board. The circuit simulation would reveal the impact of this via pair and capacitor in the system simulation. In this application, the S-parameters are treated as a “black box” behavioral model, with no interest in what is going on “inside the box.”

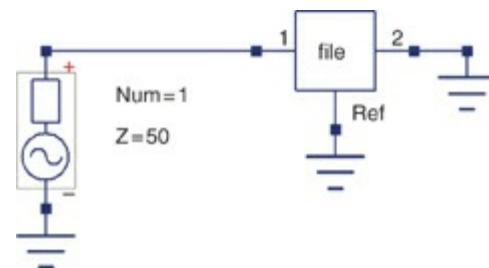
Tip

An S-parameter model for a pair of vias can be directly incorporated in a circuit stimulation. However, it is not scalable. If any changes are made to the via design, the S-parameter model must be resimulated for the new structure. This is one of the advantages of using a simple, scalable circuit topology model. Seeing the impact on the system simulation of a change in a physical parameter is quick and easy.

Although this 3D model could account for the impact from the via connection to the capacitor, we can gain little insight by inspecting the S-parameter file itself, without doing a system simulation.

However, the possibility exists to “data mine” useful performance metrics, such as the loop inductance of the vias, directly from the S-parameters.

The first step is to simulate the one-port S-parameters of the via pair, when the far end port is shorted together. This becomes the configuration of looping the current down one via and back up the other. Figure 4.24 illustrates this circuit.



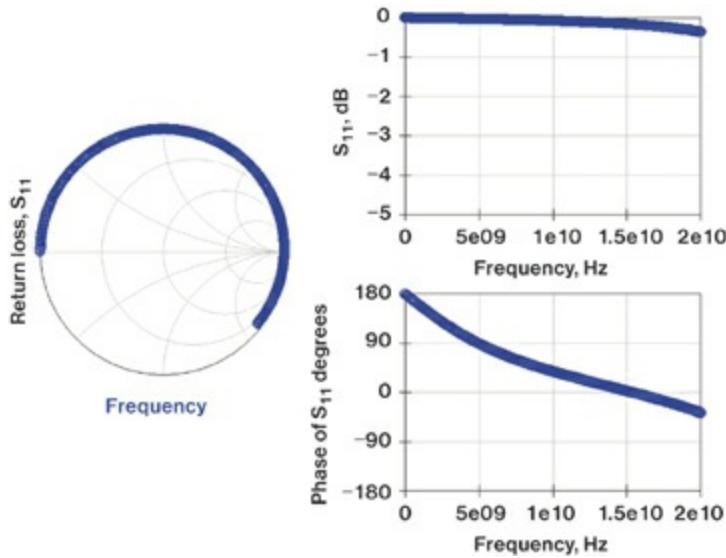
**Figure 4.24** Circuit that simulates the return loss when port 2 is shorted, using QUCS in this example.

The return loss, ( $S_{11}$ ) in this configuration, is a direct

measure of the reflected signal from the  $50 \Omega$  source impedance of port 1 by the loop inductance of the via pair. Because it looks at a short at the far end, we would expect to see a simulated return loss that has a 180-degree phase shift and starts on the far left edge of a Smith chart. [Figure 4.25](#) shows the simulated  $S_{11}$  in both a Smith chart and as magnitude and phase over frequency. It is exactly as expected for a low impedance, nearly a short.

#### Tip

We can extract loop inductance of a two-port structure as long as we short one port of the device and create a loop. We do this by resimulating the S-parameters with the port impedance of port 2 changed to  $0 \Omega$ .



**Figure 4.25** Simulated return loss of a via pair with their far end shorted together, in a Smith chart and magnitude and phase over frequency.

The return loss is the reflection coefficient, as a signal reflects from an impedance,  $Z_2$ , coming from an impedance,  $Z_1$ , and derived with

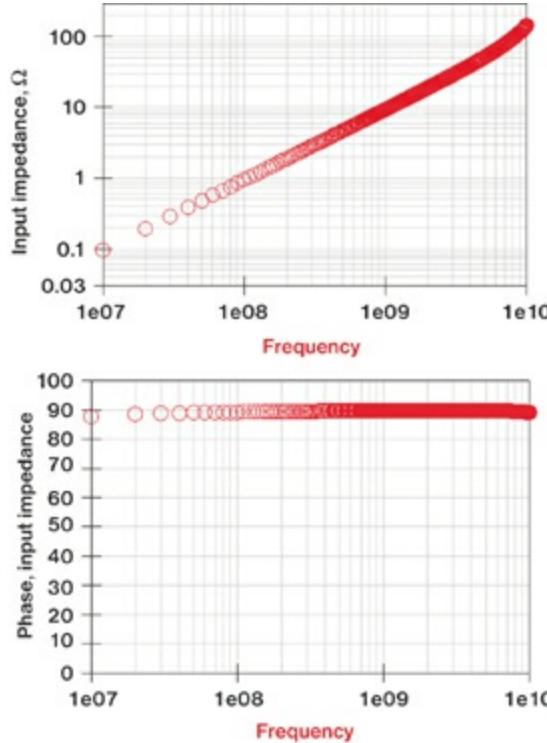
$$S_{11} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad (4.73)$$

When the source impedance  $Z_1$  is  $50 \Omega$ , the return

loss is a direct measure of the input impedance looking into the loop formed by the via pair, derived with

$$Z_{\text{input}} = Z_2 = 50 \Omega \frac{1 + S_{11}}{1 - S_{11}} \quad (4.74)$$

Because the return loss is complex, the input impedance will be complex. Figure 4.26 shows the simulated return loss and extracted input impedance as magnitude and phase.



**Figure 4.26** The calculated input impedance as magnitude and phase, from the simulated return loss when the far end of the via pair is shorted together.

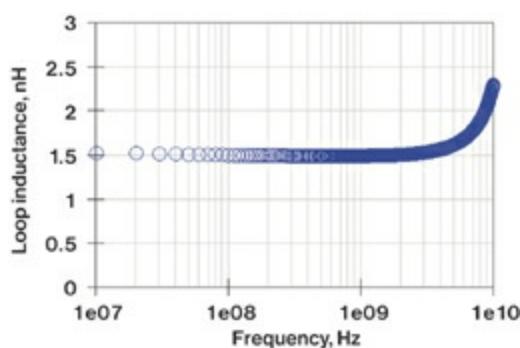
The input impedance calculated from the return loss has the signature of an ideal inductor. We can easily extract the inductance of the via pair from the impedance:

$$L = \frac{\text{imag}(Z_{\text{input}})}{2\pi f}$$

only in spectrum where L dominates, i.e., Z behaves like increasing straight line in log-log plot

$$(4.75)$$

The loop inductance is calculated across the entire frequency range as shown in Figure 4.27.



**Figure 4.27** Extracted loop inductance of the via pair from the simulated S-parameters.

In this way, we can extract the loop inductance of any complex structure from the simulated S-parameters using a 3D field solver. It is interesting to note that the 3D model for this via pair is equivalent to a loop inductance of 1.5 nH, as compared with the estimate from the twin rod approximation of 1.3 nH.

The field solver calculates a slightly higher loop inductance because it also includes the impact from the non-uniform current distribution entering and leaving the vias and some non-uniform magnetic fields at the top and bottom of the via pair.

The 3D simulation also shows that the model of the via pair as a simple ideal inductor is accurate up to about 6 GHz. This limit is imposed when the frequency is reached where the extended structure is longer than  $1/20$  of a wavelength, where it begins to behave like a distributed transmission line.

Using the rule of thumb developed in [section 4.5](#) of this chapter, the upper frequency limit is about 0.6 GHz for a 1-inch structure in air. When dielectric material slows the speed of light down, this upper frequency limit drops to about 0.3 GHz for a 1-inch structure. The via in this example is 0.06 inches long. This is  $1/16$  of an inch. If the length drops by a factor of 16, the upper frequency limit will increase by a factor of 16 to  $0.3 \text{ GHz} \times 16 = 4.8 \text{ GHz}$ . We would expect the quasi-static model

to match the structure up to about 5 GHz. In the extracted inductance shown in [Figure 4.27](#), the inductance is constant up to about 5 GHz, exactly as expected.

## 4.17 THE BOTTOM LINE

1. The loop inductance of the PDN elements limits the impedance of the PDN at high frequency and contributes to the impedance peak heights. This is why decreasing inductance is one of the most important design guidelines for the PDN.
2. Inductance is fundamentally the efficiency of creating rings of magnetic field lines at the cost of current. The more rings of magnetic field lines are created per amp of current, the higher the loop inductance.
3. Inductance is also related to the efficiency of storing energy in the magnetic field around a current loop, per amp of current.
4. Do not confuse the loop inductance of a conductor with the magnetic field density around the conductor. They are not the same. High field density is not always an indication of high inductance.
5. The quasi-static approximation for loop inductance is a good approximation as long as the physical size of the loop is less than about  $1/20$  of a wavelength in extent. In air, the quasi-static approximation is good up to a GHz frequency that is numerically  $0.6/\text{length}$  in inches.
6. We can calculate loop inductance exactly for only three simple round conductor geometries. For all other geometries, formulae for loop inductance are only an approximation.
7. In general, three geometrical features can reduce

loop inductance: shorter conductor lengths, wider conductors, and having the signal and return currents closer together.

8. When the conductors look like two planes, the loop inductance of a section shaped like a square has a loop inductance for current going down one edge and returning back through the other, independent of the size of an edge. All squares have the same loop inductance. The inductance for 1 square is called sheet inductance or loop inductance per square.
9. The parallel plate approximation for loop inductance is accurate until the line width is narrower than about 10 dielectric thicknesses.
10. All transmission lines with the same material and the same characteristic impedance have the same loop inductance per length, independent of their actual cross section.

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# Chapter 5. Practical Multi-Layer Ceramic Chip Capacitor Integration

## 5.1 WHY USE CAPACITORS?

Capacitors are an important component in the PDN ecology because they reduce impedance in the frequency band between VRM effectiveness and the chip's clock. The impedance of an ideal capacitor decreases inversely with frequency, as in

$$Z_C = \frac{-j}{\omega C} \quad (5.1)$$

where

$Z_C$  is the impedance of an ideal capacitor

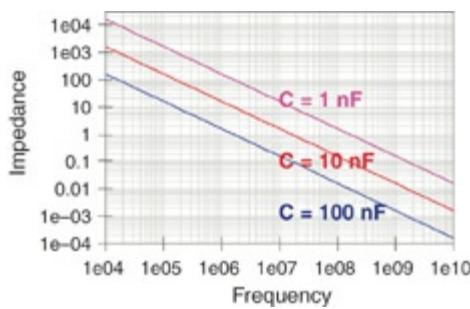
$\omega$  = the angular frequency in radians per second

$C$  = the capacitance in F

As an easy number to remember, the impedance of a 0.1  $\mu$ F capacitor at 1 MHz is about 1  $\Omega$ :

$$|Z_C| = \frac{1}{\omega C} = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 10^6 \times 10^{-9}} \approx 1 \Omega \quad (5.2)$$

Figure 5.1 shows the magnitude of the impedance of three different ideal capacitors. The larger the capacitance, the lower the impedance.



**Figure 5.1** Impedance profile of three different ideal capacitors.

This suggests that the way to achieve low impedance

in the PDN, especially at high frequency, is to just add capacitors to the board. Their impedance will always get lower at high frequency. Unfortunately, as pointed out in [Chapter 2](#), a difference exists between the behaviors of an ideal and a real capacitor.

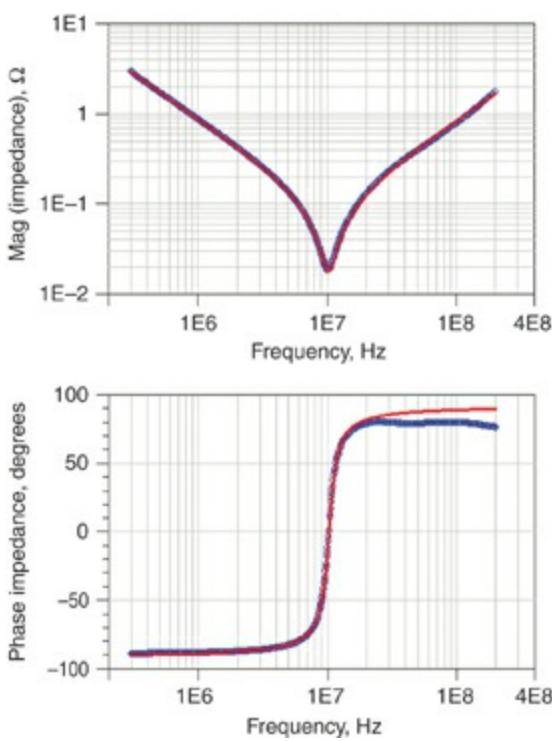
**Tip**

At first glance, capacitors look attractive to reduce the impedance of the PDN but there is a difference between the behavior of an ideal capacitor and a real capacitor. The equivalent series inductance of a real capacitor turns its low impedance into higher impedance behavior at high frequency, complicating its application.

We will leverage design features that influence the ideal C, L, and R elements of the real capacitor to engineer the impedance profile of the PDN, which is composed of single or combinations of capacitors. Having an accurate capacitor model that connects its physical features to an impedance profile is a critical part of the PDN impedance profile design strategy.

## 5.2 EQUIVALENT CIRCUIT MODELS FOR REAL CAPACITORS

A real capacitor mounted to a board only behaves like an ideal capacitor at “low” frequency, well below 1 MHz. However, under most practical design situations, we can model a real capacitor accurately by using a simple ideal series RLC circuit. [Figure 5.2](#) shows the comparison of the measured impedance of a real 0603 Multi-Layer Ceramic Chip (MLCC) capacitor and an ideal series RLC model.



**Figure 5.2** Measured impedance of a real 0603 Multi-Layer Ceramic Chip (MLCC) capacitor (thick line), mounted to a test board, compared to the simulated impedance of an ideal series RLC circuit model (thin line).

**Tip**

Remarkably, the complex impedance behavior of a real capacitor is modeled well by just three ideal circuit elements.

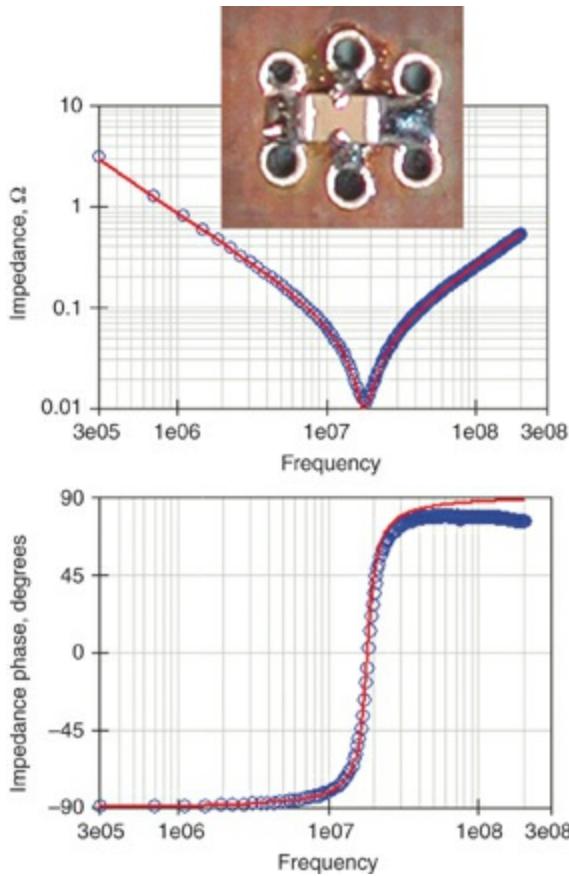
When we refer to the capacitance of a real capacitor we are describing the equivalent capacitance an ideal C element would need to match the series RLC behavior of the real capacitor.

The ESL of a capacitor is the equivalent series inductance needed in a series RLC model to match the behavior of a real capacitor in a specific mounted configuration and measured in a specific way.

The ESR of a real capacitor is the equivalent series resistance needed in a series RLC model to match the behavior of a real capacitor.

The series RLC circuit model is a powerful model to describe real capacitors. In addition to traditional MLCC

capacitors, this simple RLC ideal circuit model can also describe most other capacitor types. Figure 5.3 shows the measured and simulated impedance profile of an X2Y-style capacitor mounted with six vias.



**Figure 5.3** Measured and simulated impedance profile of an 0603 X2Y-style capacitor. The RLC model elements for this simulation are  $R = 0.01 \Omega$ ,  $C = 180 \text{ nF}$ , and  $L = 0.43 \text{ nH}$ . Sample courtesy of X2Y Attenuators.

In this special capacitor design, the two pairs of pads on the ends are connected to power and the center pair of pads are connected to ground. In this respect, this capacitor is connected to the system just like a two-terminal capacitor.

We see the versatility of the simple RLC model in how well it matches the actual measured performance of real capacitors. We can use the RLC model for accurately simulating the performance of arrays of real capacitors. We use this model to explore the important properties of capacitor combinations in the power distribution

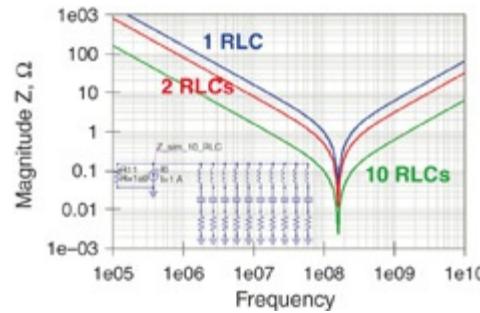
network.

At the end of this chapter we introduce a more advanced model that matches the impedance properties of real capacitors when the mounting inductance associated with them is well below 1 nH.

### 5.3 COMBINING MULTIPLE IDENTICAL CAPACITORS IN PARALLEL

When two identical RLC circuits are connected in parallel, the behavior is similar to that of an RLC circuit. It has the same shape of an RLC circuit but the element values of the new impedance profile are different.

Figure 5.4 shows the resulting impedance profile when 2 and then 10 identical capacitors are added in parallel.



**Figure 5.4** Simulated impedance profile of ten identical series RLC circuits with one RLC circuit, two RLC circuits, and ten identical RLC circuits in parallel.

The shape of the impedance profile for 10 RLC circuit models in parallel is identical to that of a single RLC model but with different values for each equivalent R, L, and C element.

At low frequency, the impedance of the 10 elements in parallel corresponds to an equivalent capacitance that is 10 times the capacitance of a single C. At high frequency, the impedance of the 10 elements in parallel is lower, corresponding to an equivalent inductance that is 1/10 the inductance of each L element. At the series self-resonant frequency (SRF), the lowest impedance of the 10 elements in parallel is equivalent to a lower R

value, equivalent to 1/10 the resistance of each R element.

The scaled values of the equivalent RLC model that has the equivalent behavior as the single RLC circuit are

$$C_n = n \times C_1 \quad (5.3)$$

$$L_n = \frac{L_1}{n} \quad (5.4)$$

$$R_n = \frac{R_1}{n} \quad (5.5)$$

where:

$C_1$  = the capacitance of the single C in the RLC model

$L_1$  = the inductance of the single L in the RLC model

$R_1$  = the resistance of the single R in the RLC model

$C_n$  = the equivalent C in an RLC model that has the same impedance as the n RLC elements in parallel

$L_n$  = the equivalent L in an RLC model that has the same impedance as the n RLC elements in parallel

$R_n$  = the equivalent R in an RLC model that has the same impedance as the n RLC elements in parallel

The scaling of similar capacitors has important consequences for PDN design. By adding multiple capacitors in parallel, the resulting impedance performance is identical to that of a single capacitor, which has more capacitance and less inductance. This is an important way of engineering lower inductance.

In practice, the inductance of a real capacitor is composed of two parts: the loop inductance of the interconnect path of the capacitor mounted to the board and the spreading inductance in the cavity from the capacitor location to the device it is decoupling. The

mounting inductance is the portion that decreases with the number of capacitors added in parallel. Their spreading inductances combine in complicated ways depending on the overlap in the current distribution in the power and ground cavity from the various capacitors.

Note also that the SRF of multiple, identical capacitors in parallel does not change. We can see this from the relationship between the SRF value and the L and C values:

$$\text{SRF}_n = \frac{159}{\sqrt{L_n C_n}} \text{ MHz} = \frac{159}{\sqrt{\frac{1}{n} L_1 n C_1}} \text{ MHz} = \frac{159}{\sqrt{L_1 C_1}} \text{ MHz} = \text{SRF}_1 \quad (5.6)$$

SRF -- no change

Likewise, the equivalent q-factor of n identical capacitors in parallel,  $q\text{-factor}_n$ , is the same as the q-factor of each individual capacitor,  $q\text{-factor}_1$ :

$$q\text{-factor}_n = \frac{1}{R_n} \sqrt{\frac{L_n}{C_n}} = \frac{n}{R_1} \sqrt{\frac{L_1}{n^2 C_1}} = \frac{1}{R_1} \sqrt{\frac{L_1}{C_1}} = q\text{-factor}_1 \quad (5.7)$$

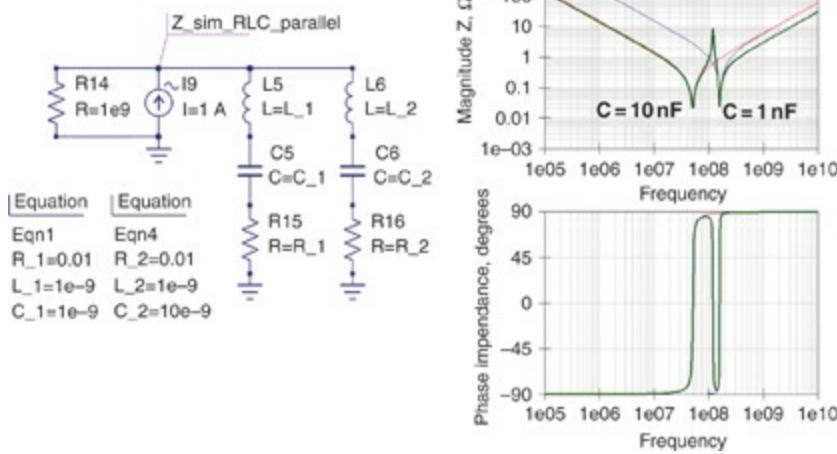
q-factor -- no change

#### Tip

When identical capacitors are added in parallel, the resulting impedance is the impedance of one capacitor scaled to lower value across the entire frequency range with the same SRF and q-factor of each individual capacitor.

## 5.4 THE PARALLEL RESONANCE FREQUENCY BETWEEN TWO DIFFERENT CAPACITORS

When two series RLC circuits are added in parallel, but with different self-resonant frequencies, a new behavior emerges in their combined impedance profile. Figure 5.5 shows the simulated impedance profile of two different ideal series RLC circuits in parallel. In this example, the R and L values are the same in the two different circuits, but the C values differ by 10 times.



**Figure 5.5** Simulated impedance profile for two series RLC circuits in parallel with values of  $R = 0.01 \Omega$ ,  $L = 1 \text{ nH}$ ,  $C = 1 \text{ nF}$ , and  $C = 10 \text{ nF}$ . Note the SRF of the circuit with the larger capacitance is at a lower frequency than the SRF of the circuit with the smaller capacitance.

We see a peak in the impedance profile between the SRFs of the individual RLC circuits. This is the signature of a parallel resonance.

For comparison, the impedance profile of each series RLC circuit by itself is also shown. Again, we see that at the low-frequency end, the impedance behavior of the parallel combination is dominated by capacitance and at the high-frequency end, by inductance. In the middle, we have the new behavior, a peak in the impedance.

At low frequency, the two series circuits are effectively connected in parallel and the equivalent capacitance of the two RLC circuits is the parallel combination of the two capacitors, which is just their sum,  $C_1 + C_2$ .

At high frequency, the two circuits are effectively connected in parallel and the equivalent inductance of the two series RLC circuits is the parallel combination of their inductances, derived with

$$L_{\text{equiv}} = \frac{L_1 \times L_2}{L_1 + L_2} \quad (5.8)$$

At the parallel resonant frequency, the two series circuits are also connected in parallel. When the parallel circuit is excited by the high impedance constant current source, current flows back and forth through the two series RLC circuits. By measuring at the middle of the circuit, we are teasing the parallel RLC circuit into resonance and measuring at the voltage generated.

Current at resonance flows back and forth through the two series circuits, which means that the resonant current is flowing around a loop involving the two series circuits. The equivalent capacitance is the series combination of the two capacitors. Likewise, the equivalent inductance is the series combination of the two inductors. However, from the point of view of the 1 A current source, a portion of the equivalent capacitance and inductance are in parallel and show a parallel resonance.

The properties we measure at the parallel resonant frequency are related to the series combination of the L and C elements in the two series RLC circuits.

**Tip**

Combining two series RLC circuits in parallel causes a new behavior to emerge and creates a peak impedance. This is due to the resonance of the two series RLC circuits excited in parallel and is referred to as a parallel resonance. Parallel resonant peaks are the most important feature of any PDN.

The peak resonant frequency is due to an interaction between the lower SRF RLC circuit trying to increase the total circuit's impedance while the higher SRF RLC circuit is trying to decrease the total circuit's impedance.

The peak impedance occurs at the *parallel resonant frequency* (PRF), where the reactances of the impedances of these two RLC circuits are equal and cross.

This condition is

$$X_1 = X_2 \quad \text{or} \quad \omega L_1 - \frac{1}{\omega C_1} = \omega L_2 - \frac{1}{\omega C_2} \quad (5.9)$$

We can extract the value of the parallel resonant frequency from this condition as

$$\text{PRF} = \frac{\omega}{2\pi} = \frac{159 \text{ MHz}}{\sqrt{(L_1 + L_2) \left( \frac{1}{C_1} + \frac{1}{C_2} \right)}} \quad (5.10)$$

where

$X_1$  = the reactance of the lower frequency series RLC circuit

$X_2$  = the reactance of the higher frequency series RLC circuit

$L_1$  = the inductance of the larger C circuit, in nH

$C_1$  = the capacitance of the larger C circuit, in nF

$L_2$  = the inductance of the small C circuit, in nH

$C_2$  = the capacitance of the small C circuit, in nF

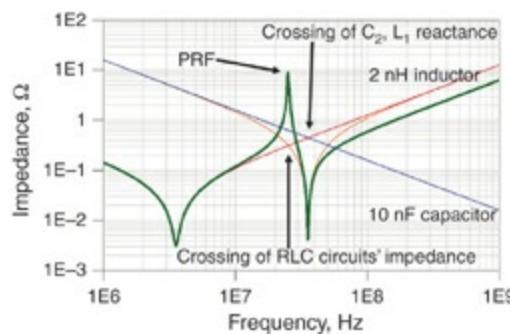
PRF is the parallel resonant frequency in MHz

For example, if the inductance in the two series RLC circuits is 2 nH, the capacitance of the smaller capacitor is 10 nF, and the capacitance of the larger capacitor is 1000 nF, the PRF is

$$\text{PRF} \sim \frac{159 \text{ MHz}}{\sqrt{(2+2)\text{nH} \times \frac{1}{\frac{1}{10} + \frac{1}{1000}} \text{nF}}} = 25.3 \text{ MHz} \quad (5.11)$$

Figure 5.6 shows the simulated impedance profile of two series RLC circuits with C and L values, as shown in Figure 5.5. The simulated PRF is exactly as predicted

with this simple analysis.



**Figure 5.6** Simulated parallel resonance compared to the impedances of the individual RLC circuits. The PRF occurs at the resonance of the series combination of the inductances and the series combination of the capacitances.

## 5.5 THE PEAK IMPEDANCE AT THE PRF

The peak value of the impedance at the PRF is difficult to accurately calculate analytically but we can simulate it. When the two capacitors have a large difference in values, but their ESL values are the same, the peak impedance varies, related to the following three groups of terms:

$$Z_{\text{peak}} \propto \left( \frac{1}{R_1 + R_2} \right) \frac{L_1}{C_2} \quad (5.12)$$

where

$Z_{\text{peak}}$  = the peak impedance at the parallel resonance frequency

$L_1$  = the inductance of either capacitor, in nH

$R_1$  = the resistance in the lower frequency SRF circuit

$R_2$  = the resistance in the higher frequency SRF circuit

$C_2$  = the capacitance of the higher frequency SRF circuit

This relationship hints at the design knobs that we can adjust to reduce the peak parallel resonant impedance. The way to reduce the peak impedance is

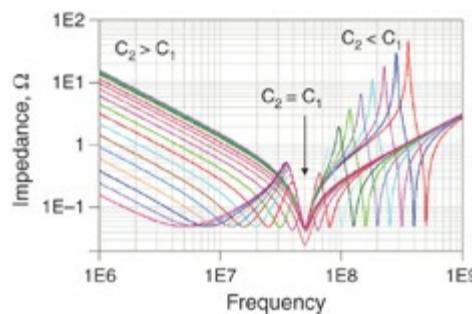
- Larger capacitance of the higher frequency SRF circuit (move capacitor values closer together)
- Smaller equivalent series inductance of the lower frequency SRF circuit
- Larger  $R_1$  and  $R_2$

**Tip**

The most important goal in robust PDN design is to reduce the peak impedances below the target impedance. We do this by leveraging the three design knobs when using multiple capacitors in parallel: closer distribution of capacitor values, lower mounting ESL, and larger capacitor ESR.

Using a simple SPICE simulation of the impedance of the two RLC circuits in parallel, we can explore design space to see the interactions between each of the features of the two circuits and the impact on the peak impedance.

In the first example, we fix the loop inductance of each capacitor at 1 nH and the ESR of each capacitor, constant at 50 m $\Omega$ . One capacitor is fixed at 10 nF and the other is swept from 0.1 nF to 1000 nF. This sweeps out a range of relative capacitor values from 1% to 100 times the fixed value. [Figure 5.7](#) shows the impedance profile of the two parallel circuits for different ratios of the two capacitors.



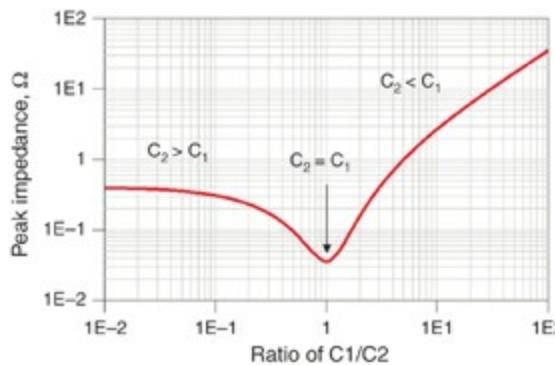
**Figure 5.7** Impedance profile of the two series RLC circuits when  $C_1$  is held constant and just  $C_2$  is varied. The ratio of  $C_1$  to  $C_2$  varies from 1% to 100 times  $C_1$ .

Simulated with Keysight ADS.

With a constant ESR across frequency and using the same value for the two capacitors, we see the minimum impedance, occurring at the SRF of each capacitor, is just the ESR of each capacitor. However, in the special case when  $C_2 = C_1$ , both capacitors are identical, they each have the same SRF and the minimum impedance of  $1/2$  the ESR of either one. The resistances are in parallel.

When  $C_2 < C_1$  and the SRF of circuit 1 is lower than the SRF of circuit 2, making  $C_2$  smaller than  $C_1$  increases the parallel impedance peak. This confirms the design guideline of bringing  $C_2$  closer to  $C_1$  to reduce the peak impedance.

When  $C_2$  is larger than  $C_1$  and the  $\text{SRF}_2 < \text{SRF}_1$ , the peak impedances saturate to a maximum value. Figure 5.8 shows this behavior of the peak impedance as a function of the ratio of  $C_1$  to  $C_2$ .



**Figure 5.8** Peak impedance at the parallel resonance as  $C_2$  only is swept. Note that the biggest impact on reducing the peak impedance is when the ratio of  $C_1/C_2$  is close to 1, within a range of about 0.5 to 2. Simulated with Keysight's ADS.

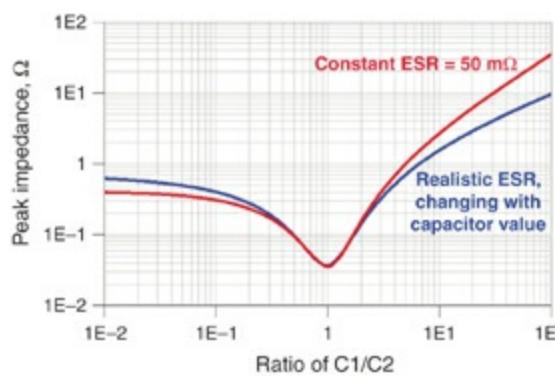
We see very clearly that to reduce the peak impedance, the closer in value  $C_1$  and  $C_2$  are, the lower the peak impedance. Of course, the minimum is when the two capacitors have the same value and the ratio is 1. As the ratio gets bigger or smaller from 1, the peak impedance rises rapidly. The region of sharpest slope

and biggest impact on reduced peak is roughly with a ratio of between a 0.5 times and 2 times on either side of 1. This suggests that the balance between the minimum number of different capacitor values with the biggest impact on reducing peak impedance might be gained if the values of the two capacitors are within a factor of two of each other.

#### Tip

When selecting capacitor values, the biggest impact on reducing the peak impedance with the fewest number of capacitor values is gained if the capacitors' values are within a factor of two of each other. This corresponds to capacitor values spaced about three values per decade. This also assumes about the same ESL for each capacitor.

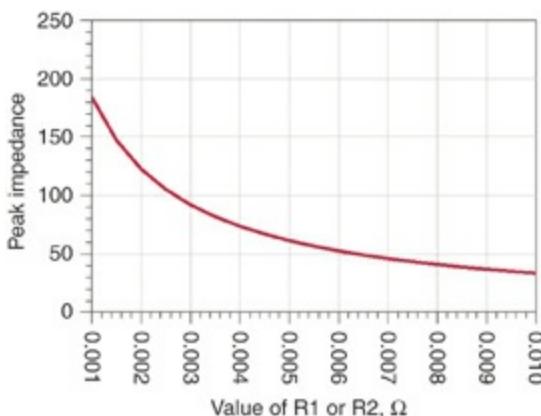
In this example, we assumed the ESR of each capacitor was the same and independent of the value of the capacitance. We show later in the chapter this is not exactly the way real capacitors behave. In reality, smaller value capacitors also have slightly higher ESR. Because higher ESR can reduce the peak impedance, the preceding analysis is affected by the ESR of the capacitor selected. [Figure 5.9](#) shows the impact of the more realistic variation in ESR with capacitor value.



**Figure 5.9** Changing the value of one capacitor from 1% to 100x the other capacitor's value, but using a realistic model for how the ESR changes with capacitor value. This has little impact when values are close, but can have an impact on peak impedances when capacitor values are much farther apart.

When the values of the two capacitors are very close together, the ESR does not vary and there is little impact on the peak impedances using the more realistic ESR model. The peaks are affected only if their values are very far apart. Because the ESR increases as the capacitor value decreases, when  $C_2$  is very small and  $C_1/C_2$  is large, the expected peak impedance is reduced by more than two times using the realistic value of ESR.

Our simple model suggests that when the ESL is the same for the two capacitors, the peak impedance is also related to the sum of the series equivalent resistances. We obtain a lower peak impedance with a higher value of the ESR of either series RLC circuit. Figure 5.10 shows the simulated peak impedance as either  $R_1$  or  $R_2$  is changed from  $0.001 \Omega$  to  $0.01 \Omega$ . Higher ESR results in lower peak impedance.



**Figure 5.10** Peak impedance as either  $R_1$  or  $R_2$  is changed, keeping all other circuit elements constant.

#### Tip

We achieve lower peak impedance if we increase the ESR of either or both capacitors. This is a strong driving force for using controlled ESR capacitors, which have higher ESR than normally found.

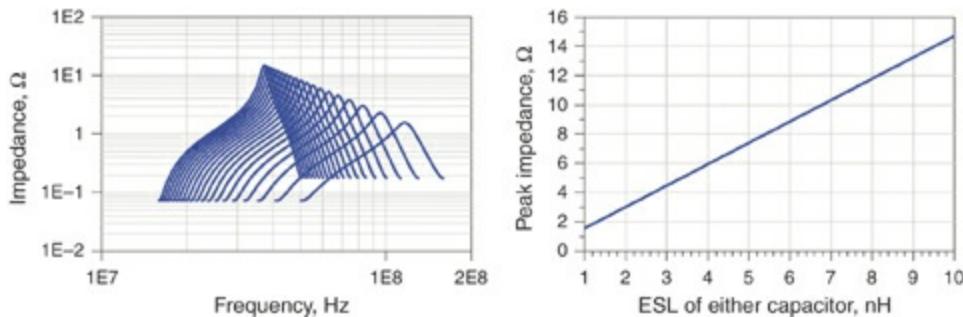
The simple estimate of Equation 5.12 suggests that we can get a lower peak by decreasing the ESL of the lower frequency SRF circuits. Decreasing only  $L_1$  increases the SRF of the lower frequency SRF circuit to higher

frequency and brings the SRFs of the two RLC circuits closer together. This decreases the peak impedance.

However, decreasing only  $L_2$  increases the SRF of the second circuit, which separates the SRFs. The peak increases slightly to a limiting value.

Decreasing both  $L_1$  and  $L_2$  by the same amount, as is typical when the same mounting geometry is used for all the MLCC capacitors, causes a reduction in the peak impedance. This impact is difficult to estimate analytically but is easy to analyze in simulation.

To illustrate this, we simulated the parallel circuit with all parameters constant except the inductances. In this example  $L_1 = L_2$  and both are decreased. [Figure 5.11](#) shows the change in impedance profile as we change the value of the inductance in each circuit together and the resulting peak height.



**Figure 5.11** Left: Simulated decrease in peak impedance profile of the parallel combination of the two RLC circuits as both  $L_1$  and  $L_2$  decrease. Right: The simulated peak impedance for the case of  $L_1 = L_2$ , simulated with Keysight's ADS.

#### Tip

Reducing the ESL of either or both capacitors always reduces the peak impedance values. Lower ESL is *always* a good design goal to reduce peak impedance.

When we use two different capacitor values, with two different SRFs, the three most important ways to reduce the peak impedance are by

- Bringing the capacitors' values closer together
- Increasing the ESR of each RLC circuit
- Decreasing the ESL of both capacitors

These are the most important driving forces in optimizing the capacitor values and integrating them into the PDN ecology.

## 5.6 ENGINEERING THE CAPACITANCE OF A CAPACITOR

Fundamentally, a capacitor is nothing more than two conductors with a dielectric between them. A multilayer ceramic chip (MLCC) capacitor is actually multiple layers of conductors separated by dielectric in parallel.

Figure 5.12 shows the structure of a parallel plate capacitor.



**Figure 5.12** Typical structure of a parallel plate capacitor and the cross section of an MLCC capacitor showing multiple parallel plates of conductors separated by dielectric.

The amount of charge that can be stored between the conductor planes is related to the overlap area and the spacing between the conductors and the number of pairs of planes in parallel. When the conductors are wide and very closely spaced, the parallel plate approximation provides a simple estimate for the resulting capacitance and is derived with

$$C[\text{pF}] = \epsilon_0 Dk n \frac{A}{h} = 225 Dk n \frac{A[\text{in}]}{h[\text{mils}]} \text{ pF} \quad (5.13)$$

where

$C$  = the capacitance of the capacitor, in pF

$\epsilon_0$  = the permittivity of free space,  $8.85 \times 10^{-12}$  F/m or

0.225 pF/in

Dk = the dielectric constant of the material between the conductors

n = the number of dielectric layers between the parallel plates

A = the area of the overlap, in square inches

h = the dielectric spacing, in mils

For example, a pair of conductors roughly in the shape of a quarter, about 1 inch in diameter and 100 mils apart, spaced by air, have a capacitance of about

$$C[\text{pF}] = \epsilon_0 Dk n \frac{A}{h} \approx 225 \times 1 \times 1 \times \frac{1[\text{in}]}{100[\text{mils}]} = 2 \text{ pF} \quad (5.14)$$

The capacitance scales with area. In a structure composed of large area parallel plates, as in a circuit board with FR4 type dielectric between the planes, we can estimate the capacitance per unit area as

$$\frac{C}{A}[\text{nF/in}^2] = \epsilon_0 Dk n \frac{1}{h} = 0.225 \times 4 \times 1 \times \frac{1}{h[\text{mils}]} \approx \frac{1}{h[\text{mils}]} \quad (5.15)$$

This is a simple relationship. The capacitance per unit area in a pair of planes in a typical circuit board in nF per square inch is about 1/dielectric\_thickness between the planes in mils.

For example, if the spacing is 3 mils, the thinnest without incurring additional expense for proprietary dielectric material, the capacitance per unit area is about  $1/3 \text{ mils} = 0.3 \text{ nF/in}^2$ . A board 10 inches on a side would have a total capacitance between the layers of about  $10 \text{ in} \times 10 \text{ in} \times 0.3 \text{ nF/in}^2 = 30 \text{ nF}$ . This is a relatively small amount of capacitance compared to the discrete capacitors applied to a board. Chapter 6 discusses how the role of the planes is not to provide high capacitance, but to provide low inductance between the packaged

components and the capacitors.

**Tip**

The capacitance per area, in nF per square inch between two planes in a circuit board, is roughly  $1/h$  with the dielectric thickness,  $h$ , in mils.

The capacitance of real capacitors is generally within 20% of the specified capacitance. Depending on the dielectric material, the capacitance may vary slightly with voltage and with temperature.

## 5.7 CAPACITOR TEMPERATURE AND VOLTAGE STABILITY

We achieve the high capacitance density in MLCC capacitors by using high Dk materials and thin spacing between the plates relative to printed circuit board parameters. This means there can be very high electric fields in the materials. Some of the high Dk materials are ferroelectric and show non-linear polarizability. Generally, higher fields reduce the DK value. The Dk is also temperature sensitive.

Capacitors fall into three classes based on the sensitivity of their capacitance to voltage and temperature. The dielectric material defines the class of the capacitors and its stability. These classes are as follow:

- **Class 1** capacitors are the most stable. They are generally composed of magnesium niobates and have Dk values ranging from 20 to 40. The Dk and resulting capacitance is stable over temperature and over voltage. One common material designation is NPo, referring to a temperature coefficient of capacitance that is less than 30 ppm/degK. Because the Dk is not very high, getting large value capacitance in class 1 capacitors is difficult. They are

most suited for filter applications where the SRF needs to be quite stable.

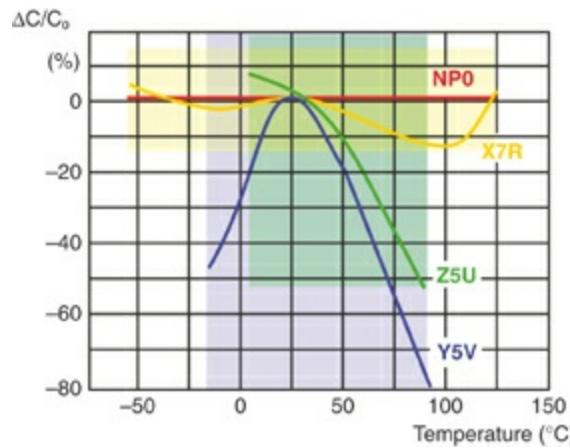
- **Class 2** capacitors are most often selected for decoupling applications. Made with dielectric materials they have a Dk typically from 200 to 14,000. The materials are usually barium titanate with various additives. This enables a large capacitance in a small volume, but because of their ferroelectric properties, they have a larger sensitivity to temperature and voltage.
- **Class 3** capacitors are made with materials that have a very high effective Dk value, but are not suitable for multilayer capacitors. Decoupling applications do not use this class of capacitor.

The EIA (Electronics Industries Alliance) has established a simple labeling format to describe the temperature range and capacitance stability over this range for class 2 dielectrics. Figure 5.13 lists the labeling specification.

Minimum temperature <sup>[1]</sup>		Maximum temperature <sup>[1]</sup>	Capacitance change permitted <sup>[1]</sup>
X	-55 °C	2	+45 °C
Y	-30 °C	4	+65 °C
Z	+10 °C	5	+85 °C
		6	+105 °C
		7	+125 °C
		8	+150 °C
		9	+200 °C
			A ±1.0%
			B ±1.5%
			C ±2.2%
			D ±3.3%
			E ±4.7%
			F ±7.5%
			L +15%/-40% <sup>[2]</sup>
			P ±10%
			R ±15%
			S ±22%
			T +22%/-33%
			U +22%/-56%
			V +22%/-82%

**Figure 5.13** EIA labeling format for class 2 capacitor materials based on the capacitance stability over temperature.

For example, X5R means a stable capacitance over the temperature range from  $-55^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  with a  $\pm 15\%$  change over this range. The X7R material extends the temperature range to  $+125^{\circ}\text{C}$ . Both X5R and X7R materials are commonly used MLCC capacitor materials. These designations also correlate slightly to the stability with voltage. [Figure 5.14](#) shows an example of the typical variation in capacitance over temperature for different material choices.



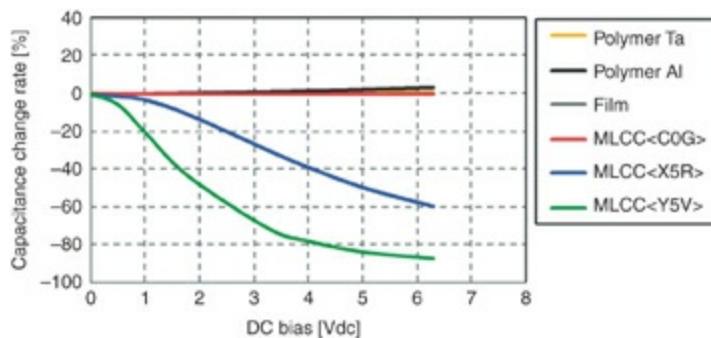
**Figure 5.14** Example of the temperature stability of various materials used in MLCCs.

**Tip**

The capacitor designation of X5R or X7R refers to the temperature range over which the capacitor is rated and the amount of capacitance change expected over this temperature range. The R refers to a  $\pm 15\%$  change expected over the rated temperature range.

In general, the higher the applied voltage, the larger the electric fields between the plates and the lower the Dk, which means the capacitance is decreased. Unfortunately, different capacitors from different vendors having the same material designation can still have a different voltage sensitivity. This means that for accurate capacitor models, reviewing the specific product specs and measuring the capacitor properties for a sample of capacitors are essential. [Figure 5.15](#) is an example of the measured voltage sensitivity for a few

different material choices.



**Figure 5.15** Example of voltage sensitivity of some material examples.

**Tip**

A far larger impact on capacitance will be from the voltage rating. Choose capacitor values, and measure them at the voltage of the application.

## 5.8 HOW MUCH CAPACITANCE IS ENOUGH?

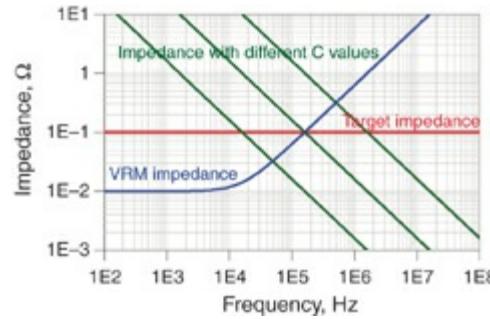
This is probably the most commonly asked question in PDN analysis, though not the most important. Only time domain analysis, including the VRM, can provide the correct answer. Large signal transitions for LDO (low drop out) regulators and SMPS (switch mode power supplies) are inherently non-linear and time variant so frequency domain analysis is not rigorously valid. We should follow the recommendations of the VRM supplier. We usually choose bulk capacitance to give good performance for a defined transient load step. However, we can roughly estimate the minimum amount of capacitance on the board for the PDN to first order by following some guiding principles with either a time domain or frequency domain analysis.

In the frequency domain, the primary role of the total capacitance on the board is to provide a low impedance at the frequency at which the voltage regulator module (VRM) is not able to do so. At this frequency, the total capacitance should be large enough so that its

impedance brings the PDN impedance below the target impedance. Because this is usually a large amount of capacitance and plays a dominant role at low frequency, it is often referred to as *bulk capacitance*.

If the bulk capacitance is too small, its impedance will be above the target impedance at the frequency where the VRM can no longer provide the low impedance.

Figure 5.16 illustrates this analysis.



**Figure 5.16** Example of the target impedance and VRM impedance showing the limit to the VRM and the impedance of three different capacitors.

The frequency limit to the VRM, when its output impedance exceeds the target impedance, depends on the target impedance and the nature of the feedback loop inside the VRM. It is usually in the 10 kHz to 1 MHz range. At this frequency, at a minimum, the impedance of the capacitor should be below the target impedance. We derive the bulk capacitance required to bring its impedance below the target impedance with

$$C_{\text{bulk}} [\text{F}] > \frac{1}{2\pi f_{\text{VRM-max}} [\text{Hz}] \times Z_{\text{target}}} \quad (5.16)$$

where

$C_{\text{bulk}}$  = the capacitance of the capacitor needed at the lowest frequency

$f_{\text{VRM-max}}$  = the frequency where the VRM impedance exceeds the target impedance

$Z_{\text{target}}$  = the PDN target impedance

For example, if the target impedance is 50 mΩ and the maximum usable frequency of the VRM is 10 kHz before its output impedance exceeds the target impedance, the minimum amount of bulk capacitance needed is roughly

$$C_{\text{bulk}} > \frac{1}{2\pi \times 10\text{kHz} \times 0.05} = 0.32 \text{ mF} = 320 \mu\text{F} \quad (5.17)$$

The bulk capacitance can be a very large value and is typically supplied by either electrolytic capacitors or tantalum capacitors. However, as the feedback loop frequency of the VRM increases, the frequency at which its output impedance exceeds the target impedance increases and a smaller bulk capacitance is needed. When the bulk capacitance required is in the 100 μF range, ceramic capacitors can supply it.

Of course, this is only a rough, initial estimate of the absolute minimum bulk capacitance required. The amount of capacitance for a robust design depends on the features of the VRM and the rest of the system and can only be accurately estimated by simulating the entire PDN ecology, but this estimate is a starting place.

We can also estimate the minimum amount of capacitance required with a time domain analysis. The bulk capacitor provides the charge storage to supply the current to the chip during the time required for the VRM to respond.

As charge flows from the bulk capacitor, the voltage across it drops. The bulk capacitance must be large enough to supply charge for a step current during the time in which the VRM cannot respond. The voltage drop on the bulk capacitor should be less than the typical 5% tolerance spec until the VRM can fully deliver the load current. The voltage drop on a capacitor is

$$\Delta V = \frac{\Delta Q}{C_{\text{bulk}}} < \text{ripple} \times V_{dd} = \frac{I_{\text{max}} \times \Delta t}{C_{\text{bulk}}} \quad (5.18)$$

From the initial description of the target impedance, the worst-case step transient current is roughly

$$I_{\text{max}} = \frac{V_{dd} \times \text{ripple}}{Z_{\text{target}}} \quad (5.19)$$

This results in an estimate of the minimum bulk capacitance needed of about

$$C_{\text{bulk}} > \frac{\Delta t}{Z_{\text{target}}} \quad (5.20)$$

If we make the connection that the highest frequency where the VRM is not effective at reducing the impedance below the target impedance is related to the time interval by

$$\Delta t = \frac{1}{2\pi f_{\text{VRM-max}}} \quad (5.21)$$

then we see that these two analyses result in exactly the same initial estimate for the minimum bulk capacitance required:

$$C_{\text{bulk}} > \frac{\Delta t}{Z_{\text{target}}} = \frac{1}{Z_{\text{target}} \times 2\pi f_{\text{VRM-max}}} \quad (5.22)$$

For example, if the target impedance is 50 mΩ and the time interval below which the VRM cannot respond is 10 μsec, corresponding to a frequency response of roughly 16 kHz, the bulk capacitance required is roughly

$$C_{\text{bulk}} > \frac{\Delta t}{Z_{\text{target}}} = \frac{10 \mu\text{sec}}{0.05 \Omega} = 200 \mu\text{F} \quad (5.23)$$

Of course, this is only a starting place estimate for the minimum capacitance required.

**Tip**

A rough estimate of the amount of capacitance required is based on the capacitance providing the voltage stability at a frequency beyond which the VRM can not respond. This is a starting place to estimate the total amount of bulk capacitance required.

To get a better estimate, we must consider the entire impedance profile of the VRM and bulk capacitor. A large peak impedance, from the parallel resonance of the effective output inductance of the VRM and the capacitance of the bulk capacitor, means a potential instability in the VRM. Although we can roughly consider this problem in the frequency domain, we must use time domain simulation for best accuracy. Switch Mode Power Supplies (SMPS) are inherently non-linear and time varying so they violate two of the most important requirements for frequency domain analysis. The impedance peak for a rising current waveform is quite different from a falling current waveform.

## **5.9 THE ESR OF REAL CAPACITORS: FIRST-AND SECOND-ORDER MODELS**

In addition to the capacitance, another intrinsic property of a capacitor is its equivalent series resistance (ESR). This is the equivalent resistance in a series RLC circuit that accounts for the losses in a real capacitor. ESR arises from a combination of the conductor loss due to the series resistance of the thin parallel sheets of conductor inside the capacitor and the dielectric loss from the ceramic material between the planes.

The simplest model for a capacitor uses a series RLC circuit with lumped circuit elements having constant parameter values. In a series RLC circuit, the real part of the impedance is simply the R value and is constant with frequency. As a first approximation, the ESR of a capacitor is constant with frequency.

Two effects contribute to a slight frequency dependence to the ESR of a real capacitor: the dielectric loss in the ceramic material and current redistribution through the plates of the capacitor with rising frequency.

We can model the dielectric loss in a capacitor with a parallel RC, with the R related to the conductance through the dielectric, G, by

$$R = \frac{1}{G} = \frac{1}{2 \times \pi \times f [\text{Hz}] \times C [\text{F}] \times Df} \quad (5.24)$$

where

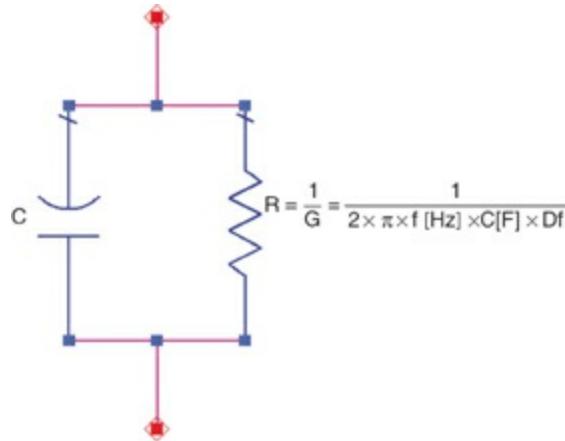
G = the conductance of the capacitor

f = the frequency of the signal through the capacitor

C = the capacitance of the capacitor

Df = the dissipation factor of the dielectric

Figure 5.17 shows an example of the circuit model for a capacitor that accounts for the dielectric loss.



**Figure 5.17** Equivalent circuit model for a real capacitor including the dielectric loss.

To first order, all the terms are constant with frequency. The frequency dependence of R comes directly from the explicit f term. As frequency increases, the parallel resistance decreases, as does the imaginary component of the impedance of the capacitor. The

impact of the dielectric loss is to increase the real part of the impedance toward lower frequency. This is the signature of a dielectric loss mechanism as the root cause of the ESR.

Only one parameter, the dissipation factor of the ceramic material Df, is needed to characterize the contribution of loss in the circuit model.

As frequency goes up, ESR goes up because current does not penetrate as far into the capacitor as it does at series resonant frequency. The current in the capacitor plates does not want to get very far from the return current in the substrate where the capacitor is mounted. This is increasingly so as the frequency goes up.

The loop inductance of the mounted capacitor is less if current stays low in the capacitor body near the mounting pads. The plates' resistance impedes current and forces it up into the capacitor body, whereas minimizing the loop inductance concentrates the current in the bottom plates. This situation is analogous to skin effect in a conductor. Not surprisingly, this phenomenon is modeled by an equation that has a square root dependence on frequency similar to skin effect. The advanced section in this chapter, section 5.15, describes this frequency-dependent inductance and ESR model of a real capacitor.

The high-frequency resistance behavior, related to a current redistribution to minimize loop inductance, is in the form of a square root of frequency dependence; we can approximate it as

$$R(f) = R_{dc} \left( 1 + \sqrt{f / F_0} \right) \quad (5.25)$$

where

$R(f)$  = the resistance as a function of frequency

$R_{dc}$  = the dc resistance of the metallization

$F_0$  = the frequency at which current depth effects begin to dominate

The impact from the current redistributing is to cause the real part of the impedance to increase with increasing frequency.

**Tip**

Two loss mechanisms contribute to the ESR of a capacitor: the dielectric loss of the ceramic and the series resistance of the conductors that make up the plates of the capacitor. We can incorporate both of these effects in a circuit model.

Figure 5.18 shows the behavior of the total impedance of a capacitor with each of these loss mechanisms selectively turned on. The real part of the impedance is dominated at low frequency by the dielectric loss and at high frequency by the decreasing depth of current penetration into the capacitor.

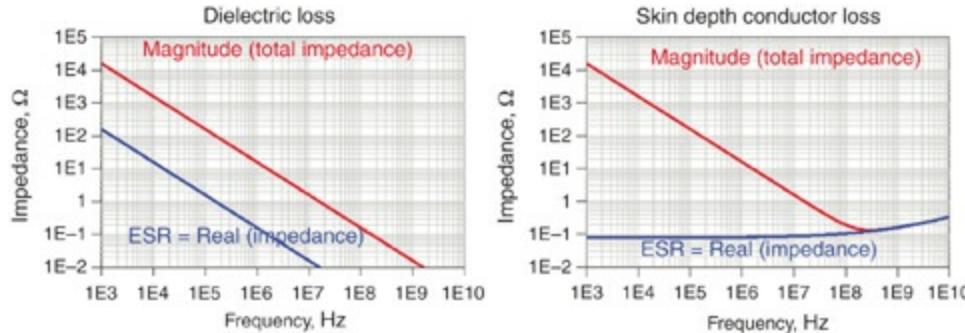
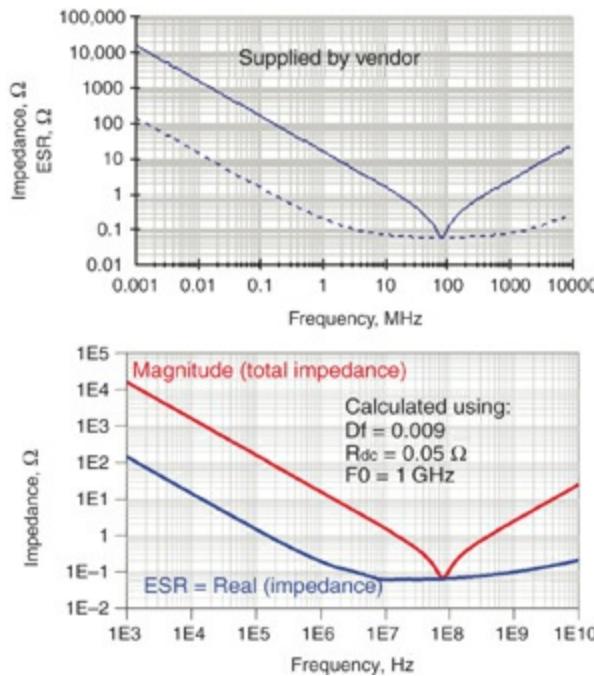


Figure 5.18 The signature of the frequency dependence of the ESR of a capacitor from two loss mechanisms.

Getting the values of the three parameters, which define the specific behavior of a real capacitor is often difficult. However, many vendors supply impedance curves for capacitors that include both mechanisms. By adjusting the three-parameter values to match the impedance curves, we can create a simple SPICE-compatible model for the real capacitor.

As an example, Figure 5.19 shows the published impedance curves for an AVX 0402 10 nF capacitor with

an ESL of 0.4 nH and simulated impedance profile using three-parameter values, which give a good match.



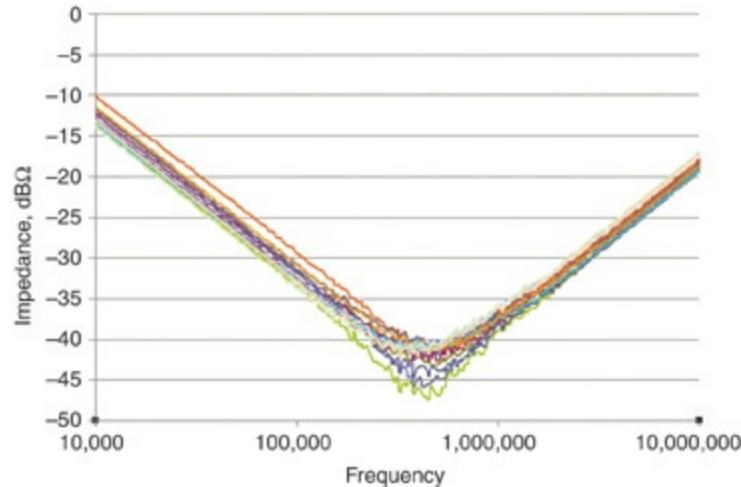
**Figure 5.19** Comparing AVX vendor-supplied and simulated impedance profile and ESR of a 10 nF capacitor.

In general, the lowest ESR will be in the 10 MHz to 100 MHz range, which is around where the SRF of these sorts of capacitors will generally lay, given ESL values about 1 nH. The higher ESR at higher frequency is useful to help damp out parallel resonances, but is a second-order factor.

Unfortunately, the specific parameters vary from capacitor to capacitor. The two practical approaches to deal with this variability are to measure each capacitor that might be used in an application and store the parameter values that best describe it in a database library, or approximate the ESR by a simple constant  $R$  value or a parameterized model.

Figure 5.20 shows an example of the distribution of measured impedance profiles for 15 different capacitors, all nominally the same 100  $\mu\text{F}$ , 1210 MLCC capacitor but from different vendors. The ESR, as read from the bottom of the impedance curves, varies from 0.01 to

$0.003 \Omega$ . This is a factor of three, which will have a direct impact on the accurate prediction of peak impedances.

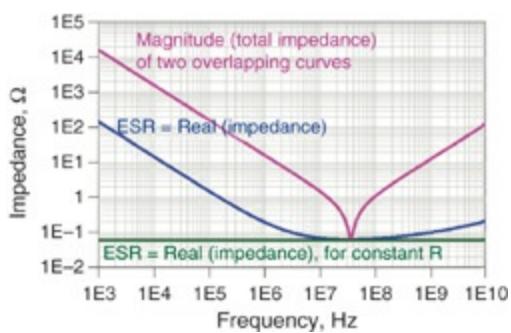


**Figure 5.20** Measured impedance profiles for 15 different nominally identical capacitors. The vertical scale is impedance, in dB. This means 0 dB is  $1 \Omega$ ,  $-20$  dB is  $0.1 \Omega$ , and  $-40$  dB is  $0.01 \Omega$ . Data is courtesy of Mike Jones, Linear Tech.

**Tip**

Be aware that the ESR of a capacitor, one of the most important terms that determine the peak impedance profile of the PDN, can vary between nominally identical capacitors by as much as three times from vendor to vendor. This means that if accurate prediction of the PDN profile is important, measuring the behavior of capacitors selected for a design is important as well.

Alternatively, if you are not going to measure the ESR of each capacitor from each vendor, you can approximate the frequency dependence of the ESR by a constant R chosen to match the lowest impedance at the SRF of the capacitor. The impedance profile is not significantly affected, and the ESR with a constant R matches the ESR with a frequency-dependent R very well in the 10 MHz to 100 MHz range. The inaccuracy of a constant R model, over a model based on specific measurements, is smaller than the variation from part to part. Figure 5.21 shows this comparison.

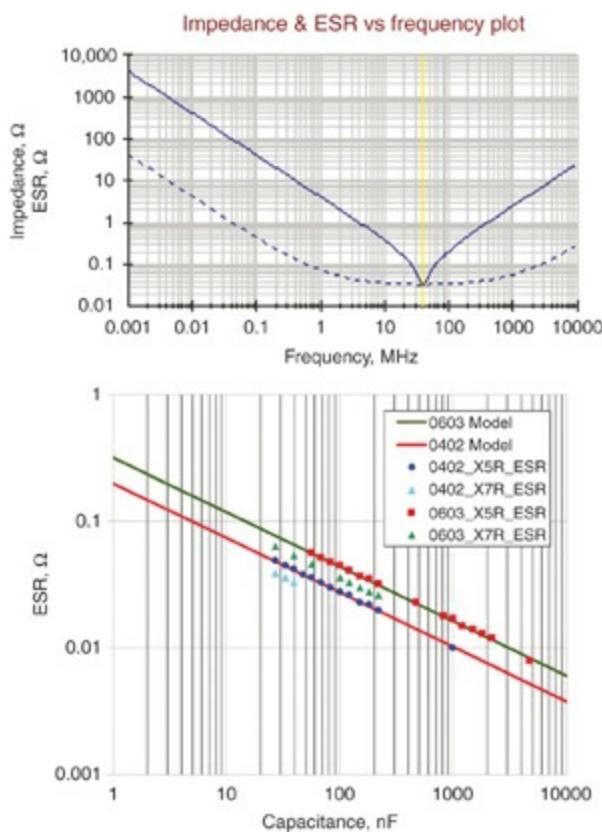


**Figure 5.21** Simulated impedance and the real part of the impedance for the case of frequency-dependent losses and a constant R value. No difference exists in the magnitudes of the impedance, and the constant R is a good approximation to the ESR in the 10 MHz to 100 MHz frequency range.

## 5.10 ESTIMATING THE ESR OF CAPACITORS FROM SPEC SHEETS

As a single parameter, the ESR of a capacitor depends on capacitor body size and the number of conductor plates in parallel. As the number of plates increases, the capacitance of the capacitor increases and the series resistance decreases. A connection exists between the capacitance and ESR for a capacitor.

We explore this relationship by data mining the information in the spec sheets of capacitors. As an example, the data for the C and ESR values for an 0603 and 0402 capacitor from AVX were extracted and plotted [1]. **Figure 5.22** shows the specified values and the comparison to a simple, empirical model for the relationship between ESR and C. The agreement is so good, it suggests that this is the relationship used by AVX in presenting the ESR for these capacitors.



**Figure 5.22 Top:** Typical specs for the impedance profile and ESR of a specific capacitor available from AVX. **Bottom:** A plot of the extracted ESR, as obtained from the preceding plot, and the value of the capacitance for 0402 and 0603 capacitors. The solid lines are the empirical models described in the text.

The empirical relationship, derived from the log-log plot of the ESR and capacitance for the case of 0603 X5R dielectric is given by

$$\text{ESR} = \frac{0.32 \Omega}{(C[\text{nF}])^{0.43}} \quad (5.26)$$

The empirical relationship between the ESR and capacitance for the case of 0402 X5R dielectric is given by

$$\text{ESR} = \frac{0.20 \Omega}{(C[\text{nF}])^{0.43}} \quad (5.27)$$

where

C = the capacitance of the capacitor in nF

ESR= the equivalent series resistance in Ω

We derived the models based on the specific capacitance and impedance values provided by AVX in its database tool, SpiCAP. Looking at the data extracted from this database, probably an analytical equation was used to create the data. All we have done with this model is reverse engineer the model used by AVX. This relationship likely will match other measured results, however, with different values for the two coefficients.

The format for the relationships in [equations 5.26](#) and [5.27](#) is the same. The only difference is the value of the resistance coefficient,  $0.32 \Omega$  in the case of the 0603 body size capacitor and  $0.20 \Omega$  for the 0402 body size capacitor. This is an incredibly useful relationship because we can now directly implement a first-order estimate for the value of the ESR of a capacitor in any SPICE circuit simulation, without having to look it up for each capacitor selected.

**Tip**

Using the reported ESR values from a vendor, we can develop and use a simple model for the ESR of different value capacitors in system simulations. This is incredibly valuable for calculating accurate impedance profiles of combinations of different value capacitors.

For example, we can explore the q-factor of a capacitor based on its ESR, C, and ESL. The q-factor is given by

$$\text{q-factor} = \frac{1}{\text{ESR}} \sqrt{\frac{\text{ESL}}{\text{C}}} \quad (5.28)$$

If the ESR were the same for all capacitors, we would expect the q-factor to decrease with the square root of the increase in the capacitance. The larger the capacitance, the lower the q-factor, and the more the damping of a self-resonance.

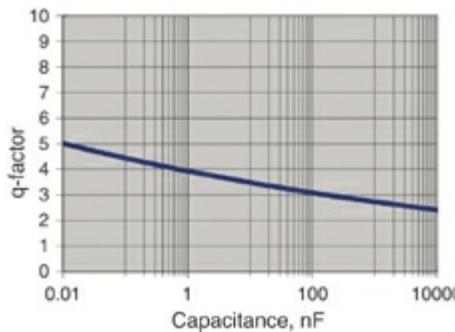
Using the value for the ESR of an 0603 capacitor, the q-factor is

$$\text{q-factor} = \frac{(C[\text{nF}])^{0.44}}{0.32} \sqrt{\frac{\text{ESL}}{C}} = \frac{(C[\text{nF}])^{-0.06}}{0.32} \sqrt{\text{ESL}[\text{nH}]} \quad (5.29)$$

The ESR will decrease just a little slower than the capacitance will increase. The q-factor will decrease only very slightly with higher capacitance. If the ESL is about 2 nH, the q-factor of an 0603 capacitor will be on the order of 4 for low values of capacitance and 2 for higher values of capacitance, as shown in [Figure 5.23](#).

**Tip**

In general, the q-factor of a capacitor will decrease very slightly for larger value capacitance. The impact is the self-resonance will have roughly the same q-factor for capacitors with different capacitance, but similar ESL.



**Figure 5.23** Estimated q-factor of an 0603 capacitor based on an ESL of 2 nH using this approximation for ESR.

## 5.11 CONTROLLED ESR CAPACITORS

The ESR of a capacitor is a critically important term influencing the peak impedance when different capacitors are combined together. Within some limits, the higher the ESR, the lower the peak impedance. In the examples shown in the previous sections, the typical values of ESR for ceramic capacitors are so low that higher values of ESR would result in lower peak impedances.

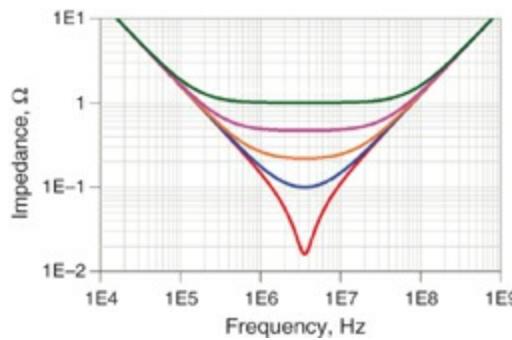
In recent years, many capacitor vendors have introduced a class of capacitors, typically described as “controlled ESR capacitors” that have custom-designed, larger series resistance. Implementation requires either shaping the metallization of the plates to make some regions narrower, or adding a small printed resistor element in series with the plates.

The magnitude of the resistance varies somewhat between vendors but ranges from about  $100\text{ m}\Omega$  to  $1.2\ \Omega$  and is independent of the capacitance. For example, Murata offers a controlled ESR capacitor series in an 0816, reversed aspect ratio body with a capacitance of  $1\ \mu\text{F}$  and ESR of  $0.1\ \Omega$ ,  $0.22\ \Omega$ ,  $0.47\ \Omega$ , and  $1\ \Omega$ .

**Figure 5.24** shows the impedance profile of this capacitor with four different values of ESR compared with the typical value of  $0.016\ \Omega$ . Note that the impedance profile of a single capacitor is used to highlight its higher ESR value.

**Tip**

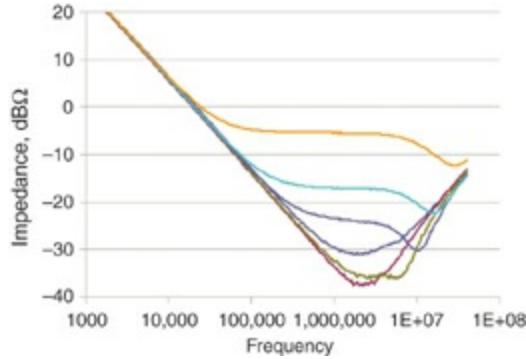
The key feature the higher ESR offers is not a higher minimum impedance at the self-resonance of a single capacitor, but a lower maximum parallel resonance peak impedance when multiple capacitors are combined.



**Figure 5.24** Simulated impedance profile of a standard ESR  $1\ \mu\text{F}$  capacitor and the same capacitor implemented with four different controlled ESR values of  $0.1$ ,  $0.22$ ,  $0.47$ , and  $1\ \Omega$ , all using the same  $2\text{ nH}$  of mounting ESL.

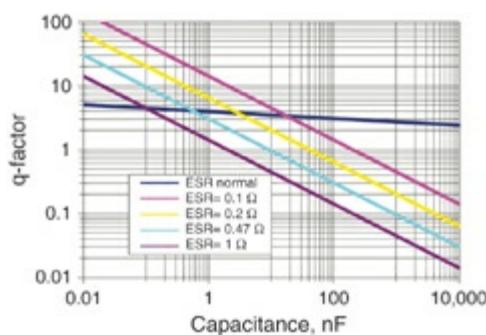
This is exactly the behavior measured in controlled

ESR capacitors. **Figure 5.25** shows the measured impedance profile of a selection of controlled ESR capacitors from TDK, which ranges from  $20\text{ m}\Omega$  to  $1\text{ }\Omega$ . Each capacitor is nominally  $10\text{ }\mu\text{F}$  but with a different ESR. The ESL for each capacitor in the specially designed test fixture was about  $0.6\text{ nH}$ .



**Figure 5.25** Measured impedance of various TDK controlled ESR capacitors, courtesy of Mike Jones, Linear Tech.

The q-factor of these capacitors is much lower than conventional capacitors in some conditions. In a controlled ESR capacitor, the ESR is fixed by design and not related to the value of the capacitance. As C increases, with both ESL and R constant, the q-factor decreases. Only high capacitance values, typically larger than  $1\text{ }\mu\text{F}$ , are available as controlled ESR capacitors. The amount of capacitance available in a controlled ESR capacitor is usually smaller than a standard capacitor in the same body size. **Figure 5.26** compares the q-factor of these capacitors with conventional capacitors at their self-resonance.



**Figure 5.26** Estimated q-factor of capacitors with different ESR values, comparing conventional 0603 and controlled ESR capacitors.

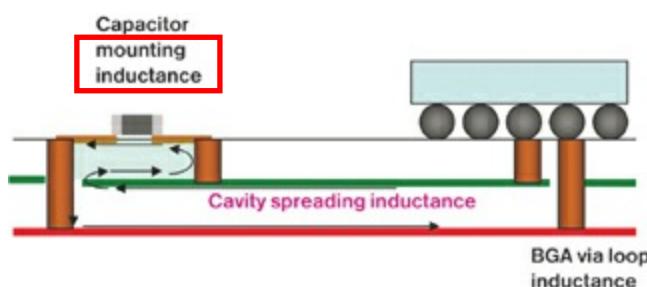
These low values of q-factor for high value C are useful when damping the parallel resonances with the VRM at low frequency and when used on an electronic package to damp the parallel resonance between on-die capacitance and package inductance.

#### Tip

Controlled ESR capacitors can be a powerful component to help damp out parallel resonances by increasing the damping of high q-factor resonances. Their benefit of lower q-factor is especially valuable for large capacitor values.

## 5.12 MOUNTING INDUCTANCE OF A CAPACITOR

The loop inductance associated with a real capacitor used in conjunction with a ball grid array (BGA) can be separated into the mounting inductance to the board, the spreading inductance in the power and ground plane cavity, and the via pair loop inductance up to the package. Figure 5.27 illustrates these three sections.



**Figure 5.27** Illustration of the three sections that compose the total ESL of a capacitor.

In this chapter, we analyze the design features that influence the mounting inductance of the capacitor to the board and to the cavity. In [Chapter 6](#), we analyze the spreading inductance of the cavity and parallel combination of multiple vias from the BGA to the cavity.

As usual, the loop inductance of a mounted capacitor is the only thing that matters. The loop of a mounted capacitor involves the partial inductance of the capacitor, sometimes called intrinsic inductance, together with the partial inductance of the mounting structure. An accurate evaluation of the loop inductance of the mounted capacitor involves the sum of two partial inductances (capacitor intrinsic and mounting structure) minus 2 times the mutual inductance between the two partial inductances.

A common practice in the industry is to obtain an RLC model for the capacitor from a capacitor supplier and combine it with the mounting structure for use in a system simulation. This approach is misleading because rarely are details provided of what geometry the ESL includes.

Even when details are provided, the supplied ESL model is usually a conservative approach because the mutual inductance associated with the capacitor partial-inductance and the mounting structure partial-inductance has been ignored. This is a small error when the product has surface traces from pads to vias and long vias associated with thick boards. However, neglecting the mutuals becomes a larger source of error as the capacitors become small (0201 size) and they are mounted on pads with embedded micro vias as is common in the mobile industry.

The intrinsic capacitor inductance supplied by a capacitor vendor depends greatly on the fixture where it is measured, and the mounting structure inductance in

a specific application depends on the specific via geometry, including the cavity design and location in the stackup.

As identified in [Figure 5.27](#), the mounting inductance of the capacitor is broken down into two sections:

- The loop inductance between the two vias to the cavity
- The loop inductance between the surface traces and the top of the cavity

We can estimate the [loop inductance of a pair of vias](#) with the simple approximation

$$L[\text{pH}] = 10 \times \ln\left(\frac{s[\text{mils}]}{r[\text{mils}]}\right) \times Len[\text{mils}] \quad (5.30)$$

where

$L$  = the loop inductance of the pair of round rods in pH

$s$  = the center-to-center spacing between the rods, in mils

$r$  = radius of the rod, in mils

$Len$  = the length of the rods, in mils

(note, this approximation is good when  $s \gg r$ )

For example, if the length of the vias from the capacitor on the top surface to the top of the power/ground plane cavity is 10 mils and the radius of the rods is 5 mils with a center-to-center spacing of 80 mils, the total loop inductance contribution from the vias is

$$L[\text{pH}] = 10 \times \ln\left(\frac{s[\text{mils}]}{r[\text{mils}]}\right) \times Len[\text{mils}] = 10 \times \ln\left(\frac{80}{5}\right) \times 10 = 280 \text{ pH} \quad (5.31)$$

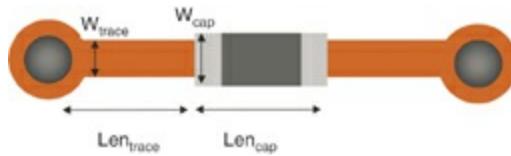
If it were possible to bring the vias closer, as for example, a pitch of 40 mils if they come off the edge of

the capacitor, rather than from end to end of surface traces, the loop inductance would be reduced slightly to

$$L[\text{pH}] = 10 \times \ln\left(\frac{s[\text{mils}]}{r[\text{mils}]}\right) \times \text{Len}[\text{mils}] = 10 \times \ln\left(\frac{40}{5}\right) \times 10 = 208 \text{ pH} \quad (5.32)$$

This suggests that to reduce the via loop inductance, a pattern bringing the vias with opposite current closer together is preferred. However, the via loop inductance is just part of the mounting inductance.

Figure 5.28 shows the geometry of the top surface traces connecting the capacitor pads to the vias connected to the cavity.



**Figure 5.28** Features of the top metallization and capacitor contributing to the mounting inductance of the capacitor.

We estimate the loop inductance of these surface traces and the top of the cavity using the approximation for the microstrip transmission line in FR4, introduced in Chapter 4:

$$L[\text{pH}] = 7.25 \times \ln\left(\frac{6 \times h[\text{mils}]}{0.8 \times w[\text{mils}]}\right) \times \text{Len}[\text{mils}] \quad (5.33)$$

where

L = the loop inductance of the surface trace and the top of the cavity, in pH  
h = distance from the trace to top of the cavity, in mils

w = width of the trace in mils  
Len = the length of the trace in mils

(Note: This is based on a simple approximation for the impedance of a microstrip transmission line.)

For example, for the special case:

$h = 10$  mils

$w = 10$  mils

$Len = 30$  mils

the loop inductance of this one leg of the top trace is

$$L[\text{pH}] = 7.25 \times \ln\left(\frac{6 \times 10}{0.8 \times 10}\right) \times 30 = 7.25 \times 2 \times 30 = 435 \text{ pH} \quad (5.34)$$

There would be 435 pH of loop inductance from each leg of the surface traces. If there were an equal length on each side of the capacitor, the total loop inductance contribution would be 870 pH.

We can use the same approximation to estimate the loop inductance of the capacitor's body contribution. However, a little uncertainty exists about the effective height of the capacitor from the top of the cavity. The capacitor is mounted to the top of the circuit board with a small solder fillet that keeps the bottom of the capacitor about 5 to 10 mils offset from the top of the board.

In addition, inside the capacitor, usually a dielectric layer is between the outside of the capacitor and the first metallization planes. To further complicate the analysis, the top dielectric layer thickness is usually not the same as the bottom dielectric layer thickness and the top and bottom are not typically labeled on the capacitor.

As a rough estimate, assuming a value of 15 mils as the distance from the surface of the board to the bottom of the plates in the capacitor is not unreasonable. Further, substantial current will be flowing through the center of the plates, so the actual distance from the top of the board to the region of the most current flow could be as large as 20 mils.

The contribution of loop inductance from the capacitor body, for the case of an 0603 capacitor, assuming the top of the cavity is 10 mils below the surface of the board is estimated as

$$h = 10 \text{ mils} + 20 \text{ mils} = 30 \text{ mils}$$

$$w = 30 \text{ mils}$$

$$Len = 60 \text{ mils}$$

$$L[\text{pH}] = 7.25 \times \ln\left(\frac{6 \times 30}{0.8 \times 30}\right) \times 60 = 7.25 \times 2 \times 60 = 870 \text{ pH} \quad (5.35)$$

This analysis identifies the relative amount of loop inductance for this typical case, as

- 208 pH = loop inductance of the vias
  - + 870 pH = loop inductance of the two legs of surface trace
  - + 870 pH = loop inductance of the capacitor body
- 1948 pH = total loop inductance associated with the mounting of the capacitor

This typical example has the top of the cavity about 10 mils below the top surface of the board and surface traces that are 30 mil long and 10 mil wide to connect an 0603 capacitor to the board. The mounted loop inductance for the capacitor is estimated at 2 nH.

**Tip**

Using common design parameters for an 0603 capacitor, without special care for engineering lowest possible mounting inductance, a typical capacitor mounting inductance is on the order of 2 nH.

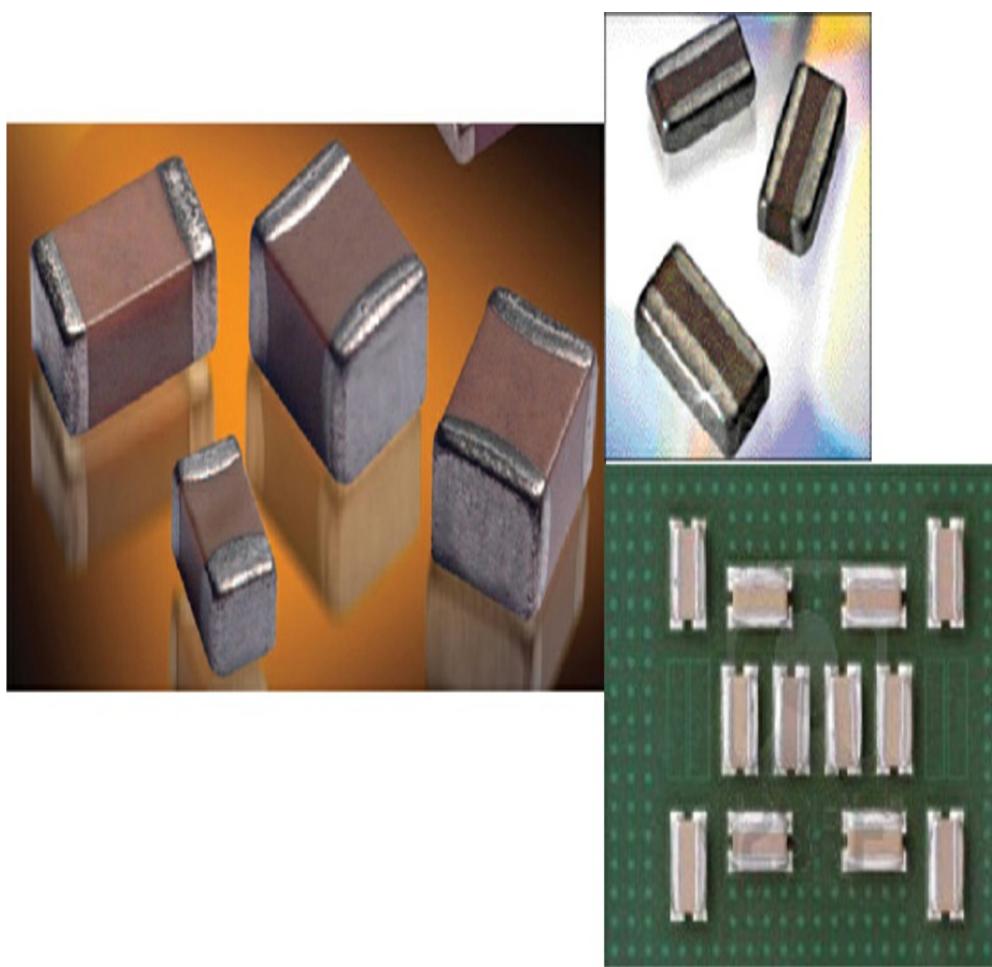
For comparison, if the capacitor were mounted under the BGA on the back side of the board, connected directly to power and ground vias in the BGA pad stack, the mounted loop inductance of the capacitor would be dominated by the via loop inductance through the board

up to the BGA. If the center-to-center ball pitch is 50 mils and the vias are 5 mil in radius, the loop inductance per length of the vias is

$$L[\text{pH/mil}] = 10 \times \ln\left(\frac{s[\text{mils}]}{r[\text{mils}]}\right) = 10 \times \ln\left(\frac{50}{5}\right) = 23 \text{ pH/mil} \quad (5.36)$$

For a board 64 mils thick, the via loop inductance is about  $64 \text{ mils} \times 23 \text{ pH/mil} = 1.5 \text{ nH}$ . We must compare this with the power plane cavity spreading inductance plus BGA via inductance to the capacitor mount on the top side of the board. Thicker boards have a higher via inductance to the backside mount compared to thinner boards. In some cases, an advantage exists to mounting capacitors directly under the BGA, but doing the analysis is always important.

An important capacitor design to consider is a reverse aspect ratio capacitor. This has the terminals along the wide side, as shown in [Figure 5.29](#). The mounting inductance for a reverse aspect ratio capacitor can have significantly lower loop inductance than a conventional capacitor, especially if all the features are optimized.



**Figure 5.29** Conventional aspect ratio capacitors and a selection of reverse aspect ratio capacitors with the terminals along their long side.

With the lower loop inductance of the reverse aspect ratio capacitor comes a reduced ESR. The number of squares between capacitor terminals influences both ESL and ESR. If the number of squares of a reverse aspect ratio capacitor is reduced from 2 to 0.5, the ESR may be reduced to 25% of a standard orientation capacitor. Although the mounted inductance can be reduced over a standard capacitor, the much lower ESR might result in a higher peak impedance due to less damping and a higher q-factor if the total loop inductance is not significantly reduced. This is why analysis is so important for each design to determine the relative tradeoffs.

A typical reverse aspect ratio capacitor in an 0306 body might have the following features:

$h_{\text{trace}} = 5 \text{ mils}$

$w_{\text{trace}} = 60 \text{ mils}$

$\text{Len}_{\text{trace}} = 10 \text{ mils} (\text{via in pad})$

$h_{\text{cap}} = 5 + 10 = 15 \text{ mils}$

$w_{\text{cap}} = 60 \text{ mils}$

$\text{Len}_{\text{cap}} = 30 \text{ mils}$

Via spacing = 40 mils

Via diameter = 10 mils

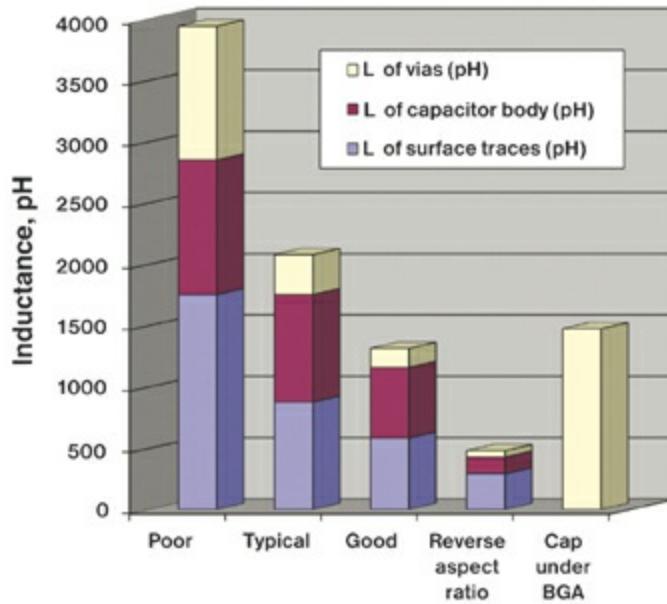
The loop inductance contribution from the traces is about 300 pH, from the capacitor body about 140 pH, and from the vias about 100 pH, for a total loop inductance of about 540 pH for the mounted capacitor. This separation into loop inductance contributions is only a rough approximation to identify the relative importance of specific sections of the mounting geometry. In general, the total mounted inductance of a capacitor is about the entire loop and we can only calculate it with a 3D field solver that takes into account the details of the entire geometry.

We implemented this simple analysis in a spreadsheet to quickly and easily compare tradeoffs between assembly design rules and the resulting mounted loop inductance. [Figure 5.30](#) shows five different examples and compares their contribution to loop inductance.

#### Tip

The mounted capacitor inductance depends on the specific features in the three regions: the loop inductance of the surface traces, the capacitor body, and the vias to the top of the cavity. Using simple approximations, we estimate these elements to explore design tradeoffs.

	Poor	Typical	Good	Reverse aspect ratio	Cap under BGA
Len- Surface traces (mils)	60	30	20	10	
Width surface traces (mils)	10	10	10	60	
Depth to cavity (mils)	30	10	5	5	64
Capacitor width (mils)	30	30	30	60	
Capacitor length (mils)	60	60	60	30	
Capacitor offset of plates (mils)	20	20	10	10	
Number of vias pairs	1	1	1	2	1
Via radius (mils)	5	5	5	5	5
Via center to center (mils)	190	130	110	40	50
L of surface traces (pH)	1753	876	584	292	
L of capacitor body (pH)	1099	876	575	137	
L of vias (pH)	1091	326	155	52	1474
Total (pH)	3943	2079	1314	481	1474



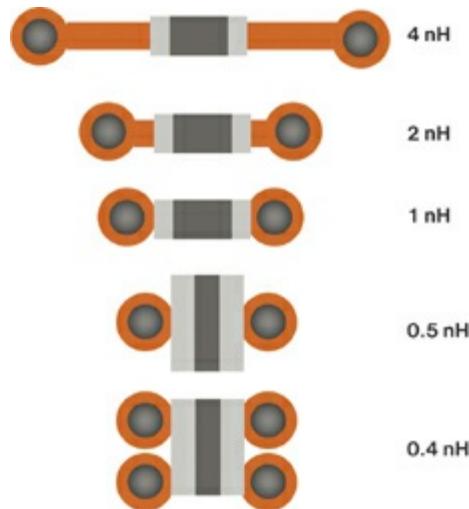
**Figure 5.30** Analysis of various capacitor-mounting options and the resulting loop inductance. For top side capacitors, we must add the loop inductance from the mount through the power plane cavity and the BGA vias to get a fair comparison with cap under BGA.

This analysis is typical of the loop inductance possible on large printed circuit boards. Smaller dimensions are possible on package substrates that have build-up layers and micro vias. The vias might only be a few mils long. Multiple vias might be placed directly under the capacitor terminals at minimum spacing. In such cases, mounting inductances as low as 100 pH are possible.

This analysis suggests that the five most important design knobs to reduce the mounting inductance of the capacitor to the surface of the board are as follow:

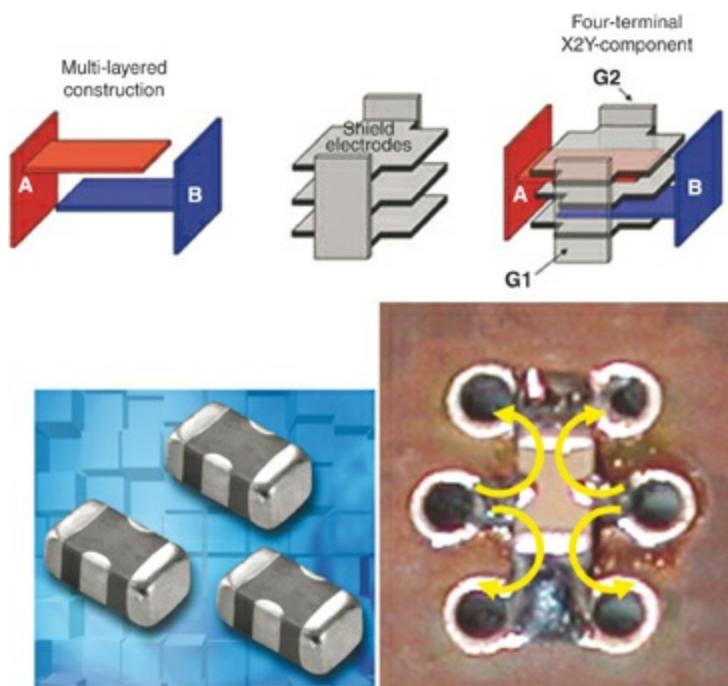
- Use short surface traces from the capacitor pads to the vias.
- Use wide surface traces from the capacitor pads to the vias.
- Arrange the top of the cavity as close to the top surface of the board as possible.
- Where possible, use reverse aspect ratio capacitors.
- Use multiple vias to hook up capacitor pads.

Figure 5.31 illustrates the general design guideline directions for lower capacitor mounting inductance [2].



**Figure 5.31** Illustration of design trends to reduce capacitor mounting inductance.

Another alternative capacitor style with low mounting inductance is the X2Y configuration, sometimes called a *three-terminal cap*. In this geometry, the terminals are configured off the ends and in the middle of the capacitor. Figure 5.32 shows the geometry and construction for an X2Y capacitor.



**Figure 5.32** Example of the X2Y capacitor that can offer very low mounting inductance. Terminals A and B are connected together to the power plane.

The X2Y capacitor is a type of interdigitated capacitor (IDC), constructed as if it were multiple capacitors in parallel, but with a via pattern that enables through-hole vias, which would not block routing channels.

As four capacitors in parallel, the net mounting inductance of the array of capacitors is the parallel combination of the loop inductance of each one. If the loop inductance of each capacitor were about 2 nH, the parallel combination of all of them would be about 0.5 nH.

Four important advantages of interdigitated capacitors are

- Multiple parallel capacitors in parallel
- Multiple via pairs in parallel
- An opportunity to leverage mutual inductance between the vias to reduce the via inductance
- A larger footprint of the vias to the cavity which reduces the spreading inductance

Most of the advantage from IDC capacitors comes

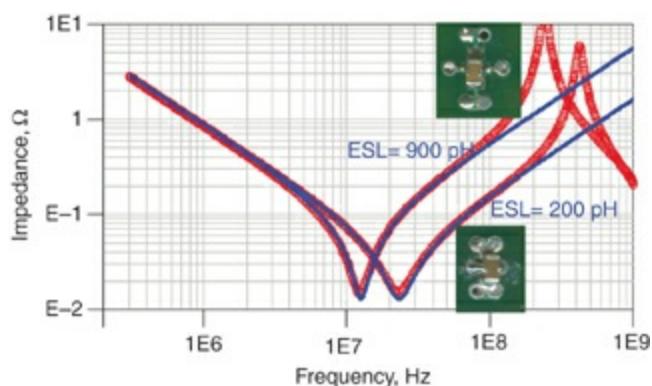
from the reduced inductance of the via configuration.

Estimation of the X2Y capacitor's mounting inductance is complicated because of multiple paths in parallel. The easiest way to estimate the performance advantage of the X2Y is to consider the mounting inductance of each quarter of the capacitor and scale this by the number of capacitors in parallel.

**Tip**

Interdigitated capacitors, such as the X2Y style, offer the advantage of multiple capacitors in parallel in the same body. This reduces the ESL of each capacitor by  $1/n$ , a significant improvement. Most of the improvement of the mounted capacitor inductance comes from the via pattern.

As with conventional capacitors, the length of the surface traces on the board strongly influences the resulting mounted loop inductance. [Figure 5.33](#) shows the measured impedance of two different X2Y capacitors mounted to a board, one with 20 mil long surface traces and the other with vias in the capacitor pads. The difference in measured loop inductance is startling. In the via in-pad configuration, the mounted loop inductance of the X2Y capacitor is as low as 200 pH. Adding just 20 mil long surface traces to the capacitor increases its mounting loop inductance to 900 pH. This is still a low value, but more than a four times increase just due to the short surface traces.



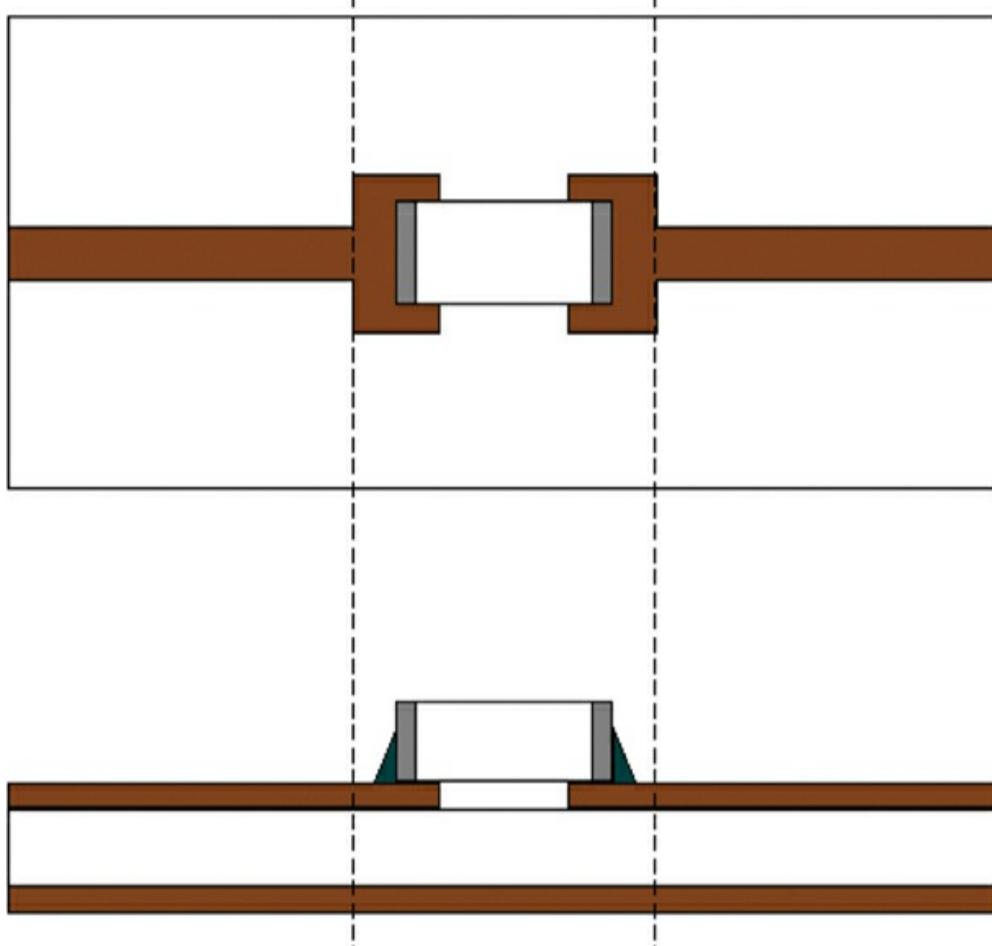
**Figure 5.33** Measured impedance of two different X<sub>2</sub>Y capacitors mounted to a board with 20 mil long surface traces and via in pad. The extracted loop inductance of these two configurations is 900 pH and 200 pH.

**Tip**

When mounting inductance is low, very small features can dramatically increase the mounting inductance. This is why attention to detail is an important element in designing the integration of a low inductance capacitor to a board.

## 5.13 USING VENDOR-SUPPLIED S-PARAMETER CAPACITOR MODELS

A common practice for capacitor vendors is to supply S-parameter models for their capacitors. Universally, these S-parameter files are derived from measurements of the capacitor in a specific “series” fixture that allows two-port measurement. [Figure 5.34](#) illustrates an example of a simple microstrip fixture for use with a VNA.



**Figure 5.34** Illustration of a typical microstrip fixture used to measure the two-port series S-parameters of a capacitor. The inductive qualities of the measurement depend on the fixture geometry and are not intrinsic to the capacitor.

The capacitor is in series between the two ports of the VNA, with some length of trace leading from the reference planes of the ports to the capacitor pads and a return path adjacent beneath the capacitor. Of course, the inductive properties of the measured S-parameter model in this configuration depend on the details of the fixture and location of the return path.

Unfortunately, many vendors and customers alike use these S-parameter models in system simulations under the mistaken belief that an S-parameter model must be accurate. After all, it goes up to 3 GHz.

To use the two-port model in a decoupling application, many users connect one port of the model to the capacitor mounting pads of their board and short

the other port to ground.

The problem with this approach is that the S-parameter model of the capacitor represents the properties of the capacitor in the specific measurement environment, with the leads to the capacitor and the position of the return path of the fixture. This might have no relationship at all to the mounting structure in the end user's system. The final application environment might have much more mounting inductance or much less mounting inductance than the configuration as measured. The results from a system-level simulation would be misleading.

**Tip**

Use caution when using a vendor-supplied S-parameter model of a capacitor in a system simulation. These models are only as good as the measurement fixture for predicting how a capacitor will behave in your system. They do not represent the same mounting inductance as you have in your application and might produce misleading results.

This is the main reason you should use S-parameter models supplied by vendors based on capacitor measurements cautiously in a system simulation. Three other reasons include

- The s-parameters are generally “corrected” in an unknown way.
- Some S-parameters are corrupted but still posted for distribution.
- Sometimes the capacitance of the component is different from its label.

Capacitor vendors that provide S-parameter models usually “correct” the measurements for passivity and reciprocity. They do not disclose the algorithm they use but it probably subtracts an offset to the magnitude of any S-parameter greater than 1 and replaces each pair of

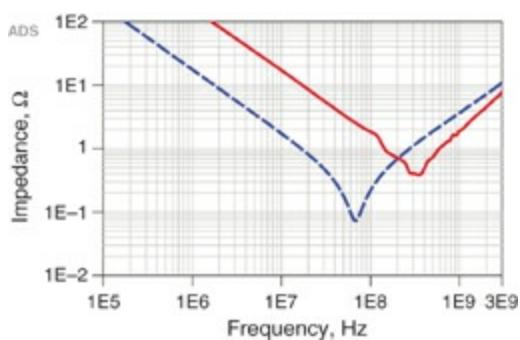
terms with their average. This is apparent in the published S-parameter values, such as in [Figure 5.35](#), which show identical S<sub>11</sub> and S<sub>22</sub> values. This can only happen if the S-parameters were simulated, or “corrected.”

S <sub>11</sub> <b>mag</b>	S <sub>11</sub> <b>phase</b>	S <sub>22</sub> <b>mag</b>	S <sub>22</sub> <b>phase</b>
0.96617446	-14.09844577	0.96617446	-14.09844577
0.96312476	-14.71015576	0.96312476	-14.71015576
0.95988758	-15.35460379	0.95988758	-15.35460379

**Figure 5.35** Small snippet of the values of S<sub>11</sub> and S<sub>22</sub> in a typical S-parameter file for three different frequencies. Note that the values of the S<sub>11</sub> and S<sub>22</sub> magnitude and phase are identical to eight decimal places.

If the corrections applied are a small percentage of the original S-parameters values, offering corrected S-parameters is not a problem. However, if we, the users, don't know how bad the S-parameters were before correction, we have no way of knowing how good or bad the data is and are not in a position to evaluate the quality of the measurements.

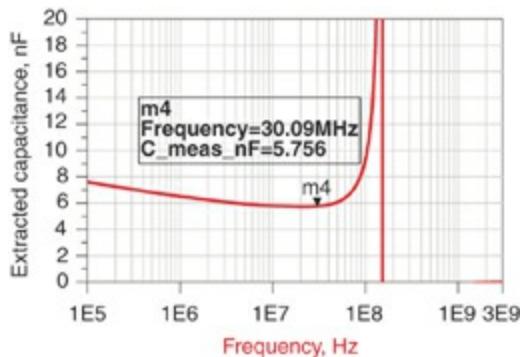
Some measurements are clearly corrupted, yet still posted and released by vendors. [Figure 5.36](#) shows the measured S-parameters converted, into impedance, showing gross distortions, compared to another set of measured S-parameters with well-behaved results.



**Figure 5.36** Example of the measured S-parameter models transformed into impedance for two different capacitors supplied by a vendor. The solid line clearly has a problem with the data. The dashed line is a similar, but higher value capacitor with a well-behaved impedance profile. The vendor should not have released the solid line data.

If the engineers who measured the S-parameters actually looked at the results and analyzed the quality of the measurements, they never would have posted these results. They would have immediately recognized something was wrong with these measurements and redone the measurements, or not posted the flawed results. This is one reason why you should never blindly trust measurements provided by vendors, but do your own analysis. Vendors should not just hire a summer intern to “crank out” results, but carefully analyze the results before they are released.

Sometimes, the measured S-parameters correspond to capacitors with values very different from the file label. For example, [Figure 5.37](#) shows the extracted capacitance from an S-parameter model posted for a 10 nF capacitor. The extracted value of 5.8 nF is much less than this. Vendors sometimes use an impedance bridge operating at 100 or 120 Hz (power line frequency) to measure capacitor values. This measured capacitance has little relevance for power integrity engineers who are trying to decouple PDNs at many MHz.



**Figure 5.37** Example of the extracted capacitance from an S-parameter model labeled as a 10 nF capacitor, but is in reality a 5.8 nF capacitor. Vendors often measure capacitors in an impedance bridge operating near 100 Hz. VNA measurements in the MHz range are more relevant.

**Tip**

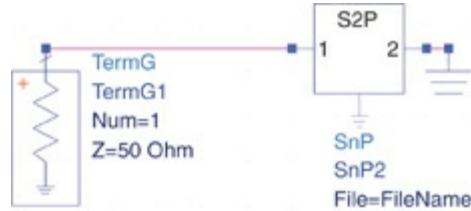
Most capacitor S-parameter models supplied by vendors are “mass produced” and their quality is *not* checked by an experienced engineer. The end user should always evaluate the quality of vendor-supplied models before using them.

## 5.14 HOW TO ANALYZE VENDOR-SUPPLIED S-PARAMETER MODELS

Having identified the problems of blindly using vendor-supplied S-parameter models, even those directly measured, we can get some potential value from these models if we use them “responsibly.” With a little analysis, we can interpret the measured S-parameters in terms of simple models and the intrinsic C and ESR extracted along with the specific ESL based on the specific fixture used.

The first step is to extract the impedance profile of the mounted capacitor from the measured S-parameters. We assume that the corrections to the measured and published models are small so they represent the S-parameters of the capacitor in its fixture. We extract the impedance profile by simulating the return loss from one end with the other end shorted. This turns the two-

port series measurement into a one-port measurement of the capacitor with its other end shorted to ground. This is the input impedance of the capacitor. [Figure 5.38](#) shows the circuit to implement this, using Keysight's ADS.



**Figure 5.38** Circuit used to simulate the one-port S-parameters of the two-port shunt model as the first step in building a simple RLC model of the capacitor using Keysight's ADS.

From the one-port return loss, we extract the complex impedance at each frequency from

$$Z(f) = 50\Omega \left( \frac{1+S_{11}(f)}{1-S_{11}(f)} \right) \quad (5.37)$$

where

$Z(f)$  = the complex impedance of the capacitor in its fixture at each frequency

$S_{11}(f)$  = the simulated complex return loss with port 2 shorted

From the complex impedance, we extract the C, ESR, and ESL for a simple series RLC model. At low frequency, we assume the impedance is due to a constant capacitance, and extract the capacitance from the imaginary part of the impedance using

$$C(f) = \frac{-1}{(\text{imag}(Z(f)) \times 2\pi \times f)} \quad (5.38)$$

where

$C(f)$  = the equivalent capacitance assuming the impedance is due to just an ideal capacitor

$f$  = the frequency at which the complex impedance is calculated

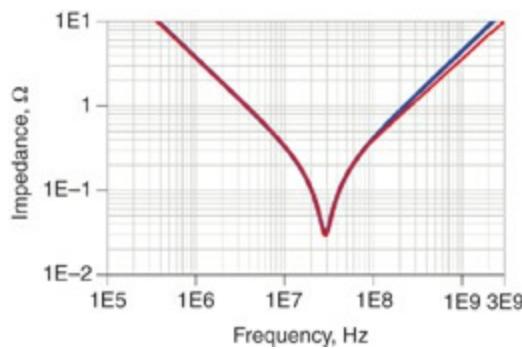
$\text{imag}(Z(f))$  = the imaginary part of the complex impedance

Likewise, we directly extract the equivalent series inductance from the imaginary component of the impedance using

$$\text{ESL}(f) = \frac{\text{imag}(Z(f))}{2\pi \times f} \quad (5.39)$$

Of course, keep in mind that this ESL is *not* intrinsic to the capacitor, but depends on the specific fixture used in the measurement with its leads from the VNA connectors to the capacitor pads and the existing return path.

Finally, we extract the ESR as the minimum in the magnitude of the measured impedance. Figure 5.39 shows the extracted impedance from the S-parameter model with the simulated impedance of a simple series RLC model, using the optimized values of ESR, ESL, and C. The agreement is very good.



**Figure 5.39** Extracted impedance profile of a 47 nF 0402 MLCC capacitor from the S-parameter model compared with a simulated impedance profile for a simple RLC circuit model using  $C = 42.6 \text{ nF}$ ,  $\text{ESL} = 0.71 \text{ nH}$ , and  $\text{ESR} = 0.0298 \Omega$ .

Using this process, we can analyze any two-port measured S-parameter model to extract the simple

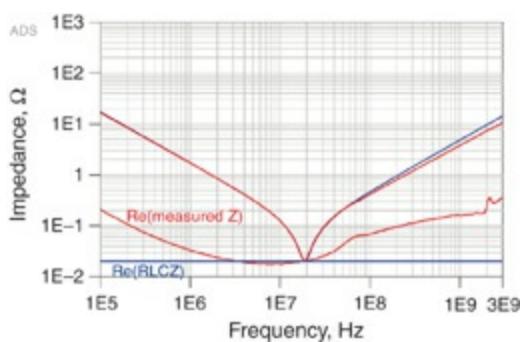
series RLC model. We can use the C value and ESR in a system-level simulation, along with an estimate of the specific mounting inductance the capacitor would see integrated into its application.

Although the series RLC circuit model is a simple model and matches the measured S-parameter models well, two important limitations exist as the mounting inductance is reduced.

The RLC model assumes the ESR is constant with frequency. This is not precisely the case. The ESR is frequency dependent. At low frequency, the loss comes from the dielectric and decreases with increasing frequency. At some point, the ESR of the real capacitor increases with frequency due to the current redistribution in the capacitor body because of skin-depth effects.

We can extract the effective series resistance of the capacitor interpreted as the real part of the impedance from the S-parameter model. This is the property that contributes to damping when this capacitor is used in a parallel circuit with another capacitor.

In [Figure 5.40](#), we compare the extracted magnitude and the real part of the impedance from the S-parameter model with the simulated impedance from the simple RLC circuit model and its constant real part. The real part of the impedance, extracted from the measured data, has the expected signature.



**Figure 5.40** The magnitude and just the real part of the impedances of the measured capacitor and simulated from the RLC model. The fitted real part of the impedance is flat at the minimum impedance and is only an approximation to the measured real part of the impedance.

When we model the capacitor with a simple RLC circuit and use the flat resistance at the impedance minimum in a circuit simulation, we underestimate the effective damping resistance of the capacitor at higher frequency. Above the SRF, the effective damping resistance is more than 2 times higher than at the SRF where the single-value ESR is fitted. The SRF is determined by the capacitance and the mounted inductance of the capacitor in the measurement fixture.

The typical frequency at which the real part of the impedance is a minimum is between 1 and 10 MHz for many capacitors. This is roughly the frequency where the skin-depth effect begins to redistribute the current in the capacitor body. This is also roughly the SRF for most capacitors in test fixtures.

This suggests that the ESR fitted from a simple RLC circuit corresponds to the minimum ESR a capacitor will ever have. It is still a figure of merit, but it is pessimistic. It does not give a realistic measure of the damping of the capacitor in a parallel resonant circuit.

In addition to underestimating the effective damping resistance of the capacitor at higher frequency, the same current redistribution mechanism in the capacitor body

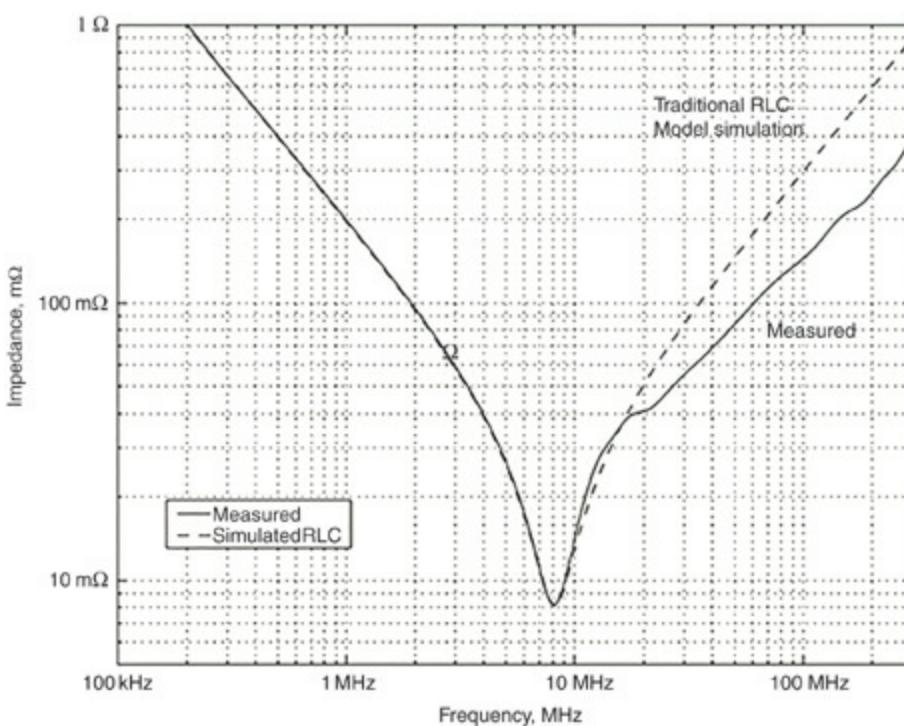
also deceases the inductance at higher frequency. This contributes to the slightly lower inductance shown in the extracted impedance profile in [Figure 5.40](#).

We need a higher bandwidth capacitor model to provide more accuracy at frequencies above SRF. This model should take into account the current redistribution and predict the higher damping resistance and lower inductance with frequency. We introduce this model in the next section.

## 5.15 ADVANCED TOPICS: A HIGHER BANDWIDTH CAPACITOR MODEL

In cases when the mounting inductance is significantly less than 1 nH, a real capacitor's impedance reveals new hidden features that bring out the frequency-dependent inductance and resistance properties. The inductance of the capacitor is dependent on the precise current distribution through the capacitor body.

This is especially the case when the top of the power and ground planes are very close to the top surface of the board, which is typical in very low inductance designs. [Figure 5.41](#) shows the measured impedance profile of a 1  $\mu$ F capacitor mounted on a low inductance fixture compared to a simple RLC model. The capacitive and series resonant portions of the curves match well.



**Figure 5.41** Measured impedance of a  $1 \mu\text{F}$  capacitor

mounted on a low inductance fixture shows the impedance does not match a simple RLC model. The capacitive slope and the impedance at series resonant frequency match well but the measured impedance at high frequency departs from that of the RLC model.

However, the measured impedance does not match the RLC model in the higher frequency, inductive portion of the curve. This is a strong indication that the capacitor's inductance is a function of frequency. A very low inductance fixture is required to make this observation. The impedance at 300 MHz of the RLC model is  $0.9 \Omega$  and the measured impedance is  $0.4 \Omega$ . This suggests that the intrinsic capacitor inductance at high frequency is less than half of what it is at the SRF.

Physically, the current wants to stay low in the capacitor at high frequency, close to the return current, which is in the mounting structure. This is similar to the skin effect where magnetic field penetration into a conductor is reduced at high frequency. The series resistance of the plates tries to force current deeper into the capacitor to include more plates in parallel and achieve a lower resistance. An equilibrium is reached

and is quantified in the skin-depth relationship discussed in section 4.9. A similar mechanism occurs in capacitors with the resistive plates forcing the current deeper and magnetic fields trying to keep the current shallow.

At series resonant frequency, all the capacitor plates are engaged in carrying current from one terminal to the other. As frequency increases, the capacitive impedance of the plates goes down. Fewer plate pairs are required to carry the capacitor current and there is no incentive from a capacitive viewpoint for current to go further up into the capacitor body, away from the return current in the mount. From an inductance and magnetic field perspective, there is strong motivation for current to stay low in the capacitor body, close to the return current.

When current is concentrated in fewer plates, the ESR goes up. Fewer capacitor plates in parallel are carrying current. This is a fortunate situation. At high frequency where parallel resonance makes a PDN impedance peak, the inductance of a capacitor reduces and the ESR increases. This is exactly what we want to reduce the q-factor of the parallel resonance. It would appear that in this case, Murphy got it wrong. The traditional RLC capacitor model is pessimistic. Broadband capacitor models are required to account for the newfound benefits at high frequency.

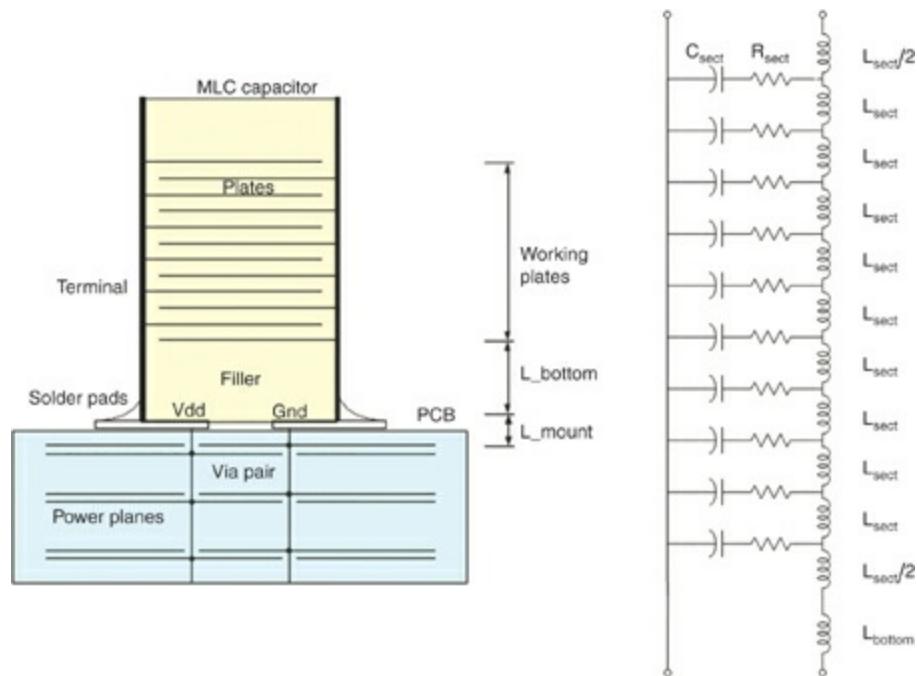
#### Tip

When the mounting inductance of a capacitor is very low, well below 1 nH, the distributed nature of a capacitor becomes apparent. Low mounting inductance reveals the decrease in capacitor inductance and the increase in ESR with higher frequency. This is a fortunate situation for q-factor reduction of parallel resonant peaks.

These two effects, the decrease in loop inductance and

the increase in resistance, are exhibited in a capacitor model that enables the change in current distribution through the capacitor body as frequency increases [3] [4] [5] [6].

Figure 5.42 shows the cross section of a capacitor mounted to a board and the equivalent circuit model. This topology is referred to as a *lossy transmission line model* for a capacitor. From a practical perspective, accounting for every plate pair is not necessary. No more than 10 parallel elements are needed to get a good match to typical capacitors on low inductance mounts.



**Figure 5.42** The physical structure of a capacitor and its equivalent lossy transmission line model.

This model includes a dissipation factor to account for dielectric loss between the plates. We can either fit this value from measured data or estimate it for the specific dielectric used. In the case of X5R capacitors, it is about 0.01. This accounts for the low-frequency behavior of the real part of the impedance.

As frequency increases, the  $L_{sect}$  elements block more and more plates from contributing to the current path and the effective loop inductance is lower. The working

capacitance is lower but that is not a problem because capacitive impedance is lower as the frequency increases. The effective equivalent series resistance, with fewer plates in parallel, is higher.

At higher frequencies, less of the current travels through the top plates of the capacitor, preferring to take the path of lowest loop inductance. This introduces a frequency-dependent loop inductance, capacitance, and resistance.

**Tip**

At higher frequencies, less of the current travels through the upper part of the capacitor, preferring to take the path of lowest loop inductance. This introduces a frequency-dependent loop inductance, capacitance, and resistance. This is apparent only when the mounting inductance, which hides these transmission line effects internal to the capacitor, is significantly less than 1 nH.

At low frequency, the impedance profile of the distributed model looks like the impedance profile of a simple RLC circuit. A connection exists between the C, ESR, and ESL of the simple series RLC model and the parameters of the distributed model. The parameters of the distributed model are extracted from the measured impedance profile.

We can easily extract the total capacitance  $C_{\text{cap}}$  from the specific impedance at a low frequency. At the SRF, the minimum impedance is the ESR. The capacitance and resistance of each section of the distributed model are related to the total  $C_{\text{cap}}$  and ESR values by

$$C_{\text{sect}} = \frac{C_{\text{cap}}}{n} \quad (5.40)$$

$$R_{\text{sect}} = \text{ESR} \times n \quad (5.41)$$

where

$n$  = the number of sections

$C_{sect}$  = the capacitance of each section

$R_{sect}$  = the resistance for each section

Getting the inductance elements of the distributed model is a little more tricky. The usual ESL of the mounted capacitor is calculated from the SRF and is related to three elements:

- The mounting inductance from the top of the board power/ground plane cavity to the cap pads,  $L_{mount}$
- The loop inductance from the top of the board pads to the bottom of the plates related to the thickness of the dielectric fill in the capacitor,  $L_{bottom}$
- The distributed loop inductance of the paths up to the parallel plates and back down again,  $L_{plates}$

$$ESL = L_{mount} + L_{bottom} + L_{plates} = L_{mount} + L_{cap} \quad (5.42)$$

where

$ESL$  = the usual value for the mounted capacitor calculated from the capacitance and SRF

$L_{mount}$  = the mounting inductance from the power plane cavity to the capacitor pads

$L_{bottom}$  = the inductance of the bottom of the capacitor related to the dielectric fill

$L_{plates}$  = the loop inductance associated with the height of the plates

$L_{cap}$  = the sum of  $L_{bottom}$  and  $L_{plates}$

The intrinsic inductance of the capacitor  $L_{cap}$  is the effective loop inductance up from the pads of the capacitor, through the plates and back down to the bottom, including the parallel connection of the plates. It includes the loop inductance of both the bottom and the plates, which is frequency dependent.

$$L_{\text{cap}} = L_{\text{bottom}} + L_{\text{plates}}$$

(5.43)

From these definitions, the distributed inductance of the plates is

$$L_{\text{plates}} = L_{\text{cap}} - L_{\text{bottom}} \quad (5.44)$$

When the mounting inductance of the capacitor is large, such as when the top of the power plane cavity is buried deep in the board stack-up, far from the capacitor plates, or there are long surface traces to the capacitor pads, the transmission line behavior of the capacitor is a tiny contribution to the total inductance and not noticeable. To observe the reduced inductance with frequency, the mounting inductance must be very small, well below 1 nH.

For a low inductance mount, the capacitor's transmission line properties dominate the inductance of a tall capacitor. The ESL is dominated by the intrinsic, distributed inductance of the capacitor composed of the loop going up to the capacitor plates, across, and back to the bottom of the capacitor. To separate the contributions of each inductance element of the capacitor, we need a way of estimating the mounting inductance and inductance of the bottom of the capacitor. These could come from a specialized measurement or from a calculation using an approximation or 3D field solver. Alternatively, if they are very small, we can extract the inductance of just the plates.

If we assume each of the three loop inductance elements acts as simple, discrete lumped loop inductor, then the measured series resonant frequency of the mounted capacitor is related to the total effective ESL and each inductance component by

$$SRF = \frac{1}{2\pi\sqrt{(ESL)C_{cap}}} = \frac{1}{2\pi\sqrt{(L_{mount} + L_{bottom} + L_{plates})C_{cap}}} \quad (5.45)$$

And after a little algebra,

$$L_{plates} = \frac{1}{(2\pi SRF)^2 C_{cap}} - L_{mount} - L_{bottom} \quad (5.46)$$

Now comes the tricky part. When we eliminate the capacitor's mounting and bottom inductances, the capacitor looks like an open transmission line on its end. It has inductance and capacitance per unit length just like a transmission line. There will be a time-of-flight down this transmission line. In this configuration, the impedance looking into the capacitor from the bottom end shows a voltage minimum when the length of the transmission line is one-quarter wavelength. This occurs at the series resonant frequency. Interestingly, the open-circuit end of the transmission line, the top of the capacitor, shows a maximum voltage at series resonant frequency.

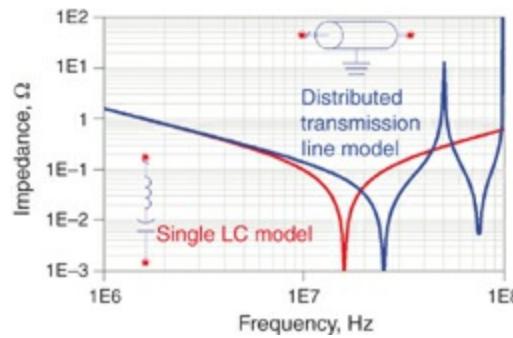
Traditionally with an RLC model, we have simply chosen an inductance to go with the capacitance to produce a minimum impedance at series resonant frequency. Although this impedance profile looks like a series resonance of a single L and C, the single L is only a substitute for the quarter-wave resonance of a transmission line section. The single L to achieve SRF and the inductance down the length of the transmission line are very different.

#### Tip

Although a quarter-wave-stub resonance of an open-ended transmission line looks like the self-resonant frequency of the total L and C in the transmission line, the frequencies are not the same. The LC circuit is just a substitute for the transmission line element and predicts an impedance minimum at a lower frequency than the transmission line model.

Figure 5.43 shows a comparison between a series LC circuit and a transmission line with similar total L and C. Obviously, they are not the same at all. The transmission line elements are related to the characteristic impedance and the time delay and also the total L and C of the line. Normally L and C are per-unit-length values but the same equations work for total L and C values, in which case we do not need to know the length of the line.

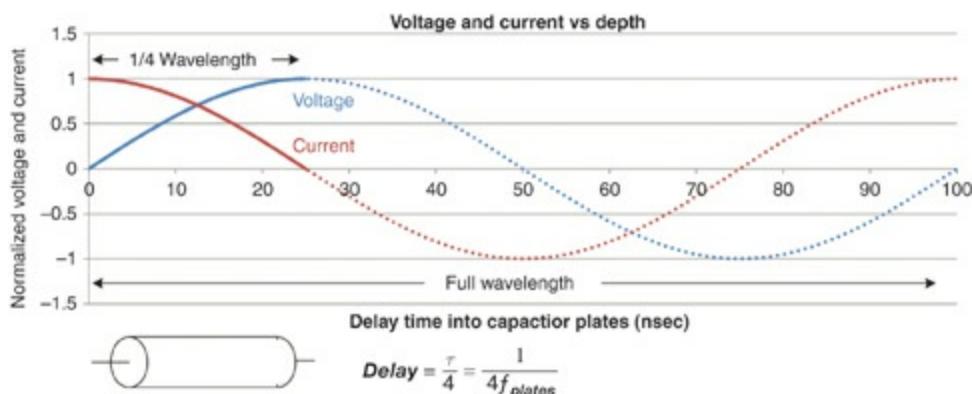
$$Z_0 = \sqrt{\frac{L}{C}} \quad \text{and} \quad TD = \sqrt{LC} \quad (5.47)$$



**Figure 5.43** Comparison of the impedance profile of a single LC circuit and a distributed transmission line model with exactly the same total L and C, but showing different resonant frequencies.

In a transmission line, the quarter-wave-stub resonance occurs at a higher frequency than the single LC circuit model approximation. After all, a transmission line is not a single LC, it is an entirely different, distributed element. It can be approximated by an LC circuit. At the SRF, the approximation is not very good. However, there is a connection between the quarter-wave-stub resonant frequency and the total L of a distributed transmission line.

At the quarter-wave-stub resonant frequency, the length of the open-ended transmission line is one-quarter wavelength, as shown in Figure 5.44.



**Figure 5.44** Voltage and current along the quarter-wavelength transmission line resonator.

If we measure the C of a transmission line from the low-frequency impedance and measure the quarter-wave-stub resonant frequency, we can extract the total L of the transmission line.

The total L of a transmission line,  $L_{tline}$  is

$$L_{tline} = \frac{TD^2}{C} \quad (5.48)$$

The TD at the quarter-wave resonant frequency is

$$TD = \frac{1}{4} \frac{1}{f_{1/4\lambda}} \quad (5.49)$$

Based on the total capacitance in the transmission line and the quarter-wave resonant frequency, the total inductance in the transmission line is

$$L_{tline} = \frac{\left( \frac{1}{4} \frac{1}{f_{1/4\lambda}} \right)^2}{C} \quad (5.50)$$

If we measure the frequency of the low-impedance dip, we can describe it in terms of the ESL of a lumped LC circuit or the quarter-wave-stub resonance of a transmission line circuit. We get the SRF with

$$SRF = \frac{1}{2\pi\sqrt{(ESL)C}} \quad (5.51)$$

Calling this the quarter-wave-stub resonant frequency, the total inductance of the transmission line length and the ESL of a simple LC circuit are related by

$$L_{tline} = \frac{\left(\frac{2\pi\sqrt{(ESL)C}}{4}\right)^2}{C} = \left(\frac{\pi}{2}\right)^2 ESL \sim 2.47 \times ESL \quad (5.52)$$

If the quarter-wave-stub resonant frequency of a transmission line were measured, but it was assumed to be the SRF of a LC circuit, the total inductance down the length of the transmission line is about 2.47 times the ESL extracted from SRF.

This means that using the frequency for minimum impedance and the capacitance from the low-frequency impedance, the total L of a distributed transmission line is calculated as 2.47 times the ESL from the SRF.

In the extraction of the plate inductance, this is the single LC section approximation. The total inductance down the length of the plates is really 2.47 times this extracted lumped value. If the  $L_{mount}$  and  $L_{bottom}$  are significant, a better estimate of the total inductance of the plates is

$$L_{tline} = \left(\frac{\pi}{2}\right)^2 \times (ESL - L_{mount} - L_{bottom}) \quad (5.53)$$

The calculated parameters for the lossy transmission line model for a capacitor are summarized as

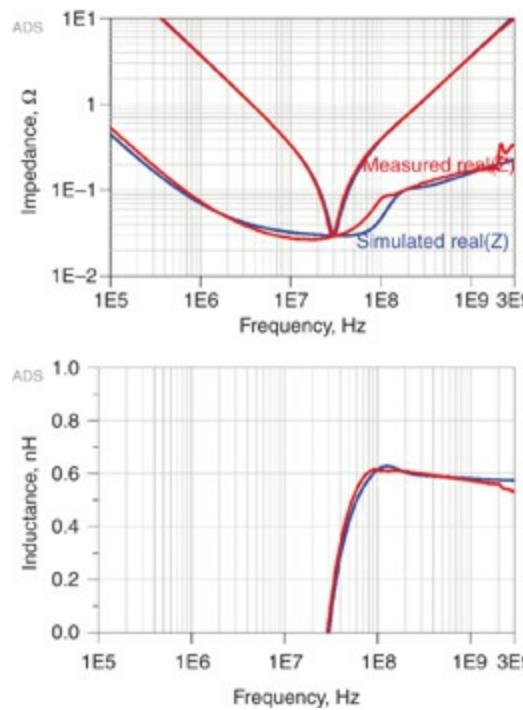
$$L_{sect} = \frac{L_{tline}}{n} \quad C_{sect} = \frac{C_{cap}}{n} \quad R_{sect} = ESR \times n \quad (5.54)$$

Converting a simple RLC model to a lossy transmission line model is easy; the only parameter needed is  $L_{bottom}$ .  $C_{cap}$  and ESR are the same as the simple RLC model. The ESL calculated from SRF is used in Equation 5.53 along with  $L_{bottom}$  to find the  $L_{tline}$  and

$L_{\text{sect}}$  inductance. Of course, this assumes that  $L_{\text{mount}}$  has already been removed from the RLC parameter model.

When we are successful in dramatically reducing the mounting inductance of a capacitor, and the top of the cavity is within a few mils of the top of the board, this ladder or lossy transmission line-equivalent circuit model more accurately predicts the capacitor's impedance profile. Most importantly, it more accurately estimates the effective frequency dependence of  $R$ , which affects the damping with parallel resonances.

Another way of arriving at values for the transmission line model is taking the measured S-parameter model and fitting parameter values to get a match between the simulated and measured values. For example, [Figure 5.45](#) shows the measured and simulated impedance and extracted inductance for a 47 nF capacitor using the S-parameter model.



**Figure 5.45** Comparing the extracted impedance and inductance from an S-parameter model and the simulated impedance and inductance of the lossy transmission line model.

In this simulation, we need to adjust only five

parameters:

- The dissipation factor of the capacitor = 0.011
- The mounting inductance = 0.570 nH
- The inductance of each section = 0.03 nH
- The resistance of each section = 0.0028 Ω
- The total capacitance = 42.6 nF

In this specific example, most of the inductance is mounting inductance. The successive change in loop inductance of each section of the plates is only 30 pH. This indicates the real intrinsic loop inductance of the capacitor and how low the effective series inductance could be if the best mounting were used.

The frequency-dependent inductance is well-matched, as is the frequency-dependent real part of the impedance. We could use this model to parameterize any of the S-parameter models supplied by vendors. We could then use it in a system-level simulation with the only change being the actual mounting inductance of the capacitor, based on the geometry of how the capacitor is connected to the cavity. This would be a realistic impedance of the frequency dependent impedance of the actual capacitor.

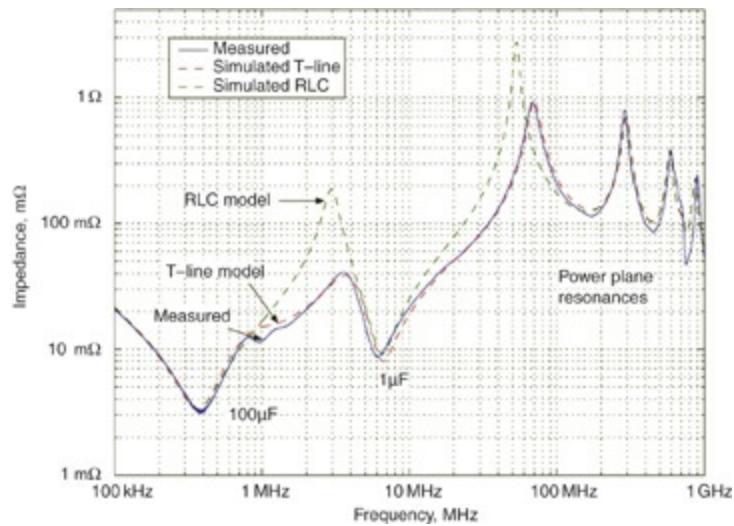
**Tip**

The most effective way of using a vendor-supplied S-parameter model is to extract the equivalent circuit element parameters in the lossy transmission line model and use these terms along with the specific mounting inductance based on how the capacitor is integrated into the cavity of the application. This model would be an accurate, high-bandwidth model of the capacitor.

One particularly useful method of converting vendor S-parameter models to lossy transmission line models is to establish a parameterized schematic similar to the one in [Figure 5.42](#) in a circuit simulator (that is, SPICE,

QUCS, or ADS). Optimize the C, ESR, ESL, and L<sub>bottom</sub> parameters of Equations 5.53 and 5.54 for best fit. You can create a library of suitable models by calling these four parameters for each physical capacitor.

Figure 5.46 compares simulation of the RLC model and the lossy transmission line model on the same graph as measured data. The system involves a 100  $\mu\text{F}$  and a 1  $\mu\text{F}$  capacitor mounted with low-inductance structures on a printed circuit board that has substantial power plane capacitance. The RLC capacitor model predicts high impedance peaks in two places of the curve.



**Figure 5.46** Simulation of RLC and lossy transmission line capacitor models compared to measurement. The lossy transmission line model does a much better job of predicting the parallel resonant peaks.

One impedance peak ( $\sim 3$  MHz) occurs when the 100  $\mu\text{F}$  capacitor has a parallel resonance with the 1  $\mu\text{F}$  capacitor. The other impedance peak ( $\sim 60$  MHz) occurs where the parallel combination of 100  $\mu\text{F}$  and 1  $\mu\text{F}$  caps resonate with the board power planes. The measured impedance peaks are greatly reduced compared to those predicted by the RLC model and are only 20% of the predicted height. The measured peaks are at higher frequency and not as sharp (lower q-factor).

The lossy transmission line model predicts impedance peaks that are very close to the measured peaks. The key to this was mounting the capacitors on very low inductance mounts. When the mounting inductance becomes less significant than the capacitor inductance, the lossy transmission line correctly predicts the frequency-dependent inductance and ESR of the ceramic capacitors. Neither model affects the power plane cavity resonances above 100 MHz.

An interesting application for this model is for capacitors embedded in a package or board substrate. The lossy transmission line model has two ports, one on the top of the capacitor and the other on the bottom. They are not at the same voltage. The top port of the model may connect to package metal next to the die bumps and the bottom port may connect to package metal near the board balls. The two-port model does not short the top of package to the bottom of package but connects them through an impedance. We should intuitively expect power flowing from the bottom port to the top port to be attenuated at high frequency as indeed it is by the lossy transmission line model.

**Tip**

The distributed, transmission line model of a capacitor is useful when the mounting inductance is engineered to be very small. We can use it to accurately describe the behavior of the capacitor when it is embedded in the package and connects the die bumps to the board balls. This model attenuates high-frequency power transmission.

Earlier in this section we mentioned that the lossy transmission line model for the capacitor predicts that at series resonant frequency, we see a minimum voltage at the capacitor pad mounts and a maximum voltage at the top (open-circuit end) of the capacitor. This is the nature of a transmission line that is in quarter-

wavelength resonance mode. It also helps to explain why we should never make PDN measurements by probing the top of a decoupling capacitor.

The lossy transmission line behaves like a quarter-wavelength resonator because it is open on one end and attached to the low board impedance on the other, as in [Figure 5.42](#). We normally think of a capacitor as a two terminal device, but it is actually distributed in nature with voltage drop across the series of plates. Transmission line effects are one reason why opposite ends of the capacitor have very different voltages at series resonant frequency.

The mounted capacitor draws maximal current and energy from the board at SRF because it is at its lowest impedance. However, the top of the capacitor has maximal voltage at that same frequency. The mounted capacitor actually amplifies PDN noise from the board when a PDN is measured by attaching an instrument to the top of the capacitor. The measured PDN noise is colored by increasing the noise at the SRF and attenuating it at other frequencies.

Another way to look at this situation is with lumped RLC components in parallel and series, as discussed in [section 2.9](#). When measuring the PDN voltage by attaching an instrument to the top of the capacitor, opposite from the board, the capacitance is in parallel with the mounting inductance. The LC combination forms a parallel resonance and impedance peak at the resonant frequency when viewed from the top. This amplifies the PDN noise voltage measured at the instrument in the resonant frequency band.

However, when the mounted capacitor is viewed from the board side, the capacitor is in series with the mounting inductance and makes a series resonant circuit. From the perspective of the board power planes,

the branch currents going into the power/ground vias and the voltage measured across the vias reveal the low impedance of a series resonant circuit. The very same mounted capacitor is a noise sink from the perspective of the board and a resonant noise amplifier from the perspective of an instrument looking down on top of the capacitor from the top of the board. Board PDN voltages should never be measured by attaching an instrument to the top of a capacitor—it is much better to dismount the capacitor and then attach the instrument to the pads.

So, both the lossy transmission line concept and lumped series/parallel resonant circuits predict the same thing. The noise voltage associated with a decoupling capacitor is opposite when viewed from the perspective of an instrument looking down on the cap or from the perspective of the board power planes looking up at the capacitor. The lossy transmission line behaves like a quarter-wavelength resonator attached to low impedance on the board end and open circuit on the other. The lumped LC elements are in series from the perspective of the board power planes and in parallel from the perspective of an instrument attached to the top of the capacitor. They have the expected impedance peaks and dips for parallel and series RLC circuits, respectively.

## 5.16 THE BOTTOM LINE

1. A real capacitor only behaves like an ideal capacitor at low frequency. It has a fundamentally different impedance behavior above about 10 MHz due to its series mounting inductance.
2. It is remarkable how well a simple ideal RLC circuit model matches the actual impedance behavior of real capacitors. This makes this model incredibly valuable for modeling real capacitors

individually or when connected in parallel.

3. In an RLC circuit, the ideal capacitance dominates the low-frequency impedance, the ideal inductance dominates the high-frequency impedance, and the minimum impedance is the ESR, which occurs at the self-resonant frequency (SRF).
4. When multiple, identical capacitors are combined in parallel, the resulting impedance profile is just the scaled impedance of each individual capacitor.
5. When two different capacitors are added in parallel, a new behavior emerges. A peak impedance exists between the two SRFs of the individual capacitors. This peak impedance is the most important feature in the PDN.
6. The three important ways of reducing the peak, parallel impedance between two capacitors are to reduce the ESL, bring the two capacitor values closer together, or increase the ESR. When optimizing the PDN impedance, take advantage of all of these design knobs.
7. Controlled ESR capacitors are important components to help damp the peak impedance caused when capacitors combine in parallel.
8. The mounting inductance of a capacitor is related to three components: the surface traces, the capacitor body, and the vias to the power and ground cavity. Reduce each of these to reduce the ESL to as low a value as practical.
9. In practical cases, reducing the mounted ESL of an MLCC capacitor to below 4 nH should always be possible. When done well, we can reduce the mounted ESL below 2 nH. In good designs, we can reduce it below 0.5 nH.
10. When the mounting inductance is well below 1

nH, the transmission line properties of a capacitor can become apparent. The transmission line model for a capacitor predicts the decreasing inductance and the increasing ESR with frequency.

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# Chapter 6. Properties of Planes and Capacitors

## 6.1 THE KEY ROLE OF PLANES

As a PDN component, the purpose of the power and ground planes in circuit boards or semiconductor packages is to connect the VRM and capacitors to the active devices and deliver a clean power supply to each active device, with an acceptably low voltage noise. The two chief factors that affect the PDN noise in the planes are the transient currents through the active devices and the planes' impedance.

We refer to the electrical structure created by the adjacent power and ground planes as a *cavity*. A cavity is any adjacent pair of planes, regardless of their DC voltage. This large, extended structure of conductors with dielectric between them traps any electric and magnetic fields and strongly influences how the fields propagate. Electromagnetic fields in the cavity “echo off the edges,” and bounce around, influenced by the cavity’s specific shape and geometry and any structures penetrating into the cavity.

### Tip

We call any pair of planes a *cavity* as it creates the boundary conditions of a waveguide to trap electromagnetic fields within it.

We shall see that unlike small, discrete components, the impedance of distributed structures such as the cavity composed of two planes is complicated. Ultimately, their three-dimensional nature affects the relationship between how currents flow in the cavity and the resulting dynamic, propagating, voltage distributions. However, we can create a few simplified

models for cavities that enable us to understand how their physical features affect the performance we need for robust PDNs.

In particular, at low frequency we model the cavity as a single lumped capacitance, corresponding to the cavity's parallel plate capacitance. The cavity inductance is well-represented by a loop inductance related to the spreading inductance between the two planes. The interaction between the cavity capacitance and cavity inductance results in a series or parallel resonant frequency depending on how we probe the cavity.

At higher frequencies, the modal resonances due to the speed of electromagnetic propagation in the cavity and the boundary conditions result in high impedance peaks.

Generally, lower impedance between the planes means a lower voltage noise generated for the same transient current. The guideline for power and ground plane design is simple: Do everything to reduce the planes' impedance.

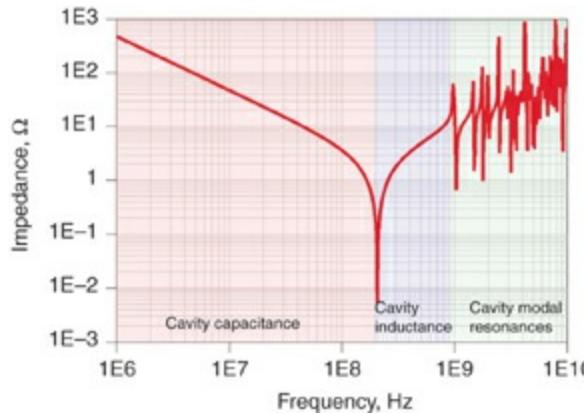
This generally translates into keeping the power and ground planes on adjacent layers in the board stackup with as thin a dielectric between them as practical. A secondary factor that influences the mounting inductance of the capacitors and IC packages on the board surface to the planes is to move the top of the power-ground cavity as close to the board's surface as practical.

#### Tip

The most important guideline in designing the planes is to do everything possible to reduce their impedance between the decoupling capacitors and the active devices. We do this by using wide planes on adjacent layers with as thin a dielectric between them as practical, placed in the stackup close to the board surfaces.

Always follow a design guideline or habit, if it is free. If it costs more to implement, we have to evaluate whether it is worth the cost: How much “bang for the buck” is there? We can only determine this by putting in the numbers—calculating the impact on PDN impedance and noise performance from the planes. This requires modeling the planes and integrating their electrical properties into the system circuit simulations.

The cavity impedance formed by the two planes depends on the cavity geometry and where we measure the impedance. [Figure 6.1](#) shows the simulated impedance looking into a pair of planes from two adjacent contact points on each of the two planes in the middle of the cavity. In this example, the planes are about 4 inches  $\times$  6 inches on a side, spaced by 64 mils and filled with FR4 dielectric.



**Figure 6.1** Impedance profile of a cavity looking in from the center showing three impedance regions.  
Simulated with Mentor Graphics HyperLynx PI.

This impedance profile shows three distinct regions: the low-frequency region, where the planes look like a capacitor; a mid-frequency region, where the planes look like an inductor; and the high-frequency region, where we see the sharp impedance transitions from the cavity modal resonances that looks like the impedance profile of a transmission line. We explore each of these three distinct frequency regimes separately.

**Tip**

Exploring cavity impedance in the frequency domain is convenient because we can divide it into three sections: the low-frequency range, where it looks like a capacitor; the mid-frequency range, where it looks like an inductor; and the high-frequency where it looks like a transmission line.

## 6.2 LOW-FREQUENCY PROPERTY OF PLANES: PARALLEL PLATE CAPACITANCE

At low frequency, the power and ground cavity impedance is all about its capacitance. We estimate this cavity capacitance using the parallel plate approximation, which assumes no fringe fields outside the boundary of the edge of the planes:

$$C = \epsilon_0 Dk \frac{A}{h} \quad (6.1)$$

where

C = the capacitance between the planes

A = area of overlap

h = the dielectric thickness between the planes

$\epsilon_0$  = the permittivity of free space =  $8.85 \times 10^{-12}$  F/m  
= 0.227 pF/inch

Dk = the dielectric constant of the material between the cavity.

In the special case of FR4 as the dielectric, with a Dk = 4.2, this reduces to a simple relationship between capacitance per unit area in pF/inch<sup>2</sup> and dielectric thickness as

$$\frac{C}{A} \left[ \frac{\text{pF}}{\text{inch}^2} \right] = \epsilon_0 Dk \frac{1}{h} = 0.227 \frac{\text{pF}}{\text{inch}} \times 4.2 \times \frac{1}{\text{h}[ \text{inches} ]} = \frac{0.95}{\text{h}[ \text{inches} ]} \sim \frac{1}{\text{h}[ \text{inches} ]} \quad (6.2)$$

If we measure the dielectric spacing between the planes in units of mils, then the capacitance per area, in nF/inch<sup>2</sup>, is simply:

$$\frac{C}{A} \left[ \frac{nF}{inch^2} \right] \sim \frac{1}{h[mil]} \quad (6.3)$$

For example, if the dielectric thickness is 3 mils, the capacitance per area between the planes is  $C = 0.3$  nF/inch<sup>2</sup>. A pair of planes that are 10 inches on a side have a capacitance of about  $0.3 \text{ nF/inch}^2 \times 100 \text{ inches}^2 = 30 \text{ nF}$ .

**Tip**

As a rough rule of thumb, the capacitance of a cavity, separated by 1 mil and filled with FR4, has a capacitance per area of about 1 nF/inch<sup>2</sup> and decreases inversely as the dielectric thickness increases.

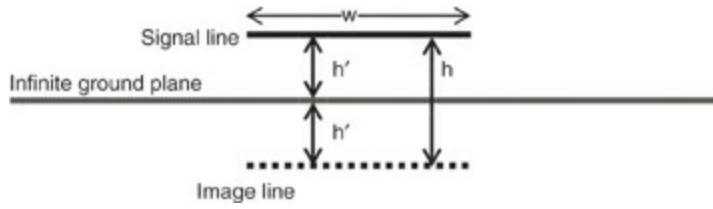
This parallel plate approximation assumes that the fringing fields around the edge of the planes are negligible. There are always fringe fields around the edges of the plates. At high aspect ratios, the parallel plate capacitance dominates and we can ignore the fringing fields. However, for smaller aspect ratios, the fringe field capacitance plays a role. We can estimate this effect.

### 6.3 LOW-FREQUENCY PROPERTY OF PLANES: FRINGE FIELD CAPACITANCE

We explore the contribution from the fringe fields around the edges of the planes that make up the cavity by comparing the parallel plate capacitance with the capacitance calculated using a field solver, which includes the parallel plate and fringe field capacitances. We expect the field solver to calculate a larger capacitance than the parallel plate approximation. The difference is the fringe field contribution.

We can even use a 2D field solver to estimate the fringe fields per length around the edges of a pair of planes. Most 2D field solvers make the approximation

that the return plane is infinitely wide. The field solver calculates the capacitance between the signal line and the plane located a distance  $h'$  (h prime) away. This is twice the capacitance as that between a signal line on the top of the plane to an image signal line located an equal distance below the plane, with a total separation of  $h$ , with  $h = 2 \times h'$ , as illustrated in Figure 6.2.



**Figure 6.2** Example of the cross section looking down the length of a transmission line of a signal line over an infinitely wide return plane and the signal line's image on the other side of the return plane.

The 2D field solver calculates the characteristic impedance of the line. From the time delay, we calculate the total capacitance of the line as

$$C = \frac{TD}{Z_0} = \frac{Len}{cZ_0} \sqrt{Dk} \quad (6.4)$$

where

$C$  = the capacitance of the signal line to the plane =  
two times the capacitance between the signal line  
and its image line

$TD$  = the time delay of the signal line as a  
transmission line

$c$  = the speed of light in air = 11.8 inches/nsec

$Z_0$  = the characteristic impedance of the signal line to  
the plane, in  $\Omega$

$Dk$  = the dielectric constant of the material between  
the signal line and the return plane

In the special case of just air between the signal and return,  $Dk = 1$  and we estimate the capacitance per

length of the microstrip as

$$C_{\text{Len}} = \frac{1}{cZ_0} = \frac{84}{Z_0} \text{ pF/inch} = 2 \times C_{\text{Len-image}} \quad (6.5)$$

The capacitance between the top conductor and the return plane is twice the capacitance between the signal line and its image, because the two capacitances are in series. This makes the capacitance between the signal line and its image

$$C_{\text{Len-image}} = \frac{1}{2} C_{\text{Len}} = \frac{42}{Z_0} \text{ pF/in} \quad (6.6)$$

This total capacitance per length between the signal line and its image line is composed of the parallel plate contribution and the fringe field capacitance along both sides of the transmission line:

$$C_{\text{Len-image}} = C_{\text{Len-pp-image}} + 2 \times C_{\text{Len-fringe-image}} \quad (6.7)$$

where

$C_{\text{Len-image}}$  = the capacitance per length between the signal and its image line, calculated from the 2D field solver

$C_{\text{Len-pp-image}}$  = the parallel plate capacitance per length calculated between the signal line and its image line

$C_{\text{Len-fringe-image}}$  = the fringe field capacitance per length along one edge of the two conductors spaced a distance,  $h$  apart

Using the parallel plate approximation, we calculate the capacitance, with no fringe fields, between the signal line and its image line as

$$C_{\text{pp-image}} = \epsilon_0 Dk \frac{w \times \text{Len}}{h} \quad (6.8)$$

From this, the parallel plate capacitance per length

between the signal line and its image line is just

$$C_{\text{Len-pp-image}} = \frac{C_{\text{pp-image}}}{\text{Len}} = \epsilon_0 Dk \frac{w}{h} = 0.227 \frac{w}{h} \text{ pF/inch} \quad (6.9)$$

where

$C_{\text{pp-image}}$  = the parallel plate capacitance between the signal line and its image line located  $2h$  away

$C_{\text{Len-pp-image}}$  = the parallel plate capacitance per length between the signal line and its image line located  $2h$  away

$\epsilon_0$  = the permittivity of free space, = 0.227 pF/inch

$Dk$  = the dielectric constant of the medium between the lines and  $Dk = 1$  for this special case

$\text{Len}$  = the length of the signal line

$w$  = the line width of the signal line

$h$  = the separation between the signal line and its image line

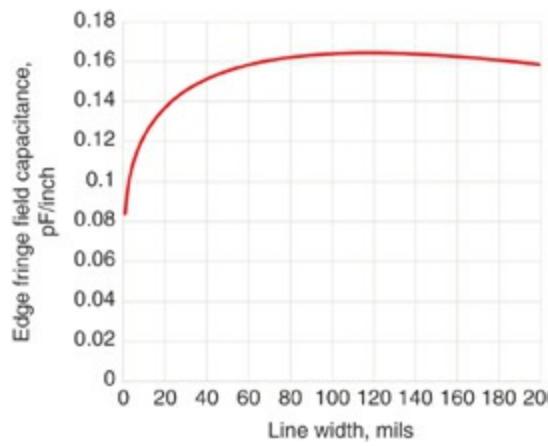
We calculate the capacitance per length from just the fringe fields along one edge of two conductors, in this case, the signal line and its image line spaced a distance  $h$ , as half the total fringe field contribution to the capacitance between these two conductors:

$$C_{\text{Len-fringe-image}} = \frac{1}{2} (C_{\text{Len-image}} - C_{\text{Len-pp-image}}) \quad (6.10)$$

We can explore this relationship and the properties of fringe fields around the edges of conductors using any 2D field solver. For example, we expect that as the line width increases above some aspect ratio, the fringe field contribution should be independent of the line width.

Using the Polar Instruments SI 9000 2D field solver, we calculate the characteristic impedance of a microstrip transmission line with air as the dielectric and  $h' = 5$  mils, as we increase the line width from 2

mils to 200 mils. This is an aspect ratio, w/h, change of 0.2 to 20. Figure 6.3 shows the extracted fringe field capacitance per length along each edge of the two conductors separated by  $2 \times 5$  mils = 10 mils. Note that above a line width of about 50 mils, or aspect ratio of 5 to 1, the fringe field capacitance is independent of line width and is about 0.16 pF/inch. For very narrow lines, the number of fringe field lines are cut in half because the field lines from both edges arise from the same location on the conductor.



**Figure 6.3** Fringe field capacitance per length along the edge of two equal width conductors separated by 10 mils, as the lines' width increases.

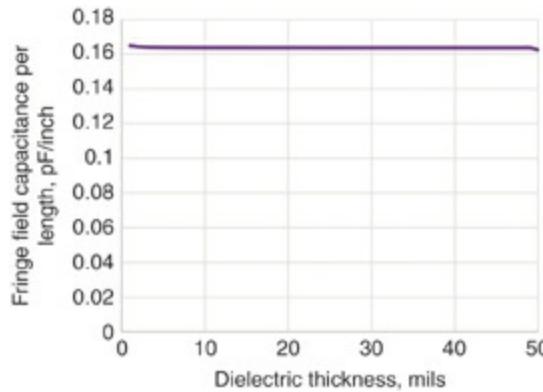
The very slight dropoff in the fringe field capacitance for line widths wider than 140 mils, or aspect ratios larger than 14, is probably due to the slight inaccuracies from the field solver from a non-optimized mesh size and very high aspect ratio structure.

It is interesting to note that for an aspect ratio greater than 10, the difference between the characteristic impedance of a microstrip and the parallel plate capacitance per length is constant. This means that the fringe field capacitance per length of edge of two planes is independent of the dielectric spacing, as long as the aspect ratio is large.

We confirm this by changing the dielectric thickness from 1 mil to 50 mils, keeping the aspect ratio of the

line width to dielectric thickness = 10 and calculating the fringe field capacitance per length of the edge.

Independent of the dielectric thickness, the fringe field capacitance of the edge is 0.16 pF/inch, as shown in Figure 6.4.



**Figure 6.4** Fringe field capacitance per length of edge between two plates in air, as the dielectric thickness between them increases at a fixed aspect ratio of 10. Note the fringe field capacitance is independent of the dielectric spacing and is about 0.16 pF/inch.

This analysis suggests that the fringe field capacitance between two plates is approximately 0.16 pF/inch of edge length. Knowing the parallel plate capacitance, we estimate the additional capacitance expected from the fringe fields and the total capacitance of the planes. This assumes the plates are filled with a dielectric of dielectric constant,  $Dk$ , which does not extend outside the plates, where the fringe fields are. The total capacitance is approximately the parallel plate capacitance and the fringe field capacitance from the four edges as

$$C_{\text{total}} = C_{\text{pp}} + C_{\text{ff}} = \epsilon_0 Dk \frac{w \times \text{Len}}{h} + 4 \times \text{Len} \times 0.16 \text{ pF/inch} \quad (6.11)$$

In the special case of a square cavity, with  $w = \text{Len}$ , this reduces to

$$C_{\text{total}} = \epsilon_0 Dk \frac{\text{Len}}{h} \text{Len} + 4 \times \text{Len} \times 0.16 \text{ pF/inch} \quad (6.12)$$

where

$C_{\text{total}}$  = the total capacitance between two plates

$C_{\text{pp}}$  = the parallel plate capacitance

$C_{\text{ff}}$  = the capacitance contribution from the fringe fields around the four edges

$Dk$  = the dielectric constant of the material between the plates

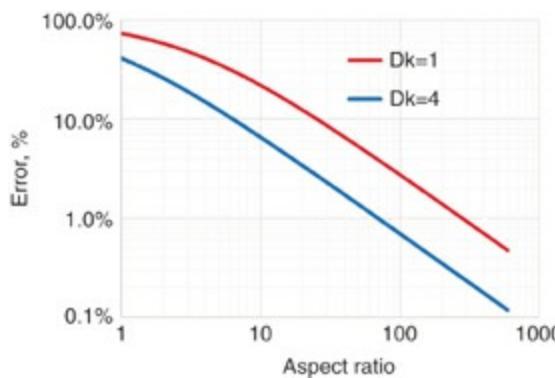
$h$  = the dielectric spacing between the plates

$\text{Len}$  = the length of a side of the square plates

We estimate the relative error of the capacitance calculated with the parallel plate approximation compared to the field solver from

$$\text{error} = \frac{\text{fringe field capacitance}}{\text{total capacitance}} = \frac{4 \times 0.16}{0.227 \times Dk \times \frac{\text{Len}}{h} + 4 \times 0.16} \quad (6.13)$$

This suggests that the error in estimating the total capacitance from just the parallel plate capacitance decreases with larger aspect ratio. **Figure 6.5** shows the relative error of the parallel plate approximation for the case of air between the plates and FR4 with a  $Dk = 4$ .



**Figure 6.5** The relative error of the parallel plate approximation with a dielectric inside the plates of 1 and 4, with air outside the plates. The higher the dielectric between the plates, the smaller the contribution from the fringe field lines and the less the error using the parallel plate approximation.

When air is between the plates, the error in using the

parallel plate capacitance is as large as 20% for a 10-to-1 aspect ratio. It drops to 7% when the plates are filled with FR4.

## 6.4 LOW-FREQUENCY PROPERTY OF PLANES: FRINGE FIELD CAPACITANCE IN POWER PUDDLES

The previous analysis assumed the dielectric fill extended only to the edge of the plates. This is the case when the plates are cut out of the board and the cavity is stand-alone. This occurs when a piece of the board is cut out to do a quick Dk measurement.

In the next example the power and ground planes are created as islands or “puddles” in the board, in which case the dielectric extends outside the cavity and increases the fringe field capacitance. In cross section, this looks very similar to a microstrip. We can use any 2D field solver to estimate the contribution to the fringe field lines. The same analysis applies as before; it is just that we use the 2D field solver to calculate the total capacitance with the fringe fields extending into the dielectric slab. The total capacitance per length, which we extract from the characteristic impedance calculated with the 2D field solver is composed of

$$C_{\text{Len-total}} = C_{\text{Len-pp}} + 2 \times C_{\text{Len-fringe}} \quad (6.14)$$

and

$$C_{\text{Len-fringe}} = \frac{1}{2} (C_{\text{Len-total}} - C_{\text{Len-pp}}) \quad (6.15)$$

The fringe field capacitance on each edge in the presence of the dielectric slab is calculated from this relationship. In the case of a square section of power plane puddle, the parallel plate capacitance is

$$C_{\text{pp}} = \epsilon_0 Dk \frac{w \times \text{Len}}{h} \quad (6.16)$$

where

$C_{pp}$  = the total parallel plate capacitance between the signal and its return

$C_{Len-pp}$  = the capacitance per length from just the parallel plate capacitance

$C_{Len-total}$  = the total capacitance per length of the microstrip transmission line

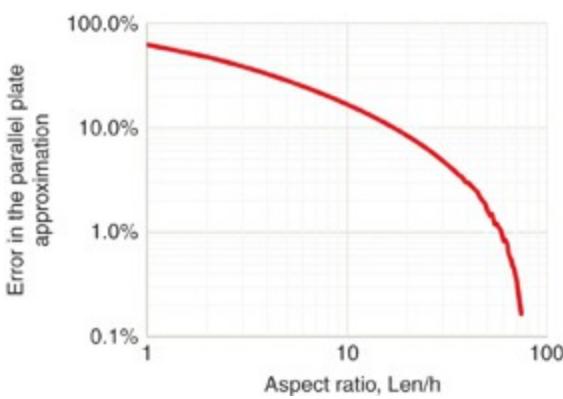
$C_{Len-fringe}$  = the capacitance per length from the fringe fields along one edge

The relative error in using the parallel plate approximation over the total capacitance is

$$\text{error} = \frac{4 \times \text{Len} \times C_{Len-fringe}}{C_{pp} + 4 \times \text{Len} \times C_{Len-fringe}} \quad (6.17)$$

The error decreases as the aspect ratio increases.

Using the special case of a square section of power puddle and  $Dk = 4$ , Figure 6.6 shows the calculated error in using the parallel plate approximation over a field solver. We see that even when the aspect ratio is as large as 10, the error is almost 20% using the parallel plate approximation. To achieve a 1% error requires an aspect ratio of 50. This might seem like a lot but we usually meet this condition. For a 6 mil dielectric thickness, we require the power puddle to be  $50 \times 6 = 300$  mils or 0.3 inches on a side to have less than 1% error. Power puddles are often bigger than 0.3 inches.



**Figure 6.6** Error in using the parallel plate approximation compared to a field solver for a square power puddle with FR4 and  $Dk = 4$ . Note that even with an aspect ratio of 10, the parallel plate error is about 20%.

#### Tip

The parallel plate approximation is accurate to only about 20% even when the aspect ratio of width to dielectric thickness is as large as 10 to 1. Keep this in mind when using a parallel plate capacitor model to calculate the capacitance between two planes.

This approximation is usually the basis of measuring the  $Dk$  of laminates: build a large cavity and measure the capacitance. From the measured capacitance and geometry, extract the  $Dk$ . This technique is only accurate at low frequency where the quasi-static approximation applies and the cavity looks like a lumped capacitor. In addition, the aspect ratio must be surprisingly high for us to get an accurate measure of the  $Dk$  using the parallel plate approximation.

When measuring the impedance between the planes, we extract the capacitance at low frequency by interpreting the impedance as a simple lumped capacitor model:

$$C = \frac{-1}{\text{imag}(Z) \times 2\pi f} \quad (6.18)$$

where

$C$  = the extracted lumped circuit equivalent

capacitance

$\text{imag}(Z)$  = the imaginary component of the complex impedance

$f$  = the sine wave frequency

From the capacitance and the parallel plate approximation, we extract the  $Dk$ :

$$Dk = \frac{C \times h}{\epsilon_0 A} \quad (6.19)$$

where

$C$  = the extracted capacitance from the impedance measurement

$h$  = the dielectric thickness between the planes in the cavity

$A$  = the area of overlap of the planes

$\epsilon_0$  = permittivity of free space, 0.227 pF/inch

As an example, we measure a simple two-layer board with top and bottom planes extending to the board edge, 4.53 inches  $\times$  6.3 inches and 64 mils thick using the two-port technique described in [Chapter 3](#). From  $S_{21}$ , we extract the impedance using

$$Z = 25\Omega \frac{S_{21}}{1 - S_{21}} \quad (6.20)$$

From the impedance, we extract the capacitance and  $Dk$ , assuming the quasi-static model and the parallel plate approximation.

For the longest dimension, 6.3 inches, the quasi-static approximation is accurate up to a frequency of about

$$f[\text{GHz}] < \frac{1}{20} \frac{c}{\lambda \sqrt{Dk}} = \frac{1}{20} \frac{11.8}{\lambda \sqrt{4}} = \frac{0.3}{\text{Len}[{\text{inches}}]} = \frac{0.3}{6.3} \sim 50 \text{ MHz} \quad (6.21)$$

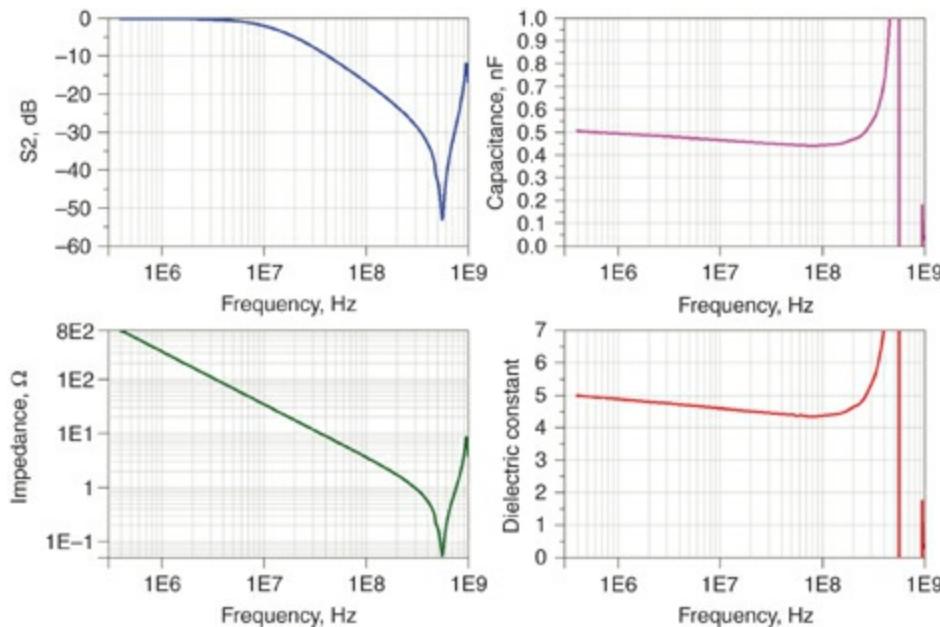
This corresponds to the physical dimension of the structure being 1/20 of a wavelength in the FR4.

The aspect ratio, the width of the narrowest side/dielectric thickness was about  $4.5/0.064 = 70$  for this board. We expect the parallel plate approximation to be accurate to less than 1%.

#### Tip

Using the capacitance of a parallel plate capacitor is the most common and simplest way of measuring the DK of a laminate substrate. Two important considerations when interpreting the capacitance are that the structure should be electrically short, with a length of a side  $< 1/20 \lambda$  of the frequency measured, and the aspect ratio of the width to the dielectric thickness should be at least 50 for better than 1% accuracy.

Figure 6.7 shows the plots for the impedance, extracted capacitance, and calculated Dk, based on the parallel plate approximation for this simple cavity. We see that the capacitance and dielectric constant are slowly decreasing with frequency. This is due to a real variation in the dielectric constant with frequency, referred to as *material dispersion*.



**Figure 6.7** The measured insertion loss of a cavity and the extracted impedance, capacitance, and dielectric constant. The frequency dependence of the dielectric constant is the dispersion in the material. The simple lumped circuit model for this cavity applies to no higher than about 50 MHz.

We see that the first dip in the impedance is at 500 MHz. The impedance begins to deviate from an ideal lumped capacitor at about 100 MHz, close to our estimated limit of 50 MHz.

The Dk for this material is extracted as about 5 at very low frequency below 1 MHz and decreases to about 4.3 at 100 MHz. The measured capacitance is slightly higher than the parallel plate estimate of this structure due to the fringe fields. Given the aspect ratio of 70, the error is about 1%. This means the extracted Dk, based on a higher capacitance, is higher than the actual Dk by about 1%.

Of course, modeling the two planes as a distributed cavity or transmission line rather than a lumped capacitor allows extraction of the dielectric constant to much higher frequency than 50 MHz.

## 6.5 LOOP INDUCTANCE OF LONG, NARROW CAVITIES

The inductance associated with a cavity is one of its most confusing electrical properties. When exploring approximations for loop inductance in [Chapter 4](#), we introduced an approximation for the loop inductance of a pair of long, wide conductors with a thin spacing between them. We also introduced the term *sheet inductance* in analogy with sheet resistance, and the number of squares down the length of the planes. We introduced loop inductance:

$$L_{\text{loop}} = \mu_0 \times h \times \frac{\text{Len}}{w} = (32 \text{ pH/mil} \times h) \times \frac{\text{Len}}{w} = L_{\text{sq}} \times n \quad (6.22)$$

where

$L_{\text{loop}}$  = loop inductance in nH

$\mu_0$  = permeability of free space =  $4\pi \times 10^{-7}$  H/m = 32

nH/inch = 32 pH/mil

Len = length of the conductors, in mils

w = width of the conductors in mils

h = dielectric thickness between the conductors in mils

$L_{sq}$  = the sheet inductance in nH/square

n = the number of squares down the length of the conductor

**Tip**

The sheet inductance of a cavity is the most important figure of merit that characterizes the inductance of a cavity. The loop inductance of any rectangular section cut out of the cavity is the sheet inductance times the number of squares that fit down the length.

In the special case of the loop inductance of two long and narrow planes, measured from one end and shorted together at the far end, we assume the current density in the top and bottom plane is uniform. In this special case, the loop inductance is related directly to the conductor lengths and spacing and inversely with the line width. Figure 6.8 shows an example of a pair of planes 30 inches long and 0.3 inches wide, with a spacing between them of 1 mil. In this geometry the aspect ratio between the width and dielectric spacing is 300/1 and the aspect ratio of the length to the width is 30/0.3 = 100/1.

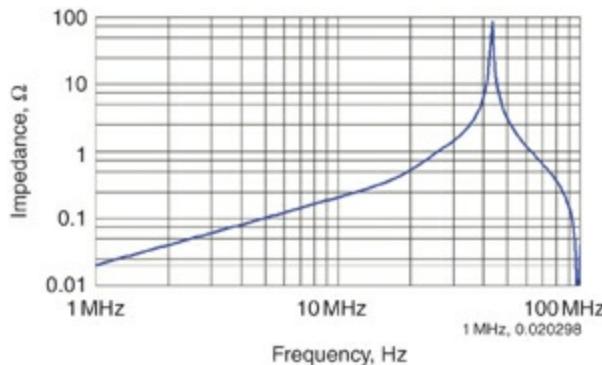


**Figure 6.8** Top view dimensions for a long and narrow cavity, with a dielectric thickness of 1 mil.

The approximation of Equation 6.22 predicts the loop inductance as viewed from one end to be

$$L_{loop} = \left(32 \text{ pH/mil} \times h\right) \times \frac{\text{Len}}{w} = \left(32 \text{ pH/mil} \times 1 \text{ mil}\right) \times \frac{30 \text{ in}}{0.3 \text{ in}} = 32 \text{ pH} \times 100 = 3.2 \text{ nH} \quad (6.23)$$

For this 30-inch-long structure, we expect the quasi-static model of describing this as a lumped inductor to apply up to about  $(6 \text{ inches/ns})/30 \text{ inches} \times 1/20 = 10 \text{ MHz}$ . One wavelength fits into the 30-inch structure at  $6/30 = 0.2 \text{ GHz} = 200 \text{ MHz}$  and the approximation is good to about  $1/20$  of a wavelength. Figure 6.9 shows the impedance profile of this structure simulated with a full-wave 3D field solver.



**Figure 6.9** Simulated impedance profile of the long and narrow cavity, shorted at the far end. Simulated with Mentor Graphics HyperLynx PI.

The impedance matches that of an inductor up to a frequency of about 20 MHz, where it increases more rapidly at the onset of the transmission line properties. Our estimate of 10 MHz as the limit to using the lumped circuit approximation is a safe estimate. From this simulated impedance curve and knowing the behavior is that of an inductor, we pick one frequency (1 MHz) and extract the inductance:

$$Z = |j\omega L| \quad \text{and} \quad L [\text{nH}] = \frac{1000}{2\pi} \frac{1}{Z_{1\text{MHz}}} Z_{1\text{MHz}} = 159 \times Z_{1\text{MHz}} \quad (6.24)$$

where

$L[\text{nH}]$  = the extracted inductance, in nH  
 $Z_{1\text{ MHz}}$  is the magnitude of the impedance at 1 MHz, if the profile is that of an inductor

In the example in Figure 6.9, the marker readout

(listed in the lower-right corner of the figure) shows the impedance at 1 MHz to be  $0.0203 \Omega$ . This results in an extracted inductance of  $159 \times 0.0203 = 3.23 \text{ nH}$ . This matches our approximation predicted from uniform current density.

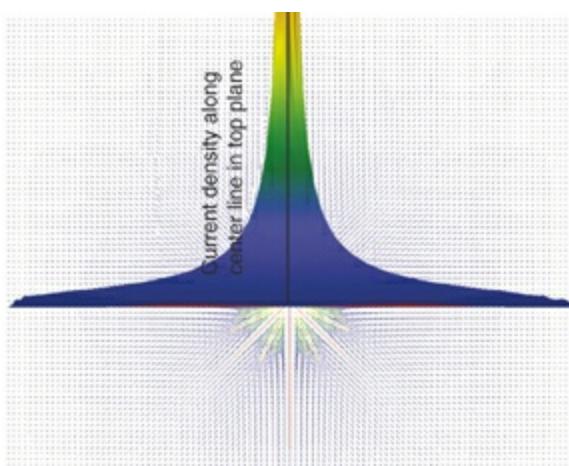
In this example, the conductor strip was only 0.3 inches wide, which is very narrow compared to the length. Even though the simulated current was launched into the cavity from a via point-contact, within a distance of a few trace widths the current fans out to be uniformly distributed down the length. This matches the assumption in the simple approximation of [Equation 6.22](#).

**Tip**

The estimated loop inductance of a pair of long narrow strips matches the value calculated with a 3D field solver. We have a good approximation for this calibration structure.

## 6.6 SPREADING INDUCTANCE IN WIDE CAVITIES

When the cavity is not long and narrow but wide, the current density in the top and bottom planes may not be uniform. When a signal is launched from small contact points between the planes, it spreads out radially from the launch points until it hits the walls and is distorted from multiple reflections. [Figure 6.10](#) shows the current density in the top conductor of a cavity as a radial current wave front spreads outward when launched at the center.



**Figure 6.10** Top view of the current distribution in the top conductor of a cavity with current spreading out radially from a central contact point. Superimposed is the profile of the initial current density along a line in the cavity. Simulated with Mentor Graphics HyperLynx PI.

As introduced in [section 4.7](#), current flow restricted to a narrower path increases the inductance of that path. As the current spreads outward from the central contact point, illustrated in [Figure 6.10](#), the loop inductance per length decreases. We refer to the loop inductance, when the current path is spreading outward from a small contact region, as the *spreading* loop inductance or just the *spreading* inductance. This is the inductance associated with the cavity. The closer we move toward the central contact point and the higher the current density, the higher the cavity spreading inductance.

**Tip**

Spreading inductance in a cavity is the loop inductance the propagating current wavefront sees as it “spreads” outward from a central contact point into the increasing dimensions of the cavity. The current loop wavefront flows between the top and bottom planes.

We will consider the cavity in two configurations. The first configuration is shorted where there is at least one via tying the top and bottom planes together with an inductive connection. The second configuration is open where the cavity looks capacitive at low frequencies. We

see the spreading inductance effect in both cases.

Current spreads out from the single observation contact point and flows through the cavity planes to find a return path.

Initially, we use an observation point at the center of a circular cavity and the return path is through a shorting wall at the outside edge of the cavity. Later we remove the shorting wall and consider displacement current as the return path. We will also consider situations where the cavity is rectangular and the contact point is at the edge or in a corner rather than the center.

The loop inductance associated with the current path is the cavity spreading inductance. It makes little difference whether the cavity is driven by a current source in the cross section of a shorting via or a voltage source looking into a small via clearance hole that separates the via and one of the planes. The current and magnetic field patterns are the same. The latter situation is a VNA port configuration.

Three equivalent ways of calculating the loop inductance are associated with the center-contacted circular cavity, as seen by the propagating current waveform:

- From the magnetic field lines encircling the launching via and Ampere's Law
- As the loop inductance of a section of coax cable with the via being the signal conductor and the return path as a shorting wall at the circumference of the cavity
- From the spreading inductance associated with the current waveform as it propagates in the cavity between the two planes as displacement current

In the first approach, the loop inductance of the cavity is allocated to the partial self-inductance of the via in

which the current flows from the top of the contact point to the bottom of the cavity. The impedance looking into a pair of circular planes has been analytically calculated [1].

We estimate the circular lines of magnetic flux from the current going through the via from Ampere's Law. We calculate the cavity's loop inductance by integrating the magnetic field lines inside the cavity. From the tangential component of the magnetic field distribution inside the cavity, we calculate the associated current distributions in the planes.

The magnetic field lines around an infinitely long round rod with a current  $I$  are concentric, circular loops that decrease in density farther from the rod's center. We calculate the  $B$  field density some distance  $R$  away from the rod from Ampere's Law:

$$B = \frac{\mu_0}{2\pi} I \frac{1}{R} \quad (6.25)$$

We assume the via from the top of the cavity to the bottom plane has a partial self-inductance of a section of the round rod of length  $h$ . When we count the rings of magnetic field lines surrounding the short via, we count the ones passing through a rectangular section of the cavity, to a distance  $R$  into the cavity. The partial self-inductance is

$$L_{via} = \frac{flux}{I} = \frac{1}{I} \iint_{R=R_{via}}^{R=R_{cavity}} B \cdot da = \frac{\mu_0}{2\pi} h \int_{R=R_{via}}^{R=R_{cavity}} \frac{1}{R} dR = \frac{\mu_0}{2\pi} \times h \times \ln\left(\frac{R_{cavity}}{R_{via}}\right) \quad (6.26)$$

where

$L_{via}$  = the partial self-inductance of the via

$B$  = the magnetic field density in the cavity from the current  $I$  passing through the via

$I$  = the current through the via

$R_{via}$  = the outer radius of the via

$R_{cavity}$  = the radius of the cavity

$h$  = the spacing between the planes of the cavity

The loop inductance associated with the current in the cavity is all assigned to the via and we derive it with

$$L_{cavity} = L_{via} = \frac{\mu_0}{2\pi} \times h \times \ln\left(\frac{R_{cavity}}{R_{via}}\right) \quad (6.27)$$

Although this approach is mathematically simple, it does not reveal much insight into how the physical design of the cavity influences the inductance seen by currents flowing between the planes.

In the second approach, we think of the via as the center conductor in a coax cable, with the return path being the displacement current at some distance from the return via. The loop inductance per length of a coax cable is

$$L_{Len-coax} = \frac{\mu_0}{2\pi} \times \ln\left(\frac{b}{a}\right) \quad (6.28)$$

And the total loop inductance of a section of coax of length, Len, is

$$L_{loop} = L_{Len-coax} \times Len = \frac{\mu_0}{2\pi} \times \ln\left(\frac{b}{a}\right) \times Len \quad (6.29)$$

where

$b$  = the outer radius of the return path

$a$  = the inner radius of the central signal path

$\mu_0$  = permeability of free space,  $4\pi \times 10^{-7}$  H/m

In the special case with

$Len = h$

$b = R_{cavity}$

$a = R_{via}$

the loop inductance of a via, modeled as a section of coax cable becomes

$$L_{\text{via-coax}} = \frac{\mu_0}{2\pi} \times h \times \ln\left(\frac{R_{\text{cavity}}}{R_{\text{via}}}\right) \quad (6.30)$$

This is the same result as in the first case, assigning all the cavity inductance to the via partial self-inductance. This comparison also gives a hint as to how to think of the inductance of a via: the current loop is the current going down the via and returning through the shorting wall between the bottom and top of the cavity at the perimeter edge. The larger the cavity, the farther the current travels and the larger the loop inductance of the via-cavity pair.

The third approach, based on the concept of cavity spreading inductance, is a powerful way of considering the influence of design features on current flow and the cavity's electrical properties. Current from a decoupling capacitor, for example, enters into a cavity and spreads out to other decoupling capacitors and to silicon load chips mounted somewhere on the same cavity using similar vias. The concept of spreading inductance gives us a tool to think about the relative placement of the several current sources and sinks that are associated with a power-ground plane cavity. Gaining this insight from the special case of cylindrical geometry current flow or from a 3D field solver is difficult.

Spreading inductance is all about the specific, non-uniform current distribution in the conductors. It often requires a 3D field solver to calculate, given the details of the planes' geometries and location of the short. We can even use a quasi-static field solver to calculate the spreading inductance of a particular cavity geometry because it is a DC effect. An accurate prediction of the higher frequency impedance of the cavity, where full-

wave effects play a role, might require a full-wave field solver.

**Tip**

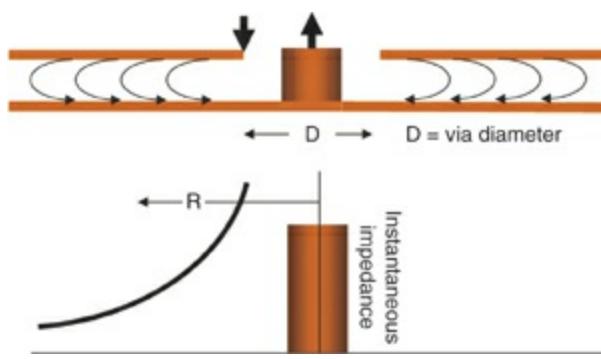
In general, the spreading inductance in a cavity depends on all the details of the current source and sink contact points and the precise current distribution in the planes. Other than a few simple cases, we can only calculate it with a 3D field solver taking into account the precise current distribution.

For the simplest case of current injected at a central point and spreading outward from the center of a circular cavity, we can derive a simple relationship about how the geometrical features influence the spreading inductance.

When we look at the low-frequency impedance the signal sees from the center, we see the capacitance at low frequency and the spreading inductance at slightly higher frequency.

When viewed at a single contact point in the cavity, the spreading inductance created by the current spreading out from the via to the cavity always sets the trend to the impedance we see looking into a plane-pair cavity at high frequency.

We estimate the spreading inductance based on the impedance the signal sees spreading outward. As the current travels from the center contact to the board edge, it encounters an instantaneous impedance each step of the way, as illustrated in [Figure 6.11](#).



**Figure 6.11** Current wave front propagating radially out from a central contact point sees an instantaneous impedance decreasing with distance.

To estimate the instantaneous impedance and spreading inductance of a cavity let us first consider a one-dimensional transmission line. When we approximate a uniform transmission line as an n-section lumped circuit model and make the sections infinitesimally small, we can calculate the characteristic impedance and time delay by solving the telegrapher's equations; the resulting wave equations reveal the familiar approximations:

$$Z_0 = \sqrt{\frac{L_{Len}}{C_{Len}}} \quad \text{and} \quad v = \frac{1}{\sqrt{L_{Len} C_{Len}}} = \frac{c}{\sqrt{Dk}} \quad (6.31)$$

where

$Z_0$  = the characteristic impedance and the instantaneous impedance

$L_{Len}$  = the loop inductance per length of the transmission line

$C_{Len}$  = the total capacitance per length of the transmission line

$v$  = the speed of the signal

$c$  = the speed of light in air

$Dk$  = the dielectric constant of the materials

Multiplying the equations in Equation 6.31:

$$Z_0 \times v = \sqrt{\frac{L_{\text{Len}}}{C_{\text{Len}}}} \times \frac{1}{\sqrt{L_{\text{Len}} \times C_{\text{Len}}}} = \frac{1}{C_{\text{Len}}} \quad \text{and} \quad Z_0 = \frac{1}{vC_{\text{Len}}} = \frac{\sqrt{Dk}}{cC_{\text{Len}}} \quad (6.32)$$

This relationship suggests that we can estimate the instantaneous impedance seen by a signal propagating in a transmission line based on the capacitance per length at that location and the dielectric constant of the medium. We calculate the instantaneous impedance seen by the radially spreading current in the cavity and estimate the spreading inductance.

As a signal is launched from the via contact and travels between the cavity's top and bottom planes, it spreads out as a circular wavefront like the ripples of water in a pond after a stone has been thrown in. We calculate the instantaneous impedance seen by the radial wave at the leading edge.

The capacitance per radial length uncovered at the leading edge of the wavefront increases as the circumference of the current wavefront increases. Using the parallel plate approximation at a distance R from the center contact, the capacitance in a short annulus of width, dR, in the direction of the radially traveling wave is

$$dC = \epsilon_0 Dk \frac{A}{h} = \epsilon_0 Dk \frac{2\pi R \times dR}{h} \quad (6.33)$$

where

$dC$  = the small capacitance in a short section of the radial path

$A$  = overlap area in the parallel plate approximation

$h$  = dielectric thickness between the planes

$R$  = distance from center of the contact point

$dR$  = small increment in path length

$Dk$  = the dielectric constant of the laminate in the cavity

The capacitance per length of the path is

$$C_{\text{Len}} = \frac{dC}{dR} = \epsilon_0 Dk \frac{2\pi R}{h} \quad (6.34)$$

where

$C_{\text{Len}}$  = the capacitance per length along the radial path

The instantaneous impedance  $Z$  the radial wavefront sees is then

$$Z = \frac{\sqrt{Dk}}{c C_{\text{Len}}} = \frac{h \sqrt{Dk}}{c \epsilon_0 Dk 2\pi R} = \frac{1}{2\pi c \epsilon_0 \sqrt{Dk}} \frac{h}{R} = \frac{1}{2\pi \sqrt{\frac{1}{\mu_0 \epsilon_0}} \sqrt{Dk}} \frac{h}{R} = \frac{\sqrt{\frac{\mu_0}{\epsilon_0}} h}{2\pi \sqrt{Dk} R} \quad (6.35)$$

Using the relationship that

$$Z_{\text{free\_space}} = \sqrt{\frac{\mu_0}{\epsilon_0}} = 377 \Omega \quad (6.36)$$

we arrive at

$$Z = \frac{\sqrt{\frac{\mu_0}{\epsilon_0}} h}{2\pi \sqrt{Dk} R} = \frac{377 \Omega}{2\pi \sqrt{Dk}} \frac{h}{R} = \frac{60 \Omega}{\sqrt{Dk}} \frac{h}{R} \quad (6.37)$$

The instantaneous impedance the current wavefront sees traveling radially outward in the cavity is described by a simple relationship. It decreases with increasing  $R$ , the distance from the central contact point. In addition, the impedance is proportional to the spacing between the planes. The thinner the dielectric spacing, the lower the impedance a signal sees.

**Tip**

The cavity thickness is the most important property seen by a current wavefront. It affects the instantaneous impedance inside the cavity. Thinner dielectric between the power and ground planes results in lower impedance for the power and return currents and lower voltage noise generated.

For example, the case of a cavity filled with FR4 having a dielectric thickness of 1 mil and looking 1 inch from a central contact point, the instantaneous impedance is

$$Z = \frac{60\Omega}{\sqrt{Dk}} \frac{h}{R} = \frac{60\Omega}{\sqrt{4}} \frac{0.001}{1} = 0.03\Omega \quad (6.38)$$

This suggests that for thin dielectrics, the impedance a propagating signal in a cavity sees is very low, typically much below 1 Ω.

In a short section of radial transmission line, we estimate the small amount of  $dL_{Loop}$  inductance from

$$dL_{Loop} = Z \times dTD = Z \times \frac{dR}{c} = Z \times \frac{dR}{c} \sqrt{Dk} \quad (6.39)$$

where

$dL_{Loop}$  = the small amount of loop inductance in a short length of a radial transmission line

$Z$  = the instantaneous impedance at the position  $R$

$dTD$  = the short-time delay of the section of radial transmission line

$dR$  = the length of the short section of radial transmission line

$c$  = speed of light in air

$Dk$  = the dielectric constant of the material in the cavity

Combining this with the relationship for the instantaneous impedance, we calculate the small amount of incremental loop inductance of a short length down the cavity as

$$dL_{Loop} = Z \times dTD = \frac{1}{2\pi c \epsilon_0 \sqrt{Dk}} \frac{h}{R} \times \frac{dR}{c} \sqrt{Dk} = \frac{h}{2\pi c^2 \epsilon_0} \times \frac{dR}{R} = \frac{\mu_0 h}{2\pi} \times \frac{dR}{R} \quad (6.40)$$

We calculate the spreading inductance for a circular cavity by integrating the incremental loop inductance as we move outward from some central contact region, where the current wavefront begins, to the cavity's outer edge. We get the spreading inductance with

$$L_{\text{spreading}} = \int_{R=R_{\text{via}}}^{R=R_{\text{cavity}}} dL_{\text{Loop}} = \int_{R=R_{\text{via}}}^{R=R_{\text{cavity}}} \frac{\mu_0}{2\pi} h \times \frac{dR}{R} = \frac{\mu_0}{2\pi} h \int_{R=R_{\text{via}}}^{R=R_{\text{cavity}}} \frac{dR}{R} \quad (6.41)$$

Performing the simple integral results in the spreading inductance from the via edge to the circular cavity edge as

$$L_{\text{spreading}} = \frac{\mu_0}{2\pi} \times h \times \ln\left(\frac{R_{\text{cavity}}}{R_{\text{via}}}\right) \quad (6.42)$$

Remarkably, this is the same relationship for the spreading inductance in the cavity as derived from the partial self-inductance of the via and from the via's coax model.

Whether we think of the cavity's inductance as a spreading inductance or as the via inductance, or the loop inductance of a section of coax, we calculate the same result. This is the spreading loop inductance the current wavefront sees in flowing between the top and bottom planes outward from the via contact point. The farther out the cavity it flows, the larger the total spreading loop inductance.

#### Tip

The spreading inductance from a point contact in a cavity depends as much on the radius of the contact region as it does on the board size. Even though the radius of the contact region is small, it strongly influences the total spreading inductance to the cavity's outer edge because it has the highest current density.

Some might find the concept of spreading inductance more intuitively satisfying than the partial self-

inductance of the via. For power integrity problems related to supplying core logic voltage rails, the important frequency range is usually far below the cavity modal resonant frequencies. By far, the most important property of the power plane cavity is the cavity spreading inductance. This is why thinking of cavities in terms of spreading inductance makes sense. For signal integrity and EMC/EMI, the cavity impedance is important, often in the GHz range. However, for core logic power integrity, thinking of cavities in terms of spreading inductance and sheet inductance is most efficient. This enables us to think in terms of squares of power/ground plane material.

Note that the spreading inductance is independent of the dielectric constant in the cavity. This is expected, because magnetic fields do not interact with dielectrics and inductance is independent of dielectric properties.

Using units of inches and ns, the spreading inductance between the two circular boundaries is

$$\begin{aligned} L_{\text{spreading}} &= \frac{1}{2\pi} \mu_0 \times h \times \ln\left(\frac{R_{\text{cavity}}}{R_{\text{via}}}\right) = \frac{1}{2\pi} 32 \text{nH/in} \times h \times \ln\left(\frac{R_{\text{cavity}}}{R_{\text{via}}}\right) \\ &= 5.1 \text{nH/in} \times h \times \ln\left(\frac{R_{\text{cavity}}}{R_{\text{via}}}\right) = 5.1 \text{pH/mil} \times h \times \ln\left(\frac{R_{\text{cavity}}}{R_{\text{via}}}\right) \end{aligned} \quad (6.43)$$

Describing the contact size and cavity dimensions in terms of diameters is often convenient. The ratio inside the natural log stays the same. The spreading inductance is

$$L_{\text{spreading}}[\text{pH}] = 5.1 \text{pH/mil} \times h[\text{mil}] \times \ln\left(\frac{D_{\text{cavity}}}{D_{\text{via}}}\right) \quad (6.44)$$

When the current wavefront starts from a contact region with a clearance hole diameter of 25 mils and the cavity is 1 inch in diameter and 1 mil thick, the

spreading inductance from the center boundary to the outer edge boundary is

$$L_{\text{spreading}}[\text{pH}] = 5.1 \frac{\text{pH}}{\text{mil}} \times h[\text{mil}] \times \ln\left(\frac{D_{\text{cavity}}}{D_{\text{via}}}\right) = 5.1 \frac{\text{pH}}{\text{mil}} \times 1 \text{ mil} \times \ln\left(\frac{1}{0.025}\right) = 18.8 \text{ pH} \quad (6.45)$$

The sheet inductance, as the loop inductance per square for a section of a cavity, is

$$L_{\text{sq}} = \mu_0 \times h = 32 \frac{\text{pH}}{\text{mil}} \times h \quad (6.46)$$

We relate the spreading inductance to the sheet inductance as

$$L_{\text{spreading}} = \frac{\mu_0}{2\pi} h \times \ln\left(\frac{D_{\text{cavity}}}{D_{\text{via}}}\right) = \frac{1}{2\pi} L_{\text{sq}} \times \ln\left(\frac{D_{\text{cavity}}}{D_{\text{via}}}\right) \quad (6.47)$$

This suggests a simple connection between the sheet inductance of a cavity and the spreading inductance between two circular, concentric boundaries. When the ratio of the cavity outside dimension to contact dimension is on the order of 500, the spreading inductance is about 1 square. This is the case when the clearance hole diameter of the contact via is on the order of 25 mils and the cavity dimension is on the order of 12 inches. Generally, the spreading inductance associated with one via is less than 1 square of sheet inductance.

**Tip**

The spreading inductance from a central contact point to the outer edge of a large cavity is approximately 1 square of sheet inductance of the cavity. For smaller boards, it is a fraction of a square of spreading inductance. Because of the log dependence on the geometry, spreading inductance varies slowly with cavity size.

## 6.7 EXTRACTING SPREADING INDUCTANCE FROM A 3D FIELD SOLVER

We can explore how reasonable this spreading inductance estimate is by comparing this result with the impedance calculated from a field solver. In most field solvers, especially full-wave, the output is S-parameters, from which we convert to impedances. We have to interpret these parameters in terms of the spreading inductance.

Once again, our approach is to model the cavity impedance as seen at a central contact point. However, this time there is no shorting wall at the cavity edge. We rely on displacement current through the plane capacitance to complete the current path. The capacitance is distributed throughout the plane. In the previous section, current traveled all the way to the cavity perimeter.

In this section, the spreading inductance is in series with the cavity's capacitance. This is only an approximation, because the cavity does not look like lumped LC elements; it looks like a radial transmission line with a non-uniform instantaneous impedance. We are only approximating it as a lumped circuit model. This lumped circuit model matches the real structure below frequencies where the physical length is  $1/20$  a wave. At higher frequency, the approximation gets worse. At low frequency, the voltage is constant across the whole plane and so the displacement current density through the plane capacitance is also constant.

#### Tip

At low frequencies where the cavity's lateral dimension is less than  $1/20$  of a wavelength, the cavity's impedance behaves approximately as a simple LC circuit. The L is the spreading inductance propagating out to the cavity's edge. The C is the cavity's capacitance.

For example, we estimate the spreading inductance

for a circular cavity with the following dimensions:

$D_{via} = 25$  mils (clearance hole diameter)

$D_{cavity} = 1$  inch

$h = 1$  mil

$Dk = 4$

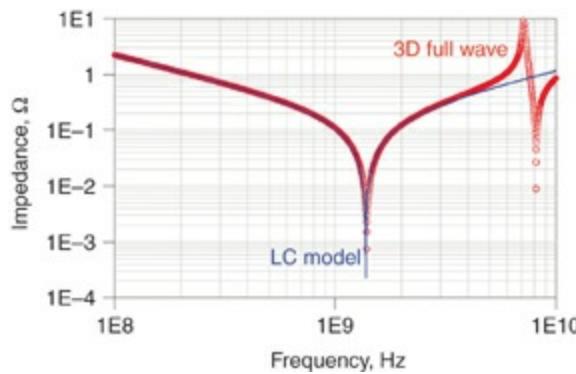
$$L_{spreading}[\text{pH}] = 5.1 \frac{\text{pH}}{\text{mil}} \times h[\text{mil}] \times \ln\left(\frac{D_{cavity}}{D_{via}}\right) = 5.1 \frac{\text{pH}}{\text{mil}} \times 1 \text{ mil} \times \ln\left(\frac{1}{0.025}\right) = 18.8 \text{ pH} \quad (6.48)$$

We approximate the parallel plate capacitance for this structure as

$$C = \epsilon_0 Dk \frac{A}{h} = 0.227 \frac{\text{pF}}{\text{in}} \times 4 \times \frac{\pi \times l^2}{4 \times 0.001} = 713 \text{ pF} \quad (6.49)$$

With an aspect ratio of 1 inch/1 mil = 1000, the parallel plate model is accurate to much better than 0.1%.

Figure 6.12 shows the impedance looking in from the central contact point simulated using a full-wave 3D field solver and simulated from a simple series LC model using these estimates.



**Figure 6.12** Simulated impedance looking into a 1-inch diameter cavity comparing the 3D full-wave calculation with a simple series LC model. Simulated with Mentor Graphics HyperLynx PI.

The agreement between the simple series LC model and the impedance from the full-wave field solver is remarkably good, up to a fraction of the cavity modal resonance at about 7 GHz. The cavity dimensions and

the materials inside determine this peak frequency. It is intrinsic to the overall cavity design and is independent of the via contact point.

The first dip in the impedance is not a structural cavity modal resonance, but is the interaction of the spreading inductance to the cavity's edge and the cavity's lumped capacitance. This frequency is not intrinsic to the cavity but changes depending on where we probe the cavity and the contact point's diameter.

**Tip**

The impedance dip looking into a plane is well approximated by the series LC resonance between the cavity capacitance and the spreading inductance from the single point of contact into the rest of the cavity. The high impedance peaks are due to the cavity modal resonances that depend on the dimensions of the cavity and material properties.

In general, the spreading inductance from a contact point to the rest of the cavity depends on the conductors' specific shape. We can only accurately evaluate it with a field solver. The excellent agreement in the last example between the calculated spreading inductance from the approximation and the 3D field solver was due to using a circular geometry in which the spreading inductance and capacitance model is an excellent approximation. Other geometries do not show such good agreement.

If we used a square geometry for the planes, the approximate spreading does not match the 3D field solver as closely. We simulated a square cavity with a 3D full-wave solver and compared it to an LC model. The central contact has a clearance hole diameter of 50 mils, the length of an edge is 5 inches and the dielectric thickness is 1 mil.

In this special geometry, we estimate the spreading inductance, based on a circular geometry with a

diameter equal to the length of a side, to be

$$L_{\text{spreading}}[\text{pH}] = 5.1 \frac{\text{pH}}{\text{mil}} \times h[\text{mil}] \times \ln\left(\frac{D_{\text{cavity}}}{D_{\text{via}}}\right) = 5.1 \frac{\text{pH}}{\text{mil}} \times 1 \text{ mil} \times \ln\left(\frac{5}{0.05}\right) = 24 \text{ pH} \quad (6.50)$$

The equivalent inductance in the 3D full-wave simulated impedance was 27.8 pH. This is still a very good approximation to the spreading inductance, given the fact that the cavity is square and not circular and we used the length of one side as the circle diameter.

## 6.8 LUMPED-CIRCUIT SERIES AND PARALLEL SELF-RESONANT FREQUENCY

At the lowest frequency, the impedance of a cavity looking in from a central point is related to the capacitance between the planes. At higher frequency, the cavity's impedance increases due to the spreading inductance from the observation point. The spreading inductance is in series with the cavity capacitance because current has to travel through the highest inductance near the contact to get to the highest capacitance that is near the cavity's perimeter. When they interact, they produce a series LC circuit with an impedance minimum.

This low impedance self-resonant frequency does not have the same physical origin as the higher frequency cavity modal resonances.

The impedance dip is due to the interactions between the lumped capacitance and lumped spreading inductance from the observation point looking outward. It occurs at a frequency that is less than a half-wave resonance and in the frequency regime where we still approximate the cavity's electrical properties as lumped circuit elements.

**Tip**

Although the cavity's electrical properties are always described by the solution of Maxwell's equations and the boundary conditions, which is what a 3D full-wave tool does, sometimes more insight comes from using a simpler model that connects electrical performance with physical features. This is why we view the impedance dip in terms of a series LC resonance.

Modeling the system as simple lumped LC elements and using the cavity capacitance and inductance, we estimate the series resonant frequency as

$$f_{\text{series}} = \frac{1}{2\pi\sqrt{C_{\text{cavity}}L_{\text{spreading}}}} \quad (6.51)$$

If we have a circular-shaped cavity with diameter D and central via contact point with contact diameter, d, the capacitance in the cavity using the parallel plate approximation is

$$C_{\text{cavity}} = \epsilon_0 D k \frac{A}{h} = \epsilon_0 D k \frac{\pi D^2}{4h} \quad (6.52)$$

The spreading inductance is

$$L_{\text{spreading}} = \frac{\mu_0}{2\pi} h \times \ln\left(\frac{D}{d}\right) \quad (6.53)$$

The series resonant frequency based on a simple series LC model is

$$\begin{aligned} f_{\text{res}} &= \frac{1}{2\pi\sqrt{L_{\text{spreading}}C_{\text{cavity}}}} = \frac{1}{2\pi\sqrt{\frac{\mu_0}{2\pi} h \ln\left(\frac{D}{d}\right) \times \epsilon_0 D k \frac{\pi D^2}{4h}}} \\ &= \frac{\sqrt{2}}{\pi} \frac{1}{D \sqrt{D k \mu_0 \epsilon_0} \sqrt{\ln\left(\frac{D}{d}\right)}} = \frac{\sqrt{2}}{\pi} \frac{c}{\sqrt{D k}} \frac{1}{D \sqrt{\ln\left(\frac{D}{d}\right)}} \end{aligned} \quad (6.54)$$

where

$f_{\text{res}}$  = the series resonant frequency

D = the diameter of the circular cavity

$d$  = the diameter of the contact point into the cavity

$Dk$  = the dielectric constant of the material in the cavity

$h$  = the dielectric spacing between the planes

$c$  = the speed of light in air

We can compare this series resonant dip with the frequency that corresponds to  $1/4$  a wavelength fitting across the diameter of the cavity. This corresponds to

$$f_{1/4\lambda} = \frac{c}{\lambda\sqrt{Dk}} = \frac{c}{4D\sqrt{Dk}} \quad (6.55)$$

We can substitute this term in the preceding relationship for the resonant frequency to obtain

$$f_{res} = \frac{\sqrt{2}}{\pi} \frac{c}{\sqrt{Dk}} \frac{1}{D\sqrt{\ln\left(\frac{D}{d}\right)}} = \frac{\sqrt{2}}{\pi} \frac{c}{4D\sqrt{Dk}} \frac{1}{\sqrt{\ln\left(\frac{D}{d}\right)}} = \frac{1.8}{\sqrt{\ln\left(\frac{D}{d}\right)}} f_{1/4\lambda} \quad (6.56)$$

When the cavity diameter is 1 inch, for example, and the via contact is 10 mils diameter, the LC series resonant frequency is

$$f_{res} = \frac{1.8}{\sqrt{\ln\left(\frac{D}{d}\right)}} f_{1/4\lambda} = \frac{1.8}{\sqrt{\ln\left(\frac{1}{0.01}\right)}} f_{1/4\lambda} = 0.84 \times f_{1/4\lambda} \quad (6.57)$$

When the cavity diameter is 5 inches, the coefficient becomes 0.72. Although the LC resonant frequency is close to the  $1/4$  wave cavity resonance, it is not the same, and depends on the contact diameter.

For the special case of FR4 material in the cavity and  $Dk = 4$ , the cavity diameter in inches, and via contact point in mils, the series resonant frequency is

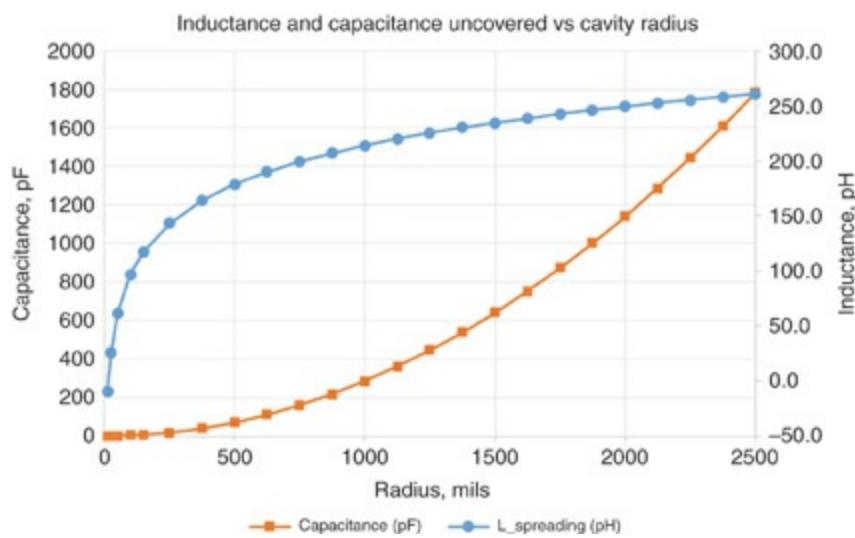
$$f_{res} = \frac{\sqrt{2}}{\pi} \frac{11.8}{\sqrt{4}} \frac{1}{D\sqrt{\ln\left(\frac{D[\text{inch}]}{d[\text{mils}]}\right)}} = \frac{2.66}{D\sqrt{\ln\left(\frac{D[\text{inch}]}{d[\text{mils}]}\right)}} \text{GHz} \quad (6.58)$$

For example, if the cavity diameter is 5 inches and the central contact point is 10 mils in diameter, the resonant frequency is

$$f_{\text{res}} = \frac{2.66}{D \sqrt{\ln\left(\frac{D[\text{inch}]}{d[\text{mils}]\}}\right)}} \text{GHz} = \frac{2.66}{5 \sqrt{\ln\left(\frac{5}{0.01}\right)}} \text{GHz} = 0.213 \text{ GHz} \quad (6.59)$$

There is an important reason why the simple lumped series LC model predicted the cavity's impedance profile so well. Most of the spreading inductance is associated with a small radius and is located near the via. Most of the capacitance is associated with the full cavity radius and is located near the plane's edge.

This principle is illustrated in [Figure 6.13](#), which shows the inductance and capacitance uncovered as a function of radius as a wavefront propagates out from the via. More than half the inductance (55%) is located within the first 250 mils but only 1% of the capacitance is located there. We need to get to 1750 mils radius to uncover 50% of the capacitance but approximately 93% of the inductance has already been uncovered by then. Current must pass through most of the inductance before it can feed the capacitance. This looks like a series LC circuit. These concepts explain why the lumped LC model is successful at predicting the first impedance dip.



**Figure 6.13** The contributions to the cavity capacitance and spreading inductance as we move outward from the center of the via contact. Note that most of the inductance arises near the contact point, whereas most of the capacitance is far away from the contact point. This makes the cavity look like a series LC circuit.

As another example of the power of this simple LC model in predicting a cavity's impedance profile when driven from central contact points, [Figure 6.14](#) shows the impedance profile simulated with a 3D full-wave tool for the special case of

$$D_{\text{cavity}} = 5 \text{ inches} \text{ (diameter of the circular cavity)}$$

$$h = 10 \text{ mils} \text{ (thickness between the planes)}$$

$$Dk = 4 \text{ (dielectric constant of the filler between the planes of the cavity)}$$

$$D_{\text{via}} = 30 \text{ mils} \text{ (contact diameter of contact point into the cavity)}$$

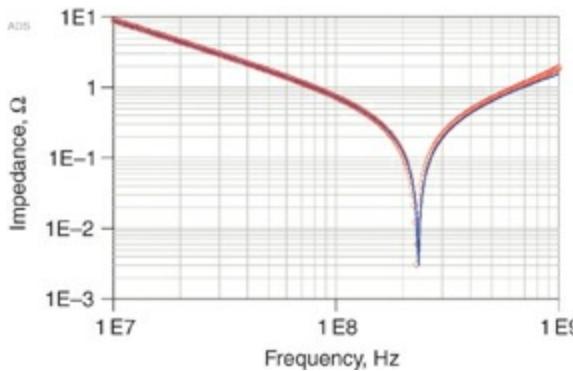
We calculate the cavity capacitance as

$$C = \epsilon_0 Dk \frac{A}{h} = 0.227 \frac{\text{pF}}{\text{in}^2} \times 4 \times \frac{\left(\frac{\pi}{4}\right)5^2}{0.01} = 1783 \text{ pF} = 1.78 \text{ nF} \quad (6.60)$$

We calculate the spreading inductance from the center point to the outer radius as

$$L_{\text{spreading}}[\text{pH}] = 5.1 \frac{\text{pH}}{\text{mil}} \times h[\text{mil}] \times \ln\left(\frac{D_{\text{cavity}}}{D_{\text{via}}}\right) = 5.1 \times 10 \times \ln\left(\frac{5}{0.03}\right) = 261 \text{ pH} \quad (6.61)$$

Superimposed on the impedance profile calculated with the 3D field solver is the impedance calculated with the series LC model using these values of L and C. The agreement is very good.

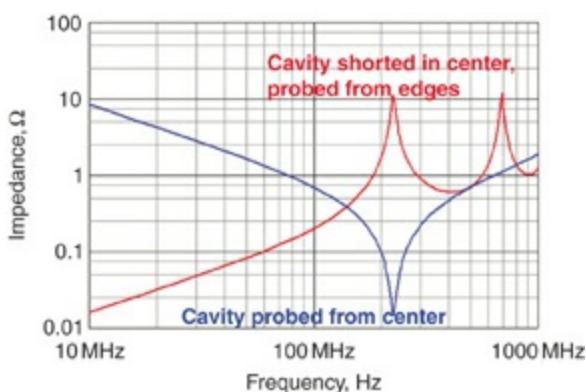


**Figure 6.14** Impedance profiles of a 5-inch diameter cavity 10 mils thick, calculated using a 3D field solver (circles) and with a simple LC model and approximation (solid line). The agreement is very good.

We simulate this impedance profile by driving the otherwise open cavity from the center contacting the top plane and using a via contact to the bottom plane. The spreading inductance is in series with the capacitance between the two planes.

We can construct a similar structure, but using a shorting via in the cavity's center and probing from the edge. In this structure, the planes are shorted together so their low-frequency impedance is determined by the spreading inductance of the cavity to the shorting via in the center. In parallel with the shorting via is the cavity capacitance. These two structures create a parallel resonance, resulting in an impedance peak.

Because the cavity capacitance and cavity spreading inductance are the same in both cases, we expect the series resonant frequency and parallel resonant frequencies to be the same. [Figure 6.15](#) shows the simulated series and parallel resonances of the same cavity. The two LC resonant frequencies are the same, as expected.



**Figure 6.15** Simulated impedance profile of the same cavity probed from the center showing the series LC resonance and then shorted at the center and probed from the two edges showing the parallel LC resonance.

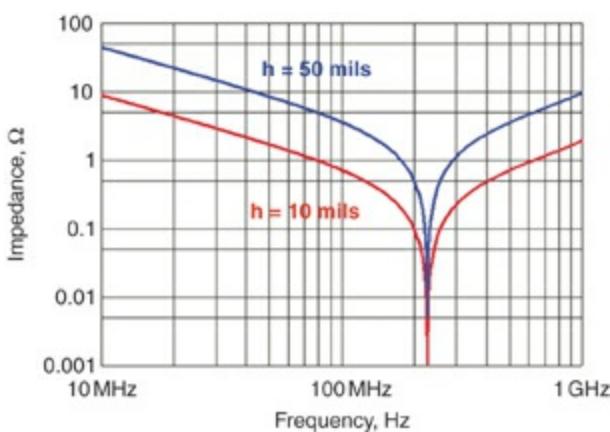
Simulated with Mentor Graphics HyperLynx PI.

## 6.9 EXPLORING THE FEATURES OF THE SERIES LC RESONANCE

Because of the very good agreement between the lumped circuit LC cavity model and the 3D full-wave simulation, we use this simple analytical model to explore some of the cavity features.

The cavity's self-resonant frequency is independent of the cavity's dielectric thickness. As the cavity spacing decreases, the capacitance increases but the inductance decreases. Because  $h$  is first order in both terms,  $h$  cancels out in the product and the resonant frequency is independent of dielectric thickness.

In Figure 6.16 shows the impedance of a cavity simulated using a 3D field solver for two different thicknesses, 10 mils to 50 mils. For the thicker cavity, the impedance of the cavity's capacitance decreased but the impedance of the higher spreading inductance increased. The product stayed the same and the resonant frequency stayed the same.



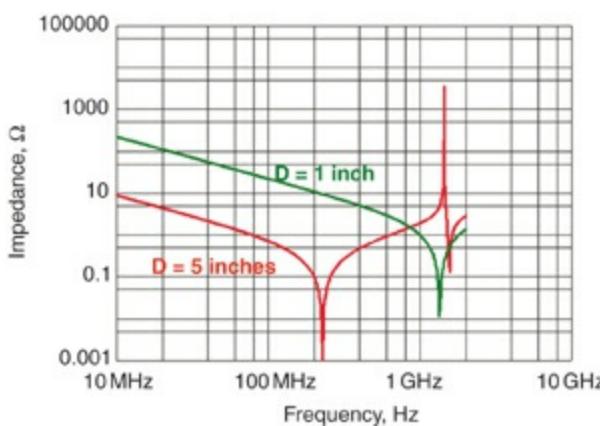
**Figure 6.16** Simulated impedance profile of a circular cavity 5 inches in diameter with thicknesses of 10 mils and 50 mils, filled with FR4, probed at the center with a contact diameter of 10 mils. Note the resonant frequencies are the same for different values of  $h$ . Simulated with Mentor Graphics HyperLynx PI.

**Tip**

The self-resonant frequency of a cavity, where the impedance is a minimum, is independent of the cavity thickness. It depends on the cavity's size and to a much less extent, the contact point's size.

The resonant frequency also increases as the cavity's diameter decreases. This is slightly faster than inversely with the cavity's diameter. A factor of five reduction in cavity diameter is slightly more than a factor of five increase in resonant frequency.

Figure 6.17 shows the impedance profile calculated with a 3D field solver for a diameter of 5 inches, and 1 inch, a  $5\times$  decrease. The analytical approximation predicted resonant frequencies of 0.213 GHz and 1.24 GHz, a  $5.8\times$  increase. The 3D field solver calculated resonant frequencies of 0.226 GHz and 1.34 GHz, a  $5.9\times$  increase. The analytical approach offers a good approximation to the spreading inductance in a cavity.



**Figure 6.17** Impedance profile of a 1-inch and 5-inch diameter cavity, each 10 mils thick. Note that the resonant frequency scales a little faster than inversely with the cavity diameter. Simulated with Mentor Graphics HyperLynx PI.

We can further approximate where we expect to find the cavity's series resonant frequency, when we probe it from the center. If we assume that the ratio of the cavity diameter to the contact diameter is on the order of 500, corresponding to a cavity 5 inches on a side and 10 mil diameter contact, the series resonant frequency is approximately

$$f_{\text{res}} = \frac{2.66 \text{ GHz}}{D[\text{inch}] \sqrt{\ln\left(\frac{D[\text{inch}]}{d[\text{inch}]\right)}}} \sim \frac{2.66 \text{ GHz}}{D[\text{inch}] \sqrt{\ln(500)}} = \frac{2.66 \text{ GHz}}{D[\text{inch}] \times 2.5} \sim \frac{1 \text{ GHz}}{D[\text{inches}]} \quad (6.62)$$

where

$f_{\text{res}}$  = the series resonance frequency of the impedance dip in a cavity

D = the diameter of the cavity in inches

d = the diameter of the contact point being probed in inches

In the preceding examples, for the case of a cavity diameter of 1 inch and 5 inches, the 3D field solver simulated series resonances at 1.34 GHz and 0.226 GHz. Our simple estimate predicts 1 GHz and 0.2 GHz. It is a reasonable first-order estimate.

**Tip**

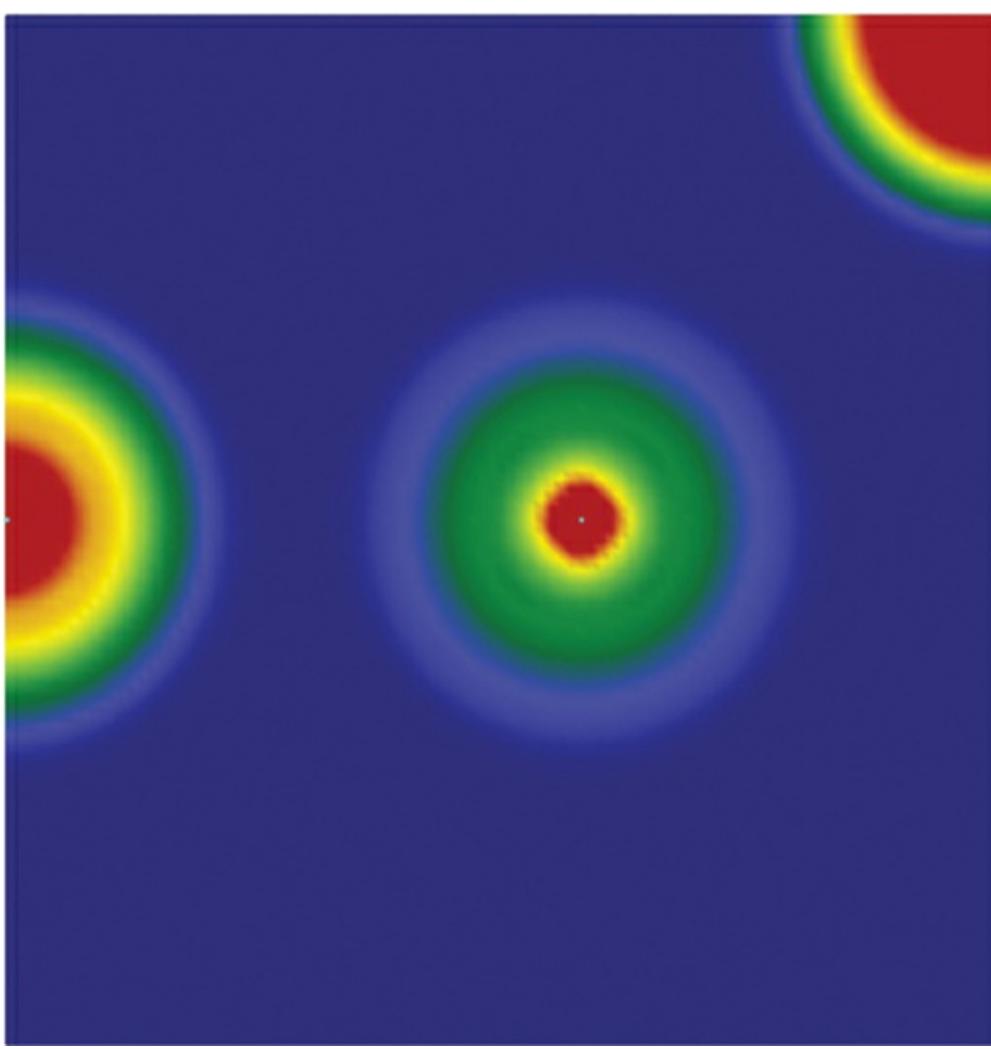
As a simple estimate, we expect the series resonance of a cavity, driven in the center, to occur at about 1 GHz/(cavity diameter in inches).

## 6.10 SPREADING INDUCTANCE AND SOURCE CONTACT LOCATION

Spreading inductance is fundamentally about how much inductance the current wavefront sees in the cavity while it spreads out from a small point. If the plane shape forces the current density to be higher, the spreading inductance is higher.

For example, if a contact point is near the board edge or corner, the current does not spread in all directions, but only into the available region of the cavity. The proximity of the plane edge “crowds” the current, forcing a higher current density and a higher spreading inductance.

Figure 6.18 shows the simulated current density in the top conductor of a cavity for three contact positions: at the board’s center, an edge, and a corner. Given these current densities, we expect the spreading inductance looking outward from the contact point to be lowest for the central point and highest for the corner.



**Figure 6.18** Current density in the top and bottom conductor of a thin cavity near three contact points. This is the initial current distribution about 0.2 ns after launch. Red means higher current density. Simulated with Mentor Graphics HyperLynx PI.

In the current density plots in [Figure 6.18](#), the highest current density is in the center of the contact region. When the contact point is near an edge, the current crowding effect forces a higher current density for a longer path length, increasing the spreading inductance.

The spreading inductance from the cavity's center is composed of four quadrants of spreading current in parallel. When we restrict the current to flow in only two of the quadrants, as when the contact point is located at an edge, only half of the plane is available for current flow and we expect twice as much spreading inductance as from the center. When the contact point

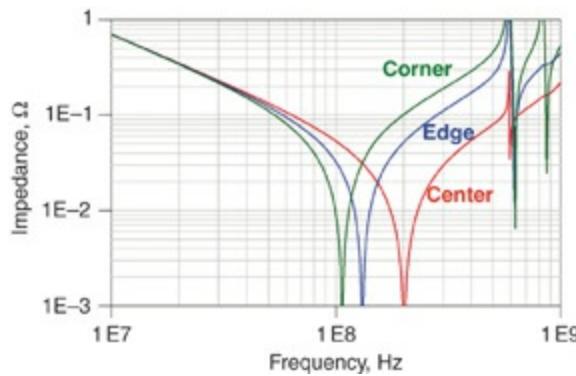
is in a corner, the spreading inductance has contribution from just one quadrant. We expect it to be higher by a factor of four compared with the center. A 3D simulation verifies these simple conclusions.

Figure 6.19 shows the impedances looking into the cavity from center, edge, and corner. From the series resonant frequencies, we estimate the spreading inductance from the edge is about two times larger than from the center and the spreading inductance from the corner is four times larger than from the center.

The higher spreading inductance lowers the series resonant frequency. The same cavity is being observed from each of the three locations but the contact position in the cavity affects the series resonant frequency. This example further illustrates that the first impedance dip is not a structural modal resonance but a lumped LC resonance.

**Tip**

The cavity's series resonant frequency depends on where we probe the cavity.



**Figure 6.19** Impedance looking from three locations into a cavity showing the same capacitance but higher inductance when the current is more constricted. Note the intrinsic cavity modal resonances, starting at about 600 MHz, are independent of where the cavity is probed.

Simulated with Mentor Graphics HyperLynx PI.

The low-frequency self-impedance of the cavity,

where it looks like a capacitor, is independent of where we probe the cavity. Every point is equivalent on the cavity. The probed impedance varies over the surface when the spreading inductance plays a role. Cavity's modal resonances exist at higher frequency. The impedance at any specific location depends strongly on the details of the modes excited at each specific frequency.

**Tip**

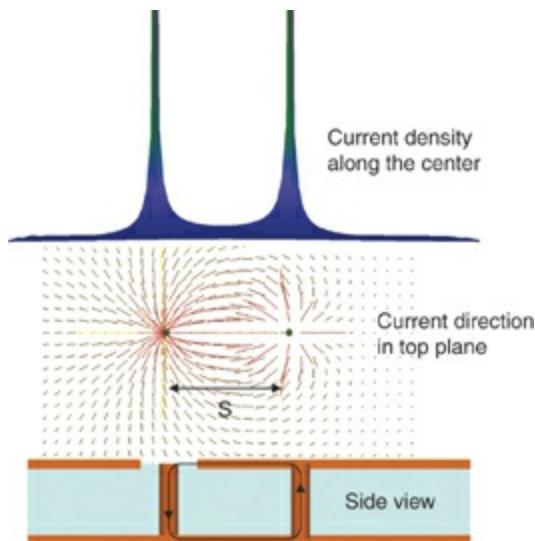
At low frequency, when the cavity looks like a capacitor, the impedance of a cavity is independent of where we probe it. When spreading inductance influences the impedance, the observation point influences the cavity's impedance. Above the series resonant frequency, it is ambiguous to refer to the "impedance of the cavity." It is not unique, and varies over the surface of the cavity.

## 6.11 SPREADING INDUCTANCE BETWEEN TWO CONTACT POINTS

So far, we have looked at the spreading inductance from one contact point into the cavity, as if the current were traveling radially outward. This is the minimum series inductance any current sees as it spreads outward from one contact point. Any other current distribution only increases the spreading inductance above this amount. We saw that when current launches from the board, the spreading inductance is two times higher than from the center. Current launched from the corner results in spreading inductance four times higher than from the center.

When the current flows between two contact points, as, for example, from a single capacitor and a single power and ground via pair in a package, the spreading inductance between these points in the cavity is higher than from a single contact point into the entire cavity. The current density is very high near the contacts.

Where current density is high, the contribution to spreading inductance is high. [Figure 6.20](#) shows the simulated current density in the top layer of a cavity when current flows from point to point, for example, a decoupling capacitor to the vias to a BGA.



**Figure 6.20** Current density in the top conductor of a cavity along a line between two contact points in a cavity. Note the high current density near the contact points to the cavity. From the low-frequency impedance looking into one contact, with the other one shorting the planes, we can extract the spreading inductance.  
Simulated with Mentor Graphics HyperLynx PI.

We expect the spreading inductance in the cavity between these two contact points to be more dependent on the features of the vias than the spacing between them. If we increase the spacing between the via contact points, the spreading inductance increases, but not by much. Because the current distribution is so non-uniform, we can only calculate the spreading inductance with a 3D field solver. Using a full-wave 3D field solver that calculates the current distribution, we explore design space and identify a few important trends and a rough approximation for the spreading inductance between two contact points.

When we measure the impedance looking into the cavity with another point in the cavity shorting the two

planes, we see the impedance of the spreading inductance between these two contact points at low frequency. The impedance looking into the cavity looks like an inductor. For this example, the cavity is 10 inches on a side and 10 mils thick. The two contact points are located along the plane's center and their spacing is increased.

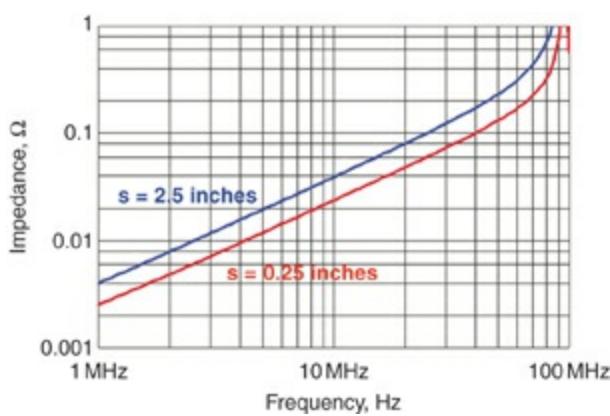
For this cavity size, we expect the quasi-static model to apply, where we can model the spreading inductance in the cavity as a simple lumped inductor at frequencies below

$$f[\text{GHz}] < \frac{1}{20} \times \frac{6 \text{ GHz}}{\text{Len}[\text{inch}]} = \frac{0.3}{10} = 0.03 \text{ GHz} = 30 \text{ MHz} \quad (6.63)$$

**Tip**

At low frequency, the impedance between two pairs of contact points in a cavity is approximately a single loop inductance. However, because the “static” current distribution is so non-uniform, we can only calculate this loop inductance accurately with a 3D field solver that solves for the specific current density.

Figure 6.21 shows an example of the 3D field solver calculated impedance for two different center-to-center separations of 0.25 inches and 2.5 inches. We see the impedance profile matches an inductor well up to about 60 MHz, close to our estimate for 1/20 of a wavelength. Because the impedance profile looks like an inductor, we use the impedance at 1 MHz to extract the loop inductance between these two points that is a direct measure of the spreading inductance.



**Figure 6.21** Impedance looking into one pair of via contacts while the other pair shorts the cavity. The cavity is 10 inches on a side with 10 mil thick spacing between the planes. Simulated with Mentor Graphics HyperLynx PI.

In this example, the impedance at 1 MHz for the two different spacings is 2.55 mΩ and 4.0 mΩ. This results in a spreading inductance of this cavity for the two spacings of

$$L[nH](s=0.25) = \frac{1}{2\pi} \frac{1}{1MHz} Z_{1MHz} = 159 \times 2.5 \text{ m}\Omega = 398 \text{ pH} \quad (6.64)$$

$$L[nH](s=2.5) = 159 \times 4.0 \text{ m}\Omega = 636 \text{ pH}$$

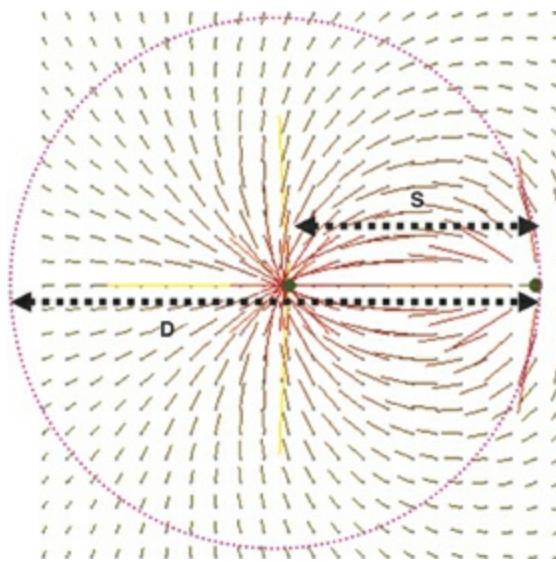
Two important observations become clear. In this cavity, with a thickness of 10 mils, the sheet inductance is  $32 \text{ pH/mil} \times 10 \text{ mils} = 320 \text{ pH/sq}$ . The spreading inductance between these two vias for both separations is approximately two squares of sheet inductance.

Secondly, even though we increased the spacing between the two contact points by ten times, the spreading inductance between these points increased by less than two times. As expected, although the spreading inductance between a pair of via contacts into a cavity does increase with separation, it is a soft dependence and does not increase anywhere close to linearly with separation distance.

**Tip**

The spreading inductance between two points in a cavity is approximately two squares of sheet inductance. The loop inductance increases very slowly, with the natural log of the separation between the two points.

Our goal is to develop a simple approximation for the spreading inductance between two contact points. This approximation would identify the important parameters and allow us to explore design space with a spreadsheet. However, because the current distribution is very non-uniform, analytically deriving the spreading inductance in terms of the geometry features is difficult. We can guess the form of this approximation by observing the current distribution between two points in a large cavity, calculated with a 3D field solver, as shown in [Figure 6.22](#).



**Figure 6.22** The current distribution between two contact points separated a distance,  $s$ , in a large cavity.

Most of the current has dropped to nothing outside a region around one of the contact points, with a diameter  $D$ , equivalent to about two times the point-to-point spacing.

The current distribution initially spreads out radially from one contact point and then concentrates down as it approaches the other contact point. Beyond this

distance, there is little current flow in the cavity. The spreading inductance for radial current in spreading out from a single contact point with diameter  $d$  to a limit of radius  $s$  beyond which the current density falls off is

$$L_{\text{point-cavity}} = \frac{1}{2\pi} L_{\text{sq}} \times \ln\left(\frac{2s}{d}\right) \quad (6.65)$$

In addition to the spreading inductance from this radial current, there is spreading inductance due to the concentration of the current as it nears the other contact point. This increases the point-to-point spreading inductance above the radial contribution alone.

We expect the point-to-point spreading inductance to be one to three times the single point spreading inductance and of the form

$$L_{\text{point-point}} = k \times L_{\text{point-cavity}} = k \times \frac{1}{2\pi} L_{\text{sq}} \times \ln\left(\frac{2s}{d}\right) \quad (6.66)$$

where

$L_{\text{point-cavity}}$  = the spreading inductance between one contact point into the cavity to a fixed radius  $s$

$L_{\text{point-point}}$  = the spreading inductance between two contact points, spaced a distance  $s$  in a cavity

$k$  = an empirically derived scaling term roughly between 1 and 3

$L_{\text{sq}}$  = the sheet inductance in the cavity =  $32 \text{ pH/mil} \times h$

$h$  = spacing between the planes in the cavity

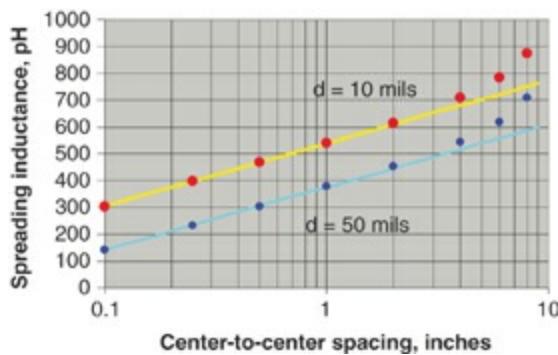
$s$  = center-to-center spacing between the contact points

$d$  = the diameter of the contact via

$D$  = the diameter of the region of the cavity centered at one contact point in which there is significant current in the cavity, with  $D = 2 \times s$

The scaling term  $k$  is a measure of how much more spreading inductance there is between the two via contacts than the spreading inductance between the center contact to the edge of the significant current distribution region. This region has a radius about the contact point equivalent to the spacing to the second contact point.

Using a 3D field solver as a virtual prototype tool, we explore how the spreading inductance varies with separation for two different pairs of identical via contact diameters,  $d = 10$  mils and  $d = 50$  mils. We compare the field solver and simple empirical model to find the value of  $k$ . Figure 6.23 shows the simulated spreading inductance as the two contact points pull apart and the estimate from this simple model, using a value of  $k = 2$ . The higher spreading inductance example is for a pair with  $d = 10$  mil diameter and the lower spreading inductance example is for the case of  $d = 50$  mils contact diameter. The circles are the spreading inductances calculated with a 3D field solver. The lines are calculated using the approximation of Equation 6.66 with  $k = 2$ .



**Figure 6.23** Spreading inductance as the center-to-center spacing between two via contacts increases for two different contact diameters. Simulated with Mentor Graphics HyperLynx PI.

**Tip**

It is remarkable that the calculated spreading inductance between two contact points in a cavity, calculated with a 3D field solver, shows a log dependence on center-to-center spacing. As one or both contact points approaches a cavity edge, the current is further constricted and the loop inductance increases by an additional factor.

It is of interest to note that when the spacing becomes comparable to the length of a side of the planes, the spreading inductance increases faster than when the contacts are close together. This is due to the current crowding as the contact points approach the edge of the planes and the current is compressed, increasing the spreading inductance.

The value of the scaling term,  $k = 2$ , that gives such a good fit to the model suggests that the spreading inductance between two points is equivalent to twice the spreading inductance of one of those points to the cavity's outer edge if the second point were on the cavity's circumference. The point-to-point spreading inductance is double the cavity spreading inductance.

Based on the very good fit to the empirical approximation, the spreading inductance between two points is

$$L_{\text{point-point}} = 2 \times \frac{1}{2\pi} L_{\text{sq}} \times \ln\left(\frac{2s}{d}\right) = \frac{1}{\pi} \times 32 \text{ pH/mil} \times h \times \ln\left(\frac{2s}{d}\right) = 10.2 \text{ pH/mil} \times h \times \ln\left(\frac{2s}{d}\right) \quad (6.67)$$

where

$L_{\text{point-point}}$  = the spreading inductance between two contact points in a cavity, in pH

$s$  = the distance between the two contact locations, in mils

$d$  = the diameter of the contact points to the cavity, in mils

$h$  = the separation between the two planes that makes

up the cavity, in mils

For example, if the cavity is 10 mils thick and the via contact points have a contact diameter of 10 mils and are spaced 1 inch apart, the spreading inductance between them is about

$$L_{\text{point-point}} = 10.2 \frac{\text{pH}}{\text{mil}} \times h \times \ln\left(\frac{2s}{d}\right) = 10.2 \frac{\text{pH}}{\text{mil}} \times 10 \times \ln\left(\frac{2000}{10}\right) = 540 \text{ pH} \quad (6.68)$$

This relationship derived for the point-to-point spreading inductance in a cavity illustrates the three features that influence the spreading inductance in the cavity between two components:

- Thickness of the cavity
- Spacing between the points
- Diameter of the contact points

The first order, most important term influencing the spreading inductance is the thickness of the cavity.

The spacing between the contact points also affects the via-to-via spreading inductance. Bring the vias closer together and the spreading inductance decreases, as expected. However, the spacing only slowly affects the spreading inductance, as the natural log of the spacing. Closer is better, but not dramatically.

The contact diameter is also important. The larger the contact area, the lower the spreading inductance, but it is softly dependent on the natural log of the diameter. This relationship suggests the contact area into the cavity is just as important as the spacing between contact points. This is a good reason why multiple vias to a capacitor pad are important. It is only partly to decrease the via loop inductance. Multiple vias also increase the effective contact diameter for the current to spread out in the cavity, reducing the cavity spreading

inductance.

**Tip**

Spreading inductance between two contact points in a cavity, such as between a capacitor and the balls of a BGA, scales to first order with the thickness between the planes. It decreases with closer spacing, but softly. The larger the contact area to the cavity, the more the current spreads out initially in the cavity and the lower the point-to-point spreading inductance.

## 6.12 THE INTERACTIONS OF A CAPACITOR AND CAVITIES

We often model a real capacitor with a series RLC circuit. The self-resonance frequency, SRF, where the impedance is a minimum, depends on the mounting inductance of the capacitor and the capacitance, given that

$$f_{\text{SRF}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{mount}} C_{\text{capacitor}}}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{mount}} [\text{nH}] \times C_{\text{capacitor}} [\text{nF}]}} \quad (6.69)$$

With a mounting inductance approximately 2 nH and a typical capacitor value of 100 nF, the SRF is on the order of 10 MHz or lower.

Below the SRF, the capacitor's impedance behaves like an ideal capacitor. Above the SRF, the capacitor's impedance behaves like an inductor. When we connect a real capacitor between the planes of a cavity, the cavity's impedance sees the capacitor's impedance in parallel.

At low frequency, the cavity's capacitance and the capacitor's capacitance adds. At high frequency, the impedance of the capacitor is high due to the mounting inductance and has no impact when shorting across the cavity's planes. However, in the intermediate frequency range a new behavior emerges between the self-resonant frequencies of the capacitor and the cavity. This is due to the parallel circuit combination of the inductance of the real capacitor and the cavity

capacitance.

**Tip**

At the frequency where the impedance of the capacitor's inductance matches the impedance of the cavity's capacitance, we get a peak in impedance from the parallel resonance of the capacitor's inductance and the cavity's capacitance.

Figure 6.24 shows an example of the simulated impedance of just the cavity by itself, the series RLC model of a capacitor with  $L = 2 \text{ nH}$ ,  $C = 100 \text{ nF}$ , and  $R = 25 \text{ m}\Omega$ , and the combination of these two circuit elements.

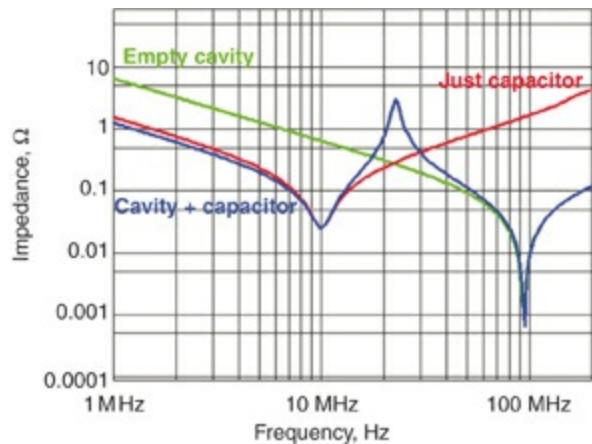


Figure 6.24 Impedance profile of just the capacitor and cavity and their combination, simulated with Mentor Graphics HyperLynx PI.

Mounting a capacitor to a cavity creates a parallel circuit, and the impedance profile shows a peak at the parallel resonant frequency. This frequency is related to the cavity capacitance and mounting inductance as

$$f_{\text{PRF}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{mount}} C_{\text{cavity}}}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{mount}} [\text{nH}] \times C_{\text{cavity}} [\text{nF}]}} \quad (6.70)$$

When the capacitor interacts with the cavity, in addition to the mounting inductance of the capacitor to the cavity, a spreading inductance is also associated with the capacitor contact to the cavity. The sum of the capacitor inductance, via mounting inductance, and

power plane spreading inductance is included in the impedance dip for the mounted capacitor at about 10 MHz.

When the spreading inductance is comparable to the mounting inductance, the location of the capacitor in the cavity influences the capacitor's effective inductance. When the spreading inductance is small, compared to the mounting inductance, the spreading inductance does not influence the total inductance and location is not important.

**Tip**

When the spreading inductance is small compared to the capacitor's mounting inductance, the location of the capacitor is not important.

The impedance dip at about 100 MHz is due to the spreading inductance of the measurement port interacting with the power plane capacitance. The presence of the mounted discrete capacitor does not significantly influence the dip.

## 6.13 THE ROLE OF SPREADING INDUCTANCE: WHEN DOES CAPACITOR LOCATION MATTER?

When there is just one capacitor and one observation point on the cavity, the equivalent inductance of the capacitor we see at the observation point is the series combination of the capacitor's mounting inductance and the spreading inductance to the capacitor.

$$L_{\text{total}} = L_{\text{mounting}} + L_{\text{spreading}} \quad (6.71)$$

Two important extreme conditions to consider are

- **Case 1:**  $L_{\text{mounting}} \gg L_{\text{spreading}}$  and the cavity is transparent and location is *not important*.
- **Case 2:**  $L_{\text{spreading}} \gg L_{\text{mounting}}$  and the cavity is not

transparent and location *is important*.

In case 1, the capacitor's mounting inductance is large and the spreading inductance is small. A large mounting inductance results if long, narrow surface traces exist from the capacitor to the vias connecting it into the cavity or the cavity is far below the capacitor. A small spreading inductance is the case if the dielectric in the cavity is very thin. In this regime, changing the location of the capacitor might change the spreading inductance but has a relatively small impact on the capacitor's total inductance. We refer to this condition as the cavity being transparent.

**Tip**

In case 1, the capacitor location is not important. Moving it anywhere over the board, compared to the observation point, has little impact on the total loop inductance between the capacitor and observation point.

The location of the capacitor is not important for impedance if the spreading inductance is very small compared to the mounting inductance. As demonstrated in [Equation 6.68](#), the spreading inductance between two points in a cavity is approximately

$$L_{\text{spreading}} = 10.2 \frac{\text{pH}}{\text{mil}} \times h \times \ln\left(\frac{2s}{d}\right) \quad (6.72)$$

where

$L_{\text{spreading}}$  = the spreading inductance between two contact points in a cavity, in pH

$s$  = the distance between the two contact locations, in mils

$d$  = the diameter of the contact points to the cavity, in mils

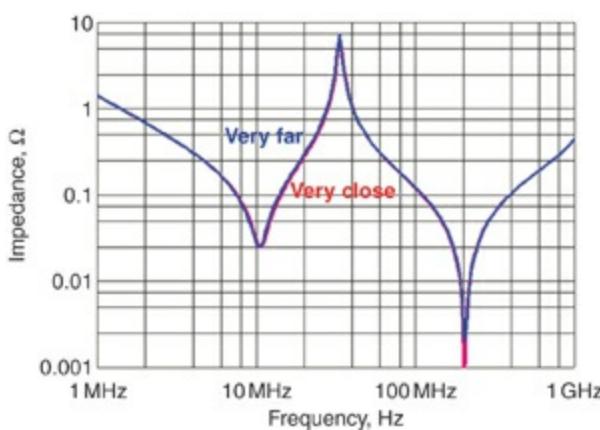
$h$  = the separation between the two planes that makes

up the cavity, in mils

In a typical case of  $s = 1$  inch and  $d = 10$  mils, the natural log term is only 5.3. This results in a spreading inductance between the two contact points of about 54 pH/mil  $\times$  h. This is equivalent to about two squares of sheet inductance. If the cavity is very thin, such as 2 mils, the spreading inductance between the capacitor and the observation point is only

$$L_{\text{spreading}} = 10.2 \frac{\text{pH}}{\text{mil}} \times h \times \ln\left(\frac{2s}{d}\right) = 10.2 \frac{\text{pH}}{\text{mil}} \times 2 \times \ln\left(\frac{2 \times 1}{0.01}\right) = 108 \text{ pH} \quad (6.73)$$

A typical mounting inductance for a capacitor on a large server board might be approximately 2 nH. This says the capacitor's position, compared to the observation point, is not important. As we move the capacitor around the cavity, the cavity is transparent and has no impact on the resulting capacitor impedance when it is mounted to the cavity. Figure 6.25 shows the impedance at a central observation point in the cavity with a 2 nH mounting inductance capacitor positioned very far and very close to the observation point. As we move the capacitor around the cavity, the capacitor's impedance is independent of position. The impedances at the two locations are indistinguishable. The cavity is transparent.



**Figure 6.25** Impedance profile from the same observation point with a capacitor having  $ESL = 2 \text{ nH}$ , positioned very far and very close to the observation point. The cavity has a dielectric thickness of 2 mils.

Simulated with Mentor Graphics HyperLynx PI.

**Tip**

When the spreading inductance is small and the mounting inductance is large, the cavity is transparent and capacitor position is not important. This is typically the case for cavities with very thin dielectric.

In case 2, the spreading inductance is large compared to the mounting inductance. Changes in the location, which affect the spreading inductance, affects the cavity's impedance. Location is important and the cavity is not transparent.

For example, if the dielectric thickness is 20 mils, we derive the spreading inductance between two points with

$$L_{\text{spreading}} = 10.2 \frac{\text{pH}}{\text{mil}} \times h \times \ln\left(\frac{2s}{d}\right) = 10.2 \frac{\text{pH}}{\text{mil}} \times 20 \text{ mil} \times \ln\left(\frac{2s}{d}\right) = 204 \text{ pH} \times \ln\left(\frac{2s}{d}\right) \quad (6.74)$$

When the contact via at the observation point is 10 mil diameter and the capacitor is 2 inches away, the spreading inductance contribution is

$$L_{\text{spreading}} = 204 \text{ pH} \times \ln\left(\frac{4000}{10}\right) = 204 \text{ pH} \times 5.99 = 1.22 \text{ nH} \quad (6.75)$$

If we bring the capacitor very close so it is only 0.2

inches from the contact location, the spreading inductance is

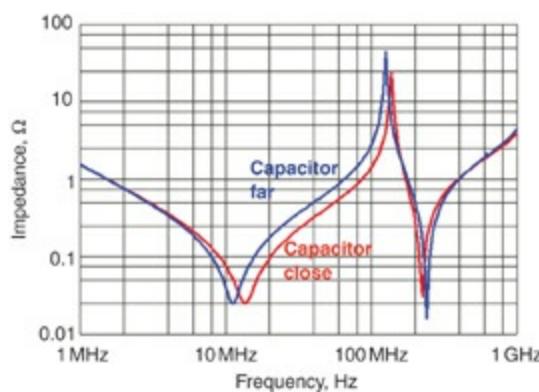
$$L_{\text{spreading}} = 204 \text{ pH} \times \ln\left(\frac{400}{10}\right) = 204 \text{ pH} \times 3.7 = 0.75 \text{ nH} \quad (6.76)$$

Some might be surprised that even though we moved the capacitor closer from 2 inches distant to 0.2 inches away, the spreading inductance, due to the natural log dependence, only decreased from 1.22 nH to 0.75 nH. Even in this extreme case, although closer is better, it's not a huge factor. Only when there is no cost premium to move the capacitor's location closer to the BGA is it worth it.

**Tip**

Even though not a big advantage exists for moving a capacitor closer to the package, if it is free, closer is always better. When it costs more due to important real estate near the package, we must evaluate the "bang for the buck" using analysis.

The capacitors' location only significantly affects its impedance profile when the capacitor's spreading inductance is significant compared to its mounting inductance. In the mobile computing industry where via in pad, small pads, and a cavity close to the top surface of the board is common, the mounting inductance is often well below 0.5 nH. In this case, moving the capacitor closer to the BGA has a noticeable effect on its impedance. A 3D field solver allows us to calculate the impact on the capacitor's inductance seen at a central observation point. This example is shown in [Figure 6.26](#).



**Figure 6.26** Impedance looking into a thick cavity with one capacitor mounted far from and close to the observation point. In this case, the spreading inductance in the cavity is large and the cavity is not transparent.  
Simulated with Mentor Graphics HyperLynx PI.

**Tip**

The spreading inductance compared to the capacitor's mounting inductance is the most important metric for quick evaluation of cavity transparency.

The condition for the cavity's being transparent or not depends on how the mounting inductance compares to the spreading inductance. We estimate a useful figure of merit for the spreading inductance between a contact point and a capacitor from the two sets of dimensions associated with [Equations 6.74](#), [6.75](#), and [6.76](#), and a separation of 2 inches and 0.2 inches. Because of the soft dependence of the natural log terms of 5.99 and 3.7, we use a rough intermediate value of 4. A rough figure of merit for the spreading inductance between a BGA and a capacitor is approximately

$$L_{\text{spreading}} = 10^{\text{pH}/\text{mil}} \times h \times 4 \sim 40^{\text{pH}/\text{mil}} \times h \quad (6.77)$$

With good engineering principles on a server board, routinely engineering a mounting inductance of less than 2 nH for each capacitor is possible. The condition to have the spreading inductance contribute no more than 20% of the mounting inductance is that the spreading inductance is <0.4 nH.

This rough figure of merit is for a transparent cavity on server boards. From the relationship in [Equation 6.77](#), a cavity 10 mils thick or thicker has a spreading inductance approximately 0.4 nH. This is the origin of an important rule of thumb and why thin dielectric in a cavity is always important.

**Tip**

When the dielectric thickness between planes is >10 mils, the cavity is not transparent and position is important. When the thickness between planes is <10 mils, the spreading inductance is small compared to mounting inductance. The cavity is relatively transparent and location not important.

When the cavity is transparent, the capacitors behave as if they are directly connected together with no inductance in their path. When the cavity is not transparent, significant spreading inductance exists between the capacitors. Although we can roughly estimate this inductance and include it in the total mounting inductance between capacitors, when position matters always do a final analysis with a 3D field solver.

Another example where the cavity is not transparent is a power trace connecting the decoupling capacitor to the observation point rather than a wide power plane. The trace might be 1 inch long and 0.2 inches wide, which amounts to five squares. With a dielectric thickness of 2 mils, the sheet inductance is  $32 \text{ pH}/\text{mil} \times 2 \text{ mils} = 64 \text{ pH/square}$ . The power trace is 5 squares  $\times 64 \text{ pH/square} = 320 \text{ pH}$ . Comparing this to a well-mounted capacitor with 500 pH inductance, even a thin dielectric power trace has significant inductance.

**Tip**

When we use power traces to connect a capacitor to a BGApad, the spreading inductance in the connection is often significant, even with a thin dielectric in the cavity. This is why performing a simple analysis is so important.

## 6.14 SATURATING THE SPREADING INDUCTANCE

The behavior of multiple capacitors on a cavity depends on their relative mounting inductance compared to the cavity spreading inductance and their location compared to the observation point.

When the cavity is transparent and the spreading inductance is small compared with the effective inductance of the capacitors, the capacitors behave as n-parallel capacitors. Their location does not affect their impedance. In effect, the combination of capacitors interacts as lumped capacitors.

As the number of capacitors increases, their parallel inductance decreases as  $1/n$ . There comes a point where the equivalent mounting inductance of the n-capacitors in parallel is less than the spreading inductance from the capacitors to the observation point. The spreading inductance dominates the inductance of the parallel capacitors on the cavity. Adding more capacitors does not decrease the total inductance. We refer to this situation as having “saturated” the spreading inductance.

**Tip**

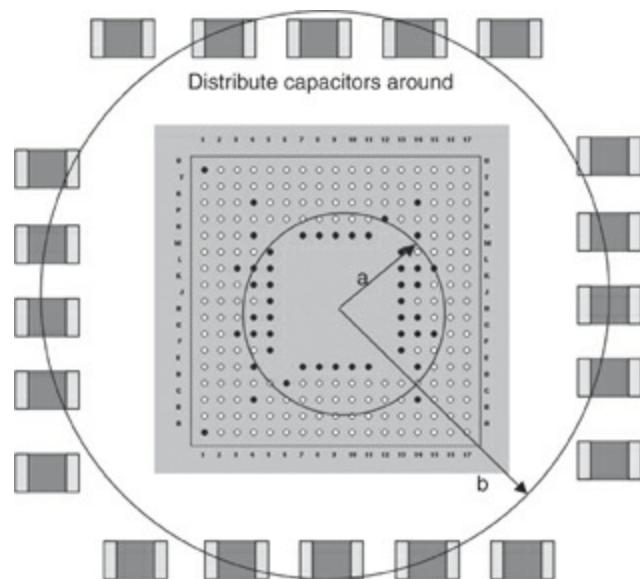
When adding more capacitors does not significantly decrease the total inductance from the capacitors to the load and their total inductance is dominated by the spreading inductance, we refer to this condition as “saturating” the spreading inductance. With saturated spreading inductance, currents from the capacitors to the observation point flow through the same region of the cavity and see the same dominant spreading inductance.

To minimize the impact from saturated spreading inductance, distributing the capacitors uniformly around the device they are decoupling is always a good habit. This spreads out the currents and minimizes their overlap in the cavity.

**Tip**

If decoupling capacitors are associated with a specific package, distribute them uniformly around the package to reduce the saturated spreading inductance and maintain the lowest effective parallel inductance to the observation point.

The power-ground connections to a packaged device are often located near the package's center. We estimate the spreading inductance for current from a distribution of capacitors to get to this central location. This is illustrated in [Figure 6.27](#).



**Figure 6.27** Distribution of capacitors around the circumference of a package.

We estimate the spreading inductance from the central region where the power/ground connections make contact to the underlying cavity, located around a radius  $a$ , to the region where the capacitors are located at a radius  $b$  from

$$L_{\text{spread}} = \frac{\mu_0}{2\pi} \times h \times \ln\left(\frac{b}{a}\right) = 5.1 \times h \times \ln\left(\frac{b}{a}\right) \quad (6.78)$$

For example, if the cavity is 10 mils thick, the inner radius is 0.25 inches, and the outer radius is 1 inch, the spreading inductance to the capacitors is roughly

$$L_{\text{spread}} = 5.1 \text{ pH/mil} \times 10 \text{ mils} \times \ln\left(\frac{1}{0.25}\right) = 71 \text{ pH} \quad (6.79)$$

When the parallel combination of all the ESL of all the capacitors is less than 71 pH, the equivalent inductance is dominated by the spreading inductance in the cavity and it is saturated. Adding more capacitors will not significantly reduce the inductance from the package to the capacitors. The relationship in Equation 6.78 identifies the three important design knobs to reduce the saturated spreading inductance:

- Reduce the cavity thickness
- Increase the distribution radius  $a$  of the BGA power-ground pads in the package
- Decrease the distance  $b$  by bringing the capacitors closer to the package

When the spreading inductance is saturated, adding capacitors under the BGA package might result in lower effective inductance.

## **6.15 CAVITY MODAL RESONANCES AND TRANSMISSION LINE PROPERTIES**

The third region in the cavity's impedance profile at the high-frequency end is where the cavity modal resonances play a role. Large, periodic peaks in the impedance profile characterize this region. These are due to the propagation of waves through the cavity and their reflection from the boundaries of the cavity and resulting interference with each other. This behavior is

referred to as *cavity modal resonances*. To understand the details, we first look at resonances in one dimension in uniform transmission lines and expand this to two dimensions.

A uniform transmission line has two terms that characterize it: a *characteristic impedance* and a *time delay*. The time delay is related to the total length of the line and the speed of a signal in the material that makes up the transmission line. If the far end of the line is open, a signal propagating down to the end of the line reflects and heads back to the source.

A sine wave is launched down the line from the source end reflects from the open at the far end and then reaches the source end. A phase difference exists between the reflected wave arriving at the source end and the incident wave at the source end. This phase difference is related to the round trip time delay and the frequency by

$$\Delta\theta = 2 \times TD \times f = \frac{2 \times Len}{v} \times f = \frac{2 \times Len}{c} \sqrt{Dk} \times f \quad (6.80)$$

where

$\Delta\theta$  = the phase difference between the incident and the reflected wave at the input to the line in cycles

TD = the time delay of the transmission line

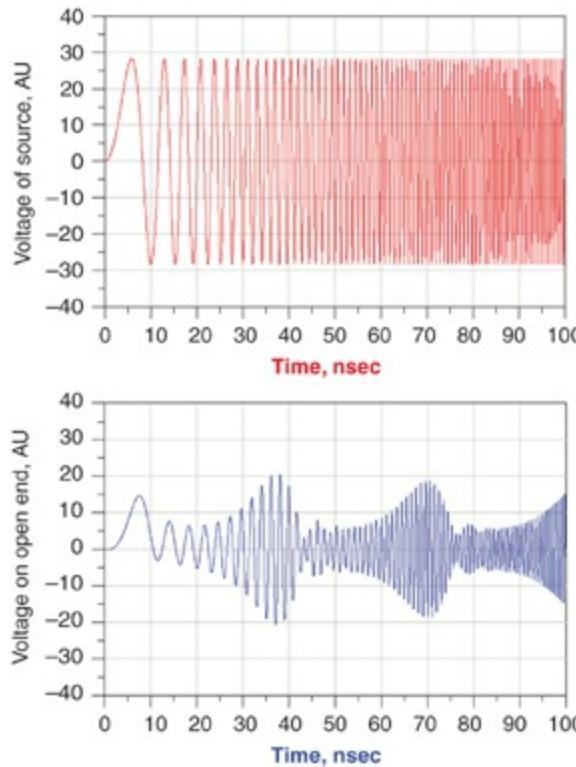
f = the frequency of the signal

Len = the length of the transmission line

If the source impedance driving the transmission line is higher than the line impedance, any signal incident to the source reflects off the source with no phase change.

When the phase of the wave reflected from the far end, having reached the source, is the same as the incident wave, it reflects in phase with the incident wave adding to the voltage on the line. Each time the wave

travels down the line, reflects, comes back to the source, reflects from the source, and starts over again, its voltage wave at each reflection continues to add to the existing wave in the transmission line. This results in very large voltages on the transmission line. Figure 6.28 shows the voltage across the open circuit at the far end of the transmission line as the frequency of the incident signal is swept from 0 Hz to 1.5 GHz into a 6-inch-long transmission line.



**Figure 6.28 Top:** Incident voltage signal into the transmission line with a swept frequency and constant amplitude. **Bottom:** The voltage on the open end of the transmission line showing that when the frequency reaches certain values, the voltage level on the line dramatically increases. These frequencies are referred to as the resonant frequencies of the transmission line.

Simulated with Keysight's ADS.

At certain frequencies, large voltages build up on the transmission line. We call this condition *resonance* and the frequencies where it occurs, *resonant frequencies* or *modes of the transmission line*. The voltage pattern on the line at each resonant frequency is a different mode

of the transmission line. The resonant frequencies are the modal frequencies of the transmission line. The voltage scales for both plots are the same.

These modal resonant frequencies are intrinsic to the transmission line and do not depend on the incident signal. Of course, whether we get a large voltage built up on the transmission line depends on whether the incident signal has any frequency components at the resonant frequencies of the line, and the source impedance. The larger the difference between the source impedance and the transmission line's characteristic impedance the larger are the voltage waves that build up. However, the frequencies where the modal resonances occur do not change with the source impedance.

**Tip**

The resonant modes of the cavity occur at the frequencies at which standing waves build up and large voltages build up across the transmission line. This is equivalent to the transmission line having a higher input impedance at the modal resonant frequencies.

The incident signal only drives a resonance in the transmission line if it has frequency components overlapping the frequencies of the transmission line modes. We refer to this situation as the signal “driving” the transmission line mode.

Constructive interference of successive reflected waves with the incident wave occurs when the phase difference between the incident wave and the first reflected wave back at the source end is an integer number of cycles:

$$\Delta\theta[\text{cycles}] = n \quad (6.81)$$

where

$\Delta\theta$  = the phase difference between the incident wave and the superimposed reflected wave, from the propagation down and back along the length of the interconnect, in cycles

$n$  = the integer number of cycles between the incident wave and the superimposed reflected wave

When the phase difference between the incident wave and the superimposed reflected wave is an integer multiple of cycles, the waves combine together, building up on each reflection. This is *driving a resonance* and the frequency at which this happens is a modal resonant frequency. It is usually designated by the number of cycles between the two waves, the integer,  $n$ .

In this example, we assume the impedances on either ends of the transmission line are the same, both higher than or both lower than the line impedance. We call the impedances on the ends of the line *boundary conditions*. When the boundary conditions on each end of the line are the same, modal resonances occur when there is a whole cycle phase shift for the wave propagating down and back on the interconnect.

When the boundary conditions are the same on each end of the line, the condition for resonance is that the round trip phase shift be an integral number of cycles, which means the round trip length is an integral number of wavelengths. This means the one-way length of the transmission line is an integral number of half wavelengths,

$$\Delta\theta[\text{cycles}] = n = \frac{2 \times \text{Len}}{\lambda_n} = \frac{2 \times \text{Len}}{\lambda_n} \quad (6.82)$$

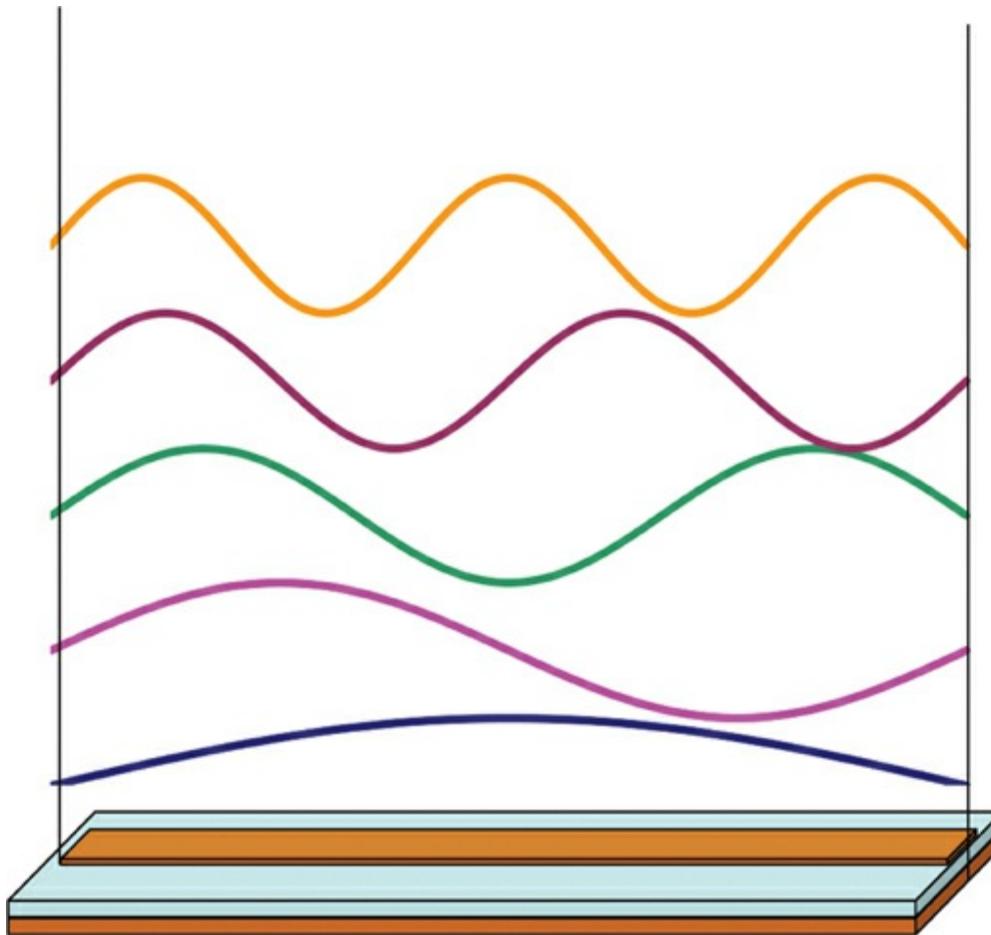
or

$$\text{Len} = n \times \frac{\lambda_n}{2} \quad (6.83)$$

and

$$\lambda_n = 2 \times \frac{\text{Len}}{n} \quad (6.84)$$

Figure 6.29 illustrates this important criterion.



**Figure 6.29** The condition for resonance is that a multiple of a half a wavelength fits between the boundaries of the transmission line. Here we show current waves with half a cycle, 1 cycle, 1.5 cycles, 2 cycles, and 2.5 cycles fitting between the ends of the transmission line.

From Equation 6.84, the condition for stimulating a modal resonance is

$$\lambda_n = 2 \times \frac{\text{Len}}{n} = \frac{v}{f_n} \quad (6.85)$$

and

$$f_n = n \times \frac{v}{2 \times \text{Len}} = n \times \frac{c}{2 \times \text{Len} \sqrt{Dk}} \quad (6.86)$$

These are the specific frequencies at which reflected waves build up and superimpose on themselves in the transmission line, starting with  $n = 1$  and increasing in frequency with  $n$ .

For example, if the transmission line is 6 inches long with FR4, the frequencies at which the successive reflected waves build up are

$$f_n = n \times \frac{c}{2 \times \text{Len} \sqrt{Dk}} = n \times \frac{6 \text{ in/nsec}}{2 \times 6 \text{ in}} = \frac{n}{2} \text{ GHz} \quad (6.87)$$

The first resonant frequency is at  $1/2$  GHz, the second at  $2/2$  GHz, and the third at  $3/2$  GHz. Note that each frequency is uniformly spaced by  $0.5$  GHz. These resonant frequencies depend only on the length of the transmission line and the speed of wave in the material of the transmission line. They are intrinsic to the transmission line.

The standing wave voltage levels on the transmission line are large at these frequencies. The actual voltage levels depend on the incident signal level, the losses in the line, and the impedance mismatch between the source impedance, the line impedance, and load impedance.

If there is a high impedance on one end and a low impedance on the other end, there is an extra phase shift of half a cycle added to the reflected wave in addition to the phase shift from propagation. The condition for waves to superimpose each time they reflect off the far end and then off the source end is still to have an integer number of cycles difference:

$$\Delta\theta[\text{cycles}] + \frac{1}{2} = n \quad (6.88)$$

When the boundary conditions are different on the

two ends of the line, the condition for resonances is

$$\Delta\theta[\text{cycles}] + \frac{1}{2} = n = \frac{2 \times \text{Len}}{\lambda_n} + \frac{1}{2} \quad \text{or} \quad \text{Len} = \left(n - \frac{1}{2}\right) \times \frac{\lambda_n}{2} \quad (6.89)$$

The first resonance corresponds to when the length is  $1/4$  a wavelength and appears at odd multiples of a quarter of a wave:  $1/4, 3/4, 5/4, 7/4$ , and so on of a wavelength. This is in contrast to the resonances when the boundary conditions are the same where they occur at even multiples of a quarter of a wavelength:  $2/4, 4/4, 6/4, 8/4$ , and so on of a wavelength.

Whether an interconnect is excited by an odd multiple or even multiple of a quarter wave depends on if the boundary conditions are the same or different on the two ends.

## 6.16 INPUT IMPEDANCE OF A TRANSMISSION LINE AND MODAL RESONANCES

One way of probing the resonant modes of a transmission line is by looking at the input impedance of the line at different frequencies.

The input impedance of a uniform transmission line open at the far end goes through peaks and valleys in its impedance. This is due to the reflection of the incident wave at the open end, interfering with the incident wave entering the transmission line. This same mechanism creates modal resonances.

One definition of impedance introduced in [Chapter 2](#) is based on the reflection coefficient of a wave. The input impedance of a transmission line is

$$Z_{\text{input}} = Z_{\text{port}} \frac{1+S_{11}}{1-S_{11}} \quad (6.90)$$

where

$Z_{\text{port}}$  = the source impedance of the signal right before

it enters the transmission line

$S_{11}$  = the reflection coefficient from the input of the transmission line

The simplest case is of a  $50 \Omega$  port impedance and an ideal  $50 \Omega$  uniform transmission line with an open circuit at the far end. The magnitude of the reflection coefficient at the open far end is 1. This reflected wave heads back to the source end. It then leaves the transmission line and enters the port, where it is seen as the reflected wave. If the phase of the reflected wave into the port is the same as the phase of the incident wave, the value of  $S_{11}$  is just a real number with a value of 1 because the phase is 0. The input impedance of the transmission line is

$$Z_{\text{input}} = Z_{\text{port}} \frac{1+S_{11}}{1-S_{11}} = Z_{\text{port}} \frac{1+1}{1-1} = \infty, \quad \text{an open} \quad (6.91)$$

This condition for the phase of  $S_{11}$  to be an integer multiple of 1 cycle is the condition for a modal resonance of the transmission line. Peaks in the transmission line's input impedance map out the line's modal resonances.

**Tip**

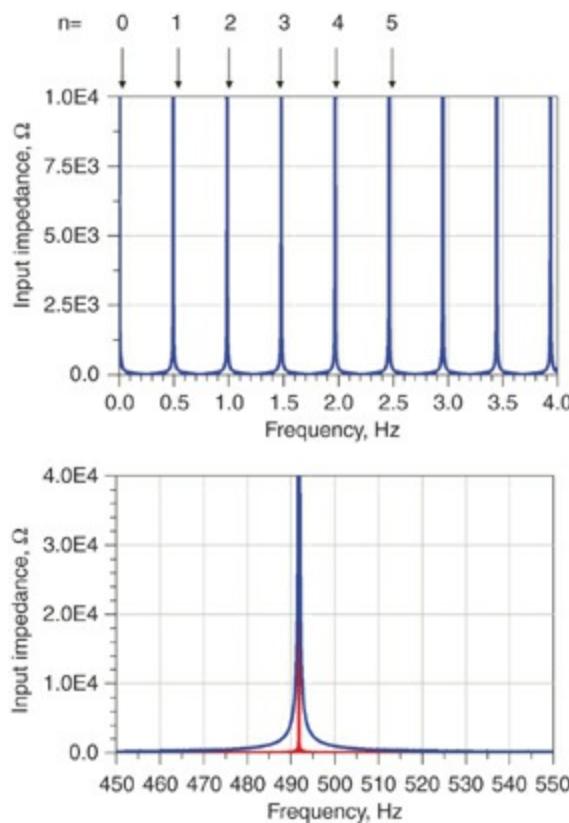
The cavity's impedance profile is a direct measure of the frequencies at which to expect resonant modes of the cavity.

If the impedance of the transmission line is high at some frequencies, then any small current injected into the transmission line at that frequency results in large voltages. This is the condition for identifying a modal resonance.

### Tip

At frequencies where the impedance looking into a transmission line is high, small currents into the transmission line generate high voltages. Both the high voltages and the high impedances are modal properties of a transmission line interacting with applied signals.

The specific shape of the input impedance profile of a transmission line depends on the characteristic impedance of the line, the impedance on the ends and the losses. However, the frequencies for the peaks stay the same. Figure 6.30 shows the input impedance of a  $50 \Omega$  characteristic impedance transmission line 6 inches long in FR4. Included is a close up of the impedance profile from both a  $1 \Omega$  and  $50 \Omega$  characteristic impedance line.



**Figure 6.30 Top:** Input impedance of a  $50 \Omega$  transmission line, open at the end, identifying each of the high impedance resonances. **Bottom:** Expanded frequency scale of the  $n = 1$  resonance comparing a characteristic impedance of  $1 \Omega$  and  $50 \Omega$ . Simulated with Keysight's ADS.

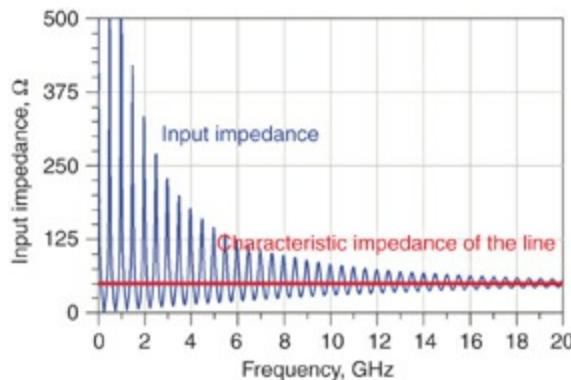
Both conductor and dielectric loss are frequency dependent. As frequency increases, the multiple reflections that contribute to the modal resonances are attenuated.

**Tip**

The higher the frequency, the larger the attenuation per length and the less amplitude left in the multiple reflected waves to interfere together. This drops the peak heights in the impedance resonances.

## 6.17 MODAL RESONANCES AND ATTENUATION

In the extreme case, when there is so much attenuation in a round trip path that there are no waves to interfere and resonate, the input impedance of the transmission line is constant and approaches the characteristic impedance of the line. [Figure 6.31](#) shows the simulated input impedance of a transmission line with frequency-dependent conductor and dielectric loss.



**Figure 6.31** Input impedance of a  $50\ \Omega$  transmission line, open at the end, with conductor and dielectric losses. Note that at high frequency where the losses are very large, the input impedance approaches the characteristic impedance of the line. The peak impedances decrease due to the losses, and the minimum impedance increase slightly. Simulated with Keysight's ADS.

A further factor strongly influences the attenuation in a transmission line and how quickly the impedance peaks decrease with higher frequency. The attenuation

per length from the conductor and dielectric losses is separated and are well approximated by [2][3]

$$A_{\text{total}}[\text{dB/Len}] = A_{\text{conductor}} + A_{\text{dielectric}} = 4.32 \left( \frac{R_{\text{Len}}}{Z_0} + G_{\text{Len}} Z_0 \right) \quad (6.92)$$

where

$A_{\text{total}}$  = the total attenuation per length in dB/length

$A_{\text{conductor}}$  = the attenuation per length in dB/length  
only from the conductor loss

$A_{\text{dielectric}}$  = the attenuation per length in dB/length  
only from the dielectric materials

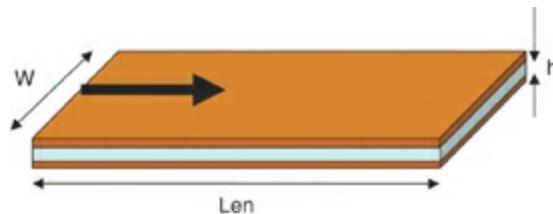
$R_{\text{Len}}$  = the series resistance per length in the two  
conductors

$Z_0$  = the characteristic impedance of the line

$G_{\text{Len}}$  = the conductance per length of the transmission  
line

In the general case of a transmission line that is composed of two wide conductors with a thin dielectric spacing between them, as shown in Figure 6.32, the characteristic impedance is approximated using the parallel plate approximation as

$$Z_0 = \frac{377 \Omega}{\sqrt{Dk}} \frac{h}{w} \quad (6.93)$$



**Figure 6.32** Identifying the dimensions of a long, wide, uniform transmission line with a signal propagating down the long axis.

It is difficult at first glance to identify how the geometry features affects the attenuation, since the characteristic impedance, the series resistance and the

conductance all depend on the transmission line geometry terms in different ways. A simple analysis of their dependence and how they combine together offers a surprising conclusion.

The dielectric loss term is independent of the geometry, depending only on the material properties of the dielectric constant, D<sub>k</sub>, and dissipation factor, D<sub>f</sub>, of the material in the cavity.

The conductance, G<sub>Len</sub>, is the “ac leakage” conductance through the dielectric between the plates, given by

$$G_{\text{Len}} = 2\pi f \times \epsilon_0 \times Dk \times Df \frac{w}{h} \quad (6.94)$$

When this is combined with the characteristic impedance, the attenuation per length from the dielectric loss is

$$\begin{aligned} A_{\text{dielectric}}[\text{dB/in}] &= 4.32(G_{\text{Len}} Z_0) = 4.32 \left( 2\pi f \times \epsilon_0 \times Dk \times Df \frac{w}{h} \times \frac{377 \Omega}{\sqrt{Dk}} \frac{h}{w} \right) \\ &= 4.32 \times 2\pi \times \epsilon_0 \times \sqrt{\frac{\mu_0}{\epsilon_0}} \times f \times Df \times \sqrt{Dk} \\ &= \frac{4.32 \times 2\pi}{11.8 \frac{\text{inch}}{\text{nsec}}} \times f \times Df \times \sqrt{Dk} = 2.3 \times f \times Df \times \sqrt{Dk} \end{aligned} \quad (6.95)$$

All the geometry terms in the dielectric's attenuation cancel out and the dielectric's attenuation is only dependent on the material properties. The dielectric's attenuation scales with frequency due to the inherent loss mechanism of the rotation of the dipoles in the dielectric, jiggled by the frequency of the applied electromagnetic wave.

#### Tip

The attenuation per length from dielectric loss in a cavity is only due to material properties and is independent of any geometry design feature.

At frequencies above the limit where the skin depth is thinner than the geometrical thickness of the conductor, the series resistance per length of the two conductors is approximately

$$R_{\text{Len}} = 2 \times \frac{8.14}{w} \sqrt{f} \Omega/\text{in} \quad (6.96)$$

This assumes current flows on the conductors' inner surfaces. The frequency dependence comes from the skin depth getting thinner as frequency increases. When we combine the series resistance with the characteristic impedance, we find the conductor loss term is

$$\begin{aligned} A_{\text{conductor}} &= 4.32 \left( \frac{R_{\text{Len}}}{Z_0} \right) = 4.32 \left( \frac{2 \times \frac{8.14}{w} \sqrt{f}}{\frac{377 \Omega}{\sqrt{Dk}} \frac{h}{w}} \right) = \frac{4.32 \times 2 \times 8.14}{377} \left( \frac{\sqrt{Dk}}{h} \sqrt{f} \right) \\ &= 0.187 \left( \frac{\sqrt{Dk}}{h} \sqrt{f} \right) \end{aligned} \quad (6.97)$$

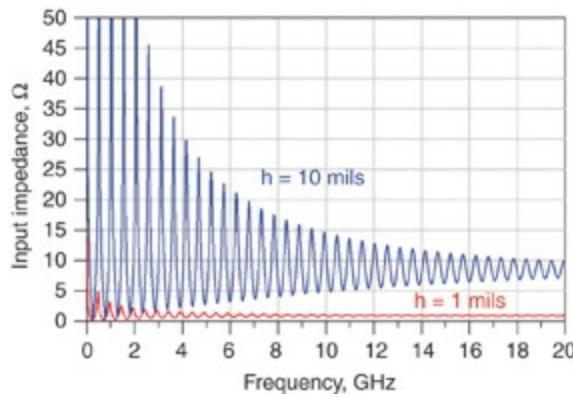
Surprisingly, the attenuation per length from the conductor loss does not depend on the line width of the transmission line. As the line width increases, the resistance decreases, but the characteristic impedance also decreases. These two terms scale the same way with increasing line width, and the ratio stays the same.

This is not the case for the dielectric thickness. The thinner the dielectric between the conductors, the smaller the characteristic impedance and the larger the attenuation. This relationship suggests that the thinner the dielectric, the more attenuation and the more damping of the peak impedances.

#### Tip

When the line width is very wide compared to the dielectric thickness, the attenuation per length from conductor loss is independent of the conductor line width. It depends inversely on dielectric thickness.

Two important benefits occur with using thinner dielectric. The characteristic impedance of the line decreases, which results in lower peak impedance heights. Secondly, the thinner the dielectric, the more attenuation from the conductor loss. Both combine to reduce the impedance peaks, especially at higher frequency. [Figure 6.33](#) illustrates this. The dramatic reduction in impedance peak heights with thinner dielectric is due to the lower impedance and the higher damping. Note the lower high-frequency impedance of the 1 mil thick dielectric line compared to the 10 mil thick dielectric transmission line.



**Figure 6.33** Input impedance of two transmission lines of the same length and line width, but different dielectric thicknesses. Simulated with Keysight's ADS.

**Tip**

The most effective way of reducing the impedance peak heights in a cavity is by using thinner dielectric between the two planes. This increases the attenuation of peaks from conductor loss and reduces the voltage noise generated inside the cavity at the cavity modal resonances.

It is also important to note that both the dielectric loss and conductor loss increase with higher  $D_k$ . A higher  $D_k$  in the material filling the cavity reduces the impedance that increases the attenuation and contributes to more damping of the peaks. However, there is a bigger improvement from thinner dielectric. Increased  $D_k$  should not be at the cost of increased  $h$  as

well.

Simulation tools based on a two-dimensional array of small transmission line segments have been developed [2]–[5]. They extend the one-dimensional concepts presented here, including the attenuation concepts, to the two-dimensional array. These were popular in the 1990s and early 2000s. One of the most useful things about them is that the power integrity engineer could get a good feel for how dimensions and materials affected the power planes and PDN performance. This was before commercial tools were widely available and PI engineers often relied on homemade tools.

Nowadays, good commercial tools are readily available. They often involve full-wave solutions and good three-dimensional meshing to accurately evaluate conductors that do not have a clear return path or plane. They output S-parameter models that we can directly imported into transient simulators. One of the most important considerations is setting up the S-parameter ports. The extracted model results are very accurate but often leave the PI engineer wondering about the internal structures that dominate the inductive or impedance results.

## 6.18 CAVITY MODES IN TWO DIMENSIONS

In the example in [Section 6.17](#), we considered a transmission line as a one-dimensional structure with propagation limited to up and down the line length. The transmission line's narrow width limits signals to propagating only along the long axis, which means waves can only interfere in one direction. This results in modes identified with just one index number. Each mode corresponds to fitting a half-wave multiple between the long axis of the transmission line.

In a cavity composed of two planes, signals propagate

in both the X and Y directions and diagonally. The principles associated with the cavity modes are identical to the case of the one-dimensional transmission line.

Waves can propagate and interfere with each other when traveling in the X direction only, in the Y direction only, or with some component in the X and some component in the Y directions [6][7].

When the boundary conditions for the cavity are open at the edges so there is no phase change upon reflection, the condition for resonant peaks to build up is that an integer multiple of a half a wavelength fits between the ends of the planes. This is the case for the X direction, the Y direction, and diagonal directions.

The three ways of fitting an integer number of half-waves within the boundaries are

- Waves reflecting back and forth along the X-axis
- Waves reflecting back and forth along the Y-axis
- Waves reflecting back and forth along both the X-and Y-axis at the same time

The condition for resonance of waves propagating along the X-axis is that an integer multiple of half wavelengths fit within the length of the cavity in the X direction:

$$n \frac{\lambda_n}{2} = \text{Len}_X \quad \text{or} \quad \lambda_n = \frac{2 \times \text{Len}_X}{n} \quad (6.98)$$

The resonant frequencies are

$$f_n = \frac{v}{\lambda_n} = n \frac{v}{2 \times \text{Len}_X} = n \times \frac{c}{2 \times \text{Len}_X \sqrt{Dk}} \quad (6.99)$$

The same condition holds for fitting multiples of half a wave along the length of the cavity in the Y direction:

$$f_m = m \times \frac{c}{2 \times \text{Len}_Y \sqrt{Dk}} \quad (6.100)$$

The frequencies of the diagonal resonant waves are

$$f_{mn} = \sqrt{f_m^2 + f_n^2} = \frac{c}{2 \times \sqrt{Dk}} \sqrt{\left(\frac{m}{Len_Y}\right)^2 + \left(\frac{n}{Len_X}\right)^2} \quad (6.101)$$

This provides an estimate of each of the modal resonant frequencies for the cavity based on the dielectric constant of the material in the cavity, the length of each side, and the mode number. In the special case of a square cavity, the resonant frequencies are

$$f_{mn} = \sqrt{f_m^2 + f_n^2} = \frac{c}{2 \times Len \times \sqrt{Dk}} \sqrt{(m)^2 + (n)^2} \quad (6.102)$$

**Tip**

The cavity modes in two dimensions are the same as for each dimension considered independently, with the addition of modes having a diagonal pattern of resonances, with m half-waves along one axis and n half-waves along the other axis.

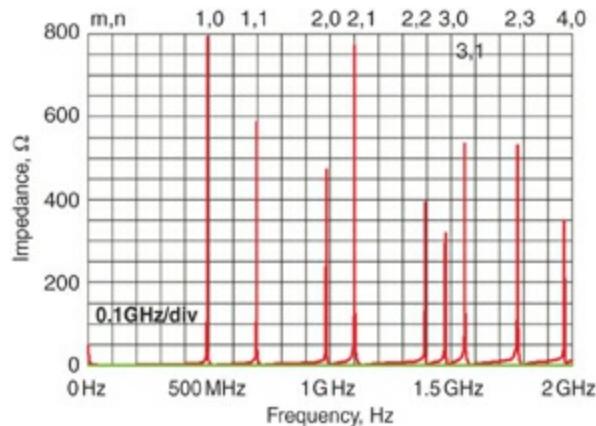
If the length of the cavity is 6 inches in FR4, the cavity modal resonances are at

$$f_{mn} = \frac{6 \text{ in/nsec}}{2 \times 6 \text{ inch}} \sqrt{(m)^2 + (n)^2} = 0.5 \text{ GHz} \sqrt{(m)^2 + (n)^2} \quad (6.103)$$

The cavity modal resonance frequencies are

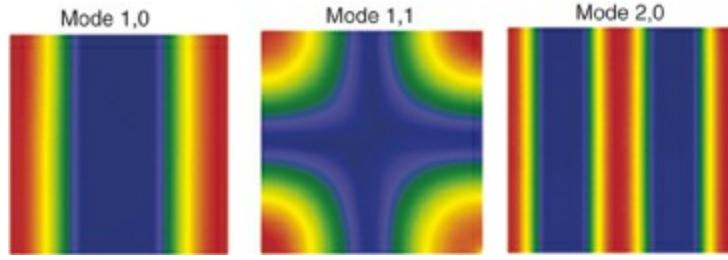
m	n	$f_{mn}$ (GHz)
1	0	0.5
0	1	0.5
1	1	0.71
2	0	1
0	2	1
2	1	1.12
1	2	1.12
2	2	1.41
3	0	1.5
0	3	1.5
3	1	1.58
1	3	1.58
2	3	1.8
4	0	2
0	4	2
3	3	2.12

These are the intrinsic resonant frequencies of the cavity modes. One way of observing the modal resonances is by looking at the cavity's input impedance from an observation point. [Figure 6.34](#) shows the simulated impedance looking into a cavity 6 inches on a side with FR4, measured from a corner. The frequencies identified as specific modes are listed with their (m, n) mode index values.



**Figure 6.34** Simulated impedance of a cavity 6 inches on a side with FR4 material showing the resonant frequencies up to 2 GHz. For each peak, the modal index values are identified. The predicted frequencies match these values very well. Simulated with Mentor Graphics HyperLynx PI.

The specific resonant frequencies of each mode of a cavity are intrinsic to the cavity. These frequency values are not affected by how or where the cavity is measured. The modes are related to the frequencies at which we get standing waves reinforcing each other as they reflect from all the boundaries of the cavity. [Figure 6.35](#) shows examples of the standing wave voltage patterns for three modes. The diagrams plot the maximum voltages present between the cavity's planes. For each of the three modes shown, we drove the cavity in a way to excite primarily that specific mode.



**Figure 6.35** Peak voltage distribution patterns between the planes of a cavity when driven at frequencies for specific modes. These voltage standing wave patterns appear between the two planes. Simulated with Mentor Graphics, HyperLynx PI.

Although the modes exist regardless of the signals present, the efficiency of injecting a signal into a specific mode and the ability to see it in an impedance measurement depends on how well the measurement point excites a signal into that mode.

**Tip**

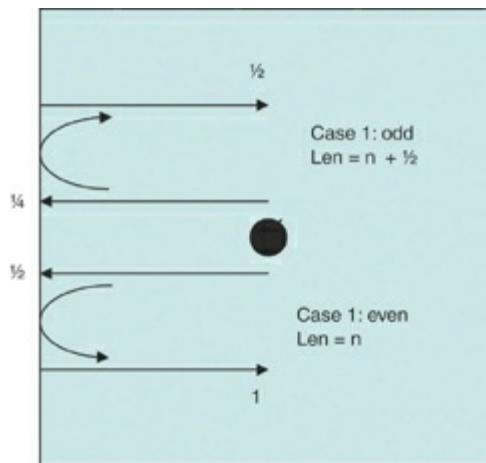
The modes of a cavity are an intrinsic property of the cavity and do not require any signal to be present to exist. Whether a signal is sensitive to a specific mode depends on the overlap and proximity of the signal's frequency components and the modal frequencies.

In the impedance plot in [Figure 6.34](#), we probed the cavity from one point at a corner of the cavity and injected a signal at the model resonant frequency,

stimulating that mode. The injected signal sends waves into every part of the cavity, in all directions. We identify each peak measured as a specific mode that was excited and every mode below 2 GHz showed up as an impedance peak.

A signal launched into the cavity from the center of the cavity does not inject a signal into the first two modes, 1,0 and 1,1. There is no voltage at the center of the cavity for these modes.

Any frequency that has an odd number of half wavelengths in the cavity has reflected waves that cancel out with the incident wave at the center. We will not be able to excite these modes from the center because they are suppressed. Only waves whose frequencies fit an even number of half-waves can be driven from the center of the cavity. Figure 6.36 illustrates why this is the case.



**Figure 6.36** Odd numbered modes are not excited when probed from the center but even numbered modes are.

In this illustration, we show the outline of the cavity with its open edge boundary conditions. The center dot is where we probe the cavity and inject the sine wave signals. We consider two cases. In the first case, the length of an edge is an odd multiple of half a wavelength. In the simplest case, this means the length

of a side is half a wavelength.

The signal comes out from the central location and spreads throughout the cavity. The waves that travel to the left reach the edge where they have a one-quarter-cycle phase difference from the incident waves being injected. They reflect and make their way to the center again, on their way to the far edge on the right. When they pass the center point where we inject the signal, their phase is half a cycle compared to the waves coming out of the source. The reflected wave and the incident wave are a half cycle out of phase from each other and cancel out.

When there is a leftover quarter wave distance from the center point to the edge, reflected waves cancel out with incident waves and no energy is injected into these modes. The modes are still there, but they are just not being excited from signals entering the cavity at the center position.

**Tip**

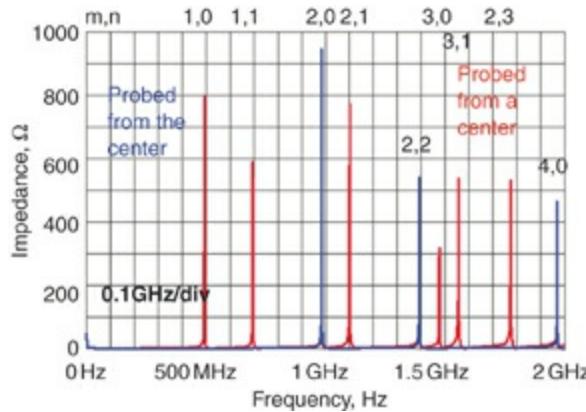
The frequency components of the signal *and* the injection point into the cavity determine whether a mode is excited by a signal. If we inject the signal where the modal pattern has a null or a zero voltage, the signal might not excite the cavity mode, even if it is at the resonant frequency.

In the second case the length of a side is an even multiple of half a wave, which means an integer number of wavelengths fits between the boundaries. In this case, the signal that makes its way to the left edge from the source point has a half cycle phase shift compared with the incident signal. When it reflects and makes its way back to the source heading to the right edge, its phase is one cycle when it passes the source. Waves coming out of the source heading to the right are in phase with the reflected waves heading to the right edge and they add,

building up and driving that mode.

When driven at the cavity's center, only modes that have even numbers for both mode indices are excited and show up as resonant peaks in the impedance profile. These are the 2,0, 2,2, and 4,0 modes below 2 GHz.

Figure 6.37 compares the resonant impedance peaks for the same cavity driven from the corner and from the center. Only the even mode index numbers show up as impedance peaks.



**Figure 6.37** Impedance profile of the same cavity driven from a corner and from the center. When driven from the center, we see only three peaks, corresponding to the frequencies of the 2,0, 2,2, and 4,0 modes.  
Simulated with Mentor Graphics HyperLynx PI.

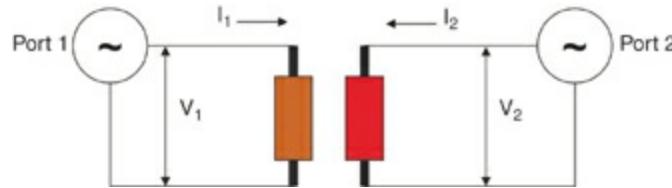
## 6.19 ADVANCED TOPIC: USING TRANSFER IMPEDANCE TO PROBE SPREADING INDUCTANCE

When we measure the self-impedance of a cavity from a single observation point, we always see the series inductance of the cavity spreading inductance dominating the cavity impedance at higher frequency. The spreading inductance will always color the cavity's higher frequency impedance. One way around this artifact is by using the transfer impedance to measure the cavity's impedance.

A more advanced way of describing impedance is the impedance matrix introduced in Chapter 2. This is a way of describing the impedance of any arbitrary number of

connections or ports, not just for a two-terminal device. The impedance matrix description is a useful tool when multiple connections to a device exist in which the ports have some sort of coupling.

Figure 6.38 shows an example of the simple case of two pairs of signal-return contact points to a common device.



**Figure 6.38** The port configuration for driving a current into one port and measuring the voltage at another port to develop the impedance matrix elements.

From each port to the device is a current and across each port is a voltage. The following equations define the voltage across each port:

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \end{aligned} \quad (6.104)$$

This relationship defines the impedance matrix elements. The diagonal impedance terms, referred to as the self-impedances, relate to our usual definition of impedance:

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \quad \text{and} \quad Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0} \quad (6.105)$$

These elements are equivalent to one-port impedance measurements. Of course, the self-impedances of a plane measured between one pair of contacts are sensitive to the spreading inductance into that contact region. This is where the off-diagonal impedance elements, sometimes referred to as *transfer impedances*, play an important role. The transfer impedance is

$$Z_{21} = \left. \frac{\mathbf{V}_2}{\mathbf{I}_1} \right|_{\mathbf{I}_2=0} \quad \text{and} \quad \mathbf{V}_2 = Z_{21} \times \mathbf{I}_1 \Big|_{\mathbf{I}_2=0} \quad (6.106)$$

We interpret the transfer impedance,  $Z_{21}$ , as the ratio of the voltage generated at the location of port 2, when a current is injected into the location of port 1. The voltage at the location of port 2 is generated by the current from port 1 flowing through the transfer impedance. Transfer impedance is not an impedance “between” the two measurement points, but is an impedance “shared” by the two different observation points.

**Tip**

Think of the transfer impedance between two measurement points in a cavity as the impedance shared by the radial current wave from one point spreading outward in the cavity.

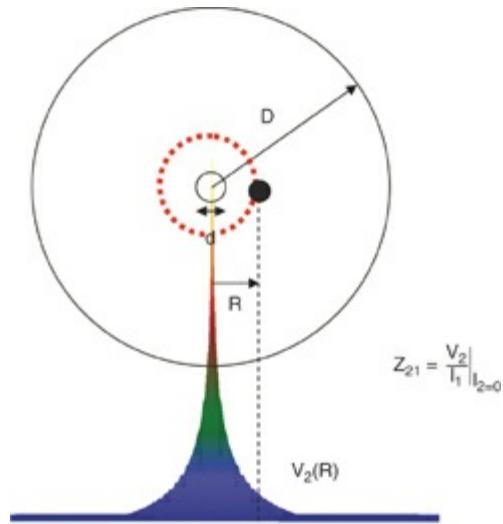
As illustrated in [Chapter 3](#), we can measure the self and transfer impedance using a two-port VNA with the ports connected appropriately, depending on what we want to measure.

When the two ports are connected to the same pair of pads, the self and the transfer impedance are the same. This is the case when simulating the two-port S-parameters. However, in a real measurement, due to residual probe effects that we cannot calibrate out, the measured self-impedance always contains some uncalibrated probe artifacts whereas the transfer impedance does not. In a measurement, the transfer impedance is always a cleaner measurement of the impedance between the two pads when both ports touch the same pads.

When different pad locations are used for ports 1 and 2, the transfer impedance is the same as the two-port impedance discussed in [Chapter 3](#):

$$Z_{21} = 25\Omega \frac{S_{21}}{1-S_{21}} \quad (6.107)$$

We can use transfer impedance to probe the distribution of spreading inductance in a cavity. Figure 6.39 illustrates a simple case of a circular cavity with port 1 connected between the two planes that make up the cavity at the center location and port 2 located some distance R from the center.



**Figure 6.39** The center point with diameter d is port 1, and port 2 is located a distance R from the center. As the current from port 1 spreads outward, the voltage in the cavity decreases through the spreading inductance and is plotted in the solid figure below. The voltage at port 2 depends on the location of port 2, and the transfer impedance depends on the location.

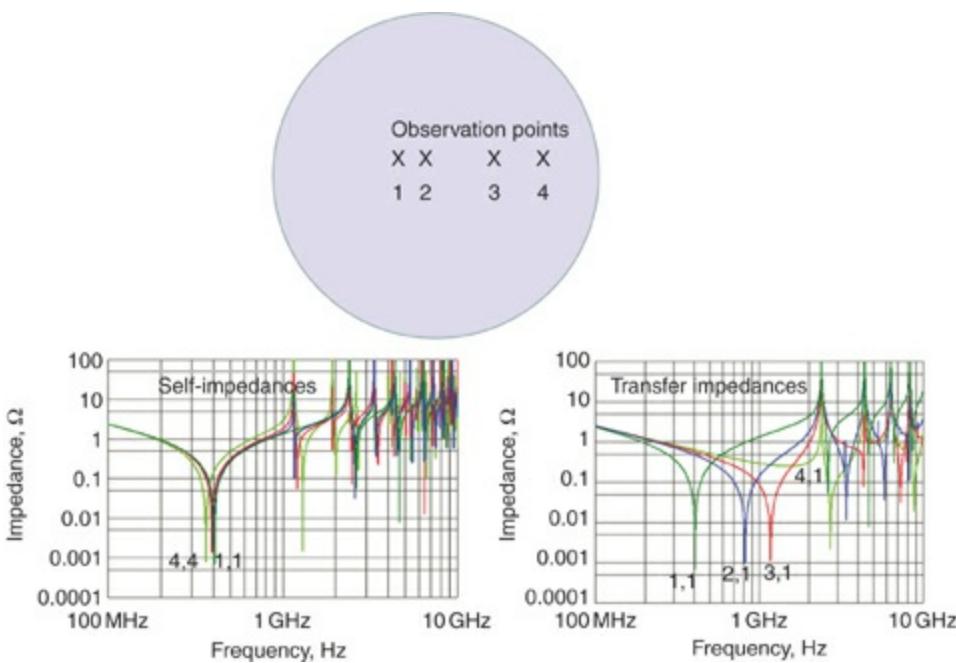
In this configuration, the voltage picked up at port 2 depends on where port 2 is located and how much spreading inductance there is in the cavity. When spreading inductance is high, the value of  $V_2$  drops off rapidly as distance increases from the center.

**Tip**

The spreading inductance between a central contact point and a second point located some distance away is equivalent to the spreading inductance a circular ring of BGA balls might see when looking into the rest of the cavity. The greater the radius of the ring of balls, the lower the shared spreading inductance they see looking into the cavity.

The value of  $V_2$  is directly related to the transfer impedance. The farther from the center the measurement point, the lower the shared spreading inductance to the edge of the cavity and the lower the voltage drop generated. This voltage measured at the location of port 2 is in a sense the voltage at that location due to the currents flowing from the ring at port 2 into the rest of the cavity. It is a measure of the impedance from the concentric ring at radius R to the edge of the cavity.

To illustrate the interpretation of transfer impedance we take the simple case of a pair of planes making a circular cavity 3 inches in diameter. Their separation is 10 mils. We add a port to the center of the cavity and add three other ports, each marked with an “x,” farther and farther away from the center. Figure 6.40 shows the simulated self-impedance and transfer impedances associated with these four observation points.



**Figure 6.40** Self- and transfer impedances on a cavity at four different observation points. **Top:** Location of the four observation points. **Bottom:** The self- and transfer impedances.

The self-impedances behave as expected. The closer the observation point is to the edge, the higher the spreading inductance, and the lower the series resonance frequency (SRF) dip. We also see a higher impedance above the SRF with more spreading inductance. This is the artifact that should reduce transfer impedance. Note that the frequencies of the modal resonances, identified by high impedance peaks, do not depend on the location of the observation point.

In the transfer impedance plot to the right, we see that the frequency of the 2,1 impedance minimum increases as the second observation point is moved away from the center. It is closer to the cavity's edge. The impedance on the high-frequency side, a rough measure of the spreading inductance, is dramatically reduced.

The transfer impedance is much less sensitive to the cavity spreading inductance as the two probe points move farther apart. For point 4, near the circumference, the cavity's impedance looks almost purely capacitive until the onset of the first modal resonance. The

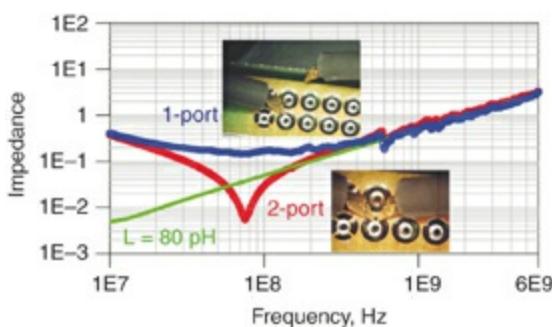
effective spreading inductance observed at this far away location is almost zero.

Interestingly, note that the peak transfer impedances, corresponding to the modal resonances of the planes, are also independent of the location for point 2. The current injected into the cavity at location 1 drives whichever modal resonances the cavity supports. Unlike the frequencies of the dips, these modal frequencies are independent of the observation points. They are intrinsic to the cavity dimensions.

In the low-frequency region where we identify clear capacitive or inductive behavior from the impedance, interpreting the self- and transfer impedances is straightforward. Above these frequencies, making sense of the impedance profiles' details (other than identifying specific modal resonances) is very difficult.

The concept of transfer impedance as a probe of the properties of a distributed cavity is very powerful when applied to measurements. For example, we can use the two-port measurement from various positions of a cavity to separate out via inductance and spreading inductance in the cavity.

We measured a board with a buried cavity consisting of two planes separated by about 1 mil with a VNA. Using one-port and two-port techniques, microprobe contacted the top of the board where the vias connect to the two planes. Figure 6.41 shows the extracted impedance measurements from these two configurations.



**Figure 6.41** Measured impedance from the top of a board through vias into the buried cavity using the one-port and two-port techniques. Also included is the impedance of an 80 pH inductance for comparison.

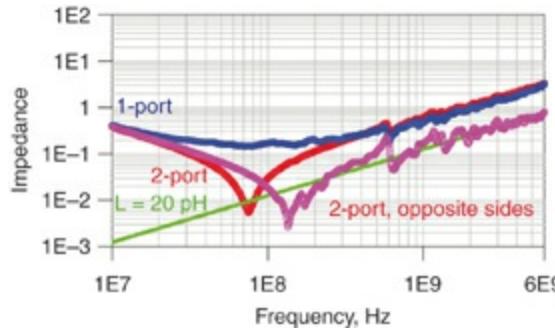
In this example, the total loop inductance looking into the cavity is about 80 pH. This includes the via pair into the top of the cavity and the spreading inductance into the planes of the cavity. The one-port measurement shows the contact impedance of the probes in series with the vias and the spreading inductance to the planes. The two-port measurement, with both microprobes touching the top surface of the same via, eliminates the probe effects, but still shows the via loop inductance in series with the spreading inductance into the cavity.

**Tip**

A measurement from the top surface of a board into a cavity through vias using two-ports is still sensitive to both the loop inductance of the via down to the cavity and also the cavity spreading inductance.

Next, we move the probes to opposite sides of the board, one touching the top of the via pair and the other probe touching the via pair on the bottom of the board. In this way, one probe drives a current into the top of the via, through the planes to the cavity's edge. The other probe measures the voltage generated on the bottom of the via pair. It is not sensitive to the voltage drop from the top of the via to the middle of the via

where the planes make contact. It is only sensitive to the voltage created as the current spreads out from the via contact point into the cavity. This two-port measurement, shown in [Figure 6.42](#), is a direct measurement of the spreading inductance both into the cavity and to its edge without the influence of the via.



**Figure 6.42** Added two-port measurement with the microprobes contacting opposite ends of the same via pair. This measurement is sensitive to the spreading inductance into the cavity.

Using contacts on opposite ends of the via, we see the impedance measurement is independent of the via loop inductance and is only sensitive to the spreading inductance of the cavity. Comparing this impedance to an ideal 20 pH inductor shows a good match to the spreading inductance.

For a 1 mil thick cavity, we expect the spreading inductance to be on the order of the cavity's sheet inductance, which is  $32 \text{ pH}/\text{mil} \times 1 \text{ mil} = 32 \text{ pH}$ . In this example, we measure about 20 pH, which is of the same order. Note also that we just begin to see some of the cavity modal resonances superimposed on the spreading inductance impedance. The higher frequency modal resonances are damped out due to the very thin dielectric in the cavity.

**Tip**

When we measure from opposite sides of a through via, using the two-port technique eliminates the via loop inductance and reveals directly the spreading inductance into the cavity. This is the best technique to measure the incredibly small spreading inductances, typically on the order of a few tens of pH.

Transfer impedance is another powerful tool used to analyze the voltage, current, and impedance properties of cavities, when the cavity contains other components.

## 6.20 THE BOTTOM LINE

1. A cavity is composed of two planes in close proximity. The impedance between the two planes shows three distinct regions.
2. At low frequency, the impedance of a cavity looks like a capacitor. This capacitance provides a simple way of measuring the Dk of a laminate material.
3. The dip in a cavity's impedance profile is similar to a self-resonant frequency of an LC circuit. The L is a direct measure of the cavity-spreading inductance. The C is the cavity parallel plate capacitance.
4. At the highest frequencies, the cavity's modal resonances dominate its impedance.
5. The effective characteristic impedance a signal sees propagating inside a cavity is often well below  $0.1 \Omega$ .
6. The spreading inductance inside a cavity depends on the current density influenced by features in the cavity that might constrict the free flow of current.
7. The spreading inductance between two points in a cavity scales with the log of the spacing between the points.
8. Adding a capacitor to a cavity creates a new

parallel resonance where the capacitor's inductance interacts with the cavity's capacitance.

9. The frequencies of a cavity's modal resonances depend only on the cavity's dimensions and the dielectric filling it.
10. The most effective way of reducing the high-frequency modal resonances of a cavity is by using very thin dielectric that damps out the peaks.

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# Chapter 7. Taming Signal Integrity Problems When Signals Change Return Planes

## 7.1 SIGNAL INTEGRITY AND PLANES

The DC voltage on a return plane has no impact on the characteristic impedance of a transmission line or on the quality of a signal propagating between the signal and return path. This means a 5 v or even a 12 v plane makes just as good a return path as a ground plane.

When the signal line transitions from one layer to another in a multilayer circuit board and its return current changes plane layers, the return current must flow between the two plane layers. Herein lies the problem. It is similar to the problem of someone falling off a building. The falling part is not the problem. The landing is the problem.

When the return current flows through the impedance of the cavity made up of two planes, it passes through the impedance of the cavity and generates a voltage between the planes. This voltage, initially created in the vicinity of where the signal via passes through the cavity, injects a propagating voltage wave into the cavity. Any other via passing through the cavity can pick up this transient voltage as cross talk.

### Tip

The primary way high-frequency noise is injected into cavities is by return currents passing through the impedance between adjacent planes inducing transient voltages. This produces cross talk and potentially contributes to radiated emissions. Both of these effects are important and involve the power planes but are unrelated to the quality of power distribution to the core voltage rails.

This is the primary mechanism by which high-

frequency noise is injected in cavities—by signals transitioning through the cavities, using each plane successively as a return path. This noise injected in the cavity has very little to do with power distribution network design. However, we include this source of noise in this chapter because it is very important for signal integrity design. It involves the same planes as used for power delivery. From an analysis of this insidious source of noise, we gain an understanding of the root cause and develop design guidelines to minimize this problem.

## 7.2 WHY THE PEAK IMPEDANCES MATTER

The same power and ground planes that carry the supply current to the rails of the integrated circuits (ICs) are also often used as the return path for signals. In the next chapter, we show that the cavity resonances in power and ground planes do not play an important role or significantly degrade power delivered to the core logic of the IC. This is because the rails on the chip do not see the high-frequency cavity modal resonant peak impedances when looking through the package lead inductance.

**Tip**

The peak impedances from cavity modal resonances are rarely an important issue in power integrity. They are very important in signal integrity and electromagnetic compatibility (EMC).

When signals transition through a cavity, their return currents can excite the cavity resonances and any other parallel resonances. When signal return currents pass through a cavity and have significant frequency components overlapping with the peak impedances, they generate excessive voltage noise between the two planes of the cavity. This noise voltage contributes to

two potential problems: enhanced cross talk, which is a signal integrity problem, and EMC violations.

In many publications in the popular literature, the power integrity, signal integrity, and EMI problems are not well-separated and often blurred together. Cavity resonances are first a signal integrity problem and can sometimes contribute to an EMC problem. They are rarely a power integrity problem. Minimizing their impact for signal integrity and EMC is important but they are usually not relevant for power integrity.

The voltage noise from return currents passing through the cavity can be a very serious signal integrity problem [1][2]. Other signal vias passing through the cavity see the voltage noise between the planes as cross talk. The more switching signals pass through the cavity, the more voltage noise is picked up by other signal vias. This cavity noise is not local to adjacent vias but is long range. It affects vias that are all over the cavity, not just the ones in close proximity to the active signal vias. This makes the problem very hard to diagnose.

**Tip**

The real problem with peak impedances in the cavity is the risk they pose for signal return currents passing through the cavity with frequency components at the peak impedances. The current, through the high impedance, can result in excessive voltages across the cavity that contributes to cross talk and EMC problems.

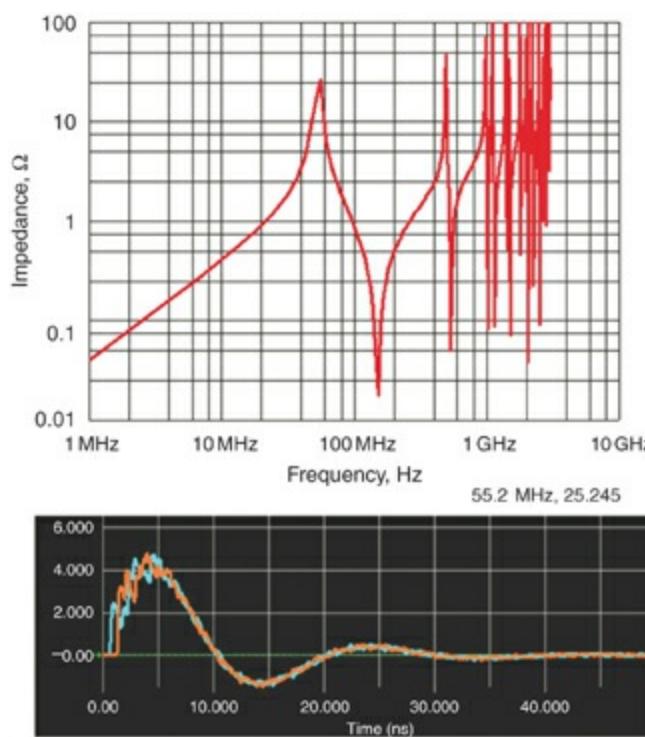
For example, a cavity 6 inches on a side composed of a power and ground plane connected to a VRM has parallel resonant impedance peaks between the inductive slope of the VRM and the capacitance slope of the cavity as well as cavity modal resonances.

At low frequency, the cavity's impedance looks like an inductor because of the series inductance of the VRM shorting the planes. This inductance combined with the

cavity capacitance results in a parallel resonant peak impedance around 55 MHz in this example. In addition, there are the cavity modal resonances that begin at around 0.5 GHz.

When a signal transient current with a rise time of 200 psec passes through the cavity in an aggressor via, it causes an equal and opposite return current to pass through and disturb the cavity. The return current might be through nearby vias or by displacement current. The voltage disturbance has frequency components up to a bandwidth of  $0.35/0.2 \text{ nsec} = 1.7 \text{ GHz}$ . It excites the cavity peak impedances at 55 MHz, 0.5 GHz, and 1 GHz.

We expect enhanced voltage noise generated at these specific frequencies. Figure 7.1 shows the impedance profile of the cavity and the voltage noise picked up on two signal vias passing through the cavity. The victim vias are positioned at opposite corners of the cavity, yet show similar noise magnitude with frequency components at 55 MHz and at about 0.5 GHz.



**Figure 7.1 Top:** Impedance profile a power plane cavity with VRM. **Bottom:** The transient voltage noise picked up by two distant signal vias passing through the cavity when an aggressive signal passes through the cavity. The voltage scale is in mV. Simulated with Mentor Graphics HyperLynx PI.

The magnitude of the noise has only minor dependence on the victim and aggressor via locations across the 6-inch  $\times$  6-inch cavity. The voltage noise in the cavity is very long range meaning that all signal vias in the cavity are affected by it. The noise induced in each victim signal via has a peak magnitude of about 5 mV, which is 1.5% of the 300 mV signal swing, just because they also pass through the cavity. A single 200 ps rise time signal launched into a  $50\ \Omega$  transmission line and cavity via produces 6 mA return current passing through the cavity. If 10 aggressor signals were to simultaneously transition through the cavity, the victims receive approximately 15% of the signal swing as noise. This is a long-range effect because the 10 aggressor signals could have passed through anywhere in the 6-inch square cavity.

Two significant frequency components appear in the

induced noise on the victim signal vias as shown in the time domain plot. The low-frequency component has a period of about 20 nsec, which is a frequency of about 50 MHz. The high-frequency noise has about three cycles in 4 nsec, or a little over 0.5 GHz. These two frequencies match the first two peaks in the impedance profile.

This enhanced voltage noise in the cavity can be a significant EMI and signal integrity problem. In any complex electronics product, with reasonable interconnect density requirements, avoiding multiple signal layers is impossible, which means signal vias are a fact of life. Whenever a signal penetrates through a cavity, its return currents have the potential of driving voltage noise between adjacent return planes. This is absolutely unavoidable.

**Tip**

The most common source of high-frequency noise in a power and ground plane cavity is from high-bandwidth return currents injected as a direct result of signal vias transitioning through the cavity. This noise is long range and contributes to via-to-via cross talk and EMI.

However, the signals' return currents don't have to create excessive voltage noise in the cavity. One way to avoid this problem is to engineer the magnitudes of the peak impedances low enough so that the switching currents do not generate significant noise voltages. Another way is to push the peak impedances up to a frequency that is beyond the bandwidth of the signal so the high impedance peaks are not excited by transient currents. We can engineer both of these solutions by optimizing features of the cavity.

As discussed in this chapter, the cavity resonances are not a problem for the power distribution network

delivering clean voltage to the core circuits of the active devices, Cavity noise is, however, a huge problem for signal integrity and EMI on many boards. Because it concerns the same cavity structures often used to transport the power, we include the design techniques to reduce the cavity noise in the next sections. This reduces signal integrity and EMI problems.

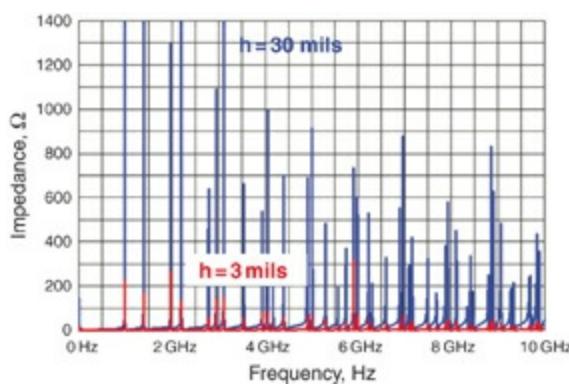
### **7.3 REDUCING CAVITY NOISE THROUGH LOWER IMPEDANCE AND HIGHER DAMPING**

We showed in [Chapter 6](#) that higher frequency signals are more highly damped than low-frequency signals in a one-dimensional transmission line. This is due to frequency-dependent loss. This means that the signals in higher order modes are more damped than lower order modes as we go up in frequency. This is also the case in a two-dimensional cavity. Higher frequency modes are damped more than lower frequency modes.

**Tip**

In general, both conductor and dielectric loss increase with frequency, and higher order modes are damped more than lower order modes. Thinner dielectric increases the damping of modal peak impedances in a cavity due to more conductor loss.

A thinner dielectric in the cavity decreases the spreading inductance in the cavity, decreases the impedance of the cavity, reduces the impedance peaks, and further increases the damping with higher frequency. These are all important advantages of using a thin dielectric in the cavity. [Figure 7.2](#) shows the impedance profile, looking into the center of two different cavities. They are 6 inches on a side and filled with FR4. The only difference is that one cavity has a 30 mil thickness between the planes and the second cavity has a 3 mils thickness.



**Figure 7.2** Impedance peaks for the two different thickness cavities. The thinner the cavity, the more highly damped and the lower the impedance peaks at the cavity resonances. Simulated with Mentor Graphics HyperLynx PI.

**Tip**

The most effective way of suppressing modal resonances in planes is to use very thin dielectric between the two planes. This reduces the impedance of the cavity, producing a lower voltage drop for the same current, and enhances the losses at higher frequency from higher conductor loss.

An intuitive way of viewing the power plane cavity is an array of two-dimensional transmission lines. You can find more details on this in the advanced section (7.15) of this chapter. The impedance of the power plane cavity is closely related to the characteristic impedance of the two-dimensional transmission line segments. Thinner dielectric reduces the inductance and increases the capacitance per length of each of the transmission line segments, thus reducing the characteristic impedance, because

$$Z_0 = \sqrt{\frac{L}{C}} \quad (7.1)$$

Consistent with this, thinner dielectric reduces the effective impedance of the cavity [3][4].

The discussion on impedance and attenuation for one-dimensional transmission lines in [Chapter 6](#) also applies to two-dimensional transmission lines. We

summarized the equations here:

$$Z_0 = \frac{377\Omega}{\sqrt{Dk}} \frac{h}{w} = \frac{1}{Y_0} \quad (7.2)$$

$$A_{\text{conductor}} = 4.24 \times \left( \frac{R_{\text{Len}}}{Z_0} \right) = 0.187 \left( \frac{\sqrt{Dk}}{h} \sqrt{f} \right) \quad [\text{dB/inches}] \quad (7.3)$$

$$A_{\text{dielectric}} = 2.3 \times f \times Df \times \sqrt{Dk} \quad [\text{dB/inches}] \quad (7.4)$$

where

$Z_0$  = the characteristic impedance of the cavity as viewed by a signal propagating parallel to one edge of the cavity

$Y_0$  = the characteristic admittance of the cavity

$R_{\text{Len}}$  = the resistance per length of the conductor, which increases with frequency due to skin depth effects

$h$  = the cavity dielectric thickness

$w$  = the width of the cavity perpendicular to the direction of propagation

$Dk$  = the dielectric constant of the material filling the cavity

$A_{\text{conductor}}$  = the attenuation per length from conductor losses

$A_{\text{dielectric}}$  = the attenuation per length from dielectric losses

$f$  = the frequency at which the attenuation is calculated

Our major goal is to reduce the cavity noise by optimizing the cavity properties. Some amount of return current needs to flow through the cavity because of aggressor signal activity. We need to do everything we can to reduce the impedance peaks because the cavity noise voltage is the product of impedance and the noise

current. We do this by both reducing the impedance of the power planes and by increasing the damping.

Based on the earlier equations, Table 7.1 summarizes the effects that dielectric thickness,  $Dk$ ,  $Df$ , and frequency have on the cavity impedance, admittance, and attenuation. We achieve the best cavity noise performance from lower impedance and increased damping. Conductor and dielectric loss are shown in the last two columns and are maximized when the quantity in the table is maximized. Clearly, the most important property is the dielectric thickness because impedance improvement and conductor loss are inversely proportional to it. Dielectric constant improves impedance and damping but only as the square root.

Cavity Parameter	$Z_0$	$Y_0 = 1/Z_0$	Conductor Loss	Dielectric Loss
Dielectric thickness	$h$	$\frac{1}{h}$	$\frac{1}{h}$	—
Dielectric constant	$\frac{1}{\sqrt{Dk}}$	$\sqrt{Dk}$	$\sqrt{Dk}$	$\sqrt{Dk}$
Dissipation factor	—	—	—	$Df$
Dielectric loss	—	—	—	1
Conductor loss	$\frac{1}{Z_0}$	$Y_0$	1	—
Frequency	—	—	$\sqrt{f}$	$f$

**Table 7.1** Summary of the important cavity parameters and how they affect the electrical properties.

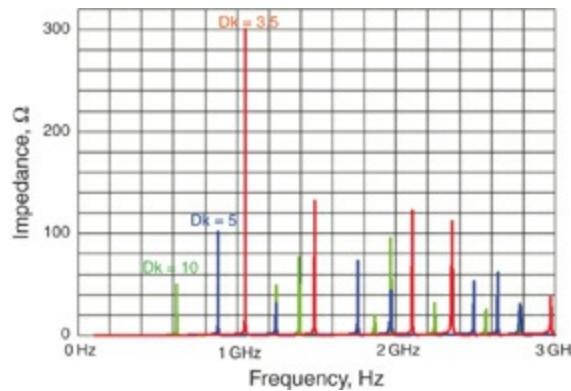
Although the dielectric loss is independent of the characteristic impedance of the cavity, the conductor loss is not. It scales inversely to the characteristic impedance. Lower characteristic impedance of transmission line segments means higher attenuation, which reduces the peak impedances at the cavity resonances.

Decreasing the dielectric thickness,  $h$ , decreases the

characteristic impedance but so does a higher dielectric constant. In addition, the attenuation from the dielectric loss is proportional to the square root of the dielectric constant, so damping from both conduction and dielectric mechanisms increases with higher dielectric constant. As long as a thicker dielectric is not required, a higher Dk always results in more attenuation, smaller peak heights, and better performance.

However, a higher Dk also shifts the cavity modal resonances to lower frequency. Sometimes this is a plus and sometimes a minus. Never use a higher Dk at the sacrifice of thicker h.

Figure 7.3 compares the impedance profiles of the same 4 mil thick cavity, 3 inches on a side, with a Dk = 3.5, 5, and 10. The frequency of the resonant peaks reduce with increasing Dk as expected because the wave velocity in the cavity has decreased.



**Figure 7.3** Impedance profile for the same 3 inch  $\times$  3 inch square cavity with three different dielectric constants. The higher the Dk, the lower the resonant frequencies, the lower the cavity impedance, and the more the damping.

In addition to thinner dielectric and higher dielectric constant, other ways of suppressing cavity resonances exist. We cover some of these approaches in the next section.

## 7.4 SUPPRESSING CAVITY RESONANCES WITH

## SHORTING VIAS

In general, the interactions of shorting vias between the cavity planes of similar voltage and the cavity's impedance are complicated. The low inductance of the shorting vias interacts with the capacitance of the cavity creating a parallel resonance. In addition, the location of the shorting vias influences the boundary conditions of the cavity and affects how waves trapped in the cavity reflect, bounce around, and interfere inside the cavity.

To avoid an impedance discontinuity and coupling of return current into the cavity, an ideal signal-return path through the cavity should look like a short length of matched impedance coax cable. This avoids an impedance discontinuity and has no stray magnetic fields inside the cavity, which drives cavity currents and induces cavity noise.

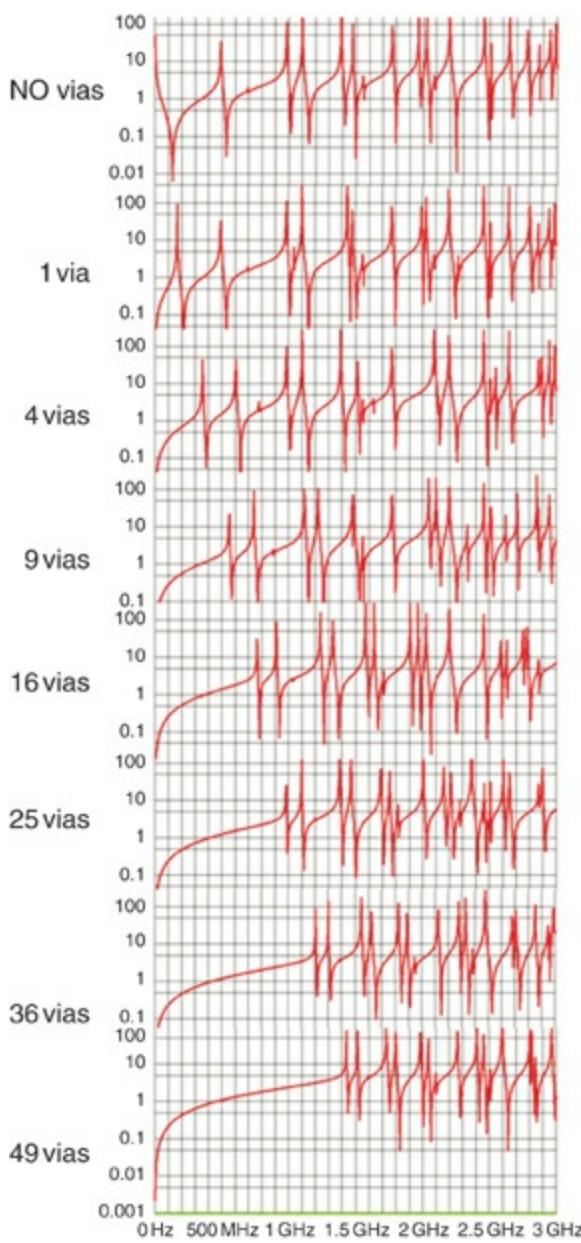
Adding enough return vias to make the signal path look like a coax is often not practical due to the larger board required. However, via engineering for a matched impedance is sometimes done for very high-speed signals, both single-ended and differential, where insertion and return loss specifications need to be met. This usually involves adjusting the clearance holes through the cavity and proximity of a few return vias. For differential signal vias, the return vias play as important a role for the common currents as they do with single-ended signal vias. The common currents are what require the return vias.

In general, we need a 3D field solver to analyze the cavity impedance at high frequency with high accuracy. However, we can make some simple arguments and develop some rules of thumb that give much insight into the behavior of cavity-shorting vias. Without resorting to a 3D field solver, we anticipate that uniformly distributed shorting vias over the surface of

the cavity are effective at suppressing cavity modal resonances. This gives the lowest spreading inductance between the vias and has the most influence on cavity modal resonances. We analyze uniformly distributed shorting vias in the following examples.

A square cavity filled with FR4, 6 inches on a side, has a first resonant peak at 500 MHz corresponding to a half a wavelength fitting in the length of the cavity. We observed the impedance profile,  $Z_{11}$ , from a contact point at an edge of the cavity. Adding one shorting via in the center of the cavity has little impact on the cavity modal resonances. Its presence only changes the low-frequency cavity impedance from capacitive to inductive.

Adding multiple shorting vias distributed uniformly across the cavity shifts the first resonance and all higher order resonances to higher frequency. Figure 7.4 shows the impact on the cavity impedance, measured from near the edge of the cavity, from adding 1, 4, 9, 16, 25, 36, and 49 shorting vias distributed uniformly over the surface of the cavity.



**Figure 7.4** Impedance profile,  $Z_{11}$ , of a cavity with an increasing number of shorting vias. Simulated with Mentor Graphics HyperLynx PI.

Adding more shorting vias to the cavity moves the first peak in the impedance profile toward higher frequency. This first peak is approximated as the parallel resonant frequency between the shorting inductance of the  $n$  vias in parallel with the cavity capacitance. As discussed in the previous chapter, we can view the spreading inductance away from the via as a lumped inductance through which current flows to a lumped capacitance that is concentrated at the furthest radius from the via.

More vias with closer spacing results in lower equivalent shorting inductance and a higher parallel resonant frequency. We can view this as many parallel inductors serving current to the entire cavity capacitance, or alternatively, as a single via serving current to a smaller cavity capacitance area. In both cases, the resonant frequency of the lumped LC circuits goes up as the number of vias increases.

**Tip**

Adding more shorting vias to the cavity reduces the loop inductance from the shorting vias to the capacitance of the cavity, which shifts the self-resonant frequency higher. This pushes the first resonant peak of the cavity to higher frequency.

We use this simple model to estimate the frequency of the first cavity resonance with  $n$  vias. As discussed in [Chapter 6](#), via inductance and the power plane spreading inductance are one and the same. They both produce the same magnetic field. The parallel resonant frequency of the cavity capacitance and the  $n$  vias in parallel is

$$f_{\text{res}} = \frac{1}{2\pi} \sqrt{\frac{1}{C_{\text{cavity}} \frac{1}{n} L_{\text{via}}}} \quad (7.5)$$

We get the cavity capacitance from the parallel plate approximation:

$$C_{\text{cavity}} = \epsilon_0 Dk \frac{Len^2}{h} \quad (7.6)$$

We approximate the partial-self-inductance of each via as a function of length (cavity separation) and some constant related to the via diameter:

$$s_{\text{via-via}} [\text{inches}] < 3 \times RT [\text{nsec}] \quad (7.17)$$

where

$f_{\text{res}}$  = the first parallel resonance frequency of the cavity

$C_{\text{cavity}}$  = the capacitance of the cavity

$L_{\text{via}}$  = the partial-self-inductance of one via

$n$  = the number of parallel shorting vias

$Len$  = the length of a side of the square cavity

$h$  = the dielectric thickness between the planes of the cavity

$k$  = a constant specific to the via, which includes the effects from the barrel diameter

The value of the constant divided by the factor of  $2\pi$  is for a reason that will become apparent shortly. We assume that the vias are uniformly distributed over the area of the cavity.

From these expressions, we estimate the resonant frequency as

$$f_{\text{res}} = \frac{1}{2\pi} \sqrt{\frac{1}{C_{\text{cavity}} \frac{1}{n} L_{\text{via}}}} = \frac{1}{2\pi} \sqrt{\frac{1}{\epsilon_0 Dk \frac{Len^2}{h} \times \frac{1}{n} \mu_0 \times h \times \left(\frac{k}{2\pi}\right)^2}} = \frac{c}{\sqrt{Dk}} \frac{\sqrt{n}}{Len k} \quad (7.8)$$

If the vias are uniformly distributed over the surface of the cavity, then the spacing between them is roughly given by

$$s_{\text{via-via}} = \frac{Len}{\sqrt{n}} \quad \text{or} \quad Len = s_{\text{via-via}} \times \sqrt{n} \quad (7.9)$$

Replacing the length so that it now is related to the via-to-via spacing, the estimated first cavity resonance is expected at

$$f_{\text{res}} = \frac{c}{\sqrt{Dk}} \frac{\sqrt{n}}{Len k} = \frac{c}{\sqrt{Dk}} \frac{1}{s_{\text{via-via}}} \frac{1}{k} \quad (7.10)$$

For any frequency, we relate the wavelength at that frequency with

$$\lambda_{\text{res}} = \frac{v}{f_{\text{res}}} = \frac{c}{\sqrt{Dk}} \frac{1}{f_{\text{res}}} = k \times s_{\text{via-via}} \quad (7.11)$$

and

$$s_{\text{via-via}} = \frac{1}{k} \lambda_{\text{res}} \quad (7.12)$$

where

$\lambda_{\text{res}}$  = the wavelength of the wave that is in the cavity at the first resonant frequency

$v$  = the speed of the signal in the medium

$c$  = speed of light in air

$Dk$  = the dielectric constant of the material filling the cavity

$f_{\text{res}}$  = the first resonant peak frequency that is not suppressed

$k$  = a constant related to the features of the via

$s_{\text{via-via}}$  = the spacing between the vias

$n$  = the number of parallel shorting vias

$Len$  = the length of a side of the square cavity

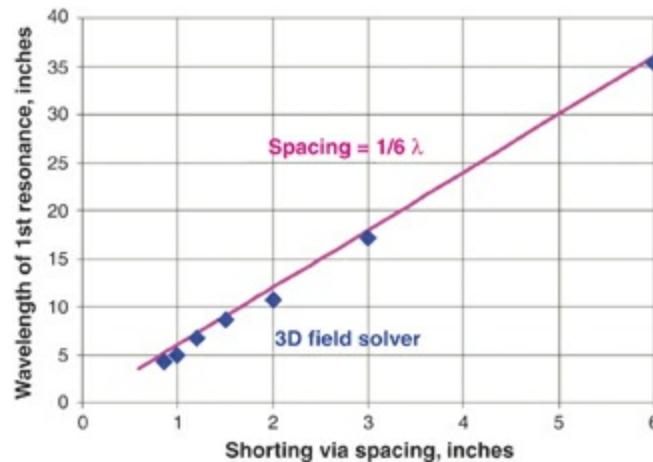
This analysis suggests a simple result. To suppress and eliminate low-frequency cavity resonances so that the first resonant frequency has a wavelength in the cavity less than some value requires a spacing between the vias related to some fraction of that wavelength. Exactly what that fraction is depends on the features of the via, but we can find it from the earlier simulation examples.

#### Tip

The spacing between the vias defines a new boundary condition. The first resonant frequency is when the via-to-via spacing is some fraction of a wavelength, or there are some number of vias per the longest wavelength. To suppress higher frequencies or shorter wavelengths requires a tighter spacing between the vias, which shrinks the longest wavelength allowed in the cavity.

Using a 3D field solver, we find the factor that determines the minimum resonant frequency of the cavity. We explore the connection between via spacing and the wavelength of the first resonant frequency for the earlier example consisting of a 6-inch square cavity, filled with FR4, having a dielectric thickness of 10 mils, and adding multiple shorting vias. Each shorting via has a diameter of 10 mils.

From the earlier simulations, we identify the frequency of the first resonance. We extract and plot the wavelength as the space between the shorting vias decreases. We expect a linear dependence. As the space between the shorting vias decreases, the wavelength of the first resonant peak decreases almost linearly. This is shown in Figure 7.5 along with the empirical fit of  $k = 6$ .



**Figure 7.5** Wavelength of the first resonant peak and the via-to-via spacing, based on the results of a 3D field solver. The line predicts the minimum resonant wavelength is six times the via-to-via spacing. Simulated with Mentor Graphics HyperLynx PI.

As a general rule of thumb, this suggests the use of at least six shorting vias per signal wavelength to suppress the cavity resonances below the frequency that has that wavelength.

**Tip**

To suppress cavity resonances driven by a signal, use a space between shorting vias of 1/6 the minimum wavelength of the signal and keep the vias uniformly distributed over the cavity.

This is a simple and powerful rule of thumb. In the special case of FR4, the speed of a signal is roughly 6 inches/nsec. The minimum spacing between vias to set the first allowed resonant frequency is roughly given by

$$f_{\text{res}}[\text{GHz}] = \frac{6 \text{ inches/nsec}}{\lambda_{\text{res}}} = \frac{6 \text{ inches/nsec}}{6 \times s_{\text{via-via}}[\text{inches}]} = \frac{1}{s_{\text{via-via}}[\text{inches}]} \quad (7.13)$$

and

$$f_{\text{res}}[\text{GHz}] = \frac{1}{s_{\text{via-via}}[\text{inches}]} \quad (7.14)$$

or

$$s_{\text{via-via}}[\text{inches}] = \frac{1}{f_{\text{res}}[\text{GHz}]} \quad (7.15)$$

For a robust design, we always want to push the first resonant frequency beyond the bandwidth of the signals. This leads to the condition

$$\text{BW}_{\text{signal}} = \frac{0.35}{RT_{\text{signal}}[\text{nsec}]} < f_{\text{res}}[\text{GHz}] = \frac{1}{s_{\text{via-via}}[\text{inches}]} \quad (7.16)$$

or

$$s_{\text{via-via}}[\text{inches}] < 3 \times RT[\text{nsec}] \quad (7.17)$$

As the signal edge propagates through an interconnect, its rising (or falling) edge has a spatial extent, given by

$$L_{\text{signal-edge}} = RT \times v = RT \left[ \text{nsec} \right] \times 6 \frac{\text{inch}}{\text{nsec}} \quad (7.18)$$

This condition for the via-to-via spacing, in inches,

less than three times the rise time in nsec, is really a condition for

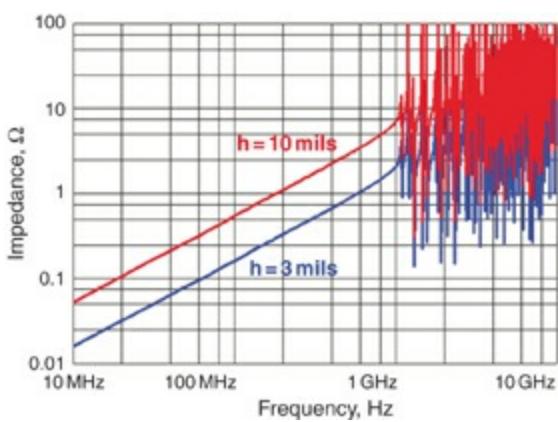
$$s_{\text{via-via}}[\text{inches}] < 3 \times RT[\text{nsec}] = 3 \times \frac{\text{Len}_{\text{signal-edge}}}{6} = \frac{\text{Len}_{\text{signal-edge}}}{2} \quad (7.19)$$

This is the origin of the common rule of thumb, to suppress any cavity resonances at or below the signal bandwidth by adding at least two shorting vias over the spatial extent of the rising edge, distributed uniformly over the cavity.

**Tip**

In the absence of a full-wave simulation, if we need to suppress resonances in a cavity filled with FR4 above a frequency  $f$  in GHz, the maximum spacing between the shorting vias,  $s$ , in inches, should be less than  $1/f$ . This is the same as adding at least two shorting vias across the rising edge of the signal.

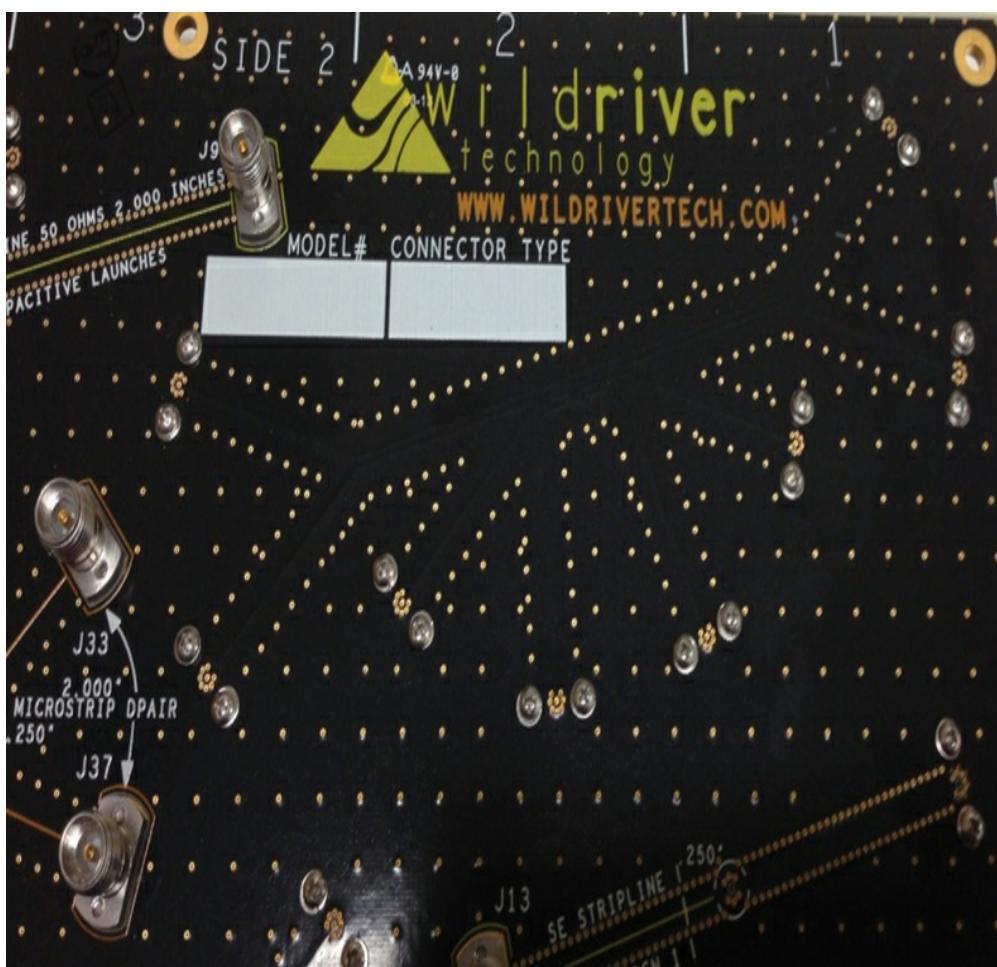
For example, if we need to suppress resonances in a board for all frequencies below 1 GHz, we should space shorting vias no farther than every 1 inch. This spacing is independent of the size of the cavity or the thickness of the dielectric between the planes of the cavity. We tested this basic assumption using a 3D field solver. We spaced an array of vias about 1 inch apart distributed uniformly on two cavities 3 mils thick and 10 mils thick. Figure 7.6 shows the impedance as viewed from one corner of the board.



**Figure 7.6** Simulated impedance profile of a cavity with shorting vias spaced every 1 inch with a cavity thickness of 3 mils and 10 mils. From the rule of thumb, we expect the lowest resonant frequency to be about 1 GHz independent of cavity thickness, and indeed it is. Simulated with Mentor Graphics HyperLynx PI.

Adding closely spaced shorting vias between all the return planes in a board is a common practice to suppress unwanted cavity resonances. This keeps the noise in the cavity low below some upper frequency.

Figure 7.7 shows an example of a test board produced by Wild River Technologies with a variety of spacings between cavity shorting vias. In the general field of the board, the via-to-via spacing is about 0.25 inches, while around some of the structures it is 0.1 inches and in some cases as tight as can be manufactured, with a spacing of 0.04 inches. The vias suppress resonant frequencies up to 4 GHz, 10 GHz, and 25 GHz, respectively.



**Figure 7.7** Example of a high-performance test board developed by Wild River Technologies showing shorting vias to suppress cavity resonances.

The most important condition to enable shorting vias between the planes in the cavity to suppress peak impedances in the cavity resonances is that the two planes of the cavity be the same voltage. This motivates the most robust design rule for signal layer transitions: Always use the same voltage planes as the return planes. Usually Vss or ground planes are used for the signal return planes.

When we follow this rule, all the ground return planes are shorted together with vias spaced apart so there are at least six shorting vias per wavelength of the highest frequency component that is allowed in the cavity. Following this design guideline eliminates high-frequency noise inside the cavity. Of course, it means more ground layers in a board, which means more total

layers in the board and thus higher cost.

**Tip**

The most robust solution for reducing cavity resonances and large induced voltage noise when signals switch through them is to use the same voltage for all return planes. This enables the opportunity to add shorting vias between them spaced apart, in inches, equal to  $1/($ the highest cavity resonant frequency allowed, in GHz $)$ . This usually means using only ground planes as the return planes.

When the two planes that make up a cavity are not the same voltage, we obviously can't add shorting vias between the planes of the cavity. Instead, the best we can do is add DC blocking capacitors between the shorting vias to keep them from shorting the planes. Because the capacitors' mounting inductance is never as low as the shorting via, using capacitors to suppress plane cavity resonances is never as effective as using the same voltage planes and adding shorting vias. Because their application is to provide a DC block, capacitors used in this application should actually be called DC blocking capacitors. Using DC blocking capacitors is always a poor second choice as a solution to suppress plane resonances.

A common argument is that using only ground planes for signal returns is an expensive way to enable the use of shorting vias to reduce the cavity noise. A cheaper proposal is to use a mix of power and ground planes for return current and add DC blocking capacitors instead of shorting vias.

However, as shown in the next section, the number of DC blocking capacitors required to achieve the same cavity resonance suppression is very large and also results in a more expensive product.

**Tip**

Reducing the cavity noise when signals change return planes costs money. You can decide whether you want to spend the money on more ground layers or on more DC blocking capacitors.

Of course, routing high-speed signals with bandwidths in excess of 1 GHz as differential pairs is a more common practice. Differential signals excite a cavity resonance much less than a single-ended or a common signal. This is because the power planes carry all the return current for single-ended signals. The signal current goes through the via but the return current injects noise into the cavity. For differential signals, the return current of each line in the pair overlaps in the cavity and being of opposite circulation direction, cancels out. With no net return current in the cavity, there is no voltage drop across the cavity impedance and no induced cavity noise.

When the differential signal vias are tightly coupled in the cavity, the noise injected into a cavity can easily be lower than  $-80$  dB for a comparable single-ended signal. This means the problem of exciting cavity resonances can be much less of an issue with differential signals.

However, any common signal component traveling through the differential vias excites the cavity resonances just as much as a single-ended signal. Because of the inevitable common signal components, we should take care to engineer the cavity impedance for differential signals just as for single-ended signals. Any source of asymmetry between the p line and the n line will convert some of the differential signal into the common signal. The most common source of mode conversion is skew either in the driver or the interconnects.

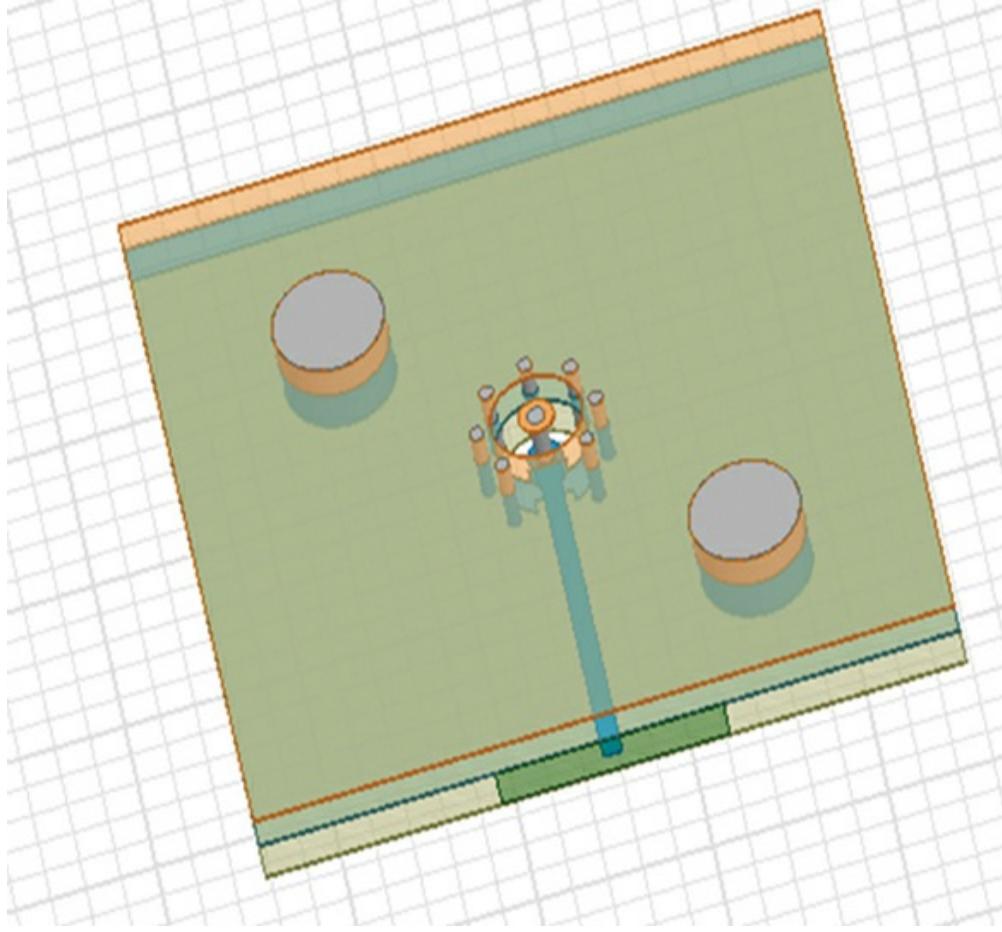
### Tip

Differential signals passing through a cavity do not excite the cavity resonances nearly as much as single-ended signals. However, the inevitable common signal components excite the cavity resonances. This is why you should take care to engineer the return planes for differential pairs just as much as for single-ended signals.

An alternative guideline exists in selecting shorting vias when signals transition same-voltage planes that make up a cavity. With no shorting vias, the return current sees the impedance of the cavity. All the return current couples into the cavity and generates long-range cavity noise.

If the signal-return path looks like a coax geometry, there will be no external magnetic fields outside the coax and no coupling of the return current into the cavity modes. There will be no long-range noise induced in the cavity in this case.

This suggests that one method of minimizing the current noise from coupling into a cavity mode is to add return vias in close proximity to the signal via that makes the geometry look like a coax. The more signal-return paths look like a coax geometry, the less coupling of the signal-return current of the via into the cavity modes and the less cavity noise generated. [Figure 7.8](#) is an example of the footprint recommended by many connector vendors for a high-bandwidth surface mount 2.92 mm rf connector connecting to a buried stripline trace in the board. The seven shorting vias make the structure look like a mini-coax interconnect. This prevents coupling into the cavity modes.



**Figure 7.8** Typical shorting via arrangement around a signal via to make the transition to the buried stripline trace look like a coax so that no return currents are coupled into the cavity modes. Figure courtesy of Molex Corp.

When adding seven return vias in proximity to a signal via is not practical, then we should use as many as practical. The more the transition looks like a coax, the less coupling into the cavity mode.

**Tip**

As a good habit, add at least one return via for each signal via that transitions. This helps minimize the noise current injected into the cavity. In the absence of a 3D field solver analysis including the specifics of number of vias, spacings, orientation, and cavity thickness and dimensions, there are no good approximations for the signal-to-cavity coupled noise.

## 7.5 SUPPRESSING CAVITY RESONANCES WITH MANY DC BLOCKING CAPACITORS

When the planes are not the same voltage, a common

recommendation is to short the planes with capacitors. The most important metric of the capacitors for this application is their mounting inductance. We should select the capacitors for a body size with a mounting inductance as small as practical. The capacitance value of the capacitors is almost irrelevant.

We are really using these capacitors as a substitute for shorting vias. The capacitors are there as a DC block, rather than to “decouple” anything. When used in this application they should be called DC blocking capacitors. Their function is to reduce the impedance of the cavity, which reduces the voltage noise in the cavity and the via-to-via cross talk when signals transition through the cavity.

**Tip**

DC blocking capacitors make poor shorting vias. Their capacitance is almost irrelevant. Their total mounting loop inductance determines their performance.

In general, a capacitance value larger than 100 nF is usually sufficient. Having a self-resonant frequency well below the lowest cavity resonance is just important. With a typical mounting inductance, approximately 2 nH, the self-resonant frequency of a collection of 100 nF capacitors is

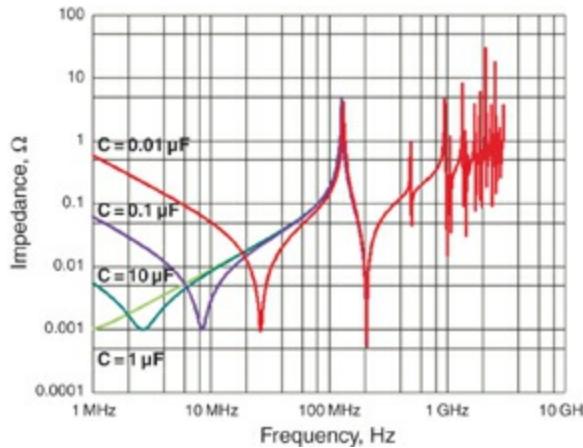
$$\text{SRF} = \frac{1}{2\pi\sqrt{LC}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{mounting}}[\text{nH}]C[\text{nF}]}} = \frac{159 \text{ MHz}}{\sqrt{2\text{nH} \times 100 \text{nF}}} = 11 \text{ MHz} \quad (7.20)$$

Above this frequency, the impedance of each capacitor is inductive, just like a shorting via. As long as the DC blocking capacitor looks inductive in the region of cavity resonances, it will act like a shorting via and suppress cavity resonances in the same way.

In this example, the capacitors look inductive in the

cavity above 11 MHz. Capacitor values larger than 100 nF still look inductive in the frequency range where cavity resonances occur.

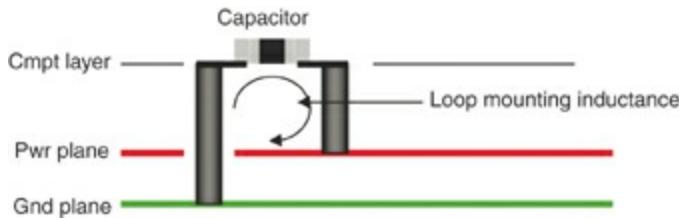
The VRM and bulk capacitors usually provide a low impedance between a power and ground plane cavity at low frequency. [Figure 7.9](#) shows the impedance profile for a cavity with 25 similar capacitors distributed over its surface, each with 2 nH of mounting inductance. Four impedance curves are shown with capacitance values of 10 nF, 100 nF, 1  $\mu$ F, and 10  $\mu$ F each. The ability to suppress the cavity resonances is identical for all capacitor values. For now, the ESRs of each capacitor is 25 m $\Omega$ . With 25 capacitors in parallel, the effective ESR at the self-resonant frequency is  $1/25 \times 25$  m $\Omega$  or 1 m $\Omega$ . A later section of this chapter considers the impact from the capacitor ESR.



**Figure 7.9** Impedance profile for a cavity 6 inches  $\times$  6 inches, with 25 identical capacitors uniformly distributed over the surface, for four different values of capacitance, from 10 nF to 10  $\mu$ F and ESL of 2 nH. The value of the capacitance has no impact on the cavity impedance profile above the self-resonant frequency.

Although the capacitance of the distributed DC blocking capacitors does not affect the cavity resonances, their inductance does. The mounting inductance of the capacitors to the cavity is the most important metric in determining cavity resonance

suppression. The capacitors are there to block DC current, not to act as decoupling capacitors. Figure 7.10 shows how a capacitor typically is mounted to a cavity and the origin of its mounting inductance.



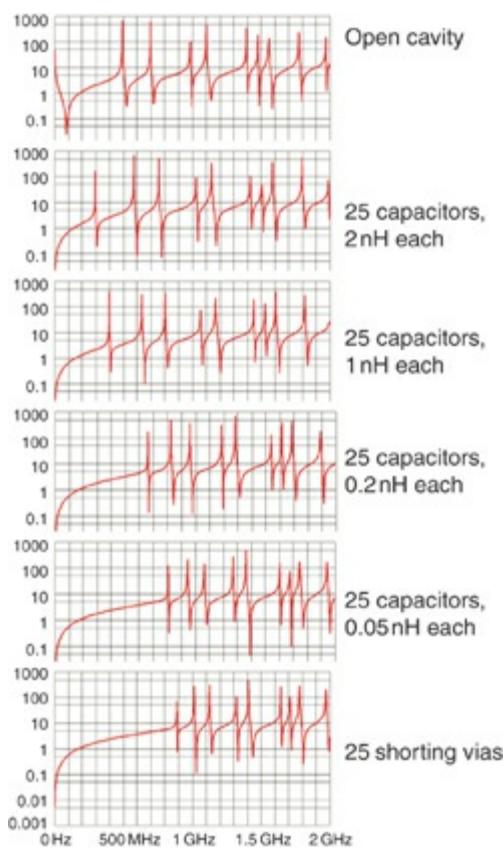
**Figure 7.10** Illustration of the contribution of the via inductance between the two planes and the loop mounting inductance of the rest of the vias to the capacitor on the component layer of the circuit board.

The higher mounting inductance of a capacitor compared to a single shorting via dramatically reduces the effectiveness of a capacitor in shorting the cavity and suppressing plane resonances.

**Tip**

Although a DC blocking capacitor provides low impedance across a cavity, its mounting inductance is always much higher than just a single shorting via. This means DC blocking capacitors are never as effective as shorting vias in suppressing cavity resonances.

Figure 7.11 shows the impedance profile for the same 6-inch square 10 mil cavity as earlier but with 25 capacitors distributed uniformly with various mounting inductances instead of shorting vias. We assume that the capacitance is large enough so that the self-resonant frequency of the capacitor is low. For the 10 mil cavity, the mounting inductance must be less than about 50 pH, which is comparable to the via-only inductance to suppress the cavity modes as effectively as shorting vias. The frequency at which cavity resonances are suppressed depends on the mounting inductance of the capacitors.



**Figure 7.11** Impedance viewed from a corner of a 6 inch on a side cavity 10 mil thick with various capacitor configurations. The major trend is that the cavity modal resonances move to higher frequency as we reduce the inductance of the mounted capacitors. Simulated with Mentor Graphics HyperLynx PI.

## 7.6 ESTIMATING THE NUMBER OF DC BLOCKING CAPACITORS TO SUPPRESS CAVITY RESONANCES

For the capacitors to be as effective as the direct shorting vias, more capacitors are required in proportion to the ratio of mounted capacitor inductance to shorting via inductance. In a square array, the spacing between the capacitors decreases with the square root of the number of capacitors  $n$ . If we use DC blocking capacitors to suppress the cavity resonances, we would need a closer spacing than for shorting vias.

We can estimate the number of capacitors required. The total inductance of the DC blocking capacitor is broken into a mounting inductance plus the via inductance. The total loop inductance to the cavity is

$$L_{\text{blocking\_cap}} = L_{\text{mount}} + L_{\text{via}} \quad (7.21)$$

where

$L_{\text{blocking\_cap}}$  = the total loop inductance of the capacitor with the planes of the cavity

$L_{\text{mount}}$  = the extra loop inductance of the mounting geometry of the capacitor

$L_{\text{via}}$  = the total inductance of a single via, equivalent to a via shorting the cavity

To first order, we assume that the total inductance of a via shorting the cavity is roughly linear with the cavity thickness,  $h$ :

$$L_{\text{via}} = h \times L_{\text{Len-via}} \quad (7.22)$$

where

$L_{\text{via}}$  = the total inductance of a via shorting the cavity

$h$  = the cavity thickness

$L_{\text{Len-via}}$  = the total inductance per length of a via shorting the cavity

We get the number of capacitors required in parallel to have the same equivalent inductance as one via directly shorting the plane with

$$L_{\text{via}} = \frac{1}{n_{\text{caps}}} L_{\text{blocking\_cap}} \quad (7.23)$$

and

$$n_{\text{caps}} = \frac{L_{\text{blocking\_cap}}}{L_{\text{via}}} = \frac{L_{\text{mount}} + h \times L_{\text{Len-via}}}{h \times L_{\text{Len-via}}} = \frac{L_{\text{mount}}}{h \times L_{\text{Len-via}}} + 1 \quad (7.24)$$

where

$n_{\text{caps}}$  = the number of capacitors needed in parallel to have the same loop inductance as one shorting via for the equivalent suppression of cavity

resonances.

The equivalent spacing between capacitors scales inversely with the square root of the number of capacitors needed per shorting via. This results in an estimate of the spacing of capacitors required to suppress cavity resonances as

$$\frac{s_{\text{vias}}}{s_{\text{caps}}} = \sqrt{n_{\text{caps}}} = \sqrt{\frac{L_{\text{mount}}}{h \times L_{\text{Len-via}}} + 1} \quad (7.25)$$

Using as the maximum spacing for vias of  $1/6$  wavelength, the maximum DC blocking capacitor spacing is

$$s_{\text{caps}} = \frac{s_{\text{vias}}}{\sqrt{\frac{L_{\text{mount}}}{h \times L_{\text{Len-via}}} + 1}} = \frac{1}{\sqrt{\frac{L_{\text{mount}}}{h \times L_{\text{Len-via}}} + 1}} \times \frac{1}{6} \lambda \quad (7.26)$$

This analysis demonstrates that using capacitors to suppress cavity resonances always requires a closer spacing to get the equivalent frequency suppression compared with just vias. The larger the mounting inductance, the smaller the spacing between the capacitors required for the same suppression frequency.

Counterintuitively, the thicker the distance between the planes in the cavity, the more effective the capacitors apparently become, approaching the effectiveness of just the shorting vias. This is because a thicker cavity means a larger total inductance of the via. If the mounting inductance stays the same, fewer additional capacitors in parallel are needed to match the total inductance of just a via. Capacitors are never as good as shorting vias but with a thicker cavity the capacitors' effectiveness approaches that of just a shorting via. Of course, thicker cavities mean less effectiveness of damping, and more spreading

inductance in the cavity, so thicker cavities are never a good design step to take on purpose.

**Tip**

As with most applications of capacitors in the PDN, the most important quality that influences their effectiveness in suppressing cavity resonances is not their capacitance, but their mounting loop inductance. You should do everything practical to reduce the mounting inductance for DC blocking capacitors.

A few examples illustrate the importance of low mounting inductance DC blocking capacitors to suppress cavity resonances. The mounting inductance usually dominates over the capacitor intrinsic inductance when the body size is 0402 or smaller. We consider four specific values for the mounting inductance of a DC blocking capacitor:

Ultimate best 0.2 nH

Best practical 0.5 nH

Well engineered 1.0 nH

Typical 2.0 nH

From the loop inductance of the mounting of the capacitor, we estimate the spacing between the capacitors required to give the same cavity mode suppression as just the shorting vias only.

In the following examples, we assume the cavity thickness is 10 mils and calculate the spacing between DC blocking capacitors required to match the same cavity resonance suppression as shorting vias. We expect that for smaller capacitor mounting inductance, the spacing between capacitors will approach the  $1/6 \lambda$  spacing required for shorting vias.

In the ultimate best case, the mounting inductance of a capacitor is as small as 0.2 nH. The mobile computing industry may achieve this with 0201 capacitors mounted

on power planes close to the surface of a board made with buildup layers. The total inductance of a via shorting out a cavity 10 mils thick is as low as 0.1 nH. In this case, the required spacing between DC blocking capacitors is about

$$s_{\text{caps}} = \frac{s_{\text{vias}}}{\sqrt{\frac{L_{\text{mount}}}{h \times L_{\text{perLen}}} + 1}} = \frac{1}{\sqrt{\frac{0.2}{0.1} + 1}} \times \frac{1}{6} \lambda = \frac{1}{\sqrt{3}} \times \frac{1}{6} \lambda \sim \frac{1}{10} \lambda \quad (7.27)$$

Applying this analysis to the other mounting inductances, the spacing between capacitors to suppress cavity modes is

Quality of case	Capacitor mounting inductance	$s_{\text{cap}}$
Ultimate best	0.2 nH	$\lambda/10$
Best practical	0.5 nH	$\lambda/15$
Well engineered	1.0 nH	$\lambda/20$
Typical	2.0 nH	$\lambda/42$

In the typical case of a mounting inductance of 2 nH, the capacitor-to-capacitor spacing would have to be  $1/42$  of a wavelength. This is a factor of seven times closer than with just the shorting vias. This is a factor of 50 times more DC blocking capacitors needed compared with just shorting vias. This is a lot of capacitors!

If suppressing cavity resonances below 1 GHz, which has a wavelength in FR4 of 6 inches is important, then it requires a spacing between capacitors of  $1/42 \times 6$  inches = 150 mils. This is 7 capacitors per linear inch or about 50 capacitors per square inch of board space. For a board 10 inches on a side, as many as  $50 \times 100$  capacitors or nearly 5,000 capacitors would be needed! This is just not practical.

Extremely low mounting inductance for the capacitors is required to keep the number of caps within reason. This is why the effectiveness of DC blocking capacitors at suppressing plane resonances is way overrated. Using

only grounds as return planes and shorting vias between the planes is far more effective.

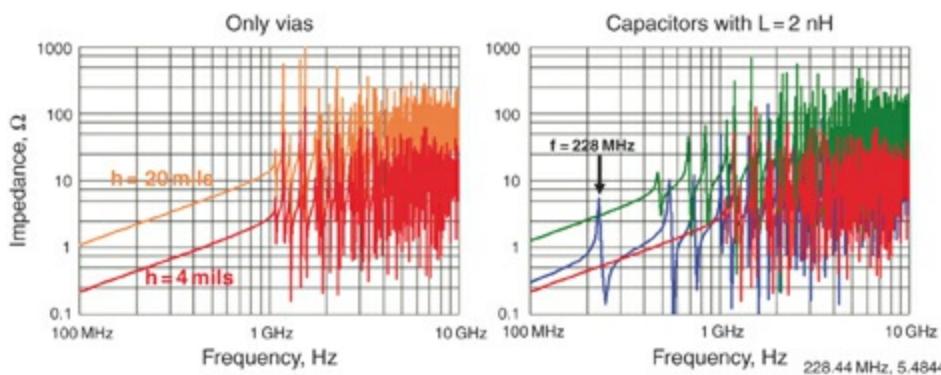
**Tip**

The most effective way of suppressing plane resonances is by using the same voltage for each plane and adding shorting vias between the planes. DC blocking capacitors cannot come close to the effectiveness of a shorting via. Whenever possible, always use the same voltage return planes.

We compared the DC blocking capacitors and shorting vias in a 3D field solver. In this example we spaced shorting vias or capacitors 1 inch apart on two cavities, one with a dielectric thickness of 4 mils and the other with a dielectric thickness of 20 mils. The mounting inductance of the DC blocking capacitors is 2 nH.

We expect the lowest resonant frequency for shorting vias to be 1 GHz based on a spacing of 1 inch. The lowest resonant frequency with the same density of capacitors is about seven times lower or 140 MHz.

With shorting vias, we expect no difference in the lowest cavity resonance when the cavity thickness is 4 mils or 20 mils thick. However, we expect a lower cavity resonance frequency with the 2 nH capacitors. This is very close to what we observed in the 3D simulation shown in Figure 7.12.



**Figure 7.12** Left: Impedance profile of two cavities 4 mils and 20 mils thick with shorting vias spaced 1 inch apart. Right: The lowest impedance plot is for the case of 4 mils thick cavity and shorting vias, included for reference. The next higher impedance traces are for a 4 mil and 20 mil thick cavity with DC blocking capacitors replacing the shorting vias.

On the 4-mil-thick cavity, we expect the lowest resonant frequency with the capacitors to be about 140 MHz. The 3D simulation shows the first resonance as 228 MHz. We estimate a lower frequency, which is about  $0.228 \text{ GHz}/1.08 \text{ GHz} = 1/5$ , close to the estimate of  $1/7$  from our simple analysis. As the cavity thickness increases, the lowest resonant frequency for the case of the DC blocking capacitors increases, exactly as expected even though the lowest frequency resonance for the case of just shorting vias did not change with thicker cavity. We include the case of the cavity impedance with just vias in this plot for comparison.

This comparison confirms that using capacitors to suppress plane resonances is not very effective unless the mounting inductance of the capacitors is extremely low. Even a well-engineered mounting inductance of 1 nH requires capacitor spacings of about  $1/20$  a wavelength.

**Tip**

DC blocking capacitors are not effective at suppressing plane resonances unless their mounting inductance is kept extremely low. In typical well-engineered situations, a spacing of 1/20 a wavelength might be required for capacitors to be effective at suppressing plane resonances.

In this analysis we attempted to push the peak impedances from the cavity resonances to a frequency above the bandwidth of the signals. This way, if transient currents exist in the cavity from switching return currents, there are no peak impedances to create excessive voltage noise. This is an especially important problem in minimizing electromagnetic emissions from cavities.

**Tip**

The estimate based on this simple analysis is a good approximation to the result from the 3D simulation. They both indicate a need for more DC blocking capacitors to push the first cavity modal resonance to higher frequency. In the absence of a 3D full-wave simulation or even a simple estimate, more capacitors result in lower risk.

From the analysis in this section, we see we can push the first peak impedance frequency higher than the signal bandwidth when the capacitor spacing for a 1 nH mounting inductance is closer than 1/20 a wavelength. The first resonance is

$$f_{\text{res}} = \frac{v}{\lambda} = \frac{c}{\sqrt{Dk} \times 20 \times s_{\text{cap}}} = \frac{11.8}{\sqrt{4 \times 20 \times s_{\text{cap}}}} = \frac{0.3}{s_{\text{cap}}[\text{inches}]} \text{ GHz} \quad (7.28)$$

If we require this first resonant frequency to be above the bandwidth of the signal, then

$$\text{BW} < f_{\text{res}} \text{ and } \frac{0.35}{RT[\text{nsec}]} < \frac{0.3}{s_{\text{cap}}[\text{inches}]} \text{ or } s_{\text{cap}}[\text{inches}] < RT[\text{nsec}] \quad (7.29)$$

And, the density of capacitors required to push the

first resonant frequency above the bandwidth of the signal is

$$\text{density}_{\text{cap}}[\text{per sq inch}] = \frac{1}{s_{\text{cap}}^2[\text{inches}]} = \frac{1}{RT^2[\text{nsec}]} \quad (7.30)$$

For example, if the rise time is 1 nsec, we need 1 DC blocking cap per square inch to suppress cavity resonance to a frequency above the signal bandwidth. If the rise time of signals is 0.3 nsec, we require about 10 capacitors per square inch.

## 7.7 DETERMINING HOW MANY DC BLOCKING CAPACITORS ARE NEEDED TO CARRY RETURN CURRENT

The previous section considered the number of DC blocking capacitors required to suppress cavity resonances above the signal bandwidth. A second consideration is the cavity noise generated when multiple single-ended signals pass through it. The shorting vias (in the case of same voltage planes) and the DC blocking caps (in the case of different voltage planes) must carry the return current. We can calculate the number of return paths required to support multiple signals from plane bounce and noise considerations.

We estimate the minimum number of capacitors required to keep the switching noise in the cavity below some level when the return currents for many signals transition through the cavity. The voltage noise is generated when the  $dI/dt$  of the return current from many signals transition through the equivalent inductance of the cavity. We estimate this based on

$$V_{\text{noise}} = L_{\text{equiv}} \frac{dI}{dt} \quad (7.31)$$

and

$$\frac{dI}{dt} = n_{sig} \times \frac{V_{sig}}{Z_0} \times \frac{1}{RT} \quad (7.32)$$

and

$$L_{equiv} = \frac{1}{n_{caps}} ESL \quad (7.33)$$

which results in

$$V_{noise} = L_{equiv} \frac{dI}{dt} = \frac{1}{n_{caps}} ESL \times n_{sig} \times \frac{V_{sig}}{Z_0} \times \frac{1}{RT} \quad (7.34)$$

and

$$\frac{V_{noise}}{V_{sig}} = \frac{n_{sig}}{n_{caps}} \times \frac{ESL}{Z_0 RT} \quad (7.35)$$

or

$$\frac{n_{sig}}{n_{caps}} = \frac{V_{noise}}{V_{sig}} \frac{Z_0 RT}{ESL} \quad (7.36)$$

where

$n_{sig}$  = the number of signals passing through a cavity

$n_{caps}$  = the number of capacitors used between the power and ground planes

$V_{noise}$  = the voltage noise in the cavity

$V_{sig}$  = the voltage of the signal

$Z_0$  = the characteristic impedance of the signal environment

$RT$  = the rise time of the signal

$ESL$  = the equivalent series mounting inductance of each capacitor

Suppose a maximum plane bounce noise of 10% is allowed for  $50 \Omega$  single-ended signals. Well-engineered DC blocking capacitors with an  $ESL$  of  $1 \text{ nH}$  are to carry the return current. The maximum ratio of signal vias to

blocking capacitors is roughly

$$C_{cavity} = \epsilon_0 Dk \frac{A}{h} = 0.225 \times 4.3 \frac{5 \times 5}{0.002} = 12 \text{ nF} \quad (7.51)$$

If the rise time is 0.5 nsec, the number of signals that can share each capacitor is about  $5 \times 0.5 = 2.5$  signal vias per DC blocking capacitor. Every two and a half signals require their own DC blocking capacitor. We can only reduce the number of capacitors by reducing the ESL of each capacitor.

**Tip**

The second criterion for determining the number of DC blocking capacitors is based on the equivalent parallel inductance of cavity impedance. It must be kept low enough so that the dI/dt plane bounce due to the switching signal edges is acceptable.

A typical mounting inductance of 2.0 nH requires the number of DC blocking capacitors to double to keep the plane bounce noise below 10%. Signals with 0.5 nsec rise time require their own DC blocking capacitor.

The density ratio for the number of signals per DC blocking cap is

$$\frac{\text{density}_{\text{sig}}}{\text{density}_{\text{caps}}} = \frac{n_{\text{sig}}}{n_{\text{caps}}} = 5 \times RT[\text{nsec}] \quad \text{or} \quad d_{\text{caps}} = d_{\text{sig}} \frac{1}{5 \times RT[\text{nsec}]} \quad (7.38)$$

where

$\text{density}_{\text{sig}}$  = the density of signal vias on the board

$\text{density}_{\text{caps}}$  = the density of DC blocking capacitors on the board for acceptable plane bounce

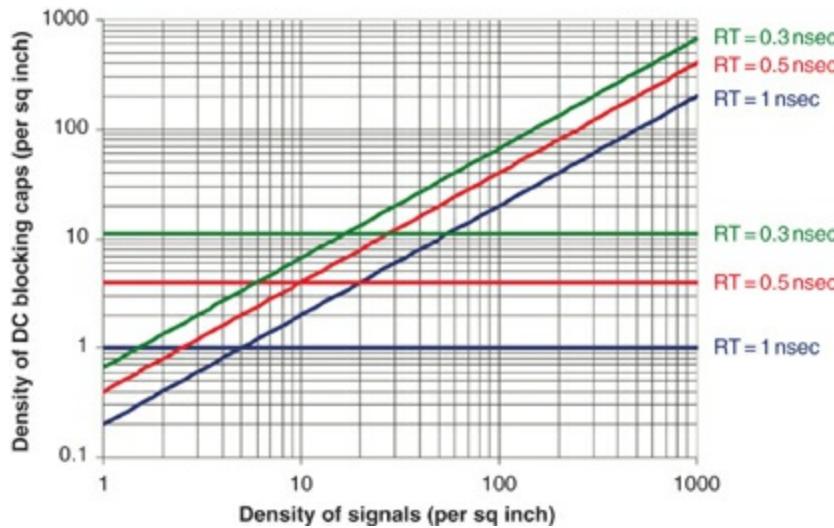
Preventing cavity resonances and dI/dt plane bounce is important. The density of capacitors should be the higher of the two requirements:

$$\text{density}_{\text{caps-returnCurrent}} = \text{density}_{\text{sig}} \frac{1}{5 \times RT[\text{nsec}]} \quad (7.39)$$

and

$$\text{density}_{\text{cap-cavity Resonance}} = \frac{1}{RT^2[\text{nsec}]} \quad (7.40)$$

In Figure 7.13, we plot the density of DC blocking capacitors required for both the requirements of pushing the first cavity resonant frequency above the bandwidth of the signal and to keep the plane bounce noise below 10%. We explore three different rise times, 1 nsec, 0.5 nsec, and 0.3 nsec.



**Figure 7.13** Comparing the minimum DC blocking capacitor density required based on two different criteria, pushing the cavity resonances above the bandwidth of signals (horizontal lines), and ensuring a low enough cavity inductance to keep the switching noise below 10% (slanted lines). Always use the larger of the two estimates.

When the rise time is 0.3 nsec and the capacitor mounting inductance is 1 nH, the minimum DC blocking capacitor density is 10 per square inch from a cavity resonance perspective. If the signal via density is more than about 20 per square inch, the DC blocking capacitor density should increase proportionally to signal-via density.

A board 5 inches  $\times$  5 inches requires a total of  $25 \times 15 = 375$  capacitors, each engineered with a mounting

inductance of less than 1 nH. This is a very expensive solution.

When differential signals are used, the net  $dI/dt$  through the cavity is ideally 0 and there is no noise in the cavity, regardless of the cavity impedance. One might think that this eliminates the need for DC blocking capacitors.

However, some common signal always exists along with the differential signal. The common signal is typically below 10% of the differential signal component in a well-engineered system. This significantly reduces the amount of net return current flowing through the cavity. On the other hand, differential signals also typically operate with much higher bandwidths and shorter rise times than single-ended signals.

In PCI-express gen III the data rate is 8 Gbps and the unit interval is 125 psec. The rise time is typically less than 50 psec. For a robust design, we should suppress cavity modes below the signal bandwidth. If different voltage planes make up the cavity, DC blocking capacitors are the only way of pushing the cavity resonances higher. This requires a DC blocking capacitor density of at least

$$\text{density}_{\text{cap-cavity Resonance}} = \frac{1}{RT^2[\text{nsec}]} = \frac{1}{0.05^2} = 400 \text{ per sq inch} \quad (7.41)$$

This is an impracticable density of DC blocking capacitors. Using adjacent planes with the same voltage is much better so that return vias suppress cavity resonances.

For differential signals, the amount of cavity noise generated depends on manufacturing asymmetries, which create mode conversion. Predicting this in a simulation is difficult. Unless asymmetries are purposefully added to the interconnect geometry,

simulations will not show common signal and will not identify the cavity noise as a potential problem. This can be very misleading.

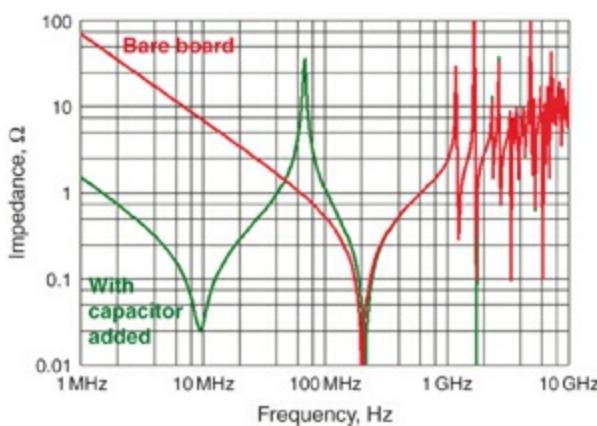
**Tip**

The bandwidth of differential signals is often so high as to require an unreasonable number of DC blocking capacitors. This is why the most effective way to manage cavity resonances is to use the same voltage planes for the return paths and add shorting vias.

## 7.8 CAVITY IMPEDANCE WITH A SUBOPTIMAL NUMBER OF DC BLOCKING CAPACITORS

Regardless of the number of DC blocking capacitors used, there will be peak impedances in the cavity's impedance profile, usually in a frequency range that overlaps signal bandwidth, when a cavity cannot use shorting vias and the required number of DC blocking capacitors is not affordable. These peaks will be a dominant noise source and contribute to signal cross talk and EMC problems.

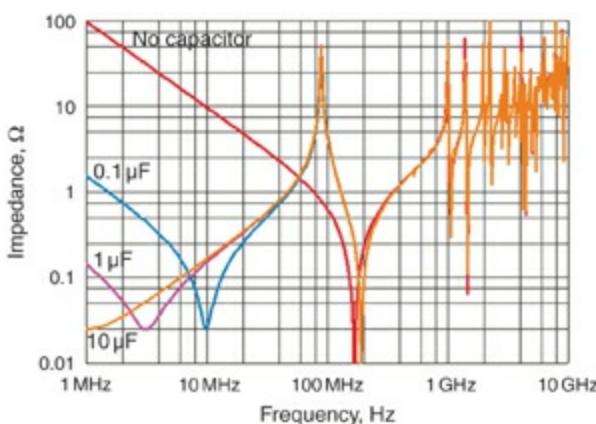
When we add a single capacitor to a cavity, the impedance profile is different from that of the bare board. [Figure 7.14](#) shows an example of a single 100 nF capacitor with 2 nH ESL and 28 mΩ ESR added to a cavity. This creates new features in the impedance profile.



**Figure 7.14** Impedance profile of a cavity with a 100 nF capacitor added to the cavity having a mounting inductance of ESL = 2 nH. Simulated with Mentor Graphics HyperLynx PI.

At low frequency, the capacitance of the added capacitor dominates the cavity impedance. Above the capacitor's self-resonance frequency, the impedance of the cavity is determined by the capacitor's mounted inductance plus spreading inductance and the cavity's capacitance.

If the capacitor's capacitance changes but its mounting inductance does not, the impedance above the capacitors self-resonant frequency is the same for all capacitor values. Figure 7.15 shows an example of the impedance at a central location for three different capacitor values but the same mounting inductance and ESR. Above the self-resonant frequency, the impedance profiles are the same.



**Figure 7.15** Impedance profile of the bare board with three different capacitors added, each with the same mounting inductance and ESR, but with successively higher capacitance. Note that above the SRF of the capacitor, the impedance profiles are identical. Simulated with Mentor Graphics HyperLynx PI.

The first dip in impedance is the self-resonant frequency of the mounted capacitor. This frequency is determined by the capacitance of the capacitor and the series combination of the mounted inductance of the capacitor to the cavity and the spreading inductance from the observation point to the capacitor.

Above the capacitor's self-resonant frequency, the impedance goes up from the capacitor's mounted inductance plus the spreading inductance.

#### Tip

Above the self-resonant frequency of the capacitor, the impedance profile is independent of the capacitance value added to the cavity. It depends on the capacitor's mounting inductance and spreading inductance. The value of the capacitance of the capacitor added to the plane has a second- or third-order importance compared to the mounting inductance of the capacitor.

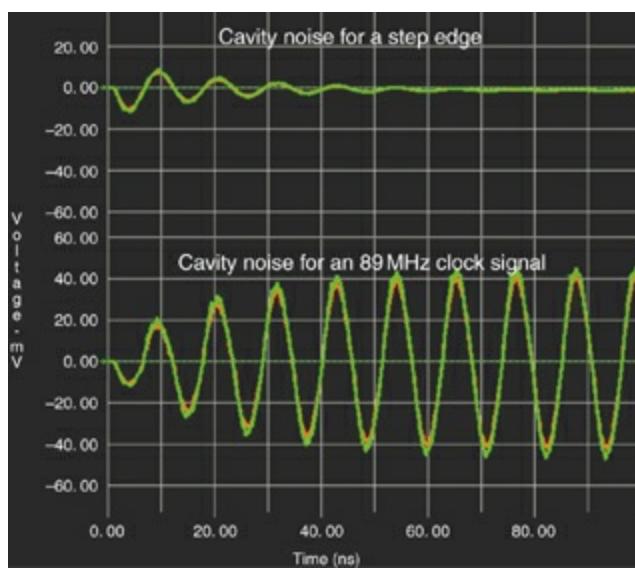
This new peak, created by the mounted capacitor, is in addition to the cavity modal resonant peaks and it is at a relatively low frequency. Cavity currents with frequency components near the parallel resonant frequency, about 89 MHz in this example, see a very high impedance and

can generate a lot of voltage noise.

For example, a 6 mA, 0.4 nsec rise time signal flows through a signal via with return current on the two cavity planes. The return current excites all the peak frequencies below its bandwidth, about 1 GHz. The step edge excites only the impedance peaks below 1 GHz, in this case the one at 89 MHz. We expect to see ringing in the cavity voltage noise at 89 MHz, decaying away with the q-factor of this parallel peak impedance.

A clock signal at 89 MHz would strongly drive the cavity resonance at 89 MHz and generate even higher voltages in the cavity. Because this frequency is below the cavity modal frequencies, the entire cavity bounces together and the noise is the same everywhere in the cavity. Other vias passing anywhere through the cavity see the same voltage noise between the cavity planes as cross talk or noise.

Figure 7.16 is an example of the simulated voltage noise between the two planes of the cavity measured between two opposite points on each of the planes. Simulation results are shown for the two cases: a 0.4 nsec step edge and an 89 MHz square wave of 6 mA of current flowing through the cavity. After a few cycles, the voltage noise in the cavity builds up to almost 90 mV peak to peak. The figure also shows the voltage between two planes in the cavity measured at two very separate locations, and no difference exists.



**Figure 7.16** Voltage noise induced between the two planes of a cavity when a 6 mA step edge of current passes through the cavity and when the signal is an 89 MHz clock. The noise in the cavity is as large as 90 mV peak to peak. Simulated with Mentor Graphics HyperLynx PI.

#### Tip

This suggests that the most important design principle to suppress cavity noise induced by transient currents is to reduce the peak impedances of the cavity as viewed at any location in the cavity. The peak impedances generate the large voltages that appear as noise and cross talk.

The cause of the peak impedance has nothing to do with the amount of capacitance in the capacitor. It has everything to do with the parallel resonance of the capacitors' mounted and spreading inductance and the cavity's capacitance. Once again, the most important way to reduce the peak height is to reduce the mounted inductance of the capacitor and the spreading inductance to the plane capacitance. Upcoming sections cover other ways to engineer lower peak heights as well.

## 7.9 SPREADING INDUCTANCE AND CAPACITOR MOUNTING INDUCTANCE

The frequency of the parallel resonant peak when we add identical capacitors to a cavity depends on the

effective inductance of the capacitors and the capacitance of the cavity. These terms are

$$L_{\text{caps}} = \frac{1}{n} (ESL + L_{\text{spread}}) \quad (7.42)$$

The cavity capacitance is

$$C_{\text{cavity}} = \epsilon_0 Dk \frac{A}{h} \quad (7.43)$$

The parallel resonant frequency is

$$f_{\text{PRF}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{caps}} C_{\text{cavity}}}} = \frac{1}{2\pi} \frac{1}{\sqrt{\left(\frac{1}{n} (ESL + L_{\text{spread}})\right) \times \epsilon_0 Dk \frac{A}{h}}} \quad (7.44)$$

where

$L_{\text{caps}}$  = the effective inductance of all the capacitors in parallel

$n$  = number of capacitors in parallel

$ESL$  = the mounting inductance of each capacitor

$L_{\text{spread}}$  = the spreading inductance in the cavity, on the order of 1 square of sheet inductance

$C_{\text{cavity}}$  = the capacitance of the cavity

$\epsilon_0$  = the permittivity of free space, 0.225 pF/inch

$Dk$  = the dielectric constant of the material filling the cavity

$A$  = the overlap surface area of the planes that make up the cavity

$h$  = the dielectric thickness between the planes that make up the cavity

This identifies the important terms that influence the parallel resonant frequency. If the parallel resonant frequency is pushed above the bandwidth of the signals, the cavity impedance looks inductive at frequency components of the current. We estimate the return

bounce from the cavity from the effective inductance of the cavity and the total  $dI/dt$  of the switching return currents. We can estimate how many capacitors we need based on the maximum allowed return bounce induced cavity noise. See [section 7.7](#) for the analysis.

[Equations 7.42](#) and [7.43](#) point out the most important design guidelines to push the parallel resonant frequency higher while not degrading other aspects of the impedance profile:

- Engineer a low ESL for each mounted capacitor
- Use multiple capacitors in parallel
- Use as small a size cavity with as low a capacitance as practical

Reducing the ESL of each mounted capacitor and the cavity-spreading inductance with thinner dielectric is important to reduce the parallel resonant peak impedance and push it to higher frequency. Even though thinner dielectric in the cavity increases the cavity capacitance, the other advantages from lower spreading inductance and damping of modal resonances outweigh the higher capacitance.

**Tip**

Do everything possible to engineer a lower mounting inductance of the capacitors. This pushes the parallel resonant frequency higher, reduces the inductance, which generates return bounce noise in the cavity, and reduces the impedance at the peaks.

Whether to use a larger or smaller cavity is a tradeoff. A larger cavity has more capacitance, which results in lower parallel resonant peak impedance heights, but also lower parallel resonant peak frequencies and lower cavity modal frequencies. A smaller cavity has higher parallel resonant frequencies but also higher parallel resonance peak impedances.

Generally, the size of the cavity to use is not a choice. In smaller form factor products, the cavity size is small. In large form factor products, some planes cover the entire board and other planes localize as “power puddles.” Planes in the cavity that carry return current should be continuous so that return currents do not cross the boundaries of the planes. Otherwise, additional switching noise is introduced.

After following these design guidelines, the last feature to reduce the peak heights is damping, as discussed in the next section.

## **7.10 USING DAMPING TO SUPPRESS PARALLEL RESONANT PEAKS CREATED BY A FEW CAPACITORS**

One of the most effective ways of reducing the parallel resonant peak impedance height is by decreasing the q-factor of the circuit, which generally means adding some kind of damping resistance.

In circuits composed of just capacitors, the resistance comes from the equivalent series resistance (ESR) of the individual capacitors. Dielectric loss and conductor loss both contribute to damping in MLCC capacitors and contribute to the ESR, but conductor loss dominates.

The ESR is effectively the resistance from the edge terminals of the capacitors spreading out through conductor plates.

With higher values of capacitance, more plates are sandwiched together in parallel. The ESR goes down because of more parallel paths. Larger value capacitors have lower ESR for the same body size.

The ESR of a typical 0402 ceramic multilayer chip capacitor (MLCC) as described in Chapter 5 is approximately

$$ESR = \frac{0.20 \Omega}{(C[nF])^{0.43}} \quad (7.45)$$

where C is the capacitance in nF.

For example, a 100 nF capacitor has an ESR of roughly

$$ESR = \frac{0.20 \Omega}{(C[nF])^{0.43}} = \frac{0.20 \Omega}{(100)^{0.43}} = 28 \text{ m}\Omega \quad (7.46)$$

whereas a 10 μF capacitor has an ESR of roughly

$$ESR = \frac{0.20 \Omega}{(C[nF])^{0.43}} = \frac{0.20 \Omega}{(10,000)^{0.43}} = 3.8 \text{ m}\Omega \quad (7.47)$$

The effective ESR is reduced when there are n capacitors in parallel.

$$ESR_{\text{caps}} = \frac{1}{n} ESR \quad (7.48)$$

When the only losses are from the capacitors and the cavity is lossless, the q-factor of the parallel resonance is given by

$$\text{q-factor}_{\text{cap-cavity}} = \frac{n}{ESR} \sqrt{\frac{\frac{1}{n}(ESL_{\text{cap}} + L_{\text{spread}})}{C_{\text{cavity}}}} \quad (7.49)$$

The peak impedance at the parallel resonance is approximately

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{n}{ESR} \frac{\left(\frac{1}{n}(ESL_{\text{cap}} + L_{\text{spread}})\right)}{C_{\text{cavity}}} = \frac{1}{ESR} \frac{(ESL_{\text{cap}} + nL_{\text{spread}})}{C_{\text{cavity}}} \quad (7.50)$$

This relationship points out two important regimes:

- Spreading inductance is small compared to the capacitor mounting inductance.
- Spreading inductance is comparable to the capacitor mounting inductance.

When the spreading inductance is very small compared to the mounting inductance of the capacitors in parallel, which is the case for a transparent cavity, the peak impedance value is independent of the number of capacitors.

**Tip**

Astonishingly, when the spreading inductance is small, adding more capacitors does not change the peak impedance height. This has important consequences for engineering smaller peak heights at the parallel resonance with the cavity capacitance.

Adding more capacitors pushes the parallel resonance to higher frequency, which decreases the peak height. However, at the same time, adding more capacitors reduces the effective ESR, which increases the peak height. These two effects cancel out and the peak height is mostly independent of the number of capacitors added to the cavity.

Consider this example with the parameters of

$$C = 10 \mu\text{F}$$

$$h = 2 \text{ mils}$$

$$A = 5 \text{ inches} \times 5 \text{ inches}$$

$$Dk = 4.3$$

$$ESL = 2 \text{ nH}$$

$$ESR = 3.5 \text{ m}\Omega$$

$$n = 1 \text{ and } 9$$

We get the cavity capacitance with

$$C_{\text{cavity}} = \epsilon_0 Dk \frac{A}{h} = 0.225 \times 4.3 \frac{5 \times 5}{0.002} = 12 \text{ nF} \quad (7.51)$$

The spreading inductance between the capacitors and central observation point is roughly equivalent to one square of sheet inductance

$$L_{\text{spread}} = 32 \text{ pH/mil} \times 2 \text{ mils} = 0.064 \text{ nH} \quad (7.52)$$

The parallel inductance of all nine capacitors is

$$ESL_{\text{caps}} = \frac{1}{n} ESL = \frac{1}{9} 2 \text{nH} = 0.22 \text{nH} \quad (7.53)$$

The effective inductance of the capacitors in parallel is still larger than the spreading inductance of the cavity so we can safely ignore the spreading inductance in this example.

The parallel peak resonant frequencies with one capacitor and nine capacitors are

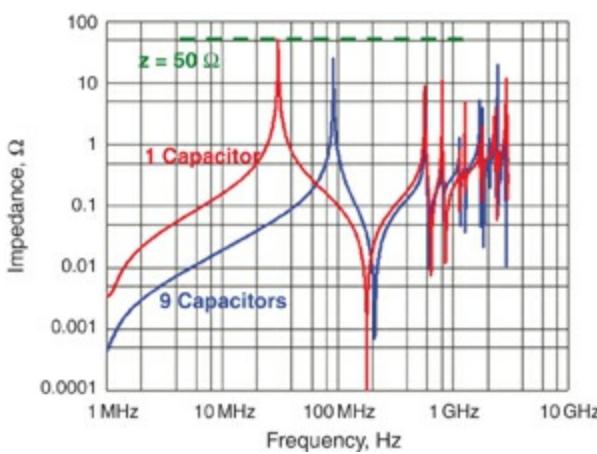
$$f_{\text{res}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{caps}} C_{\text{cavity}}}} = \frac{159 \text{MHz}}{\sqrt{(2 \text{nH}) \times 12 \text{nF}}} = 32 \text{MHz} \quad (7.54)$$

$$f_{\text{res}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{caps}} C_{\text{cavity}}}} = \frac{159 \text{MHz}}{\sqrt{\left(\frac{1}{9} 2 \text{nH}\right) \times 12 \text{nF}}} = 98 \text{MHz} \quad (7.55)$$

We estimate the peak impedance with one or nine capacitors as

$$Z_{\text{peak}} = \frac{1}{ESR} \frac{(ESL_{\text{cap}} + nL_{\text{spread}})}{C_{\text{cavity}}} = \frac{1}{0.0035} \frac{2 \text{nH}}{12 \text{nF}} = 48 \Omega \quad (7.56)$$

Figure 7.17 shows the simulated impedance profile of one and nine identical capacitors on the same cavity with a 2 mil thickness. The cavity is lossless so the only damping is from the ESR of the capacitors. Each capacitor was selected as 10  $\mu\text{F}$  with an ESR of 3.5  $\text{m}\Omega$  and a mounting inductance of 2 nH.



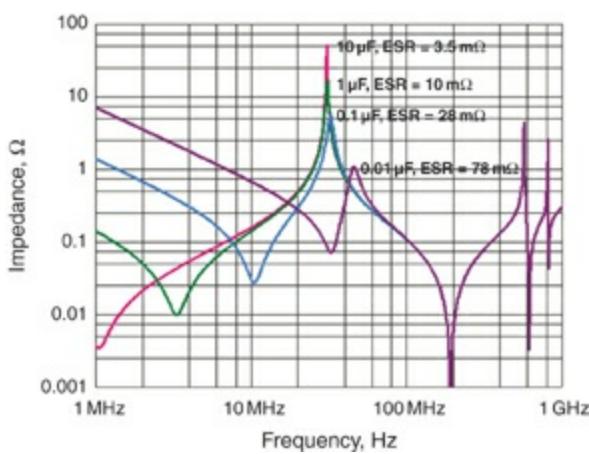
**Figure 7.17** Impedance profile of a cavity with one and with nine identical capacitors. Even though the number of capacitors increased by nine times, the peak impedance decreased by less than two times. Simulated with Mentor Graphics HyperLynx.

It is remarkable that simple estimates are able to predict the performance simulated with a 3D field solver so well. The estimated parallel resonance peak frequencies are 32 MHz and 98 MHz, compared with the simulated values of 31 MHz and 91 MHz. The estimated peak impedance is 48  $\Omega$ , compared with the simulated value of 50  $\Omega$ .

#### Tip

Although many problems are complicated and require a field solver for an accurate solution, never underestimate the value of a simple analytical model. After you confirm it by comparing it to a numerical simulation, it provides valuable design insight into the direction to look for better performance.

This simple model illustrates an important principle to reduce the first parallel resonant peak impedance height. In addition to lower ESL and larger cavity capacitance, another way to reduce the peak height is the capacitor ESR. We obtain larger ESR by using smaller value capacitors or controlled ESR capacitors. Figure 7.18 shows the simulated impedance profiles of a single capacitor on the same cavity for four different values of capacitance and corresponding intrinsic ESRs.



**Figure 7.18** Simulated impedance profile of individual capacitors mounted to a lossless cavity showing that larger capacitor values and smaller ESR increases the first parallel resonant peak height. Simulated with Mentor Graphics HyperLynx.

This clearly illustrates the importance of capacitor ESR: higher is better. Select smaller value capacitors, not for their capacitance value, but because they have higher ESR.

**Tip**

Always consider small value capacitors, not for their capacitance, but for their higher ESR and potential benefit in damping parallel peak resonances.

Note that we did not include cavity losses in this analysis. When the cavity losses are included, the peak heights are reduced and the large value capacitors do not look as bad as they do here.

## 7.11 CAVITY LOSSES AND IMPEDANCE PEAK REDUCTION

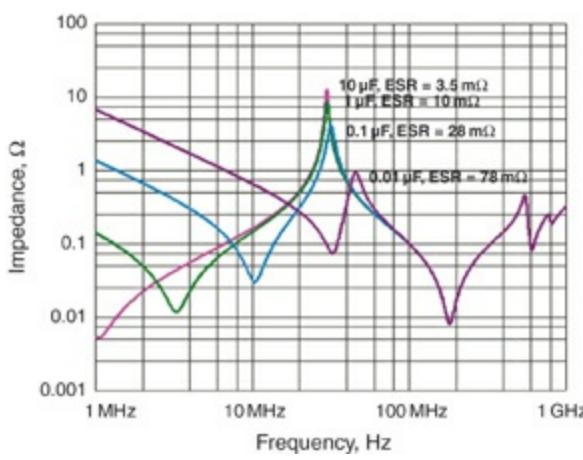
In addition to the loss from the capacitor's ESR, there are also the cavity losses from the dielectric and conductor. We estimate the relative damping from the conductor loss in the cavity by comparing the series resistance in the planes with the ESR of the capacitor. The series resistance of the planes is about 1 square of sheet resistance in both surfaces at about 100 MHz, the

frequency of the parallel resonance.

For 1/2 oz copper, the sheet resistance is about  $1 \text{ m}\Omega/\text{square}$  at DC. The geometrical thickness is about 17  $\mu\text{m}$ . At 100 MHz the skin depth of copper is about 6.6  $\mu\text{m}$ , about 40% the geometrical thickness. This makes the spreading resistance in each plane about  $1 \text{ m}\Omega/40\% = 2.5 \text{ m}\Omega$ . With current paths in the top and bottom planes in series, the total series resistance in the cavity is about  $5 \text{ m}\Omega$ . This value is approximately the ESR of the  $10 \mu\text{F}$  capacitor. It drops the q-factor and therefore the peak impedance roughly in half for this large capacitor.

For the case of the  $0.1 \mu\text{F}$  capacitor, the ESR is  $28 \text{ m}\Omega$ , much larger than the  $5 \text{ m}\Omega$  of series resistance in the planes. Cavity series resistance drops the peak impedance relatively less when the higher ESR caps are used.

The impact of dielectric loss to the cavity is more difficult to estimate but can be included in the simulation. The previous examples did not include the cavity losses. The cavity losses are included in Figure 7.19.



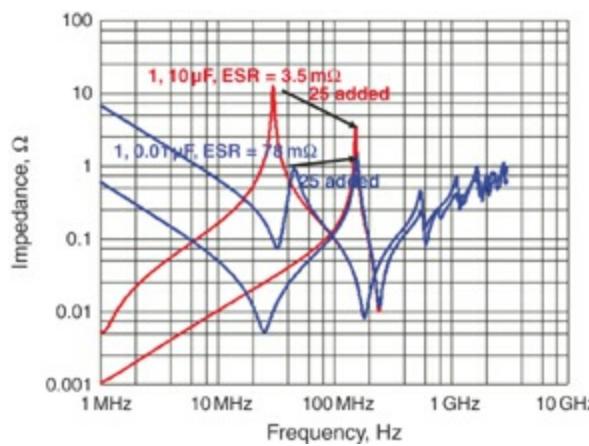
**Figure 7.19** Simulated impedance profile of individual capacitors mounted to a cavity with conductor and dielectric loss. The peak height for the small value capacitor is unchanged, whereas the peak height for the  $10 \mu\text{F}$  capacitor is reduced from  $50 \Omega$  to  $12 \Omega$  by the losses in the cavity. Simulated with Mentor Graphics HyperLynx.

This suggests that the losses in the cavity are an important contributor to reducing the peak heights at parallel resonances and should be included in simulation. The additional cavity loss reduces the difference in performance between the large-value capacitors and the small-value capacitors, each with their different ESR values.

When we add more identical capacitors to the cavity, the peak impedance with cavity losses included does not change much. For high ESR capacitors, the capacitors dominate the losses and the cavity losses are not important.

But when we add multiple, identical, large-value capacitors with small ESR to the cavity and include the cavity losses, the peak impedance decreases with the increasing number of capacitors. Due to the complex interactions of the capacitor and cavity losses, estimating this effect is difficult. It can only be accurately determined in a 3D simulation. [Figure 7.20](#) compares the peak impedances for 1 and 25 identical capacitors on a cavity with losses included for the case

of a 0.01  $\mu\text{F}$  capacitor and 10  $\mu\text{F}$  capacitor.



**Figure 7.20** Simulated impedance profile of 1 and 25 identical capacitors with losses in the cavity for a 10  $\mu\text{F}$  and 0.01  $\mu\text{F}$  capacitor. Simulated with Mentor Graphics HyperLynx PI.

This suggests that smaller value capacitors with their higher ESR are more effective at reducing peak heights than large-value capacitors when many DC blocking capacitors are added to the board. Multiple small value capacitors do not reduce the impedance height compared to a single small-value capacitor; they just shift the peak frequency.

**Tip**

Multiple, higher ESR capacitors do not reduce parallel resonances with the cavity capacitance compared to a single small-value capacitor. More capacitors in parallel reduce their equivalent ESR. They do shift the parallel resonant frequency.

The variation in the ESR of a capacitor with its capacitance and the impact of cavity losses for different ESR values makes the analysis of peak heights for a combination of capacitor values very complicated. We can only accurately analyze it using a 3D simulation.

## 7.12 USING MULTIPLE CAPACITOR VALUES TO SUPPRESS IMPEDANCE PEAK

The goal in engineering the power and ground plane

cavity is to keep the peak impedance heights low. The design is not robust if there are peaks in the frequency range where return current spectral components can stimulate them. The product might or might not work depending on the height and frequency of the impedance peaks and frequency components of the return current. The only way to evaluate is to know the transient return current waveforms and have an accurate impedance profile of the cavity. This is a very difficult task and not often done.

**Tip**

If there are peaks in the cavity's impedance profile in the frequency range of signal components, a good chance exists of excessive cross talk or EMI with large enough current transients. The only way of accurately predicting the expected noise is with knowledge of the transient current waveform.

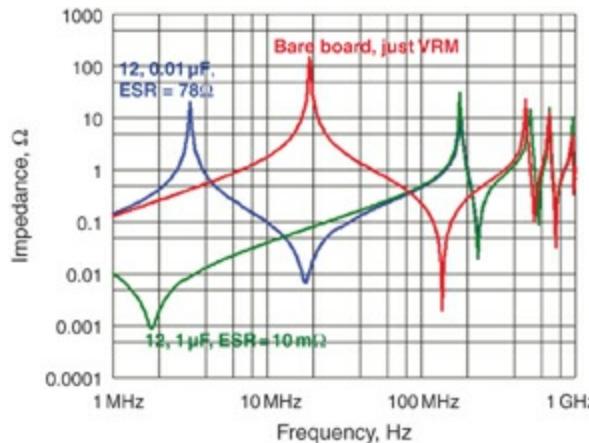
In the absence of a complete system simulation, all we can hope for is to “increase our luck” by engineering peak impedances as low as possible given the finite number of capacitors used. For a fixed number of capacitors, we understand that the precise values have only a small impact on the impedance peak height between the parallel inductance of the several capacitors and the cavity capacitance.

Normally we engineer PDNs with power planes to meet a relatively flat impedance profile up to some frequency for power integrity reasons. The VRM and associated bulk caps and high-frequency capacitors of various values are combined to accomplish this. However, at a higher frequency after the decoupling capacitors have gone inductive, there will always be a parallel resonance impedance peak with the power plane capacitance.

The parallel resonance of the capacitors' mounting

inductance and the cavity's capacitance result in a peak almost independent of the capacitor values used for power integrity. We do not expect the capacitor selection to have much impact on the height of the parallel resonant peak, cross talk, or EMI.

Although smaller value capacitors have higher ESR and lower peak heights, they create a more harmful low-frequency resonance with the VRM. Figure 7.21 compares two extreme cases of 12 identical capacitors, 1  $\mu\text{F}$  or 0.01  $\mu\text{F}$ , with the same ESL of 2 nH. The peak at 200 MHz is about 1/3 lower with the small value of capacitors, but the low-frequency parallel resonance at 3 MHz is very large.



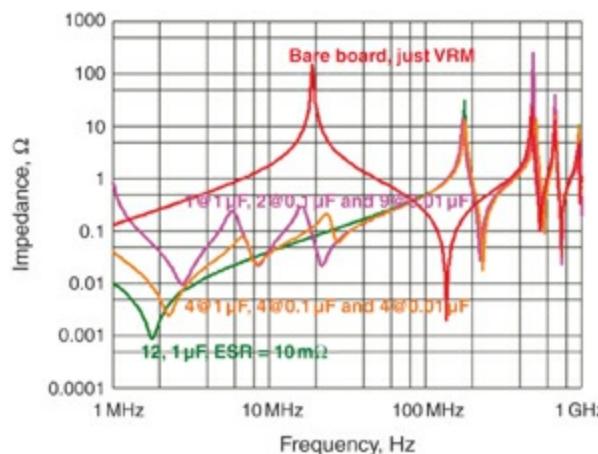
**Figure 7.21** Comparison of the impedance of a board, a VRM, and 12 capacitors with two different combinations. Simulated with Mentor Graphics HyperLynx PI.

In this example, just the bare board and VRM produce a large parallel resonance at about 20 MHz, due to the parallel resonance of the VRM series inductance and the cavity's capacitance.

Adding 12 identical, 0.01  $\mu\text{F}$  capacitors to the board creates two parallel resonances. The 3 MHz resonance is due to the inductance of the VRM and the capacitance of the 12 capacitors. The parallel resonance at 200 MHz is from the combination of capacitors' inductance and the cavity's capacitance.

The first parallel resonance is pushed to much lower frequency and lower peak impedance by using twelve 1  $\mu\text{F}$  capacitors. However, the peak impedance at 200 MHz is increased due to the lower ESR of the high-value capacitors.

Could there be a better combination of capacitor values to balance these two parallel resonances? Having some higher ESR capacitors against the high-frequency peak impedance and some large capacitors against the low-frequency parallel resonance might be desirable. In Figure 7.22, we compare two combinations of 12 capacitors: three each of 1  $\mu\text{F}$ , 0.1  $\mu\text{F}$ , and 0.01  $\mu\text{F}$  and the second combination of one at 1  $\mu\text{F}$ , two at 0.1  $\mu\text{F}$ , and nine at 0.01  $\mu\text{F}$ .



**Figure 7.22** Comparing three combinations of 12 capacitors total. Any combination of large- and small-value capacitors gives the same parallel resonant peak height. Simulated with Mentor Graphics HyperLynx PI.

We see that just about any combination of small and large values of capacitors gives about the same parallel resonance peak height at 200 MHz. The precise combination is not important and the difference is not very large. The other parallel resonant peak frequencies are shifted around with the specific combination of capacitor values. These new peak frequencies could be better or they could be a problem. Without knowing the frequency components of the cavity return currents,

there is no way of judging which result is good or bad, better, or worse.

This suggests that a few low- and high-value capacitors are better than all the same size in trying to reduce the parallel resonant peak height, but the difference is very small.

**Tip**

When selecting capacitor values to reduce the first impedance peak in a cavity to reduce via-to-via cross talk and EMI, the precise values of capacitors are not important. Adding a few, small value capacitors probably helps reduce the parallel resonant peak heights but provides only a very small benefit.

We usually engineer a flat impedance profile for power integrity purposes. With knowledge of the dominant frequency components in the return current's spectrum, we can select specific capacitor values to reduce the peak at specific frequencies. In the absence of any information about the spectrum of the return currents, any of these capacitor combinations may work. Using three different values of capacitor is common practice as is having all of them the same value. We see here that not much difference exists in the impedance profiles and either approach may work, and both approaches are equally risky. The number of capacitors used is the more important term.

**Tip**

The most important design principle when selecting capacitors to reduce the impedance of a cavity is to use more, low inductance capacitors.

## 7.13 USING CONTROLLED ESR CAPACITORS TO REDUCE PEAK IMPEDANCE HEIGHTS

When we use a suboptimal number of capacitors on a board, peak impedances exist in the frequency range

below the bandwidth of the signal. Although this might be “low cost,” it is not robust. An alternative approach can reduce the peak heights and engineer the cavity to be more robust by using controlled ESR capacitors.

These are typically capacitors of  $1 \mu\text{F}$  or  $10 \mu\text{F}$  with ESR engineered higher than normal and typically in the range of  $0.2 \Omega$  to  $1 \Omega$ .

**Tip**

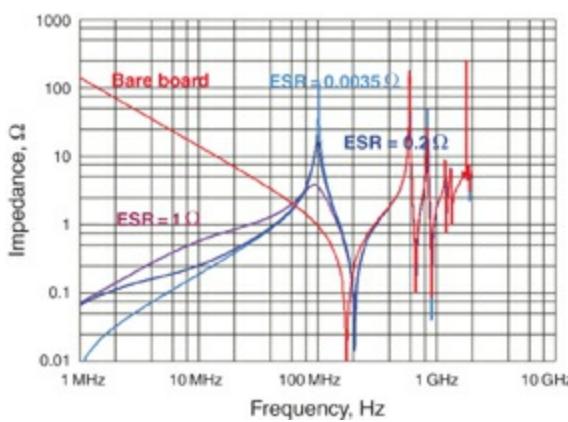
The highest ESR in conventional MLCC capacitors is still so low that the q-factor of the capacitor and cavity parallel resonance is still well above 1.

The q-factor of the cavity resonance dramatically reduces and the peak impedance dramatically lowers if we engineer the capacitor ESR much higher than the intrinsic ESR of MLCC capacitors. The peak impedance at the parallel resonance of the capacitors’ ESL and the cavity’s capacitance is

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{n}{\text{ESR}} \frac{\left( \frac{1}{n} (\text{ESL}_{\text{cap}} + L_{\text{spread}}) \right)}{C_{\text{cavity}}} \quad (7.57)$$

Increasing the ESR of the capacitor decreases the peak impedance.

Figure 7.23 shows the simulated impedance profiles of a single  $10 \mu\text{F}$  capacitor with  $\text{ESL} = 2 \text{nH}$  and three different ESR values. Increasing the ESR to  $1 \Omega$  drops the peak impedance by a factor of 20 or more.

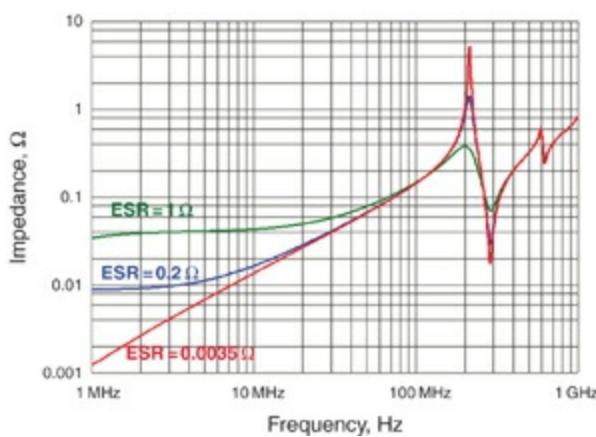


**Figure 7.23** Impedance profile of the same  $10 \mu\text{F}$  capacitor on a board with a VRM for three different ESR values. The low value of  $0.0035 \Omega$  is the typical ESR for a  $10 \mu\text{F}$  MLCC capacitor. The values of  $0.2 \Omega$  and  $1 \Omega$  are typical values for controlled ESR capacitors.  
Simulated with Mentor Graphics HyperLynx PI.

There is no impact on the impedance peaks of the higher frequency cavity modal resonances from the ESR of the capacitor, as expected. The impact is on the parallel resonance formed by the inductance of the capacitor and the cavity capacitance.

When we use multiple capacitors in parallel, the resonant frequency shifts up due to the lower ESL of the parallel combination, but the impact from the higher ESR capacitors is still prominent. [Figure 7.24](#) shows a close-up of the impedance profile of 16 identical capacitors distributed over the surface of the cavity for three different values of ESR:  $0.0035 \Omega$ ,  $0.2 \Omega$ , and  $1 \Omega$ . The higher ESR dramatically damps the parallel resonance.

Although controlled ESR capacitors are effective at reducing impedance peaks, meeting a low target impedance for power integrity purposes by using a reasonable number of controlled ESR capacitors is usually difficult.



**Figure 7.24** Impedance profile for a cavity with VRM and 25 identical capacitors, each  $10 \mu\text{F}$  and  $2 \text{nH}$  mounting inductance. Three different values of ESR are compared:  $0.0035 \Omega$ ,  $0.2 \Omega$ , and  $1 \Omega$ . Note the significant damping of the peak impedance. Simulated with Mentor Graphics HyperLynx PI.

#### Tip

When a limited number of capacitors are added to the cavity, the most effective way of reducing the peak impedance values in a board is by using controlled ESR capacitors with ESR values as much as  $1 \Omega$ , and multiple capacitors in parallel.

An important aspect with controlled ESR capacitors is that at low frequency, the impedance of the cavity is limited by the parallel combination of the higher ESR values. This is the impedance any transient current through the cavity sees and sets another limit on the minimum number of capacitors required to keep the cavity noise to an acceptable level.

If the impedance profile is flat, then the voltage noise in the cavity is related to the total return current flowing through the cavity and this minimum impedance. We get the cavity noise with

$$V_{\text{noise}} = R_{\text{equiv}} \times n_{\text{sig}} \frac{V_{\text{sig}}}{Z_0} \quad (7.58)$$

and

$$R_{\text{equiv}} = \frac{1}{n_{\text{caps}}} \text{ESR} \quad (7.59)$$

or

$$\frac{V_{\text{noise}}}{V_{\text{sig}}} = \frac{\text{ESR}}{n_{\text{caps}}} \frac{n_{\text{sig}}}{Z_0} = \frac{n_{\text{sig}}}{n_{\text{caps}}} \frac{\text{ESR}}{Z_0} \quad (7.60)$$

and

$$\frac{n_{\text{sig}}}{n_{\text{caps}}} = \frac{V_{\text{noise}}}{V_{\text{sig}}} \frac{Z_0}{\text{ESR}} \quad (7.61)$$

For example, if the signal's impedance is  $50 \Omega$ , and the ESR of each capacitor is  $1 \Omega$ , a 10% cavity noise limit requires

$$\frac{n_{\text{sig}}}{n_{\text{caps}}} = \frac{V_{\text{noise}}}{V_{\text{sig}}} \frac{Z_0}{\text{ESR}} = 0.10 \frac{50}{1} = 5 \quad (7.62)$$

We should compare this to the estimate of the number of signals that share a DC blocking capacitor based on the plane bounce created when passing through the inductance of the capacitors. When the ESL is  $1 \text{ nH}$ , the estimate from Equation 7.37 is

$$\frac{n_{\text{sig}}}{n_{\text{caps}}} = 5 \times RT[\text{nsec}] \quad (7.63)$$

When the rise time is  $1 \text{ nsec}$ , the same number of DC blocking capacitors is estimated from rise time and ESR considerations.

When using controlled ESR capacitors, both the ESL and the ESR are important design parameters.

## 7.14 SUMMARY OF THE MOST IMPORTANT DESIGN PRINCIPLES FOR MANAGING RETURN PLANES

The preceding detailed analysis suggests a simple, but important set of guidelines when designing robust return planes in a multilayer board where many signals transition between different planes:

- The most robust design uses the same return plane voltage, such as Vss and all similar voltage return planes are connected together with shorting vias spaced closer than 1/6 the wavelength of the highest frequency component of the signal. This is a spacing between shorting vias, in inches, three times the rise time in nsec.
- If this cannot be arranged, then we can use pairs of planes with different voltages as returns, with as thin as practical dielectric between adjacent planes. Shorting vias still connect between similar voltage planes with a spacing as discussing in the preceding bullet.
- When enough shorting vias to suppress cavity modes is not practical, then at least one return via should be added adjacent to each signal via. This helps reduce the coupling of return current into the cavity.
- When the voltage of the planes that make up a cavity are different, add DC blocking capacitors to the cavity with as low a mounting inductance as practical. This is their most important property.
- The optimal density of DC blocking capacitors is when they push the cavity resonant frequency beyond the bandwidth of the signal. When the mounting inductance is as low as 1 nH each, this is a minimum density of roughly

$$\text{density}_{\text{cap-res}}[\text{per sq inch}] = \frac{1}{RT^2[\text{nsec}]} \quad (7.64)$$

- The second condition that determines the DC blocking capacitor density is the switching noise through the inductance of the cavity and the signal-via density. The capacitor density to keep switching noise less than 10% of the signal swing is related to the signal-via density by

$$\text{density}_{\text{caps}} = \text{density}_{\text{sig}} \frac{1}{5 \times \text{RT}[\text{nsec}]} \quad (7.65)$$

- For a robust design, use the larger of these two densities. In many cases, this results in a large number of capacitors.
- If less than this optimal number of capacitors is used, the cavity will not be robust to switching noise. Use a density of capacitors at least as large as the earlier estimate to reduce switching noise.
- If you know the significant peaks in the transient current frequency profile, select capacitor values to minimize the peak impedance at these frequencies.
- If you do not know the peak transient current frequencies, all combinations of different capacitor values are equally risky, whether all 1  $\mu\text{F}$  capacitors or a distribution of 1  $\mu\text{F}$ , 0.1  $\mu\text{F}$ , and 0.01  $\mu\text{F}$  capacitors. The most important quality is low ESL and more capacitors.
- If possible, use controlled ESR capacitors to reduce the peak impedance values at the parallel resonances. This might determine a minimum limit on the power integrity target impedance.

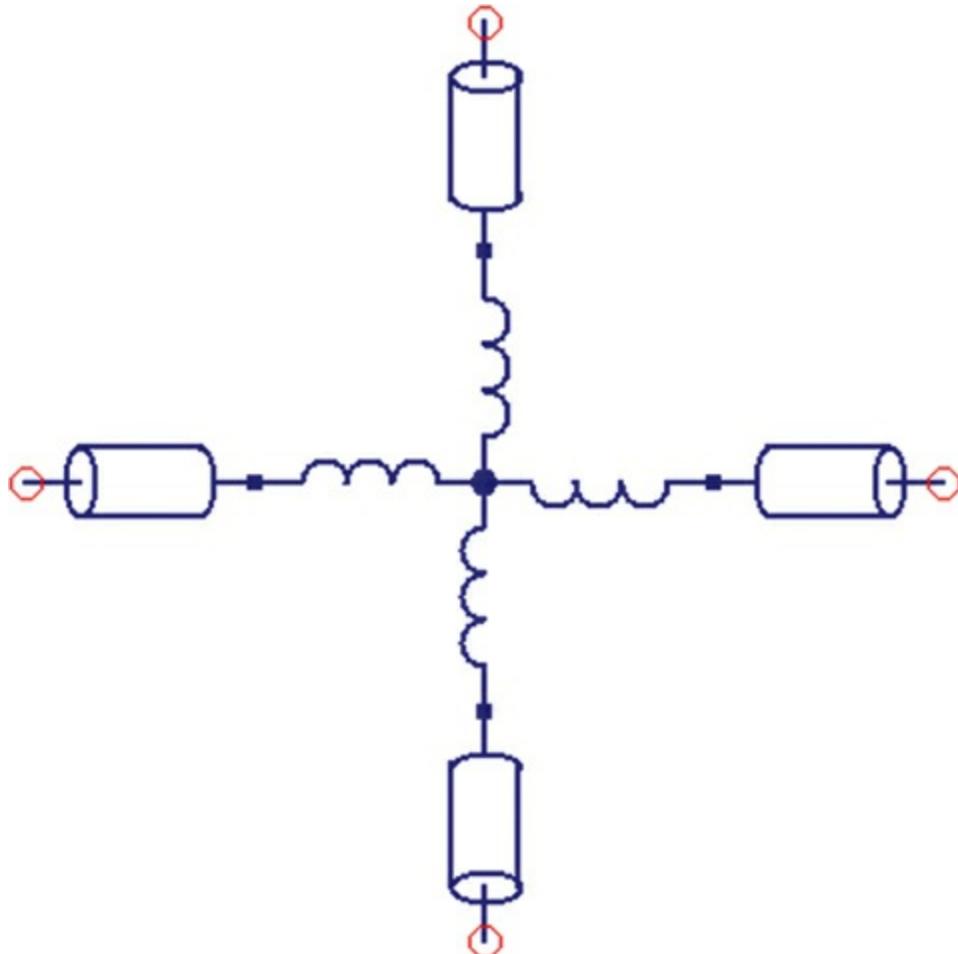
Although many other possible configurations might work, they will not be as robust as following these design guidelines and determining whether the plane configuration will be acceptable without running a full-wave 3D simulation of the transient currents will be difficult.

Regardless, because of the complication of the spreading inductance in the cavity and the interactions of the cavity losses and impedance with the added capacitors, the only way to obtain an accurate estimate of the expected cavity noise is with a 3D full-wave simulator including the transient current waveforms.

## 7.15 ADVANCED TOPIC: MODELING PLANES WITH TRANSMISSION LINE CIRCUITS

Although some simulator tools allow the direct incorporation of S-parameter files in circuit simulations, not all of them do. Simulating the impedance profile of planes in any SPICE-compatible circuit simulator using a simple transmission line model is possible [3]–[6].

When we probe it from the center, we can represent a cavity by four transmission lines oriented radially outward. In addition, there will be some spreading inductance feeding each transmission line from the central observation point. [Figure 7.25](#) shows the transmission line circuit model for this cavity model.

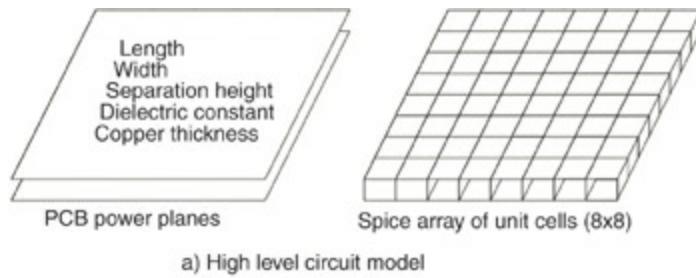


**Figure 7.25** Equivalent approximate circuit model for a cavity as it appears from a central observation point, modeled as four segments with a spreading inductance and a uniform transmission line.

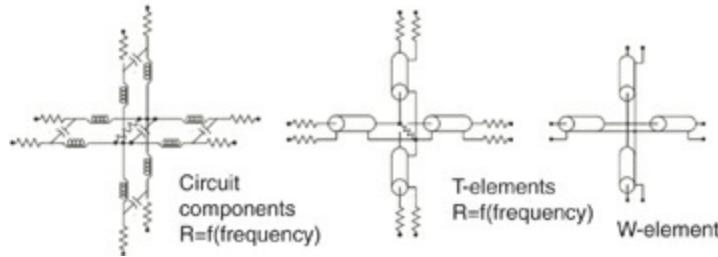
This model is the simplest approximation of a cavity,

using one unit cell to describe the entire cavity. Constructing a more complex model with an interconnected mesh array of these unit cells is possible to model higher order modes and arbitrary cavity shapes. This is the basis of the SPICE-compatible model used in some commercial simulators.

Figure 7.26 shows an example of a power plane SPICE model consisting of a repeated unit cell of short transmission line elements. W-element transmission line segments or ideal segments with series and parallel resistors are used to account for loss. Alternatively, a bedspring model of simple RLC elements may be used [4]. In this transmission line array, the transmission line grid automatically takes into account the spreading inductance.



a) High level circuit model



**Figure 7.26** An interconnected mesh of small transmission line elements used to build up an entire power and ground plane cavity that is SPICE compatible.

The single unit cell of four transmission line segments is a simple approximation that captures the low-frequency impedance properties of the cavity and the first few modal resonances. Its chief advantage is that it can be used in any SPICE simulator to include some resonance effects and it simulates very quickly.

In this model, the length of each transmission line is 1/2 times the length of the cavity and the value of the characteristic impedance of each transmission line is adjusted to match the capacitance in 1/4 of a cavity. The capacitance of the cavity is

$$C_{\text{cavity}} = \epsilon_0 Dk \frac{Len_{\text{cavity}}^2}{h_{\text{cavity}}} \quad (7.66)$$

The time delay of the transmission line segments is

$$TD = \frac{0.5 \times Len_{\text{cavity}} \times \sqrt{Dk}}{c} \quad (7.67)$$

The characteristic impedance of each segment is

$$Z_0 = \frac{TD}{0.25 * C_{\text{cavity}}} = \frac{0.5 \times Len_{\text{cavity}} \times \sqrt{Dk}}{c \times 0.25 \epsilon_0 Dk \frac{Len_{\text{cavity}}^2}{h_{\text{cavity}}}} = \frac{2 \times h_{\text{cavity}}}{11.8 \times \epsilon_0 \sqrt{Dk} \times Len_{\text{cavity}}} \quad (7.68)$$

where

$C_{\text{cavity}}$  = the capacitance of the cavity

$\epsilon_0$  = permeability of free space,  $0.225 \times 10^{-3}$  nF/inch

$Dk$  = the dielectric constant of the material in the cavity

$Len_{\text{cavity}}$  = the length of a side of the cavity

$h_{\text{cavity}}$  = the thickness of the dielectric in the cavity

$c$  = speed of light in vacuum = 11.8 in/nsec

As an example, we simulated the impedance of a cavity with the following features using a 3D field solver and by using the simple single unit cell of four transmission lines and four inductors.

$Len_{\text{cavity}} = 5$  inches

$Dk = 4.3$

$h_{\text{cavity}} = 10$  mils

In this cavity example, we get the characteristic

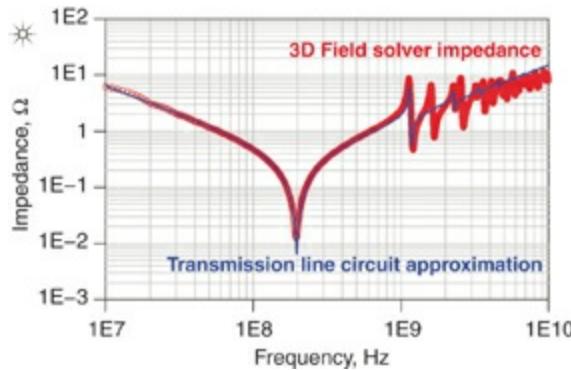
impedance by

$$Z_0 = \frac{2 \times h_{\text{cavity}}}{11.8 \times \epsilon_0 \sqrt{Dk} \times \text{Len}_{\text{cavity}}} = \frac{2 \times 0.01}{11.8 \times 0.225 \times 10^{-3} \sqrt{4.3} \times 5} = 0.73 \Omega \quad (7.69)$$

The spreading inductance from a central observation point to the edge of the cavity is roughly 1/2 to 1 square of spreading inductance, depending on the size of the cavity and the size of the contact region.

As a rough starting place, we can use a total spreading inductance of 3/4 of a square. This is divided up into four inductors, in parallel, feeding the four transmission lines. This allocates three squares of spreading inductance into each transmission line.

Figure 7.27 compares the impedance profiles of the transmission line circuit approximation, and as calculated with a 3D field solver.



**Figure 7.27** Impedance profiles of the cavity as extracted with a 3D field solver and as approximated by four parallel transmission lines with a total of three squares of spreading inductance in parallel. Note that the SRF and first cavity resonance are well approximated by the transmission line model.

The agreement is excellent. Slight variations in probe port positions amplify or attenuate resonant modes at higher frequency. The simple four-transmission line model does not have enough spatial positions to capture all the higher frequency modal resonances. A more complex array of 64 unit cells or more will show the

higher order modes. When we use a cavity as part of the return path of a signal via, we can use this model as an approximation of the impedance of the return path. We can quickly add various capacitors to this model to evaluate the impact of the cavity resonances and even cross talk between channels.

## 7.16 THE BOTTOM LINE

1. When return currents of signals pass through the impedance of a cavity, they induce voltage noise in the cavity and create signal integrity and EMI problems. Rarely is this a power integrity problem for circuits on-die that consume current from the PDN.
2. The frequency components of the voltage noise are related to the peak impedances in the cavity's impedance and the frequency components of the return currents.
3. The goal in designing the cavity is to push the peak frequency components above the bandwidth of the signals and secondly to reduce the peak heights below a dangerous level.
4. A thinner dielectric in the cavity is the most effective way of reducing the peak heights of the modal resonance.
5. The most effective way of pushing up the parallel resonant frequencies in a cavity is by adding shorting vias between the planes of the cavity. This requires the voltage of the planes to be the same.
6. The most important criterion in cavity design is to use return planes that are the same voltage for all signals so that shorting vias may be added.
7. If the voltage of the two planes in the cavity are not the same voltage, the only alternative is to use DC blocking capacitors in series with the shorting

vias. DC blocking capacitors make poor shorting vias.

8. It takes a much higher density of DC blocking capacitors to push the cavity resonances to higher frequency than shorting vias.
9. The most important property of a DC blocking capacitor is its mounting inductance. The second most important property is its ESR.
10. With a suboptimal number of DC blocking capacitors, designing a robust cavity is difficult. Careful simulation including the specific transient return current spectrum and the specific impedance of the cavity is critically important.

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# Chapter 8. The PDN Ecology

So far we have looked at the principles behind the behavior of the PDN and its components. The most important property of the components of the PDN is how they interact. The capacitance of an element can interact in a parallel combination with the inductance of another element. This results in a parallel resonance and a peak impedance.

Although the industry focuses much attention on how low an impedance we can obtain by adding capacitors to a PDN, the peak impedances are what cause the real problems. Interactions between components are generally what create these peaks. This means we must analyze the entire PDN system as a whole. This is the PDN ecology.

The real problems and design strategies are based on the interactions between components as they exist in the entire PDN ecology. Only by knowing the nature of these interactions can we analyze the optimized properties of each component. Ultimately, we must evaluate the final performance based on the entire ecology.

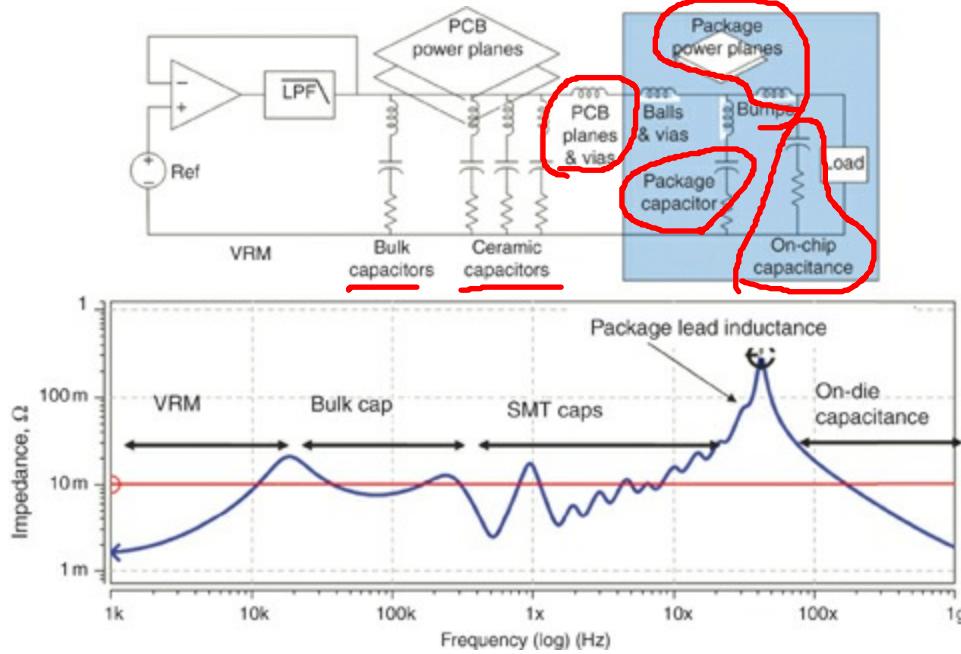
This chapter takes a thorough look at each section of the PDN ecology and how they all interact.

## 8.1 PUTTING THE ELEMENTS TOGETHER: THE PDN ECOLOGY AND THE FREQUENCY DOMAIN

The PDN consists of all the interconnects from the VRM to the power rails on the die. Each and every element in this path plays a role in delivering a low noise, constant voltage supply to the power rails on the die.

The frequency domain is a convenient perspective to analyze the PDN because specific elements of the PDN

dominate the impedance behavior in specific frequency regions. Figure 8.1 illustrates a typical frequency domain impedance profile as seen from the die pads and the physical elements that contribute to each region.



**Figure 8.1 Top:** Features of the PDN ecology.  
**Bottom:** Impedance profile *as seen* by the pads on the die.

Six specific elements of the PDN play significant roles:

- The on-die capacitance
- The package PDN, including on-package decoupling (OPD) capacitors
- The board-level power and ground planes
- The MLCC board-level decoupling capacitors
- The bulk decoupling capacitors associated with the VRM
- The voltage regulation module (VRM) and its immediate bulk decoupling capacitors

The value of this perspective is that we can identify specific physical elements that affect specific frequency ranges of the PDN profile. The danger with this approach is that trying to optimize each element

separately can be misleading.

The most important features of the PDN, the peak impedances, are due to interactions at the boundaries of features. If attention is paid only within specific regions, such as the VRM or the MLCC capacitors, the resulting PDN system might not be optimized.

**Tip**

The least effective way of optimizing the PDN elements is to consider each element separately. The real problems in the PDN arise at the interactions between these six elements. We must optimize the entire PDN ecology, not each element separately.

We refer to the entire PDN system as an ecology of elements where the interactions between elements, how well each element plays with the others, is the most important factor. For example, the interaction of the on-die capacitance and package PDN creates the biggest peak impedance. The interaction of the VRM and its various bulk capacitors affects the stability of the supply. In this context, we separate the VRM into two parts: the regulation module, which has the control electronics, inductor, and other active circuitry; and the bulk decoupling capacitor. The interactions of the power and ground planes and the MLCC capacitors with the package PDN and on-die capacitance can make or break an otherwise robust PDN.

Yet all too often the popular literature focuses on the selection of MLCC capacitors without regard to the rest of the system, which means that design guidelines for selecting capacitor values can be meaningless.

**Tip**

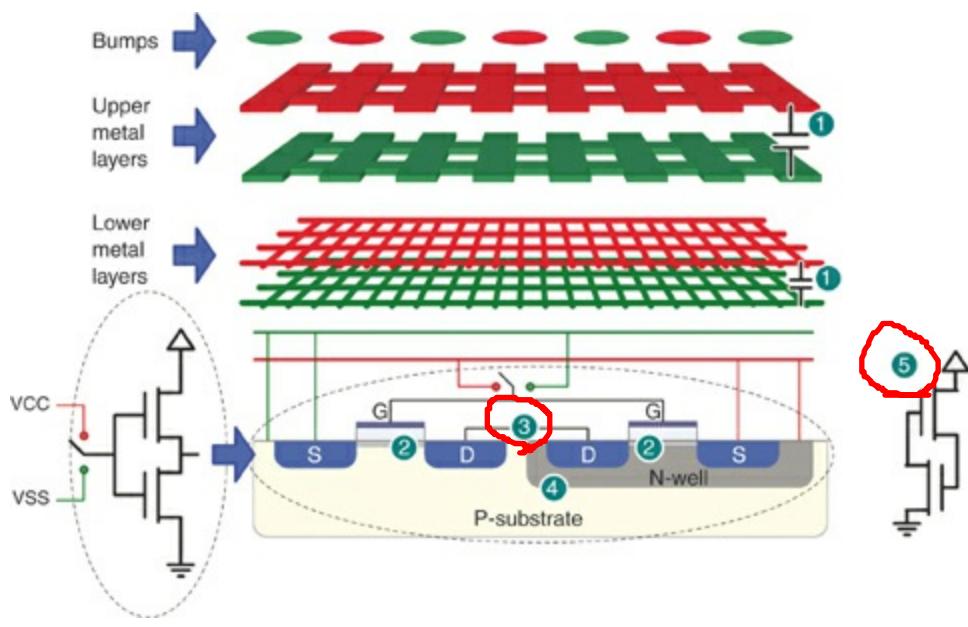
The most important features of the PDN, which influence the performance, are the peaks in the impedance. These are most strongly affected by the interactions between elements in the PDN. This is why the entire PDN ecology is important.

The peaks in the impedance profile arise when elements affecting one frequency regime interact with elements affecting the adjacent frequency regime. The next sections briefly explore each of these regimes and offer design guidelines to reduce the peak impedances.

## **8.2 AT THE HIGH-FREQUENCY END: THE ON-DIE DECOUPLING CAPACITANCE**

The most important structure in the PDN and the only feature that influences the impedance of the on-die power rails in the highest frequency range is the on-die decoupling capacitance (ODC), together with resistance. This is formed by a combination of five elements [1], illustrated in Figure 8.2:

- The on-die power/ground metallization grid network
- The distributed gate capacitance between the collection of p and n transistors in typical CMOS circuits
- The on-die signal load capacitance being driven by the on-state transistor
- Silicon diffusion junctions
- Additional intentionally added on-die decoupling capacitance



**Figure 8.2** The five sources of on-die decoupling capacitance: 1) metallization, 2) gate, 3) load, 4) diffusion junctions, and 5) intentionally added capacitance.

The on-die decoupling capacitance plays the very important role of providing low PDN impedance at the highest frequencies. In the GHz regime, the on-die decoupling capacitance is the *only* feature providing a low impedance and keeping the voltage noise on the power rail below an acceptable level. If insufficient on-die decoupling capacitance exists, nothing can be done in the rest of the system to compensate.

#### Tip

The on-die decoupling capacitance establishes a low impedance at the highest frequency. Without enough on-die decoupling capacitance, the device might fail independent of what you do in the rest of the system.

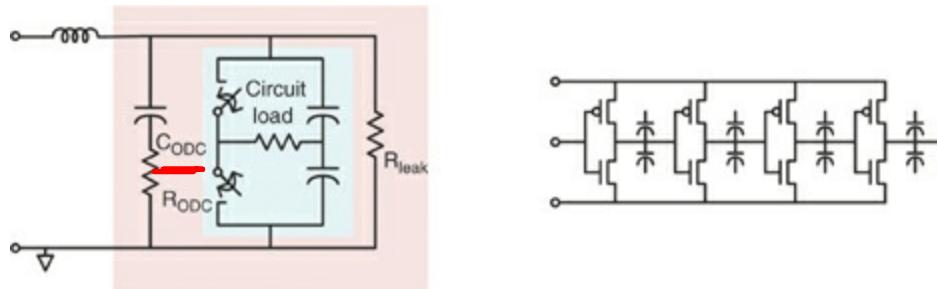
You can do nothing at the board level to compensate for insufficient on-die decoupling capacitance. For a robust and cost-effective PDN, knowing the value of the on-die capacitance is important input information to the design process. Unfortunately, this parameter is difficult to get from semiconductor suppliers.

When we can't get the on-die capacitance from the chip supplier and it is important to know, we can "reverse engineer" a rough estimate. We must assume that the semiconductor vendor engineered a minimally acceptable amount of on-die capacitance.

**Tip**

The on-die decoupling capacitance is a critical design parameter for the PDN ecology. Always ask the semiconductor provider for this value. When we cannot get a realistic value, we can estimate a reasonable minimum value based on a few simple assumptions.

We can estimate the on-die capacitance using a time domain approach. Transient current flows from all the non-switching capacitance to charge up the capacitance that switched (load capacitance), as illustrated in [Figure 8.3](#). We can estimate the minimum amount of on-die decoupling capacitance required so that the Vdd rail droops less than 10% each clock cycle when the load capacitance is switched. This is known as *clock edge noise*, and we further discuss it in [Chapters 9 and 10](#).



**Figure 8.3** Circuit showing the on-die decoupling capacitance (outer shaded region) from the gates and interconnects that provide the local charge storage to charge up the switched capacitance load (shaded inner region) each clock cycle.

From this simple circuit we calculate the voltage droop on the Vdd rail from charge conservation considerations and  $q = CV$ .

$$\frac{V_{dd1}}{V_{dd0}} = \frac{C_{ODC}}{C_{ODC} + C_{load}} \quad (8.1)$$

If we keep the final  $V_{dd1}$  voltage within 10% of the initial  $V_{dd0}$ , then the ratio of the rail voltage after switching to the voltage before switching is 90%. The required on-die decoupling capacitance is

$$C_{ODC} = 9 \times C_{load} \quad (8.2)$$


---

where

$V_{dd0}$  = the nominal rail voltage

$V_{dd1}$  = the new rail voltage after switching

$C_{ODC}$  = the on-die decoupling capacitance

$C_{load}$  = the average on-die load capacitance being charged and discharged each clock cycle

The ratio of the load capacitance switched per cycle to the on-die decoupling capacitance is the “switching factor.” This ratio determines the initial voltage drop on the power rail when all the gates switch on each clock edge.

We estimate the average load capacitance being charged and discharged each clock cycle based on the average power dissipated by the core of the die, neglecting the leakage current. The energy stored in the load capacitance is

$$U = \frac{1}{2} C_{load} V_{dd}^2 \quad (8.3)$$

In any RC circuit, the energy dissipated through the resistor and turned into Joule heat is equal to the energy stored in the capacitor, whether the capacitor is charging or discharging. If we assume that gates are switched on or off with each edge of the clock, so that a comparable load capacitance is charged or discharged in each half cycle, then the total energy dissipated through

resistive elements each clock cycle is twice the energy stored in the load. If this energy is switched at the clock frequency, the **average power consumption** is

$$\langle \text{power} \rangle = \underline{2} \times U \times F_{\text{clock}} = 2 \times \frac{1}{2} C_{\text{load}} V_{\text{dd}}^2 \times F_{\text{clock}} \quad (8.4)$$

from which the load capacitance is

$$C_{\text{load}} = \frac{\langle \text{power} \rangle}{V_{\text{dd}}^2 \times F_{\text{clock}}} \quad (8.5)$$

and the  $C_{\text{ODC}}$  is

$$C_{\text{ODC}} = 9 \times C_{\text{load}} = 9 \times \frac{\langle \text{power} \rangle}{V_{\text{dd}}^2 \times F_{\text{clock}}} \quad \begin{array}{l} \text{proportion to: power} \\ \text{Inverse prop. to: vdd}^2, F \end{array} \quad (8.6)$$

For 1-watt power dissipation from a 1 v Vdd rail and a clock frequency of 1 GHz, the on-die decoupling capacitance required to keep the rail collapse below 10% is

$$C_{\text{ODC}} = 9 \times \frac{\langle \text{power} \rangle}{V_{\text{dd}}^2 \times F_{\text{clock}}} = 9 \times \frac{1 \text{ watt}}{1 \text{ v}^2 \times 1 \text{ GHz}} = 9 \text{ nF} \quad (8.7)$$

This suggests a scaling based on the power consumption of the die. We can reasonably expect on-die capacitance values on the order of 100 nF for chips dissipating 10 watts. In high-power chips, values as much as 1000 nF are not unreasonable.

#### Tip

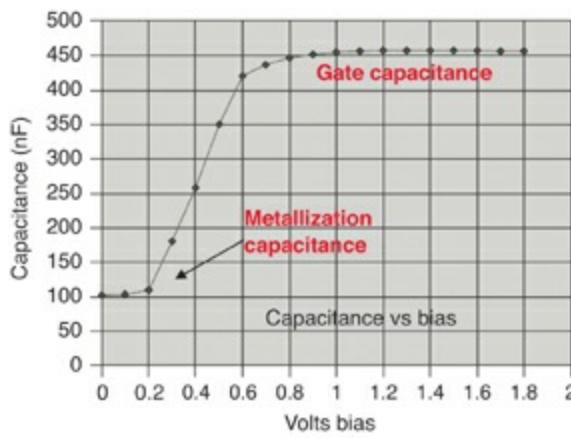
Using a time domain approach we can roughly estimate the minimum on-die decoupling capacitance to be on the order of **10 nF for 1 watt chips**. This scales with the power consumption of the rail.

After the die design is mature, we can estimate the intrinsic sources of on-die decoupling capacitance from parasitic extraction tools based on the circuit design and

technology node data.

When insufficient decoupling capacitance is available from intrinsic sources, additional die area is often used for decoupling capacitance using either MOS or MIM (metal-insulator-metal) structures. Typical capacitance density for 90 nm CMOS technology is approximately 1 nF/mm<sup>2</sup>. Die area reduction is a strong motivation for accurate capacitance extraction and power-noise analysis tools.

The amount of on-die decoupling capacitance is an important metric of the high-frequency PDN. We can easily measure it, as illustrated in Chapter 3. The package balls are probed with VNA ports.  $S_{21}$  measurements and conversion to  $Z_{21}$  is usually the most accurate way to measure low impedances at high frequency. Impedance in the appropriate frequency band is converted to capacitance by  $Z = 1 / j\omega C$ . On-die capacitance is often a strong function of voltage. Figure 8.4 shows an example of the measured on-die decoupling capacitance with the die biased off and gradually biased on.



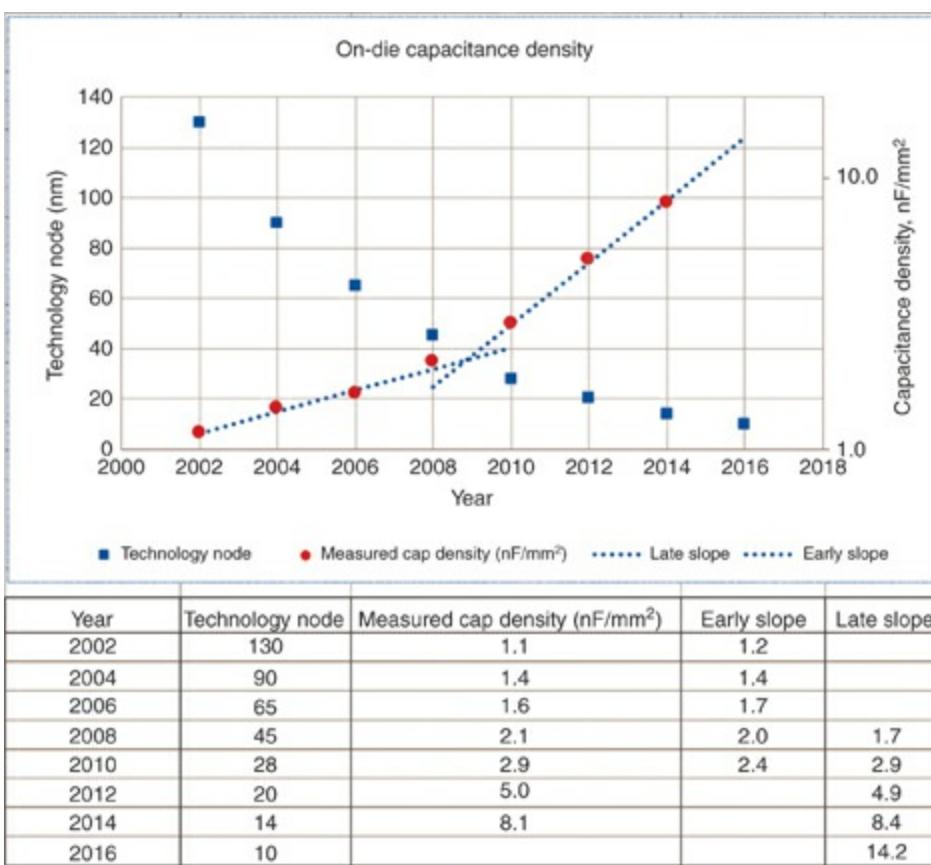
**Figure 8.4** Measured on-die decoupling capacitance for a small chip as the bias voltage is turned on.

With no bias voltage the on-die decoupling capacitance is dominated by the passive Vdd and Vss power grid metallization and diffusion capacitance and

is about 100 nF. When the chip is powered on, the decoupling capacitance increases from the CMOS gates and the interconnect capacitance that is now connected through the outputs of the CMOS gates [2]. In this example, the total on-die decoupling capacitance is about 450 nF.

As we discuss in [Chapters 9 and 10](#), [power density](#) and [capacitance density](#) are closely related. Power is consumed when capacitive loads are switched. The switching factor (fraction of all the on-die circuits that switch per clock cycle) can be no more than about 15% without creating excessive clock cycle noise. Capacitance density and power density increase at about the same rate on future process nodes.

The on-die capacitance density has been increasing at about 1.2 times to 1.7 times for each technology node generation. [Figure 8.5](#) shows the historical trend for on-die capacitance density over the last several technology process nodes. For the first decade of this century, the ODC density seemed to increase about 1.2 times with each process node. The trend for the second decade is about 1.7 times for each process node. As of this writing, we expect that the FinFET technology at the 10 nm node will continue on this trend line. The majority of on-die capacitance is now related to the wiring channels.



**Figure 8.5** Historical trends in on-die decoupling capacitance. **Top:** Graph of the technical node dimensions (squares) and the on-die capacitance per area (circles). The on-die capacitance scale is a log scale.  
**Bottom:** Tabulation of the plotted data.

The capacitance and power density trend has implication for the on-die power path resistance. The ESR associated with on-die capacitance is often inversely proportional to capacitance. The capacitance density is relatively constant for a technology node assuming that designers have used the die area in the most efficient way possible. Some series resistance always exists for the on-die capacitance. As die area goes up there is more capacitance in parallel and more ESR in parallel so ESR being inversely proportional to capacitance makes sense.

For several technology nodes, the product of R and C has been about 250 ps, and for good reason. Chip designers have found it necessary to dedicate more and more metal resource to the power path to avoid

suffering excessive voltage drop with increasing power density. As clock frequencies and power densities go up, this time constant is likely to go down to accommodate the timing requirements of the die. In any case, on-die capacitance, power density, and ESR are closely related. The PDN designer can count on an ESR and capacitance RC time constant of approximately 250 ps that is trending downward with future technology nodes. This is true for large circuit blocks such as processor cores. There will be some RC time constant for IO circuits but it is not necessarily 250 ps. This has important implications for PDN damping.

**Tip**

Historically, a connection has existed between the on-die ESR and the on-die capacitance. This combination has an effective RC time constant of about 250 ps. Knowing how the on-die capacitance scales enables a rough estimate of how the ESR scales. This is important when estimating the damping and q-factor of some aspects of the PDN.

Based on this general rule of thumb connecting the RC time constant, the on-die capacitance, and ESR, we can estimate the ESR, which contributes to PDN damping as

$$\text{ESR}_{\text{on-die}} = \frac{0.25 \text{ nsec}}{C_{\text{ODC}} [\text{nF}]} \quad (8.8)$$

For example, if the on-die capacitance is 50 nF, the ESR is 5 mΩ. If the on-die capacitance is 200 nF, the ESR is 1.2 mΩ.

Measuring ESR while measuring capacitance is best but ESR is often harder to interpret. Measurements often depend upon probe positioning and the size and area of the on-die capacitance being measured. On-die ESR is best measured for small die areas and then scaled up to large die areas using the RC time constant.

Measurements for large die areas tend to be driven by horizontal package and die wiring resistance rather than the vertical resistance from bumps to on-die capacitance immediately below the bumps.

The ESR in series with on-die capacitance vertically underneath the package bumps and balls is part of the resonant current path and contributes to damping.

For larger die areas, the horizontal resistance in the die power bus, rather than vertical ESR, limits the effective radius for on-die decoupling capacitance [3][4].

Horizontal die power bus resistance should not be confused with vertical ESR resistance; they are two different things. The horizontal resistance forms an RC time constant that is not necessarily the same as the vertical RC time constant. The horizontal time constant has implications on how quickly on-die disturbances can propagate to other circuits on the die.

During normal operation, small localized on-die circuits consume substantial charge from local on-die capacitance and cause a localized voltage droop. Nearby on-die capacitance comes to the aid by supplying charge but this can only happen after the horizontal RC time constant expires. The local disturbance propagates out into the rest of the die governed by the horizontal RC time constant. Refer to Figure 3.42 in Chapter 3 for a diagram of the horizontal and vertical resistance and section 3.14 for more detailed information on measuring on-die decoupling capacitance.

For small die areas on the order of several square millimeters with relatively square aspect ratios, the relaxation time is several hundred ps. The *relaxation time* is the amount of time that it takes for the whole on-die power bus to relax to the same voltage after a disturbance. For large die areas where the on-die power bus is long and narrow and has high aspect ratio, the

relaxation time can be more than 1 ns. This has implication for PDN situations that can be considered lumped nodes and others that are distributed across time and space. The only way to analyze these situations is with a complex 3D model that takes into account the local current draw from the PDN, the precise distribution of the on-die decoupling capacitance, and the on-die power bus resistance.

We can illustrate the principles for engineering the system-level PDN by using a simple lumped circuit model for the on-die PDN assuming a single C, R, and L value. For small circuit core areas where the on-die PDN relaxation time constant is a small part of the clock period, the on-die power bus is likely to be strong enough to hold all the bumps together. The lumped circuit approximation gives highly accurate results as the local power bus fully relaxes back to the same distributed voltage during the clock cycle.

**Tip**

Although compelling PDN reasons exist to engineer a higher ESR on-die to provide damping for critical parallel resonances, the chip design community is often reluctant to add any additional series resistance for fear of DC IR drop. Circuits that do not consume much power and current can tolerate and greatly benefit from intentional resistance added in the power path.

High-power circuits require low-resistance power paths with little damping. Fortunately, high-power circuits benefit from load damping, which is further discussed in [Chapter 10](#). If we need to, we can spend additional die area on damping capacitance with intentional ESR but this comes at the cost of die area or additional layers.

Because the spacing between the on-die power and ground paths associated with the power bus are typically so close, the equivalent series inductance is very small,

on the order of 0.1 pH. The series impedance of the power bus is  $R + j\omega L$ . The resistance term is usually more important than the inductance term up to tens of GHz.

The on-die PDN is usually well represented by the series combination of the C<sub>ODC</sub> and the on-die ESR. The capacitance dominates the impedance up to a corner frequency where the ESR becomes important. **Figure 8.6** shows an example of the impedance profile desired for the case of a 5 watt chip, operating at a 1 GHz clock frequency, with a C<sub>ODC</sub> = 50 nF, ESR = 5 mΩ, and an ESL = 0.1 pH. The RC product is 250 ps as discussed previously. **ESL is not important below 10 GHz.**



**Figure 8.6** Impedance profile as seen from the pads of the die for an on-die decoupling capacitance of 50 nF, ESR of 5 mΩ, and ESL of 0.1 pH. The on-die ESR becomes apparent above 400 MHz. Frequency beyond 10 GHz is required to see any ESL.

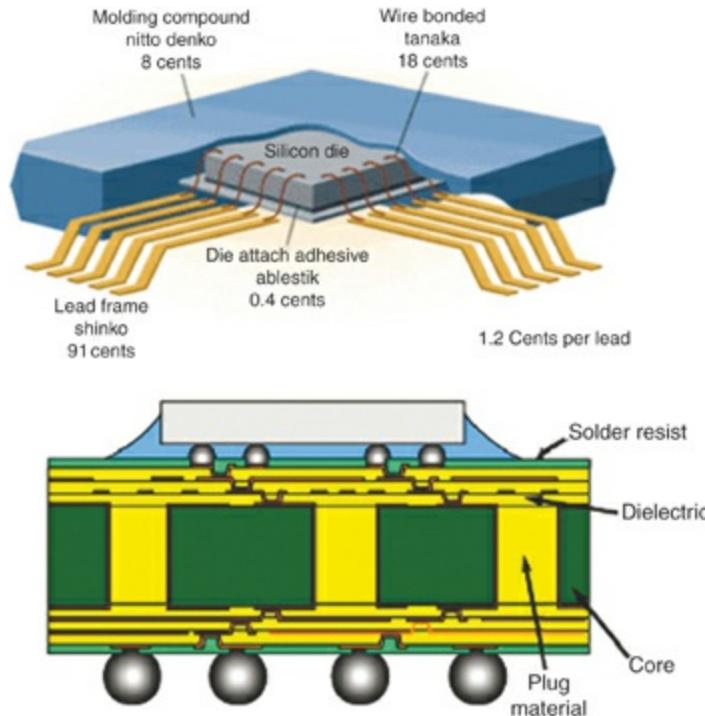
### 8.3 THE PACKAGE PDN

The package PDN spans the network from the die pads to the circuit board vias and planes. This consists of

- The wire bonds or solder balls from the die to the package substrate
- The connections between the die pads and internal package planes
- The on-package decoupling capacitors if present
- The connection between the package and board formed by solder balls or leads

- The vias in the circuit board from the top pads into the cavity of the circuit board planes. The package determines the location of the board vias but the board stackup determines the length of the vias

Two typical but different package cross-section examples are a leaded package and a multilayer BGA package, as shown in Figure 8.7.



**Figure 8.7 Top:** Illustration of the features in a leaded package. **Bottom:** The interconnect paths inside a typical BGA package.

In the absence of on-package decoupling capacitors, the impedance profile of the package PDN, as viewed from the parallel combination of the pads on the die to the planes in the circuit board, is inductive up to very high frequencies. The frequency at which the package PDN is no longer inductive is set by either the modal cavity resonances in the package planes or the total path length through the package exceeding 1/10 of a wavelength.

For a large BGA 1 inch on a side, the first modal cavity resonance in the internal power-ground cavity has a

frequency of about

$$f_{\text{res}}[\text{GHz}] = \frac{12 \frac{\text{inch}}{\text{nsec}}}{\sqrt{Dk}} \frac{1}{2 \times \text{Len}[\text{inches}]} \sim 6 \frac{1}{2 \times 1} = 3 \text{ GHz} \quad (8.9)$$

half wavelength in dielec = 25.4mm

where

$f_{\text{res}}$  = the first resonant frequency of a square cavity  
when one-half of a wavelength fits between the ends

$Dk$  = the dielectric constant of the material in the cavity, typically around 4

$\text{Len}$  = the length of a side of the package, in inches

We get the frequency where the total interconnect length exceeds 1/10 of a wavelength with

$$f_{\text{res}}[\text{GHz}] = \frac{12 \frac{\text{inch}}{\text{nsec}}}{\sqrt{Dk}} \frac{1}{10 \times \text{Len}[\text{inches}]} \sim 6 \frac{1}{10 \times 1} = 600 \text{ MHz} \quad (8.10)$$

This analysis suggests that for frequencies below about 600 MHz, we can approximate the impedance of an individual PDN current path inside the package as a lumped inductor.

The equivalent parallel inductance of the interconnect paths from the die pads to the power planes of the circuit board depends on the details of the package and board physical structures. This makes generalizing the loop inductance of the package PDN difficult.

However, the package-to-board inductance is just as important in the PDN ecology as the on-die capacitance parameter. Without an accurate estimate for the equivalent package lead inductance, having a robust and cost-effective PDN design is difficult. We must add design margin to make it robust, which means increase the cost. This is why asking your semiconductor vendor for an accurate package model for the PDN is so important.

**Tip**

Asking your semiconductor vendor for an accurate package PDN model is always important. Rarely will you get it, but you should always ask for it. If you cannot get the model from the semiconductor supplier, you will have to estimate the package lead inductance using some knowledge of the package design in order to simulate and optimize the PDN.

Estimating the equivalent package lead inductance is difficult because of the huge range of possible values. For a large multilayer package with hundreds of power and ground solder balls and multiple pairs of power and ground planes, the equivalent loop inductance can be as low as a few pH. In the case of a leaded quad flat pack (QFP) package, with leads as long as 0.5 inches, and only two pairs used for power and ground, the equivalent inductance may be as much as 10 nH. This is a factor of a 10,000 difference in the equivalent package inductance. It all depends on the specific details.

The simplest approach for estimating the loop inductance in the package PDN is to assume that each discrete path through the package, other than through planes, has some loop inductance per length and a total length. If there are  $n$  pairs of paths in parallel, we approximate the equivalent loop inductance as

$$L_{loop} = \frac{1}{n_{pairs}} \times L_{per-len} \times Len \quad (8.11)$$

where

$L_{loop}$  = the equivalent loop inductance of the package  
PDN

$n_{pairs}$  = the number of power-ground pin pairs

$L_{per-len}$  = the loop inductance per length, with 20  
pH/mil a good estimate

$Len$  = the effective length of each of the pairs

This assumes that the loop inductance of the package

power and ground planes is a small contribution compared to the discrete paths. This might not always be the case.

For example, in a multilayer BGA, there might be a total length including the PCB vias, the solder balls, the short traces in the package to the planes, and then the C4 connections to the die, on the order of 50 mils. If there are 100 power and ground pairs, the equivalent loop inductance is on the order of

$$L_{\text{loop}} = \frac{1}{n_{\text{pairs}}} \times L_{\text{per-len}} \times Len = \frac{1}{100} \times 20 \frac{\text{pH}}{\text{mil}} \times 50 \text{ mil} = 10 \text{ pH} \quad (8.12)$$

The power and ground planes might have a thickness of 1 mil, in which case the sheet inductance is  $32 \text{ pH/mil} \times 1 \text{ mil} = 32 \text{ pH}$ . The spreading inductance through the planes might be approximately of 1 square, or about 32 pH. Depending on the number of planes and the number of power and ground connections, the spreading inductance may or may not be significant. This makes generalization difficult, especially at the small package inductance end.

In a small leaded package or a two-layer BGA package, such as a chip scale package (CSP) the total lead length might be on the order of 250 mils and there may be 20 power and ground pairs. The total loop inductance is approximately

$$L_{\text{loop}} = \frac{1}{n_{\text{pairs}}} \times L_{\text{per-len}} \times Len = \frac{1}{20} \times 20 \frac{\text{pH}}{\text{mil}} \times 250 \text{ mil} = 250 \text{ pH} \quad (8.13)$$

Although these approaches offer a rough estimate of the effective package lead inductance, the only way to get a more accurate estimate is to measure it or to perform a 3D simulation from detailed knowledge of the internal package structure. From the measured or simulated S-parameters, all the power and ground paths

can be bussed in parallel, shorted at one end, and the  $S_{11}$  between the power and ground connections at the other end calculated. We estimate the equivalent loop inductance from the  $S_{11}(f)$  using

$$Z_{\text{loop}}(f) = 50\Omega \frac{(1+S_{11}(f))}{(1-S_{11}(f))} \quad \text{and} \quad L_{\text{loop}} = \frac{\text{imag}(Z_{\text{loop}}(f))}{2\pi f} \quad (8.14)$$

Both the S-parameters and the impedance are complex numbers.

We can sometimes use one other approach to provide a rough estimate of the equivalent loop inductance of the package when no other data is available. It relies on “reverse engineering” the lead inductance based on the estimated number of power and ground path pairs and their lengths.

We start with the assumption that the minimum number of power/ground pin pairs is set by the maximum allowed current through one pair, and the total, maximum current feeding the PDN.

For example, an IPC recommendation for the maximum current handling capacity of a 10 mil diameter via is about 2A. A 1 mil diameter gold wire bond has a max current rating of about 1A with a more conservative limit closer to 0.25A.

If we assume the minimum number of distinct power and ground paths in a package are limited by the maximum total current based on the average power dissipation, we can estimate how many power-ground pin pairs may be used in a package.

The minimum number of power-ground pairs is roughly,

$$n_{\text{pairs}} > \frac{I_{\text{ave}}}{I_{\text{max\_pair}}} = \frac{\langle \text{power} \rangle}{V_{\text{dd}} \times I_{\text{max}}} \quad (8.15)$$

where

$n_{pairs}$  = the minimum number of power and ground pin pairs

$I_{max\_pair}$  = the maximum current capacity rating of any pair

$V_{dd}$  = the rail voltage

$\langle power \rangle$  = the average power dissipation of the core

For example, for a device with 10 watt power dissipation in the core, with a 1v rail and using the conservative value of  $I_{max\_pair} = 1/4$  A, the minimum number of pin pairs is approximately

$$n_{pairs} > \frac{I_{ave}}{I_{max\_pair}} = \frac{\langle power \rangle}{V_{dd} \times I_{max\_pair}} = \frac{10 \text{ watts}}{1\text{v} \times 0.25\text{A}} = 40 \quad (8.16)$$

This suggests another estimate for the loop inductance of the package PDN to be about

$$L_{loop} = \frac{1}{n_{pairs}} \times L_{per-len} \times Len = \frac{V_{dd} \times I_{max\_pair}}{\langle power \rangle} \times L_{per-len} \times Len \quad (8.17)$$

where

$n_{pairs}$  = the minimum number of power-ground pin pairs

$I_{max\_pair}$  = the maximum current capacity rating of any pair (in A)

$V_{dd}$  = the rail voltage (in v)

$\langle power \rangle$  = the average power dissipation of the core (in watts)

$L_{loop}$  = the equivalent loop inductance of the entire package's PDN (in pH)

$L_{per-len}$  = the loop inductance per length, (in pH/mil) with 20 pH/mil a good estimate

$Len$  = the effective length of each of the pairs (in mils)

The scaling is consistent with what would be expected. The loop inductance should increase with the inductance per length of each pair and the length of each pair. If the maximum current capacity increases, fewer pin pairs are needed and the loop inductance increases. If the average power dissipation of the core increases, the number of pin pairs would increase and the loop inductance would decrease.

For a moderate size device in a small, leaded package, we would estimate the features as

$$\text{Len} = 250 \text{ mils}$$

$$L_{\text{per-len}} = 20 \text{ pH/mil}$$

$$V_{dd} = 1 \text{ v}$$

$$I_{\text{max\_pair}} = 0.25 \text{ A}$$

$$\langle \text{power} \rangle = 5 \text{ watts}$$

We roughly estimate the total loop inductance of the package PDN as

$$L_{\text{loop}} = \frac{V_{dd} \times I_{\text{max\_pair}}}{\langle \text{power} \rangle} \times L_{\text{per-len}} \times \text{Len} = \frac{1 \times 0.25}{5} \times 20 \times 250 = 250 \text{ pH} \quad (8.18)$$

For the case of a large multilayer BGA, the features might be

$$\text{Len} = 100 \text{ mils}$$

$$L_{\text{per-len}} = 20 \text{ pH/mil}$$

$$V_{dd} = 1 \text{ v}$$

$$I_{\text{max\_pair}} = 0.25 \text{ A}$$

$$\langle \text{power} \rangle = 25 \text{ watts}$$

And the total loop inductance in the package PDN as

$$L_{\text{loop}} = \frac{V_{dd} \times I_{\text{max\_pair}}}{\langle \text{power} \rangle} \times L_{\text{per-len}} \times \text{Len} = \frac{1 \times 0.25}{25} \times 20 \times 100 = 20 \text{ pH} \quad (8.19)$$

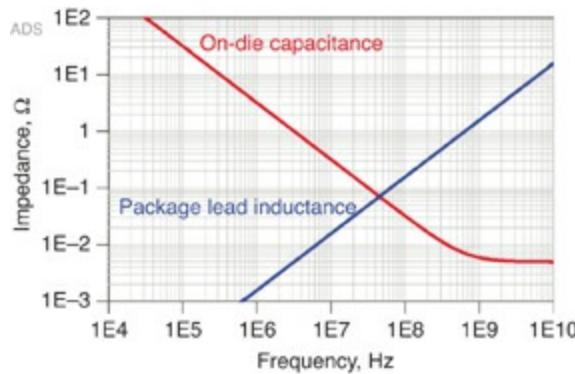
These are typical values of the package loop inductance that we might expect.

In addition to the loop inductance, some series resistance exists in each path. The series resistance of a via and solder ball is on the order of  $10 \text{ m}\Omega$ . The sheet resistance of a 1/2 oz copper is  $1 \text{ m}\Omega/\text{square}$ .

Interconnect traces implemented with as many as 10 squares total contribute approximately  $10 \text{ m}\Omega$  to series resistance.

The total ESR for a single power-ground pair path is  $20 \text{ m}\Omega$  in each leg or a total of  $40 \text{ m}\Omega$ . With 20 pairs in parallel, the effective ESR of the package path is on the order of  $2 \text{ m}\Omega$ . This is a small contribution to the total ESR compared with the on-die ESR of  $5 \text{ m}\Omega$ , associated with the  $50 \text{ nF}$  of on-die decoupling capacitance.

For example, [Figure 8.8](#) shows the impedance profile from the chip attach side of a package looking into the rest of the package, through the circuit board vias to the board's power and ground cavity, assuming the best case impedance on the board, where the cavity is shorted together. This impedance is for a typical small leaded chip scale package for a 5 watt device with  $L_{\text{loop}} = 250 \text{ pH}$ ,  $\text{ESR} = 5 \text{ m}\Omega$ , and on-die capacitance of  $50 \text{ nF}$ .



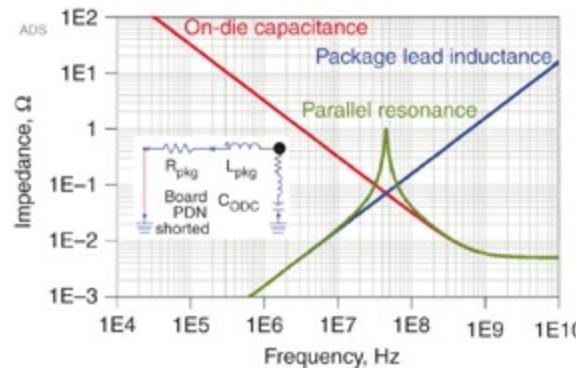
**Figure 8.8** Impedance profile of the package leads when the board side is shorted together using  $\text{ESL} = 250 \text{ pH}$ , and  $50 \text{ nF}$  on-die capacitance, with  $5 \text{ m}\Omega$  ESR simulated with Keysight's ADS.

## 8.4 THE BANDINI MOUNTAIN

The impedance profile from the die pads looking outward, especially at low frequency, depends on what is

connected to the other side of the package leads. When we take the “very best case,” and the impedance of the board PDN is the lowest possible, a dead short, the chip pads see the on-die decoupling capacitance and the package lead inductance in parallel. The combination of these two elements produces a parallel resonance, which is the most important feature in the PDN ecology.

Figure 8.9 shows the equivalent circuit from the die’s perspective and the resulting impedance profile for the case of an on-die decoupling capacitance of 50 nF, 5 mΩ, and 250 pH of package lead inductance.



**Figure 8.9** Impedance profile as seen by the die pads of the on-die capacitance and package lead inductance shorted on the board side. Simulated with Keysight’s ADS. Inset is the equivalent circuit model simulated.

This peak impedance at the parallel resonance of the on-die capacitance and the package loop inductance is a generic feature in all devices. This feature is usually the largest peak in the impedance profile and causes big problems if significant transient power currents exist with frequency components beyond this peak impedance. In this example, the parallel resonant frequency is about 45 MHz.

#### Tip

The parallel combination of the on-die capacitance and the package loop inductance creates a parallel resonance peak impedance, which is the most important feature of the entire PDN ecology and is the principle driving force in PDN design.

Here we see the first example of new emergent behavior when we start to build the PDN ecology. The interactions of the on-die decoupling capacitance and package loop inductance result in new behavior, which has very significant impact.

This feature in the PDN impedance profile has been coined by the late industry icon, Steve Weir, as the Bandini Mountain, named after the Bandini Fertilizer Company, formerly of Vernon, California.

Steve Weir was an early participant at DesignCon conferences and published many of the foundation building papers on PDN design principles [5]–[7]. He was also known for his wry sense of humor and the uncanny ability to see connections between widely different fields. This was fueled by his breadth of knowledge on the most esoteric topics.

He saw this parallel resonant peak in the PDN profile, often the most obnoxious feature in a PDN, and immediately saw its connection to an event that occurred during the 1984 summer Olympics, held in Los Angeles. This is the story that he would tell and why he coined this PDN peak, the Bandini Mountain.

The Bandini Fertilizer Company was a large fertilizer producer located southeast of downtown Los Angeles. To show off how large a supplier it was, it decided to capitalize on the publicity associated with the 1984 summer Olympics. So, it built a 100-foot-tall mountain of fertilizer and filmed commercials featuring its mountain as the backdrop to three different Olympic events.

It hired professional athletes to stage mock Olympic events featuring the mountain made of manure. There was a shotput, a triple jump, and a pole vault event, all staged with the Bandini Mountain as the target. Dave Kenworthy, the pole vaulter, later confessed to the *LA*

*Times* that when filming the commercial he did not actually land in a pile of manure but the commercials were filmed to certainly give that impression.

Unfortunately, so much money was spent on the commercials and they were so unsuccessful at increasing sales of fertilizer that the company soon went out of business, leaving behind the 100-foot-tall mountain of manure, in the summer time, near Los Angeles, with more than a million visitors attending the summer Olympics.

The local newspapers began referring to this abandoned mountain of fertilizer as the Bandini Mountain. Since then, the term *Bandini Mountain* has been associated with any tall pile of manure. This has led to a number of takeoffs, such as the t-shirt that reads:

“Good news: you are king of the mountain. Bad news: it’s the Bandini Mountain.”

When the PDN impedance profile is observed from the die’s perspective, the parallel resonance peak impedance looks surprisingly like a mountain. Because the role it plays in the PDN is so odorous, Steve Weir immediately saw the connection and would jokingly refer to this impedance peak as the Bandini Mountain, an apt description.

The peak impedance value of the Bandini Mountain is mostly related to the q-factor of the LC resonator, which is related to the ESR of the two elements. The ESR of the package leads and the ESR of the on-die capacitor often contribute to a high q-factor for the resonant peak impedance with values approaching  $1 \Omega$ .

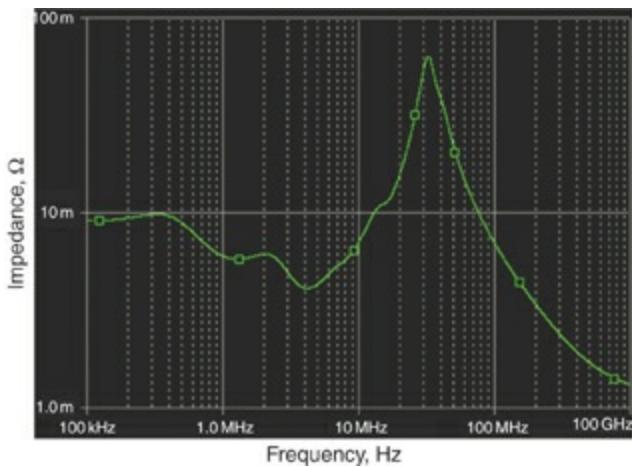
The frequency of the Bandini Mountain peak impedance depends on the parallel resonant frequency, which we get with

$$f_{\text{Bandini}}[\text{MHz}] = \frac{1}{2\pi\sqrt{L_{\text{pkg}}C_{\text{ODC}}}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{pkg}}[\text{nH}]C_{\text{ODC}}[\text{nF}]}} \quad (8.20)$$

In Figure 8.9, the predicted parallel resonant frequency from the 50 nF on-die capacitance and 250 pH of package lead inductance is

$$f_{\text{Bandini}}[\text{MHz}] = \frac{159 \text{ MHz}}{\sqrt{L_{\text{pkg}}[\text{nH}]C_{\text{ODC}}[\text{nF}]}} = \frac{159 \text{ MHz}}{\sqrt{0.25\text{nH} \times 50\text{nF}}} = 45 \text{ MHz} \quad (8.21)$$

The Bandini Mountain always involves the on-die capacitance looking out into the package loop inductance and is a feature of all PDNs. The use of on-package decoupling capacitors can mitigate the peak by reducing the loop inductance and providing damping resistance but an impedance peak is still associated with the on-die capacitance and package loop inductance. Figure 8.10 is an example of the measured impedance profile of a chip in a BGA package, showing its Bandini Mountain.



**Figure 8.10** Measured impedance profile of a test chip showing the Bandini Mountain at 33 MHz

#### Tip

The Bandini Mountain is the most important feature in the PDN ecology, yet it is also the most difficult to get accurate design information about because it must come from the semiconductor vendor.

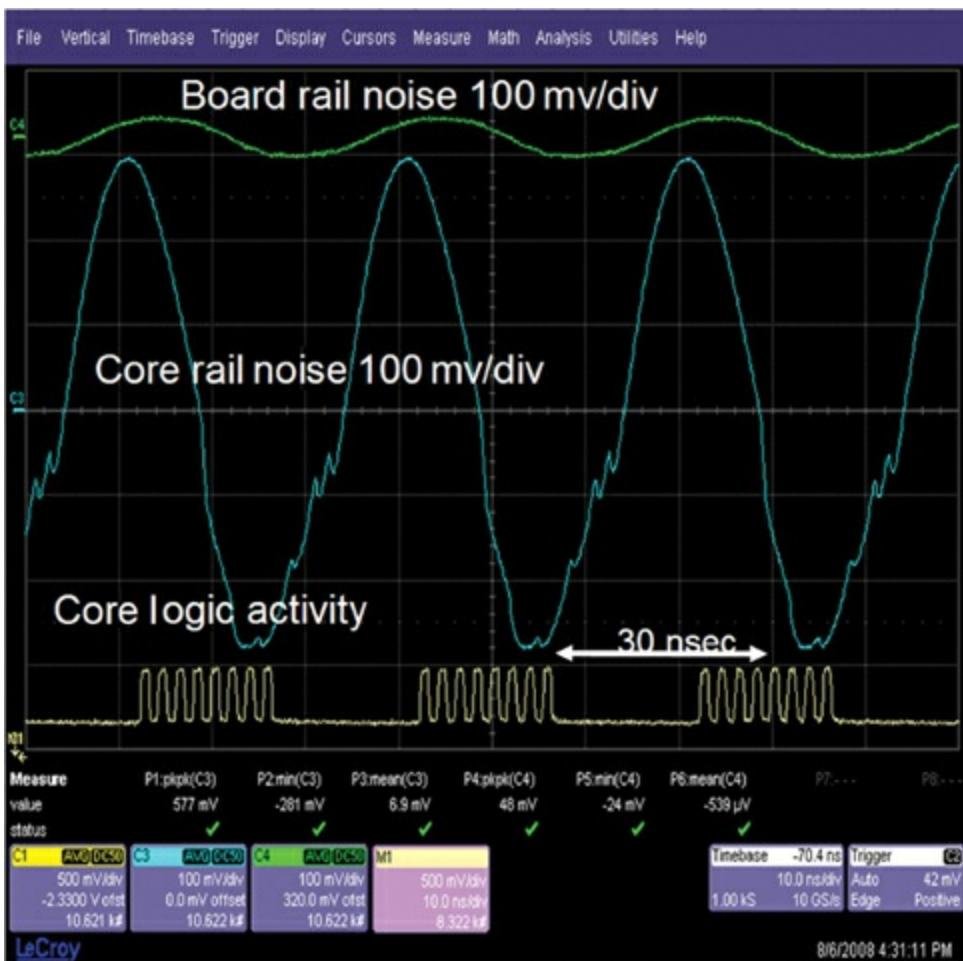
In general, estimating the value of the Bandini Mountain frequency is difficult because it depends on just how much on-die decoupling capacitance is present and the package loop inductance. These values vary depending on the specific chip and the specific package selection.

Although the semiconductor vendors usually know these PDN parameters for their devices, they are reluctant to release this information. The possibility exists to make power “viruses” that stimulate the impedance peak. Microcode could be written that rapidly toggles a large number of gates and modulate power at the Bandini Mountain frequency. This would drive the maximum PDN transient current with a dangerous first harmonic through the Bandini Mountain peak impedance. A large modulated current through a high impedance results in a large voltage noise amplitude on the power rail.

**Tip**

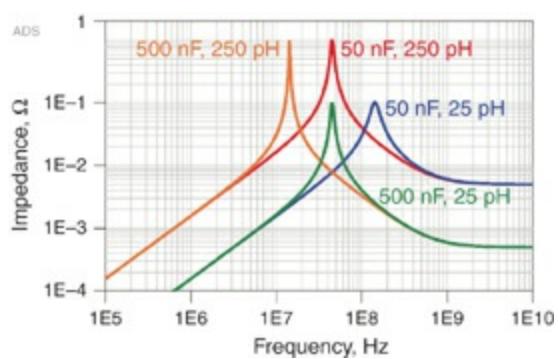
Semiconductor suppliers are reluctant to reveal such vulnerabilities of their devices. The Bandini Mountain is difficult and expensive to fix.

In the case of the Bandini Mountain peak frequency of 33 MHz in [Figure 8.10](#), transient currents generated in the on-die PDN with large amplitudes at 33 MHz would flow through this peak impedance resulting in large voltages at the die circuits. [Figure 8.11](#) is an example of the measured rail voltage with large transient currents switching at 33 MHz in this test chip. The on-die voltage noise of 600 mV peak to peak would exceed any reasonable noise budget. We provide more details on how this voltage was measured and the PDN circuit parameters that enabled it in [Chapter 10](#).



**Figure 8.11** Measured voltage noise on the die rails and on the board when the maximum transient currents had a large first harmonic at the Bandini Mountain frequency.

Unfortunately, the two dominant features that most strongly influence the peak impedance of the Bandini Mountain, the on-die decoupling capacitance and the package lead inductance, are not accessible to most designers. They are determined by the semiconductor vendor. Increasing the on-die decoupling capacitance and decreasing the package lead inductance will both significantly reduce the peak impedance. [Figure 8.12](#) is an example of the impedance profile with four different combinations of on-die capacitance and package loop inductance and an ESR that scales inversely with the on-die capacitance.



**Figure 8.12** Impedance profiles of just the on-die decoupling capacitance and the package lead inductance for the four combinations shown.

The Bandini Mountain impedance peak is not related to the power plane cavity impedance peaks discussed in Chapters 6 and 7. Those impedance peaks were measured by probing the power planes directly. The Bandini Mountain impedance peak is measured by probing the on-die capacitance, as difficult as that might be.

For power integrity purposes, we are concerned about the quality of the PDN voltage at the silicon circuit terminals. Above the Bandini peak frequency, the on-die capacitance controls the on-die PDN impedance. The package and board inductance together with the on-die capacitance are responsible for the Bandini peak and filters any power cavity resonance that might be present at the board level. This is where board-level signal integrity issues are divorced from the on-die power integrity issues.

**Tip**

The only good thing about the Bandini Mountain is that it allows us to separate signal integrity and power integrity problems at a specific frequency.

## 8.5 ESTIMATING THE TYPICAL BANDINI MOUNTAIN FREQUENCY

Knowing the Bandini Mountain frequency is important.

*Always ask the semiconductor vendor for information about the on-die decoupling capacitance and package PDN inductance. Sometimes, this information is released under NDA. When the on-die capacitance and package lead inductance are known, the intrinsic Bandini Mountain frequency, when the board looks like a dead short, is simply given by*

$$f_{\text{Bandini}} [\text{GHz}] = \frac{1}{2\pi} \frac{1}{\sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]}} \quad (8.22)$$

For example, if the on-die capacitance is 50 nF and the package lead inductance is 0.25 nH, we estimate the Bandini Mountain frequency as

$$f_{\text{Bandini}} [\text{GHz}] = \frac{1}{2\pi} \frac{1}{\sqrt{50 \text{nF} \times 0.25 \text{nH}}} = 45 \text{MHz} \quad (8.23)$$

However, in the absence of good input, and using the general rule that “Sometimes an okay answer NOW! is better than a good answer late,” we can roughly estimate where the Bandini Mountain frequency should appear based on the simple model we developed earlier for the on-die decoupling capacitance and the package loop inductance. We can also measure the on-die decoupling capacitance using VNA techniques described in a previous chapter.

We developed the simple estimates of

$$C_{\text{ODC}} = 9 \times \frac{\langle \text{power} \rangle}{V_{\text{dd}}^2 \times F_{\text{clock}}} \quad \text{and} \quad L_{\text{loop}} = \frac{V_{\text{dd}} \times I_{\text{max\_pair}} \times L_{\text{per-len}} \times Len}{\langle \text{power} \rangle} \quad (8.24)$$

where

$C_{\text{ODC}}$  = the on die capacitance in nF

$\langle \text{power} \rangle$  = the average power in watts

$V_{\text{dd}}$  = the Vdd voltage rail in v

$F_{\text{clock}}$  = the clock frequency in GHz

$L_{loop}$  = the loop inductance in nH

$I_{max\_pair}$  = the maximum current carrying capacity of a power-ground pair, in A

$L_{per\_len}$  = the loop inductance per length of a power and ground lead pair in nH/inch, roughly 20 nH/inch

Len = the lead length in inches

Combining these together with the peak impedance frequency, the Bandini Mountain frequency is

$$f_{Bandini} = \frac{159 \text{ MHz}}{\sqrt{\frac{V_{dd} \times I_{max\_pair}}{\langle \text{power} \rangle} \times L_{per\_len} \times Len \times 9 \times \frac{\langle \text{power} \rangle}{V_{dd}^2 \times F_{clock}}}} \quad (8.25)$$
$$= 53 \text{ MHz} \sqrt{\frac{V_{dd} \times F_{clock} [\text{GHz}]}{I_{max\_pair} \times L_{per\_len} \times Len [\text{inches}]}}$$

Remarkably, the average power of the device cancels out. The higher the power dissipation, the larger the on-die capacitance should be. But the higher the power dissipation, the lower the equivalent loop inductance should be due to the many more leads required in parallel to handle the higher current. Because the Bandini Mountain frequency is related to the product of the C and L, the impact from the average power disappears.

Using this simple relationship, we explore some typical examples to estimate the resulting Bandini Mountain frequency range we might expect.

At the lower frequency end, we could imagine a QFP packaged device operating at 250 MHz and expect a Bandini frequency, based on

$V_{dd} = 1 \text{ V}$

$F_{clock} = 0.25 \text{ GHz}$

$I_{max\_pair} = 0.5 \text{ A}$

$$L_{\text{per-len}} = 20 \text{ nH/inch}$$

$$\text{Len} = 0.5 \text{ inches}$$

resulting in a Bandini Mountain frequency of roughly

$$f_{\text{Bandini}} = 53 \text{ MHz} \sqrt{\frac{V_{dd} \times F_{\text{clock}} [\text{GHz}]}{I_{\text{max}} \times L_{\text{per-len}} \times \text{Len} [\text{inches}]}} = 53 \text{ MHz} \sqrt{\frac{1 \times 0.25}{0.5 \times 20 \times 0.5}} = 12 \text{ MHz} \quad (8.26)$$

At the other extreme, if there were a high-performance package with a combination of circuit board via length, solder ball length, and C4 length, with multiple internal planes, the total path length might be as short as 50 mils, operating at a 3 GHz frequency, and with  $I_{\text{max\_pair}} = 0.5 \text{ A}$ , resulting in a Bandini frequency of

$$f_{\text{Bandini}} = 53 \text{ MHz} \sqrt{\frac{V_{dd} \times F_{\text{clock}} [\text{GHz}]}{I_{\text{max}} \times L_{\text{per-len}} \times \text{Len} [\text{inches}]}} = 53 \text{ MHz} \sqrt{\frac{1 \times 3}{0.5 \times 20 \times 0.05}} = 130 \text{ MHz} \quad (8.27)$$

These examples represent two rather extreme situations that give reasonable bounds for the sort of values expected for the Bandini frequency, roughly in the 10 MHz to 100 MHz range.

For the highest performance devices, the Bandini Mountain frequency is in the 100 MHz range. The highest performance devices are also likely to have on-package decoupling capacitors (OPD). The loop inductance from the ODC to the OPD is usually the biggest challenge. Although some design philosophies call for the series resonant frequency of the OPD to sit right on top of the Bandini Mountain, this is seldom done. Manufacturing tolerances and the readily available capacitor values make this difficult.

Usually the lowest possible loop inductance is engineered for the package path between the die pads and the OPD. The OPD is sized to have at least five times the capacitance of the ODC. For damping purposes, having the ESR for the OPD close to the target

impedance is desirable. With this design philosophy, the OPD significantly reduces the height of the Bandini Mountain but does not eliminate it. The most OPD benefit is obtained with minimum loop inductance and optimum damping from the OPD. This often provides the board relief by minimizing the number of high-frequency board capacitors required.

This suggests that in the absence of detailed information about the specifics of the semiconductor device, assuming a value of the Bandini frequency in the range 10 MHz to 50 MHz is not unreasonable. For very high-end devices, such as communications devices and some memory circuits, it could be as high as 200 MHz.

**Tip**

The reason that knowing the on-die capacitance and the equivalent package lead inductance is so important is to know the properties of the Bandini Mountain. In the absence of accurate values, estimate the features using the reverse-engineering methods discussed previously.

Good reasons actually exist as to why you will rarely get Bandini Mountain parameters from semiconductor suppliers. For power integrity engineers, the Bandini Mountain is the most challenging aspect of PDN design. To a large extent, it determines the performance of the PDN and the performance of circuits that draw power from it. As demonstrated in [Chapters 9 and 10](#), the step response and resonance response noise is directly proportional to its characteristics and height.

PI engineers know exactly how to fix it. You just add on-die capacitance or reduce the package loop inductance, both of which are outrageously expensive.

If customers find out about the PDN parameters that generate the Bandini Mountain impedance peak and compare it to the target impedance, they are likely to

demand that it be fixed. Fixing the Bandini Mountain to the point where the target impedance is met would make the product so expensive that few customers would be willing to buy it. They will go somewhere else to save costs.

This is why silicon customers rarely get the PDN parameters necessary for an accurate simulation of the Bandini Mountain from their semiconductor suppliers. It is also why this odorous problem has acquired this appropriate name.

## 8.6 INTRINSIC DAMPING OF THE BANDINI MOUNTAIN

In any parallel circuit, four performance metrics describe the important features of the circuit: the parallel resonant frequency, the characteristic impedance, the peak impedance at the resonance frequency, and the quality factor or q-factor, which describes the damping.

PRF,  $Z_0$ ,  $Z_{peak}$ , q-factor

The characteristic impedance of a parallel resonant circuit depends only on the L and C values that make up the circuit.

When describing transmission lines, we refer to the instantaneous impedance the signal sees as it propagates as an impedance that characterizes the transmission line. This instantaneous impedance is defined as the *characteristic impedance* of the transmission line. Knowing the characteristic impedance tells us the one and only instantaneous impedance a signal would see.

In the same way, the characteristic impedance of a parallel resonant LC circuit characterizes the circuit. We often refer to this impedance as the *characteristic impedance* of the circuit.

In both cases, the characteristic impedance is the

impedance value where the inductive reactance crosses capacitive reactance.

**Tip**

Although the words we use are the same, the characteristic impedance of a transmission line and the characteristic impedance of a parallel LC circuit do not refer to the same fundamental property. They are just both impedances that characterize the structures.

In the simple parallel RLC circuit introduced to illustrate the Bandini Mountain, with  $L = 0.25 \text{ nH}$  and  $C = 50 \text{ nF}$  capacitance, we derive the characteristic impedance of the circuit with

$$Z_0[\Omega] = \sqrt{\frac{L_{\text{pkg}}[\text{nH}]}{C_{\text{ODC}}[\text{nF}]}} = \sqrt{\frac{0.25 \text{ nH}}{50 \text{ nF}}} = 0.071 \Omega \quad (8.28)$$

The characteristic impedance of the Bandini Mountain peak relates to two important performance features. The characteristic impedance establishes the lowest impedance that we can achieve for the PDN under the best conditions.

Second, as we show in Chapter 9, the characteristic impedance of the parallel resonant peak also relates to the transient voltage drop for a step current stimulus.

We derive the resonant frequency of the Bandini Mountain for this example with

$$f_{\text{Bandini}}[\text{GHz}] = \frac{1}{2\pi} \frac{1}{\sqrt{C_{\text{ODC}}[\text{nF}] \times L_{\text{package}}[\text{nH}]}} = \frac{1}{2\pi} \frac{1}{\sqrt{50 \text{ nF} \times 0.25 \text{ nH}}} = 45 \text{ MHz} \quad (8.29)$$

The q-factor of this parallel resonant circuit and the estimated peak impedance depend on the loss or damping in the circuit. This is related to the ESR of the on-die decoupling capacitance and the series resistance of the board-level losses such as from package leads, on-package capacitors, board-level interconnects, and

MLCC capacitors.

When the board-level losses are much less than those from on-die resistance, the main source of damping of the Bandini Mountain is the ESR on die. Using the rule of thumb introduced earlier that the on-die RC time constant is roughly 0.25 ns, we can estimate the q-factor for the Bandini Mountain in this special case.

$$q\text{-factor} = \frac{1}{ESR} \sqrt{\frac{L_{\text{package}}}{C_{\text{ODC}}}} = \frac{C_{\text{ODC}} [\text{nF}]}{0.25} \sqrt{\frac{L_{\text{package}}}{C_{\text{ODC}}}} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} \quad (8.30)$$

For example, for the case of a 50 nF ODC and 250 pH package lead inductance, we estimate the ESR as

$$ESR = \frac{0.25}{50 \text{nF}} = 5 \text{ m}\Omega \quad (8.31)$$

The q-factor is

$$q\text{-factor} = \frac{Z_0}{R} = \frac{0.071\Omega}{0.005\Omega} = 14 \quad (8.32)$$

or

$$q\text{-factor} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} = \frac{1}{0.25} \sqrt{50 \times 0.25} = 14 \quad (8.33)$$

Note the similarity of the q-factor to the frequency of the Bandini Mountain. Using this relationship, we can relate the q-factor to the frequency of the Bandini Mountain as

$$q\text{-factor} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} = \frac{1}{0.25} \frac{1}{2\pi f_{\text{Bandini}} [\text{GHz}]} = \frac{0.64}{f_{\text{Bandini}} [\text{GHz}]} \quad (8.34)$$

For example, if the *only* source of damping is from the on-die resistance and the Bandini Mountain peak impedance is 45 MHz, the q-factor is

$$q\text{-factor} = \frac{0.64}{f_{\text{Bandini}} [\text{GHz}]} = \frac{0.64}{0.045} = 14 \quad (8.35)$$

This is a very high q-factor. If this were the q-factor of the Bandini Mountain, when connected to the rest of the PDN ecology we would need other damping sources to bring the Bandini Mountain peak impedance down to acceptable limits.

The maximum frequency limit ( $f_{\text{max\_limit}}$ ) is the frequency where q-factor is no longer important. It is taken as 200 MHz.

$$\text{q-factor} = \frac{0.64}{f_{\text{Bandini}} [\text{GHz}]} = \frac{0.64}{0.2} = 3.2 \quad (8.36)$$

This suggests that to keep the q-factor low and the Bandini Mountain peak impedance low, higher frequency Bandini Mountain parallel resonances are better. One driving force is the package lead inductance. Lower is always better.

#### Tip

If the damping is due only to on-die resistance, Bandini Mountain frequencies above 200 MHz will have a q-factor smaller than 3. At this level, board-level damping sources will have only a small impact on the Bandini Mountain.

The peak impedance of the Bandini Mountain, when the **only damping is from on-die resistance**, is related to the q-factor and the characteristic impedance as

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{1}{\text{ESR}} \frac{L_{\text{package}}}{C_{\text{ODC}}} = \frac{C_{\text{ODC}} [\text{nF}]}{0.25} \frac{L_{\text{package}} [\text{nH}]}{C_{\text{ODC}} [\text{nF}]} = \frac{L_{\text{package}} [\text{nH}]}{0.25} \quad (8.37)$$

This suggests a rather remarkable behavior. The peak impedance of the Bandini Mountain, when the only source of damping is the on-die ESR, is independent of the on-die capacitance and depends only on the package lead inductance and 250 ps RC time constant. This is exactly what we observed in [Figure 8.12](#). For the two cases with the same ESL, the peak impedances were

identical, even though the on-die capacitance varied by 10 times.

When the  $\text{ESL} = 0.025 \text{ nH}$ , we estimate the peak impedance to be  $0.1 \Omega$ . This again, is exactly what was simulated.

This analysis suggests that to achieve a peak impedance below  $10 \text{ m}\Omega$  requires a package lead inductance of about  $2.5 \text{ pH}$ .

**Tip**

When the intrinsic damping of the Bandini Mountain resonance is dominated by the on-die resistance, the peak impedance height is directly related to the package lead inductance. This is another reason why we should reduce package lead inductance as low as possible. A lower package lead inductance results in a lower peak impedance.

These estimates for the peak impedance and q-factor of the Bandini Mountain are the worst-case estimates because the board is assumed to be lossless. There will always be some damping from the package and board-level interconnects to reduce the q-factor and reduce the peak height.

**Tip**

In high q-factor Bandini Mountain systems, such as when the peak frequency is below 200 MHz, resistive board-level features can be important engineering levers to reduce the Bandini Mountain peak height.

This relationship for the peak impedance clearly identifies the three important design knobs to adjust to reduce the peak impedance of the Bandini Mountain:

- Decrease the package lead inductance
- Increase the on-die decoupling capacitance
- Increase the ESR of the package loop or the on-die capacitance

We explore these design elements in a later section.

## 8.7 THE POWER-GROUND PLANES WITH MULTIPLE VIA PAIR CONTACTS

The balls of the package connect to vias in the circuit board and then to the buried power and ground planes that make up the cavity in the board. The impedance of the cavity, as viewed from a power and ground via pair, can only be accurately simulated using a 3D full-wave field solver that takes into account the shape of the planes, their physical features, and the observation points. In this section we consider the cavity and VRM. In the next section we include the packaged die.

The output of all 3D full-wave field solvers is an S-parameter file based on the ports set up as observation points into the cavity. These S-parameter models are really equivalent circuit models of the cavity's electrical properties as viewed from the ports.

For example, we expect a square cavity 5 inches on a side and 10 mils thick filled with FR4 to have a capacitive impedance profile at low frequency. When viewed from a central point, we expect a self-resonance dip followed by the peaks of the cavity modal resonances. To get the impedance profile, we simulate the S-parameters and then convert the impedance from the one-port S-parameters using

$$Z_{11} = 50\Omega \frac{1+S_{11}}{1-S_{11}} \quad (8.38)$$

where

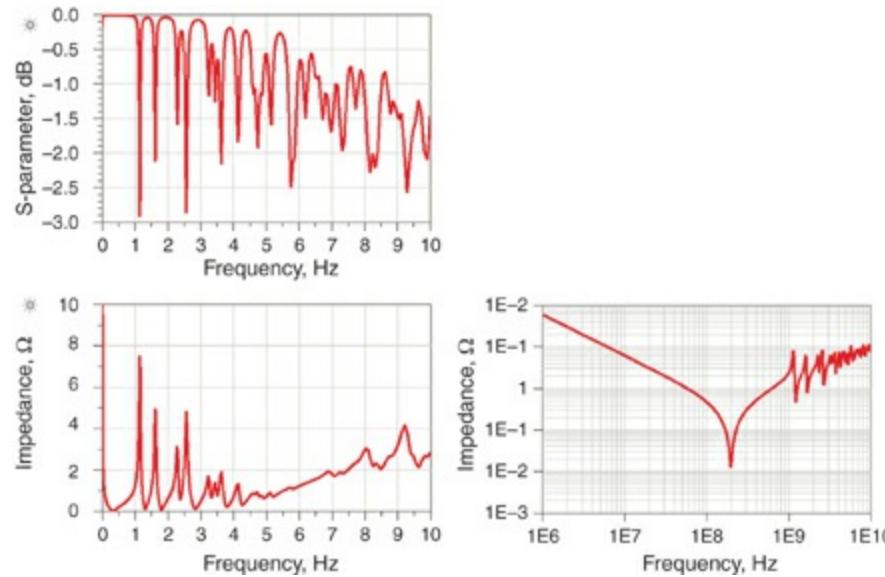
$Z_{11}$  = the impedance looking into the cavity from the observation port, often referred to as the “self” impedance

$S_{11}$  = the computed return loss from the port 1 connection to the cavity

(Note: Both  $Z_{11}$  and  $S_{11}$  are complex numbers and vary with frequency.)

Although the expected impedance profile is obvious, imagining the S-parameter behavior is much more difficult because much of its valuable information is actually in the phase. This is why the impedance profile is preferred even though we actually simulate S-parameters. We can easily interpret features of the impedance profile on log scales compared to S-parameters.

Figure 8.13 shows the S-parameters simulated for this cavity and the resulting impedance profile from one observation point at the center of the cavity.



**Figure 8.13** S-parameters and impedance profile for a cavity 5 inches on a side, probed from the center, on a linear frequency scale, compared to the more conventional log-log plot of impedance on the right, simulated with Mentor Graphics HyperLynx PI.

When the package has multiple via contacts into the board-level cavity, the S-parameter model has multiple ports. Using the S-parameter file as a behavioral circuit model, we can parallel up all the ports and extract the equivalent impedance the multiple ports see looking into the board-level cavity. This is the equivalent

impedance a BGA package sees looking into several PCB vias connected to the board-level cavity.

We expect that at low frequency, whether we have 1 port or 10 ports in parallel looking into the cavity, we will see the same impedance associated with the capacitance of the cavity from each port.

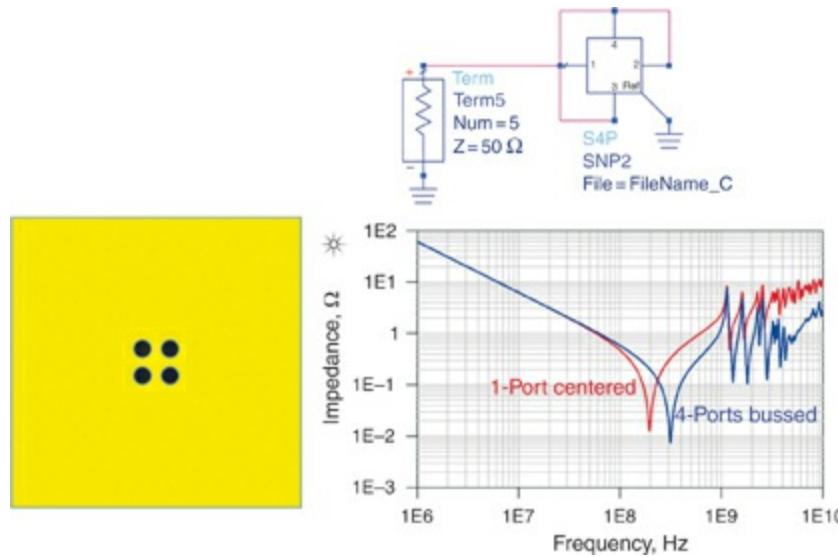
In the frequency regime where inductance plays a role, how the cavity is contacted will influence the spreading inductance and the impedance profile.

A single port on single via pair is likely to have a significant and dominant inductance into the cavity whereas the parallel combination of many via loop inductances may be insignificant compared to the spreading inductance into the cavity. By placing multiple via pairs in parallel, the effect of the vias is diminished leaving just the cavity inductance. This shifts the self-resonant frequency to higher frequency with more ports in parallel.

This is consistent with the equivalent lumped LC model for a via looking into a cavity discussed in [Chapter 6](#). The impedance dip is similar to that of a series LC circuit. When four vias access the cavity, the ESL from parallel vias and larger effective diameter probing into the cavity reduce the inductance to the plane capacitance. The cavity capacitance remains the same so the frequency of the dip is increased.

The modal frequencies of the cavity should not be significantly changed with multiple parallel contacts to the cavity. The modal resonant peaks are due to multiples of one-half wavelength fitting into the cavity. A via or multiple vias positioned in the cavity have little effect on the wave velocity or time of flight between cavity boundaries. The modal resonant peak frequencies are not expected to change with the addition of measurement vias into the cavity.

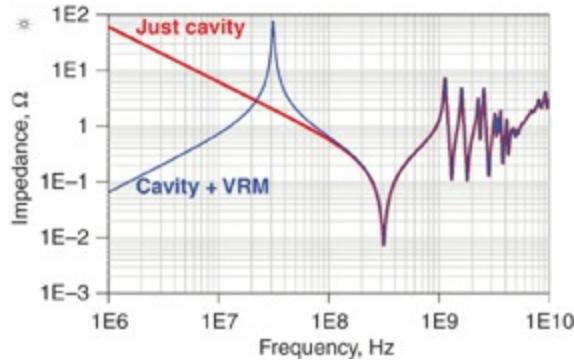
For example, when four parallel via pairs in close proximity contact the cavity, we can calculate the impedance each sees in the cavity by assigning each via pair a port, and then parallel them up in circuit simulation as a self-impedance. [Figure 8.14](#) shows an example of the location of the four ports on the cavity, the circuit that connects the four ports in parallel, and the resulting self-impedance compared with a single port making contact to the center of the cavity.



**Figure 8.14** Comparing the simulated impedance profile extracted from a 3D field solver for a cavity probed at one contact via and at four contact vias in parallel and the circuit used to bus the four ports in parallel. Note, the impact of the four points in parallel is to decrease the spreading and BGA via inductance into the cavity. The modal resonances are at the same frequencies.

More typically, a VRM is connected to the cavity. As discussed in [Chapter 3](#), we can approximate a VRM as a series combination of R and L elements. This simple model does not include any bulk capacitor associated with the VRM for now. A simple VRM with  $R = 1 \text{ m}\Omega$  and  $L = 10 \text{ nH}$  was connected between the power and ground planes of the cavity in [Figure 8.14](#) and probed at four contact points. The simulated four-port S-parameters were bussed together in a circuit simulator.

Figure 8.15 shows the simulated impedance representing the VRM only connected to the cavity compared to the empty cavity.



**Figure 8.15** Impedance profiles of the same cavity with and without a VRM attached. Simulated with Mentor Graphics HyperLynx PI.

The parameters for this simulation example were

Cavity size: 5 inches  $\times$  5 inches

Cavity thickness: 10 mils

Cavity Dk = 4.3

VRM inductance = 10 nH

VRM series resistance = 1 m $\Omega$

In this way, we are able to account for the impedance profile of the cavity when viewed by multiple via contacts from a package, including other components connected to the cavity. The dominant impact of multiple contacts to the cavity is to decrease the spreading and BGA via inductance into the cavity.

## 8.8 LOOKING FROM THE CHIP THROUGH THE PACKAGE INTO THE PCB CAVITY

We now add the package and die to the simulation of the VRM and S-parameter model of the cavity shown in the previous section. One of the important features we see looking into the impedance of a board cavity is the cavity modal resonances above 1 GHz. Although these represent high peak impedances and are of significant

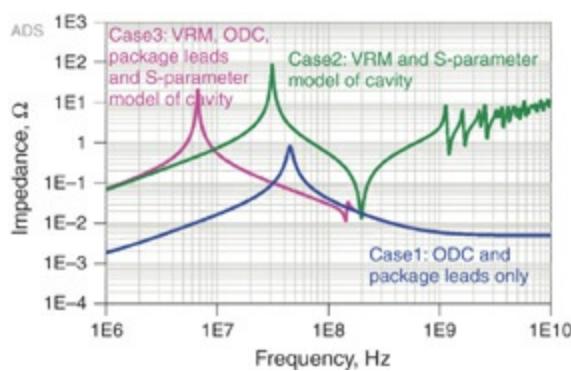
concern for signal integrity and EMI/EMC problems, they are not seen by the die pads and do not affect the power quality for the on-die circuits.

When looking through the package, the die sees the rest of the board through the package loop inductance, which increases with higher frequency. It sees the on-die decoupling capacitance whose impedance increases at the Bandini frequency when interacting with the package inductance. This means the impedances of the cavity resonances, usually much higher than the Bandini Mountain frequency, are filtered through the higher impedance and play no role for the on-die impedance and on-die PDN noise. This is in striking contrast to the case when signals see the noisy environment of the cavity directly.

We illustrate this with a simple example. The on-die capacitance is 50 nF with 5 mΩ ESR and the package lead inductance is 250 pH. The board-level cavity is 5 inches on a side, with a spacing between the planes of 10 mils. A simple VRM is connected to the cavity. We explore the simulated impedance profiles of three cases:

- **Case 1:** The impedance from the die pads with the ODC and package lead inductance alone, with the ends of the package shorted to Vss.
- **Case 2:** The impedance of the cavity with the simple VRM alone, as viewed at the PCB vias where the package would normally attach.
- **Case 3:** The impedance from the die pads, looking through the package to the cavity with the simple VRM attached.

Figure 8.16 shows the simulated impedance profiles.



**Figure 8.16** Impedance profiles for three cases. The PCB modal cavity resonances are not visible to the die after the filtering effect of the package inductance and on-die capacitance. Simulated with Keysight's ADS.

When the package leads on the board side are connected to Vss in case 1 (with the package and ODC alone) the impedance seen by the die pads is low at low frequency. It's just the shorted lead inductance. The parallel resonant peak at about 45 MHz is from the package inductance and the on-die capacitance.

The impedance of case 2 (looking into the board cavity with the simple VRM) shows the VRM inductance at low frequency. The parallel resonance peak at about 30 MHz is from the VRM inductance and the cavity capacitance. The impedance dip at about 200 MHz is the series LC resonance of the cavity discussed in Chapters 6 and 7. Board modal resonances are clearly visible at high frequency, above 1 GHz.

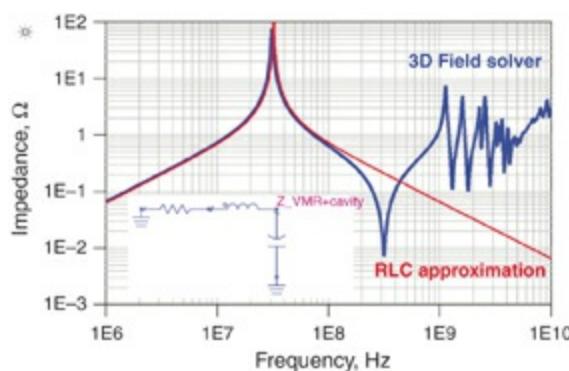
In case 3, the package loop inductance includes the cavity connected to the VRM, about 10 nH. Viewed from the package die pads, the on-die capacitance is in parallel with the package loop inductance and VRM inductance because both are in series to ground. This shifts the impedance peak to much lower frequency. The Bandini Mountain, which is the parallel combination of on-die capacitance looking out into the package loop inductance, is very high. Compared to the shorted package, the Bandini Mountain peak frequency is now at 7 MHz, shifted down from 45 MHz.

The die pads see none of the cavity resonances. The package inductance together with the on-die capacitance forms a filter that hides the board cavity resonances from the die. The same impedances that form the Bandini Mountain also form the filter that hides the board modal resonances from the die circuits. The on-die capacitance makes an impedance much lower than the board cavity.

One new feature in the impedance profile is seen by the die pads when the cavity is attached. At about 180 MHz, there is a small impedance disturbance, both a peak and a dip. This is due in large part to the parallel circuit of the package lead inductance and spreading inductance of the cavity, with the cavity capacitance. This feature is shifted to slightly lower frequency than the series resonance impedance dip of the cavity spreading inductance and the cavity capacitance, due to the slightly higher loop inductance of the package leads.

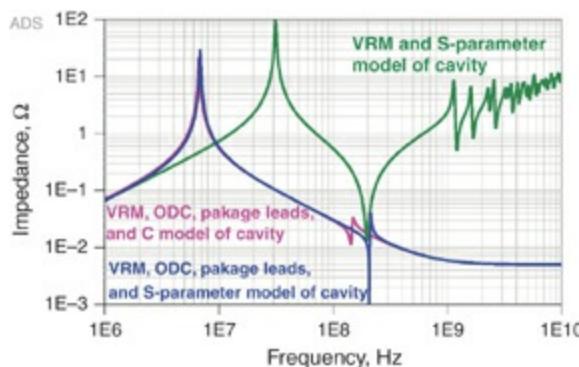
Above this frequency, the impedance seen by the die pads is due to the on-die decoupling capacitance. Below this frequency, the impedance is the parallel combination of both the on-die decoupling and the cavity capacitance, resulting in a slightly lower impedance. This is demonstrated by simplifying the model of the cavity to include just its capacitance and showing that these impedance features are still present.

The simplest model for the cavity is an ideal capacitor. With the VRM attached, the equivalent circuit is the R and L of the VRM in parallel with the cavity capacitance because the cavity capacitance returns to ground. The cavity impedance from the 3D field solver with the VRM attached is compared in [Figure 8.17](#) to this simple lumped circuit model where the cavity capacitance is estimated from the dimensions.



**Figure 8.17** Impedance profiles of the VRM connected to the cavity extracted with a 3D field solver and using a simple lumped circuit approximation based on the dimensions of the cavity.

Using this approximation, the impedance profile is well matched up to 100 MHz where the spreading inductance effects in the cavity, which are not included in the simple model, become apparent. We use this approximate lumped circuit model of the cavity and the VRM connected to the package lead inductance to explore what the die pads see, compared to the 3D model of the cavity. [Figure 8.18](#) compares the impedance seen in the cavity itself, and by the die pads for these three cases: the S-parameter, 3D cavity model, and the lumped capacitance cavity model.



**Figure 8.18** The impedance as *seen* in the cavity and at the die pads for the package connected to the 3D S-parameter cavity model and VRM with the simple RLC cavity model.

Remarkably, the impedance profiles as seen from the die pads are similar for the 3D cavity model and the simple RLC model. The small impedance disturbance at

about 180 MHz and the shift in the impedance line at this frequency are apparent in both cases. The disturbance is due to the interaction of the cavity capacitance and package or cavity spreading inductance. In this example, the cavity capacitance was about 7.2 nF and the package lead inductance was 0.25 nH.

This small disturbance is not sensitive to changing the VRM inductance but very sensitive to changing the cavity capacitance.

**Tip**

This analysis demonstrates that the cavity has little impact on the impedance as seen by the die pads. The cavity is mostly transparent for the die pads looking into the board cavity through the package.

To account for the peak impedance associated with the cavity, adding a capacitor in parallel with the PDN corresponding to the cavity capacitance is usually sufficient. This dramatically simplifies the modeling of the PDN profile. The cavity modal resonances are not important for the power integrity problem.

## **8.9 ROLE OF THE CAVITY: SMALL BOARDS, LARGE BOARDS, AND “POWER PUDDLES”**

From the die pad’s perspective, looking through the package into the board, the cavity resonances play no role at all. The cavity behaves just like a lumped capacitor. This means that other than contributing spreading inductance between the MLCC capacitors and the pads of the BGA, the cavity’s properties have little impact on power integrity applications. We can make this same comment for the package power planes. The plane capacitance and cavity resonances do not disturb low impedance power to the core logic because they are overwhelmed by the on-die capacitance. Spreading

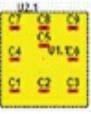
inductance is the significant property of cavities.

The following example illustrates this effect. The impedance looking into a 10 mil thick cavity was simulated and observed from a central observation point using  $S_{11}$  and  $Z_{11}$  techniques. On the cavity were nine decoupling capacitors each of  $100 \mu\text{F}$  with  $1 \text{nH}$  of mounting inductance and  $25 \text{ m}\Omega$  ESR. The impedance and S-parameters from two different size cavities were simulated; one cavity was 1 inch on a side and the other cavity was 10 inches on a side. This is a factor of 100 difference in cavity capacitance. The value of the capacitances of the two cavities are

$$C_{\text{cavity-1inch}} = 0.225 \frac{\text{pF}}{\text{inch}} \times Dk \times \frac{A}{h} = 0.225 \frac{\text{pF}}{\text{inch}} \times 4.3 \times \frac{1 \text{inch}^2}{0.01 \text{inch}} = 0.1 \text{nF} \quad (8.39)$$

$$C_{\text{cavity-10inch}} = 0.225 \frac{\text{pF}}{\text{inch}} \times Dk \times \frac{A}{h} = 0.225 \frac{\text{pF}}{\text{inch}} \times 4.3 \times \frac{100 \text{inch}^2}{0.01 \text{inch}} = 10 \text{nF} \quad (8.40)$$

Figure 8.19 shows these two cavities at relative scale.



**Figure 8.19** The two cavities in this example, to scale.

The one on the left is 1 inch on a side, and the one on the right is 10 inches on a side. Each has nine capacitors.

The impedance is simulated from the center.

The impedance as seen at the center of the cavity with just capacitors added has four distinctive impedance features.

At the lowest frequency, the impedance is related to the capacitance of the capacitors. For these two cases of the same capacitors on different cavities, the impedance profile will be the same.

The next higher frequency impedance feature is the self-resonant frequency of the capacitors. This should be the same for each cavity and is expected as

$$f_{\text{SRF}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{cap}}[\text{nH}]C_{\text{cap}}[\text{nF}]}} = \frac{159 \text{ MHz}}{\sqrt{1 \text{nH} \times 100 \text{nF}}} = 15.9 \text{ MHz} \quad (8.41)$$

When we add the spreading inductance between the

capacitors and the observation point, this self-resonant frequency shifts to slightly lower frequency.

The third higher frequency impedance feature is the parallel resonance of the capacitor's mounting inductance and cavity's capacitance. This is different for the small and large cavity, each expected at

$$f_{\text{caps-cavity-1inch}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{caps}}[\text{nH}]C_{\text{cavity}}[\text{nF}]}} = \frac{159 \text{ MHz}}{\sqrt{\frac{1}{9} \text{ nH} \times 0.1 \text{ nF}}} = 1500 \text{ MHz} \quad (8.42)$$

$$f_{\text{caps-cavity-10 inch}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{caps}}[\text{nH}]C_{\text{cavity}}[\text{nF}]}} = \frac{159 \text{ MHz}}{\sqrt{\frac{1}{9} \text{ nH} \times 10 \text{ nF}}} = 150 \text{ MHz} \quad (8.43)$$

Including the spreading inductance of the cavity shifts these resonant frequencies to lower frequency.

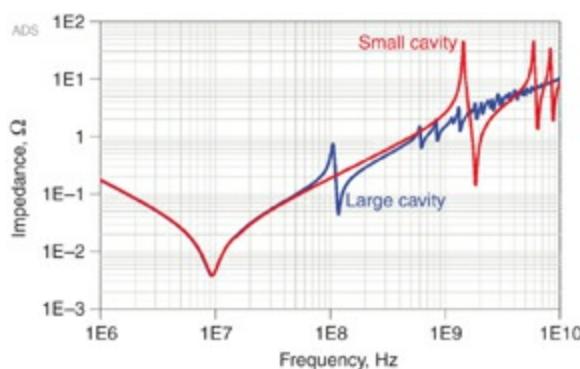
Finally, the first modal resonance frequency expected will be different for the two size cavities. We estimate them as

$$f_{\text{modal-1inch}} = n \times \frac{c}{\sqrt{Dk} \times 2 \times \text{Len}} = 2 \times \frac{11.8 \text{ inches/nsec}}{\sqrt{4.3} \times 2 \times 1 \text{ inch}} = 5.7 \text{ GHz} \quad (8.44)$$

$$f_{\text{modal-10 inch}} = n \times \frac{c}{\sqrt{Dk} \times 2 \times \text{Len}} = 2 \times \frac{11.8 \text{ inches/nsec}}{\sqrt{4.3} \times 2 \times 10 \text{ inch}} = 0.57 \text{ GHz} \quad (8.45)$$

Because the cavity is driven and observed from the center, the first mode excited is with  $n = 2$ .

The impedance profiles of these two size cavities with the same capacitors were calculated with a 3D field solver and are shown in Figure 8.20.



**Figure 8.20** Impedance profiles of the two cavities with nine identical capacitors attached.

The simulated impedance profile shows exactly what is expected. The differences are due to the interactions of the capacitor's spreading inductance and the cavities' capacitance and the on-set of modal resonances. The frequencies at which this happens is very close to the estimates.

The parallel resonances of the capacitors and the cavities are simulated as 105 MHz and 1300 MHz. These are slightly lower than the estimates of 150 MHz and 1500 MHz, due to the estimates' not including the cavity spreading inductance.

The first modal resonances are simulated as 6 GHz and 0.6 GHz, very close to the estimates of 5.7 GHz and 0.57 GHz.

**Tip**

Simple approximations are quite effective at estimating the important features in the impedance profile of PDN components.

We added the S-parameter behavioral models of these two cavities with their components to the circuit composed of the on-die capacitance and the package lead inductance.

The values for this example were

On-die capacitance: 50 nF

Package lead inductance: 250 pH

Cavity thickness: 10 mils

Cavity Dk: 4.3

Cavity size: 1 inch  $\times$  1 inch and 10 inch  $\times$  10 inch

Probed from the center

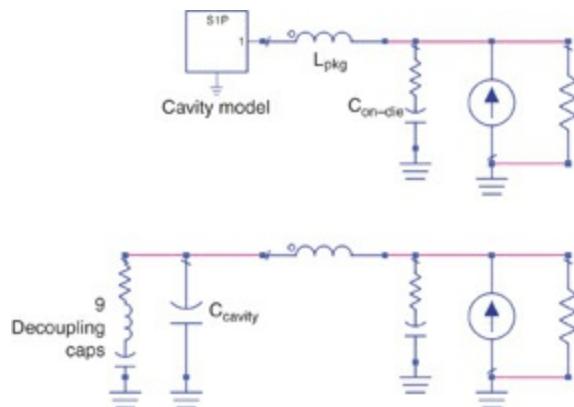
Nine identical decoupling capacitors

Capacitance of each capacitor: 100 nF

Mounting inductance of each capacitor: 1 nH

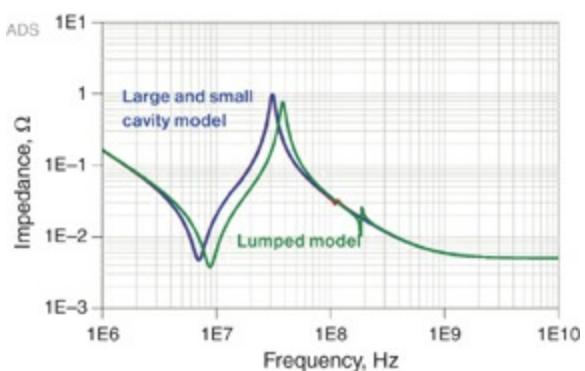
ESR of each capacitor: 25 m $\Omega$

We compared the simulated impedance from the die pads with the behavioral S-parameter models of the cavities with the lumped circuit model of the cavity composed of just a lumped capacitor and the nine decoupling capacitors in parallel. Figure 8.21 shows these two circuits.



**Figure 8.21 Top:** Circuit that simulates the impedance looking into the cavity from the die pads, through the package lead inductance using a behavioral model for the two different size cavities. **Bottom:** The same model of the on-die capacitance and package lead inductance, but using a lumped circuit model for cavity and the nine capacitors in parallel.

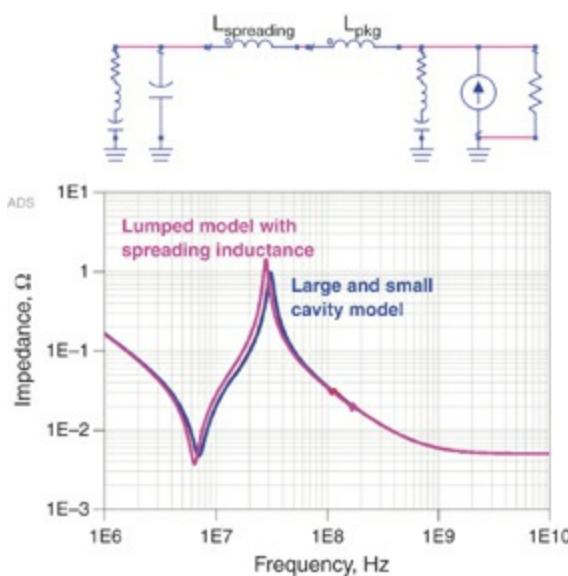
Figure 8.22 shows the impedance profiles calculated from these two models. The impedance profiles of both the 1-inch and 10-inch cavity behavioral models are identical on this scale.



**Figure 8.22** Simulated impedance profiles of the PDN as viewed from the die pads using S-parameter behavioral models for each cavity (two traces on top of each other) and a lumped circuit model of the cavity. Virtually no difference exists when using a 1-inch or 10-inch size cavity in the behavioral model.

The simulated impedance profiles based on the lumped circuit model of the cavity and its components matches the S-parameter behavioral models well. This lumped model does not include any spreading inductance in the cavity between the central observation point, assumed to be the point of attachment of the package, to the array of capacitors.

If we add a spreading inductance from the package to the capacitors, equivalent to 1 square of sheet inductance, to the lumped circuit model, the agreement between the S-parameter models of the cavity and the lumped circuit model of the cavity, as shown in Figure 8.23, is excellent.



**Figure 8.23** When we add a spreading inductance of 1 square to the lumped circuit model, as shown at the top, the agreement between the lumped circuit model and the S-parameter–based behavioral model is excellent for the PDN as seen by the die.

#### Tip

The spreading inductance from the decoupling capacitors to the package is approximately 1 square of sheet inductance, depending on proximity of the capacitors.

This analysis has three important consequences that directly impact design decisions.

First, the most important role of the cavity in influencing the impedance profile of the PDN as seen at the die pads is in providing the low spreading inductance from the package pads to the decoupling capacitors. The capacitance in the cavity is irrelevant. The size of the cavity, outside the location of the decoupling capacitors, is irrelevant for the PDN.

#### Tip

The most important function of the cavity for the PDN is providing low spreading inductance from the decoupling capacitors to the package. This means thinner is better.

This is contrary to what is often reported in the

popular literature: that the cavity provides low impedance (capacitance) to the chip at high frequency. As shown earlier, the low impedance at high frequency is provided by the on-die capacitance. The die pads do not see the cavity capacitance at high frequency. At low frequency, the capacitance of the decoupling capacitors swamps the relatively small capacitance in the cavity.

**Tip**

Contrary to popular accounts in the literature, the cavity capacitance does not provide the low impedance at high frequency. The on-die capacitance does. The cavity contributes spreading inductance but its capacitance is not important.

Second, the high-frequency peak impedances in the cavity from modal resonances or interactions with other components, near and above the Bandini Mountain, in the 100 MHz and above frequency range, are not seen at the die pads. The high impedance of the package leads and low impedance of the on-die capacitance dominates over these resonances.

**Tip**

Impedance peaks seen in the cavity impedance profile above the Bandini frequency are not seen by the pads on the die.

Once again we state that the cavity resonances, which play such an important role when signals' return currents transition through the cavity, contributing to signal integrity problems such as cross talk and possible EMI problems of enhanced radiated emissions, play no role in supplying low impedance power to the core logic rails. After we select the decoupling capacitors for the PDN, we might add additional capacitors to suppress the plane resonances to reduce signal integrity and EMI problems. These are two separate design requirements.

One approach to balancing both design requirements is to select the capacitors for the PDN, then add additional capacitors using as small a body size as practical, so as to enable as low a mounting inductance as possible, and using as large a capacitance in that body size with no cost penalty. This way, parallel resonances from the larger value capacitors are at lower frequency than the typical Bandini Mountain frequencies.

**Tip**

Selecting capacitor values for a low PDN impedance is a different design requirement than selecting capacitors to reduce the cavity impedance. They both require low mounting inductance, but the similarity in requirements ends there.

Finally, because the size of the cavity does not affect the PDN from the die pad's perspective, for PDN performance, it is only important to design the cavity to connect the decoupling capacitors to the package it decouples. This is especially important when many power rails are routed on one layer. The path from the VRM to the group of decoupling capacitors can have high inductance as long as the path from the capacitors to the package pads is designed for as low a spreading inductance as practical.

This principle gives rise to the possible use of *power puddles*, islands of power and ground planes in the vicinity of the package that do not extend much beyond the location of the decoupling capacitors. Even plane segments can be used to allow many voltage rails to share the same layer. This is an optimized design, providing, of course, the power planes are not used as return paths for signals.

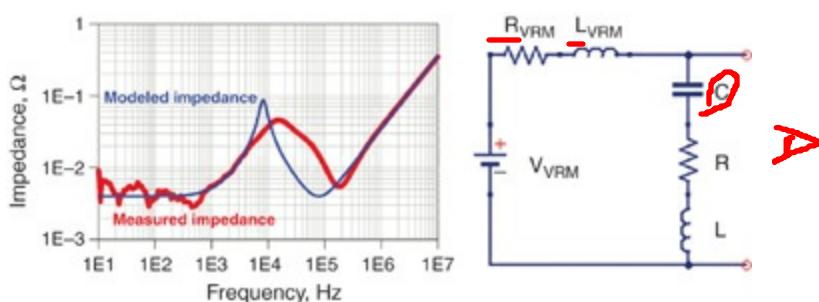
**Tip**

A common design feature is to use *power puddles*, regions of power and ground planes from the decoupling capacitors to the package power and ground pads. The design of the rest of the power and ground distribution is less important.

## 8.10 AT THE LOW FREQUENCY: THE VRM AND ITS BULK CAPACITOR

A voltage regulator module keeps its output voltage constant by using feedback from a sense line, compared to a voltage reference, to control some element that affects its output voltage. This can be a pulse generator that drives a  $dI/dt$  through an inductor to generate the voltage at the output, as in a switching regulator, or a series field effect transistor (FET) gate, which regulates the current flow from a higher voltage reservoir as in a linear regulator. Although using the entire feedback circuitry in the model of the VRM is possible, in many applications, we can approximate the actual behavior of the feedback circuitry in the VRM under typical use conditions with a simple series R and L circuit. In addition to the RL elements are the associated bulk decoupling capacitor and any others that might be placed on the board.

For example, the measured output impedance of a typical DC-to-DC point of a load switching regulator was compared with the simulated impedance of a simple circuit. The circuit model for the simple VRM is a voltage source and series RL elements. In this example, a decoupling capacitor was also included in the measured circuit. Figure 8.24 shows the measured output impedance of this regulator compared with the simulated impedance of the model.



**Figure 8.24** Measured and simulated impedance of a typical VRM.

The series resistance in the VRM simulated model was  $4 \text{ m}\Omega$  and the equivalent inductance was  $500 \text{ nH}$ . The decoupling capacitor had values of  $740 \mu\text{F}$ ,  $4 \text{ m}\Omega$ , and  $5.7 \text{ nH}$ . It is remarkable that to a good approximation, the complicated feedback circuitry still behaves like a simple RL circuit. Although the match is not perfect, it is a good first order estimate. This RL model dramatically simplifies incorporating a VRM into a system simulation to observe how it interacts with the impedance of the cavity.

The value of  $500 \text{ nH}$  is not related to a physical structure that has this large a loop inductance but is a measure of the feedback loop time constant. A faster circuit response would have emulated a lower loop inductance in the impedance profile. Depending on the type of regulator, the equivalent loop inductance could vary from  $1 \text{ nH}$  to  $1,000 \text{ nH}$ . This is an important feature of any VRM.

#### Tip

We can model most VRMs as a simple series RL circuit. The L is based on the feedback circuitry of the VRM and is not related to a physical structure.

L depends on how fast it ramps up current, based on 8.46

One way of estimating the equivalent VRM inductance is from knowledge of the response time. The key question is “How long does it take the VRM inductor to slew the full transient current?” This is a

large signal question that usually involves the VRM going from nearly zero current to nearly maximum current. It is closely related to the step response for the VRM but without drawing current from the bulk capacitor. We then calculate the equivalent VRM inductance from the  $V=L \cdot di/dt$  equation. V is taken as the tolerance for the PDN, probably 5% of Vdd.

For example, for a 1 V PDN with 0.5A transient current and a VRM that ramps up its inductor current in 1  $\mu$ s, an estimate for the inductance is

$$L = \frac{V}{\frac{dI}{dt}} = \frac{5\% \times 1\text{V}}{\frac{0.5\text{A}}{1\mu\text{sec}}} = 100\text{nH} \quad (8.46)$$

Because of the large effective series inductance, the VRM by itself has an impedance that exceeds any reasonable target impedance even at low frequency. This PDN needs bulk decoupling capacitors added to the board to bring the impedance down in the low-frequency regime.

The faster the feedback loop of the VRM, the lower the equivalent inductance and the higher the parallel resonant frequency. Above the parallel resonant frequency of the VRM and cavity capacitance, the impedance of the cavity is completely independent of the VRM.

At frequencies below the series LC resonance of the cavity, the impedance of the cavity is independent of the location where it is measured. Above this frequency, the impedance depends on the spreading inductance to the observation point.

assume Z\_target dominated by L, which is valid statement near VRM's f\_max

faster feedback, i.e. larger  $di/dt \Rightarrow$  smaller L needed, smaller impedance Because L here works constructively L decides the highest resonant freq that VRM can impact

#### Tip

Usually, the effective series inductance of the VRM is much higher than any additional interconnect-related inductance from the VRM to the observation point. The interconnect inductance slightly increases the effective VRM loop inductance.

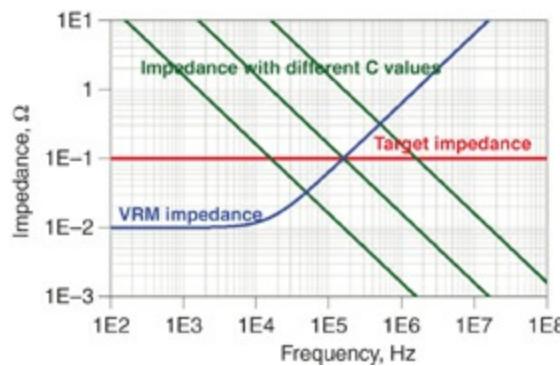
## 8.11 BULK CAPACITORS: HOW MUCH CAPACITANCE IS ENOUGH?

This is probably the most commonly asked question in PDN analysis, though not the most important. We can roughly estimate the minimum amount of capacitance on the board for one rail of the PDN with either a time domain or frequency domain analysis.

In the frequency domain, a primary role of the board capacitance is to provide a low impedance in the frequency range where the voltage regulator module (VRM) cannot. In this frequency band, the total capacitance should be large enough so that its impedance brings the PDN impedance below the target impedance. Because this is usually a large amount of capacitance and plays a dominant role at low frequency, it is often referred to as **bulk capacitance**.

Also the size of the cap are larger

If the bulk capacitance is too small, its impedance is above the target impedance at the frequency where the VRM cannot provide the low impedance. Figure 8.25 illustrates this analysis.



**Figure 8.25** Example of the target and VRM impedances showing the limit to the VRM and the impedances of three different capacitors.

The high-frequency limit to the effectiveness of the VRM, when its output impedance exceeds the target impedance, depends on the target impedance and the nature of the feedback loop inside the VRM. The **highest useful frequency of the VRM** is estimated from the

condition that

$$Z_{\text{VRM}} > Z_{\text{target}} \quad \text{or} \quad 2\pi f_{\text{VRM-max}} L_{\text{VRM}} > Z_{\text{target}} \quad (8.47)$$

impedance curve section  
that dominated by L in  
8.25

and

$$f_{\text{VRM-max}} > \frac{Z_{\text{target}}}{2\pi L_{\text{VRM}}} = 159 \text{ MHz} \frac{Z_{\text{target}} [\Omega]}{L_{\text{VRM}} [\text{nH}]} \quad (8.48)$$

In general, when the target impedance is low the VRM needs to have a faster feedback loop so the equivalent inductance is low.

For example, if the target impedance is  $0.01 \Omega$ , the VRM inductance might be on the order of  $10 \text{ nH}$ . This results in a maximum frequency range for the VRM of about

$$f_{\text{VRM-max}} > 159 \text{ MHz} \frac{Z_{\text{target}} [\Omega]}{L_{\text{VRM}} [\text{nH}]} = 159 \text{ MHz} \frac{0.01 \Omega}{10 \text{ nH}} = 159 \text{ kHz} \quad (8.49)$$

It is usually in the  $10 \text{ kHz}$  to  $1 \text{ MHz}$  range. At this frequency the impedance of the capacitor should be below the target impedance. We derive the minimum bulk capacitance required to bring its impedance below the target impedance at the highest effective frequency of the VRM with

$$Z_{\text{bulk}} < Z_{\text{target}} \quad \text{or} \quad \frac{1}{2\pi f_{\text{VRM-max}} C_{\text{bulk}}} < Z_{\text{target}} \quad (8.50)$$

C\_bulk min ==> Z curve furthest to right

? only valid in region where C dominates Z\_bulk

which results in

$$C_{\text{bulk}} > \frac{1}{2\pi f_{\text{VRM-max}} \times Z_{\text{target}}} = \frac{2\pi L_{\text{VRM}}}{2\pi Z_{\text{target}} \times Z_{\text{target}}} = \frac{L_{\text{VRM}}}{Z_{\text{target}}^2} \quad (8.51)$$

where

$C_{\text{bulk}}$  = the capacitance of the capacitor needed at the lowest frequency

$f_{\text{VRM-max}}$  = the frequency where the VRM impedance exceeds the target impedance

$Z_{\text{target}}$  = the PDN target impedance

$L_{\text{VRM}}$  = the equivalent inductance of the VRM

The condition in equation 8.51 for selecting enough bulk capacitance is really a condition that

$$\boxed{Z_{\text{target}} > Z_0 = \sqrt{\frac{L_{\text{VRM}}}{C_{\text{bulk}}}}} \quad \text{or} \quad \boxed{C_{\text{bulk}} > \frac{L_{\text{VRM}}}{Z_{\text{target}}^2}} \quad (8.52)$$

This condition started out to be, “Select a bulk capacitance large enough so its impedance crosses the target impedance at the same frequency as the VRM’s impedance crosses the target impedance.” Recall that the definition of the characteristic impedance of a parallel LC circuit is the impedance at which the capacitive reactance matches the inductive reactance. These are the same criteria.

The characteristic impedance of the LC circuit is the lowest peak impedance the parallel resonance circuit can achieve in the best condition of critical damping. This is a starting place, minimum capacitance estimate. Larger values of bulk capacitance may be needed to increase the damping and bring the peak impedance to an acceptable level.

For example, if the target impedance is  $10 \text{ m}\Omega$ , we would want the characteristic impedance of the parallel circuit to be less than  $10 \text{ m}\Omega$ . If the VRM inductance is  $20 \text{ nH}$ , the upper frequency limit to the VRM is roughly

$$f_{\text{VRM\_max}} > 159 \text{ MHz} \frac{Z_{\text{target}}}{L_{\text{VRM}}[\text{nH}]} = 159 \text{ MHz} \frac{0.01\Omega}{20 \text{ nH}} = 80 \text{ kHz} \quad (8.53)$$

$Z_{\text{target}}, L_{\text{VRM}}$   
==>  $f_{\text{max}}$   
==>  $C_{\text{bulk}}$

The minimum amount of bulk capacitance needed is roughly

$$C_{\text{bulk}} > \frac{L_{\text{VRM}}}{Z_{\text{target}}^2} = \frac{20 \text{ nH}}{0.01^2} = 200 \mu\text{F} \quad (8.54)$$

We can also estimate the minimum amount of capacitance required from a **time domain analysis**. The bulk capacitor provides the charge storage to supply the current flow to the die during the time before the VRM responds.

As charge flows from the bulk capacitor, the voltage across it drops. We select enough capacitance so that for the time in which the VRM cannot respond, the voltage drop on the bulk capacitor is under the typical 5% tolerance spec. The voltage drop on a capacitor is

$$\text{ripple} \times V_{dd} = \Delta V = \frac{\Delta Q}{C_{bulk}} = \frac{I_{max} \times \Delta t}{C_{bulk}} \quad (8.55)$$

And, from the initial description of the target impedance, the worst-case transient current is roughly

$$I_{max} = \frac{V_{dd} \times \text{ripple}}{Z_{target}} \quad (8.56) \quad \boxed{\text{resulted } I_{max}}$$

This results in an estimate of the minimum bulk capacitance needed of about

$$\text{ripple} \times V_{dd} = \frac{\frac{V_{dd} \times \text{ripple}}{Z_{target}} \times \Delta t}{C_{bulk}} \quad (8.57)$$

or

$$C_{bulk} > \frac{\Delta t}{Z_{target}} \quad (8.58)$$

If we make the connection that the highest frequency where the VRM is not effective at reducing the impedance below the target impedance is related to the time interval by

$$\Delta t = \frac{1}{2\pi f_{VRM-\max}} \quad (8.59)$$

We see that both frequency domain and time domain analyses result in exactly the same initial estimate for the minimum bulk capacitance required:

$$C_{\text{bulk}} > \frac{L_{\text{VRM}}}{Z_{\text{target}}^2} = \frac{20 \text{nH}}{0.01^2} = 200 \mu\text{F} \quad (8.62)$$

These simple estimates suggest that the typical bulk capacitor values required are in the 100–1,000 of  $\mu\text{F}$ . PDNs with very low target impedances and VRMs with a low-frequency feedback loop require larger value capacitors.

larger L ==>  
lower f\_VRM max  
(8.48)

## 8.12 OPTIMIZING THE BULK CAPACITOR AND VRM

The estimates in the previous section are just a starting place for estimating the bulk decoupling capacitance. To get a better estimate, we must consider the impedance profile of the VRM and bulk capacitor. Just as we saw with the on-die capacitance and the package lead inductance, when an inductive element connects to a capacitive element a new behavior emerges: the peak parallel impedance. This is often the biggest problem in the PDN.

A large peak impedance from the parallel resonance of the effective output inductance of the VRM and the bulk capacitor can also mean a potential instability in the VRM. Although we can consider this problem roughly in the frequency domain, we must use time domain simulation for the best accuracy. Switch Mode Power Supplies (SMPS) are inherently non-linear and time varying so they violate two of the most important requirements for frequency domain analysis. The impedance peak for a rising current waveform is very different from a falling current waveform.

**Tip**

This is why, in the absence of your own SPICE simulation including the non-linear model of the VRM, first start with the bulk capacitor recommendations of the VRM supplier, who, presumably, has done a SPICE simulation to evaluate the transient voltage noise and stability.

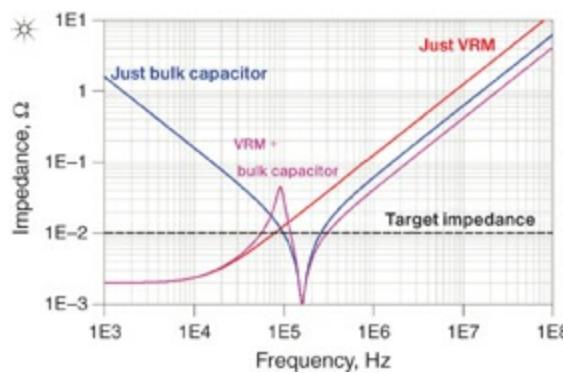
As a starting place, we explore the optimum bulk capacitance based on the impedance profile in the frequency domain. Using a VRM having  $R = 2 \text{ m}\Omega$  and  $L = 20 \text{ nH}$ , with a target impedance of  $10 \text{ m}\Omega$ , we estimate the frequency at which the target impedance is exceeded by the VRM:

$$f_{\text{VRM-max}} > 159 \text{ MHz} \frac{Z_{\text{target}}}{L_{\text{VRM}}[\text{nH}]} = 159 \text{ MHz} \frac{0.01\Omega}{20 \text{ nH}} = 80 \text{ kHz} \quad (8.61)$$

and the bulk capacitance required:

$$C_{\text{bulk}} > \frac{L_{\text{VRM}}}{Z_{\text{target}}^2} = \frac{20 \text{ nH}}{0.01^2} = 200 \mu\text{F} \quad (8.62)$$

When we add this capacitor to the VRM, the impedance profile has a large parallel peak impedance at around 90 kHz, as shown in Figure 8.26.



**Figure 8.26** Impedance profile for the VRM and bulk capacitor in isolation and when combined showing the parallel resonant peak impedance around 90 kHz.

In this example, the peak impedance exceeds the target impedance by a factor of three. Although this might be acceptable for a marginally robust PDN, the

peak might introduce some instability with the VRM, and should be lowered. It is caused by the combination of the inductance of the VRM, the capacitance of the bulk capacitor, and the ESR of the capacitor. The VRM resistance also influences the peak impedance but this is generally very small compared with the ESR of the capacitor.

We estimate the q-factor of the parallel resonant circuit in this example, assuming an MLCC capacitor, as,

$$\text{q-factor} = \frac{1}{\text{ESR}} Z_0 = \frac{1}{\text{ESR}} \sqrt{\frac{L_{\text{VRM}}}{C_{\text{bulk}}}} = \frac{1}{0.002} \sqrt{\frac{20 \text{nH}}{200,000 \text{nF}}} = 5 \quad (8.63)$$

This is a problem with using ceramic MLCC capacitors as bulk decoupling capacitors. For large capacitor values, their ESR is small and result in underdamped parallel resonances.

In the extreme case, when the MLCC capacitance is very high, all the damping is provided by the output resistance of the VRM. In this case, the q-factor decreases as the MLCC capacitance increases. We estimate just how much MLCC capacitance is required so that the q-factor is 1.

The condition for critically damped is a q-factor = 1:

$$1 = \frac{1}{\text{ESR}} \sqrt{\frac{L_{\text{VRM}}}{C_{\text{bulk}}}} \quad \text{or} \quad C_{\text{bulk}} = \frac{L_{\text{VRM}}}{\text{ESR}^2} \quad (8.64)$$

This relationship identifies the amount of bulk capacitance to add to a VRM so that the parallel resonance is critically damped using just the DC output impedance of the VRM as the damping source.

With a  $2 \text{ m}\Omega$  DC output impedance,  $20 \text{ nH}$  effective inductance VRM, the amount of capacitance required to be critically damped by the VRM output resistance is a bulk capacitance of

$$C_{\text{bulk}} - \frac{L_{\text{VRM}}}{ESR^2} = \frac{20 \text{nH}}{0.002^2} = 5,000 \mu\text{F} \quad (8.65)$$

This is an absurdly high amount for a single MLCC capacitor, or even a handful. This is a danger when using large value MLCC capacitors as bulk decoupling capacitors. They will not provide enough ESR damping to critically damp the parallel resonant peak with the VRM. Relying on the very low DC output impedance of the VRM would require more capacitance than MLCC capacitors can provide.

This suggests that generally, using large-value ceramic MLCC capacitors will result in an underdamped peak, which may be significantly above the target impedance.

**Tip**

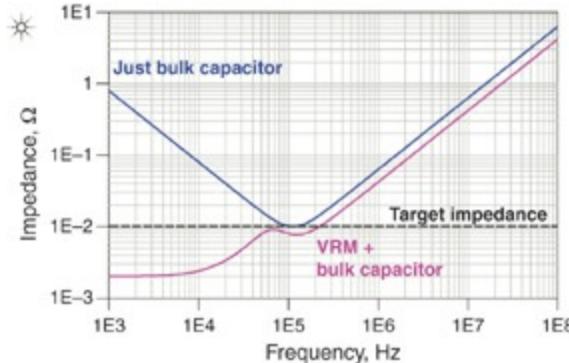
Although providing enough capacitance to meet the first criterion with ceramic capacitors might be possible, there is no guarantee the parallel resonant peak will be below the target impedance.

An alternative solution is to use tantalum or electrolytic capacitors for bulk decoupling, not so much for their higher capacitance, but for their higher ESR. Usually, the ESR of electrolytic capacitors are on the order of  $0.02 \Omega$  to  $0.1 \Omega$ . The number of capacitors should be selected to bring their parallel equivalent resistance below the target impedance.

The ESR of both electrolytic and tantalum capacitors vary depending on the body size and style used. They range from about  $5 \text{ m}\Omega$  to  $1 \Omega$ . Of course, multiple identical capacitors in parallel have an even smaller ESR, reduced by the number of capacitors in parallel. The ESR value should be selected based on a value that reduces the peak impedance below the target impedance. The minimum condition is for a

characteristic impedance at the target impedance and a q-factor of 1, which means a total ESR at the target impedance.

Figure 8.27 shows the impedance profile of the bulk capacitor and in combination with the VRM when we select the ESR to be equal to the target impedance.



**Figure 8.27** Impedance profile when the bulk capacitors' combined ESR equals the target impedance.

Note the peak has been almost eliminated.

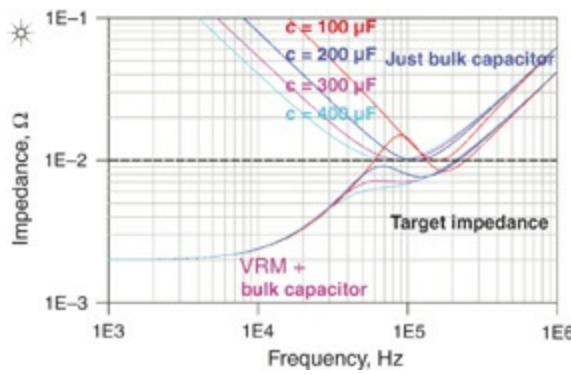
As the capacitance of the bulk capacitors increases, the impedance of the PDN just decreases with the q-factor remaining low. If the ESR is too high, the impedance in the frequency range where the bulk capacitor affects the PDN will be too high.

This suggests a simple algorithm when selecting bulk capacitors:

1. Evaluate the recommendations from the VRM supplier.
2. Identify the approximate output inductance of the VRM.
3. Identify the target impedance.
4. Select enough total capacitance to provide the minimum bulk capacitance based on the estimate in equation 8.51.
5. Select a capacitor type and number of capacitors to give an ESR equal to the target impedance.
6. More capacitance adds some margin, provided the

q-factor is low.

Figure 8.28 illustrates the impedance profiles using bulk capacitors selected by an ESR = target impedance and increasing the total capacitance from 100  $\mu\text{F}$  to 400  $\mu\text{F}$ . A capacitance smaller than the estimated value results in too large of a peak impedance. The q-factor is higher due to the capacitance being too small. When the bulk capacitance is selected based on the target impedance and VRM inductance, the PDN impedance profile is very good. Larger values of capacitance only decrease the impedance and the q-factor, maintaining a stable VRM.



**Figure 8.28** Impedance profiles when the bulk capacitance is changed, but the ESR is selected based on matching the target impedance.

## 8.13 BUILDING THE PDN ECOSYSTEM: THE VRM, BULK CAPACITOR, CAVITY, PACKAGE, AND ON-DIE CAPACITANCE

The interactions of the VRM and bulk capacitors typically happen below 1 MHz. Above this frequency, the impedance of the bulk capacitors and VRM look like an inductor. This inductance value is the parallel combination of the VRM and the bulk capacitor's inductance, on the order of 10 nH depending on the specific details. When the VRM is added to a board with a power and ground cavity connecting it to a package, the package will see the inductance associated with the VRM. It will add to the package lead inductance and

spreading inductance of the cavity. Usually the spreading inductance is insignificant compared to the inductance associated with the VRM and bulk capacitor.

From the chip's perspective, the cavity looks like additional inductance in series with the package lead inductance. The combined inductance of the VRM and bulk capacitors is typically more than an order of magnitude larger than the package lead inductance.

Compared with the shorted package leads alone, the equivalent inductance of the VRM, bulk capacitors, board, and package increases the Bandini Mountain peak impedance and shifts the peak frequency lower. Recall that the Bandini Mountain is formed from the on-die capacitance looking out into the loop inductance attached to the die pads.

**Tip**

The series inductance of the VRM, bulk capacitors cavity spreading inductance, and the package lead inductance significantly increases the peak of the Bandini Mountain compared to a board that looks like a dead short.

To illustrate the important principles of how the Bandini Mountain is affected by the board environment and how we can engineer the MLCC capacitors to reduce the peak impedances, we start with a typical example:

On-die capacitance: 50 nF

On-die capacitance ESR: 5 mΩ

Package lead inductance: 250 pH

As stated previously, we assume that on-die resistance is consistent with the 250 ps time constant and the on-chip resistance is the dominant damping mechanism. The four important figures of merit for this intrinsic Bandini Mountain, if the board were a dead short, are

$$\text{q-factor} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} = \frac{1}{0.25} \sqrt{50 \times 0.25} = 14 \quad (8.68)$$

$$f_{\text{Bandini}} [\text{MHz}] = \frac{159}{\sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]}} = \frac{159}{\sqrt{50 \text{nF} \times 0.25 \text{nH}}} = 45 \text{ MHz} \quad (8.67)$$

$$\text{q-factor} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} = \frac{1}{0.25} \sqrt{50 \times 0.25} = 14 \quad (8.68)$$

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{L_{\text{package}} [\text{nH}]}{0.25} = \frac{0.25}{0.25} = 1 \Omega \quad (8.69)$$

With a characteristic impedance of  $71 \text{ m}\Omega$ , it is not possible to get all the impedance peaks below  $71 \text{ m}\Omega$  in the very best case. On a practical basis, engineering the peak impedance below about 2 times the characteristic impedance, leveraging nearly optimum selection of MLCC component, is difficult. This means achieving a target impedance of at most,  $150 \text{ m}\Omega$ , under the best conditions, may be possible.

In this example, the board components consist of

Cavity thickness: 10 mils

Cavity Dk: 4.3

Cavity size: 5 inch  $\times$  5 inch

Cavity capacitance: 2.4 nF

Probed from the center

VRM inductance: 10 nH

compared with pkge  
inductance 250 pH

VRM resistance: 1 m $\Omega$

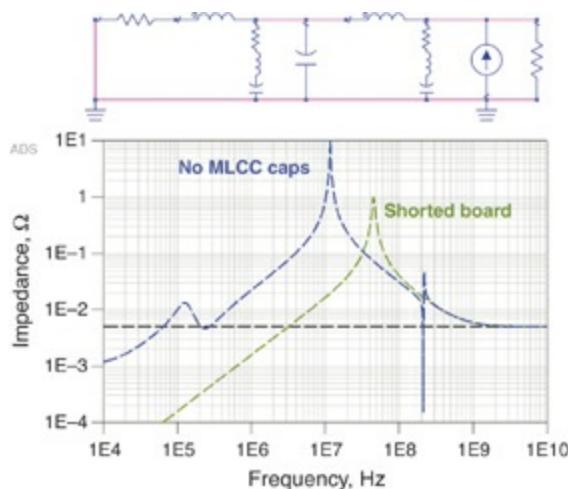
1 bulk decoupling capacitor

Capacitance of bulk capacitor: 100  $\mu$ F

Mounting inductance of each bulk capacitor: 5 nH

ESR of each bulk capacitor: 5  $\text{m}\Omega$

Figure 8.29 shows the Bandini Mountain impedance when the board is shorted, and the resulting impedance profile as seen from the pads of the die with the VRM, bulk capacitor, and cavity.



**Figure 8.29** The board-level circuit model and the resulting impedance profiles as *viewed* from the pads on the die for the case of the package attached to a shorted board and the board with the VRM, bulk caps, and cavity. The model (top) includes the VRM and bulk capacitor, cavity capacitance, package lead inductance, and on-die capacitance.

As expected, the Bandini Mountain peak impedance when the board is shorted is  $1 \Omega$  and occurs at 45 MHz. Adding the board-level elements to the PDN ecology leaves a huge Bandini Mountain at 10 MHz as the dominant feature of the PDN.

The circuit model shows the VRM in parallel with the bulk capacitor. The ODC is in parallel with the series combination of package lead inductance and VRM/bulk capacitor. This highlights how the circuit elements combine to contribute to the peak impedance.

We roughly estimate the peak impedance when the packaged chip is attached to the board ecology from

$$Z_{\text{peak}} = \frac{1}{R_{\text{brd}}} \times (Z_0)^2 = \frac{1}{Z_{\text{target}}} \times (Z_0)^2 \quad (8.72)$$

This is close to the simulated peak impedance of 9.6  $\Omega$ . This is a very high impedance.

### Tip

If the PDN is composed of just the cavity, VRM, and bulk capacitors, with no additional MLCC capacitors, the resulting Bandini Mountain seen by the die could be an absolute disaster for almost any reasonable product.

With no additional decoupling capacitors, the peak height of  $1\Omega$ – $10\ \Omega$  might be sufficiently low to allow the system to “work” under some test conditions. If the transient current frequency components generated by the test code are well away from the Bandini Mountain or if the microcode generates very small current amplitudes, the voltage noise created by the transient current passing through this PDN impedance might not cause any observable failures. For test purposes, the product might “work.”

This is why a product might still “work” even after removing all the MLCC decoupling capacitors from a board. “Working” under a specific test condition is not necessarily a measure of a product’s robustness under all in-use conditions.

Given this packaged die, the only way of reducing the peak impedance by board-level adjustments is to decrease the bulk capacitor’s mounting inductance or increase its ESR. Higher bulk capacitance has no impact on this Bandini peak because it is not about its capacitance. It’s about the inductance of the bulk capacitor.

pkge die, means  
ODC and pkge inductance are fixed

We generally accomplish these two design goals, reducing the inductance shorting across the bulk capacitor or increasing the series resistance at the board level, by adding MLCC capacitors to the board. This is their primary purpose.

**Tip**

In this example, without additional MLCC capacitors, the peak impedance of the PDN is  $10 \Omega$ . Engineering the peak below  $0.15 \Omega$  should be possible. This would result in a much more robust PDN. The challenge is how to do this.

When the intrinsic q-factor of the Bandini Mountain is low, there is already considerable damping at the die level and adding damping resistance from the board-level capacitors generally is not effective.

When the q-factor of the Bandini Mountain is high, and there is little damping from the on-die interconnects, damping from the board can be very effective. These represent the two strategies when selecting the number and values of capacitor to engineer a lower Bandini Mountain.

**Tip**

This is why we look toward adding MLCC capacitors to further reduce the PDN impedance. The chief role of the added MLCC decoupling capacitors is to reduce the peak of the large Bandini Mountain by adding a low inductance that shorts the VRM and bulk capacitor's inductance. In some cases, the MLCC capacitors provide additional series damping resistance. Capacitor values must also be selected to keep other parallel resonant peaks acceptably low.

The PDN ecology to which we add the MLCC capacitors include the VRM, bulk capacitors, cavity, package, and on-die capacitance. This is the starting ecology onto which we place the MLCC decoupling capacitors. The question is, “What strategy should we use to select the MLCC capacitor values and numbers to bring this total impedance profile below the target impedance?”

## **8.14 THE FUNDAMENTAL LIMITS TO THE PEAK IMPEDANCE**

The goal in selecting additional MLCC capacitors for the

board is to reduce the impedance peaks to an acceptable level, as seen by the pads on the die. The acceptable height of the peaks depends upon the acceptable risk. The most robust system has all peaks below the target impedance, but this comes at a higher cost. A reasonable balance between robust design and low cost is to keep the Bandini Mountain peak below about three times the target impedance and all other peaks below the target impedance.

One important engineering question in PDN design is what to do at the board level to reduce the peak heights. There is always the on-die decoupling capacitance and the package lead inductance but these are often outside the control of the board designer. The packaged die sets the ultimate limit for how low the Bandini Mountain peak impedance can be.

In the seemingly “best case” with the board covered on every square inch with “perfect” very low inductance decoupling capacitors, the impedance of the cavity is nearly  $0 \Omega$ . Is this really the best solution for the PDN?

Surprisingly, the answer is no. If the board is a dead short, the equivalent inductance of the cavity is  $0 \text{ nH}$ , but this is in series with the package lead inductance. The pads on the die still see a Bandini Mountain.

In this specific example, the q-factor of 14 is rather high. We can reduce peak impedance with damping provided by the board-level components.

**Tip**

Engineering the board to have the lowest possible impedance is not the best goal to reduce all peaks in the PDN impedance profile.

If even the “ideal case” of a dead short on the board does not reduce the Bandini Mountain, how can the

impedance profile at the board level possibly be improved over a dead short?

The answer lies in the principles of engineering lower peaks in any high q-factor parallel resonant circuit. If the q-factor is large, greater than about 3, if we cannot reduce the package lead inductance, the most effective way of reducing the peak height is adding more damping with a series resistive element at the board level.

The **optimum impedance profile of the board** should not be a dead short, but should look electrically like a **resistor**. This means the cavity, as seen by the package pads, should have an impedance profile that is flat, in the frequency range of the Bandini Mountain, roughly in the 1 MHz to 200 MHz frequency range. This is practical for PDNs with a target impedance in the 100 mΩ range but might not be practical for target impedances below 10 mΩ. For PDNs in the 10 mΩ and lower range, capacitors are needed on package to extend the flat impedance to higher frequency and manage the damping of the Bandini Mountain.

**Tip**

One effective way of reducing the Bandini Mountain peak impedance, especially in a high q-factor system, is by making the board look like a resistor in the 1 MHz to 200 MHz range of the Bandini Mountain peak impedance.

We approximate the peak impedance of the Bandini Mountain when the packaged chip is attached to the board with

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{1}{R_{\text{brd}} + \text{ESR}} \times (Z_0)^2 = \frac{1}{R_{\text{brd}} + \text{ESR}} \times \frac{L_{\text{pkg}}}{C_{\text{ODC}}} \quad (8.71)$$

This suggests, counterintuitively, that the higher the series resistance, the lower the peak impedance. This is because the series resistance is a damping resistance

and the higher the resistance, the higher the damping. This relationship holds up as long as the q-factor is > ~2. When the q-factor is 1, the error is about 40%.

When the series resistance is above the target impedance, the PDN impedance is higher than the target impedance at frequencies below the peak impedance frequency. Having a higher series resistance than the target impedance is counterproductive.

The optimum resistance to select for the board is equivalent to the target impedance. A lower value means not as much damping, resulting in a higher peak impedance. A higher value than the target impedance means a PDN impedance above the target impedance.

**Tip**

The optimum board-level resistance to damp out the Bandini Mountain is equal to the target impedance.

When the board-level resistance is equivalent to the target impedance, the peak impedance is roughly

$$Z_{\text{peak}} = \frac{1}{R_{\text{brd}}} \times (Z_0)^2 = \frac{1}{Z_{\text{target}}} \times (Z_0)^2 \quad (8.72)$$

When the board-level impedance equals the target impedance, the condition for the peak impedance to be below the target impedance is

$$Z_{\text{target}} > Z_{\text{peak}} = \frac{1}{Z_{\text{target}}} \times (Z_0)^2 \quad (8.73)$$

or

$$Z_{\text{target}} > Z_0 \quad (8.74)$$

This is an important observation. If the characteristic impedance of the Bandini Mountain is above the target impedance, reducing the peak impedance below the

target impedance is impossible. The only way to achieve a lower peak impedance is by decreasing the package lead inductance or increasing the on-die capacitance. This is why **lower package lead inductance and larger on-die decoupling capacitance** are such important design goals.

**Tip**

The peak impedance at the Bandini Mountain frequency, in the absolute best case, can never be lower than the characteristic impedance of the package lead inductance and on-die decoupling capacitance. Engineering it below about two times the characteristic impedance is difficult.

For example, in the case of equation 8.71 with a 0.25 nH package lead inductance and 50 nF on-die decoupling capacitance, the characteristic impedance of the Bandini Mountain is

$$Z_0 = \sqrt{\frac{L_{\text{pkg}}}{C_{\text{die}}}} = \sqrt{\frac{0.25 \text{ nH}}{50 \text{ nF}}} = 71 \text{ m}\Omega \quad (8.75)$$

In principle, no value of board-level resistance reduces the PDN impedance below 71 mΩ across a wide bandwidth. To achieve a target impedance even close to 71 mΩ requires a board-level resistance on the order of 71 mΩ:

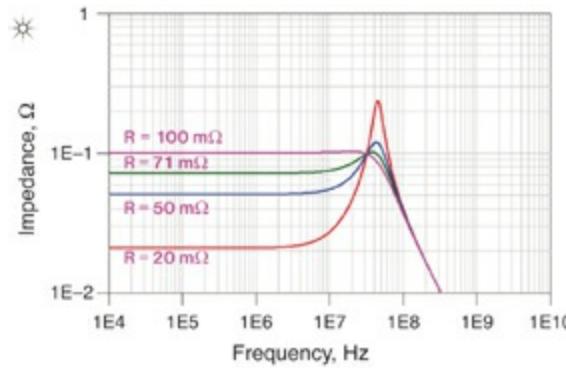
$$\begin{aligned} R_{\text{brd}} &= \frac{1}{Z_{\text{peak}}} \times (Z_0)^2 - \text{ESR}_{\text{on-die}} = \frac{1}{Z_{\text{target}}} \times (Z_0)^2 - \text{ESR}_{\text{on-die}} \\ &= \frac{1}{71 \text{ m}\Omega} \times (71 \text{ m}\Omega)^2 - 0.005 \Omega = 66 \text{ m}\Omega \end{aligned} \quad (8.76)$$

A lower board-level resistance results in less damping and a higher peak impedance. A higher board-level resistance results in a higher impedance at lower frequencies.

Note that within this context, the target impedance is far above the skin effect resistance. When target

impedances are close to  $1 \text{ m}\Omega$ , frequency-dependent board loss becomes important for both damping purposes and conduction purposes.

Figure 8.30 shows an example of the PDN impedance simulated from the die pads of this on-die capacitance and package lead inductance for the case of four different board-level resistances:  $20 \text{ m}\Omega$ ,  $50 \text{ m}\Omega$ ,  $71 \text{ m}\Omega$ , and  $100 \text{ m}\Omega$ .



**Figure 8.30** Impedance profiles from the die pads for different board-level resistances. Note the peak impedance using  $71 \text{ m}\Omega$ , equivalent to the characteristic impedance of the Bandini Mountain, is about  $100 \text{ m}\Omega$ .

This simulation shows a simulated peak of  $100 \text{ m}\Omega$  when the board-level impedance equals the characteristic impedance of the Bandini Mountain. This is an indication of the approximate nature of the relationships described in equation 8.71.

This analysis points out three important observations:

1. The characteristic impedance of the on-die capacitance and package lead inductance sets the fundamental limit to how low of a peak impedance can be achieved. This is an important number to know. If this characteristic impedance is higher than half the target impedance, meeting the target impedance at the parallel resonant frequency of the Bandini Mountain is nearly impossible.
2. The optimum board-level resistance is equivalent to the target impedance. A lower value will not

contribute enough damping whereas a higher value has too large an impedance at lower frequencies.

3. A higher board-level resistance generally requires fewer components than a lower board-level resistance and can be achieved at lower cost. This makes achieving a board-level resistance equal to the target impedance the most robust and cost-effective design guideline.

As a starting place to analyze the MLCC capacitors to add to the board to manage the peak impedance, we consider two ways of estimating the number of capacitors we might need:

1. At the higher frequency, enough capacitors are needed so their inductive impedance is below the target impedance.
2. The inductance of the parallel combination of mounted board capacitors should be less than the package lead inductance. However, we reach a point of diminishing returns when the board inductance is much less than the package lead inductance.

These conditions are

$$n_1 > 2\pi f_{\max\_lim} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} \quad (8.77)$$

$$n_2 > \frac{\text{ESL}_{\text{cap}}}{L_{\text{package}}} \quad (8.78)$$

Note that the analysis here is approximate. Although it offers important design guidelines, we should obtain the final, optimized value of board-level resistance through circuit simulation.

With this perspective, that the absolute best case for a robust and cost-effective PDN is achieved with a board-

level impedance looking like a resistance equivalent to the target impedance, we analyze some of the popular approaches to optimize the board-level PDN to explore their impact.

## 8.15 USING ONE VALUE MLCC CAPACITOR ON THE BOARD-GENERAL FEATURES

board level decap

The starting place is the impedance profile, as seen at the die pads, looking through the package to the board, with the board containing the cavity, the VRM, and the bulk capacitors. To illustrate the design principles, we choose the same representative system as earlier. In [Chapter 10](#), we explore the impact of a broader set of case studies. In this initial system, we use the following starting place:

Target Impedance = 100 mΩ

Max freq = 0.2 GHz

On-die capacitance: 50 nF

On-die capacitance ESR: 5 mΩ

Package lead inductance: 250 pH

Cavity thickness: 10 mils

Cavity Dk: 4.3

Cavity size: 5 inch × 5 inch

Cavity capacitance: 2.4 nF

Probed from the center

VRM inductance: 10 nH

VRM resistance: 1 mΩ

1 bulk decoupling capacitor

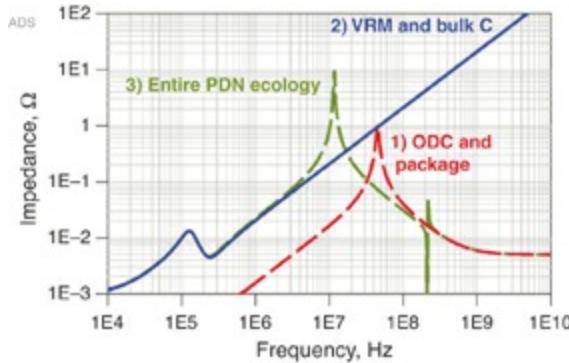
Bulk decoupling capacitance per capacitor: 100 μF

Bulk decoupling capacitor ESR: 5 mΩ

Bulk decoupling capacitor mounting inductance: 5 nH

Three impedance profiles graphically illustrate this condition: 1) the die-level impedance with the board

being a dead short, 2) the impedance of the cavity with just the VRM and bulk capacitor attached, and 3) the die-level impedance when the packaged chip is connected to the cavity with the VRM and bulk capacitor. Figure 8.31 shows these three perspectives.



**Figure 8.31** Three important impedance profiles for the starting place of this case study: 1) ODC and package inductance with a shorted board, 2) VRM, cavity, and bulk capacitor, and 3) the combination of the entire PDN ecosystem.

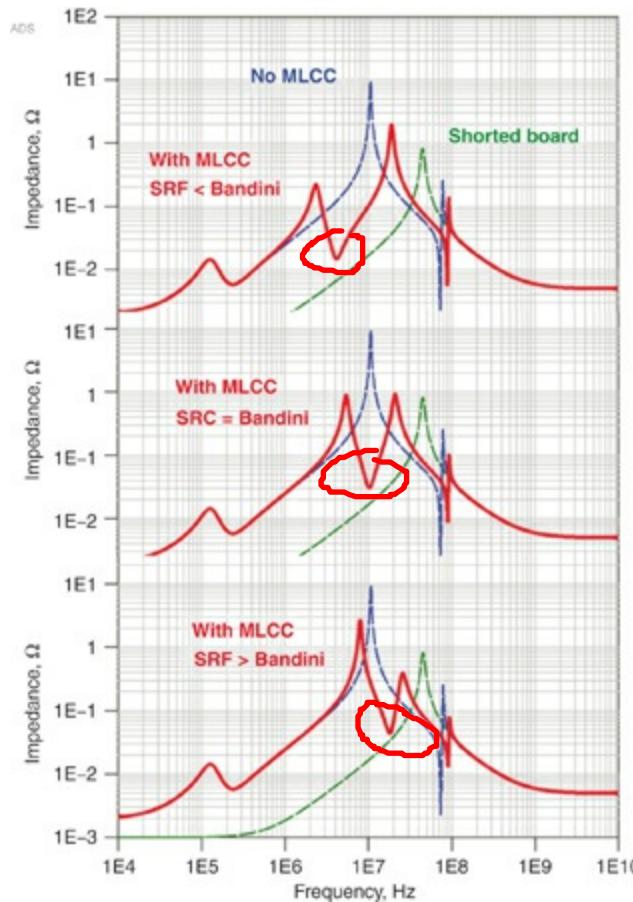
Two extreme cases for the impedance profiles as seen by the die pads are when the package power balls are shorted to the ground balls and when the power balls are connected to the VRM and bulk capacitor. When the shorted package is replaced with the VRM and bulk capacitor, we see the Bandini Mountain has shifted to lower frequency and the peak impedance has increased. Additional MLCC capacitors are added to the VRM and bulk cap to mitigate this peak.

We can estimate how many capacitors we might need to bring this impedance profile below the target impedance using the two conditions described by equations 8.77 and 8.78:

$$n_1 > 2\pi f_{\max\_lim} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} = 2\pi \times 0.2 \text{GHz} \times \frac{1}{0.1} l = 13 \quad (8.79)$$

$$n_2 > \frac{\text{ESL}_{\text{cap}}}{L_{\text{package}}} = \frac{1}{0.25} = 4 \quad (8.80)$$

Initially, we'll analyze the impact from the addition of one MLCC capacitor on the impedance profile, as seen by the die pads. The impact on the board-level impedance profile depends on the self-resonant frequency (SRF) of the capacitor. The SRF can be higher, lower, or equal to the Bandini Mountain peak frequency. [Figure 8.32](#) shows these three cases compared with the two extreme cases with no MLCC capacitors. We assume the mounting inductance of the MLCC is 1 nH regardless of its value. Its ESR is calculated dynamically, based on the value of its capacitance and the model introduced in [Chapter 5](#).



**Figure 8.32** Impedance profile, as viewed from the die pads, with the package attached to the board for three different values of MLCC capacitance, compared with the two limiting cases of a shorted board and no MLCC capacitor.

Without an MLCC capacitor, the Bandini Mountain is created by the parallel resonance of the on-die

capacitance and the bulk capacitor's inductance in series with the package lead inductance. With a shorted board, the Bandini Mountain is created by the parallel resonance of the on-die capacitance and the package lead inductance alone.

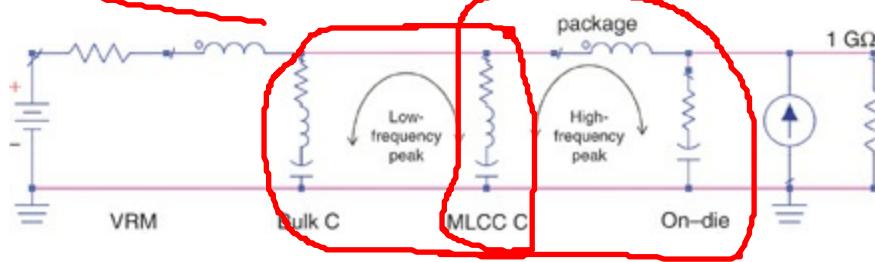
With the addition of a single value MLCC to the board, two parallel resonance peaks are created by different combinations of inductances and capacitances. The circuit model in [Figure 8.33](#) illustrates the parallel circuit combinations that result in the two peaks.

The low-frequency peak is created by the parallel resonance between the bulk capacitor's inductance and MLCC inductance and the series combination of the bulk capacitance and MLCC capacitance.

Parallel LC mainly responsible

The high-frequency peak is created by the parallel resonance of the MLCC inductance and package inductance in parallel with the on-die capacitance.

Note: board inductance/capacitance quite weak when compared



**Figure 8.33** Equivalent circuit model of a single MLCC on a board with the on-die capacitance, package lead inductance, bulk capacitor, and VRM.

Adding an MLCC capacitor always reduces the Bandini Mountain peak impedance over not adding any MLCC capacitors. Any value of capacitance lowers the peak impedance value. However, some values and numbers enable a lower peak than others. This is because the ESL of the MLCC capacitor adds in parallel to the board with the VRM inductance and lowers the equivalent inductance as seen by the on-die pads. This reduces the characteristic impedance of the Bandini Mountain.

**Tip**

Adding *any* value capacitor to a board with just a VRM and bulk capacitor *always* reduces the peak impedance but some values of capacitance reduce the peak impedance more than others.

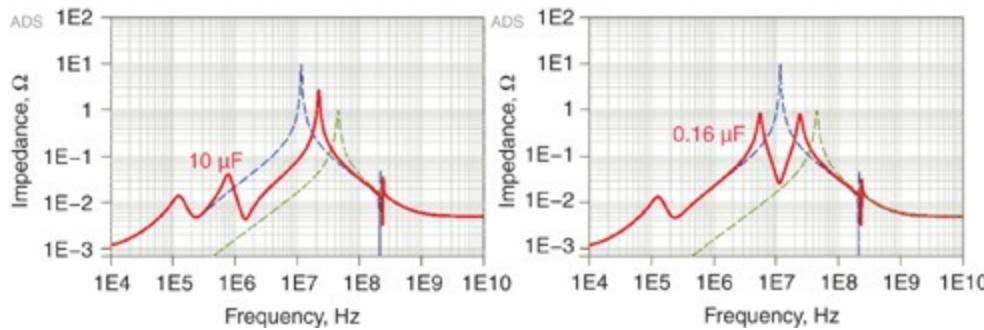
## 8.16 OPTIMIZING THE SINGLE MLCC CAPACITANCE VALUE

In the absence of knowing the values of the on-die capacitance, the package lead inductance, and the properties of the bulk capacitor, there is no way of estimating what single value of MLCC capacitor we should add to the board to give the best performance. This is why an application note that recommends adding 10  $\mu\text{F}$  MLCC capacitors is an arbitrary recommendation and has no basis in reality.

**Tip**

An application note that says to add 10  $\mu\text{F}$  capacitors as decoupling capacitors is usually completely arbitrary.

Larger is not always better. For example, [Figure 8.34](#) shows the impedance profile of a single 10  $\mu\text{F}$  capacitor and a single 0.16  $\mu\text{F}$  capacitor added to the board.

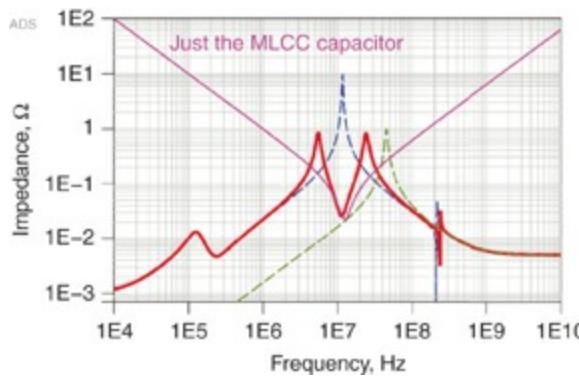


**Figure 8.34** The impedance profile viewed from the die pads mounted to a board with a VRM, bulk capacitor, and a single MLCC capacitor. **Left:** A single 10  $\mu\text{F}$  MLCC capacitor added to the board. **Right:** A single 0.16  $\mu\text{F}$  capacitor added to the board. Larger is not always better.

When a single capacitor is used, the optimum value,

which results in the lowest peak impedance, is when the SRF of the MLCC capacitor is close to the existing Bandini Mountain peak frequency. The dip in the impedance profile with the MLCC added is not exactly at the intrinsic SRF of the MLCC. The dip frequency corresponds to the series resonance of the MLCC capacitance and the series combination of the MLCC inductance, mounting inductance, any spreading inductance, and the package lead inductance. Generally, this is a slightly lower frequency than just the SRF of the MLCC alone.

The smaller the package lead inductance compared to the MLCC inductance, the closer the dip frequency is to the SRF of the MLCC. [Figure 8.35](#) shows the impedance profile of the board with a single 0.16  $\mu\text{F}$  MLCC capacitor and the intrinsic impedance of just the MLCC capacitor and its mounting inductance and ESR. The dips are close but not exactly the same.



**Figure 8.35** Impedance profile of the 160 nF MLCC by itself and when mounted to the board. Note the low impedance dip frequencies are not exactly the same.

If the details of the Bandini Mountain are known, optimizing the single MLCC capacitor value to minimize the peak impedances is possible. A starting place goal is to adjust the SRF of the MLCC to match the Bandini Mountain frequency. This condition is

$$f_{\text{SRF}} = f_{\text{bandini}} \quad (8.81)$$

These terms are

$$f_{SRF} = \frac{159 \text{ MHz}}{\sqrt{ESL_{MLCC} \times C_{MLCC}}} \quad \text{and} \quad f_{Bandini} = \frac{159 \text{ MHz}}{\sqrt{ESL_{bulkC} \times C_{on-die}}} \quad (8.82)$$

This results in

$$\frac{159 \text{ MHz}}{\sqrt{ESL_{MLCC} \times C_{MLCC}}} = \frac{159 \text{ MHz}}{\sqrt{ESL_{bulkC} \times C_{on-die}}} \quad (8.83)$$

Solving for  $C_{MLCC}$ ,

$$C_{MLCC} = C_{on-die} \frac{ESL_{bulkC}}{ESL_{MLCC}} \quad (8.84)$$

In the example of the board described in [section 8.15](#), the mounting inductance of the bulk capacitor was 5 nH whereas the mounting inductance of the MLCC capacitor was 1 nH and the on-die capacitance was 50 nF. This results in an estimate for the optimum MLCC capacitance of

$$C_{MLCC} = C_{on-die} \frac{ESL_{bulkC}}{ESL_{MLCC}} = 50 \text{ nF} \frac{5 \text{ nH}}{1 \text{ nH}} = 250 \text{ nF} \quad (8.85)$$

The actual optimized MLCC capacitance of the last simulation shown in [Figure 8.35](#) was 160 nF, close to this estimate.

In principle, matching the SRF of the MLCC to the Bandini Mountain should be possible using other combinations of capacitance and mounting inductance. The product determines the SRF. However, a word of caution is necessary. Manufacturing tolerances for MLCC capacitors and mounting geometries make sitting exactly on top of the Bandini Mountain difficult. The frequency of the Bandini Mountain is often a moving target because of power gating on-die during different use conditions.

**Tip**

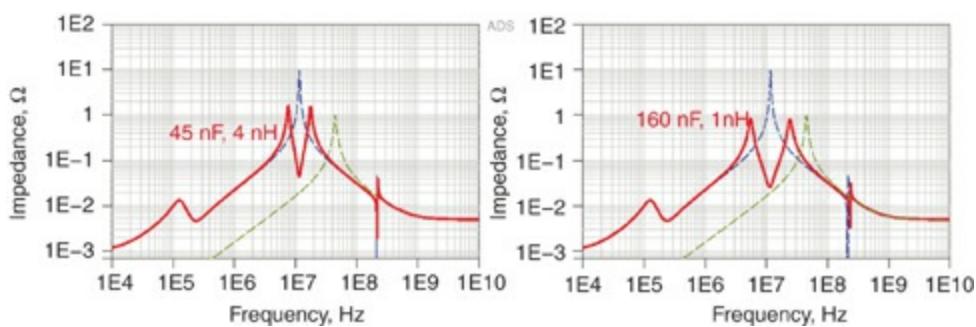
Make any attempt to sit on top of a Bandini Mountain with several capacitor values and low q series resonances to give a broad impedance remedy. Attempts to sit on high q resonant peaks with high q SRF capacitors are usually not successful.

Another contributor to the reduced peak height with the addition of an MLCC capacitor comes from the higher ESR of the MLCC capacitor that damps some of the parallel resonance. The q-factor for this specific Bandini Mountain is 14, high enough that board-level damping will help reduce the peak height.

This would suggest using a smaller value capacitor with its larger ESR might be better. To match the SRF to the Bandini peak with a smaller capacitor the mounting inductance would have to be increased.

But, the reduction in peak height is roughly first order with mounting inductance and the reduction in peak height from ESR is at best second order in capacitor value. The tradeoff usually favors a bigger impact from lower inductance over smaller capacitance with its higher ESR. Reduction of capacitor mounting inductance is the most important thing that we can do to improve decoupling capacitor effectiveness [8].

For example, two values of ESL were simulated, 1 nH and 4 nH, with optimized capacitance values of 160 nF and 45 nF. They each have the same self-resonant frequency, yet the lower MLCC inductance value results in a lower peak impedance, as shown in Figure 8.36.



**Figure 8.36** Impedance profiles of two different MLCC

configurations, with the same SRF. The lower inductance MLCC results in lower peak impedance.

Once again, we see lower inductance is better. It always results in lower parallel resonant peak impedances, though not always a linear dependence. In this example, the peak impedances were  $0.84 \Omega$  with  $1 \text{ nH}$  and  $1.65 \Omega$  with  $4 \text{ nH}$ .

**Tip**

This analysis reinforces the [golden rule in optimizing the PDN](#). [Lower mounting inductance is always better](#). As a good habit, if it is free, you should do everything to reduce capacitor mounting inductance. When it is not free, you should perform analysis to evaluate the cost-performance tradeoffs.

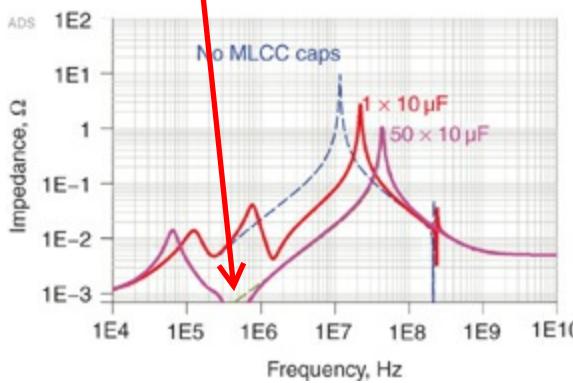
Just as larger capacitance is not always better, more identical capacitors are not always better. Arbitrarily increasing the number of capacitors with identical values affects the two parallel resonant peaks differently.

More MLCC capacitors increase the total MLCC capacitance and reduce the low-frequency parallel resonance peak height. This is a good thing.

More MLCC capacitors also reduce the equivalent parallel combination of all the mounting inductances. This should reduce the higher frequency parallel resonant peak height. When this total equivalent inductance is of the order of the package lead inductance, further increases in the number of MLCC

capacitors has little impact on the total series inductance. The further downside of more MLCC capacitors is that the parallel combination of the ESRs reduces the damping resistance and might actually increase the higher frequency peak impedance.

Figure 8.37 shows an example of the impedance profile from the die pads with a single  $10 \mu\text{F}$  capacitor and 50 identical  $10 \mu\text{F}$  MLCC capacitors. The low-frequency peak near 700 kHz is dramatically reduced with more capacitors, because the total capacitance has increased.

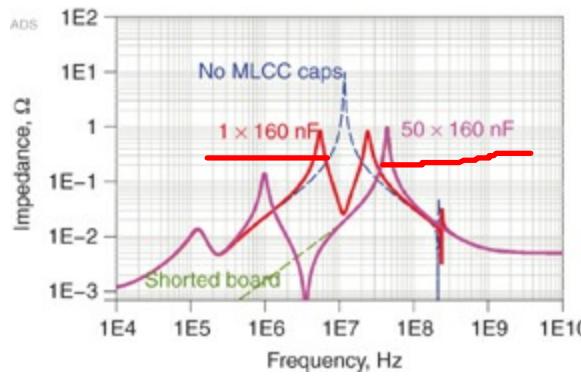


**Figure 8.37** Comparing the impedance profile from the die pads of a single  $10 \mu\text{F}$  capacitor and 50 identical  $10 \mu\text{F}$  capacitors. The impedance profile with 50 MLCC capacitors is identical to the intrinsic Bandini Mountain with a shorted board.

With 50 MLCC capacitors, each with 1 nH of mounting inductance, their parallel equivalent inductance is 20 pH, much lower than the 250 pH of package lead inductance. These capacitors act as a short across the bulk capacitor and the impedance profile from the die pads is identical to the intrinsic Bandini Mountain. The impedance profiles are on top of each other. Adding more capacitors would have no impact on the Bandini Mountain because it is limited by the on-die capacitance and package lead inductance.

If the capacitance value of one capacitor is optimized, adding more identical capacitors will generally result in

a higher peak impedance. In this high q-factor example, because some of the reduction in peak height is due to damping from the ESR of the capacitor, more capacitors in parallel means lower ESR and less damping, which can result in a higher peak impedance. This means a single, optimized capacitor can have lower peak heights than even 50 identical, optimized capacitors, as shown in Figure 8.38.



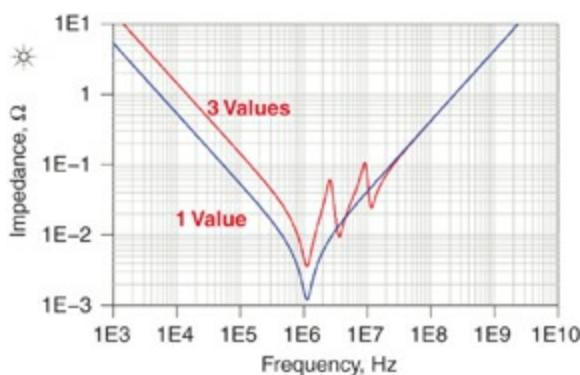
**Figure 8.38** Impact of one optimized MLCC capacitor and 50 identical capacitors. More is not better.

**Tip**

When you're selecting only one value of MLCC capacitor, more capacitors are not better. Compared to selecting a single, optimized capacitor, more capacitors and more capacitance often result in higher peak impedances, a worse choice, or at best, more expensive.

## 8.17 USING THREE DIFFERENT VALUES OF MLCC CAPACITORS ON THE BOARD

We often see a recommendation in application notes that adding three different value capacitors per power pin, a  $10\ \mu\text{F}$ ,  $1\ \mu\text{F}$ , and  $0.1\ \mu\text{F}$  capacitor, is better than three capacitors of all the same value. When this recommendation is offered, it is sometimes justified based on the impedance profile comparison of three capacitors, all  $10\ \mu\text{F}$  compared with the three different values, as shown in Figure 8.39.



**Figure 8.39** Impedance profile of two sets of three capacitors, each with the same ESL of 2 nH. One set has all three capacitors with the same 10  $\mu\text{F}$  capacitance. The other set has three different values of 10  $\mu\text{F}$ , 1  $\mu\text{F}$ , and 0.1  $\mu\text{F}$ . The ESR is adjusted for each capacitor based on its capacitance. Which is better?

At low frequency, the three 10  $\mu\text{F}$  capacitors have lower impedance. At high frequency, all three capacitors have the same ESL and they have the same impedance. The impedance profiles are slightly different in the mid-frequency range. Which is better for the PDN?

The argument in favor of three different values goes something like this: The three different values offer lower impedance at the higher frequencies, at their self-resonant frequencies. The small value capacitor provides a low impedance at the highest frequency. However, when we use realistic ESR values, we find the minimum impedance values are not so low compared with the impedance of the three identical capacitors.

The argument for similar value capacitors goes like this: The impedance at the SRF is lowest with a single capacitor value and because it's all about inductance, three capacitors are really three inductors at high frequency so it doesn't matter what their capacitance is. Lower impedance is always better so the single value capacitor, which has lower impedance, is better.

Which collection of capacitor values is really better for the PDN?

As we have seen throughout this book so far, low

impedances in certain frequency bands are not important. Low PDN impedances can actually be detrimental if they cause other parallel impedance peaks to pop up somewhere else for lack of damping. The real performance figure of merit is the peak impedances, with the Bandini Mountain peak usually the largest. Which combination of capacitors provides the lowest Bandini Mountain peak impedance? To answer that we need to include the on-die capacitance and package inductance in the circuit simulation.

**Tip**

How low the impedance goes is not important to PDN design. It's all about how high the impedance peaks are. The answer to the question, "Which distribution is better?" can only be answered if we know which combination offers lower peak impedances with the entire PDN ecology included.

The analysis of multiple capacitors in parallel with the package lead inductance and on-die decoupling capacitance, VRM, and bulk capacitance, is complicated. Interactions occur between the capacitors and between all capacitors and the package lead inductance.

**Tip**

The peak impedance from the VRM, bulk capacitor, and on-die capacitance usually reduces when we add more MLCC capacitors to the board compared to no MLCC capacitors. This is mostly due to the MLCC capacitors' mounting inductance in parallel with the bulk capacitors' mounting inductance, reducing the impedance peak. To first order, the values of the capacitors are irrelevant.

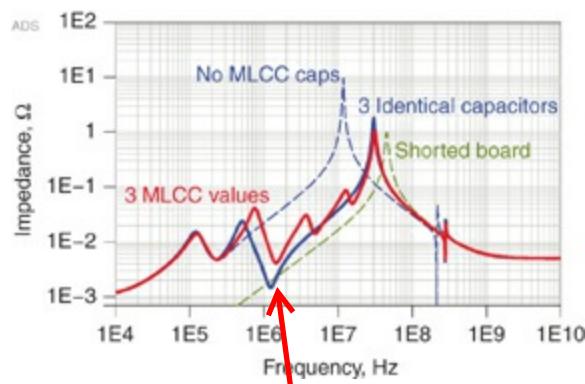
Without knowing the details of the rest of the ecology, predicting which combination is better is impossible. Unless the capacitor values are picked carefully, chances are they will not be optimized.

Additional capacitors on the board always reduce the loop inductance as seen by the die because of inductors

in parallel. This usually reduces the peak impedance, but some capacitor combinations are better than others because of the damping they provide and the interactions with the peaks.

Figure 8.40 shows an example of the simulated impedance profile of the three capacitor combinations compared to the bulk capacitor alone and the shorted package. The peak impedance of the three different values is slightly lower than the case of three identical capacitors because the small value capacitors have higher ESR and they contribute board-level damping to the high q-factor Bandini Mountain.

The impedance profiles approach the case of the shorted Bandini Mountain because three capacitors in parallel have an ESL of 300 pH, comparable to the 250 pH of the package lead inductance. More capacitors in parallel would approach a board-level short. Each combination of capacitor values is equally risky.



**Figure 8.40** Impedance profile of the same PDN ecology with two combinations of three MLCC capacitors, all 10  $\mu\text{F}$  and a set with values of 10  $\mu\text{F}$ , 1  $\mu\text{F}$ , and 0.1  $\mu\text{F}$ . Note a slightly lower peak from three different values due to the higher ESR of the small capacitors.

Which impedance profile is better? If the transient PDN currents are small, or if the large currents have frequency components near 2 MHz, then both capacitor selections work just fine. In fact, no capacitors might

work just as well.

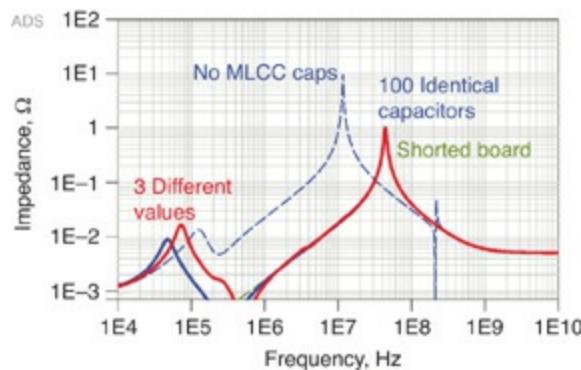
However, if there are large transient currents with frequency components at 30 MHz, both capacitor combinations are equally bad and no capacitors might actually be better.

**Tip**

Choosing three capacitors and using either all the same or three different values is completely arbitrary. Without information about the rest of the board, both choices are better than no capacitors, but are equally risky and neither offers a hope of a robust PDN.

In fact, just adding more capacitors with these fixed values only makes the board look more and more like a dead short at the Bandini Mountain peak frequency.

Figure 8.41 shows the simulated impedance profile with 100 total capacitors, all at 10  $\mu\text{F}$  and with 33 at 10  $\mu\text{F}$ , 33 at 1  $\mu\text{F}$ , and 34 at 0.1  $\mu\text{F}$ . In addition to there being no difference in the impedance profiles, they match the limiting case of a shorted board very closely.



**Figure 8.41** Impedance profiles of 100 capacitors added to the PDN ecology in two combinations: all the same 10  $\mu\text{F}$  and with three values of 10  $\mu\text{F}$ , 1  $\mu\text{F}$ , and 0.1  $\mu\text{F}$ . Each combination is identical to the Bandini Mountain with a shorted board.

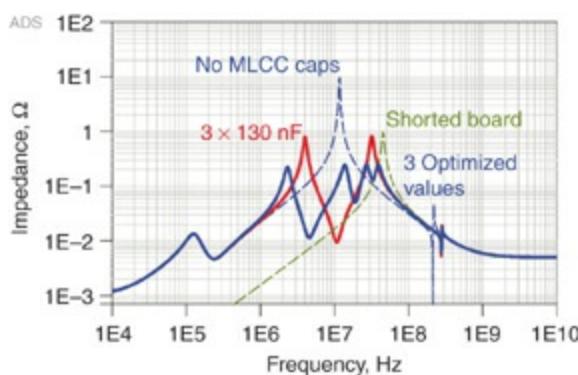
Whether we use all the same or three different values, or whether we use 3 capacitors or 300 capacitors, if we select them arbitrarily, the PDN will never be better than if the board were a dead short and shows a large

peak impedance at the Bandini Mountain. Just throwing more capacitors on the board has little impact on the Bandini Mountain peak. The PDN will not be robust and the product can be very expensive.

## 8.18 OPTIMIZING THE VALUES OF THREE CAPACITORS

In the examples in [section 8.16](#), using one value of capacitance, the lowest peak impedance was obtained if the capacitor value and number were optimized. When just one value of capacitance was used, the peak impedance, in this specific example, was reduced from  $10 \Omega$  to  $0.9 \Omega$ . We did this by implementing the lowest practical mounting inductance for the capacitor and selecting a [capacitor value that gave an SRF close to the peak of Bandini Mountain.](#)

When we use three capacitors, each with a different value of capacitance, we can find a new optimized combination. Using a simple SPICE circuit to manually try combinations that result in a minimum peak impedance, we find the optimized values of  $1000 \text{ nF}$ ,  $60 \text{ nF}$ , and  $20$  to give a peak height of less than  $0.3 \Omega$ . [Figure 8.42](#) compares the optimized impedance profiles when we used three capacitors, all the same value or three different values.



**Figure 8.42** Impedance profiles of the PDN ecology with optimized capacitors, three of identical value and three different values. Without MLCC capacitors, the peak impedance was  $10\ \Omega$ . With three identical optimized MLCC capacitors, the peak is reduced to  $0.8\ \Omega$ . With three different optimized capacitor values the peak impedance is reduced to  $0.25\ \Omega$ .

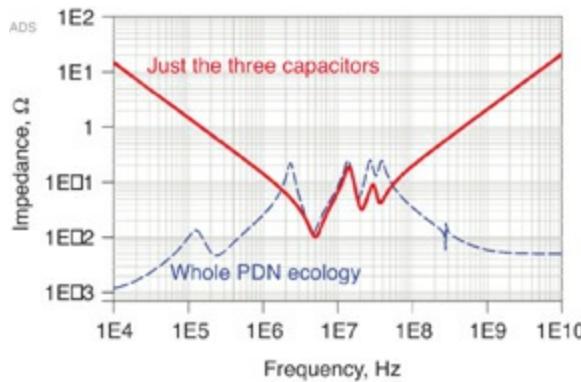
This example clearly shows the power of optimizing capacitors to reduce the peak impedance in a PDN. With just three capacitor values optimized for the entire PDN ecology, the peak impedance was reduced from  $10\ \Omega$  to  $0.25\ \Omega$ , a factor of 40 reduction. The risk associated with a high impedance peak was also reduced.

This is an example of achieving a lower peak impedance with three different optimized capacitor values than if the board were a dead short. This is due to the board-level damping contributed by the smaller value MLCC capacitors reducing the q-factor of the Bandini Mountain. In this example, the characteristic impedance of the Bandini Mountain is of  $0.07\ \Omega$  and its intrinsic q-factor is 14. Adding the capacitors reduced the peak to  $0.25\ \Omega$ , corresponding to a q-factor of about 3.5.

#### Tip

Using three optimized capacitor values dramatically reduces the peak impedance. This requires careful selection based on all the features of the PDN ecology. Selecting the optimum values without knowledge of the total ecology is difficult.

Looking at the impedance profiles of just the three different capacitors, alone and when mounted with the PDN ecology, is interesting. Figure 8.43 shows these comparisons.



**Figure 8.43** Comparing combinations of three capacitors mounted to the PDN (dotted lines) with the impedance of the three capacitors in isolation.

From these examples, we see the power of optimization. The optimum capacitor values depend very much on the on-die decoupling capacitance, the package lead inductance, and the ESL of each capacitor. If any of these parameters were to change, the capacitor values would not be optimized and there would be a larger peak impedance.

#### Tip

The only way to optimize the capacitor values using just three different capacitor values is if we know all the details of the Bandini Mountain and the capacitor models. The usual lack of information about all the details is why optimizing capacitor values when using only one or three different values is so difficult.

This approach suggests that optimizing the capacitor values to reduce the peak height of the Bandini Mountain might be possible, but only if we know all the details about the system.

**Tip**

If we are going to go to the trouble of optimizing the MLCC capacitor values, why limit ourselves to only three different values?

To first order, when the Bandini Mountain is high q, we want the board to contribute loss to damp out the peak impedance. The impedance profile of the board-level MLCC capacitors should look resistive around the Bandini peak with an impedance equivalent to the target impedance. To second order, we further optimize the capacitor values and the number we choose, using a circuit simulation to select for a reduced Bandini Mountain peak height.

This is the basis of the *Frequency Domain Target Impedance Method* (FDTIM) to optimize the capacitor value selection for the PDN.

### **8.19 THE FREQUENCY DOMAIN TARGET IMPEDANCE METHOD (**FDTIM**) FOR SELECTING CAPACITOR VALUES AND THE MINIMUM NUMBER OF CAPACITORS**

The principle of the FDTIM [9] is based on three important guidelines:

1. A minimum total number of capacitors is selected to reduce the total equivalent inductance of the board below the package lead inductance. This will result in a Bandini Mountain based on the on-die capacitance and package lead inductance.
2. When the Bandini Mountain has a high q-factor, which generally occurs when the peak frequency is less than 200 MHz, capacitor values and their number are selected to create a flat impedance profile close to the target impedance. This acts to damp out the Bandini Mountain. Too small a flat impedance value and there is not enough damping

resistance to reduce the high q-factor of the Bandini Mountain, and the capacitors will have no impact on the impedance profile. Too large a flat impedance and the peak will not be reduced below this impedance.

3. When the Bandini Mountain has a low q-factor, generally when the peak frequency is above 200 MHz, the resulting Bandini Mountain is not very sensitive to the board-level losses and the capacitor values will not have a large impact on reducing the Bandini Mountain peak impedance. Using enough capacitors to keep the board-level inductance small compared to the package lead inductance is important.

**Tip**

The goal of the FDTIM is to optimize the values and numbers of capacitors to result in a flat impedance profile with peaks below the target impedance. We can select these using a simple process involving capacitor ESR, manually optimized or even automated using a circuit simulation.

The first step in the capacitor selection process is to estimate the characteristic impedance and q-factor of the Bandini Mountain composed of the on-die capacitance and the package lead inductance. After all, this sets the limit to the lowest achievable PDN impedance. For a shorter board.

Of course, if the characteristic impedance of the Bandini Mountain is not significantly less than the target impedance, no capacitor combination brings the Bandini peak below the target impedance. In this case, the only way to engineer a robust PDN in this case is to

1. Increase the on-die decoupling capacitance.
2. Reduce the package lead inductance.
3. Add on-package capacitors.

For example, if the on-die decoupling capacitance is 50 nF and the package lead inductance is 0.25 nH, the characteristic impedance is

$$Z_0 = \sqrt{\frac{L_{\text{pkg}}}{C_{\text{die}}}} = \sqrt{\frac{0.25 \text{nH}}{50 \text{nF}}} = 71 \text{m}\Omega \quad (8.86)$$

The lowest possible target impedance that could be achieved in the absolute best case is 0.071 Ω. It is possible, in principle, to achieve a target impedance of about twice the characteristic impedance, or 0.15 Ω using optimized capacitor values.

The second step is to do everything possible to reduce the mounting inductance of all the MLCC capacitors. The parallel combination of all the capacitor mounting inductance, with the series contribution of the cavity spreading inductance, is in series with the package lead inductance.

We can estimate the number of capacitors needed using the two preceding conditions as

$$n_1 > 2\pi f_{\text{max\_lim}} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} = 2\pi \times 0.2 \text{GHz} \times \frac{1}{0.1} l = 13 \quad (8.87)$$

$$n_2 > \frac{\text{ESL}_{\text{cap}}}{L_{\text{package}}} = \frac{1}{0.25} = 4 \quad (8.88)$$

When the MLCC equivalent inductance is comparable to or less than the package lead inductance, additional capacitors will not reduce the series inductance with the on-die capacitance and more capacitors will have little impact on the Bandini Mountain. This sets a limit on the minimum number of capacitors that can make a difference. The minimum number is when their parallel inductance is equal to the package lead inductance in series with any spreading inductance. More than the minimum will have marginal impact, limited by the

cap L (in parallel) is in Series with pkge lead L, when seen by die

if cap L < pkge lead L, then pkge lead L will dominate

package lead inductance.

An extreme case might be

$$f_{\max\_lim} = 200 \text{ MHz} = 0.2 \text{ GHz}$$

$$Z_{target} = 0.001 \Omega$$

$$ESL_{cap} = 2 \text{ nH}$$

The minimum number of capacitors in this case is

$$n_{min} > 2\pi f_{\max\_lim} \times \frac{1}{Z_{target}} ESL_{cap} = 2\pi \times 0.2 \text{ GHz} \times \frac{1}{0.001} 2 \text{ nH} = 2500 \quad (8.89)$$

We see again the importance of lower mounting inductance. The lower the mounting inductance, the fewer capacitors required and the lower the cost.

**Tip**

Every pH of mounting inductance means more capacitors needed, which costs money. If it is free, you should do everything in the design of the capacitors' mounting to reduce their inductance.

## 8.20 SELECTING CAPACITOR VALUES WITH THE FDTIM

MLCC capacitors are not available in a continuous range of values. In most capacitor vendors' catalogs, capacitor values within one body size are distributed three values per decade with values of 1, 22, and 47. The typical highest value for small body size MLCC capacitors is roughly about 22  $\mu\text{F}$ .

The **smallest value capacitor** that we should use is roughly estimated based on the goal to select a capacitor with a self-resonant frequency higher than the highest frequency Bandini peak.

where capacitive behavior dominates of the cap

We get the self-resonant frequency of a capacitor with

$$f_{SRF} = \frac{159 \text{ MHz}}{\sqrt{ESL[\text{nH}] \times C[\text{nF}]}} \quad (8.90)$$

For this to be above the Bandini Mountain frequency requires

$$f_{\text{Bandini}} < f_{\text{SRF}} = \frac{159 \text{ MHz}}{\sqrt{\text{ESL[nH]} \times \text{C[nF]}}} \quad (8.91)$$

The capacitance is calculated for the SRF of the smallest capacitor to be above the Bandini peak frequency. With a peak frequency of 200 MHz and an ESL of 1 nH, the smallest capacitor value should be less than

$$C[\text{nF}] < \left( \frac{159 \text{ MHz}}{f_{\text{Bandini}}} \right)^2 \frac{1}{\text{ESL[nH]}} = \left( \frac{159 \text{ MHz}}{200} \right)^2 \frac{1}{1} = 0.6 \text{ nF} \sim 1 \text{ nF} \quad (8.92)$$

In the mobile computing space, a mounted capacitor might be as low as 0.3 nH. The lowest capacitance would then be 2 nF.

From 22  $\mu\text{F}$  to 1 nF, taking three different values per decade, there are as many as 14 different values of capacitors. This list is the pool of capacitor values from which to select.

If no information about the PDN ecology is available, the goal in engineering the capacitor selection is to get a flat impedance profile over the widest frequency range using as few different values and as few total number of capacitors as practical.

**Tip**

The goal in selecting the capacitor values and number of each value is to create an impedance profile that is flat and below the target impedance with as few capacitors as practical. This is the purpose of the FDTIM.

The simplest way of automating the number of capacitors for each value is to select their number so their minimum impedance is equal to the target impedance. When the target impedance is very small, on

the order of a few  $\text{m}\Omega$ , many capacitors at each value will be needed. With a distribution of three values per decade, the impedance minimums are close to the impedance maximums. Selecting for a minimum impedance below the target impedance gives an impedance distribution with peaks not far above the target impedance.

This condition is easy to estimate based on the ESR of each capacitor value. The minimum impedance at the SRF of each capacitor is related to the ESR of the capacitor and the number of capacitors with that value. We estimate the number of capacitors needed to bring the minimum impedance of the capacitor down to the target impedance from

$$Z_{\text{target}} = \frac{\text{ESR}_{\text{cap}}}{n_{\text{cap}}} \quad \text{or} \quad n_{\text{cap}} = \frac{\text{ESR}_{\text{cap}}}{Z_{\text{target}}} \quad (8.93)$$

This is a good approximate starting place for selecting the number of capacitors for each value. It works well for low target impedance, but is not very efficient for higher target impedances.

**Tip**

Automating the number of capacitors required based on bringing their minimum impedances below the target impedance is easy. It results in an impedance profile slightly above the target impedance. Selecting a target impedance slightly below the required impedance would result in a robust impedance profile.

For example, if the ESL of each capacitor were  $1 \text{ nH}$  and the maximum frequency is  $200 \text{ MHz}$ , and the target impedance is  $0.1 \Omega$ , our estimate for a minimum total number of capacitors would be 13.

When the target impedance is high, or the minimum number of total capacitors is on the order of 13, not every available value of capacitor from  $22 \mu\text{F}$  to  $1 \text{nF}$  will

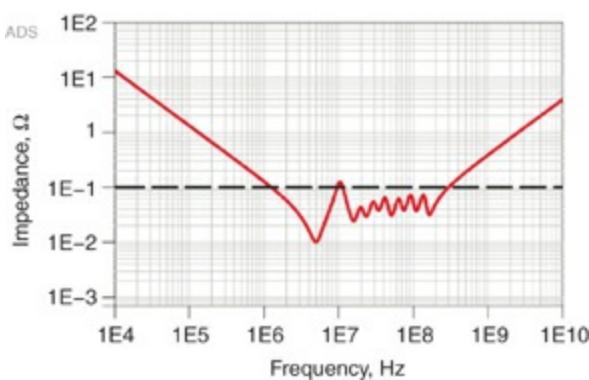
be used. The larger value capacitors will not contribute damping to the high q-factor Bandini Mountain, and can be selected one per decade value.

Using a simple SPICE circuit to simulate the impedance profile of many capacitors in parallel, we optimized the number and values to give a flat impedance profile, near, but below  $0.1 \Omega$ , from 1 MHz to 200 MHz. Below 1 MHz, the bulk capacitors must bring down the PDN impedance. Above 200 MHz, the on-die capacitance brings down the impedance profile. We used the following numbers and values of capacitors:

$22\mu F$	0
$10\mu F$	0
$4.7\mu F$	0
$2.2\mu F$	0
$1\mu F$	1
$470 nF$	0
$220 nF$	0
$100 nF$	1
$47 nF$	1
$22 nF$	1
$10 nF$	2
$4.7 nF$	2
$2.2 nF$	3
$1 nF$	5
<hr/>	
Total	16

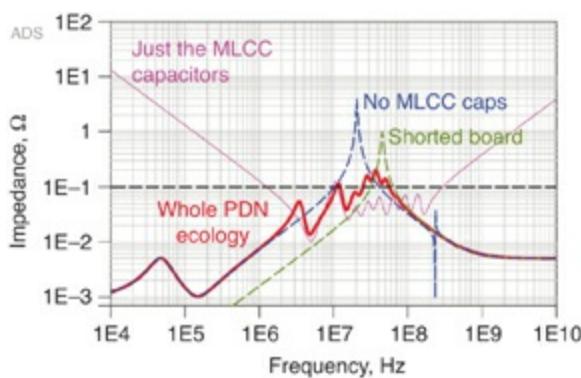
Bulk caps that have SRF at low freq, i.e. large C, according to  $1/\sqrt{LC}$ ,

This is close to our estimate of the minimum number of capacitors being 13. Figure 8.44 shows the impedance profile of just these capacitors and their equivalent series inductance and resistance. Note that they are slightly below the  $0.1 \Omega$  target impedance. Due to the discrete nature of the capacitors, it is not possible by reducing the number of capacitors to raise their peak impedances closer to the target value without going over.



**Figure 8.44** Simulated impedance profile of 16 capacitors distributed in value to result in a flat impedance profile from 1 MHz to 200 MHz.

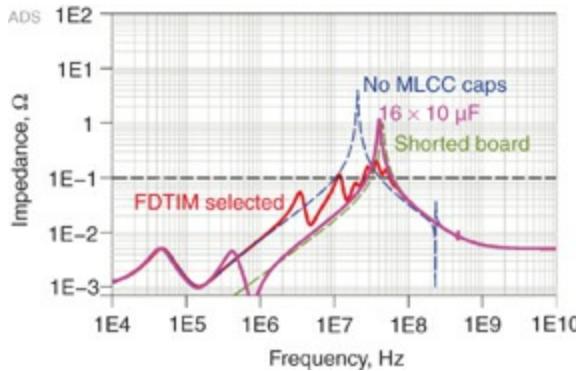
When we add these 16 capacitors to the complete PDN ecology, their flat impedance damps out the high q-factor Bandini Mountain and lowers the peak impedance. Figure 8.45 shows this impedance profile. In this example, we increased the bulk decoupling capacitors to provide the low impedance at low frequency. Without the MLCC capacitors, the peak impedance at the board level was  $3\ \Omega$ . With this distribution of capacitor values, the peak impedance was reduced to  $0.2\ \Omega$ . This is close to the practical limit of  $0.15\ \Omega$ .



**Figure 8.45** Simulated impedance profile of the 16 capacitors selected by the FDTIM attached to the rest of the PDN ecology showing a peak impedance of  $0.2\ \Omega$ .

The advantage of the FDTIM is to select a distribution of capacitors values without knowing the details of the Bandini Mountain. If 16 capacitors, all  $10\ \mu\text{F}$ , were added to the board, at best, they would make the board

look like a short and the impedance profile would be the Bandini Mountain of the on-die capacitance and package lead inductance. This has a peak height of  $1\ \Omega$ . We can reduce this by a factor of five using the FDTIM. Figure 8.46 shows this comparison of 16 capacitors selected by the FDTIM and chosen as all  $10\ \mu\text{F}$  values.



**Figure 8.46** Impedance profiles of 16 capacitors added to the board PDN ecology selected as  $16 \times 10\ \mu\text{F}$  and distributed using the FDTIM.

When the q-factor for the Bandini Mountain is low, as when the peak frequency is closer to 200 MHz, the impact from the capacitor selection is less and the peak impedance is not sensitive to the capacitor values.

## 8.21 WHEN THE ON-DIE CAPACITANCE IS LARGE AND PACKAGE LEAD INDUCTANCE IS SMALL

In this section we look at the case of a higher power device designed with a much higher on-die capacitance and engineered with a very low package lead inductance. The conditions are

$$\text{On-die capacitance} = 400\ \text{nF}$$

$$\text{Package lead inductance} = 0.0025\ \text{nH}$$

$$\text{On-die ESR} = 0.25/400 = 0.6\ \text{m}\Omega$$

The intrinsic properties of this Bandini Mountain are

$$Z_0[\Omega] = \sqrt{\frac{L_{\text{pkg}}[\text{nH}]}{C_{\text{ODC}}[\text{nF}]}} = \sqrt{\frac{0.0025\text{nH}}{400\text{nF}}} = 2.5\ \text{m}\Omega \quad (8.94)$$

$$f_{\text{Bandini}} [\text{MHz}] = \frac{159}{\sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]}} = \frac{159}{\sqrt{400 \text{nF} \times 0.0025 \text{nH}}} = 160 \text{ MHz} \quad (8.95)$$

$$\text{q-factor} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} = \frac{1}{0.25} \sqrt{400 \times 0.0025} = 4 \quad (8.96)$$

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{L_{\text{package}} [\text{nH}]}{0.25} = \frac{0.0025}{0.25} = 10 \text{ m}\Omega \quad (8.97)$$

If this device were attached to a board that had so many capacitors as to appear as a dead short, the Bandini Mountain peak impedance would be  $10 \text{ m}\Omega$ . With a characteristic impedance of  $2.5 \text{ m}\Omega$ , reducing the peak impedance much below  $5 \text{ m}\Omega$  will be difficult because a q-factor of less than 2 would be required.

If the target impedance is  $5 \text{ m}\Omega$ , a VRM with an output impedance no more than about  $1 \text{ m}\Omega$  is required. We assume an effective output inductance of the feedback loop as  $3 \text{ nH}$ . This requires a bulk decoupling capacitance of at least

$$C_{\text{bulk}} > \frac{1}{2\pi f_{\text{VRM-max}} \times Z_{\text{target}}} = \frac{2\pi L_{\text{VRM}}}{2\pi Z_{\text{target}} \times Z_{\text{target}}} = \frac{L_{\text{VRM}}}{Z_{\text{target}}^2} = \frac{3 \text{nH}}{0.005^2} = 120 \mu\text{F} \quad (8.98)$$

To the VRM, we add one bulk capacitor with the following features:

Bulk decoupling capacitance per capacitor:  $200 \mu\text{F}$

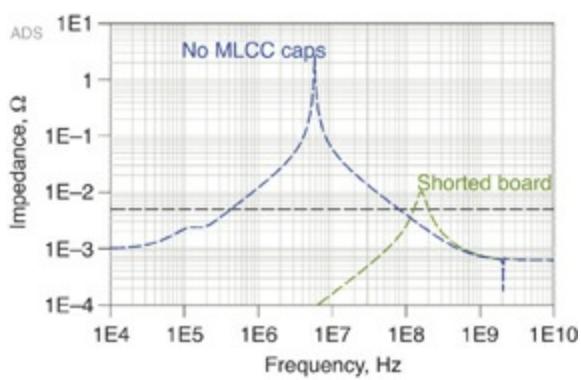
Bulk decoupling capacitor ESR:  $5 \text{ m}\Omega$

Bulk decoupling capacitor mounting inductance:  $5 \text{ nH}$

VRM inductance:  $3 \text{ nH}$

VRM resistance:  $1 \text{ m}\Omega$

Figure 8.47 shows the impedance profile of the shorted Bandini Mountain and the board-level PDN ecology. The Bandini Mountain peak impedance estimate of  $10 \text{ m}\Omega$  matches the simulation very well, as does the estimated frequency of  $160 \text{ MHz}$ .



**Figure 8.47** Impedance profiles of the board-level PDN ecology and the shorted Bandini Mountain.

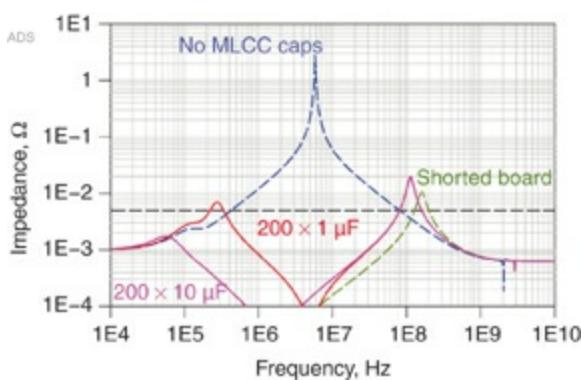
The goal of the board-level MLCC capacitors is to bring the peak impedance of  $3 \Omega$  as close to the ultimate practical limit of  $5 \text{ m}\Omega$  as possible, or to an acceptably low impedance level.

We can estimate the number of capacitors needed based on the two conditions introduced earlier:

$$n_1 > 2\pi f_{\max\_lim} \times \frac{1}{Z_{target}} \text{ESL}_{cap} = 2\pi \times 0.2 \text{ GHz} \times \frac{1}{0.005} \times 0.5 = 125 \quad (8.99)$$

$$n_2 > \frac{\text{ESL}_{cap}}{L_{package}} = \frac{0.5}{0.0025} = 200 \quad (8.100)$$

For either condition, this is a lot of capacitors. Even getting to this value required aggressively engineering the mounting inductance to be  $0.5 \text{ nH}$ . Figure 8.48 shows the impact of selecting 200 identical capacitors, either  $1 \mu\text{F}$  or  $10 \mu\text{F}$ . Their impedance profiles are identical, and closely match the shorted Bandini Mountain impedance.



**Figure 8.48** Impedance profiles of the PDN ecology with 200 identical capacitors, either 1  $\mu\text{F}$  each or 10  $\mu\text{F}$  each.

With no optimization of capacitor values but just adding enough to make a low equivalent series inductance comparable to the package lead inductance, the peak height is reduced from  $3 \Omega$  to  $.02 \Omega$ . This is a factor 100 reduction in peak impedance, a huge improvement.

These capacitors provide no real damping, so they do not reduce the Bandini Mountain peak below the intrinsic value. With a characteristic impedance of  $2.5 \text{ m}\Omega$ , this peak impedance is more than a factor of  $20/2.5 = 8$  above the characteristic impedance. This is a rough measure of the q-factor of this peak. This high value suggests that further reducing the peak height might be possible by applying the FDTIM.

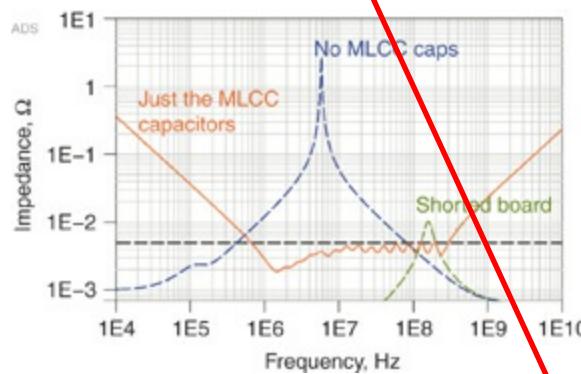
We estimated the number of capacitors required at each value to bring the impedance below the target impedance using

$$n_{\text{cap}} = \frac{\text{ESR}_{\text{cap}}}{Z_{\text{target}}} \quad (8.101)$$

This results in a distribution of values as

22µF	1
10µF	1
4.7µF	1
2.2µF	1
1µF	2
470nF	2
220nF	3
100nF	5
47nF	7
22nF	10
10nF	14
4.7nF	20
2.2nF	28
1nF	40
Total	135

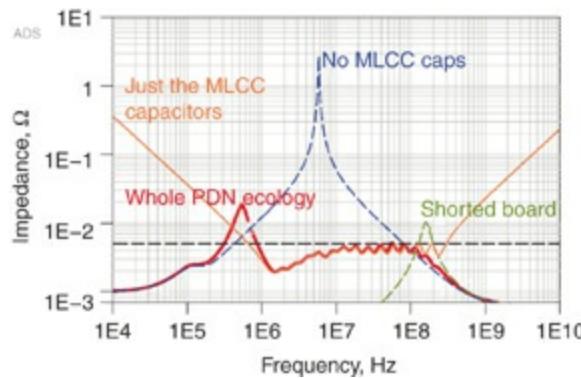
This distribution of capacitor values and numbers result in an impedance profile of just the capacitors, which meets the condition of being slightly below the target impedance of  $5 \text{ m}\Omega$ . Figure 8.49 shows the impedance profiles of the RDN ecology without MLCC capacitors and the Bandini Mountain with a shorted board, compared with the impedance profile of just these 135 capacitors.



**Figure 8.49** Impedance profile of 135 capacitors with three values per decade from  $22 \mu\text{F}$  to  $1 \text{nF}$  based on an impedance minimum below the  $0.005 \Omega$  target impedance, shown as the horizontal dotted line.

The smaller the capacitor value, the higher its ESR and the more capacitors needed at that value to bring their minimum impedance below the target impedance.

When these capacitors are added to the rest of the PDN ecology, the impedance profile is less than the intrinsic Bandini Mountain peak due to the higher damping. This results in a peak meeting the  $5 \text{ m}\Omega$  level. This impedance profile is shown in [Figure 8.50](#).



**Figure 8.50** Impedance profiles of the board-level PDN ecology with the 135 optimized capacitor values showing an impedance profile that meets the  $5 \text{ m}\Omega$  target impedance.

Without any MLCC capacitors, the peak impedance was  $3 \Omega$ . Just throwing 200 capacitors on the board, the peak was dropped to  $20 \text{ m}\Omega$ . The Bandini peak impedance when connected to a shorted board is  $20 \text{ m}\Omega$ . The slightly higher peak impedance with the identical value MLCC capacitors added to the board is because their parallel inductance is only comparable to the package lead inductance, and so about double the inductance of the Bandini Mountain.

When we add an optimized distribution of capacitors to the board with a total number of only 135 capacitors, but with a flat impedance profile, the resulting peak impedance drops below  $5 \text{ m}\Omega$  across the entire frequency range except for the low frequency.

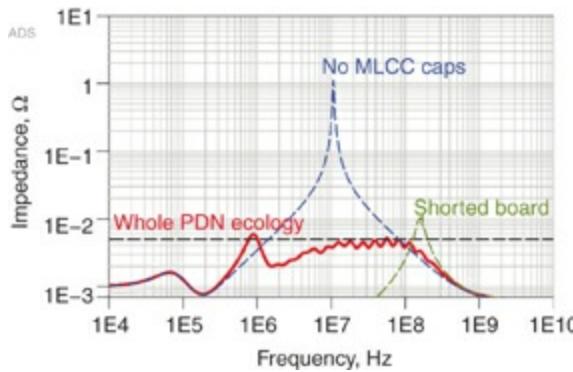
Although just throwing a lot of high-value capacitors onto the board is quick and easy and dramatically reduces the peak impedance value, using the FDTIM, without knowing any details of the Bandini Mountain, results in fewer capacitors and lower peak impedance.

This is a more robust design and lower cost.

**Tip**

Applying the FDTIM to select optimized capacitor values results in a lower cost *and* more robust PDN than just throwing a large number of high-value capacitors on the board.

There is still a slightly higher impedance in the 1 MHz frequency region due to the lower target impedance and using only one bulk capacitor. A larger parallel resonance exists between the VRM and bulk capacitor. We can easily manage this by reducing the mounting inductance of the bulk capacitor and adding more bulk capacitors. Figure 8.51 shows the final impedance profile with the mounting inductance to the bulk capacitors reduced from 5 nH to 4 nH and the number of 200  $\mu$ F capacitors increased from 1 to 6.



**Figure 8.51** The final PDN ecology impedance profile using optimized bulk capacitors and MLCC capacitors to bring the overall impedance profile below the target value across the entire frequency domain.

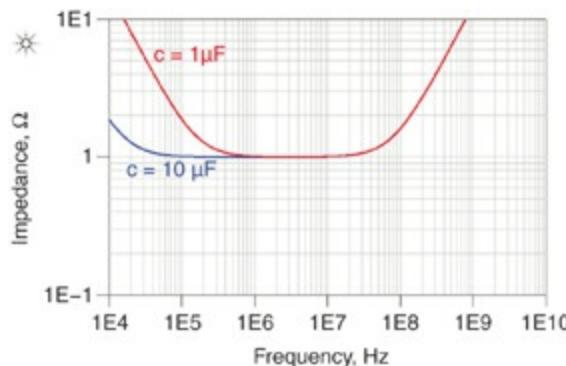
## 8.22 AN ALTERNATIVE DECOUPLING STRATEGY USING CONTROLLED ESR CAPACITORS

An important goal in PDN design is to reduce the impedance peak at the Bandini Mountain. We saw this accomplished by engineering the board-level impedance to look like a resistor with a flat impedance of roughly the target impedance. Using the FDTIM, we engineered the impedance profile by carefully selecting capacitor

values. Another way of achieving a flat impedance profile is to use controlled ESR capacitors.

Although these types of capacitors are currently not used as much as conventional MLCC capacitors, they can offer significant performance advantages and are much simpler to implement in a system. Typically, the maximum capacitance in a given body size is 1/10 that of a standard capacitor. Inductance might be higher because of the way controlled ESR is accomplished. They tend to be costly and are only offered by a few suppliers. Current values of capacitors available are 1  $\mu\text{F}$  and 10  $\mu\text{F}$  with resistances of 0.1 to 1  $\Omega$ .

When controlled ESR capacitors are added to the PDN ecology, as the only type of MLCC capacitor, their impedance is dominated by their higher ESR. The impedance profile shows a broad flat response centered at their SRF. Figure 8.52 shows the impedance profile of two controlled ESR capacitors, 1  $\mu\text{F}$  and 10  $\mu\text{F}$ , both with a 2 nH mounting inductance and 1  $\Omega$  ESR.



**Figure 8.52** Impedance profile of two controlled ESR capacitors with an ESR of 1  $\Omega$  and 2 nH of mounting inductance with 1  $\mu\text{F}$  and 10  $\mu\text{F}$  of capacitance. Note that the impedance profiles are flat and independent of capacitance in the frequency range of a typical Bandini Mountain.

Their impedance profiles, independent of capacitor value, are flat in the important frequency range. As always, getting the lowest mounting inductance is

important to offer the flat impedance up to the highest frequency.

A third condition is introduced to estimate the number of MLCC capacitors in addition to the previous two, restated here:

1. At the higher frequency, enough capacitors are needed so their inductive impedance is below the target impedance.
2. The inductance of the parallel combination of mounted board capacitors should be less than the package lead inductance. However, we reach a point of diminishing returns when the board inductance is much less than the package lead inductance.
3. In the mid-frequency region, enough capacitors are needed so their parallel resistance is close to and below the target impedance.

These conditions are

$$n_1 > 2\pi f_{\max\_lim} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} \quad (8.102)$$

$$n_2 > \frac{\text{ESL}_{\text{cap}}}{L_{\text{package}}} \quad (8.103)$$

$$n_3 > \frac{\text{ESR}_{\text{cap}}}{Z_{\text{target}}} = \frac{1}{0.1} = 10 \quad (8.107)$$

We consider the two case studies introduced in section 8.15. The first case uses the following conditions:

Target impedance =  $0.1 \Omega$

Up to  $0.2$  GHz

On-die capacitance:  $50$  nF

Package lead inductance:  $250$  pH

Cavity:  $2.4$  nF

MLCC capacitor: various

MLCC ESR: based on the C

MLCC ESL: 1 nH

Number: various

VRM inductance = 10 nH

VRM resistance = 1 mΩ

Bulk capacitor: 200 nF

Bulk capacitor ESL: 5 nH

Bulk capacitor ESR: 5 mΩ

Number: 1

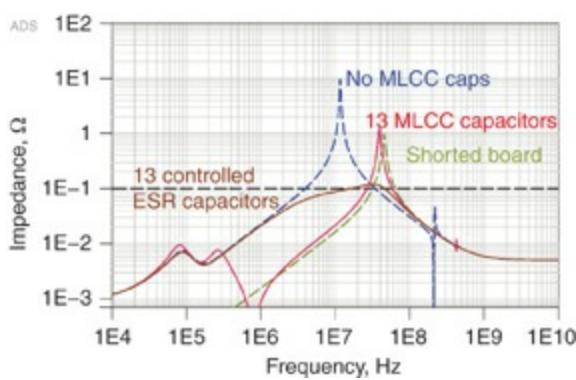
The three conditions for the number of MLCC capacitors, assuming an ESR of 1 Ω for the controlled ESR capacitor, are

$$n_1 > 2\pi f_{\max\_lim} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} = 2\pi \times 0.2 \times \frac{1}{0.1} 1 = 13 \quad (8.105)$$

$$n_2 > \frac{\text{ESL}_{\text{cap}}}{L_{\text{package}}} = \frac{1}{0.25} = 4 \quad (8.106)$$

$$n_3 > \frac{\text{ESR}_{\text{cap}}}{Z_{\text{target}}} = \frac{1}{0.1} = 10 \quad (8.107)$$

In this example, without knowing anything about the Bandini Mountain features, using 13 conventional capacitors results in a peak very close to the Bandini Mountain. This is shown in Figure 8.53. In this case, because the q-factor of the Bandini Mountain is high, if the board-level components provide no additional damping, the impedance profile will be similar to the intrinsic Bandini Mountain.



**Figure 8.53** Impedance profiles for the case of 13 capacitors added to the board-level PDN ecology, all the same  $10 \mu\text{F}$  conventional MLCC capacitors and 13 controlled ESR capacitors, each  $10 \mu\text{F}$  and  $\text{ESR} = 1 \Omega$ .

Using controlled ESR capacitors to add damping to the board, the peak impedance drops down to about  $130 \text{ m}\Omega$ . This is about two times the characteristic impedance of the Bandini Mountain and close to the best, practical peak impedance that can be obtained.

**Tip**

This example demonstrates the power of using controlled ESR capacitors. If the details of the Bandini Mountain are not known, they can be an effective way of archiving the lowest practical peak impedance. They are still no guarantee of meeting the target impedance, if the Bandini Mountain characteristic impedance is not below the target impedance.

The second example has the following conditions:

Target impedance =  $0.005 \Omega$

Max frequency =  $0.2 \text{ GHz}$

On-die capacitance:  $400 \text{ nF}$

Package lead inductance:  $2.5 \text{ pH}$

Cavity:  $2.4 \text{ nF}$

MLCC capacitor: various

MLCC ESR: based on the C

MLCC ESL:  $1 \text{ nH}$

Number: various

VRM inductance =  $3 \text{ nH}$

VRM resistance = 1 mΩ

Bulk capacitor: 200 nF

Bulk capacitor ESL: 5 nH

Bulk capacitor ESR: 5 mΩ

Number: 1

Up to 0.2 GHz

The estimated number of capacitors needed using the earlier three conditions are

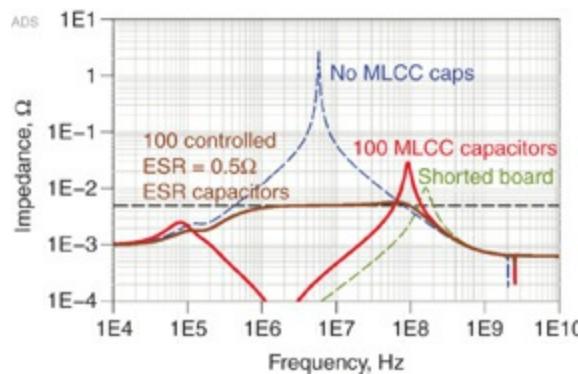
$$n_1 > 2\pi f_{\max\_lim} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} = 2\pi \times 0.2 \times \frac{1}{0.005} \times 0.5 = 125 \quad (8.108)$$

$$n_2 > \frac{\text{ESL}_{\text{cap}}}{L_{\text{package}}} = \frac{0.5}{0.0025} = 200 \quad (8.109)$$

$$n_3 > \frac{\text{ESR}_{\text{cap}}}{Z_{\text{target}}} = \frac{0.5}{0.005} = 100 \quad (8.110)$$

This suggests that we might obtain an acceptably low impedance profile with 100 controlled ESR capacitors each 0.5 Ω.

Figure 8.54 shows the impedance profiles for the two cases of  $100 \times 10 \mu\text{F}$  capacitors, each of them conventional and each of them as 0.5 Ω controlled ESR.



**Figure 8.54** Impedance profiles comparing conventional and controlled ESR capacitors.

Although the design of the PDN using controlled ESR capacitors is much simpler than using conventional ESR capacitors selected using the FDTIM, it comes at a

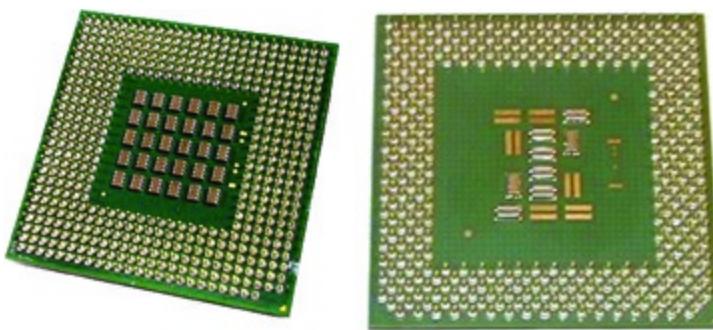
higher cost. The current costs of controlled ESR capacitors is about five times the cost of conventional capacitors. The integrated total cost of ownership (TCOO) is less than this premium because assembly costs sometimes dominate capacitor costs and the assembly costs are the same.

**Tip**

Given the simpler process of selecting controlled ESR capacitors, consider them as an option in designing the PDN. They offer less chance of design confusion. If their TCOO can be reduced to an acceptable level, they can be a viable option in a robust PDN design.

## 8.23 ON-PACKAGE DECOUPLING (OPD) CAPACITORS

Yet another alternative technology to consider for a robust and cost-effective PDN, especially for low target impedances, is adding on-package decoupling capacitors (OPD). This technique is typically implemented for the lowest target impedance devices and for high-end chips. Figure 8.55 shows a few examples of packages with OPD capacitors.



**Figure 8.55** On-package decoupling capacitors on opposite side from die.

Examples of multilayer packages with OPD capacitors. Because the real estate on packages is more expensive than on board and the package substrates are implemented with finer features, the OPD capacitors are typically interdigitated or reverse aspect ratio to enable

lower mounting inductance. Of course, this alternative would only be available to the semiconductor provider.

As customers of the semiconductor vendors, we should always ask for OPD capacitors. They always reduce the requirements of the board design and enable us to design for a lower target impedance. However, it comes at a more expensive semiconductor component cost.

**Tip**

Even though this added component cost might result in a lower total system cost, it is sometimes a difficult purchasing decision when the purchasing agent is graded on reducing component costs. This is why design engineers should be more involved in the purchasing decisions.

Generally, because the package substrate uses finer design rules than the board to accommodate the flip chip attach and high-density routing, we can use interdigitated and reverse aspect ratio capacitors, which require finer features for mounting. These generally have the lowest mounting inductance possible, on the order of 0.2 nH or less. In addition, the added cost of controlled ESR capacitors in these configurations is a smaller increment and more easily justified.

A simple example illustrates the power of OPD capacitors. In this case, the on-die capacitance is 400 nF with 10% of the total package lead inductance in the chip attach side, leaving 90% of the total chip to board inductance to the package to board side. The total chip-to-board mounting inductance is 50 pH.

The figures of merit for this Bandini Mountain are

$$Z_0[\Omega] = \sqrt{\frac{L_{\text{pkg}}[\text{nH}]}{C_{\text{ODC}}[\text{nF}]}} = \sqrt{\frac{0.05\text{nH}}{400\text{nF}}} = 11\text{m}\Omega \quad (8.111)$$

$$f_{\text{Bandini}} [\text{MHz}] = \frac{159}{\sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]}} = \frac{159}{\sqrt{400 \text{nF} \times 0.05 \text{nH}}} = 35 \text{ MHz} \quad (8.112)$$

$$\text{q-factor} = \frac{1}{0.25} \sqrt{C_{\text{ODC}} [\text{nF}] \times L_{\text{package}} [\text{nH}]} = \frac{1}{0.25} \sqrt{400 \times 0.05} = 18 \quad (8.113)$$

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{L_{\text{package}} [\text{nH}]}{0.25} = \frac{0.05}{0.25} = 200 \text{ m}\Omega \quad (8.114)$$

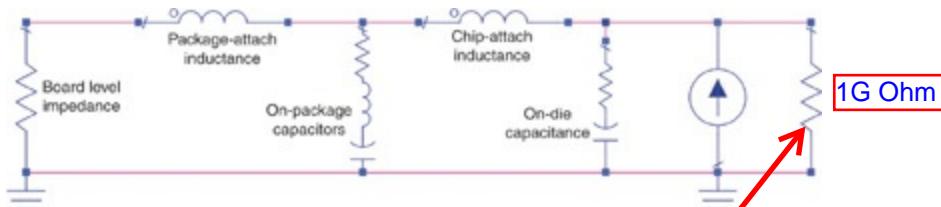
The large q-factor suggests that damping from other sources than the on-die resistance will be an important lever to engineer lower peak impedances. This is the condition when controlled ESR capacitors can have a large impact.

With a characteristic impedance of 11 mΩ, the lowest practical target impedance that could be obtained would be about 20 mΩ.

The minimum number of on-board MLCC capacitors that might be needed, assuming 0.5 nH mounting inductance using the assumptions in condition 1 is

$$n_l > 2\pi f_{\text{max\_lim}} \times \frac{1}{Z_{\text{target}}} \text{ESL}_{\text{cap}} = 2\pi \times 0.2 \times \frac{1}{0.02} 0.5 = 32 \quad (8.115)$$

Figure 8.56 shows the equivalent circuit of the OPD capacitors splitting the chip-attach inductance and the package-attach inductance.



**Figure 8.56** Equivalent circuit which includes the on-die capacitance, the OPD capacitors and the chip-attach and package-attach inductance. The resistor on the far right of the circuit is a high value to satisfy simulator DC path requirements.

In effect, the package-to-board inductance shorts out any parallel impedance from the OPD capacitors. If the

equivalent parallel mounting inductance of all the OPD capacitors is significantly greater than the 0.045 nH of package-to-board inductance, the OPD capacitors would have little impact on the die-pad impedance.

However, when the parallel combination of the OPD capacitors is comparable to or smaller than the package to board inductance, the OPD capacitors split the Bandini Mountain into two peaks. This is the first important criterion for effective OPD design and selection.

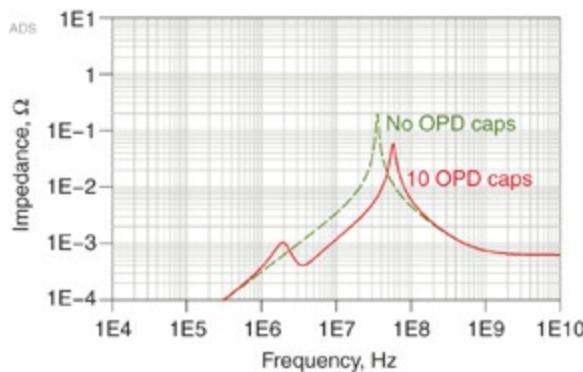
In this case, the higher frequency Bandini Mountain resonance is created by the parallel combination of the on-die capacitance and the equivalent inductance of the OPD capacitors in parallel with the package-to-board mounting inductance.

The parallel inductance of the OPD with the package-to-board mounting inductance is always less than the package-to-board mounting inductance by itself. This has two consequences. First, the peak frequency is shifted to higher frequency and second, the characteristic impedance of the modified Bandini Mountain is decreased for this peak. This contributes to a lower impedance peak height [10].

A lower frequency peak is created by the parallel combination of the OPD capacitance and the package-to-board inductance in series with the OPD inductance. As long as the OPD capacitance is much larger than the on-die capacitance, this lower frequency peak is always at lower frequency and lower characteristic impedance than the Bandini Mountain without the OPD.

Figure 8.57 is an example of the impedance from the die pads, with and without ten OPD capacitors, each with 0.2 nH of mounting inductance and 10  $\mu$ F in size. Their parallel inductance is 20 pH, about half the package-to-board loop inductance. This illustrates the

two important impacts of adding OPD capacitors.

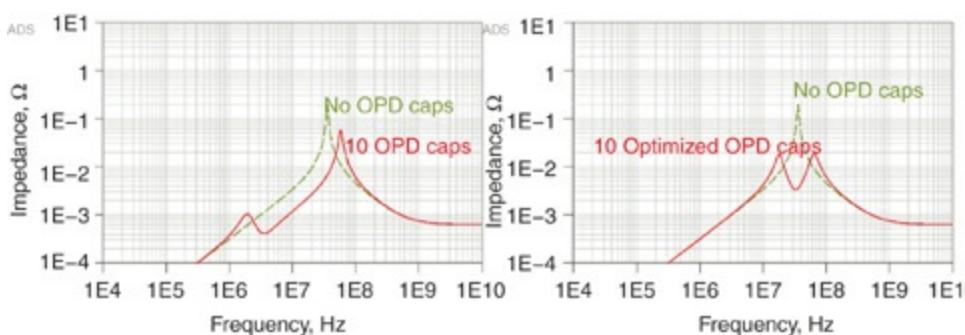


**Figure 8.57** Impedance profile from the die pads, with and without OPD capacitors with the package connected to a shorted board. In this example, 10 OPD were added, with a parallel inductance about half the package-to-board inductance.

Just as with any single-valued capacitors added to a circuit with an existing parallel resonance, we can optimize the capacitor value for the lowest peak impedance. A good approximation of the optimum capacitance is when the SRF of the added OPD capacitors is close to the Bandini Mountain peak with no OPD. In this example, the OPD capacitor value required is about

$$C_{OPD} = C_{on-die} \frac{ESL_{totalPkgAttach}}{ESL_{OPD}} = 400 \text{ nF} \frac{0.05 \text{ nH}}{0.2 \text{ nH}} = 100 \text{ nF} = 0.1 \mu\text{F} \quad (8.116)$$

It is not true that more capacitance or more capacitors are always better. A few OPD capacitors, with optimized capacitor values, are much better than a lot of unoptimized capacitors. Figure 8.58 shows the decrease in impedance peak height using 10 OPD capacitors 0.1  $\mu\text{F}$  each compared with 10 10  $\mu\text{F}$  capacitors. The reduction in peak impedance is from 60 m $\Omega$  to 20 m $\Omega$ .



**Figure 8.58** Die pad impedance profiles with different combinations of single-valued OPD capacitors: 10  $\mu\text{F}$  and 0.1  $\mu\text{F}$  capacitor values.

This illustrates the importance of knowing the details of the Bandini Mountain to enable optimized capacitor selection. A lot of large value capacitors is not better than a few optimized capacitors.

**Tip**

Costs generally go up with increased component count. The most robust solution is with the lowest peak height. The most robust and cost-effective solution is when the OPD capacitor value is optimized for the chip-package Bandini Mountain.

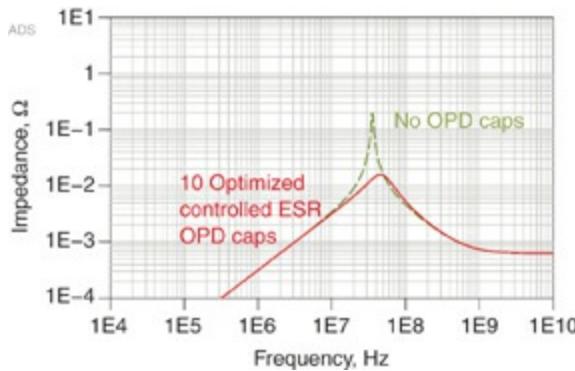
When using OPD capacitors, making them as controlled ESR capacitors is often cost effective. The purpose of the capacitors is to provide more damping to lower the q-factor and reduce the Bandini Mountain.

The condition is to engineer their parallel resistance to be close to the target impedance. In this example, the characteristic impedance of the Bandini Mountain is 2.5 m $\Omega$ . The lowest target impedance that might be achieved in practice is about 5 m $\Omega$ . If only 10 controlled ESR capacitors are used, the optimum value of the controlled ESR is 0.05  $\Omega$ .

$$n_3 > \frac{\text{ESR}_{\text{cap}}}{Z_{\text{target}}} = \frac{0.05}{0.005} = 10 \quad (8.117)$$

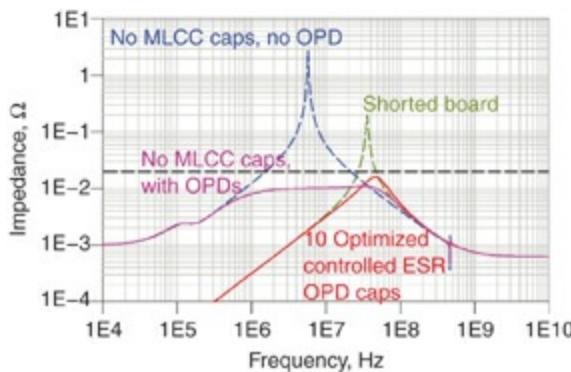
The lowest value of a controlled ESR capacitor generally available is 0.1  $\Omega$ . This would result in a final

impedance close to  $10 \text{ m}\Omega$ . Figure 8.59 shows the simulated impedance profile of 10 controlled ESR capacitors each of  $0.1 \Omega$  ESR. The peak impedance is reduced to about  $15 \text{ m}\Omega$ .



**Figure 8.59** Impact on the impedance profile using 10 controlled ESR capacitors.

When we place this package on the board, the impedance profile when interacting with the rest of the PDN ecology is remarkably stable. Figure 8.60 shows the impedance profile when the package is connected to a short, with and without the OPDs using controlled ESR capacitors, and when connected to the board, with and without these OPDs.



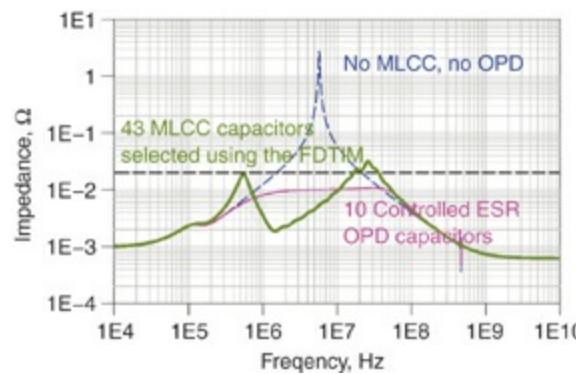
**Figure 8.60** Impedance profiles comparing with and without controlled ESR OPD capacitors.

It is remarkable the power of the controlled ESR capacitors to manage the peak impedances from the Bandini Mountain.

Using just 10 controlled ESR capacitors on the package, each  $10 \mu\text{F}$  in size, we would need no additional

MLCC capacitors on the board to keep the impedance below this target impedance.

The alternative is using the FDTIM to optimize the values of conventional MLCC capacitors to meet the target impedance. Using the FDTIM outlined in [section 8.20](#), 43 capacitors were selected, slightly more than the 32 minimum number estimated above. [Figure 8.61](#) shows the impedance profiles from the chip pads, for the entire PDN ecology, for the cases of 10 controlled ESR capacitors and 43 MLCC board-level capacitors selected using the FDTIM algorithm.



**Figure 8.61** Impedance profiles as seen on the die pads for the same chip and package, for the two cases of using controlled ESR OPD and using conventional MLCC capacitors on the board.

This example illustrates the value of using controlled ESR capacitors in the package. The result is a more robust PDN with fewer components and a flatter impedance profile. The cost is the addition of more expensive controlled ESR capacitors taking up the more expensive real estate of the package. However, this approach also reduces the risk of not selecting optimized capacitor distributions on the board. OPD controlled ESR capacitors can dramatically reduce the burden of on-board MLCC capacitors.

**Tip**

Using controlled ESR capacitors as OPD dramatically reduces the requirements for MLCC capacitors on the board. This is a significant risk reduction step. Many large FPGA, processor and ASIC packages use controlled ESR OPD capacitors for this reason.

## 8.24 ADVANCED SECTION: IMPACT OF MULTIPLE CHIPS ON THE BOARD SHARING THE SAME RAIL

So far in this analysis, we've considered one power rail used to deliver clean power to one chip. In many products, multiple chips share the same power rail on the board. In this case, the other chips act as decoupling capacitors on the board.

From the die pad's perspective on one chip, looking into the PDN, the other chips look like board-level decoupling capacitors, just like MLCC capacitors. The difference is that the component values are different from conventional MLCC capacitors.

The ESL value will generally be lower than a typical MLCC, because there are multiple power and ground connections in parallel. This is a good feature, because it will help to reduce the parallel inductance of the other MLCC capacitors.

The on-die ESR value is often lower than an MLCC's. For example, a 50 nF on-die capacitance might have an ESR of  $0.25/50 = 5 \text{ m}\Omega$ , whereas a 50 nF MLCC would have an ESR of about

$$\text{ESR} [\Omega] = \frac{0.2}{C[\text{nF}]^{0.43}} = \frac{0.2}{50^{0.43}} = 37 \text{ m}\Omega \quad (8.118)$$

This is generally not a good feature, because it will not contribute to any damping of the Bandini Mountain, and might short out damping already present.

The capacitance is generally on the order of 50 to 500

nF, in the range similar to MLCC capacitors.

One metric of the impact the other chips play in the PDN comes from the self-resonant frequency of the on-die capacitance and package lead inductance, as viewed from the board side looking into the package. We derive the SRF with

$$f_{\text{SRF}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{pkg}}[\text{nH}] \times C_{\text{die}}[\text{nF}]}} \quad (8.119)$$

When the two die on the board are identical, the SRF of one chip as seen on the board will be the same as the Bandini Mountain frequency. For typical values of package lead inductance of 0.25 nH and on-die capacitance of 50 nF, the SRF is on the order of

$$f_{\text{SRF}} = \frac{159 \text{ MHz}}{\sqrt{L_{\text{pkg}}[\text{nH}] \times C_{\text{die}}[\text{nF}]}} = \frac{159 \text{ MHz}}{\sqrt{0.25 \times 50}} = 45 \text{ MHz} \quad (8.120)$$

The SRF of the various packaged chips on the board appear as capacitors with SRF values in the vicinity of the Bandini Mountain of the other chips.

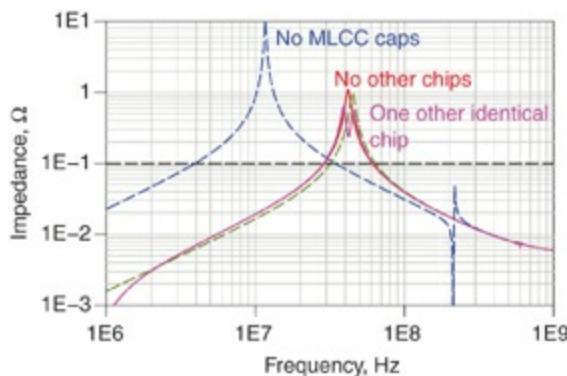
The presence of the other chips will have a different impact in a system where the board-level components do not contribute damping and when the board-level components do provide damping.

When many, unoptimized MLCC capacitors are on the board, the PDN impedance, as viewed at the die-pads on one chip, has a Bandini Mountain at roughly the shorted value. The MLCC capacitors are just to reduce the inductance of the board-level PDN and results in the shorted Bandini Mountain profile. The addition of other low-loss capacitors with SRF near this frequency has the impact of slightly reducing the Bandini Mountain.

### Tip

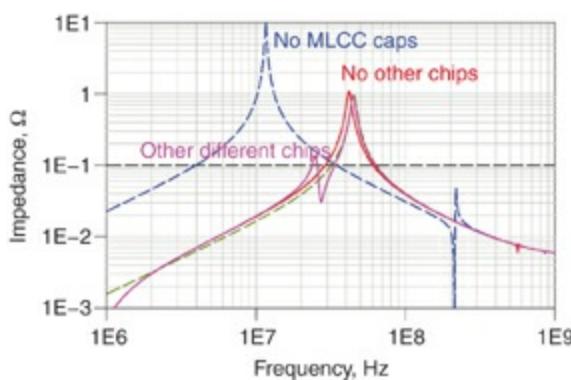
Without the intent to optimize performance, the presence of the other chips on the board generally has the impact of slightly reducing the Bandini Mountain. This means that having more chips on the board sharing the same power rail might reduce the peak impedances, if the MLCC capacitor values are not optimized.

Figure 8.62 shows an example of this behavior. Two identical chips are on the board. One of them acts as a decoupling capacitor for the other. Because they have the same resonant frequency, one splits the Bandini Mountain of the other. Thirteen other  $10 \mu\text{F}$  capacitors are on the board with an ESL of  $0.5 \text{ nH}$  each.



**Figure 8.62** Impedance profiles from the pads on one die with a board having 13  $10 \mu\text{F}$  MLCC capacitors and with and without another chip on the board.

Generally, the resonant frequencies of the various chips on the board will not be the same. This means the impact from other chips on the board will be at frequencies other than the Bandini Mountain. Figure 8.63 shows an example of the impedance profiles with and without multiple, non-identical chips on the board. The impact is to reduce the peak height of the Bandini Mountain, very slightly.

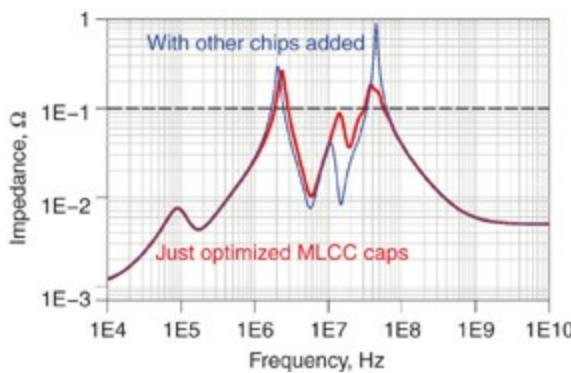


**Figure 8.63** Impedance profiles of a board with 13 identical MLCC capacitors and with and without multiple, non-identical chips. Note only a slight difference in the Bandini Peaks.

**Tip**

The impact from other chips on the board will slightly decrease the Bandini Mountain and add small resonances at other frequencies.

When we select the MLCC capacitor values to provide a flat impedance, they contribute to damping the Bandini Mountain and decrease its intrinsic impedance peak. When we add chips to the board, they typically lower ESR and lower ESL will act to short out some of this damping resistance and cause the Bandini Mountain peak to grow. **Figure 8.64** is an example of an optimized MLCC capacitor distribution with the same additional chips added to the shared power rail.



**Figure 8.64** Impedance profiles for the same board with optimized MLCC capacitors that contributes damping of the Bandini Mountain. Adding a few chips to the board shorts out the damping resistance and increases the Bandini Mountain peak impedance.

**Tip**

The impact of additional chips sharing the power rail might make a poor PDN slightly less poor, although it might make a robust PDN slightly less robust.

## 8.25 THE BOTTOM LINE

1. The PDN ecology consists of all the interconnects from the pads on the die to the pads of the VRM. Every element in the PDN contributes to the impedance profile, with some elements dominating performance in certain frequency ranges.
2. At the highest frequency, the on-die decoupling capacitance provides the low impedance at the highest frequency.
3. The most important features of the PDN are the peak impedances. These usually arise from the parallel combination of a capacitor and inductor.
4. The most important parallel resonance is between the on-die decoupling capacitance and the package lead inductance. We give this peak the special name, the Bandini Mountain.
5. The two most important figures of merit for the Bandini Mountain are its characteristic impedance and the peak frequency. The characteristic impedance sets the lowest possible peak impedance for the PDN. The peak frequency is most commonly in the 10 MHz to 100 MHz range.
6. The only role the power and ground planes play is to provide low spreading inductance from the MLCC capacitors to the pads of the BGA. Cavity resonances and the capacitance in the cavity play only a tiny role in the PDN impedance. The size of the cavity is irrelevant for the quality of the PDN as viewed from the die.

7. The most important design principle when selecting the capacitor values for the PDN is to reduce the peak impedance of the Bandini Mountain reasonably close to the target impedance.
8. Using identical values or three different decade values of MLCC capacitors makes little difference in their impact on the PDN impedance. If you don't know the on-die capacitance and package lead inductance, optimizing the capacitor values is difficult.
9. One effective way of reducing the Bandini Mountain peak is to make the board-level PDN impedance look like a resistor with a resistance equal to the target impedance, in the range of roughly 1 MHz to 50 MHz. This provides damping for the Bandini Mountain.
10. The frequency domain target impedance method (FDTIM) is a process that selects capacitor values to produce a flat impedance profile. If you know the features of the Bandini Mountain, you can select capacitor values to reduce the Bandini Mountain. If you do not know them, the FDTIM results in the most robust PDN.

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# Chapter 9. Transient Currents and PDN Voltage Noise

## 9.1 WHAT'S SO IMPORTANT ABOUT THE TRANSIENT CURRENT?

The voltage noise generated on the core power distribution network depends strongly on the specific transient current flowing between the Vdd and Vss rails and the PDN impedance. If the PDN current draw of the die were constant, the only consideration in PDN design would be the PDN's DC resistance. This quality is referred to as the IR drop in the PDN.

Because many regulators have an external sense line that is used as the source of feedback voltage to regulate the output voltage, attaching the sense lines in close electrical proximity to the die pads ensures the constant DC voltage is close to the intended voltage. This allows for a trivial PDN design effort and we wouldn't have to worry about anything other than resistance.

Rarely are we afforded the luxury of a die routinely running microcode that results in a constant PDN current. The specific transient current waveform, its frequency components and when they turn on, along with the PDN impedance, are ultimately what determine the voltage noise on the die pads. This means defining a robust spec for the PDN impedance is not possible without knowing the important features of the transient current for the specific devices being fed by the PDN.

### Tip

Defining a spec for a robust PDN is not possible without knowing some details of the worst-case transient currents generated by the die during its operation. Not knowing the transient current features means we can do no better than guess at an acceptable PDN.

Of course, the current through the core or I/O depends strongly on the chip's specific functioning, which might vary from application to application, depending on the microcode running at any moment. By examining a few special cases with simplified assumptions, we can create an approximate, parameterized model for the transient current to use to explore design space and find reasonable limits and a basis for a PDN impedance specification.

**Tip**

More accurate knowledge of the core transient current's specific features results in more accurate specifications for the PDN impedance and voltage rail noise. This means smaller design margins required and a more cost-effective design.

The voltage on the die's power rail depends in a complex way on the rail's transient current load and the PDN's impedance profile. What makes this analysis tricky is that we describe the transient current load stimulus in the time domain, and the impedance profile in the frequency domain.

The explicit assumptions we have to make to use a frequency domain description of the impedance profile to analyze the voltage response from a time domain current stimulus is that the circuits responsible for the impedance profile are linear and time invariant.

These assumptions are not always met, especially in the VRM and the die's dynamic load. Both of these features result in impedance profiles, and especially damping qualities, that change with time as the microcode running in the core executes. As illustrated in this chapter and Chapter 10, transient simulation results can closely match the predictions based on a time invariant analysis given the correct assumptions.

In particular, we analyze the voltage response from

three specific transient current waveforms. Each transient current waveform is sensitive to a different feature in the frequency domain description of the PDN, which influences the voltage response. Based on these behaviors, we can make some generalities about the PDN impedance profile's performance requirements.

These three specific transient current waveforms are

- The single clock pulse, impulse response
- Step current response
- Resonant response

In each case, the transient current waveform's features interact with the PDN impedance profile's features to create a specific voltage response. Knowing any two of the terms allows us to estimate the third.

**Tip**

The three important terms are transient current waveform, impedance profile, and voltage response. If we know any two of the features we can deduce the third for each specific transient current waveform. We can take advantage of this valuable observation to advance our knowledge of the PDN design from generation to generation.

We apply and extend any knowledge learned about the PDN features and load current in one generation of product to the next generation of product. This is often all the starting information we have for a PDN design.

In this chapter, we explore the design features that influence the voltage response from a transient current. A few special-case transient current waveforms stimulate the well-understood voltage responses. These enable interpretations of the PDN impedance profile, including the interaction with specific current patterns, to create voltage responses.

In its simplest structure, a PDN impedance profile is composed of two behaviors: flat regions and peaks. The

impedance profile of a flat region is constant with frequency. Each peak is described in terms of a resonant frequency, a characteristic impedance, and a q-factor. The transient current waveforms interact with these two regions differently.

By analyzing the voltage response for each transient current waveform from flat regions and peaks, we can set limits on acceptable features in the PDN impedance profile. We first consider a flat impedance profile and a transient current with broadband spectral content.

## 9.2 A FLAT IMPEDANCE PROFILE, A TRANSIENT CURRENT, AND A TARGET IMPEDANCE

If the PDN impedance profile is flat with frequency, that is, behaving like a resistor, then the voltage noise response to any transient current is directly related to the flat impedance value, as

$$V_{\text{noise}} = I_{\text{transient}} \times Z_{\text{PDN}} \quad (9.1)$$

The goal in PDN design is to keep the PDN voltage noise below some tolerance noise limit, given by

$$V_{\text{tolerance}} = V_{\text{dd}} \times \text{tolerance} \quad (9.2)$$

This defines a limit to the voltage noise as

$$V_{\text{noise}} = I_{\text{transient}} \times Z_{\text{PDN}} < V_{\text{dd}} \times \text{tolerance} \quad (9.3)$$

To achieve this voltage noise limit requires the flat impedance be below a value defined as the **target impedance** [1][2]:

$$Z_{\text{PDN}} < \frac{V_{\text{tolerance}}}{I_{\text{transient}}} = \frac{V_{\text{dd}} \times \text{tolerance}}{I_{\text{transient}}} = Z_{\text{target}} \quad (9.4)$$

For example, a 1 volt PDN that supports a worst-case 1 A transient current with broadband frequency components and has a 5% voltage tolerance, which is 50

mV, has a target impedance of

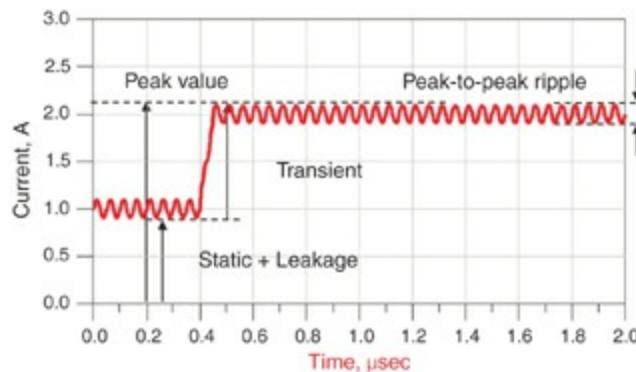
$$Z_{\text{target}} = \frac{V_{\text{dd}} \times \text{tolerance}}{I_{\text{transient}}} = \frac{1 \text{ volt} \times 5\%}{1 \text{ A}} = 50 \text{ m}\Omega \quad (9.5)$$

**Tip**

The target impedance is a starting place to define a limit on the PDN impedance in the flat regions, based on knowledge of the worst-case transient current.

To calculate a target impedance for the PDN's flat regions, we need an estimate on the worst-case transient current load.

The starting place model for the core PDN current draw for a die is a transient change in current between a minimum value and a maximum value. [Figure 9.1](#) shows an example of a simple core current behavior with a transient change.



**Figure 9.1** A simple example of a transient current showing a quiescent current level followed by a peak or maximum current draw. The difference between these two levels is the transient current.

The **transient current** is the maximum current change in the current drawn by the die for any possible operation. This usually occurs when the chip operation changes from an idle state to a heavy logic transition load. In this case, the transient current is just the difference between the two limits

$$I_{\text{transient}} = I_{\max} - I_{\min} \quad (9.6)$$

In a typical case with a constant clock frequency, the minimum current is due to static operation plus leakage current and maybe some clock generation and distribution circuitry. The peak current, or maximum current, is when the device is drawing the most current from the PDN.

### **9.3 ESTIMATING THE TRANSIENT CURRENT TO CALCULATE THE TARGET IMPEDANCE WITH A FLAT IMPEDANCE PROFILE**

The real challenge in establishing a target impedance is in getting values for the transient current. This information is rarely provided by the semiconductor vendor, as it often depends on the microcode running and the specific application.

One term that is often available is the maximum current draw for a rail. This is the basis for determining the specs for the VRM. If the maximum current is known, the task is then to decide how much of this maximum current actually changes to be considered transient current.

In one extreme, a device is sitting at very low idle current and suddenly turns on full force, drawing its maximum current. In this case, the transient current is the maximum current.

In the other extreme, the device is always running the same code and always drawing the same, constant current, in which case the transient current is nearly zero except at start up.

Without any specific knowledge of the device's operation, we can still make some estimates to bound the problem. In a typical FPGA and large gate count chips, the difference between the minimum, steady-state current, and the maximum rated current may be about 50%. It depends a lot on the aggressiveness of the

chip's power-saving techniques. Two decades ago, some processor chips consumed 90% of power when they were idle. This was back in the days when power consumption was not a big issue. Many chips in the mobile industry can go from 1% to 100% power in just a few microseconds or less. For these chips, the transient current is 100% of their maximum current. Without any other information, 50% of the maximum current is a good estimate for the transient current

$$I_{\text{transient}} = 0.5 \times I_{\text{max}} \quad (9.7)$$

We then use this value to estimate the target impedance as our starting place when establishing a design spec for the flat portion of the PDN.

**Tip**

Although you should always ask your semiconductor vendor for the worst-case transient current values for their devices, rarely will you get a realistic answer. You must often rely on estimates.

This means inherent uncertainty exists in the transient current and therefore in the calculated target impedance.

**Tip**

You can always "buy insurance" to reduce risk by assuming a lower target impedance and paying more for the PDN. The better your knowledge, the less insurance you have to buy.

## 9.4 THE ACTUAL PDN CURRENT PROFILE THROUGH A DIE

At its simplest, the current behavior through the PDN rails on a die is modeled as a constant current source, with some modulation. This is a good first-order model for the die behavior, which allows us to quickly simulate some of the important features and design guidelines

for a robust PDN. However, it is not actually how the current draw from the PDN behaves.

In this section, we introduce a more sophisticated model for the on-die PDN current draw, which allows us to create a set of standard switching waveforms that are used to test and characterize a PDN.

**Tip**

Using switched current patterns, we find the most pathological cases that test the limits of a robust PDN.

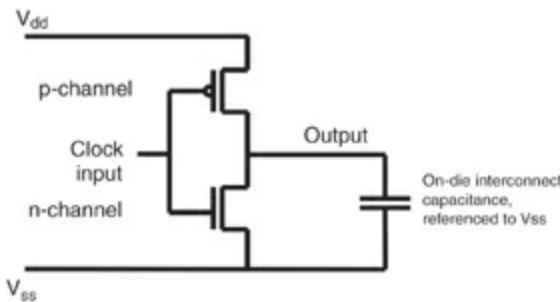
Modeling the current flow through the core of a chip is complicated in general. It depends on the precise current draw from each gate, each gate's relative timing, and the microcode running. The microcode determines how many gates switch in the core region. Circuits that share the same power and ground rails have a common impedance in the metallization that distributes the power to the core on-die gates.

With a transistor-level model of the core and a parasitic extraction of the interconnects distributing current to the gates of the core, simulating the specific current through each of the Vdd and Vss connections to the core gates is possible. Simulating PDN current for the specific microcode running on the device might even be possible. This is a complicated process and requires detailed models of the gates, interconnects, and software. After we are done, we have a point solution for that specific modeled system and code with no guarantee of other microcode performance or insights to apply to the next design.

**Tip**

As a practical approach, approximating the current flow in a core region of a chip and estimating the current signature and its magnitude under typical and worst-case conditions is possible. The specific details vary from device to device, but the general approach is the same. The starting place is the current flow through each gate that makes up the core.

In a typical CMOS-based system, the fundamental circuit for a simple inverter gate is a push-pull circuit composed of the series combination of a p-channel and n-channel FET between the Vdd and Vss rails, as diagrammed in [Figure 9.2](#). The gate output drives some number of inputs to other gates configured into combinational logic elements and blocks.



**Figure 9.2** A simplified electrical model of a gate on-die driving a capacitive load. The capacitance between the driven line and Vss depends on the input gate capacitance of the next gate and the interconnect metallization.

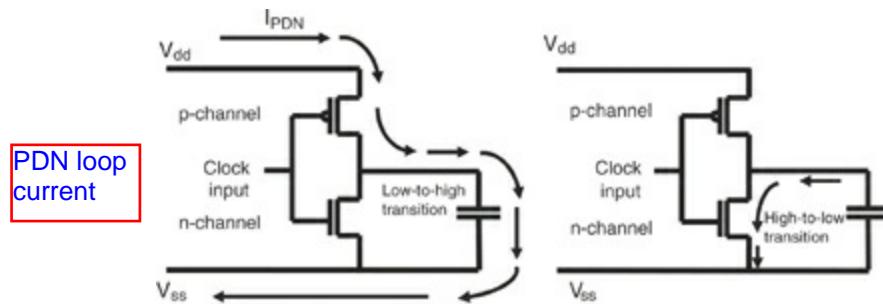
The output load any one gate sees is the capacitance of the combination of the metallization of the output net and input gate capacitances of the gates connected to its output. Electrically, the load looks like a single lumped capacitor. Other functional gates have a similar architecture, driving a capacitive load.

**Tip**

Each of the internal gates on-die is driving some lumped capacitive load depending on what they are connected to.

The equivalent circuit of the capacitive load depends on the interconnect metallization and the Vdd and Vss lines on the die. To introduce this topic, assume that the interconnect metal is near only Vss metal layers and other signals that are driven to Vss. In this case, the capacitance is referenced only to Vss and is modeled as a single capacitor.

When the p-channel turns on, the output node experiences a rising transition, charge flows through the p-channel into this single capacitor from Vdd, and the voltage on the output capacitor rises. When the p-channel turns off and the n-channel turns on, the output node experiences a falling transition. Charge flows through the n-channel, out of the capacitor in the negative direction and it discharges. [Figure 9.3](#) shows these current flow patterns.

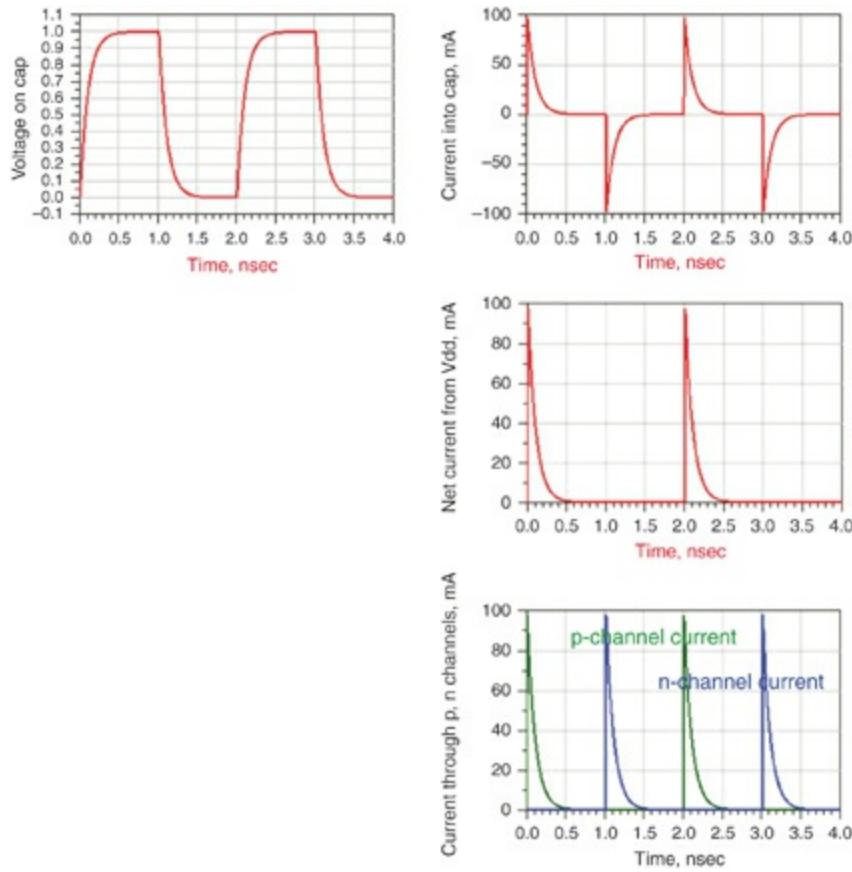


**Figure 9.3** Charging and discharging current flow patterns for the output capacitance occur on the rising and falling edges of the output node voltage.

When the output load is referenced only to the Vss rail, the PDN current only flows between the Vdd and Vss on the charging cycle, not during the discharging cycle, and it flows on the rising voltage transition. The charging current profile has a fast rise corresponding to the turn on time of the gate and the RC charging time constant to charge the capacitive load. In this case the R is the channel's on-resistance and the C is the output load capacitance.

For example, if the on-resistance is  $10 \Omega$  and the

output load capacitance is 1 pF, this is a 10 psec charging time. This time is very short compared to a clock cycle. The net PDN current flow from the Vdd to Vss rails is a pulse train, occurring once per clock cycle. Figure 9.4 illustrates the important features of the voltage waveforms on the output capacitor node, the current flowing into it in the positive direction, the current flowing out of it in the negative direction, the net PDN current from the Vdd rail to the Vss rail, and the alternating currents through the p-channel and n-channel.



**Figure 9.4** **Top row:** Voltage on the interconnect capacitor and current into the capacitor when it is referenced to Vss only. **Middle:** Net PDN current from Vdd to Vss, happening once per clock cycle. **Bottom:** The current through each of the transistor channels.

The charging current when the output node transitions from low-to-high comes from the Vdd source and flows through to the Vss node as displacement current through the capacitor. This is a transient current

through the Vdd-Vss power rail and is often referred to as the **PDN loop current**. The charge that flows into the capacitor results in a PDN transient current pulse occurring at the clock transition. The total charge stored on the capacitor that flows during charging or discharging is the area under the current waveform, and derive it with

$$Q_{\text{clk\_edge}} = \int_0^T I_{\text{clk\_edge}}(t) dt = C \times V_{\text{dd}} \quad (9.8)$$

where

$Q_{\text{clk\_edge}}$  = total charge that flows in during the edge of one clock cycle to charge up the load capacitor

$I_{\text{clk\_edge}}$  = the current that flows from Vdd during a clock edge

$T$  = the time for one period, which contains one pulse

$C$  = the interconnect capacitance and capacitance of the next gate

$V_{\text{dd}}$  = the core voltage supply

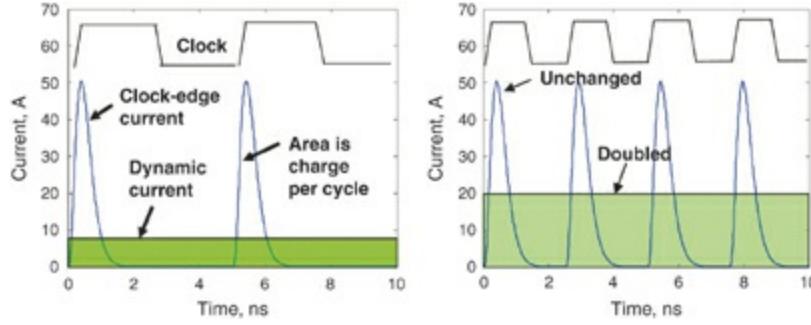
Because the current pulse begins only at the clock edge, it is referred to as the **clock-edge current** [3][4]. The clock edge triggers the clock-edge current.

The clock-edge current profile in each clock cycle is independent of the clock frequency. It only flows after the rising edge of the clock, which is usually when most of the gate activity happens, just after data is released by a latch. The average current over one cycle (also called the dynamic current) flows through the Vdd rail into the p-channel through the capacitor and into the Vss rail and is this total charge over one clock period:

$$I_{\text{dynamic}} = \frac{Q_{\text{clk-edge}}}{T} \quad (9.9)$$

If the clock frequency doubles, each clock-edge

current pulse stays the same; they just occur twice as often and the average or dynamic current doubles, as shown in Figure 9.5.



**Figure 9.5** Example of the clock-edge current and the dynamic current when the clock frequency is doubled.

This is the source of the dynamic current that draws power from the Vdd rail and initiates the transient PDN current consumed by the chip. It flows through the rest of the PDN network and ultimately consumes power from the VRM. The total dynamic current through the Vdd-Vss rails depends on the number of on-die gates that switch, the total capacitance charging and discharging, and the changes in each clock cycle as different logic functions are performed.

The on-die decoupling capacitance filters the clock-edge current spikes and smooths them out. The current that flows through the package bumps looks more like the dynamic current waveform, which has been averaged over a clock cycle.

**Tip**

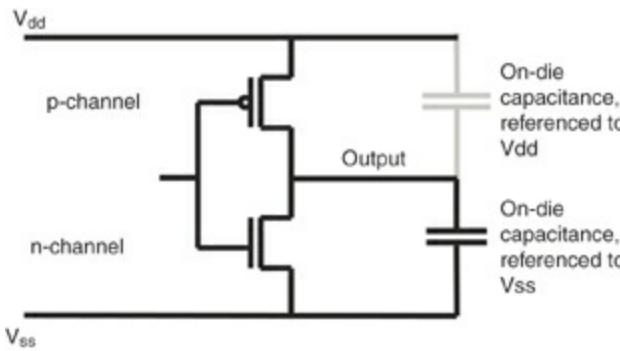
The clock-edge charge pulses are smoothed out by the on-die capacitance to look like the averaged clock-edge current by the time the PDN current flows through the package leads into the board PDN.

In general, the PDN current draw from the die is related to the modulation of the capacitive load due to different gates switching each clock cycle and

modulation of the clock frequency in cases where the clock is manipulated to speed up, slow down, or even stop to save power. We approximate these behaviors with a modulated transient current profile of the PDN current.

## 9.5 CLOCK-EDGE CURRENT WHEN CAPACITANCE IS REFERENCED TO BOTH VSS AND VDD

Interconnect capacitance is typically referenced to both the Vss and Vdd rails on-die. The on-die gate-to-gate interconnects might be sandwiched between Vdd and Vss metal layers. Due to the probability of high and low states of the output, wires on adjacent signals, and the next gate's input gate capacitance, the load capacitance is referenced to both rails. There is often symmetry between the Vdd and Vss power structures on-die and interconnect capacitance to Vdd is just as likely as to Vss. Load capacitance to Vdd is approximately equal to load capacitance to Vss, as shown in Figure 9.6.



**Figure 9.6** Equivalent circuit model of the load capacitance when the output capacitance is referenced to both the Vss and the Vdd rail. This is the usual case.

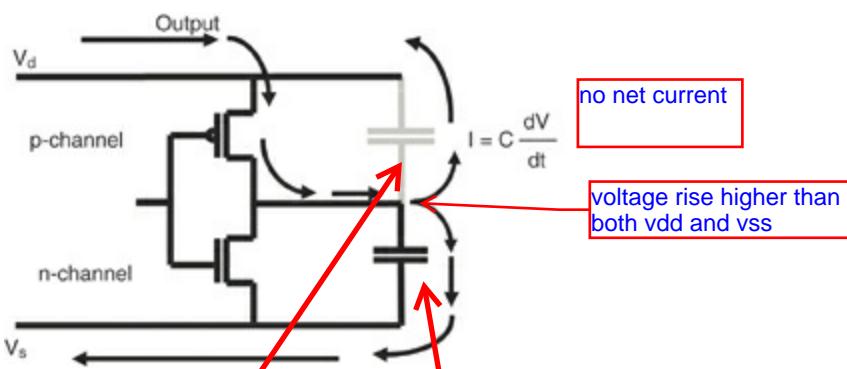
The charging and discharging current flow for the rising and falling transitions of the output node are slightly different compared to the single capacitor to Vss case. When the p-channel turns on and current flows into the output load capacitance, the Vss capacitor charges up and the Vdd capacitor discharges. The initial

PDN loop current's magnitude is the same as with a single reference because it is limited by the p-channel's on-resistance. Because the load capacitance has doubled, the RC time constant to charge up the capacitance has increased and the total integrated charge that flows into the output load through the p-channel has doubled, assuming the capacitance to the Vdd rail is the same as to the Vss rail.

When the rising transition current hits the output capacitor, the displacement current flowing through the capacitor, driven by the  $C^*dV/dt$ , splits. Half flows to the Vss rail, the same amount as in the case of single-ended referenced output capacitance, and half flows up to the Vdd rail. The output node's increasing voltage relative to both rails drives this displacement current. The DC voltage across a capacitor is not what drives the displacement current through it but the change in voltage,  $dV/dt$ .

In a low-to-high transition, the capacitor coupled to the Vdd rail is effectively “discharged” by the p-channel transistor. The charge across this capacitor flows through the p-channel and no net current flows through the PDN to discharge this capacitor. The net PDN current charges up the Vss referenced capacitor.

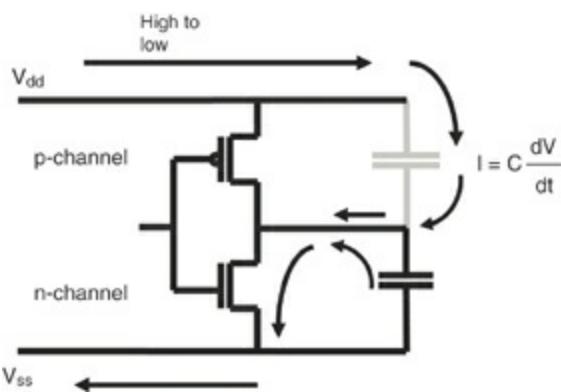
Figure 9.7 shows these charging and discharging current flows associated with the rising transition.



**Figure 9.7** Rising, low-to-high transition current flows into the output load capacitance when it is referenced to both the V<sub>ss</sub> and V<sub>dd</sub> nodes. PDN current flows during the low-to-high transition.

While the entire rising transition current flows out of the Vdd node through the p-channel, half of it flows back up to the Vdd node through the capacitive load to the Vdd node. The net result is that **half the charging current**, the fraction that flows to the **Vss node**, **flows through the PDN loop**. This is half the switching current and half the total integrated charge over one cycle.

When the p-channel turns off and the n-channel turns on in a **high-to-low transition**, the load capacitance discharges through the n-channel. Because the voltage on the output node is decreasing, the  $dV/dt$  is in the opposite direction as the charging cycle and displacement current flows through the Vdd capacitance to the output node and through the n-channel to Vss. This results in a **net current flow from the Vdd rail to the Vss rail** and is part of the PDN loop transient current; see Figure 9.8.



**Figure 9.8** Falling, high-to-low transition current flows from the output load capacitance when it is referenced to both the  $V_{ss}$  and  $V_{dd}$  nodes. PDN current flows during the high-to-low transition.

When the output gate capacitance is referenced to both the  $V_{ss}$  and  $V_{dd}$  rails, a net current flow exists between the  $V_{dd}$  and  $V_{ss}$  rails during both the rising and falling gate transitions. This means a current pulse initiated by a clock edge flows around the PDN loop during both the rising and the falling gate transitions.

The p-channel and n-channel currents are twice the PDN loop current due to energy stored in the capacitors during each half-cycle and dissipated in the FETs as the voltage transitions.

This is true for the clock tree. PDN current is drawn on both the rising and falling edge of the clock. This draws current impulses at twice the clock frequency.

However, the situation for combinational logic is a little different. Latches on the rising edge of the clock release data. PDN current is consumed as all the logic circuits come to their final states no matter which direction the gates switch. The combinational logic does not activate again until the rising edge of the next clock cycle.

#### Tip

Logic gates draw PDN current once per clock cycle and the clock tree draws current twice per clock cycle.

If the capacitive coupling between the output metallization and the Vdd rail is different from the capacitive coupling to the Vss rail, a different current flows on the rising or falling edges from Vdd to Vss. Wires in the wiring channels are more likely to be next to the output wires of other gates and have an equal probability of being high or low. A probability also exists that the neighboring wires are switching one direction or the other. In the end, the cumulative capacitive load for all the gate outputs balances between Vdd and Vss.

**Tip**

The rail-to-rail current flows around the PDN loop and contributes to the dynamic current consumed, creating a noise voltage across the PDN's impedance.

This example represents the current drawn from the PDN during clock and data activity. The clock tree is often an “H” fan-out of several stages of buffers and inverters. The clock edge propagates through the inverter fanouts until it reaches the final stage of the clock tree and latches where it releases data to propagate through the combinational logic. Assuming that all logic paths meet timing requirements, all clock-edge activity completes before the next clock edge. This activity involves many output nodes making transitions, either rising or falling. Current is consumed from the PDN on both rising and falling transitions of the output nodes for each clock-edge event.

## **9.6 MEASUREMENT EXAMPLE: EMBEDDED CONTROLLER PROCESSOR**

We can measure clock-edge currents indirectly when they generate a voltage drop on the die rails as the current passes through the PDN impedance. To illustrate this principle, we configured a simple

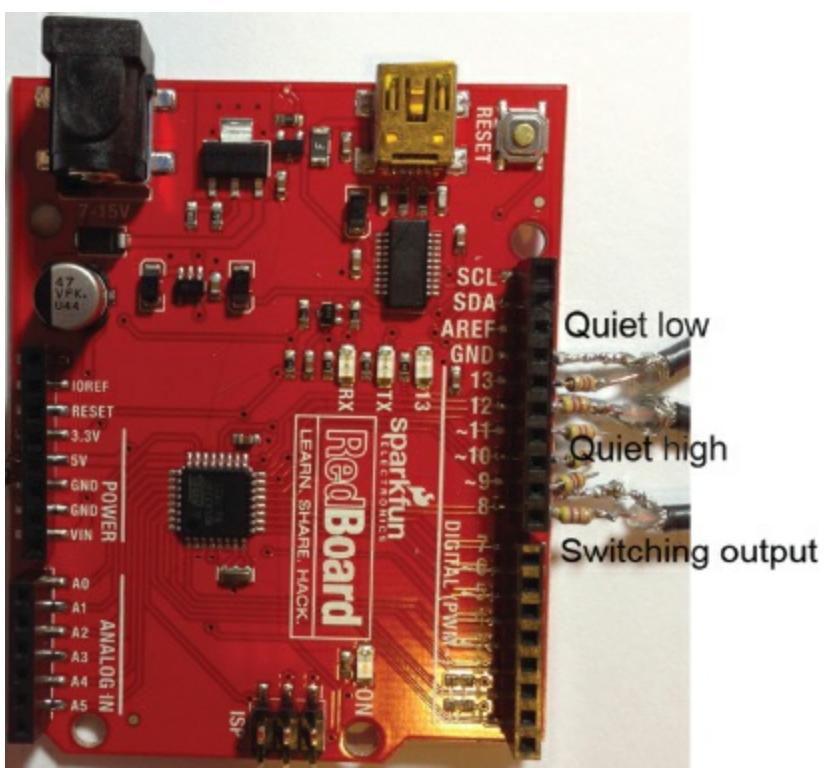
embedded controller processor, with a single, common 5 V power rail for both the core and I/O to measure the voltage on the Vdd and Vss rails.

We set one output pin at a constant HIGH value. This means we connected its output to the Vdd rail on the die. We set another output pin at a constant LOW. This means we connected its output pin to the Vss rail on the die. We connected these output pins through a  $450\ \Omega$  resistor and then through a  $50\ \Omega$  coax into a  $50\ \Omega$  scope input.

The voltage measured by the scope on the HIGH line is a replication of the on-die Vdd waveform. It has been divided down by the driver resistance, output net resistance, the  $450$  resistor, and the  $50\ \Omega$  termination on the scope. We observed the waveform launched into the coax cable connected to a signal trace and board ground on the scope.

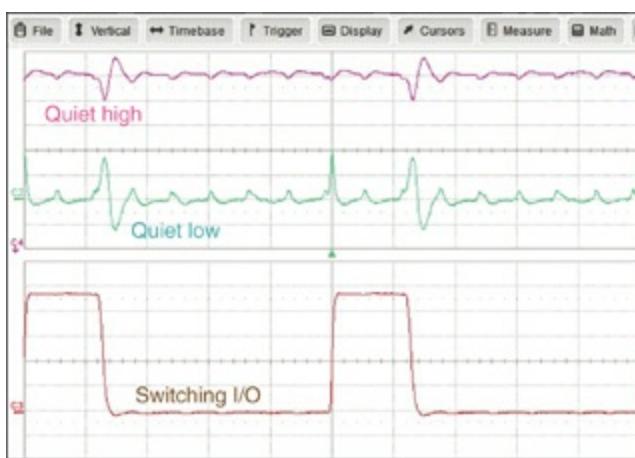
The voltage measured by the scope on the LOW line was the voltage difference between the local Vss rail on the die and the local ground where the coax cable was connected.

We programmed a third output pin to toggle off and on as quickly as possible. Its output also went through a  $450\ \Omega$  resistor to a coax cable and then into the scope's third channel. Using the  $450\ \Omega$  resistors cuts the current draw through the I/O pins to only  $5v/500\ \Omega = 10\ mA$ . Figure 9.9 shows a close-up of the embedded controller with the resistors and coax cables connected.



**Figure 9.9** Embedded controller (an Arduino microcontroller) instrumented to measure the on-die Vdd and Vss rails using quiet LOW and quiet HIGH sense lines as the I/O bank switches.

We measured the voltage noise with a Teledyne LeCroy HDO 12-bit resolution scope. The clock rate for this embedded controller was only 16 MHz, determined by an on-board crystal. This is a period of 60 nsec, a very long time compared to the 3 nsec rise time of the signals coming off the driver pins. The microcode running on the microcontroller kept the I/O voltage on the switching pin LOW for three clock cycles and HIGH for one clock cycle. Figure 9.10 shows the waveform for the three signals.



**Figure 9.10** Measured scope traces of the three signals.

**Top trace:** Output of one line pegged HIGH. This is the voltage on the Vdd rail. The scale is 100 mV per division.

The Vdd rail was 5 V. **Middle:** The output pin pegged LOW. This is the voltage on the Vss rail on the die, relative to the local board ground where the coax cable connected. The scale is 100 mV/div. **Bottom:** The I/O pin switching. The vertical scale is 1 V/div. The time base for all the traces is 50 nsec/div.

During the three clock cycles when the output is low, or the one clock cycle during which the output is high, the clock-edge current, which switches through the PDN loop on both the rising clock edge and falling clock edge, is apparent. As the Vdd current flows through the PDN and package lead inductance, the Vdd rail on-die collapses by about 20 mV. The same return current through the ground lead inductance generates a positive voltage on the Vss rail of magnitude 35 mV on each clock edge.

The rail compression from the clock-edge current occurs at twice the clock frequency, happening on each clock edge. This is due to a combination of load capacitance referenced to both Vdd and Vss and comparable gate activity in the clock distribution tree switching on both the rising and falling edge of the clock while the chip activity is near idle state.

When more gate activity occurs, such as when the I/O latches are set up at output drivers on the rising edge of

the clock, there is more PDN current switching and a larger rail collapse. The asymmetry in rail collapse between the output pin's rising and falling edges might be related to the different combinational logic activity that is switched on the two clock-edge cycles. Or the asymmetry might be related to the way that output nets are referenced to return paths in the traditional simultaneous switch noise (SSN) problem.

**Tip**

Although the clock distribution network creates clock-edge current on both the rising and falling clock edges, the logic switching creates clock-edge current only on the rising edge of the clock.

The specific amount of current flow either looping through the on-die PDN or just flowing through the Vss rail depends on the details of the on-die capacitance and which gates are switching or latched on each clock edge. This example illustrates that current only flows through the PDN on the clock edges. This signature is the most important feature of the current through the on-die PDN rails.

Regardless of whether the output capacitance is referenced to just the Vss rail or both the Vss and Vdd rail, a train of current pulses is coincident with the clock. This results in an average current over one clock cycle, which we refer to as dynamic current. It is related to the clock frequency and the total on-die load capacitance that is charged and discharged each cycle.

The dynamic current through the PDN is the averaged clock-edge currents over one cycle, as follows:

$$I_{\text{dynamic}} = \frac{\text{charge per clock edge}}{\text{period of clock cycle}} = \frac{Q_{\text{clk-edge}}}{T} = Q_{\text{clk-edge}} \times f_{\text{clock}} \quad (9.10)$$

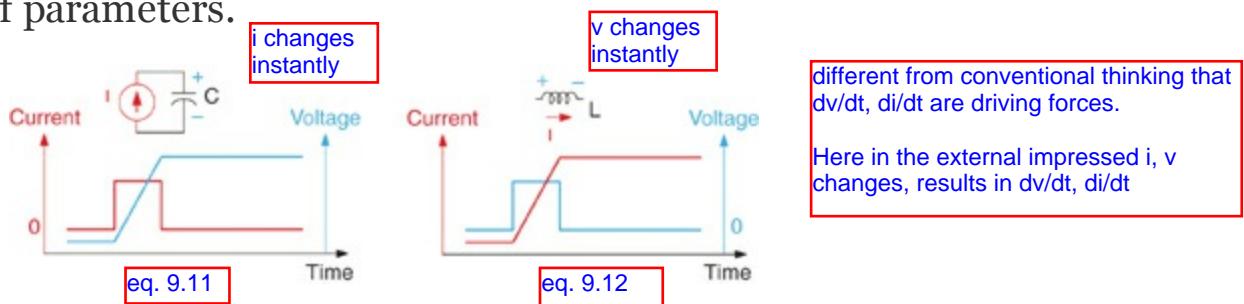
**Tip**

Ultimately, The patterns in the dynamic current, as a result of the gate activity and microcode running, is what creates the current profiles and contributes to the transient current.

## 9.7 THE REAL ORIGIN OF PDN NOISE—HOW CLOCK-EDGE CURRENT DRIVES PDN NOISE

When clock-edge current flows, as gates switch into capacitive loads, the voltage across the on-die capacitor drops with every clock-edge event. This creates a voltage across the PDN inductor, drives a  $di/dt$  through the inductor, and current comes in from the outside world to replenish the charge consumed by the clock edge. The sequence of events is confusing, yet important to understand the real mechanism of noise generation on the PDN.

We begin by reviewing the current and voltage relationships for a capacitor and inductor as shown in Figure 9.11. In a capacitor, a relationship exists between the change in charge stored on the capacitor and the change in voltage across it. In an inductor, a relationship exists between the change in voltage across it and the change in current through it. These relationships describe the instantaneous connection between the pairs of parameters.



**Figure 9.11** Voltage and current relationships for a capacitor and inductor.  $i/C$  and  $v/L$  are the forcing functions that cause voltage to change across a capacitor and current to change through an inductor.

Does a changing charge stored on a capacitor cause a voltage drop or does a voltage drop cause a change in

charge stored? Does a changing current through an inductor cause a voltage drop or does a voltage drop across an inductor cause a changing current?

Which is the cause and which is the effect is situational. Just as when we ask, “Is the glass half-full or half-empty?” the answer is, “It depends.” If we are filling the glass, the glass is half-full. If we are emptying the glass, the glass is half-empty.

**Tip**

If a capacitor is in a circuit where the charge is drawn off, the voltage across it will change. If an inductor is in a circuit where the voltage across it changes, the current through it will change.

The current entering or exiting a **capacitor** can change instantaneously; that is, in square wave fashion. The voltage across the capacitor can only change gradually according to the current integrated through it. The governing equations for a capacitor are

$$\frac{dv}{dt} = \frac{i}{C} \quad \text{and} \quad v = \frac{1}{C} \int i \times dt \quad \begin{array}{l} i \text{ is really } i(t) \\ \boxed{\phantom{v}} \end{array} \quad (9.11)$$

For an **inductor**, the roles of voltage and current reverse. The voltage across the inductor can change instantaneously but the current through an inductor can only change gradually according to the voltage across it.

The governing equations are

$$\frac{di}{dt} = \frac{v}{L} \quad \text{and} \quad i = \frac{1}{L} \int v \, dt \quad \begin{array}{l} v \text{ is really } v(t) \\ \boxed{\phantom{i}} \end{array} \quad (9.12)$$

applies when  $\Delta v$  is instant, while  $\Delta i$  is gradual. For example, when ODC charge depletes.

Here, the terms  $i/C$  and  $v/L$  are the **forcing functions** that cause voltage to change across a capacitor and current to change through an inductor, respectively.

As shown in Figure 9.11, the **current** into the capacitor is zero for a long time, **instantaneously goes up to a constant value** and then drops back down to zero. The

voltage across the capacitor is constant during time periods where there is no current. When a constant current into the capacitor exists, the voltage rises gradually. If  $i/C$  is the forcing function, the changing voltage,  $dv/dt$ , is the result.

We can most easily see this in the form of this equation as

$$i = \frac{dQ}{dt} = C \frac{dv}{dt} \quad \text{and} \quad \Delta Q = C \Delta V \quad \text{or} \quad \boxed{\Delta V = \frac{\Delta Q}{C}} \quad (9.13)$$

for caps, charge depletes will decrease E field strength & voltage (an integration of E field).

So both charge, E-field, voltage drop gradually for caps

In the case of the CMOS PDN, where **on-die capacitance (ODC)** occurs naturally around the load circuits, **charge depletion of the ODC is the cause of the voltage drop**. **Multiple gates switching draw charge from the ODC, causing its voltage to drop**. Charge is consumed with each clock cycle and removed from the on-die capacitance C.

**Step 1**

This is the root cause of PDN noise. We have the proverbial two capacitances **at different voltages** and a switch that closes instantaneously to try to bring both capacitances to the same voltage. An **impulse of current (charge) flows between the ODC and the load capacitance** as fast as the FET transconductance and wiring resistance will allow, thus **creating PDN noise**. From the preceding equations, the most obvious ways to **reduce PDN noise,  $\Delta V$ , is to increase the ODC or reduce the charge consumed by the load capacitance**.

**Step 2**

**Step 3**

#### Tip

The fundamental root cause of PDN noise is charge consumed when gates switch and charge up capacitive loads, consuming charge from the on-die decoupling capacitance. The most effective way to reduce PDN noise is to increase the ODC capacitance so that the voltage drop noise, which drives the rest of the PDN noise, is reduced.

This makes the role of on-die capacitance important

for CMOS PDNs.

The ODC protects the core logic circuits from external voltage noise on the Vdd supply. The voltage across the on-die circuit terminals does not change unless some noise current is integrated through the ODC. To get on die, the external noise on the Vdd rail, relative to the Vss rail, has to get through the package leads' high impedance and then it sees the ODC's low impedance. This voltage divider filters out system noise from appearing across the on-die circuits. This means PDN noise is usually a result of self-aggression where circuits consume charge from the ODC. External circuits, on the far side of package inductance, might generate noise by coupling into the loop inductance but the best way to protect against it is with strong on-die capacitance.

The first step in generating PDN voltage noise is with the **charge consumption in gates**. This **drives a voltage drop on the on-die PDN rail**. This **voltage-difference** on the package lead's **die side**, compared to the package lead's **board side**, is what drives the changing current through the inductor.of pkge lead

charge consumed in gates ==> \del V, i.e.,  
on die PDN rail drop ==> rail drop across  
pkge inductor ==> di/dt in package

#### Tip

This perspective, that a voltage drop across the ODC from charge depletion in charging up on-die circuitry is what drives the  $di/dt$  through the package lead, is contrary to the way we typically learn about inductance. In the case of on-die PDN noise, the forcing function is the voltage drop across the package lead inductance, and the response is a  $di/dt$  through the package lead.

In Figure 9.11, the current through the inductor is constant during time periods where zero voltage is across it. When a voltage difference exists across the inductor, the current rises. The **forcing function to change the current in the inductor is the  $v/L$  and the  $di/dt$  is the result**.

voltage diff. can be instant across L  
But, voltage on pkge lead die end drops gradually

We most easily see this in the integral equation. The

time integral of voltage across the inductor causes a 9.12  
change in current. For the simple PDN circuit, the  
voltage across the on-die capacitance must fall and  
cause a voltage drop across the inductor before current  
will come in through the inductor from the outside  
world.

There must be some PDN voltage noise (voltage drop  
across the on-die capacitor) to stimulate additional  
current to come in from the external power source. The  
ratio of v/L determines how fast current comes in from 9.12  
the outside world to replenish the charge consumed  
from the on-die capacitor by the CMOS circuits. A larger  
**voltage droop** across the ODC,  $\Delta V$ , causes a larger  
voltage drop across the inductor and creates a larger  
 $di/dt$  (current comes in faster).

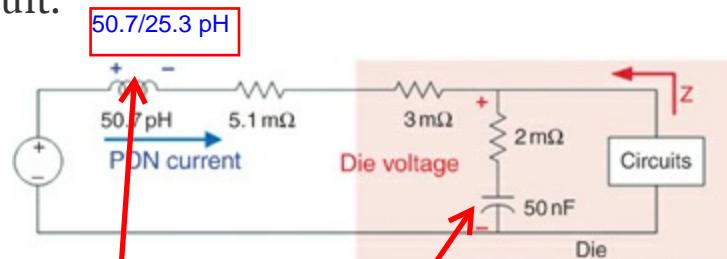
In the same way, a **smaller inductor value L** with the  
same capacitor voltage droop causes a larger  $di/dt$  and  
brings current in faster to replenish the on-die capacitor  
voltage faster. Larger voltage droops are not good for the  
CMOS circuits and will usually cause  $F_{max}$  degradation.  
Reducing the PDN loop inductance to bring current in  
faster is much better, but of course, this implies a more  
expensive PDN.

The preceding discussion provides much insight into  
the PDN mechanism for drawing current in CMOS  
circuits. The nature of CMOS PDNs is simply that the  
voltage across the ODC must droop before we can get  
more package current. We must always leave some  
tolerance for on-die circuit voltage to droop. This is the  
same tolerance that we use in the target impedance  
calculation. The die will not get any additional current  
from the outside world until the voltage droops. The  
rate at which current can possibly increase ( $di/dt$ , slope)  
from the package inductance is equal to  $v/L$ . Lower  
inductance is always better because it brings current in

to the aid of the voltage droop faster.

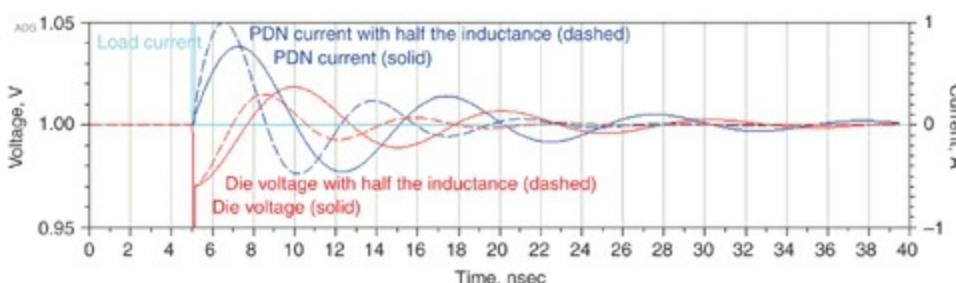
To illustrate these principles, we constructed a simple circuit, as shown in [Figure 9.12](#). The block labeled “circuits” is the switched capacitor network, which, once triggered, causes a single clock edge of total charge or an impulse of clock-edge current to flow. This decreases the voltage across the ODC capacitor, causing a voltage drop across the inductor, which drives a  $di/dt$  through the circuit.

full physical process of PDN noise source



**Figure 9.12** Circuit to illustrate the timing sequence of events in generating PDN noise on the die and the role the ODC and package lead inductance plays.

We simulated the voltage across the ODC and the resulting current through the inductance with an impulse of current corresponding to a single clock-edge current. [Figure 9.13](#) shows the effect of cutting the inductance value in half. The solid curves show the current and voltage for a 50.7 pH inductance and the dashed curves show results with 25.3 pH inductance. In this case the load current was a clock-edge impulse with the time width reduced to just 100 psec to enhance the effects. The impulse of current is much higher than the PDN current and is off scale on this plot.



**Figure 9.13** Simulating the voltage across the ODC and current through the inductor from the single clock-edge current when we cut the inductance value in half. This plot shows the voltage across the ODC as the initial downward droop and the current through the inductor as the upward sine waves.

When the clock-edge impulse current flows, the on-die capacitance voltage immediately drops 31 mV, which is a consequence of  $\Delta V = \Delta Q/C$ . During the short time duration of the load current an additional voltage drop occurs because of the  $2 \text{ m}\Omega$  resistance in series with the on-die capacitance.

With reduced inductance, the current curve's slope is larger ( $2 \times di/dt$ ). The initial voltage sags on the ODC are the same because any reasonably sized inductor is not capable of delivering current during the short duration current impulse. However, in the first few nsecs after the event, clearly the current ramps up faster and voltage reverberations reduce when we cut the inductance in half. The resonant frequency has been increased by 25% (frequency goes as the square root of inductance) and the q-factor has been reduced (the number of ringing cycles has been reduced).

initial vdroop is same regardless of pkge L, since pkge L is not able to supply current/charge yet

The question of what is the cause and what is the effect in PDN elements is confusing because the perspective depends on the source of the driving function.

In I/O circuits, as distinct from core logic circuits, where signals are switching large, off-die currents, the driving function for noise on the external power rails is

the  $di/dt$  of the switching current and the loop mutual inductance between aggressive I/O loops and quiet I/O loops. The response is the induced voltage noise generated on the quiet loops.

inductive coupling,

Not capacitive coupling, which caused by  $dV/dt$

What is commonly referred to as **ground bounce** is really the inductively coupled cross talk between I/O loop inductances. How we assign the distributed loop inductances into specific total inductances of parts of the loop is up to us, depending on the question we are trying to ask.

In one approach, when there are shared return leads, we can assign the loop inductance of the signal-return loop as a total inductance in the return path. When the aggressor signal loop switches, a  $di/dt$  flows through the aggressor circuit, through the shared total inductance of the return path. This  $di/dt$  acts as the forcing function and generates a voltage drop across the common return inductance.

noise source is  $di/dt$   
==> generates  $\Delta V$

This is one way, but not the only way of thinking about the origin of ground bounce.

This example is another case where the term *power integrity* encompasses two very different problems with different root causes and solutions. Although it is lumped under the general heading of power integrity, reducing switching noise in the I/O paths is a separate problem from reducing voltage noise on the Vdd rail of core logic.

When core logic switches, the **small signal  $di/dt$** , which is the slope of current on time axis, is not the cause of PDN noise but rather **the result of  $v/L$** .

**Tip**

When resupplying the charge on the ODC, we want the  $di/dt$  to be as high as possible to reduce the voltage noise on the ODC. A smaller package lead inductance allows a larger  $di/dt$  and reduces the on-die rail noise.

The big enemy of PDN performance is the transient current that results from the switched capacitive load on the die and the sequence of clock edges and charge consumed per edge. This is the large signal,  $dI$ , the maximum current minus the minimum current. The transient current is closely related to the energy or power that the PDN must deliver. The rise time of the transient current,  $dT$ , determines the portion of the PDN that must deliver the  $dI$ . Very fast transient currents (that is, sudden string of clock-edge impulses) must be delivered from the on-die capacitance.

The package inductance prevents current from coming from the package during a fast clock cycle period. If the large signal  $dT$  is a little longer and happens over several clock cycles, the transient current is delivered from the on-package capacitor. If the  $dT$  is longer yet, the transient current may be delivered from the board capacitors in several tens of clock cycles or from the VRM in several hundreds of clock cycles.

**Tip**

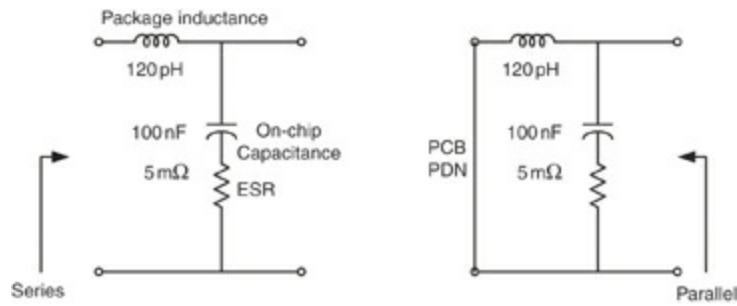
The amount of large signal transient current,  $dI$ , is the quantity we use in the target impedance calculation. The length of time  $dT$  simply determines where in the PDN it comes from.

## 9.8 EQUATIONS THAT GOVERN A PDN IMPEDANCE PEAK

Before evaluating the voltage signatures on the PDN from the various dynamic current signatures, we set up a simple PDN case study with the important features

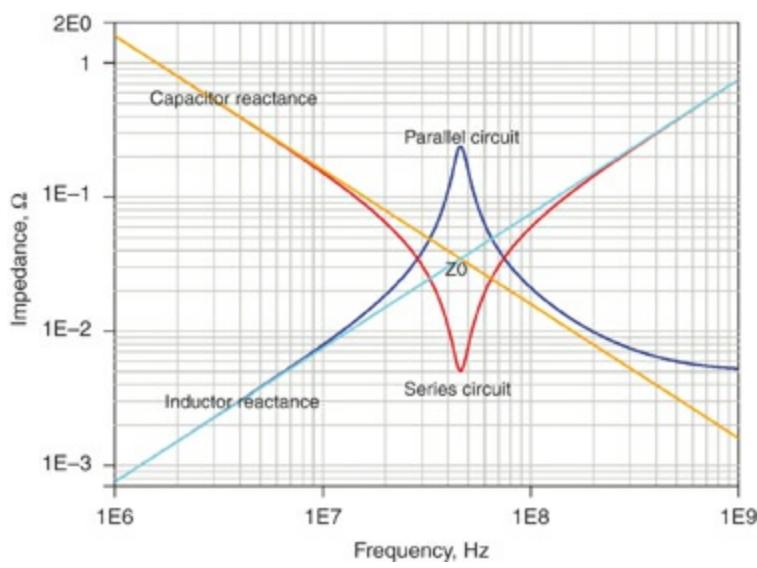
that affect the voltage behavior.

Figure 9.14 shows the typical RLC circuit representing the on-die capacitance and package lead inductance with some series damping resistance. When we view a capacitive die in an inductive package from the board side, the components are in series and a resonant dip in impedance is expected. When we view the RLC circuit from the die's perspective, and assuming that the package is attached to a low impedance board PDN, the components are in parallel and a resonant peak impedance is expected.



**Figure 9.14** Series and parallel circuits for a capacitive die in an inductive package with identical component values. When viewed from the board side, such as in a VNA measurement, the components are in series. When viewed from the perspective of the functioning circuits on-die, the components are in parallel. The PCB PDN is often a very low impedance and is represented by a short.

Figure 9.15 shows the impedance of the series and parallel circuits together with the impedance of the inductor alone and the capacitor alone.



**Figure 9.15** The impedance curves for series and parallel resonant circuits have the same resonant frequency. Note that the reactive components' impedances cross at the resonant frequency and with a value of the characteristic impedance of the circuit,  $Z_0$ .

Both circuits have the same resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (9.14)$$

The impedance of the inductor and capacitor crosses at the resonant frequency and is the same. Because this impedance value characterizes the resonance, we call it the characteristic impedance of the circuit  $Z_0$ . This impedance has nothing to do with a characteristic impedance of a transmission line. This impedance just “characterizes” this circuit.

The characteristic impedance of the resonant circuit is the reactance of either the inductance or capacitance at the resonant frequency. We calculate this from the impedance of the C or L at resonance:

$$Z_0 = 2\pi f_0 L \quad \text{or} \quad Z_0 = \frac{1}{2\pi f_0 C} \quad (9.15)$$

Applying the resonant frequency for an LC circuit, the characteristic impedance is

$$Z_0 = 2\pi f_0 L = 2\pi \frac{1}{2\pi\sqrt{LC}} L = \sqrt{\frac{L}{C}} \quad (9.16)$$

For the series resonance, the impedance bottoms out with a value of R and the q-factor is the reactance divided by the resistance at resonance:

$$\text{q-factor} = \frac{Z_0}{R} \quad (9.17)$$

By observation, the parallel impedance peak is as far above  $Z_0$  as the series impedance is below  $Z_0$ . We estimate the impedance peak from

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 = \frac{Z_0}{R} \times Z_0 = \frac{Z_0^2}{R} = \frac{1}{R} \frac{L}{C} \quad (9.18)$$

This equation is accurate when the q-factor is high but is not accurate when the q-factor is close to 1.

We can use these equations in several ways to form a basis for PDN design:

1. If we know the RLC values, we can calculate the resonant frequency, characteristic impedance, q-factor, and impedance peak height.
2. If we measure the resonant frequency and q-factor and the initial voltage dip to a known impulse current, we can calculate the RLC values.
3. If we desire certain impedance peak properties, we can engineer RLC values to obtain the desired properties.

For example, if the on-die capacitance is 50 nF and we desire an impedance peak of 100 mΩ at 100 MHz, we can engineer R and L values to obtain these values. A simple spreadsheet, further developed in [Chapter 10](#), calculates all the important features using the basic PDN properties from these circuit parameters. [Table 9.1](#) summarizes an example.

Frequency Domain		
Vdd	1	V
Core cap	50	nF
PDN loop inductance	50.7	pH
PDN loop resistance	10.1	mΩ
Resonant frequency	100	MHz
PDN $Z_0$	32	mΩ
q-factor from PDN loop	3.15	
Expected impedance peak	100	mΩ
Assumed die resistance	5.0	mΩ
External PDN loop resistance	5.1	mΩ

C

L

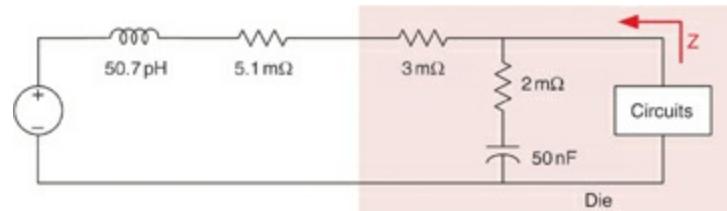
R

9.16

**Table 9.1** PDN parameters in the shaded portion determine the PDN properties, which are calculated with simple equations.

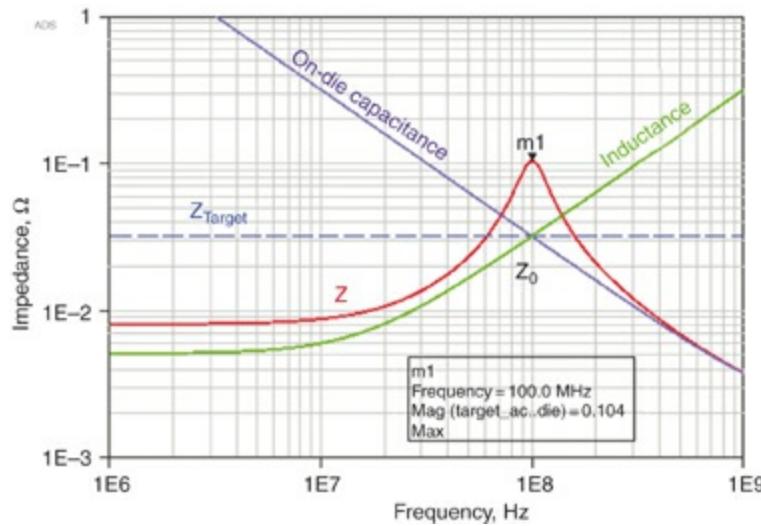
Starting with a typical on-die capacitance of 50 nF and using the earlier equations, we choose the other PDN parameters to achieve the desired impedance peak. We back calculate an inductance of 50.7 pH to deliver the desired resonant frequency of 100 MHz. We calculate the characteristic impedance,  $Z_0 = 32 \text{ m}\Omega$ , from the C and L values. To achieve the desired impedance peak of 100 mΩ, the q-factor must be 3.15. Working backwards from this and the calculated  $Z_0$ , the PDN loop resistance must be 10.1 mΩ.

Figure 9.16 shows a circuit diagram for this PDN. The PDN loop resistance has been arbitrarily broken up into a portion in series with the on-die capacitance and a portion in both inside and outside the package.



**Figure 9.16** PDN circuit schematic with circuit parameters that give the desired PDN properties: 100 mΩ peak impedance at 100 MHz.

Figure 9.17 shows the simulated impedance from the die pads' perspective. The impedance peak is at 100 MHz and nearly  $100 \text{ m}\Omega$  as expected. For this example, we wanted the target impedance to be the same impedance as the characteristic impedance,  $32 \text{ m}\Omega$ . As discussed in the next section, this enables us to demonstrate the properties of a PDN whose impedance peak exceeds the target impedance but has a  $Z_0$  characteristic impedance that meets the target impedance.



**Figure 9.17** ADS frequency domain simulation of the PDN. As predicted by simple equations, the impedance peak is at 100 MHz and nearly  $100 \text{ m}\Omega$ .

## 9.9 THE MOST IMPORTANT CURRENT WAVEFORMS THAT CHARACTERIZE THE PDN

We can extract or characterize all the important performance properties of the PDN from the PDN voltage response to three different transient current waveforms [4][5]:

- 1. Impulse:** A single clock-edge current, a fast impulse of current (charge, in very short time) associated with a single clock edge. A comparable signature is an anti-impulse, which is a single missing clock current impulse in a series of impulses.

**2. Step:** An abrupt turn-on of the dynamic current from a minimum value to the maximum value and holding steady at the high value. This type of current often happens when clocks are abruptly started or changed in frequency or when a processor pipeline abruptly restarts after data is recovered from a cache miss. Rise time might be as fast as the clock edge.

**3. Resonance:** Microcode causes step dynamic currents to occur over and over again at a PDN resonant frequency. The probability of this is low but the effects are devastating for the PDN that significantly exceeds the target impedance. It is modeled as a train of square waves with an amplitude of the transient current.

These current waveforms serve two purposes. When we know the PDN's RLC parameters, these current waveforms help us predict the expected PDN voltage noise under many conditions. This is a metric for the expected PDN noise.

In addition, if we can drive a PDN with these current waveforms and measure the PDN response, we can “reverse engineer” the properties of the PDN and extract fundamental figures of merit to build an accurate PDN model.

**Tip**

We use these three types of current waveforms to predict the PDN response or, from the measured response, “reverse engineer” the PDN equivalent circuit model.

We calculate time domain parameters for the PDN using the frequency domain parameters discussed in the previous section. Table 9.2 shows the input parameters and calculated results listed in the spreadsheet. We list

the equations that produce the expected results in the next three sections. For this study, we adjusted the dynamic current to force the target impedance to be the same as the characteristic impedance.

Time Domain		
Dynamic current	1.55	A
$f_{clock}$	1	GHz
Target impedance	32	$m\Omega$
Charge per clock cycle ( $Q_{cycle}$ )	1.55	nCoul
Expected clock-edge droop (impulse)	31	mV
Expected step response droop	49	mV
Expected peak-peak noise at resonance	198	mV

**Table 9.2** Time domain parameters to go with the frequency domain parameters listed in the case study set up. The shaded portion is inputs and the rest of the values are calculated. We calculate the expected clock edge and step response droops as well as the resonant p-p noise from closed-form equations.

Suppose we have a steady dynamic current of 1.55 A. Logic switching on the rising edge of the clock drives the dynamic current in this example. We know this if we see a (1.55 A) increase in the bench power supply current after turning on the clock. The transient current is the maximum current minus the minimum current and is 1.55 A in this example. The calculated target impedance for a  $\pm 5\%$  ripple is 32  $m\Omega$  when the Vdd is 1 V:

$$Z_{target} = \frac{Vdd \times \text{tolerance}}{I_{transient}} = \frac{1V \times 5\%}{1.55A} = 32 m\Omega \quad (9.19)$$

Because we chose 1.55 A, the target impedance reference line intersects the capacitive and inductive reactance curves right at the  $Z_0$  crossover point. We use these parameters to demonstrate the properties of a PDN whose characteristic impedance exactly meets the target impedance.

**Tip**

The simplest way of stimulating the single resonance PDN circuit is using a constant current source with three waveforms.

Although the actual load to a PDN does not behave exactly like a constant current source, this type of source is a simple starting place and can be implemented in all versions of SPICE simulators.

In the next sections, we demonstrate the PDN response to the impulse, step, and resonance current waveforms and show how the PDN features contribute to the features in the voltage response. In [section 9.17](#), we introduce a more sophisticated PDN load based on a train of pulses of clock-edge current, which are generated by switched capacitors. The general features of the PDN response to the switched capacitor load are the same as when using a constant current source.

## 9.10 PDN RESPONSE TO AN **IMPULSE** OF DYNAMIC CURRENT

For the simple case of a 1 GHz clock and 1.55 A of dynamic current, the average clock-edge charge per cycle is

$$Q_{\text{clk-edge}} = I_{\text{dynamic}} \times T = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} = \frac{1.55 \text{ A}}{1 \text{ GHz}} = 1.55 \text{ nC} \quad (9.20)$$

Given this average clock-edge charge flowing each clock cycle, we observe the PDN voltage response to this impulse of dynamic current. From the voltage responses we extract or “reverse engineer” the PDN features. A single clock-edge impulse is isolated in the lab by slowing down the 1 GHz clock to perhaps 10 MHz. The same impulse of charge is consumed in 1 nsec and the impulse response is observed in the quiet period before the next clock edge.

When this charge per clock cycle flows, it depletes the charge from the on-die capacitance, ODC. This results in

a voltage drop  $\Delta V$  on the ODC given by

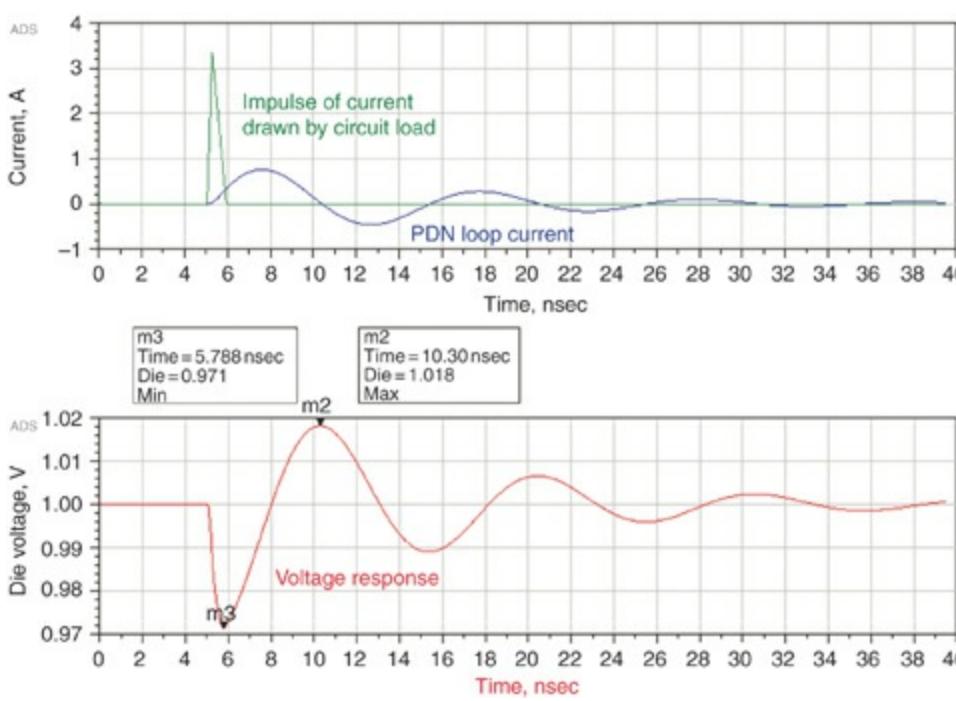
$$\Delta V = \frac{Q_{\text{clk-edge}}}{C_{\text{ODC}}} \quad (9.21)$$

We assume the time for this clock-edge current to flow is short compared with the PDN circuit's response time. In this case, all the charge comes from the ODC and results in the initial voltage drop. This initial voltage drop from a single impulse of dynamic current is the **clock-edge droop**. We expect the droop voltage response to a single clock edge of charge flow for the earlier PDN example to be

$$\Delta V_{\text{clock edge}} = \frac{Q_{\text{clk-edge}}}{C_{\text{ODC}}} = \frac{1}{C_{\text{ODC}}} \frac{I_{\text{dynamic}}}{f_{\text{clock}}} = \frac{1}{50 \text{nF}} \frac{1.55 \text{A}}{1 \text{GHz}} = 31 \text{mV} \quad (9.22)$$

After the initial impulse is drawn, we expect the PDN circuit to ring at the LC circuit's resonant frequency and to damp out with the q-factor as determined by the series resistance.

We used Keysight ADS to simulate the impulse response and obtain a voltage waveform to compare against the estimate based on the circuit model. Figure 9.18 shows the impulse response for the earlier simple PDN circuit. We constructed a current source with a triangle wave to consume 1.55 nCoul from the PDN in 1 nsec. This is the amount of average charge drawn after each rising clock edge when the dynamic current is 1.55 A and the on-die clock is running at 1 GHz.



after droop, why overshoot ?  
-- because current cannot stop instantly from pkge inductance.  
This is also a character of resonant circuit.

LC resonance ? what is time gap btw m2 & m3 ? Q factor ?

**Figure 9.18 Top:** An impulse of current drawn from the on-die capacitance through the Vdd to Vss rails and the resulting current flowing around external loop in the earlier simple PDN circuit. **Bottom:** Voltage response across the die pads from the single current impulse. Note the initial voltage dip is 29 mV, compared with the 31 mV predicted.

The current from the ODC is oscillating both below and above zero. This indicates that during some time periods, current is actually flowing out of the die and back into the external PDN. This is typical of resonant systems as energy moves back and forth between the inductor and the capacitor (magnetic field and electric field).

#### Tip

The impulse response reveals much about the PDN's properties. We get a measure of the on-die capacitance from the initial droop, the LC resonant frequency from the ringing frequency and the Q-factor from the number of cycles the ringing lasts.

Even though the current impulse only lasts for 1 nsec, the system rings out for 40 nsec. The voltage on the die pads shows the expected response of an RLC circuit. We

see the voltage and current ringing out for a long time (more than 40 nsec) after the initial 1 nsec impulse of load current. The period of the ringing reveals the PDN resonant frequency. With a period of about 10 nsec, we estimate the resonant frequency as 100 MHz, exactly the value engineered for this PDN.

The damping of the waveform reveals the q-factor. About three complete cycles of ringing are readily identifiable, which indicates a q-factor of about 3. We calculated the q-factor of the circuit in Table 9.1 as 3.15.

By simply examining a measured impulse response in the lab and using the on-die capacitance estimated from the depth of the droop or speculating about the inductance, we can calculate all other PDN parameters using equation 9.22.

The estimate in equation 9.23 predicted 31 mV of droop but only 29 mV was simulated. The difference is because a small amount of charge came into the die from the board-level supply during the impulse duration. In other words, the 1 nsec duration of impulse current was not quite insignificant compared to the 10 nsec period of the PDN resonant circuit.

**Tip**

The only way to mitigate the clock-edge droop is with on-die capacitance. No other design feature in the PDN has an impact reducing the initial clock-edge voltage droop.

Reduction of PDN loop inductance would have very little effect on the droop because the impulse event is over before the PDN loop current ramps up.

## **9.11 PDN RESPONSE TO A STEP CHANGE IN DYNAMIC CURRENT**

When the current source load on the die is a step change in current of magnitude  $I_o$ , the PDN voltage, as observed

on the die pads, responds with a damped sine wave of voltage with an offset based on the IR drop from the  $I_0$  constant current. This is the step response of a parallel RLC circuit.

The initial droop of the damped voltage sine wave response is

$$V_{\text{droop}} = Z_0 \times I_0 \quad (9.23)$$

The rest of the response is a damped sine wave with the LC circuit's frequency and the q-factor related to the damping resistance. If the step current is the same as the maximum transient current that defines the target impedance, then

$$I_0 = \frac{V_{\text{dd}} \times \text{ripple}}{Z_{\text{target}}} \quad (9.24)$$

and

$$V_{\text{droop}} = Z_0 \times I_0 = Z_0 \times \frac{V_{\text{dd}} \times \text{ripple}}{Z_{\text{target}}} = \frac{Z_0}{Z_{\text{target}}} (V_{\text{dd}} \times \text{ripple}) \quad (9.25)$$

For the PDN voltage amplitude response to a step current (consistent with the target impedance) to be less than the acceptable level of PDN voltage noise, we require

$$Z_0 < Z_{\text{target}} \quad (9.26)$$

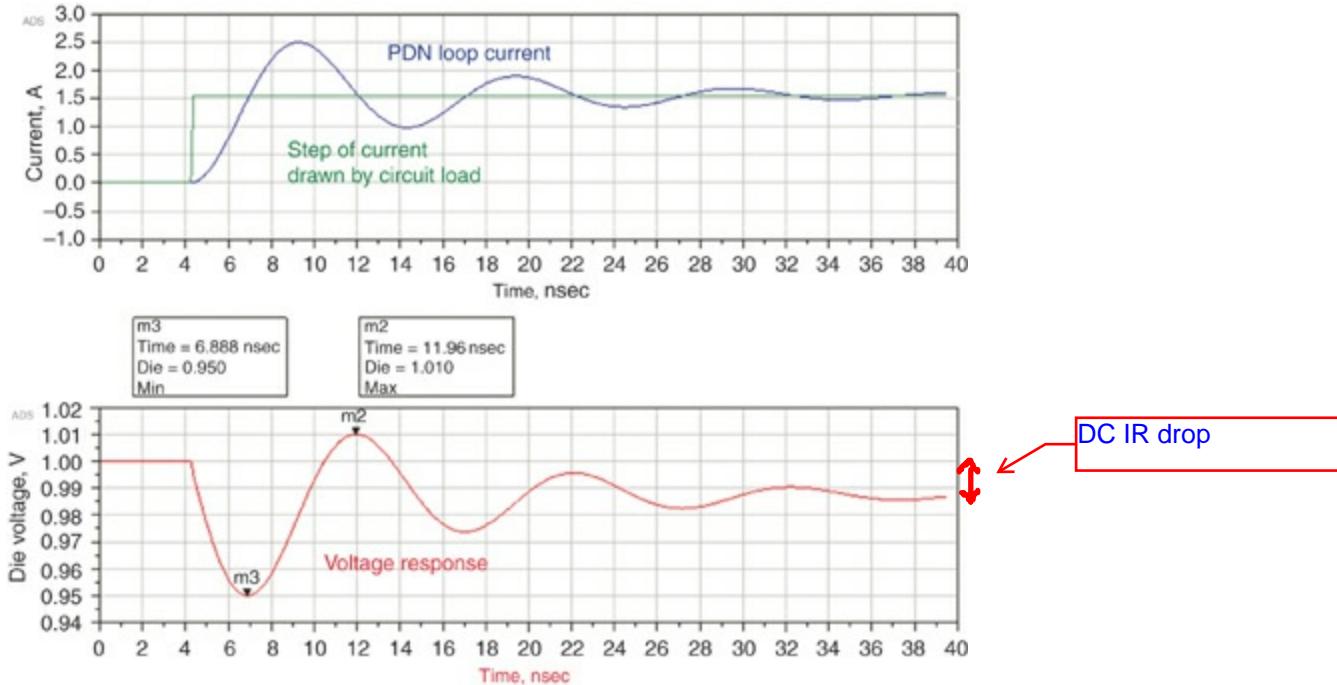
#### Tip

To keep the PDN voltage noise generated by the maximum step current within tolerance, we need the characteristic impedance of the PDN peaks to be less than the target impedance. This is an important design requirement for a marginally robust PDN.

If the characteristic impedance of the Bandini Mountain is higher than the target impedance, a maximum step current load will cause the initial droop

on the PDN to exceed the noise limits.

Figure 9.19 shows the simulation results for a step response of the simple PDN. A current source circuit load consumes a step of 1.55 A. Step currents often happen with clock gating, abrupt changes in clock frequency, and cache misses.



**Figure 9.19** The simple PDN circuit's response to a current step. A PDN where the characteristic impedance meets the target impedance has a step response droop approximately the same as the voltage tolerance used in the target impedance calculation, in this case 50 mV or 5% of 1 V.

Similar to the impulse response, the step current response has high-frequency content and causes the PDN to respond with a damped sinusoid. Evidence of the resonant frequency and q-factor is clearly visible. The major difference compared to the impulse response is the peak voltage droop and the final voltage value associated with DC current causing a DC IR voltage drop.

The simple equations above predict that the voltage droop from the step response is

$$V_{\text{step}} = I_{\text{step}} \times Z_0 = 1.55 \text{ A} \times 32 \text{ m}\Omega = 49 \text{ mV} \quad (9.27)$$

?? why 9.27 use  $I \times Z$ , but 9.22 use  $\Delta \text{el Q/C}$  ?

Zo is at only one freq, but current is not all at single freq, 9.27 could be problematic

The simulated droop is 50 mV, the difference coming from round off error. For this PDN, we engineered the target impedance to be the characteristic impedance by selecting the transient current as 1.55 A. The voltage droop is 5% down from 1 volt, consistent with the tolerance used in the target impedance calculation.

Because the voltage on the die in a step current response is the transient current times the characteristic impedance, as illustrated in this simulation, the maximum voltage droop exceeds the voltage tolerance when

$$Z_0 > Z_{\text{target}} \quad (9.28)$$

This criterion for the characteristic impedance of the Bandini Mountain peak to be less than the target impedance is specifically to keep the voltage droop from a transient step current response within the tolerance limit.

**Tip**

The step current response is a common occurrence and the condition for the **characteristic impedance to be below the target impedance is** an important ingredient to a marginally or reasonably robust PDN.

The only way to engineer less step response droop is to reduce the characteristic impedance of the resonance. We do this by either increasing the ODC capacitance or reducing the mounted package loop inductance, because the characteristic impedance is

$$Z_0 = \sqrt{\frac{L}{C}} \quad (9.29)$$

An alternative engineered solution is to add on-package decoupling capacitors. This reduces the effective lead inductance the ODC sees and reduces the

characteristic impedance of the dominant Bandini Mountain. Of course, it is essential the on-package capacitors have very low mounting inductance.

Having  $Z_0$  meet the target impedance is not the only criterion for a marginally robust PDN.

As we show in the next section, the PDN voltage noise resulting from the maximum current modulated at the resonant frequency is likely to exceed the voltage tolerance unless the peak impedance is below the target impedance.

## 9.12 PDN RESPONSE TO A **SQUARE WAVE** OF DYNAMIC CURRENT AT RESONANCE

In the third current waveform, the dynamic current is in the form of a square wave at the resonant frequency with a **peak-to-peak transient current**. The first harmonic of the square wave signal drives a peak voltage in the resonant circuit.

We calculate the peak-to-peak voltage noise based on the sine wave frequency component of the current at the first harmonic and the peak impedance. If the peak-to-peak current in the square wave is  $I_{\text{transient}}$ , the sine wave peak-to-peak current amplitude of the first harmonic,  $I_{\text{pk-pk}}$  is

$$I_{\text{pk-pk}} = \frac{4}{\pi} \times I_{\text{transient}} \quad (9.30)$$

As a result of the Fourier Transform, the first harmonic's peak-to-peak current is actually larger by the factor of  $4/\pi$  than the square wave's peak-to-peak value. The peak-to-peak voltage generated is this peak-to-peak current flowing through the peak impedance at the resonant frequency. At the resonant frequency, the peak impedance is

$$Z_{\text{peak}} = \text{q-factor} \times Z_0 \quad (9.31)$$

And the peak-to-peak voltage generated when the square wave of current drives the resonant frequency is

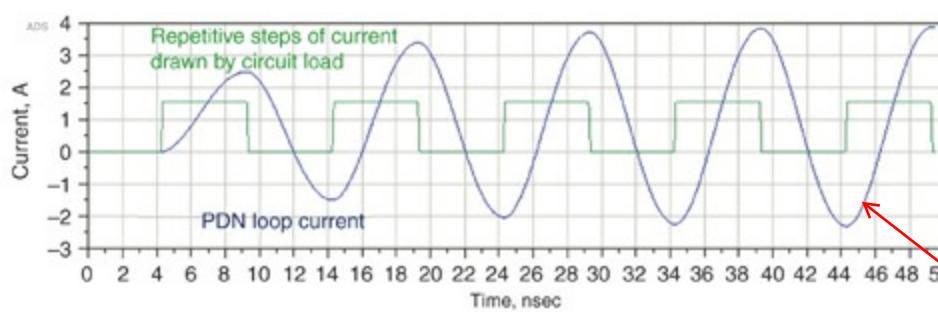
$$V_{\text{pk-pk}} = \frac{4}{\pi} I_{\text{pk-pk}} Z_{\text{peak}} = \frac{4}{\pi} I_{\text{transient}} \times \text{q-factor} \times Z_0 \quad (9.32)$$

To confirm these design principles, we simulate the resonant response of the PDN example above, which has a peak impedance of  $100 \text{ m}\Omega$ , by using the same  $1.55 \text{ A}$  peak-to-peak square wave of dynamic current as in the step response example. The periodic current steps are always in the positive direction and do not change with time. However, the PDN loop current, the current through the on-die capacitance, and package lead inductance builds up and increases with time.

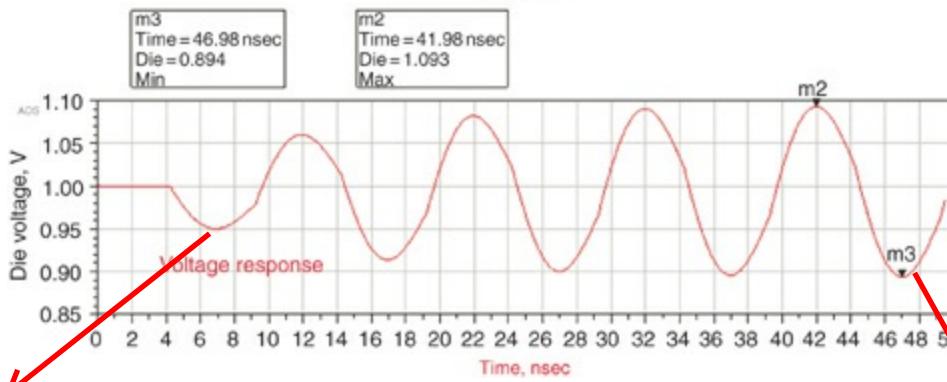
We expect the peak-to-peak PDN voltage response to the square wave of load current to be

$$V_{\text{pk-pk}} = \frac{4}{\pi} I_{\text{pk-pk}} Z_{\text{peak}} = \frac{4}{\pi} I_{\text{transient}} \times \text{q-factor} \times Z_0 = \frac{4}{\pi} 1.55 \text{ A} \times 100 \text{ m}\Omega = 198 \text{ mV} \quad (9.33)$$

Figure 9.20 shows the simulated resonance response of this PDN example with a  $1.55 \text{ A}$  peak-to-peak square wave of dynamic current.



cmp with step/impulse waveform, now PDN current is double sided, Pos - Neg = 1.55A



vdroop close to step response

magnify first vdroop by  $4/\pi$

**Figure 9.20** The simple PDN's resonance response. The PDN loop current is much higher than the current source that initiated the response. Energy from one cycle superimposes upon another cycle as magnetic energy and electric energy build up in the inductor and capacitor.

Each current step of the load is in phase with the current that is already flowing in the PDN loop. This grows the PDN loop current. Note that the PDN loop current ranges between 4 A out of the board and -2.5 A back into the board even though the circuit load is only consuming 1.55 A.

This phenomenon is common in resonant circuits. Energy transfers between the inductor and capacitor and builds up to levels higher than the stimulating current. For some periods of time, current is flowing out of the die back into the board that powers the system. Note that a one-sided transient current has caused a two-sided voltage response because of the resonant circuit. This is the major reason why the target impedance calculation involves a one-sided transient current even though there is a two-sided, plus and minus voltage tolerance.

same impedance profile applies to currents flow both directions

The time it takes the resonance to reach maximum

peaks is related to the q-factor. For a system with a q-factor of 3, it takes about three cycles to reach the maximum excursion. We saw this in the impulse response when it took about three cycles for the waveform to die out. The q-factor is an indication of how many cycles can possibly reinforce each other and superimpose energy from cycle to cycle.

**Tip**

The impedance peak's q-factor does not affect the step response initial droop; only the characteristic impedance of the resonant peak is what affects the step response.

In the simulation, the peak-to-peak voltage at resonance built up to 201 mV, very close to the 198 mV estimated prediction. This is because the actual impedance peak in simulation was slightly more than 100 mΩ calculated in the simple estimate.

**Tip**

The two ways to reduce the peak resonant voltage amplitude are to reduce the peak impedance by reducing the q-factor of the resonance and by reducing the peak's characteristic impedance. We do this by increasing the damping resistance and by reducing inductance or increasing the ODC.

The peak voltage noise is related to the q-factor and characteristic impedance of the resonant peak and the transient current. In this example, we selected the target impedance based on the transient current value and voltage tolerance:

$$I_{\text{transient}} = \frac{V_{\text{noise}}}{Z_{\text{target}}} \quad (9.34)$$

The peak-to-peak voltage noise is related to the impedance peak by

$$V_{pk-pk} = \frac{4}{\pi} I_{transient} \times Z_{peak} \quad (9.35)$$

From these relationships, the peak-to-peak noise is also related to

$$V_{pk-pk} = \frac{4}{\pi} \frac{V_{noise}}{Z_{target}} \times Z_{peak} \quad (9.36)$$

and

$$Z_{peak} = Z_{target} \frac{V_{pk-pk}}{V_{noise}} \frac{\pi}{4} \quad (9.37)$$

Taking the very conservative approach that the peak-to-peak voltage is twice the single-ended noise allowed, we see that the condition for the voltage to be within spec when the resonant peak is driven with the maximum peak-to-peak current requires the peak impedance to be below about

$$Z_{peak} < Z_{target} \frac{\pi}{2} = 1.6 \times Z_{target} \quad (9.38)$$

This observation suggests that the condition that all the PDN's impedance features be below the target impedance is a little conservative by a factor of 1.6 at resonant peaks. Peak impedances at parallel resonances could be 1.6 times the target impedance and still achieve a marginally robust PDN with worst-case voltage noise below the tolerance limits.

To require the worst-case voltage noise on the PDN to be below the noise tolerance at all frequencies, is really to require:

1. The impedance profile in flat regions to be below the target impedance
2. The characteristic impedance of all peaks to be below the target impedance
3. The peak impedances at resonances to be below

## 1.6 times the target impedance

Generally, having real products fully stimulate a resonance peak is difficult but not impossible. The maximum transient current steps have to be drawn at just the right time and phase to reinforce the resonance.

### Tip

Usually energy at the resonant frequency does not come with the full current transient, or full current transients do not repeat at precisely the resonant frequency. Complete stimulation of a resonant frequency by microcode is a rare event and difficult to implement even when you are trying to do so.

It can, however, be done in a lab setting by intentionally clock gating at the resonant frequency.

For aircraft and spacecraft designs where human lives are at stake and other applications where failure is not an option, the recommendations is to have the impedance peak be below the target impedance. This is a much more stringent requirement than the characteristic impedance be below the target impedance.

A fully robust PDN, where all impedance peaks are below the target impedance, is almost always more expensive than a PDN where just the characteristic impedance meets the target impedance.

### Tip

The target impedance is a quantity calculated from knowledge of the product circuits, including the voltage tolerance and transient current consumption. A fully robust PDN has an impedance peak that is below the target impedance. A marginally or reasonably robust but cost-effective PDN has a characteristic impedance of the Bandini Mountain that meets the target impedance.

## 9.13 TARGET IMPEDANCE AND THE TRANSIENT AND AC STEADY-STATE RESPONSES

In this section, we re-examine the target impedance in

light of the previous sections on impulse, step, and resonance response. We find that the definition of target impedance works well for wideband, transient responses, particularly when the PDN has a flat impedance profile. For AC steady state and PDNs that have no more than one impedance peak, the target impedance is conservative by about a factor of 1.6.

The traditional definition of target impedance is

$$Z_{\text{target}} = \frac{V_{\text{dd}} \times \text{tolerance}}{I_{\text{transient}}} \quad (9.39)$$

The transient current has been defined as the maximum current minus the minimum current, which is essentially a peak-to-peak current. We usually think of tolerance in terms of percentage, often 5%, but we usually mean  $\pm 5\%$  when we talk about a 5% tolerance. The tolerance value is like an amplitude that is double sided. This is in contrast to the transient current, which is peak to peak and single sided.

This definition works well for a resistive PDN. When the maximum current is consumed, the die voltage drops to  $-5\%$ . When the current goes away, the voltage returns to nominal. It also works well for PDNs that have a flat impedance profile. The concept of a “load line” or “adaptive voltage positioning” [6] is sometimes used in the VRM to ensure that when the maximum current is consumed and the voltage drops 5%, the regulation loop does not return the voltage to the nominal value. In this case, the die voltage stays between nominal voltage and  $-5\%$ .

However, in many PDN situations a voltage droop occurs and the die voltage automatically recenters in response to the droop. One example is the VRM regulation loop. If DC IR drop is responsible for a 5% voltage droop after a transient current attack, the

regulation loop without a load line or adaptive voltage positioning might restore the die voltage to its nominal position, depending on the position of the feedback point for the regulation loop.

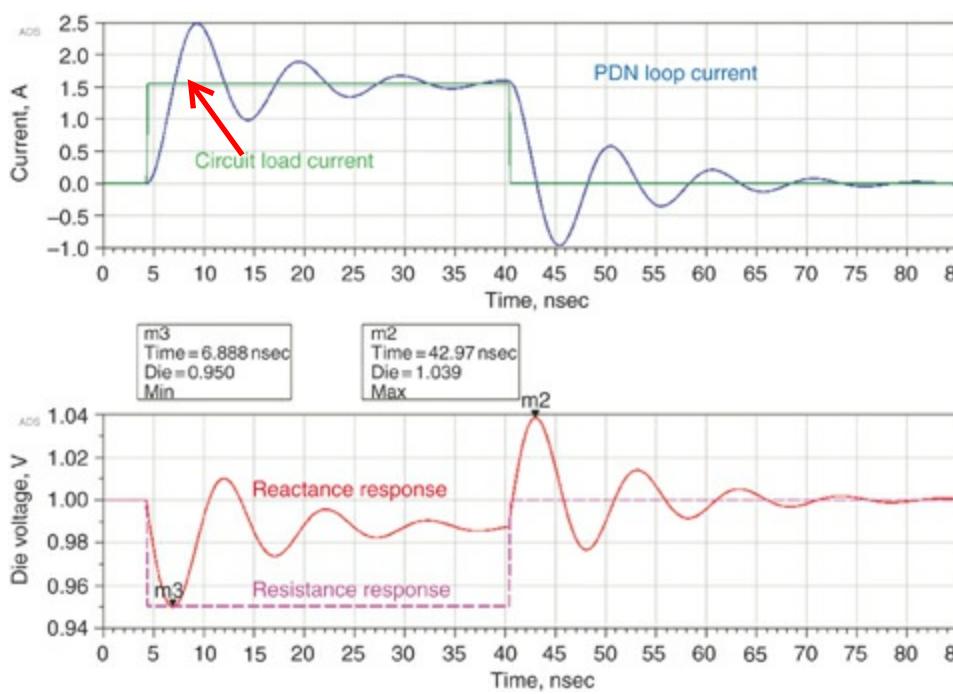
Another common example is the case of an inductive PDN section followed by a capacitor. A fast transient causes the die voltage to droop when the capacitor consumes charge but the inductor will restore the die voltage to its original value after several PDN time constants. In these examples the die voltage has been recentered after a transient current attack.

Sometime after the current attack, a current release occurs and the current returns to its minimum value. A PDN that has recentered the die voltage by either regulation loop or inductor response now experiences a voltage spike that is essentially the same magnitude but opposite in direction of the original voltage droop.

**Tip**

The transient response to a flat impedance profile with a VRM, which recenters the voltage, or to an LC PDN, tends to take up the plus and minus voltage tolerance (double sided) in response to a complete transient current event (single sided). The definition of transient current is consistent with these situations.

For example, in the transient response shown in [Figure 9.21](#), the PDN has been in a stable, zero current state for a long time. All of a sudden the PDN is stimulated with a step of current that is 1.55 A high. Then after about 40 nsec, the 1.55 A current goes away. We will look at responses of an LC PDN and a resistive PDN to this step current waveform.



**Figure 9.21** A typical transient current and the PDN response. **Top:** Transient current through the die and through the external PDN. **Bottom:** The voltage's on the die-pads for the case of a resistive and reactive PDN.

As demonstrated in previous examples, a typical reactive PDN with package and board loop inductance together with the on-die capacitance forms an impedance peak. The circuit current is initially delivered by the on-die capacitance and the voltage sags. This puts a voltage across the inductive loop and current accelerates from the board and package with a  $di/dt$  according to  $V/L$ . The voltage waveform bottoms out at the current transient times the characteristic impedance of the reactive elements.

$$V_{\text{step}} = I_{\text{step}} \times Z_0 = 1.55 \text{ A} \times 32 \text{ m}\Omega = 49.6 \text{ mV} \quad (9.40)$$

Also shown in Figure 9.21 is the response from a purely resistive PDN of  $32 \text{ m}\Omega$ . This is the same as the characteristic impedance and the target impedance of the PDN for this chosen current.

As expected, the  $32 \text{ m}\Omega$  resistive PDN and the reactive PDN with  $Z_0 = 32 \text{ m}\Omega$  give the same voltage droop after the current attack. The resistive PDN stays at the

maximum droop but the reactive PDN recovers to nearly the starting voltage. This is because the impedance of the inductor is low at low frequency (increasing time). The voltage waveform rings out and settles to a value that is the DC IR drop for the PDN. In this case, it is  $1.55 \text{ A} \times (5.1 + 3) \text{ m}\Omega = 12.5 \text{ mV}$  down from the starting value of 1 V. The reactive PDN recenters the voltage close to the starting voltage. This value varies depending upon the location of the series resistance in the PDN topology.

Then at 40 nsec, the 1.55 A load step current goes away. As expected, the resistive PDN immediately returns to its initial voltage. The reactive PDN, which has nearly recentered itself then experiences an inductive kick that sends the voltage well above the starting voltage. This is because current that is flowing in the inductor does not want to immediately stop. It flows into the capacitor and charges it up 39 mV above the starting voltage. This is almost 50 mV above the recentered voltage.

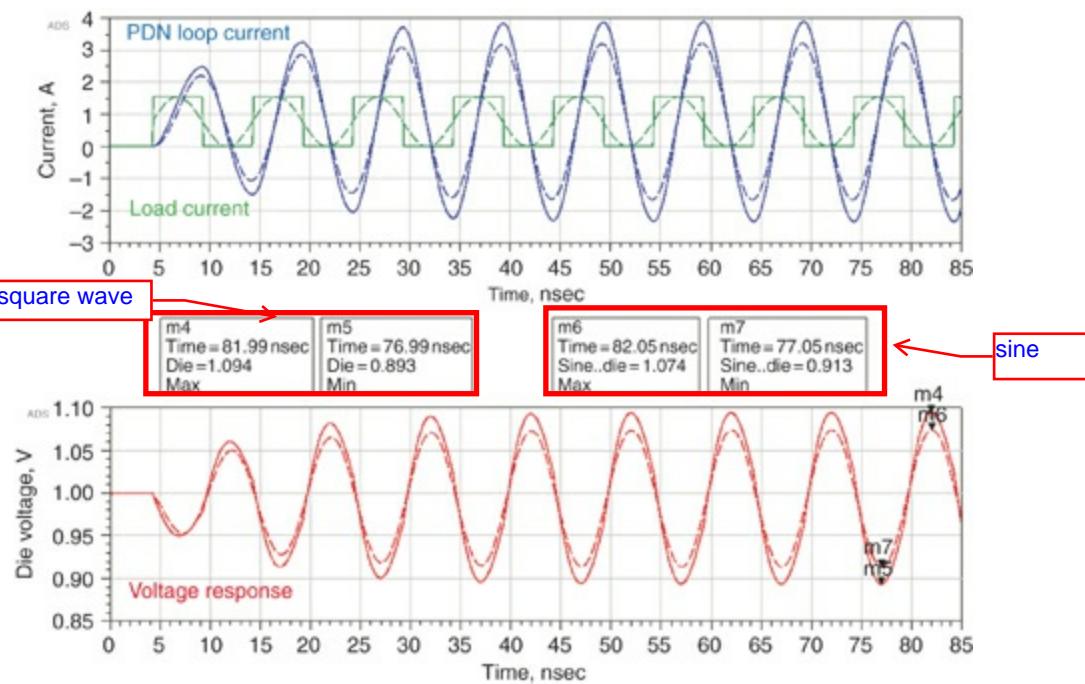
This transient current example clearly shows how a single-sided current has caused a double-sided voltage response. The initial droop was  $I_{\text{step}} \times Z_0$  in the negative direction. After the PDN voltage recentered and the current went away, the voltage response was  $I_{\text{step}} \times Z_0$  in the positive direction. A similar phenomenon occurs when a VRM regulation loop recenters the PDN voltage due to DC IR drop. After the current step goes away, a momentary PDN voltage peak occurs that is nearly as high as the droop was deep.

**Tip**

The target Impedance definition is consistent with the transient response. The equation involves a single-sided, peak-to-peak current and a voltage tolerance that is double sided; that is,  $\pm 5\%$ .

The situation is a little different in frequency domain analysis, which assumes an AC steady-state response. This is the familiar situation where we calculate the frequency domain impedance by dividing the sine wave voltage at a frequency by the sine wave current at the same frequency. The analysis assumes pure sinusoids that have been going for a long time. This is the case with every VNA measurement.

**Figure 9.22** shows the PDN stimulated with a square wave (solid) and a sine wave (dashed) current. The peak-to-peak excursions are 1.55 A, which is an amplitude of 0.775 A. The initial droop at about 7 nsec is the transient response. It is about 50 mV deep and is consistent with the transient response shown in the previous figure.



**Figure 9.22** Time domain response of a sine wave from initial turn on to reaching the steady state. **Top:** The current draw from the die and from the rest of the PDN. Solid lines are associated with square wave stimulating current; dashed lines are for the sine wave stimulating current. **Bottom:** The voltage response on the die pads for the steady-state current. The square wave amplitudes are  $4/\pi$  larger than the sine wave amplitudes.

As time goes on and the PDN is stimulated at the

resonant frequency, the steady-state AC response develops. For AC steady state, the voltage waveform is related to the impedance peak rather than the characteristic impedance. The simulated impedance peak is  $0.104 \Omega$ . We can use either the amplitude or the peak-to-peak current waveforms along with the impedance peak's value to predict the voltage waveform.

for a given sine, voltage should relate to the impedance at that freq, right ?

For the sine wave current, the expected peak-to-peak voltage is

$$V_{\text{pk-pk}} = I_{\text{pk-pk}} \times Z_{\text{peak}} = I_{\text{transient}} \times Z_{\text{peak}} = 1.55 \text{ A} \times 0.104 \Omega = 0.161 \text{ V pk-pk} \quad (9.41)$$

The simulated peak-to-peak voltage is  $1.074 - 0.913 = 0.161 \text{ V}$ , just as predicted.

For the square wave current, the expected peak-to-peak voltage is

$$V_{\text{pk-pk}} = \frac{4}{\pi} I_{\text{pk-pk}} \times Z_{\text{peak}} = \frac{4}{\pi} I_{\text{transient}} \times Z_{\text{peak}} = \frac{4}{3.14159} 1.55 \text{ A} \times 0.104 \Omega = 0.205 \text{ V} \quad (9.42)$$

The simulated peak-to-peak voltage is  $1.094 - 0.893 = 0.201 \text{ V}$ .

In the target impedance definition, we used a one-sided peak-to-peak value for the transient current and a double-sided amplitude value for the voltage tolerance. This worked well for the case of transient currents and peak voltage excursions.

For the AC steady-state response, we saw that the peak-to-peak transient sine wave current matched the predicted voltage response if we called the voltage response the peak-to-peak voltage. If we call the voltage response the amplitude, then a peak-to-peak sine wave transient current and the target impedance predict a voltage response that is twice as large as the amplitude.

This means that in the special case of the steady-state AC response, the definition of target impedance and peak-to-peak sine wave transient current predicts a

given it square or sine wave

voltage response twice the tolerance limit. In this special case, the target impedance limit is conservative by two times.

If we have a square wave of transient current, its peak-to-peak current has a first harmonic sine wave peak-to-peak value that is  $4/\pi$  times the square wave peak-to-peak value. This reduces the conservative factor by  $\pi/4 \times 2 =$  only 1.6 times the target impedance.

because vdroop is only half , while target impedance generally assumes full

**Tip**

For AC steady state and a single impedance peak, after all transients have died out and the PDN voltage has recentered, the target impedance is conservative by only a factor of 1.6.

The condition of a square wave of transient current driving at precisely the resonant frequency is a low probability occurrence. When we view this rare event in the frequency domain, we might conclude that the worst-case peak voltage noise on the PDN could be kept below the tolerance limits if PDN impedance peaks were kept below 1.6 times the target impedance value.

As demonstrated in an upcoming section on rogue waves, in this even more extremely rare situation, we use up all the AC steady-state margin plus some more. This condition arises when a PDN with an extreme case of several high q-factor resonances that all meet the target impedance are stimulated with an extremely highly tuned current waveform.

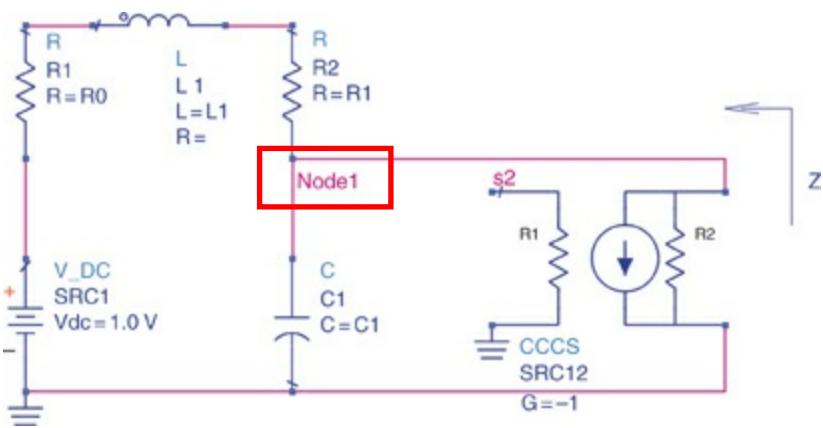
## 9.14 IMPACT OF REACTIVE ELEMENTS, Q-FACTOR, AND PEAK IMPEDANCES ON PDN VOLTAGE NOISE

As we have seen in earlier sections, the PDN isn't a resistive network with a constant impedance with frequency. It is modeled as an assortment of capacitive and inductive elements corresponding to the

interconnect's physical features and with added discrete capacitor elements. These reactive elements with high q-factors store energy and generate larger voltage and current excursions than are found in a purely resistive network. The impedance profile shows peaks.

However, even with peaks in the impedance profile, if the peak impedances are below the target impedance, regardless of the q-factor of the peaks, the worst-case voltages with the maximum current transient are almost always below the noise tolerance. Rogue waves, discussed in the next section, are an exception to this rule but these are extremely rare events. Our use of a single target impedance as a design goal for the PDN is still a useful metric even with a reactive impedance profile. To demonstrate this, we next consider several PDNs with a similar peak impedance but very different q-factors. The responses to repeating sine or square waves are similar but the step responses are different, depending on the q-factor and damping.

A simple PDN that exhibits the Bandini Mountain feature is composed of a single L and C element with some resistive loss terms, as shown in Figure 9.23. This could represent the on-die capacitance and the package lead inductance. Through this PDN profile, we draw the maximum transient current as a step current and then as a sine wave at the resonant frequency and compare the voltage noise response with our tolerance spec as we change the damping in the PDN.



**Figure 9.23** Simple circuit model for a PDN showing just a single L and C element with associated damping resistance in each term. The impedance is measured from node 1, corresponding to the on-die pads.

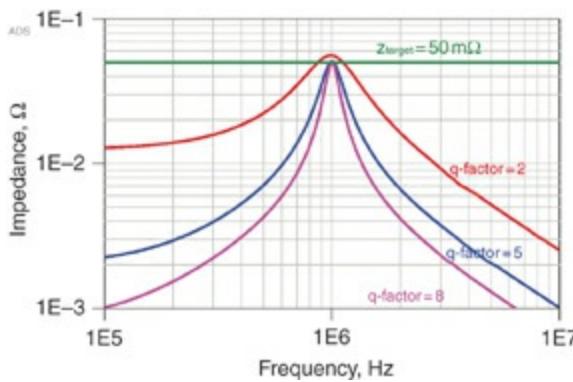
We used the circuit in [Figure 9.23](#) to demonstrate the impedance versus frequency of several PDNs with several q-factors. We simulated the impedance looking into node1. The resistor elements are there on either side of the inductor to be consistent with the model to be simulated in the next section on rogue waves.

If the damping resistance was all we changed, the resonant frequency would have stayed the same and the peak impedance value would have increased as the q-factor increased. This is the behavior we are used to seeing in an RLC circuit. However, we engineered the circuit's L and C so the peak amplitude always stayed the same, at the target impedance, as we adjusted the q-factor.

We adjusted the inductor and capacitor values with each set of resistors to engineer the same resonant frequency of 1 MHz, the same peak impedance of 50 mΩ, but different q-factors. The q-factors ranged from 0 to 8. For comparison, the q-factor of a purely resistive PDN is always zero, because the resistor does not store any energy.

[Figure 9.24](#) shows the impedance profiles for four different combinations of R, L, and C values. We used the equations developed in [section 9.13](#) to obtain an

impedance peak of  $50 \text{ m}\Omega$  at 1 MHz.



**Figure 9.24** Impedance profile for four different combinations of circuit elements with different q-factors.  
All combinations have a peak impedance of  $50 \text{ m}\Omega$ .

Table 9.3 shows the parameter values for these four scenarios. For the case of a q-factor of 0, we zeroed out the reactive elements and the PDN network was just the  $50 \text{ m}\Omega$  resistance.

q-factor	0	2	5	8	Units
Target Z	0.05				Ω
Resonant freq	1				MHz
Loop L	—	3.98	1.59	0.99	nH
Loop C	—	6,366	15,916	25,465	nF
$Z_0$	—	0.025	0.010	0.006	Ω
Loop R	0.050	0.013	0.002	0.001	Ω

**Table 9.3** Values for each parameter in the four scenarios with PDN profiles having different q-factors but the same peak impedances.

The  $50 \text{ m}\Omega$  resistor is the obvious straight line. As the q-factor increases, the peaks become sharper. The peak impedance for each PDN profile meets the same  $50 \text{ m}\Omega$  target impedance. A PDN with a higher q-factor must have a lower inductance, a higher capacitance, and lower loop resistance. The characteristic impedance  $Z_0$  is lower but the product of  $Z_0$  and the q-factor are the same. The PDNs have a similar peak impedance even though the q-factors and sharpness of the parallel

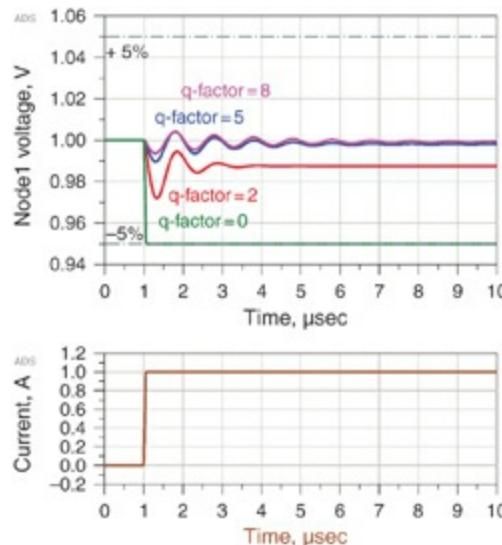
resonances are very different.

First we look at the voltage response to a step current, which is related to the characteristic impedance of the peak. Higher q-factor peaks have a lower characteristic impedance and a smaller voltage response. This is counterintuitive. Of course, a higher q-factor means the ringing lasts for a longer period of time.

**Tip**

We specially engineered these PDN circuits to have the same resonant frequency and impedance peaks by manipulating the inductance, capacitance, and q-factor. The resonance responses are similar even though the step responses are dramatically different. This is counterintuitive and demonstrates the roles of characteristic impedance and q-factors.

The voltage noise was simulated on the die pads across the capacitor for a step current transient of 1 A. Figure 9.25 shows the voltage response for each of the four impedance profiles.



**Figure 9.25** Voltages responses simulated for each of the four PDN impedance profiles with the same 1 A step current. The voltage noise is well contained between the  $\pm 5\%$  horizontal, dotted, voltage tolerance lines.

As expected, the  $50 \text{ m}\Omega$  resistor PDN had a 50 mV drop. It dissipates power, has a DC IR drop and has a flat frequency response. The voltage response is just a

constant DC drop.

The PDN with q-factor = 2 has a 24 mV droop, because its characteristic impedance is  $1/2 \times 50 \text{ m}\Omega$ . It shows some DC voltage loss due to the 13 mΩ of resistance in its path. The PDNs with higher q-factors show less DC IR drop because the loop resistance is lower. The requirement to keep the impedance peak below the calculated target impedance is conservative for the case of step currents, a single resonant peak, and high q-factors.

This simulation shows the general trend. Lower characteristic impedance PDNs (higher q-factors in this case) have lower reactance at resonance and smaller peak voltage noise generated by the same current. This behavior is only counterintuitive because we engineered the peak impedances to be the same by making some impedance peaks sharper.

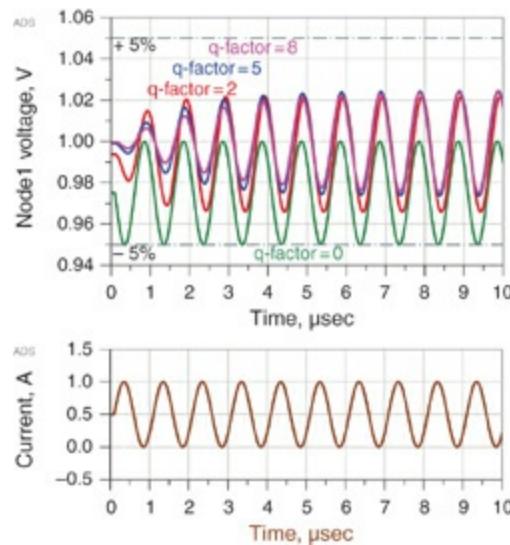
**Tip**

When the impedance peaks are engineered to be the same height but different q-factors, the maximum droop for a step current load decreases with higher q-factor as expected. The droop response is proportional to the characteristic impedance of the resonance.

In fact, the higher the q-factor, at constant peak impedance, the lower the reactance at resonance and the smaller the voltage noise associated with a step transient current. As the q-factor increases, the ringing lasts for more cycles. The q-factor is a good estimate for the number of visible cycles in the damped sinusoid waveform. The q-factor of 2 has about two dips, the q-factor of 5 has about five dips, and the q-factor of 8 has about eight dips, all at the same resonant frequency. Another way to look at this is that higher q-factor resonances have more “time memory” of events that

have taken place in the past.

Next, a pure sine wave current is drawn from node1 of the PDN. To be consistent with the 1 A step, the sine wave is 1 A peak to peak and is generated with a 0.5 A amplitude and a 0.5 A DC offset current. This makes the maximum current 1 A and the minimum current 0 A similar to the 1 A step of current. Figure 9.26 shows the simulated response of the PDN voltage to the sine wave of load current.



**Figure 9.26 Top:** Noise voltage from sine wave current excitation of each PDN impedance profile.

**Bottom:** The sine wave current profile showing a 1 A peak-to-peak value.

As expected, the resistor PDN with flat frequency response shows a waveform between 0.95 V and 1.0 V. The target impedance calculation allowed for 5% of 1 V or 50 mV drop and that is exactly what this simulation shows. Both the step response and sinusoid response of the flat  $50 \text{ m}\Omega$  PDN profile have resulted in 50 mV droops.

In contrast, the PDNs with  $50 \text{ m}\Omega$  impedance peaks behave differently. There is less resistance at DC so the curves are centered closer to the nominal PDN voltage value of 1 V. The amplitude builds up over several cycles. The PDN with q-factor of 2 takes just a couple of

cycles to build up to its maximum, the PDN with q-factor of 5 takes about five cycles, and the PDN with q-factor of 8 takes about eight cycles to build up to the maximum.

Recall that the initial step response dips of the higher q-factor PDNs were not as deep, but the ringing lasted longer. This enables a longer time for superposition of dips upon dips and peaks upon peaks when stimulated with a repeating waveform. If the sinusoid stimulation lasts long enough, all  $50\text{ m}\Omega$  resonant peaks end up with  $50\text{ mV}$  of p-p noise because they must without regard to q-factor.

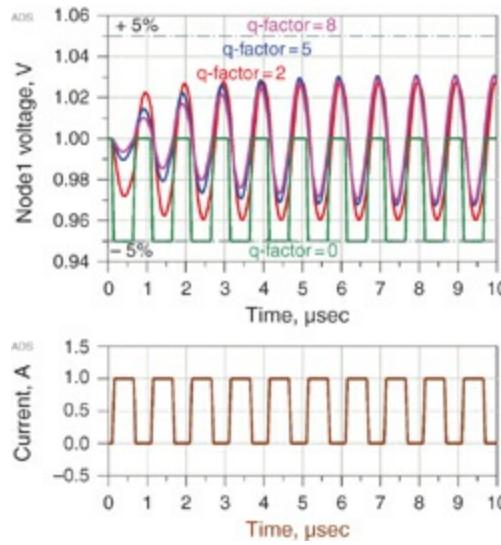
The PDN with q-factor of 2 exceeded the target impedance by about  $6\text{ m}\Omega$  and so the p-p voltage swing is about  $56\text{ mV}$ , a little more than the other PDNs that met the target impedance and had  $50\text{ mV}$  p-p voltage waveforms.

An important observation is that PDNs with low DC resistance spend the majority of the time centered on the nominal voltage. Positive load currents (meaning that the load only draws current and does not push current back into the PDN) cause both voltage dips and voltage peaks relative to the nominal PDN voltage when reactive elements are involved. This is particularly true at resonant frequency. This is another clear example of a single-sided current stimulating a double-sided voltage response.

#### Tip

If the PDN resonant peak exactly meets target impedance and the PDN is stimulated with a sine wave current having a peak-to-peak value equal to the full transient current, the peak-to-peak voltage is the same as the tolerance voltage used in the target impedance calculation (that is,  $50\text{ mV}$ ), independent of the peak's sharpness. This is a factor of 2 safety margin because the peak-to-peak voltage will be centered for high q-factor PDNs. The voltage waveform is centered on the nominal voltage if the PDN has low DC IR drop.

As a final example in this section, we used a square wave of current to stimulate the PDN. Once again, the current drawn by the load is between 0 and 1 A. Figure 9.27 shows the voltage response to the square wave excitation. The  $50\text{ m}\Omega$  resistor PDN has a 50 mV square wave response as expected with voltages between 950 mV and 1 V. Because of the flat frequency response, square waves of all frequency behave the same with a resistive PDN.



**Figure 9.27 Top:** Voltage response generated on each PDN to a square wave current excitation. **Bottom:** The square wave of current drawn in each PDN impedance.

The PDNs with q-factors of 2, 5, and 8 respond to the square wave similarly to the way they responded to the sine wave. They take approximately two, five, and eight cycles, respectively, to build up to their maximum peak-to-peak values. The higher q-factor waveforms are centered near the nominal voltage. The lower q-factor PDN shows a lower average voltage because of DC IR drop in the current path.

The peak-to-peak voltage for higher q-factor PDNs is  $4/\pi$  higher than that of the zero q-factor PDN (straight  $50\text{ }\Omega$  resistor) when the PDN is stimulated by a square wave current. As discussed earlier, the impedance peak is a filter that brings out the first harmonic of the square

wave. The p-p amplitude is

$$V_{pk-pk} = \frac{4}{\pi} \times Z_{peak} \times I_{transient} = \frac{4}{\pi} \times 50 \text{ m}\Omega \times 1 \text{ A} = 64 \text{ mV} \quad (9.43)$$

**Tip**

In each of the transient waveforms with a single peak in the impedance profile, using a target impedance based on the maximum transient current and the voltage noise tolerance is a good design practice. It provides a little bit of margin when the PDN is driven by a resonant square wave of maximum current.

The flat, resistive impedance profile takes up the whole voltage tolerance. Impedance profiles with reactive peaks allow the noise voltage to recenter around the nominal voltage, particularly with higher q-factors, and the voltage droops are not as severe. The voltage noise for reactive PDNs eats up only a portion of the tolerance.

This is not always the case when there are multiple, nearly equal value peaks in the PDN, as we show in the next section.

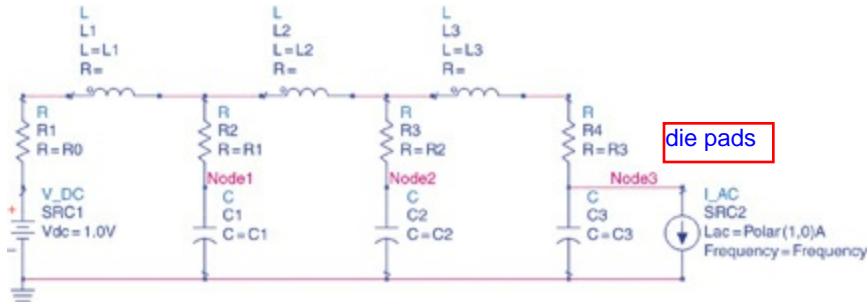
## 9.15 ROGUE WAVES

As shown by the simulation for step, sine, and square wave transient currents, PDNs that meet the target impedance do not have voltage excursions beyond  $\pm 5\%$  tolerance. This is true for PDNs with just one major impedance peak in the system. Keeping the impedance peaks below the target impedance was a good method for managing the voltage noise.

However, if there are several major peaks of similar height and high q-factor, the possibility exists for energy from current at one peak frequency to continue to drive the PDN while the other peak frequencies are stimulated. This can lead to voltage noise, which builds up by superimposing the waves of one resonance into

the waves of the next resonance and the following resonance, resulting in a composite waveform that exceeds the peak voltage from any single resonance and exceeds the tolerance used in the target impedance calculation. This very special situation has been termed a *rogue wave effect*. It was first introduced by Xiang Hu in his PhD thesis and related publications [7]–[9].

To illustrate this phenomenon, we designed a simple PDN with three parallel resonances, each of equal q-factor and peak impedance, but with very different self-resonant frequencies. We used the equations discussed in section 9.14 to accomplish this. Figure 9.28 shows the circuit engineered to represent this PDN.



**Figure 9.28** Carefully contrived PDN circuit that has three impedance peaks at different frequencies and of comparable peak impedances.

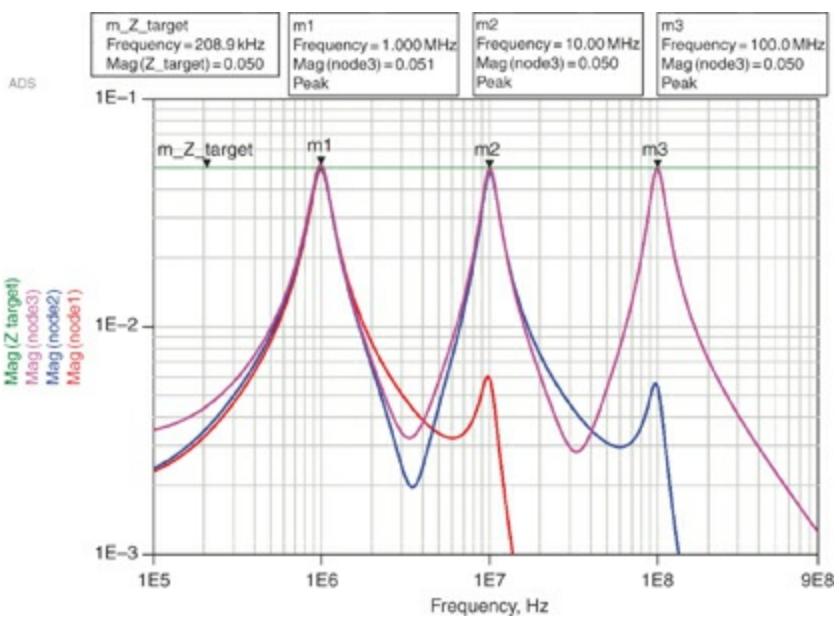
The circuit values were based on engineering the same q-factor and peak impedance but different resonant frequencies. Table 9.4 summarizes the final circuit values.

Component Parameters for Rogue Wave Simulation				
Transient current	1			A
Voltage	1			V
Tolerance	5			%
Z_target	0.050			$\Omega$
q-factor	4			
	Peak 1	Peak 2	Peak 3	
Frequency	1	10	100	MHz
L_loop	2.0	0.2	0.02	nH
C_loop	11459	1146	127	nF
Z <sub>0</sub>	0.013	0.013	0.013	$\Omega$
C1, C2, C3	11459	1273.2	143.24	nF
R_estimate	1.563			m $\Omega$
R1, R2, R3	1.531	1.194	1.219	m $\Omega$
R0	1.813			
R0, R1, R2, and R3 are adjusted slightly to bring peak to 50 m $\Omega$ .				

**Table 9.4** Parameters that define the three impedance peaks.

This topology enables each loop to have the same resistance making it easier to manage q-factors. The topology enables us to choose the loop inductance and loop capacitance such that the impedance peaks are at 1, 10, and 100 MHz. We chose the inductance and resistance to achieve the desired resonant peak height and q-factor.

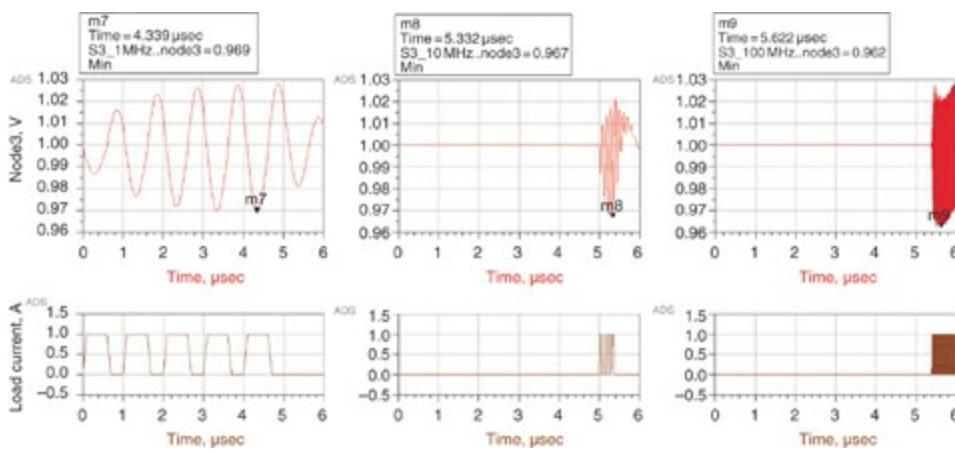
We simulated the circuit's frequency domain impedance using the AC current source attached to node3, the die pads. With a 1 A amplitude, the voltage at node3 is equivalent to the impedance in  $\Omega$ . In addition, the voltages measured at each of the intermediate nodes are also shown in Figure 9.29.



**Figure 9.29** Impedance simulated on the three nodes of the circuit in *Figure 9.28* by observing the voltage produced by a 1 A AC current source. Note that the voltage on node3 is the effective impedance as viewed from the chip pads (node1). We adjusted the circuit elements to produce three different parallel resonant peaks each with the same q-factor and peak impedance.

The impedance from node3, the die pads, shows resonant peaks at 1, 10, and 100 MHz, each meeting the target impedance of  $50 \text{ m}\Omega$ . The q-factor is 4 for each case. Peak m1 is associated with the resonance at node1, peak m2 is associated with the resonance at node2, and m3 is associated with the resonance of node3.

We used a square wave current to stimulate each of the PDN peaks. Because the q-factor is 4, it took about four cycles to achieve the maximum ringing. We used a different frequency square wave to stimulate each peak. To ensure that only one peak is stimulated at a time for each square wave, we adjusted the rise time to reduce the energy of the tenth harmonic, which would stimulate the next higher peak. *Figure 9.30* shows the current waveforms driving the PDN and the resulting voltage noise on the die pads.



**Figure 9.30** Square wave excitation of each PDN peak using different frequency square waves and the time sequence of each square wave of current. Note, with the same q-factor of 4, it takes about four cycles for the voltage to reach its steady state, maximum value.

The plot on the left is stimulated with a 1 MHz square wave current between 0 and 1 A. We used a sufficiently slow rise and fall time so that the higher resonant frequencies are not stimulated by the edge rate. The 1 MHz resonance reaches a maximum depth of 969 mV at about 4.3  $\mu$ sec, well above the 950 mV associated with the 5% tolerance used in the target impedance calculation.

The square waves of current are timed to not overlap. This maintains the current range within the 0 to 1 A assumption for transient current used in the target impedance calculation. In this set of waveforms, each square wave sequence happens in isolation of the others. We observe that the voltage response from each set of square wave cycles reach a similar depth.

Beginning at about 5  $\mu$ sec the 10 MHz square wave current begins as shown in the middle plot. We allowed it to run for four cycles to bring out the maximum voltage waveform of the second resonance. The voltage droops down to 967 mV at 5.33  $\mu$ sec, which is a little lower than the first resonant minimum. This is probably because the 10 MHz square wave current has stimulated

both the 1 MHz and 10 MHz peak. The rise time is limited on the 10 MHz square wave so that the 100 MHz peak is not stimulated.

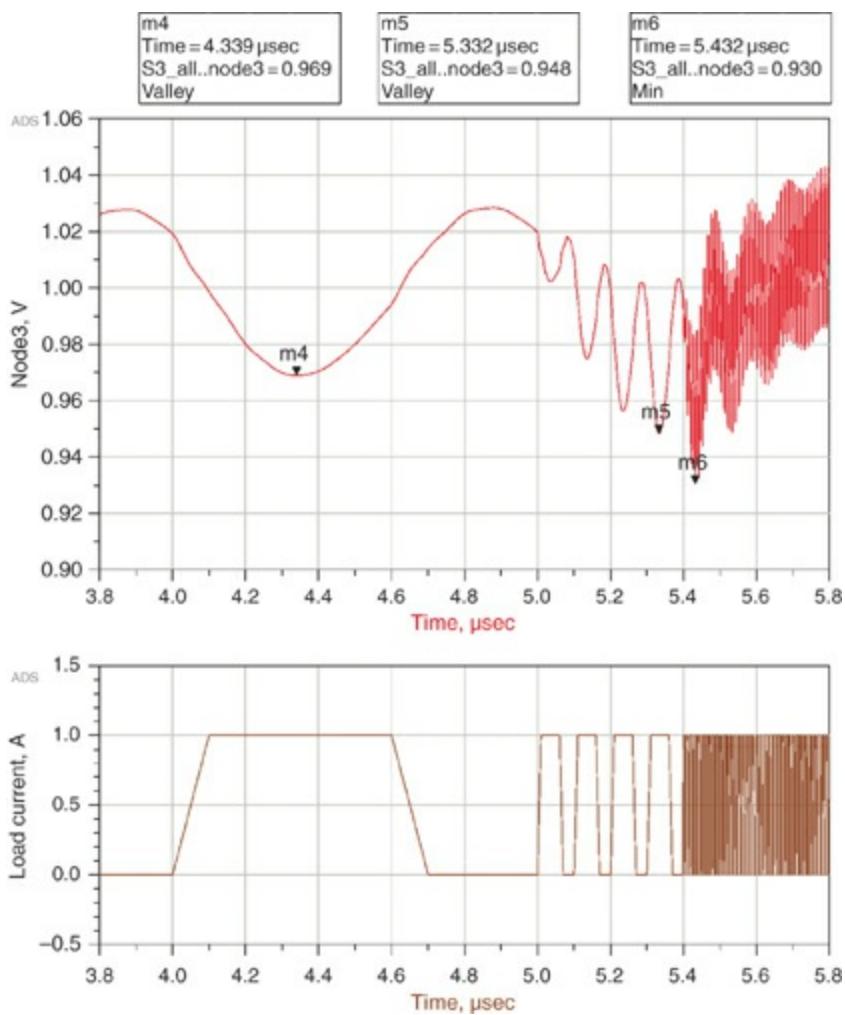
Then at about 5.4  $\mu$ sec the 100 MHz current square wave begins. The deepest dip for 100 MHz is 962 mV at 5.62  $\mu$ sec. This time all three resonant peaks are being stimulated by the 100 MHz current waveform. This is the deepest dip so far but is still comfortably above Vdd -5% (950 mV).

**Tip**

When we apply a square wave of current at constant frequency to excite and stimulate just one peak in isolation, we see that the peak voltage response is well within the  $\pm 5\%$  tolerance associated with our target impedance metric. The target impedance is a robust indicator of expected PDN noise.

However, if we carefully sequence these same square waves of current, we can build up a rogue wave that has a maximum voltage response that exceeds the  $\pm 5\%$  tolerance.

To generate a rogue wave, we stimulated each impedance peak in sequence. After the peak voltages of the low-frequency resonance have been reached, the next resonant peak is excited. After both the first and second resonant peaks have been excited, the third resonance is stimulated before the other two die down. In this way, the rogue wave builds from this carefully timed sequence of different frequency square waves of current. Figure 9.31 shows the resulting voltage response on the die pads from this carefully engineered sequence of square wave trains.



**Figure 9.31 Top:** The resulting voltage response on the die pads from the buildup of the first, second, and then third resonance. Note the maximum voltage response in this case exceeds the  $\pm 5\%$  tolerance used in the target impedance calculation, even though each peak was below the target impedance. **Bottom:** The carefully engineered sequence of trains of square wave current to sequentially drive each of the three resonances to their maximum voltage.

The pathological case of the rogue wave occurs when all three resonances are stimulated in exactly the timed sequence as shown in Figure 9.31. The 1, 10, and 100 MHz square wave trains shown in the figure are now concatenated together to stimulate each resonance in turn. As shown by the current waveform, the load never drew more than 1 A or less than 0 A. We zoomed in on the horizontal axis to show just the last of the 1 MHz pulses. The 10 MHz pulses begin at 5 μsec and 100 MHz pulses begin at 5.4 μsec. We chose the timing to

maximize the effect of each resonance in turn and then go on to the next resonance before the previous one dies out.

The upper part of the figure shows the PDN response. The marker M4 shows the expected 969 mV from the 1 MHz resonance alone. The marker M5 shows 948 mV, which has been achieved by compounding 10 MHz waveform onto the 1 MHz waveform at just the right moment (phase of the 1 MHz waveform). This is the first time we have seen the voltage waveform drop below 950 mV. Then the 100 MHz current square wave load begins when the compounded 1 MHz and 10 MHz waveforms max out. The voltage droops to 930 mV, which is 7% below the nominal Vdd voltage and exceeds the 5% tolerance used in the target impedance calculation.

This example demonstrates that the voltage tolerance can be exceeded on a PDN that meets target impedance over the entire frequency range. The key to this was to store up energy in resonances and let them continue to ring out as new resonant peaks are stimulated. The reactive elements essentially have memory of previous events and are capable of delivering energy back into the system long after the events are over.

This situation is made worse with higher q-factors. In this example with q-factors of only 4, stimulation of two resonant peaks could barely exceed the voltage tolerance and it took the stimulation of three resonant peaks in a perfectly timed manner to degrade from a 5% tolerance to a 7% tolerance.

If the q-factors were 10 or more, the resulting voltage excursions would have far exceeded the tolerance limit. Also, if the peak impedances exceeded the target impedance, the magnitude of the rogue wave could be even higher.

In practice, getting code to completely stimulate a single resonant peak is difficult. Stimulating two resonant peaks is very difficult and stimulating the second resonance in perfect phase with the first resonance is even more so. The probability of code stimulating a third resonance in proper phase with the first two resonances is extremely low.

**Tip**

This analysis focused on minimizing the PDN droops. We could do a similar study with waveforms intended to minimize the PDN voltage spikes. The conclusion is the same: keep the impedance profile as flat as possible and center up the voltage by minimizing DC IR drop or by regulator feedback position.

Just as tornadoes seem to be attracted to trailer parks, microcode loops seem to be attracted to parallel resonant peaks in the PDN. However unlikely a rogue wave event is, with enough products and different applications, it might occur if there are multiple parallel resonant peaks with high q-factor, even if they never exceed the target impedance.

**Tip**

The very unlikely, but still possible occurrence of rogue waves is another reason why engineering reduced q-factors in all PDN resonances is a good practice. Economics dictate that there will be an undesirable Bandini Mountain, but you should design the rest of the PDN to eliminate impedance peaks, particularly those with high q-factor.

## **9.16 A ROBUST DESIGN STRATEGY IN THE PRESENCE OF ROGUE WAVES**

The rogue wave has three PDN features in its root cause:

1. A PDN with multiple, comparable impedance peaks at or slightly above the target impedance
2. A PDN with multiple peaks having a high q-factor

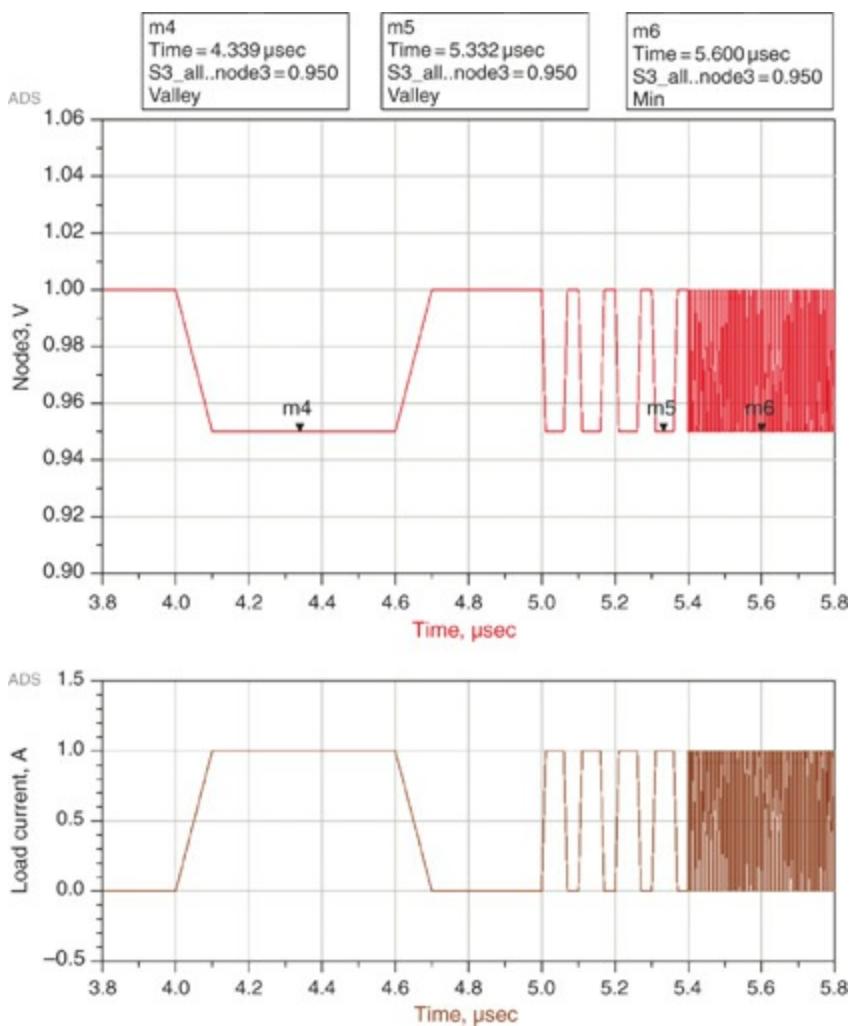
### 3. A carefully sequenced series of transient currents that stimulate each peak in turn

However unlikely a rogue wave is, good PDN design can manage it. There is nothing that we can do about the current waveforms. There is always some customer with some application that could generate just the right square wave frequencies and maximum current amplitude sequenced in just the right order and the right timing to drive a rogue wave.

We saw earlier that if we engineer the PDN with just one dominant parallel resonant peak impedance, at the target impedance, no possibility of a rogue wave exists and the maximum voltage transient is always within the tolerance limit.

If there are multiple, comparable impedance peaks at the target impedance, the lower their q-factor, the less time the ringing of each peak will last. This means the less time the response from one resonance will overlap with others. In the extreme case of a resistive PDN, there is no resonance and no overlap of ringing.

We applied the same pathological current waveform of sequencing square wave trains to the PDN with a resistive impedance. Figure 9.32 shows the resulting voltage noise on the PDN. Because the current never exceeded the 1 A spec, the voltage noise never exceed the  $\pm 5\%$  tolerance. The voltage waveform always stays between 950 mV and 1 V.



**Figure 9.32** Voltage noise on a resistive PDN using the same rogue wave stimulating square wave *current train* as before. **Top:** The resulting voltage noise on the die pads showing a voltage excursion always less than the 5% tolerance spec. **Bottom:** The stimulating current waveform.

This suggests that a good way to design a fully robust PDN is to make the impedance as flat as possible below the target impedance and avoid resonant peaks. Make the DC resistance as low as possible because the PDN noise waveform will be centered up around the nominal voltage. We can accomplish this by bringing the regulator feedback point close to the load.

The maximum transient current is the information we are most likely to have about the load. Most CMOS loads can draw a maximum transient current and no more. For power-saving reasons, the DC resistance is usually made small, so the PDN voltage recenters itself

near the nominal power supply voltage after a transient. We can often achieve better circuit performance and/or power savings by minimizing DC IR drop or regulating the fully loaded voltage back near nominal, thus giving rise to double-sided voltage responses when the load comes and goes away.

In contrast, PDN design philosophies exist that involve adaptive voltage positioning [6] or load lines that allow and actually force the PDN voltage to sag with load. The PDN impedance is flat from DC up to the highest frequencies. The PDN voltage is actually regulated down under high load conditions so that when the load releases, the inductive kick does not push the on-die circuit voltage as far above nominal as it might have otherwise. These systems are intended to reduce the overshoots on the high side but might have more power loss for the same circuit performance. They essentially position themselves near  $-5\%$  voltage when fully to reduce the maximum PDN voltage swing.

The target impedance concept is useful both in the case where the VRM regulates out DC IR drop and in the case where we use adaptive voltage positioning techniques. Consider the target impedance as a reference line to be compared with the actual PDN impedance. It is not a law or a specification that guarantees that the voltage tolerance will be met if the actual PDN impedance profile meets target impedance.

As demonstrated in this chapter, a PDN with a single impedance peak that meets target impedance is conservative by a factor of 2 for a pure sine wave current load and is conservative by a factor of 1.6 for a square wave current load at the resonant frequency.

For flat resistive portions of the PDN impedance profile—that is, where we use the FDTIM method to choose board capacitors—a broadband transient current

waveform of any shape will result in a voltage droop that is the same as the tolerance in the target impedance calculation.

In the special case of rogue waves involving multiple high q-factor impedance peaks and highly improbable, pathologically sequenced current events, the possibility exists to exceed the voltage tolerance even if the PDN impedance meets the target impedance across the entire frequency range.

We should design the PDN for every electronic product with cost and risk tolerance in mind. In general, PDNs where all impedance peaks meet target impedance in all frequency ranges are considered to be fully robust. PDNs where the characteristic impedance meets target impedance are considered to be marginally robust. PDNs with Bandini Mountains where the characteristic impedance exceeds the target impedance are vulnerable to customer code that might happen to stimulate the impedance peak.

## **9.17 CLOCK-EDGE CURRENT IMPULSES FROM SWITCHED CAPACITOR LOADS**

As discussed earlier, CMOS circuits draw dynamic current only when the clock switches. All dynamic current consumed by CMOS devices has its beginning in charge impulses consumed at clock edges. A circuit model using switched capacitor elements is developed to do exactly this.

Instead of using a constant current source or resistive load, charge is consumed each time the capacitors are switched. We use a new type of load called the **Switched Capacitor Load (SCL) [10]** to demonstrate impulse, step, and resonance current waveforms similar to those discussed earlier in this chapter, which were based on constant current source loads, but this time with the

SCL. We then use the SCL to address clock gating, clock swallowing, and power gating.

The most common type of load used for PDN analysis is a constant current source, possibly controlled by a piece-wise-linear (PWL) time sequence. This is easy and straightforward to implement, but the current source draws the specified amount of current no matter how much voltage is on the PDN rail at the moment.

CMOS does not behave this way. The dynamic current drawn by a CMOS load on the power rail is proportional to voltage and behaves exactly like a resistive element. As shown in previous examples, the PDN voltage at the circuit terminals is very much a function of time. As the voltage droops, less current should be drawn from the PDN. As the PDN voltage increases, more current should be drawn from the PDN. This actually provides damping (loss) to resonating PDN components. However, with a constant current source, current is predetermined, does not change with load, and no damping is provided.

A few years ago, attempts were made to use a resistor load to draw current from the PDN in simulations. The motivation was to draw current proportional to voltage and provide damping from the load. It is possible to have resistors in SPICE or other circuit simulators that are a function of time. By changing the resistor value with time, we can obtain a transient current with any desired ramp rate. This works well but it is somewhat cumbersome to provide a time sequence of resistor values to draw the proper amount of current.

A better possibility is to use switched capacitors to draw load current. Earlier in this chapter we saw that CMOS circuits consume dynamic current because of charging and discharging of capacitive loads.

**Tip**

Switched capacitor loads are a better representation of the inner workings of CMOS and provide valuable insight and intuition into the behavior of CMOS loads. PDN behaviors including the noise expected across the on-die capacitance and the PDN noise experienced at the circuit terminals are clearly demonstrated by this type of load. The load current decreases and increases and moves with the PDN voltage just like CMOS. This approach also emulates the damping expected.

CMOS circuits actually provide more PDN damping when they are drawing heavy current (low parallel resistance) compared to when they draw little current (high parallel resistance). This indicates that with the step and resonance responses, damping changes as a function of time because the current load changes as a function of time. This is a very non-linear, time-dependent effect that can only be transferred to the frequency domain as an average. For frequency domain analysis, all circuit elements must be linear and time invariant.

**Tip**

Although we can do much PDN analysis in the frequency domain, we must move into the time domain to capture the time-varying nature of damping that comes from CMOS loads. The switched capacitor load handles all of this because it consumes a current in exactly the same way as dynamic CMOS current. Close examination of the step response for high current loads reveals a different q-factor for the current attack and the current release.

This switched capacitor load example uses the same PDN impedance peak used in [section 9.8](#). For convenience, we have repeated the PDN parameters and expected droop performance in [Table 9.5](#). We engineered the impedance peak to be  $100 \text{ m}\Omega$  at 100 MHz using simple closed-form equations. We manipulated the target impedance to be at the PDN characteristic impedance by choosing the transient current to be 1.55 A.

Frequency Domain		
Vdd	1	V
Core cap	50	nF
PDN loop inductance	50.7	pH
PDN loop resistance	10.1	mΩ
Resonant frequency	100	MHz
PDN $Z_0$	32	mΩ
q-factor from PDN loop	3.15	
Expected impedance peak	100	mΩ
Assumed die resistance	5.0	mΩ
External PDN loop resistance	5.1	mΩ
Time Domain		
Dynamic current	1.55	A
$f_{clock}$	1	GHz
Target impedance	32	mΩ
Charge per clock cycle ( $Q_{cycle}$ )	1.55	nCoul
Expected clock-edge droop (impulse)	31	mV
Expected step response droop	49	mV
Expected peak-peak noise at resonance	198	mV

**Table 9.5** Parameters used to set up the circuits used in the switched capacitor load simulations.

With the given clock frequency of 1 GHz, we calculated the charge consumed per clock cycle:

$$Q_{clk\text{-edge}} = I_{dynamic} \times T = \frac{I_{dynamic}}{f_{clock}} = \frac{1.55 \text{ A}}{1 \text{ GHz}} = 1.55 \text{ nC} \quad (9.44)$$

We easily calculate the amount of load capacitance that must have switched, assuming a 1 V PDN, from  $Q = CV$  to be 1.55 nF. This means that in the average clock cycle, 1.55 nF is switched between power and ground. As discussed earlier, current is consumed on both the rising and falling edge of a switched output when load capacitors are connected to both Vdd and Vss. If the load capacitors are both 1.55 nF, then 1.55 nC is consumed from the PDN on both the rising and falling edge of the

charge consumed is constant

switch.

We want current to be consumed throughout the whole clock period to emulate the distribution of timings of the various combinational logic elements switching. We need to use a half-clock and switch both Vdd and Vss load capacitance to accomplish this. In this sense, the switched capacitor load has a different clock definition running at half-frequency compared to real CMOS circuitry. The SCL is based on a half-clock that consumes current on both edges. The SCL load draws current for each full-frequency CMOS clock cycle, but the important point is that current does not drop to zero halfway through the clock period. It smoothly diminishes to zero just before the beginning of the next clock cycle similar to real CMOS loads.

Real CMOS circuitry consumes major current when the clock's rising edge releases latched data into the combinational logic. A minor current is consumed on the clock's falling edge. Logic circuits continue to draw current through the remainder of the clock cycle until all switching is complete. This is required because a set-up time must be satisfied before the next rising edge of the clock. The PDN load current is highest at the beginning of the clock cycle and diminishes to zero at the end. This is sometimes called a *Poisson profile* and is well known in statistics. In the following simulations, the switched capacitor load uses a clock that is half of the real CMOS product clock frequency and has the current diminish to zero for each half period of the half-clock.

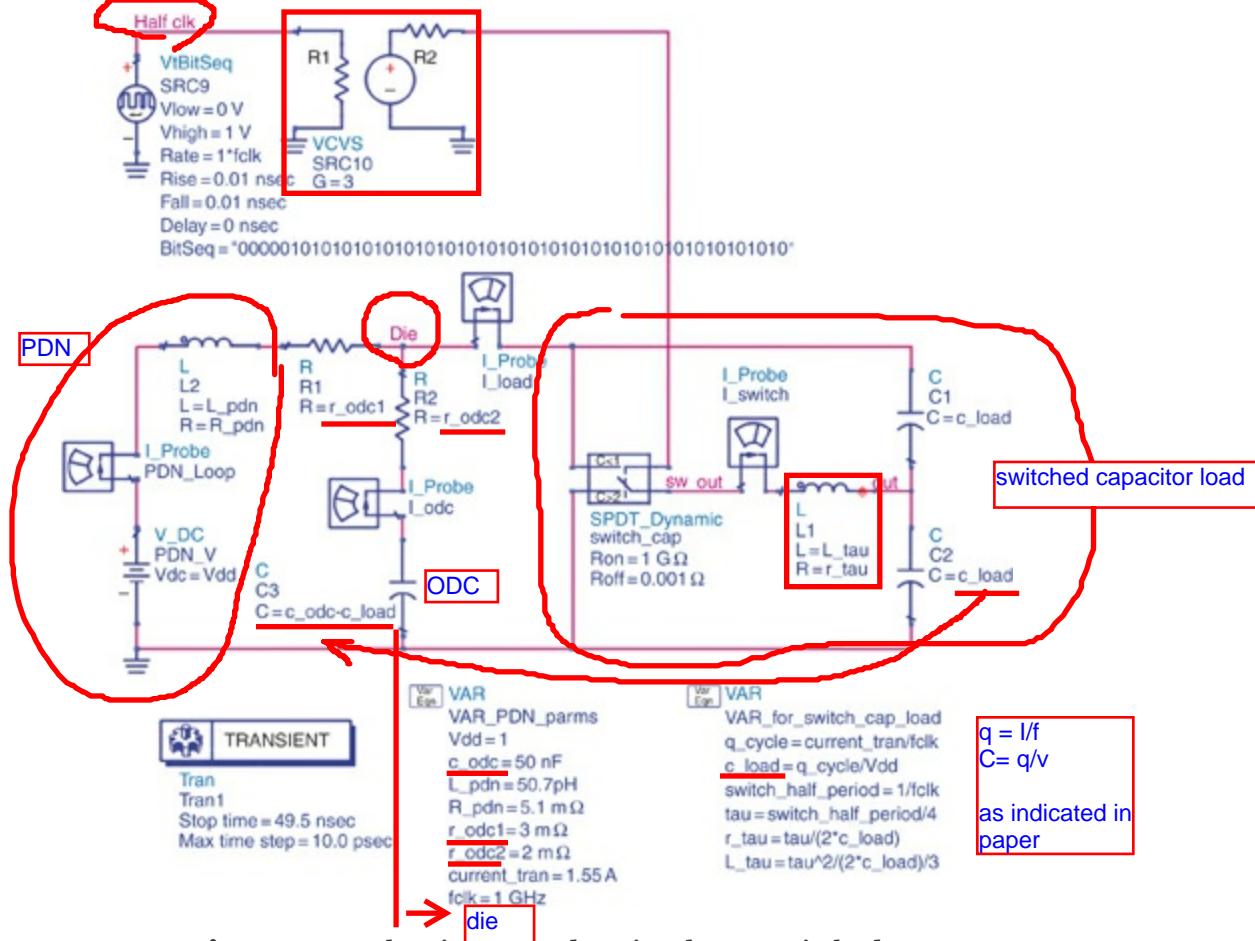
In an alternative topology, the output capacitance is to Vss only and the switch runs at full-clock frequency. In this case, PDN current is only consumed from the PDN during the first half of the clock cycle when the Vdd switch is closed. No current is consumed when the Vss

switch is closed because there is no load capacitance to Vdd. This creates a current profile that is very heavy early in the clock cycle and creates unrealistic voltage droops due to ODC ESR IR drop. For this reason, the half-clock topology is preferred.

In the following simulations for the switched capacitor load, we have both Vdd and Vss load capacitance (like the CMOS product) but initiate the PDN current by a clock that is half the frequency of CMOS product. This emulates the logic PDN current waveform but does not capture the small current consumed on the falling edge of the real product clock.

We evaluated the behavior of the switched capacitor load when the PDN supplying it had a single impedance peak, composed of the core, on-die capacitance, PDN package loop inductance, and PDN package series resistance. The values of all the elements of the circuit simulated are also shown earlier in Table 9.5.

We used ADS for the circuit simulation for the switched capacitor load. Figure 9.33 shows a complete schematic including parameter calculations. The major RLC PDN elements are in the middle left portion. The switched capacitor load is in the middle right portion. We calculated C\_load from the transient current and clock frequency parameters.



**Figure 9.33** The circuit used to simulate a switched capacitor load. A sequence of bits determines the timing for the capacitor load to switch on and off. Changing this pattern allows us to stimulate any current signature.

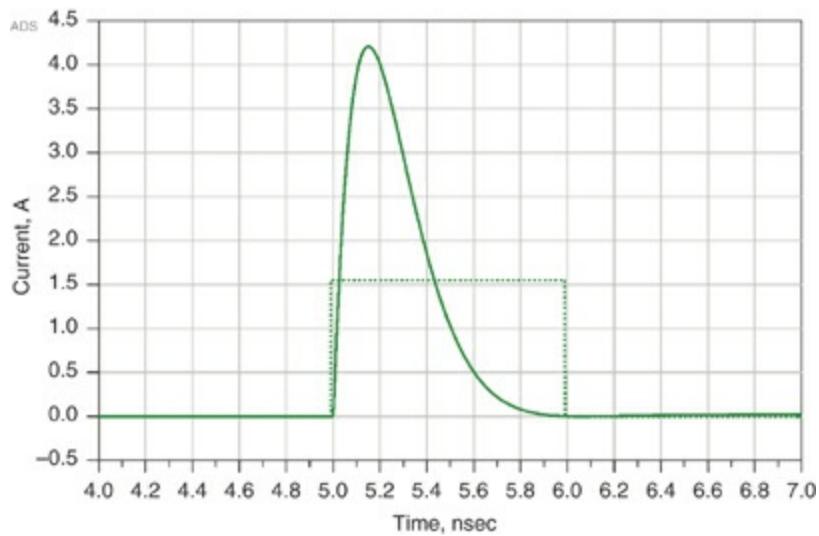
We use a bit sequence element at the top of the schematic to deliver the half-clock input waveform for the switch. The bit sequence shown in the schematic produces a current step response, but alternative sequences to produce the impulse and resonance responses are possible. There are five os in the sequence, which produce a quiet period for 5 nsec. Then the sequence begins to alternate 1s and os, which produces a square wave at half the 1 GHz clock frequency. On each edge of this square wave the PDN consumes a current impulse, which coincides with the rising edge of the 1 GHz clock.

The bit sequencer provides a convenient and easy way to deliver many desired patterns to the switched capacitor load. We either have an impulse at each clock

edge or we don't according to the bit sequence pattern. This is useful for simulating a class of PDN issues that involve clock manipulations. We demonstrate a technique for gradually increasing the charge consumed over several clock cycles in the next chapter.

Ammeters in several branches of the circuit topology enable us to observe the current in the switch, the current consumed by the load, the current delivered from the on-die capacitance, and the current delivered from the external PDN (from the VRM, through the board and through the package BGA balls).

Figure 9.34 shows a single current impulse. Also shown in the same figure is a square wave of current that is 1.55 A for 1 nsec. The area under both curves is 1.55 nC. The current begins with an input waveform transition at 5 nsec.



**Figure 9.34** Current waveforms generated in the switched capacitor circuit, showing the equivalent constant dynamic current for one clock cycle and the impulse of current from the switching of the capacitive load. This impulse diminishes to zero in a Poisson profile 1 nsec after being initiated by a half-clock pattern and is appropriate for a 1 GHz clock.

The circuit element L1 controls the shape of this curve with both inductive and resistive properties. If the L1 component were not there, current would have

immediately filled the load capacitors in an extremely short period of time. The current comes from the charge stored in the on-die capacitance charge reservoir, C<sub>3</sub>. Only the on-die resistance, R<sub>2</sub>, and the switch resistance stand between the charge reservoir and the switched load and by themselves would have allowed a huge inrush of current.

We empirically chose the inductance and resistance of L<sub>1</sub> to make the current waveform spread out over the whole clock cycle, 1 nsec in this case. We chose the RC time constant, tau, to be 1/4 of the system clock period. If we had chosen a smaller tau (1/10 of clock period), the current waveform would have been very tall and dropped off to zero long before the clock period was over, which would be the case if we were running the circuit at less than the maximum frequency. If we had chosen a larger tau, our circuits would still be drawing current after the clock cycle was over, which would have been the case if we did not meet set-up time. We chose the RC time constant so that the current drops to zero before the next clock edge.

The L<sub>1</sub> inductor is not a physical inductor in the die but rather is chosen to make the waveform ramp up properly. With zero inductance, the maximum current would have been a lot higher. It would have had a sharp peak immediately after the switch is closed. However, this does not happen in real product. A clock tree gradually draws more current from the PDN as the clock fans out. Maximum current is drawn shortly after the clock cycle is started and then it dwindles off to nothing as the clock cycle completes.

**Tip**

Commercial software is available to obtain the expected current waveform from the on-chip transistor design and interconnect parasitics, but it is expensive and complex. For the purposes of this simulation, we got a current impulse time profile by adjusting simple R and L parameters.

The current waveform's shape is important because it must be drawn through  $R_2$ . If the current ramps up too fast, the simulation shows a large voltage droop for the die circuits because of the  $R_2$  IR drop. The values of  $R_1$  and  $R_2$  are important. The sum of  $R_1$  and  $R_2$  form the 250 psec time constant discussed in Chapter 8.

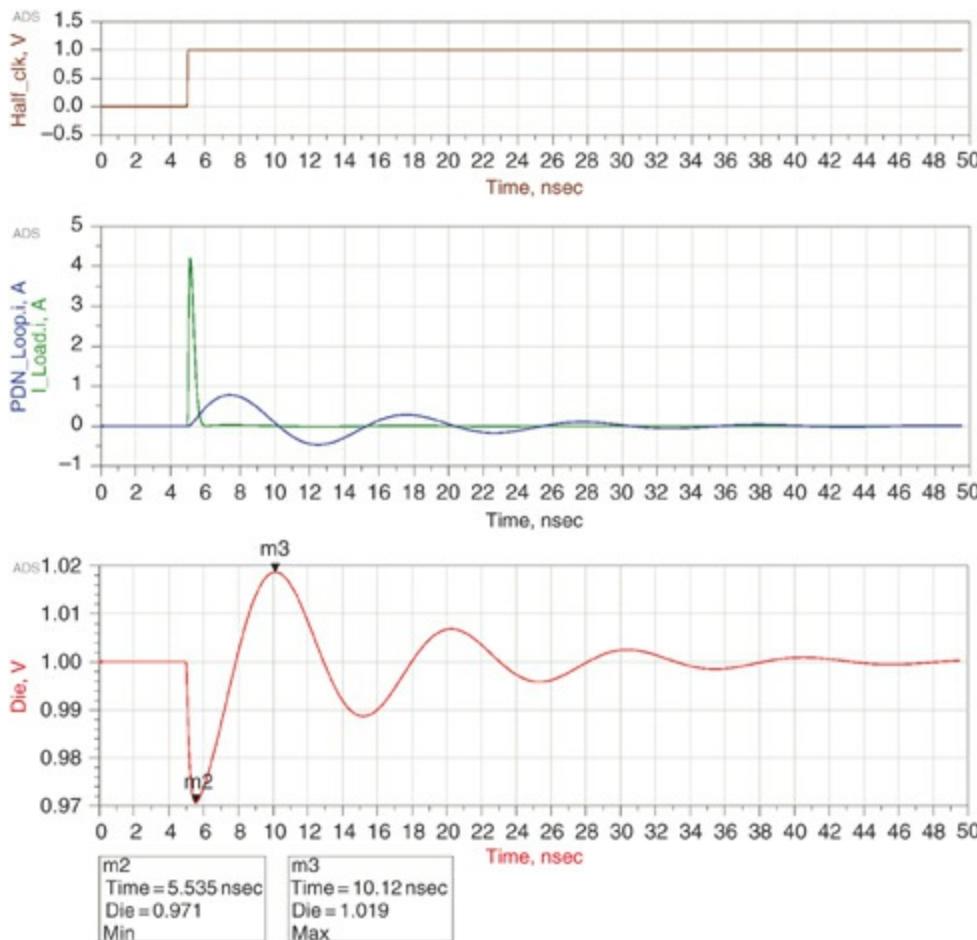
Determining the individual values of  $R_1$  and  $R_2$  by measurement is not possible.  $R_1$  generates DC IR drop and power loss for current coming in from the package.  $R_2$  generates IR drop for clock-edge noise. A reasonable assumption is to put 60% in the  $R_1$  position and 40% in the  $R_2$  position.

The chosen PDN circuit topology for simulation and the parameters applied to each dramatically affect the simulation results including voltage droops seen by the die circuits. All PDN simulators make assumptions for this topology and parameter distribution either explicitly or implicitly. Simulation results depend largely on the choices made for these assumptions. This circuit topology is obviously an extreme abstraction of the complex power grid and distributed capacitance found on a die. The intention is to focus on the interaction between the board, package, and on-die capacitance and account for an appropriate amount of damping.

### Tip

Obviously, this simple PDN and switched capacitor load circuit is an oversimplification of a complex distributed network. By working with this simple circuit, we gain much insight and intuition for dealing with software tools and complex database extractions. They all have the same issues and potential of widely varying results depending upon the assumptions we make. In any case, we chose parameters for this simulation that provide the expected results for PDNs with CMOS devices.

**Figure 9.35** shows the impulse response. The input waveform has made exactly one transition at 5 nsec. This is the same impulse as discussed in the previous section using a current impulse from a constant current source, but now we see the ringing decay for the PDN loop current and on-die voltage response with a capacitive load.



**Figure 9.35** Impulse response of the PDN circuit using a switched capacitor load. The impulse response is similar to the case in [Figure 9.18](#) using a constant current impulse.

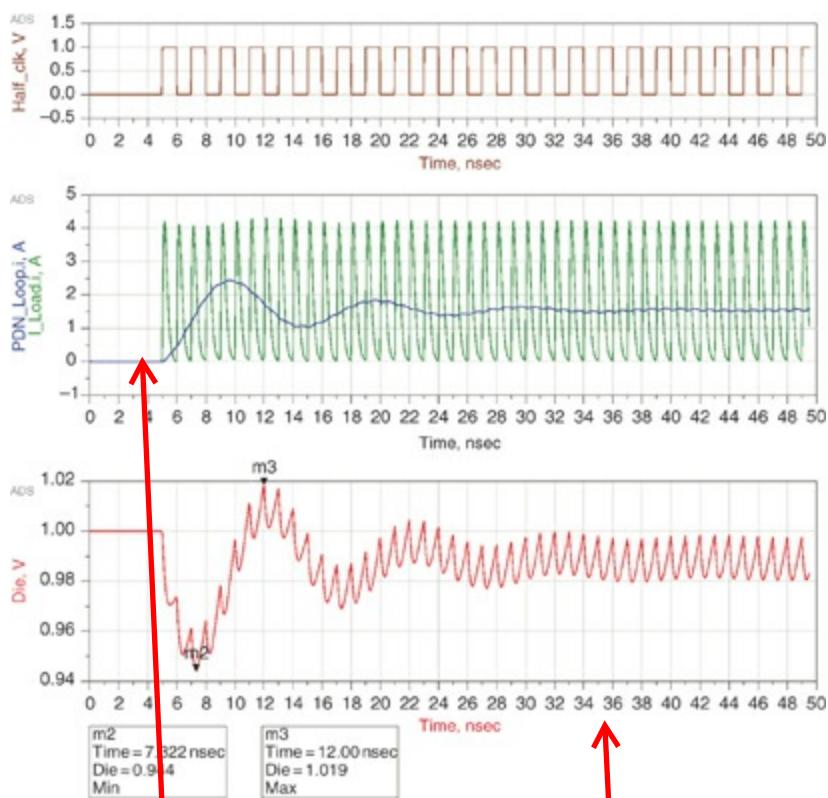
## 9.18 TRANSIENT CURRENT WAVEFORMS COMPOSED OF A SERIES OF CLOCK IMPULSES

These results are similar to those shown where we used a current source rather than switched capacitor load to draw the PDN current. The simulated droop of  $1.000 - 0.971 = 29$  mV is close to the calculated 31 mV:

$$\Delta V_{\text{clock edge}} = \frac{Q_{\text{clk-edge}}}{ODC} = \frac{1}{ODC} \frac{I_{\text{dynamic}}}{f_{\text{clock}}} = \frac{1}{50 \text{nF}} \frac{1.55 \text{A}}{1 \text{GHz}} = 31 \text{mV} \quad (9.45)$$

The difference is because a small amount of charge came in from the PDN inductance during the 1 nsec time period when the circuits consumed the charge.

Figure 9.36 shows the step response created by the switched capacitor load. We can compare this to the case of a constant current source used to draw a simple square step function of current. The top of the figure shows the input waveform, which is a half-clock for the 1 GHz system clock. As shown in the second panel, the half-clock has drawn a current impulse on each half-clock edge. The tops of the current impulses are not at the same value because the current changes slightly as a function of PDN voltage.



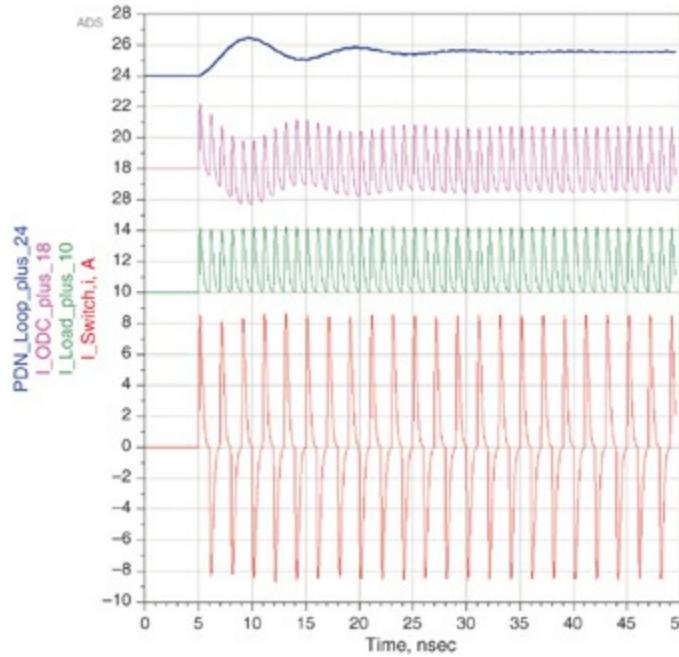
**Figure 9.36** PDN response for a step current from a switched capacitor load. The top graph shows a half-clock driving the switch, which is half the clock frequency. The middle graph shows the current impulses drawn by the switched capacitor load on the rising edge of each full-CMOS clock cycle and the current flow through the package from the system PDN. The bottom trace shows the voltage noise on the die.

The same second panel shows the PDN loop current from the package. The on-die capacitance together with the PDN loop inductance forms a low pass filter. The clock-edge noise is almost completely filtered out of the loop current coming in through the BGA pads.

The bottom panel shows the on-die capacitance voltage-noise waveforms that the on-die circuits see. The clock-edge noise is clearly visible. The envelope is the expected step response. The  $1.000 - 0.944 = 56$  mV droop is a little more than we predicted for the step response because clock-edge noise is superimposed upon the step response:

$$V_{\text{step}} = I_{\text{step}} \times Z_0 = 1.55 \text{ A} \times 32 \text{ m}\Omega = 49 \text{ mV} \quad (9.46)$$

Figure 9.37 shows currents in different branches of the switched capacitor load topology. The waveforms have been offset so we can see them better. The bottom waveform is the switch current. It goes in both the positive and negative direction because current flows both ways through the switch. It is also double in magnitude because we are charging up one of the load capacitors at the same time we discharge the other load capacitor.



**Figure 9.37** Current waveforms in other branches of the PDN circuit. Waveforms have been offset for better visibility and should be considered 2 A per division like on a scope. **Top trace:** Current coming in from the BGA and the board-level PDN. **Second from the top:** Current through the on-die decoupling capacitance. **Third from the top:** The current through the on-die PDN rail from the capacitive load. **Bottom trace:** Current through the switch that charges or discharges the capacitor load.

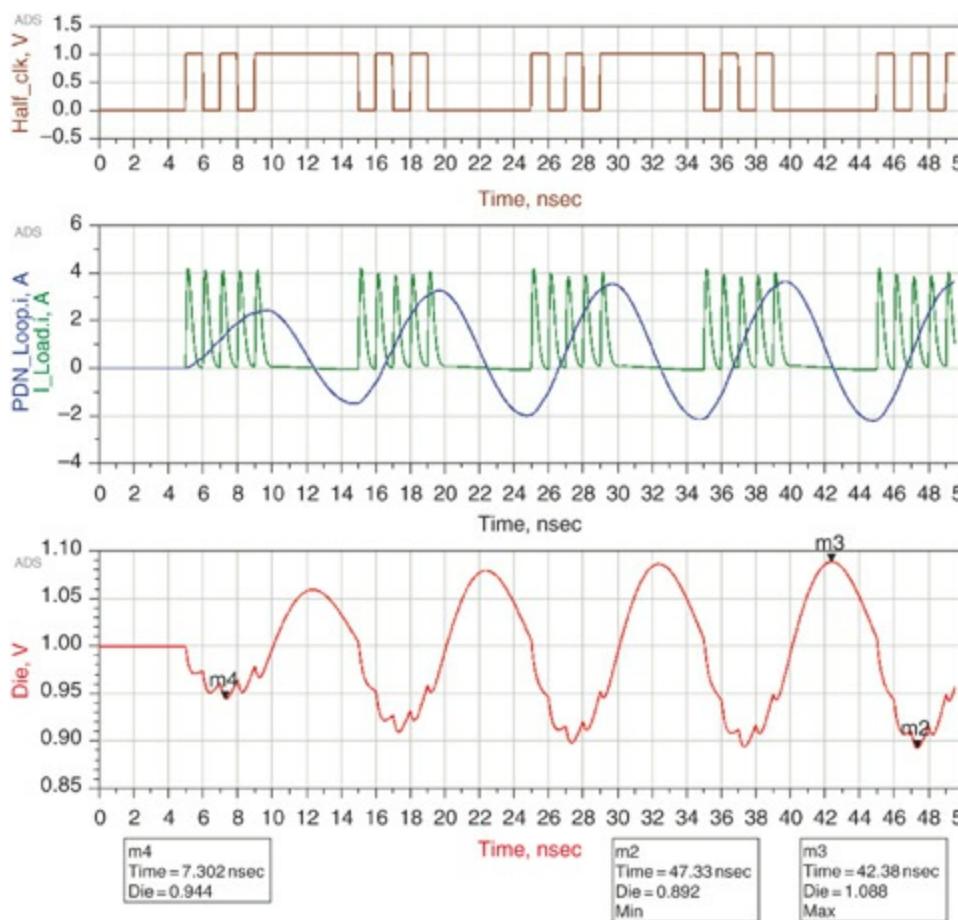
The second waveform from the bottom is the load current flowing from Vdd to Vss on-die PDN rails and is the same as shown Figure 9.36. It is well behaved with each clock cycle responding to the PDN voltage with a slightly varying amplitude.

The third waveform from the bottom is the on-die

capacitance current. Clearly it is supplying the spiky clock-edge current consumed by the load. It also has the lower frequency damped sinusoid current associated with the impulse response of the PDN resonant loop.

The top waveform is the BGA bump loop current that flows into the die from the package. The Bandini Mountain's LC low pass filter has filtered out nearly all waveform spikiness. The sum of the BGA bump loop current and the on-die capacitance current is simply the load current. This is a simple application of Kirchhoff's current law that says the sum of currents into a node is zero.

Figure 9.38 shows the resonance response generated by the switched capacitor load. We can compare it to the simulation in Figure 9.22 where a constant current source load was used to generate a similar response. The top panel shows the input pattern with the edges that have drawn the current impulses. The second panel shows the current resonance building up. With more noise on the PDN, the changes in current impulse height become a little more obvious.



**Figure 9.38** Current response for a resonant square wave of clock pulses. **Top:** The bit pattern into the switch to emulate this worst-case switching pattern. **Middle:** The clock-edge current impulses with a 50% duty cycle and repeat frequency of 100 MHz to drive the 100 MHz impedance peak resonance. **Bottom:** The voltage noise on the die pads, growing with each cycle.

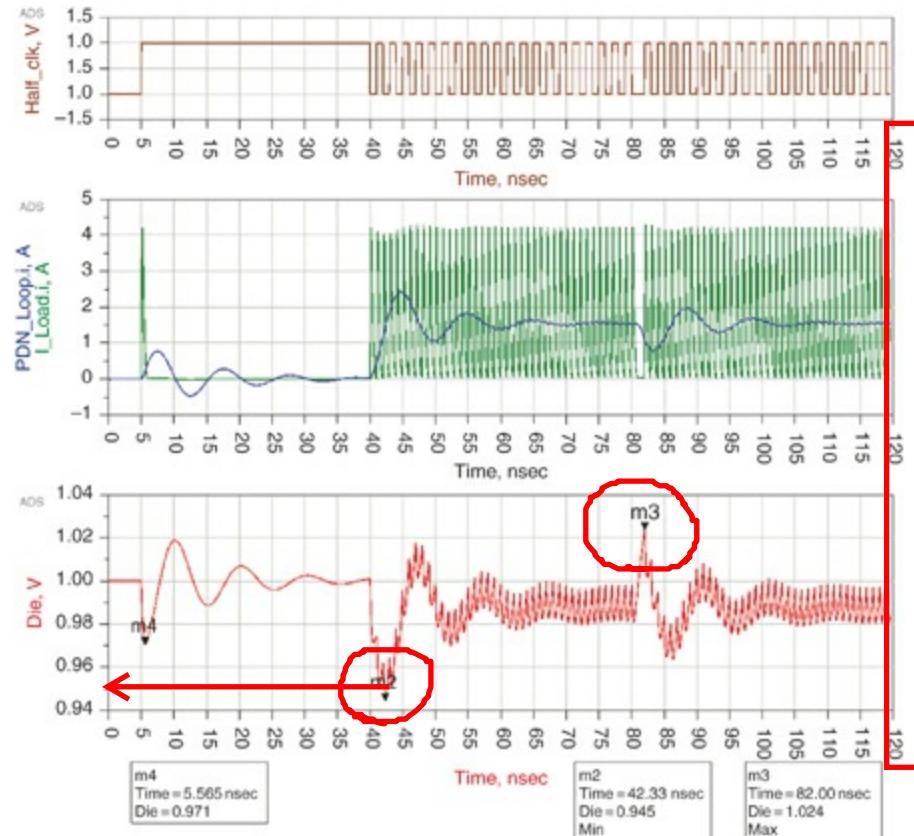
The bottom panel is the voltage response on the die pads. It takes about three resonant periods for the amplitude to grow to a maximum because the q-factor is a little over 3. The peak-to-peak noise is  $1.088 - 0.892 = 196 \text{ mV}$ , which is just slightly less than the predicted result even though clock-edge noise is superimposed upon it:

$$V_{\text{pk-pk}} = \frac{4}{\pi} I_{\text{transient}} Z_{\text{peak}} = \frac{4}{\pi} 1.55 \text{ A} \times 100 \text{ m}\Omega = 198 \text{ mV} \quad (9.47)$$

The switched capacitor load provides a little more damping than a constant current source load that measured out at 201 mV peak to peak for the same PDN.

Figure 9.39 shows a bit sequence that reveals the impulse, step, and anti-impulse responses for easy comparison all in one simulation. The anti-impulse is from a missing current impulse. It is similar but the opposite of the impulse response.

simulate clock gating



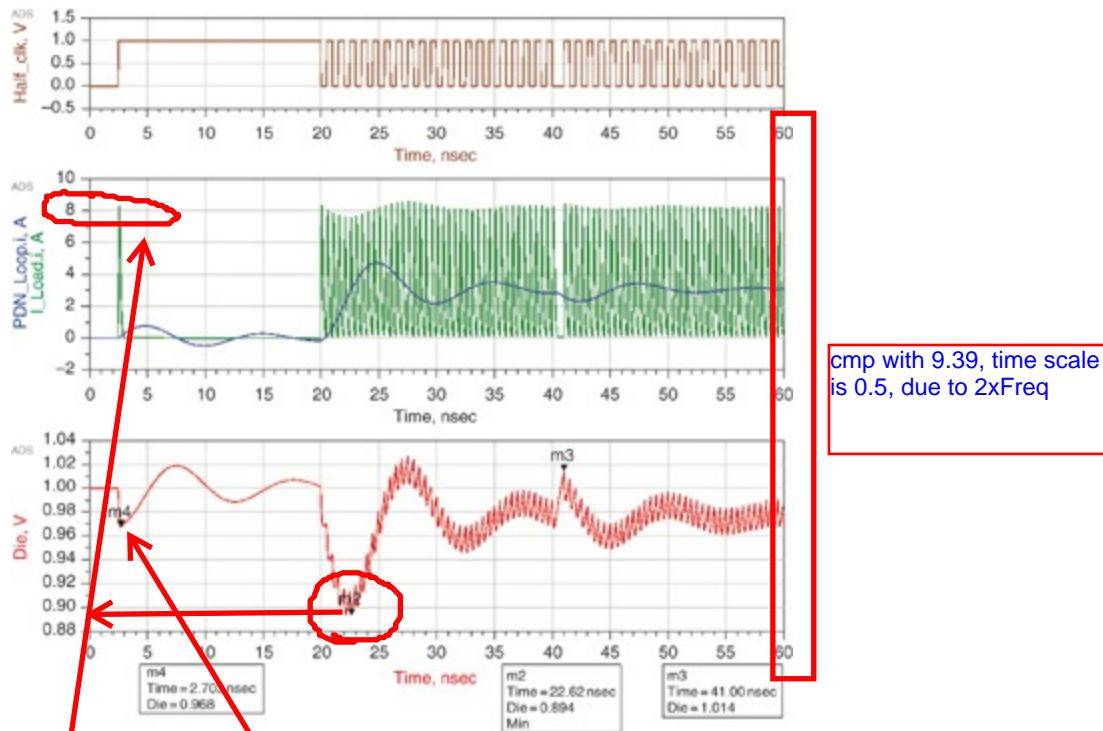
**Figure 9.39** Combination of the single clock-edge impulse, the steady-state impulse train, and the case of a missing clock edge. **Top:** The bit pattern into the switch controlling the capacitor load. **Middle:** The current flow through the on-die PDN and the BGA balls from the board-level PDN. **Bottom:** The voltage noise on the die pads.

Prior to the anti-impulse, PDN current had settled down to a constant 1.55 A. All of a sudden, there was a missing clock edge. The die failed to consume the current that was already coming in from the package inductance. The charge has nowhere to go so it charges up the on-die capacitance with similar amount of charge that the original impulse response consumes. The result is an on-die capacitance voltage spike and PDN damped sinusoid ringing that is nearly opposite that of the

impulse response. This simulation gives a hint about how dangerous clock swallowing is for PDN noise.

Figure 9.40 shows what happens if we take the same circuits and double the clock frequency from 1 GHz to 2 GHz. The RLC parameters for L1 ( $L_{\tau}$ ,  $R_{\tau}$ ) have automatically adjusted so that all the clock-edge charge is consumed in the shorter clock period. This means that the current impulse is taller and narrower. The capacitive loads are the same so the clock-edge current impulse consumes the same charge but it happens twice as often so the dynamic current has doubled.

taller means larger current, due to higher freq x same charge per cycle



**Figure 9.40** Same switched capacitor load but at twice the clock frequency. The current impulses are taller and narrower so that the same charge is consumed per impulse; therefore, the impulse response is the same. The dynamic current has doubled because there are twice as many impulses in the same amount of time.

The impulse and anti-impulse waveforms have not changed because they have the same charge. Therefore, they have the same droops and spikes as with the 1 GHz clock. However, the step response has doubled because the dynamic current has doubled. The predicted step

response droop is

$$V_{\text{step}} = I_{\text{step}} \times Z_0 = \underline{\underline{3.10 \text{ A} \times 32 \text{ m}\Omega = 98 \text{ mV}}} \quad (9.48)$$

The measured droop is  $1.000 - 0.894 = 106 \text{ mV}$  because the clock-edge noise is superimposed on the step response.

## 9.19 ADVANCED SECTION: APPLYING CLOCK GATING, CLOCK SWALLOWING, AND POWER GATING TO REAL CMOS SITUATIONS

The previous several figures show the effects of clock gating. At about 2 nsec into the simulations, we see the effect that a single clock pulse has on the PDN. It is the same as the impulse response from clock-edge noise.

When a clock is abruptly gated on, we see the step response signature shown at about 20 nsec. The PDN voltage droops to a voltage that is approximately the transient current times the characteristic impedance of the PDN's Bandini Mountain. This is not a problem for a PDN impedance peak where the characteristic impedance meets target impedance. It is a problem for a PDN where the characteristic impedance is a factor of two above the target impedance. It suffers a voltage droop that is twice the voltage tolerance when the clock is gated on.

### Tip

APDN in which the characteristic impedance meets the target impedance is able to sustain a full transient current step. When the clock is abruptly gated on, the PDN stays within the voltage tolerance. PDN designs where the characteristic impedance substantially exceeds the target impedance will have trouble with these transients.

The resonance response is stimulated by clock gating in a repetitive manner that stimulates the PDN resonant peak to the fullest extent. The PDN voltage response is

generally well behaved as long as the q-factor is not more than 1.6 for a PDN with a single impedance peak.

Pulse swallowing is a form of clock gating and has become a popular way to manage overcurrent and thermal situations. The simplest example of this is the anti-impulse response shown at about 40 nsec. A single clock pulse has been swallowed by clock gating and is quite disruptive to the PDN.

Figure 9.41 is an example where the clock is gated to half-frequency and then to full-frequency. The clock is gated on to 100% at about 10 nsec, cut to half-frequency by swallowing every other clock pulse at about 50 nsec and brought back to full-frequency at about 100 nsec.

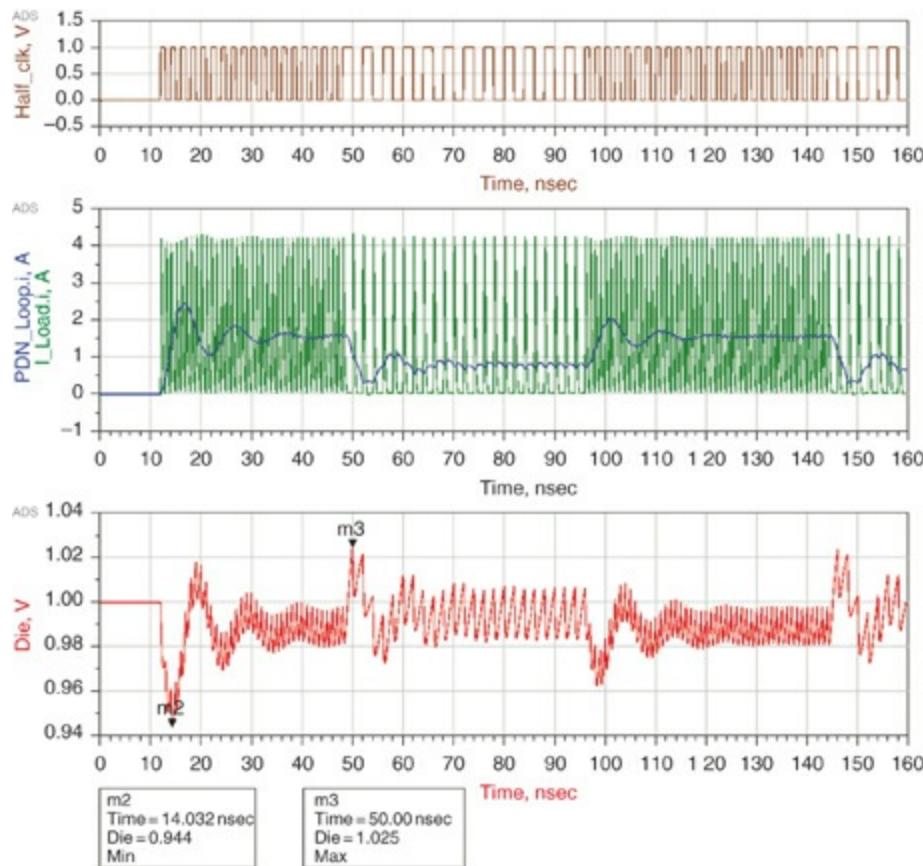


Figure 9.41 Waveforms in which the clock frequency is modulated, first at full-frequency, then half-frequency, then at full-frequency by using clock swallowing techniques. The modulated clock frequency modulates the dynamic current and we see a partial step response in the on-die PDN voltage.

The PDN voltage excursions behave as expected. The

full-clock nominally brings 50 mV or 5% droop; shifting to half-clock brings 25 mV or 2.5% overshoot; and going back to full-clock from half-clock brings a 2.5% droop.

Clock-edge noise riding on top of the underlying current transitions causes the high-frequency droops to be a little more than this. The switched capacitor load, which mimics the behavior of CMOS circuits, demonstrates these fundamental effects with the effects of changes in damping included.

Figure 9.42 shows some more detail on clock swallowing. The 1 GHz clock is gated on at 12 nsec and the PDN suffers the familiar clock gate droop. At about 48 nsec, one out of four clock pulses are swallowed. This is represented by the clock swallowing pattern of 111011101110. The PDN voltage suffers the familiar anti-impulse response with the first missing clock pulse. It then settles down to a steady-state situation with the peak-to-peak noise almost twice as big as it was with 100% clock.

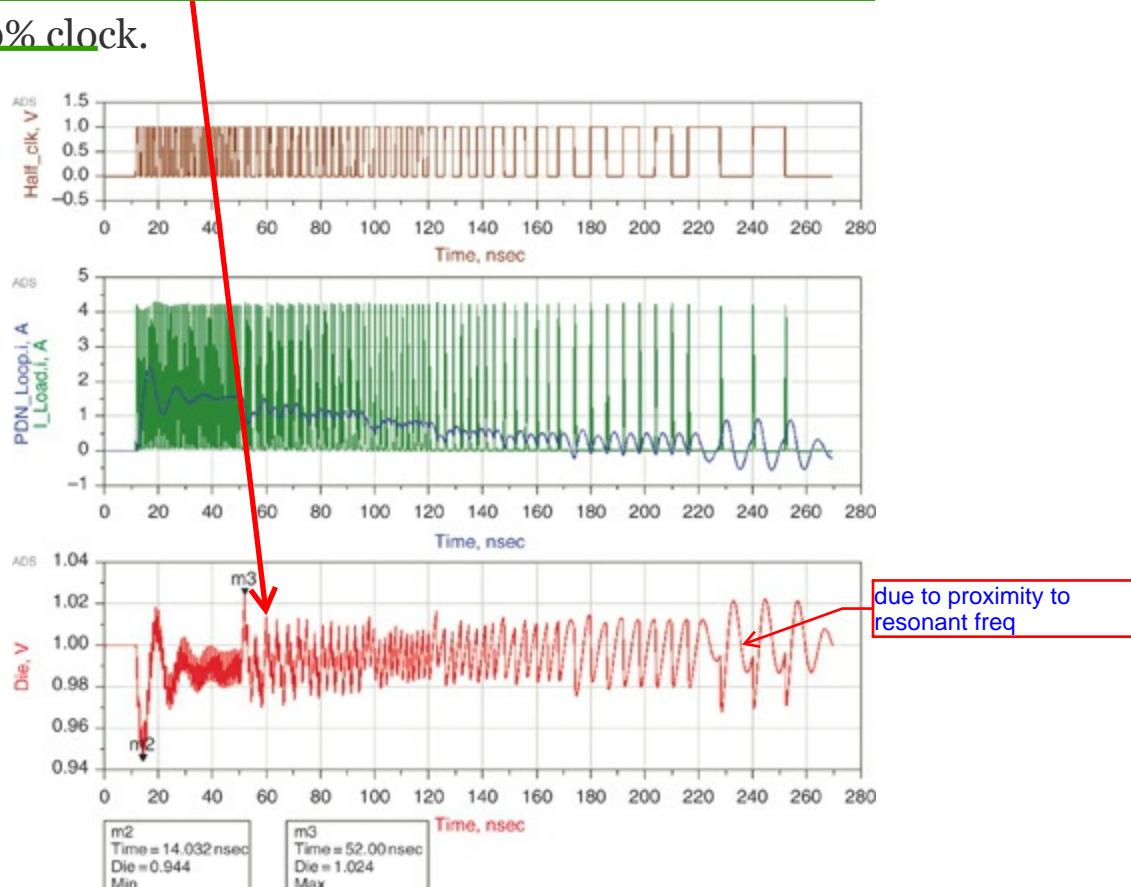


Figure 9.42 Waveforms when the clock is modulated by swallowing different number of clock pulses.

At 72 nsec, the clock swallows one out of three clock pulses, which is represented by 110110110110 pattern. Continuing on at

- 96 nsec: the clock swallows 1/2 the clock pulses with the 101010101010 pattern
- 120 nsec: the clock swallows 2/3 of the clock pulses with the 100100100100 pattern
- 144 nsec: the clock swallows 3/4 of the clock pulses with the 100010001000 pattern
- 168 nsec: the clock swallows 5/6 of the clock pulses with the 100000100000 pattern
- 216 nsec: the clock swallows 11/12 of the clock pulses with the 100000000000 pattern

The 12-bit pattern is useful because it gives a rich selection of lower power states, but clearly there is an impact on PDN performance with erratic clock pulses. The final pattern with a 1/12 subharmonic (83 MHz) is close to the 100 MHz PDN resonant frequency. The power transients reduce with lower clock frequency. The PDN response might be better or worse depending on the impedance peak's q-factor. In this case, the power transients reduce by a factor of 12, and the impedance profile is the same as it always was, but we see substantial peak-to-peak noise in the time domain. We have entered into a steady-state stimulation of the resonance at greatly reduced power. Clock-edge noise is more prominent after current has relaxed in the inductor because of the longer time period between clock edges.

**Tip**

As demonstrated by this example, clock swallowing is quite disruptive for the PDN. It essentially causes abrupt transient currents that occur very quickly, in essentially one clock cycle. At this level, just looking at transient current is not sufficient. Accurately predicting the PDN performance requires a simulation that involves the PDN resonant peak in the frequency domain and a sequence of current impulses that comes with the rising clock edge in a time domain analysis. The switched capacitor load is well suited for this.

The specific details of the clock pulse history and the exact timing of the next clock pulse are important. The PDN essentially has memory and stored energy from the recent past. Our PDN has a resonant frequency that is 100 MHz with a 10 nsec period. The time constant for the PDN is

$$\boxed{\tau = \frac{1}{\omega} = \frac{1}{2\pi f_0}} = 1.5 \text{ nsec} \quad (9.49)$$

Several time constants must transpire before the PDN comes to steady state. The 1 GHz clock (1 nsec period), is on a similar time scale as the PDN time constant. This explains why clock swallowing is so disruptive to PDNs and the exact sequence and timing of clock pulses is very important in predicting PDN noise with clock activity. With higher clock frequencies (2 GHz, 5 GHz, 10 GHz, and so on) there are many clock cycles in the PDN time constant and each individual clock cycle becomes less disruptive.

Once again, a PDN with an impedance peak that meets target impedance, or at least has a characteristic impedance that meets target impedance, is marginally or reasonably robust for clock gating and clock swallowing events.

**Tip**

APDN that is not robust becomes highly vulnerable to clock manipulations, which cause substantial fast transient current events. The switched capacitor load is well suited for simulation of clock manipulations because it consumes current impulses that change according to the PDN voltage, which often has a profile that varies with time for these events.

## 9.20 ADVANCED SECTION: POWER GATING

We can analyze power gate function as a special case for the switched capacitor load. To save power, entire power domains are often collapsed to zero volts by using a power switch or power gate.

**Tip**

We use clock gating to reduce the dynamic power to zero and power gating to eliminate even the leakage current. This is important in battery-powered applications where a product might spend much of its life in an extremely low power mode and then be brought to life whenever high performance is expected.

For the power gate problem, there is usually some always-on circuitry upstream of the power gate switch and some sometimes-on circuitry downstream of the power gate switch that we can either power up or down. Capacitance is associated with both the upstream and downstream domains. Generally, the circuitry upstream of the power gate switch needs to continue functioning at full-speed without interruption. The power gate problem is to raise up the voltage on the downstream domain without disrupting the circuits functioning on the upstream domain.

When the power gate switch is abruptly closed, current rushes in from the upstream side to the downstream side very quickly and is often called **inrush current**. A certain amount of charge is stored in the upstream capacitance. This is all the energy we have on the die to use during the power gate operation.

If a low-resistance power gate switch is abruptly closed, charge sharing occurs between the upstream and downstream nodes. This might happen in less than 1 nsec and there is not sufficient time to bring in charge from the external PDN to the die. The package inductor is high impedance and blocks current from coming in from the outside world for a short duration of time. The charge that is in the on-die capacitance, upstream of the switch, is immediately shared with the on-die capacitance downstream of the switch. Simple charge-sharing equations reveal that if the downstream capacitance is the same as the upstream capacitance,  $C_{up} = C_{down}$ , the on-die voltage drops in half when the switch is closed.

The amount of charge before and after switch closure is

$$Q = C_{up} \times V_{dd} \quad (9.50)$$

The final voltage after switch closure is

$$V_{dd+} = \frac{Q}{C_{up} + C_{down}} = \frac{C_{up} \times V_{dd-}}{C_{up} + C_{down}} = V_{dd-} \frac{C_{up}}{C_{up} + C_{down}} = \frac{V_{dd-}}{2} \quad (9.51)$$

where:

$C_{up}$  is the upstream capacitance

$C_{down}$  is the downstream capacitance

$V_{dd-}$  is the voltage on the upstream capacitance before the switch

$V_{dd+}$  is the voltage on the upstream and downstream capacitance after the switch

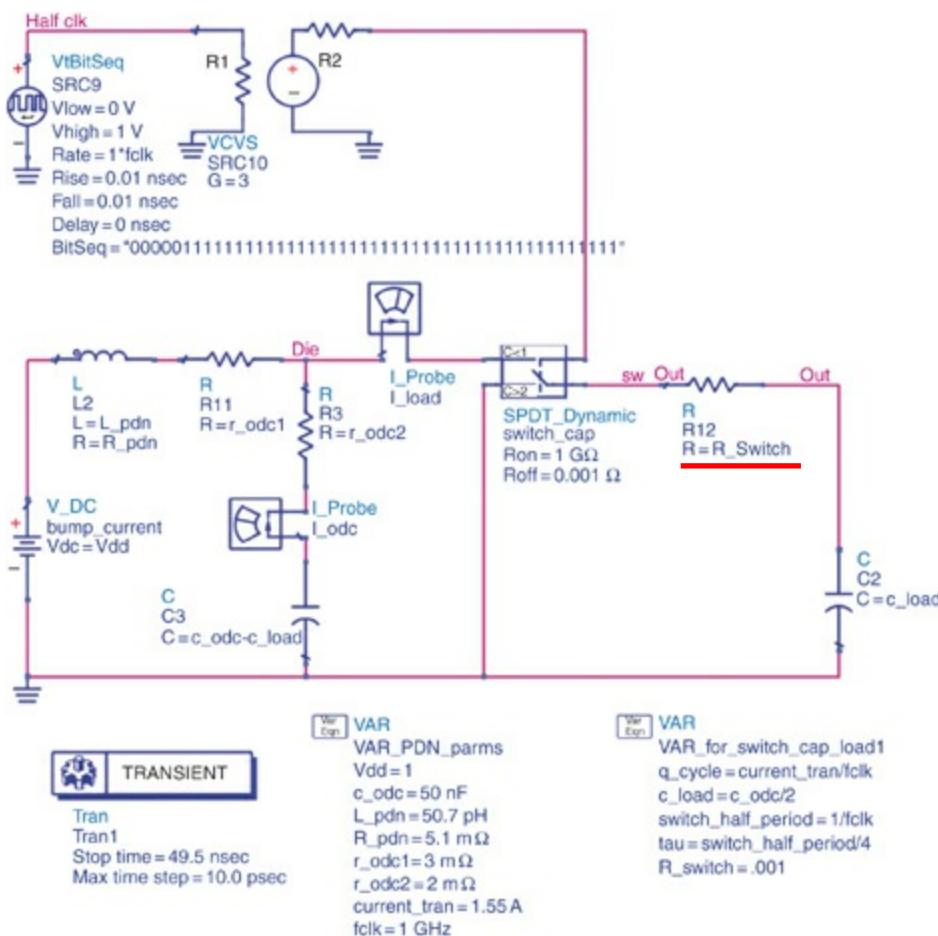
And this assumes the special case of  $C_{up} = C_{down}$

The circuits in the always-on domain upstream of the power gate switch have their PDN voltage momentarily cut in half. This will most likely have a devastating effect on the circuit timing and might cause a functional

failure.

The impact on the PDN voltage rail is simulated for power gating using a schematic similar to clock gating, shown in [Figure 9.43](#). This is the same basic PDN topology as used in the switched capacitor load. We have used similar parameters so that the PDN impedance peak and resonant frequency are the same. The difference is that the load capacitance is only to ground (not to Vdd) and has been substantially increased. There is 25 nF upstream of the power gate and 25 nF downstream.

no longer a CMOS switching model

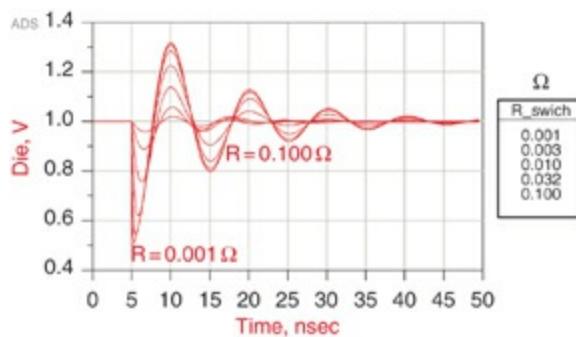


**Figure 9.43** Schematic used to simulate the impact from power gating. The load capacitance is now the downstream on-die capacitance, which is suddenly switched into the rest of the powered part of the die.

Figure 9.44 shows the simulation results for several values of the switch resistance,  $R_{\text{switch}}$ . When the switch resistance is  $1 \text{ m}\Omega$ , the PDN voltage upstream of

the power gate droops to approximately 0.5 V, half of the nominal PDN voltage as predicted. The PDN rings out in the familiar impulse response associated with the resonant peak. This simulation has several values for  $R_{\text{switch}}$  ranging from  $0.001 \Omega$  to  $1 \Omega$  in a logarithmic progression.

The optimum value of resistance depends on the capacitance upstream and downstream of the power gate switch. With more resistance there is always less voltage droop but longer charge up time. Generally, we should size the resistance with the PDN time constant and PDN resonant frequency to make sure the package inductor brings charge in from the outside world instead of the power gate consuming all the charge from the upstream capacitance.



**Figure 9.44** Voltage on the upstream rail when we connect the downstream part of the die with different values of series resistance. Note the ringing noise from the rest of the off-chip PDN circuitry.

Clearly, the impact on the always-on, upstream side of the power gate is much less, about 16 mV, when the switch is  $1 \Omega$  compared to 500 mV when the switch is  $1 \text{ m}\Omega$ .

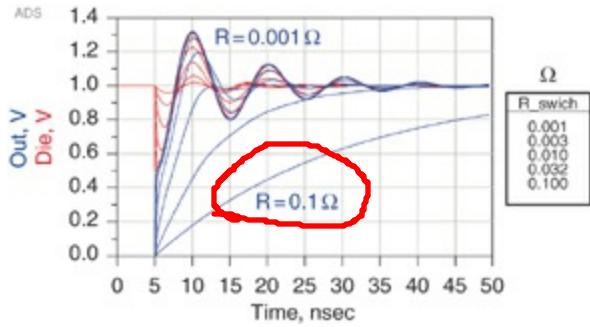
essentially larger  
 $Z_{xy}$ , better isolation  
btw up/down stream  
sides

#### Tip

The higher the switch resistance, the less inrush current it draws. The upstream PDN voltage is well behaved with more power gate resistance and circuits in the die's upstream section are able to function normally.

Figure 9.45 shows the voltage on both the upstream and downstream sides of the power gate. Clearly, the rise time on the downstream node is much slower with higher switch resistance as expected. There is a clear tradeoff between noise on the upstream side and time delay for the rise time on the downstream side.

less noise on upstream side, means charge would need to wait for L\_pkge, hence slower delay for downstream rise time



**Figure 9.45** Voltage noise on the upstream part of the die and at the output of the switch connecting the downstream part of the die for different series resistance values in the switch.

The keys to managing the PDN noise on the upstream side of the power gate and latency on the downstream side are the **time constants**. Impedance peak frequency determines the reactive PDN time constant. The impedance peak is at 100 MHz, the resonant period is 10 nsec, and the reactive time constant is

$$\tau = \frac{1}{\omega} = \frac{1}{2\pi f_0} = \sqrt{LC} = 1.58 \text{ nsec} \quad (9.52)$$

time constant is the exp coefficient, for RC: exp (-t/RC), for EM wave: exp (-omega\*t - kz), hence 1/omega is the time constant

With low q-factor (close to 1) several time constants must transpire before the PDN comes close to equilibrium. This is how long it takes to fully ramp up the current in the inductor. With higher q-factors, close to 3 in this case, we must wait much longer, three times the resonant period, which is  $3 \times 2\pi = 19$  time constants before the PDN comes close to equilibrium.

The objective is to have the power gate draw charge (current) from the upstream side slow enough that the external PDN can provide the current rather than draw

charge from the upstream capacitance.

**Tip**

This means that the RC time constant of the power gate switch  
should be much longer than reactive PDN time constant.

**Table 9.6** shows the calculations for the reactive PDN time constant as well as the resistive RC time constant associated with power gate switch resistance and downstream capacitance.

Time Constants for Power Gating							
Inductance	50						pH
Capacitance	50						nF
Reactive time constant sqrt (LC)	1.58						nsec
R	0.001	0.003	0.01	0.032	0.1	0.3	1
Resistive time constant (RC)	0.025	0.075	0.25	0.8	2.5	7.5	25
							nsec

**Table 9.6** Elements of a spreadsheet used to estimate the series resistance of the power gating switch to match time constants to the rest of the PDN.

Usually the reactive PDN time constant is strongly set by board and package inductance and on-die capacitance considerations. It then becomes a matter of power gate circuit design to slow the inrush current down sufficiently so that the PDN voltage on the upstream side of the switch stays within tolerance. The curves in **Figure 9.45** and **Table 9.6** suggest that we should make the RC time constant at least 20 times the reactive PDN time constant. In this example we have managed inrush current by means of resistance. Other possible ways include turning on a sequence of small switches spaced out in time for optimum performance.

## 9.21 THE BOTTOM LINE

1. The target impedance is the most important design

metric for the PDN. With a well-established target impedance, which requires substantial knowledge of the transient current, we can make the best cost and performance trade-offs.

2. When obtaining accurate values for the transient current draw of the PDN is not possible, as a rough approximation, using a value equal to one-half the maximum current is a reasonable starting place.
3. The current draw of the PDN consists of impulses of current (charge) consumed on each clock edge. We see the PDN voltage response to these current pulses at the on-die voltage rails, but it is usually filtered out into a slower rising edge transient current at the board level by the on-die capacitance and package lead inductance.
4. The voltage noise on the die is not driven by  $L\frac{di}{dt}$  but by voltage droop in the on-die decoupling capacitance. This creates  $V/L$ , which drives the  $di/dt$  through the inductive portion of the PDN. A large  $di/dt$  is associated with low inductance and is a good thing because it restores the depleted charge in the on-die capacitor and reduces the duration of the PDN noise.
5. Three current waveforms demonstrate fundamental PDN noise profiles under specific cases: a single clock-edge impulse, a step response, and a periodic resonant response. We predict the properties of the PDN responses to these three current loads with a simple model of the PDN.
6. An important condition for engineering a marginally or reasonably robust PDN is to keep the characteristic impedance of any peak below the target impedance. This ensures the voltage response to a step transient current never exceeds the PDN tolerance spec.

7. For a fully robust PDN, the peak impedances should not exceed the target impedance. For a marginally robust and cost-effective PDN, the characteristic impedances should not exceed the target impedance.
8. A switched capacitor load model is better to use than a constant current source. It draws a current that is proportional to PDN voltage and provides damping. We can explore the PDN response for many aggressive conditions, such as clock gating, clock swallowing, frequency manipulations, and power gating, using the switched capacitor load.
9. Although rogue waves are an interesting phenomenon, their likelihood is extremely low. By engineering a flat impedance profile, or at least having low q-factor peaks, rogue waves cannot build up. They only need to be considered in cases where extremely high reliability is required from the PDN.
10. Power-saving techniques such as modulating the clock frequency, swallowing clock pulses, and the die's power-gating regions put strain on the PDN by increasing the transient currents. The lower power consumption offered by these techniques requires lower PDN impedances. They come at the cost of either more expensive PDN designs or higher risk of PDN noise exceeding tolerance requirements.

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# Chapter 10. Putting It All Together: A Practical Approach to PDN Design

In this last chapter, we pull together the concepts and design principles introduced throughout this book to walk through a few specific case studies. Of course, every design is custom. Although the specific details of the transient currents, the features of the on-die capacitance, and package lead inductance will vary, the design principles and the design flow is the same.

We've introduced the essential principles as a solid foundation to understanding how physical design influences the electrical performance. We've shown the three most important transient current waveforms that stimulate the voltage noise on the PDN and the features in the frequency domain impedance profile that affect the noise features in the time domain.

Now, we look at balancing the design tradeoffs with a practical and efficient process to get to an acceptable design quickly.

## 10.1 REITERATING OUR GOAL IN PDN DESIGN

The goal in robust and cost-effective PDN design is to engineer a power distribution system that results in voltage levels on the die within specifications under operating conditions at lowest cost.

A fully robust PDN design means maintaining acceptable voltage levels under *all* possible operating conditions, running all possible code. This is important in aircraft, spacecraft, life support, and autopilot systems where failure is not an option. A fully robust PDN is the most expensive type: leveraging more components; more board layers; more expensive

materials; more expensive measurement and simulation tools; and longer design, analysis, and test times.

A reasonably or marginally robust PDN means meeting the voltage specifications under a wide range of operating conditions, but accepting the risk of failure in rare, worst-case situations. Of course, this notion of a “reasonably robust” PDN is a vague term based on meeting an acceptable level of risk. A reasonably robust PDN costs less to implement.

**Tip**

Every PDN is unique and tells its own story. The constraints, performance, cost, and risk targets are different for each design. This means we must analyze each PDN to find the right set of tradeoffs for that specific application.

The challenge is to quickly and efficiently explore the design space to find acceptable values for all the important design features that results in either a robust or cost-effective PDN. The general strategy involves a three-step process:

1. Leverage engineering judgement, rules of thumb, and simple approximations and estimates to establish a first-pass design proposal. Identify the important input design parameters and their effect on output performance parameters. Use this information to provide general design guidelines so we know which parameters are important and in which direction to move them to meet the design goals. Select a reasonable starting value for each important design parameter based on the design guidelines and the cost and manufacturing constraints. In other words, do everything possible that is free, reasonable, and quick to reduce PDN noise.
2. Leverage a linearized spreadsheet-based model to

optimize PDN parameters. Quickly iterate on tradeoffs that affect system-level performance to arrive at a second-pass design proposal. This takes longer but results in higher confidence that the final design is reasonably robust.

3. Leverage sophisticated field solver models and time and frequency domain circuit simulations to verify and further optimize the design parameters. The more accurate the models included, the higher the confidence in the final simulation and the lower the risk. Evaluate the noise performance compared to tolerance limits. Evaluate the design margin compared to the acceptable risk and the cost. This design and analysis approach takes longer and is more expensive but reduces uncertainty and risk.

Regardless of the approach, we always have the option to “overdesign” the PDN, effectively paying extra for insurance to supplement uncertainty in the predicted results. This might be because of input information that is poorly known. Having complete starting information reduces both our uncertainty and the need for costly insurance.

**Tip**

Always consider the option to pay more for an “overdesigned” product, effectively buying insurance to reduce the risk.

We've already introduced many power integrity principles to implement these processes and reach design goals throughout this book. In this chapter, we pull together and summarize the important principles. We introduce a linearized spreadsheet model to explore the tradeoffs in design space. Finally, we apply this analysis approach using examples that illustrate

features in PDN design that improve performance at reasonable cost.

## 10.2 SUMMARY OF THE MOST IMPORTANT POWER INTEGRITY PRINCIPLES

We evaluate PDN design first by looking at the frequency domain impedance profile from the chips' perspective. However, the frequency domain is not the whole picture and time domain analysis is also important. Assuming the PDN is linear, time invariant, and passive, the analysis in the frequency and time domains provides the same information.

Two special portions of the PDN are not linear and time invariant and technically invalidate frequency domain analysis. One is a switched mode power supply (SMPS) where the circuit topology changes with time and the effective output impedance changes with the load. The other is the on-die circuits that change capacitance with switching activity and current load in time. To most accurately simulate these portions of the PDN, a transient simulation is essential.

However, frequency domain simulation is so valuable that we conjure up some moderately accurate linear models for the non-linear PDN portions so that we can evaluate the rest of the system. The SMPS is represented by a few linear elements and enables us to connect a constant voltage source to the rest of the PDN. Load current consumed by capacitive circuits switching in time on the die behave like a linear damping resistance and can be averaged and represented in the frequency domain.

From the maximum time averaged current that flows through the die during the most aggressive micro-code operations and the maximum tolerable voltage noise on the power rail, we establish a **target impedance**. If we

engineer the PDN impedance everywhere to be below this target impedance, the PDN voltage will be fully robust and almost certainly within the voltage tolerance limits.

**Tip**

It is desirable to meet the PDN target impedance across the broad frequency range; however, it may be exceeded at certain peak frequencies. Peaks influence the step response and the resonant-driven response. A marginally robust PDN has the  $Z_0$  of all peaks below target impedance. A fully robust PDN has all impedance peaks below target impedance. [Chapter 9](#) details these conditions.

Generally, the **biggest challenge in PDN design** is determining reasonable transient currents on which to base a target impedance. We can employ three approaches to arrive at a transient current estimate:

1. We can estimate transient currents from the number of gates switching, the on-die load capacitance, and the clock frequency. This requires a parasitic extraction of the functional blocks and some idea of the number of gates that switch.
2. We can measure the current draw from the bench power supply on previous products to make inferences on the maximum and minimum current consumed and estimate the transient current for the next product.
3. If we know the PDN impedance profile from either simulation or measurement and measure the voltage noise on the die using package sense pins, we can back out the transient current that must have been consumed to stimulate the observed voltage.

**Tip**

Generally, the hardest design parameter to estimate is the **transient current**. Apply every method available to estimate a reasonable value. The more accurate the estimate, the less design margin is required and the lower the product cost for the same level of risk.

Often, we apply these processes to the previous generation of the product to extrapolate and predict the performance of the next generation of product.

After securing the estimate of the transient current, we use it to estimate a target impedance for the PDN. The goal in a fully robust PDN design is to reduce the maximum peak impedance values to be below the target impedance.

**Tip**

Focusing on the impedance dips is totally irrelevant. The peaks are what have the potential to contribute to major PDN noise violations.

We generally represent and model PDN resonant peaks as the parallel combination of a capacitance (C), an inductance (L), and some series resistance (R) arising from physical structures in the system. The three most important terms that determine the properties of the impedance peak in both the frequency and time domains are the **peak frequency, the characteristic impedance of the peak, and the q-factor** of the resonance. From these fundamental figures of merit, we can calculate the peak impedance.

We calculate their resonant frequency and characteristic impedance with

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L \times C}} \quad (10.1)$$

$$Z_0 = \sqrt{\frac{L}{C}} \quad (10.2)$$

where

L = the loop inductance

C = the capacitance

R = the resistance

$Z_0$  = the “characteristic” impedance of the peak

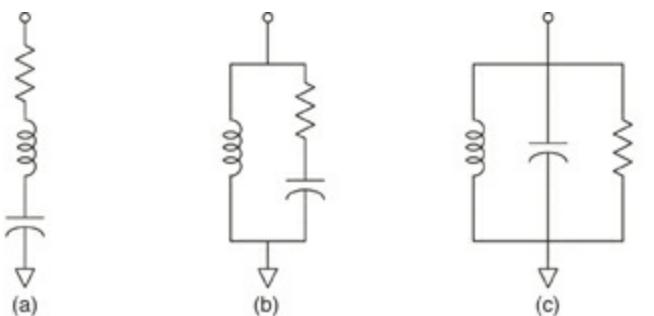
$f_{res}$  = the resonant frequency of the peak

As discussed in Chapters 2 and 9, there are series and parallel resonant circuits. The circuit topology of the L and C elements determine whether the resonance is a series or parallel resonance. Series resonant circuits form a “V” or a valley in the impedance profile with a minimum impedance determined by the ESR, the equivalent series resistance.

Parallel resonant circuits form an impedance peak. The resistance associated with the circuit determines the peak height. The resistance can be in series or in parallel with the LC elements.

Although it's not often discussed, defining an “equivalent parallel resistance” is possible. This would be a resistor in parallel with a pure inductance and pure capacitance. The parallel resistance determines the height of parallel resonant peak in the impedance profile.

Figure 10.1 shows three RLC circuits with the three different topologies.



Series RLC circuit

Parallel RLC circuit.  
Damping resistance is  
in series with L and CParallel RLC circuit.  
Damping resistance is  
in parallel with L and C

**Figure 10.1** Series and parallel resonant circuits. Circuit (a) is a series resonance circuit. Circuits (b) and (c) are both parallel resonators because L and C are in parallel.

Circuit (b) has the loss element in series with the resonant current and circuit (c) has the loss element in parallel with the resonant voltage.

To calculate the q-factor for each circuit we must determine whether the resistive loss element is in series with the resonant current or in parallel with the resonant voltage. Both (b) and (c) are parallel resonant circuits but (b) has the loss element in series with the resonant current and (c) has the loss element in parallel with the resonant voltage.

Circuit (a) is a series RLC with losses from the equivalent series resistance (ESR). The impedance profile is in the shape of a valley. The R term is in series with the resonant current and losses go as  $I^2R$ . At resonance, a higher R means more power losses and a lower q-factor. The q-factor is inverse to the R term. The q-factor for the series LC circuit, with the R term in series with the LC elements is

$$\text{q-factor}_{\text{series}} = \frac{Z_0}{R_{\text{series}}} \quad (10.3)$$

The q-factor subscript identifies the circuit topology of how the loss element connects to the LC elements.

Circuit (b) is a parallel circuit because the L and C elements are in parallel when measured from the top port with respect to ground. The impedance profile has a

peak. The resistor is in series with the resonant current and losses go as  $I^2R$ . At resonance, a higher R means more power losses and a lower q-factor. The q-factor is inverse to the R term. The q-factor for the parallel LC circuit with the R term in series with the LC elements is

$$\text{q-factor}_{\text{series}} = \frac{Z_0}{R_{\text{series}}} \quad (10.4)$$

Circuit (c) is also a parallel circuit because the L and C elements are in parallel when measured from the top port with respect to ground. But this time the loss element is in parallel with the reactive components that carry the resonant current. It is in parallel with the resonant voltage. The losses go as  $V^2/R$  as the voltage builds up across the reactive elements. At resonance, the power losses decrease with increasing resistance and the q-factor increases. The q-factor is proportional to the R term.

$$\text{q-factor}_{\text{parallel}} = \frac{R_{\text{parallel}}}{Z_0} \quad (10.5)$$

pay attention to R, Z position

From the R, L, and C terms, we calculate the resonant frequency, characteristic impedance, and q-factor for a parallel resonant circuit, and based on the circuit topology of the R term, we find the peak impedance at resonance as

$$Z_{\text{peak}} = Z_0 \times \text{q-factor} \quad (10.6)$$

When the R term is in series with the parallel LC, the peak impedance is

$$Z_{\text{peak}} = Z_0 \times \text{q-factor}_{\text{series}} = Z_0 \times \frac{Z_0}{R_{\text{series}}} \quad (10.7)$$

When the **R term is in parallel with the parallel LC**, the peak impedance is

$$\underline{Z_{\text{peak}}} = Z_0 \times \text{q-factor}_{\text{parallel}} = Z_0 \times \frac{\underline{R_{\text{parallel}}}}{Z_0} = R_{\text{parallel}} \quad (10.8)$$

We estimate the voltage droop response on the power rail from a step transient current or alternatively, estimate the peak's characteristic impedance from the observed voltage response to a known step transient current.

$$V_{\text{droop}} = I_{\text{step}} \times Z_0 = I_{\text{step}} \times \sqrt{\frac{L}{C}} \quad (10.9)$$

This relationship is often the most important way of estimating or confirming the step transient current in a PDN. If we can determine the characteristic impedance of the peak, we can extract the step current from the measured voltage droop on the PDN rail of the die pads.

#### Tip

An important method for estimating the largest transient current step (such as when the processor cores transition from an idle state to fully engaged) is to measure the initial voltage droop and use some knowledge of the peak's characteristic impedance.

To keep the step response droop within the acceptable tolerance, the characteristic impedance of the peak must be below the target impedance.

The resonant frequency of the peak is the ringing frequency of the voltage noise response to a step current change.

The q-factor is an indication of the number of cycles of ringing that lasts after the transient response.

In the most extreme condition, when the microcode causes a repetitive transient current square wave at the peak resonant frequency, which is sustained for at least a q-factor of cycles, the resulting peak-to-peak voltage noise is

$$V_{\text{pk-pk}} = I_{\text{pk-pk}} Z_{\text{peak}} = \frac{4}{\pi} I_{\text{transient}} \times \text{q-factor}_{\text{series}} \times Z_0 = \frac{4}{\pi} I_{\text{transient}} \times \frac{1}{R C} L \quad (10.10)$$

where

$V_{\text{pk-pk}}$  = the peak-to-peak voltage noise on the circuit

$I_{\text{pk-pk}}$  = the equivalent sine wave amplitude of the first harmonic of the square wave transient current

$I_{\text{transient}}$  = the peak-to-peak square wave of transient current at the resonant frequency

$\text{q-factor}_{\text{series}}$  = the quality factor of the RLC circuit, assuming the R term is in series with the parallel LC terms

The condition for this relationship to be accurate is that the q-factor must be  $> 2$ .

Assuming the average rail voltage is at the nominal value, the condition to keep the amplitude of the voltage noise within the voltage tolerance limit is that the peak impedance must be below about  $\pi/2 = 1.6$  times the target impedance when there is a single or dominant impedance peak. Chapter 9 describes this in detail.

These design parameters and resulting performance parameters give insight into the root cause of PDN performance limitations and the parameters to tweak to optimize noise performance. Likewise, the measured voltage noise and impedance profile give insight into the transient current features.

**Tip**

To reduce the voltage response to a transient current step, increase the capacitance or decrease the inductance.

The most significant peak in all PDN impedance profiles is usually the Bandini Mountain brought about by the on-die capacitance and the package lead inductance. The residual series resistance associated

with the on-die metallization and the series resistance of the package conductors contribute to the R of the circuit.

In addition, the non-linear switching of the CMOS circuitry contributes a parallel conductance loss term. This adds design margin by increasing the effective damping and decreasing the q-factor of the circuit.

**Tip**

The most effective ways of reducing the peak impedance of the Bandini Mountain are by increasing the on-die capacitance, reducing the package series inductance, and increasing the damping resistance.

**Tip**

Also available to the semiconductor provider is the option of adding on-package capacitors.

Adding on-package decoupling capacitors (OPD) splits the Bandini Mountain into two peaks. The advantage of on-package decoupling capacitors is the possibility the two peaks will have lower peak impedances than the original Bandini Mountain. We can usually reduce the lower frequency peak by choosing a sufficiently large capacitance for the OPD but we can reduce the higher frequency peak only through reducing the mounted inductance of the OPD and controlling its ESR.

The board-level MLCC capacitor components add to the package lead inductance, making the peak higher. When we use a limited number of capacitor values on the board, the possibility of reducing the Bandini Mountain exists by optimizing their capacitance values so their self-resonant frequencies extend up to and beyond the Bandini Mountain peak.

**Tip**

Without on-package decoupling capacitors, optimized capacitor values on the board can reduce the Bandini Mountain impedance peak.

This approach requires detailed knowledge of all the parameter values and is sensitive to the precise values of the board-level decoupling capacitors and their mounting inductance.

**Tip**

A generalized and more robust design strategy for the board-level PDN is to select a variety of capacitor values so their resulting impedance profile is flat and looks resistive all the way to the frequency of the Bandini Mountain.

In the absence of a package capacitor, a board impedance profile that is flat like a resistor provides damping for the Bandini Mountain peak. For this strategy to work, two important conditions must be met. The characteristic impedance of the Bandini Mountain must be less than the target impedance and the flat impedance profile at the board must be close to, but below the target impedance.

The impedances of each peak in the PDN, as viewed from the chip's perspective, are fundamentally limited by the loop inductances associated with each PDN element.

**Tip**

To achieve the lowest peak impedances and the lowest voltage noise, engineer the lowest loop inductances for each element in the system.

Generally, the three design goals to reduce loop inductance of power-ground interconnect structures are

1. Make the conductors short.

2. Bring the power and ground paths close together.
3. Make the conductors wide.

On a practical basis, these design goals translate to four important design guidelines when implementing PDN power-ground interconnects:

1. Use via-in-pad to attach capacitors to the board or vias as close as practical to the pad.
2. Use a thin dielectric between adjacent power and ground planes to reduce the spreading inductance. With thin dielectric, proximity of the capacitors to the package is second order.
3. In the stackup, place adjacent power and ground planes as close as possible to the surface where components are mounted.
4. Use as many parallel paths in the power-ground interconnects as practical.

These are the most important design guidelines for power-ground interconnect that result in a robust PDN.

### **10.3 INTRODUCING A SPREADSHEET TO EXPLORE DESIGN SPACE**

The first step toward exploring the design space is through engineering judgement, rules of thumb, and making simple approximations as outlined in the preceding section. The next level of analysis is using a spreadsheet to begin to explore the interconnectedness of all the design parameters.

As is often the case, improving the performance in one area means reducing the performance or increasing the cost in another area. This is often referred to as the “law of unintended consequences,” or the “whack-a-mole” problem. A spreadsheet is a useful tool to explore design space and tackle the important task of balancing design tradeoffs.

In this section, we introduce a spreadsheet and a few case study examples. Then we advance to a more accurate simulation. Along the way we illustrate the accuracy of the spreadsheet analysis by comparing it to circuit simulations and comparing the simulated predictions to measured results.

**Tip**

The combination of these three approaches: following general design guidelines, optimizing parameter values with a spreadsheet, and performing final verification in a circuit simulation, is a powerful process to quickly and efficiently converge on a cost-effective and robust PDN.

We can separate PDN design into input design parameters and predicted performance metrics that result from the analysis. This lends itself to spreadsheet analysis [1]. We have constructed a simple spreadsheet to combine the important input parameters and PDN relationships introduced in this book to estimate performance metric results. Table 10.1 shows the complete spreadsheet. It is best used for sizing, planning, and optimizing the PDN design. It is useful for working backward from measured data to see what the PDN parameters must have been and establishing model-to-hardware correlation. It is not a verification tool and is not based on any artwork or design databases.

1	Type	PDN Parameters	Value	Units		
2	Input	Voltage	1.00	V		
3	Input	Max current consumed	10.0	A		
4	Input	Min current consumed (with clock)	2.0	A		

5	Input	Leakage current (without clock)	1.0	A		
6	Result	Maximum dynamic current	9.0	A		
7	Result	Minimum dynamic current	1.0	A		
8	Input	AC tolerance	5.00	%		
9	Result	Transient current	8.0	A		
10	Result	AC target impedance	6.3	mΩ		
11	Input	DC tolerance	1.00	%		
12	Result	DC target impedance	1.00	mΩ		
13		Clock-edge noise (0th droop)				
14	Input	clock frequency	2,000	MHz		
15	Result	charge per cycle	4.5	nCoul/ cycle		
16	Result	load capacitance that switched	4.5	nF		
17	Result	switch factor	4.5	%		
18		Die				
19	Input	On-die capacitance	100	nF		
20	Result	R_die1—based on 60% of 250 pSec time constant	1.5	mΩ		
21	Result	R_die2—based on 40% of 250 pSec time constant	1.0	mΩ		
22		R_leak—assume $I_{leak} = a \cdot V_{dd}^3$				
23	Result	a—calculated from Vdd and $I_{leak}$	1			
24	Result	R at Vdd = $dV_{dd}/dI_{leak}$ (slope)	333	mΩ		
25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
26	Extract	Package series inductance	29			pH
27	Extract	R-pkg-dc—in the power current path	0.403			mΩ
28	Extract	R-pkg-ac at resonant frequency (additional)	0.430			mΩ
29	Extract	Board series inductance or VRM	19	96	10,000	pH

30	Extract	R-board-dc—in the power current path	0.043	0.97	0.2	mΩ
31	Extract	R-board-ac at resonant frequency (additional)	0.060	0.0		mΩ
32	Input	Number of board caps	10	6		
33		Discrete capacitor parameters (partial loop)				
34	Input	Capacitance	1.0	22		μF
35	Result	ESR	10.3	4.3		mΩ
36	Input	Partial inductance associated with cap body	600	1,200		pH
37		Capacitor mount properties (partial loop)				
38	Extract	Mounting resistance from vias	0.778	3.892		mΩ
39	Input	Horizontal pad or trace inductance	1	1		pH
40	Extract	Vertical inductance from vias	372	1,861		pH
41		Parallel mounted capacitor loop properties				
42	Result	Capacitance	10,000	132,000		nF
43	Result	Resistance	0.6	1.4		mΩ
44	Result	Inductance	84	510		pH
45	Result	Resonant loop capacitance	99.0	9,382	142,100	nF
46	Result	Resonant loop resistance (excluding ODC ESR)	1.548	2.954	1.573	mΩ
47	Result	Resonant loop inductance	132	690	10,510	pH
48	Result	$Z_0$ , Reactance at resonance	36	8.6	8.6	mΩ
49	Result	q-factor (combined from contributors)	2.5	2.4	4.0	
50	Result	q-factor from leakage	9.1	39	39	
51	Result	q-factor from load loss	5.5	23.3	23.3	
52	Result	q-factor from on-die capacitance ESR	15			
53	Result	q-factor from loop resistance (excluding ODC ESR)	24	2.9	5.5	

54		PDN Figures of Merit				
55	FD result	Peak frequency	44.1	1.98	0.130	MHz
56	FD result	Peak impedance	91	21	34	mΩ
57	FD result	PDN ratio (ratio of Z to Ztarget)	14	3.3	5.5	
58	TD result	Clock-edge droop (impulse response)	45			mV
59	TD result	Step response droop	292	69	69	mV
60	TD result	Resonance response (peak to peak)	922	211	348	mV
61	DC result	DC resistance from VRM to circuits	3.1			mΩ
62	DC result	DC power loss for max current	312			mW
		Inputs				

**Table 10.1** The complete PDN Resonant Calculator (PRC) in spreadsheet form including sections for top-level inputs, resonant loops and extracted figures of merit.

The most important features of any PDN are the impedance peaks, their resonant frequencies, characteristic impedances, and q-factors. From the input information about the PDN current loads and clock frequency, we calculate the expected voltage noise response to the three primary transient current waveforms: impulse, step, and resonant excitation.

The frequency domain figures of merit of the peaks and the time domain figures of merit of the maximum voltage noise are what we can base a judgement on of whether the PDN is acceptable as designed.

We designed this spreadsheet to analyze a PDN with three distinct peaks, separated by roughly a decade in frequency. These are created from the loops dominated by

- The on-die capacitance, package lead inductance, and MLCC inductance
- The MLCC capacitors and bulk capacitor loop inductance
- The bulk capacitors and VRM

These simple analytical estimates for the design parameters are translated into equivalent circuit elements and performance figures of merit. The predicted noise results are surprisingly close when compared with more detailed circuit simulations. This is another example of the power of simple approximations to “quickly get us to an acceptable answer.”

**Tip**

The goal of any analysis is to get us to an acceptable answer as quickly as possible. That is the purpose of the PDN resonance calculator spreadsheet presented here. This spreadsheet is not meant to be the final design tool for a PDN. On the contrary, it is meant to be the starting place to quickly evaluate some of the expected performance metrics given the starting parameters and design constraints. It identifies the most important design parameters and, equally important, the insignificant parameters that we can ignore.

The spreadsheet has six sections:

- PDN voltage, current, and target impedance calculations
- odd dip clock-edge noise features
- On-die properties
- Peak analysis for each of three different peaks
- Performance figures of merit in the frequency and time domains
- Calculation of the interconnect loop inductance of vertical and horizontal structures

In the following sections, we describe this spreadsheet's features in detail. The complete spreadsheet is available on the book's website at [www.informit.com/9780132735551](http://www.informit.com/9780132735551).

## **10.4 LINES 1–12: PDN INPUT VOLTAGE, CURRENT, AND TARGET IMPEDANCE PARAMETERS**

The first section of the spreadsheet sets up the important input terms that define the PDN rail. Table 10.2 shows these first twelve lines.

1	Type	PDN Parameters	Value	Units
2	Input	Voltage	1.00	V
3	Input	Max current consumed	10.0	A
4	Input	Min current consumed (with clock)	2.0	A
5	Input	Leakage current (without clock)	1.0	A
6	Result	Maximum dynamic current	9.0	A
7	Result	Minimum dynamic current	1.0	A
8	Input	AC tolerance	5.00	%

9	Result	Transient current	8.0	A
10	Result	AC target impedance	6.3	mΩ
11	Input	DC tolerance	1.00	%
12	Result	DC target impedance	1.00	mΩ

**Table 10.2** Setting up the PDN performance parameters.

**Line 2, input, voltage.** This is the Vdd rail voltage. The default value is 1 v.

**Line 3, input, max current consumed.** This is the maximum current consumed by the PDN rail when the maximum number of gates are switching. It is composed of the leakage current, the current from the clock network, and the additional current when the gates are switching. The default value is 10 A. This is the time averaged current draw from the power supply when running a section of microcode.

**Line 4, input, minimum current consumed (with clock).** This is the minimum current consumed by the rail when just the clock network is switching. The default value is 2 A.

**Line 5, input, leakage current (without clock).** This is the leakage current between the Vdd and Vss rails that depends on the technology node, the gate oxide thickness, threshold voltage, Vdd setting, and the total number of gates on the die. Because much of the leakage current is due to tunneling through very thin oxides and subthreshold current, the leakage current is not linear with Vdd but is an exponential and often

varies as Vdd<sup>3</sup>. The default value is 1 A.

**Line 6, result, Maximum dynamic current.**

This is the maximum current that flows, not including the leakage current. This is also the average rail current that flows each clock cycle from all the load capacitance being charged and discharged per clock cycle, for all the gates. We calculated it as

$$\text{Maximum Dynamic Current} = \text{maximum current consumed} - \text{leakage current}$$

The default calculated value is 9 A.

**Line 7, result, minimum dynamic current.**

Dynamic current is the average current that is consumed each clock cycle to charge and discharge the load capacitance. The minimum current is drawn when only the clock distribution elements are switching. This is

$$\text{Minimum Dynamic Current} = \text{the minimum current consumed with the clock} - \text{the leakage current}$$

The default value calculated in this example is 1 A.

**Line 8, input, the AC Tolerance.** This is the amplitude of the double-sided noise that can be tolerated on the Vdd rail. It is the amplitude above or below the nominal value, not the peak-to-peak noise. The default value is 5%, which means that voltage excursions to  $\pm 5\%$  are tolerated.

**Line 9, result, the transient current.** This is the peak-to-peak changing current we expect to see when the microcode changes from quiescent to most switching. We calculate it from

$$\text{Transient Current} = \text{maximum dynamic current} - \text{the minimum dynamic current}$$

The default value is calculated as 8 A.

**Line 10, result, the AC Target impedance.** This is the well-known target impedance used as the goal in engineering the PDN impedance profile. As we have shown many times, it is

$$Z_{\text{target-AC}} = \frac{V_{dd} \times \text{tolerance\_AC}}{I_{\text{transient}}} \quad (10.11)$$

In the spreadsheet, the target impedance calculated from default parameters is 6.3 mΩ. This establishes a target for the flat regions of the PDN and for the peak's characteristic impedance for a marginally robust design. As mentioned in the previous section, even the peaks' top should be below this target impedance for a fully robust PDN.

**Line 11, input, the DC voltage noise tolerance.**

This is the allowable DC offset voltage as a percentage of Vdd—in other words, the amount of voltage noise allowable from DC IR drop. It may be partially compensated out by the VRM sense line and feedback circuitry. This value basically determines the allowable DC voltage drop in the PDN from the VRM feedback point to the pads on the die. It is not always specified, but should be a small value compared to the AC tolerance. In this example, the default value is 1%.

**Line 12, result, the DC target impedance.** This is related to the maximum allowable DC series resistance in the PDN path. We calculate the DC target impedance similarly to the AC target impedance except that the maximum current consumed includes leakage and is everything that flows through the DC series resistance. We calculate it as

$$Z_{\text{target-DC}} = \frac{V_{dd} \times \text{tolerance\_DC}}{I_{\text{max}}} \quad (10.12)$$

The DC target impedance calculated from the default parameters in this spreadsheet is  $1\text{ m}\Omega$ .

The terms in this section of the spreadsheet allow us to calculate the target impedances used to establish design goals for the PDN.

## 10.5 LINES 13-24: 0TH DIP (CLOCK-EDGE) NOISE AND ON-DIE PARAMETERS

This section covers information for estimating the noise generated on isolated clock edges. Clock-edge noise is due to charging the load capacitance after each rising clock edge. Table 10.3 shows a snapshot of these lines.

13		Clock-edge noise (0th droop)		
14	Input	Clock frequency	2,000	MHz
15	Result	Charge per cycle	4.5	nCoul/cycle
16	Result	Load capacitance that switched	4.5	nF
17	Result	Switch factor	4.5	%
18		Die		
19	Input	On-die capacitance	100	nF
20	Result	R_diel1—based on 60% of 250 psec time constant	1.5	$\text{m}\Omega$
21	Result	R_diel2—based on 40% of 250 psec time constant	1.0	$\text{m}\Omega$
22		R_leak—assume $I_{\text{leak}}=a \cdot V_{\text{dd}}^3$		
23	Result	a—calculated from Vdd and I_leak	1	
24	Result	R at Vdd = $dV_{\text{dd}}/dI_{\text{leak}}$ (slope)	333	$\text{m}\Omega$

**Table 10.3** Input parameters to calculate the clock-edge noise.

The clock-edge noise is also known as the *0th droop*. The term *1st droop* is reserved for the droop associated with the first impedance peak, *2th droop* is associated with the second impedance peak, and so on. Several *oth* droops associated with several clock cycles are usually involved in creating the *1st* droop.

Clock-edge noise is all about load capacitance being charged up during the clock cycle. Although we might find this by using an on-die parasitic extraction tool, knowledge about the code vector, and gate utilization, we use the current drawn by the die to estimate these

important input parameters. Measured current is easier to obtain than the actual load capacitance switched on each clock edge. We use time average current and clock frequency to obtain the charge consumed during an average clock cycle.

**Line 14, input, clock frequency.** This is the clock frequency the chip runs at when we measure the maximum current. Use the maximum clock frequency in MHz in this line. The default value is 2,000 MHz.

**Line 15, result, the charge in nC consumed to switch the voltage on the output load**

**capacitance during an average clock cycle.** The chip is configured to draw the maximum dynamic current. The average current consumed by the gates each cycle times the period of one cycle in nsec is the average charge per cycle. The value calculated from default parameters is 4.5 nC/cycle. We calculate it from

$$Q_{\text{clk-cycle}} = I_{\text{dyn\_max}} \times T_{\text{clk}} = I_{\text{dyn\_max}} \times \frac{1}{F_{\text{clk}}} \quad (10.13)$$

**Line 16, result, the load capacitance that switches.**

Given the amount of charge that flows per clock cycle and that it flows into a load capacitance to charge it up to the Vdd rail, we can easily estimate the output load capacitance. The value calculated from default parameters in this example is 4.5 nF. We calculate it from

$$C_{\text{switched}} = \frac{Q_{\text{clk-cycle}}}{V_{\text{dd}}} \quad (10.14)$$

**Line 17, result, switch factor.** This is the ratio of the maximum capacitance that is switched per cycle to the total on-die decoupling capacitance due to the entire distributed capacitance of the Vdd rail. The total on-die decoupling capacitance is a term that is input in the next

line. The value calculated from default parameters is 4.5%. We get the switch factor with

$$\text{SwitchFactor} = \frac{C_{\text{switched}}}{C_{\text{ODC}}} \quad (10.15)$$

**Line 19, input, on-die capacitance.** This is the total amount of on-die decoupling capacitance used by the Vdd rail. This is sometimes a closely guarded secret of the semiconductor vendor. Using a VNA and calibrated probes as discussed in [Chapter 3](#), we can measure it when the device is powered on, as long as there are no on-package decoupling capacitors or power gates that disconnect sections of the die. The default value in this example is 100 nF.

**Lines 20 and 21, result, the on-die series resistance.** These two terms are the equivalent series resistance associated with the on-die capacitance. They come from the metallization of the Vdd, Vss, the chip-attach interconnects, and the FET transconductance. The value of R\_die1 is the contribution of on-die metallization, which contributes to the DC IR voltage drop in series with the power path. The value of R\_die2 is the contribution of the FET transconductance and signal wire resistance that leads to the capacitance of the next gate. It is in series with the on-die capacitance that does not switch when a portion of the gates switch.

The sum of R\_die1 and R\_die2 is the equivalent resistance in series with the on-die capacitance when we measure it from the package balls or die bumps, looking in toward the circuits. Larger die areas have more capacitance because small areas of parallel capacitance add together. Larger die areas have less resistance because the conductances ( $1/R$ ) in parallel add together. The RC product remains a constant no matter how much die area is measured. As discussed in [Chapter 8](#), a

reasonable RC time constant is 250 ps.

A substantial amount of on-die capacitance comes from the wiring capacitance to adjacent wires that each have a probability of being driven high or low. Measurements from the package balls or die bumps cannot distinguish between R\_die1 and R\_die2. Obviously, on-die capacitance with its series resistance is a very distributed problem. For a simple simulation circuit topology, these two resistors account for the DC IR drop and the capacitance ESR presented to the switching circuits. It is estimated that 60% of the resistance belongs to R\_die1 and 40% of the resistance belongs to R\_die2. Based on these assumptions, we calculate the two resistances from

$$R_{die1} = 0.6 \times \frac{0.25 \text{ nsec}}{C_{ODC}} \quad (10.16)$$

and

$$R_{die2} = 0.4 \times \frac{0.25 \text{ nsec}}{C_{ODC}} \quad (10.17)$$

**Line 22, comment, is the leakage resistance.** An important damping term is the shunt resistance from leakage current between the Vdd and Vss rails. Empirically, this is of the form

$$I_{leakage} = a \times V_{dd}^3 \quad (10.18)$$

where “a” is a coefficient related to the silicon technology node, the threshold voltages, and the gate area on the die. It is a strong function of temperature. We can extract this coefficient by knowing the leakage current at the nominal Vdd rail voltage, which we can get by measuring the quiescent current draw when the clock is in its off, quiet state.

**Line 23, result, the value of the coefficient, a.**

We calculate this from

$$a = \frac{I_{\text{leakage}}}{V_{dd}^3} \quad (10.19)$$

In this example, the default value is calculated as 1 when the leakage current is 1 A and the Vdd is 1 V.

### ***Line 24, result, the dynamic leakage***

**resistance.** The leakage current acts as a shunt resistance. However, it is not the DC resistance that contributes to the damping, but the small signal dynamic impedance. This is the slope of the leakage current, Vdd rail voltage curve. We get the dynamic resistance with

$$R_{\text{leakage-dynamic}} = \frac{dV_{dd}}{dI_{\text{leakage}}} = \frac{1}{3 \times a \times V_{dd}^2} = \frac{V_{dd}^3}{3 \times I_{\text{leakage}} \times V_{dd}^2} = \frac{V_{dd}}{3 \times I_{\text{leakage}}} \quad (10.20)$$

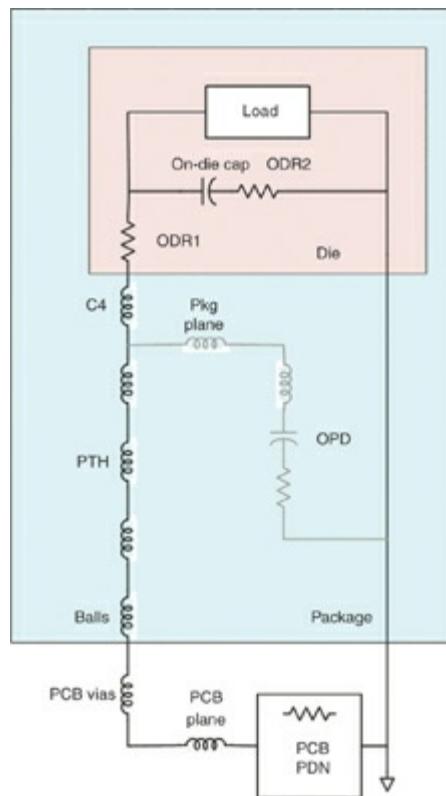
In the default case, the dynamic damping resistance is 330 mΩ as a shunt resistance across the on-die decoupling capacitance.

These terms are the input parameters used to estimate the figures of merit for the PDN performance in the frequency and time domains for each of the impedance peaks.

## **10.6 EXTRACTING THE MOUNTING INDUCTANCE AND RESISTANCE**

Inductance and resistance from the die pads to the MLCC capacitors are associated with the package and PCB structures, and we estimate them from the geometries and materials. Structures are classified into two types: vertical where the cross section is cylindrical in nature and horizontal where the structures are planar in nature. The vertical structures are the vias, balls, and bumps. The horizontal structures include power planes and power traces.

These interconnect elements connect the distributed on-die decoupling capacitance to the board-level power distribution and ultimately the MLCC capacitors mounted to the board. Figure 10.2 shows a schematic of each of the important circuit elements. We can calculate each of these elements based on the geometry and material properties using a few simple approximations [2].



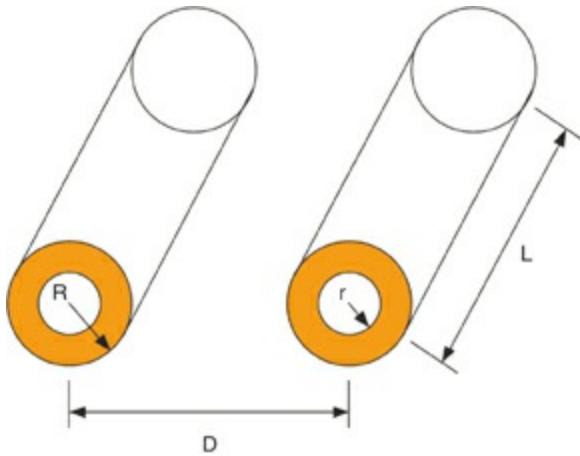
**Figure 10.2** Schematic identifying each of the resistive and inductive circuit elements between the on-die decoupling capacitance and the MLCC capacitors. The shaded colors show the die and package boundaries, and on-package decoupling is included for reference.

We estimate the loop resistance at DC, the AC resistance due to skin effects, and loop inductance at the resonant frequency using simple approximations. Chapter 4 covers these in detail, but we offer them here again for completeness. These are the approximations integrated in the spreadsheet calculations in the “extraction” tab.

Of course, 3D field solvers give a more accurate value

for the loop inductances and resistance. The approximations typically give values accurate to within 10%–20% and are an excellent starting place. They give reasonable predictions and focus attention on the structures that dominate the PDN properties at resonance.

The basis for vertical structure calculation is the twin rod approximation, illustrated in Figure 10.3.



**Figure 10.3** The features of the twin rod approximation for the loop inductance, assuming the two rods are connected together at their far end.

The loop inductance per length of this structure is

$$L_{\text{Len}} = \frac{\mu_0}{\pi} \cosh^{-1} \left( \frac{D}{2R} \right) = \frac{\mu_0}{\pi} \ln \left( \left( \frac{D}{2R} \right) + \sqrt{\left( \frac{D}{2R} \right)^2 - 1} \right) \quad (10.21)$$

where

$L_{\text{Len}}$  = the loop inductance per length, in pH/mm

$D$  = the center-to-center spacing, in mm

$R$  = the outer radius of the rods, in mm

$\mu_0$  = permeability of free space =  $4\pi \times 10^{-4}$  H/mm

We assume the current to be on the outer surface of the conductors.

The DC loop resistance per length is

$$R_{Len} = \frac{2}{\sigma(\text{cross-sectional area})} = \frac{2}{\sigma(\pi R^2 - \pi r^2)} \quad (10.22)$$

where

$R_{Len}$  = the resistance per length of the entire loop

$\sigma$  = the conductivity of the material, often copper

The factor of 2 accounts for the two paths in series

$R$  = the outer radius of the rod, in mm

$r$  = the inner radius of the rod, in mm

The skin effect causes the inside diameter to change as a function of frequency. The skin depth is

$$\delta = \frac{1}{\sqrt{f\mu_0\sigma}} \quad (10.23)$$

where

$\delta$  = the skin depth in mm

$f$  = the sine wave frequency, in MHz

$\mu_0$  = the permeability of free space =  $4\pi \times 10^{-4}$  H/mm

$\sigma$  = the conductivity of copper in Siemens/m

When the current is skin depth limited, the cross-sectional area through which current travels is reduced. If we assume the skin depth is thin compared to the outer radius of the conductor, then the high-frequency resistance per length at a frequency  $f$  is

$$R_{Len-ac} = \frac{2}{\sigma(\text{cross-sectional area})} = \frac{2}{\sigma(2\pi R \times \delta)} \quad (10.24)$$

To simplify the calculation, we pick a frequency of 100 MHz as the reference frequency, where the skin depth of copper is 6.6  $\mu\text{m}$ , for example, and calculate the loop resistance at this frequency. Because the skin depth scales with the square root of frequency, we scale the resistance at any other frequency by

$$R_{Len-ac} = \frac{R_{Len-ac-100MHz}}{\sqrt{\frac{f}{100MHz}}} \quad (10.25)$$

The frequencies we care about are the resonant frequencies.

From these simple formulas, we calculate the per-unit-length loop inductance and resistance for the twin rod structure. It is then a matter of multiplying by the length and accounting for multiple pairs in parallel to determine the inductance and resistance of vertical PDN structures.

When multiple pairs of vertical interconnects are routed in parallel, loop mutual inductance interactions will exist between the pairs. If there were no mutual inductance interactions, the total loop inductance of n pairs of loops in parallel would be

$$L_{total} = \frac{1}{n} L_{pair} \quad (10.26)$$

This possibility exists for an array of pairs of pins to have a higher loop inductance than the parallel combination of the individual pairs. This could happen, for example, if all the Vcc pins are positioned close to each other. Their mutual inductance would increase the parallel loop inductance per pair. It would be as if the normalized loop inductance per pin pair were higher than the isolated pair.

Of course, the way to reduce the parallel combination of multiple pin pairs is to place the pins in a checkerboard array, interleaving the Vdd and Vss pins. Because the currents on adjacent pins flow in opposite directions, the mutual inductance acts to reduce the total parallel combination of pins in parallel. It would be as if the per pin-pair loop inductance were less than the isolated value.

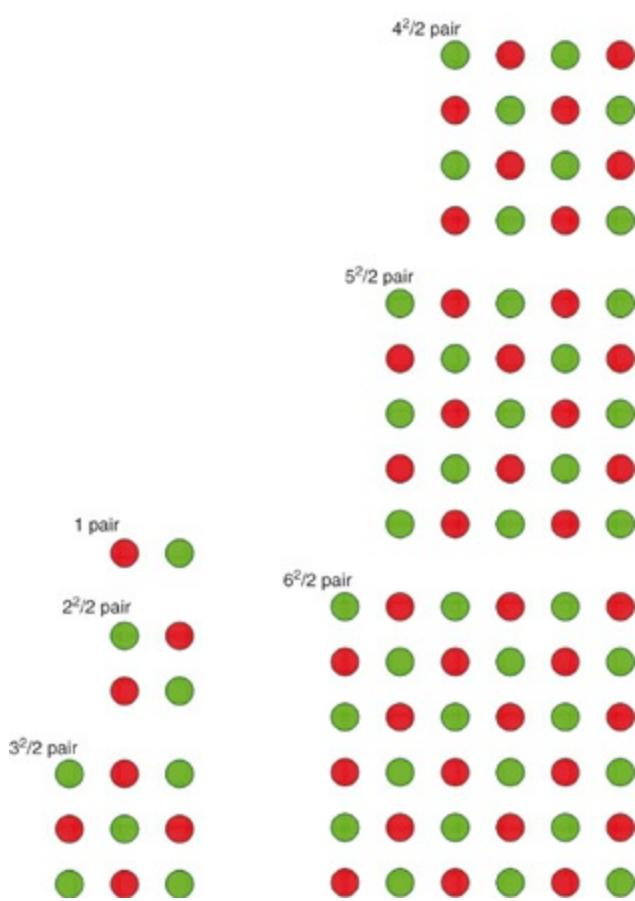
In a checkerboard pattern, each Vdd pin looks out for four directions (north, south, east, and west) and sees a Vss pin for return current. Similarly, each Vss looks out for four directions and sees a Vdd pin for return current. Total loop inductance is minimized in this way.

With two pairs arranged in a  $2 \times 2$  array, less total inductance is expected than what is predicted by two isolated pairs of twin lead transmission line in parallel. Similarly, a  $4 \times 4$  array with eight pairs of Vdd and Vss pins arranged in a checkerboard pattern has less inductance than predicted by eight isolated twin lead pairs in parallel. This inductance reduction is called the checkerboard reduction factor.

**Tip**

The mutual inductance between one pin and its four nearest neighbors with opposite directed current reduces the average pin-pair loop inductance over their isolated loop inductance. The actual pin-pair loop inductance is scaled from the isolated pin-pair loop inductance by the *checkerboard reduction factor*. If adjacent pins had current in the same direction, the effective pin-pair loop inductance would be higher than 1.

Figure 10.4 shows Vdd and Vss pins arranged as 1 pair ( $1 \times 2$ ), 2 pair ( $2 \times 2$ ), 4.5 pair ( $3 \times 3$ ), 8 pair ( $4 \times 4$ ), 12.5 pair ( $5 \times 5$ ), and 18 pair ( $6 \times 6$ ). A pair means a Vdd and Vss conductor where the inductance is estimated using the twin rod equation. The total loop inductance is found from 3D electromagnetic extraction, which includes all the mutual interactions for each pattern and is normalized to the “per pair” value for each configuration.



**Figure 10.4** Checkerboard patterns for an array of  $n$  power and ground pin pairs interleaved to give the lowest total loop inductance. As the number of pins in the array increases, the mutual interactions reach a saturation level.

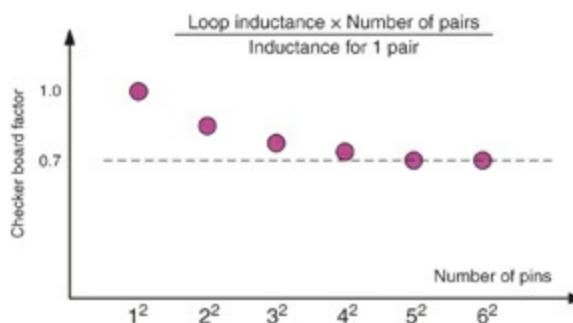
A single pair has the inductance predicted by the twin lead approximation. Adding more pairs into the area reduces the normalized loop inductance per pair. With enough pairs in the checkerboard pattern, the normalized inductance reaches an asymptote and flattens out the checkerboard reduction factor.

All pin configurations have a checkerboard factor for inductance, but its specific value depends on a lot of factors such as the number of pairs, the ratio of diameter to pitch, the frequency, the exact configuration of the pins, and so on.

If the pattern is not a checkerboard but some of the Vdd pins are clumped together and some of the Vss pins are clumped together, the factor can be more than 1. This indicates that the specific pin configuration has a

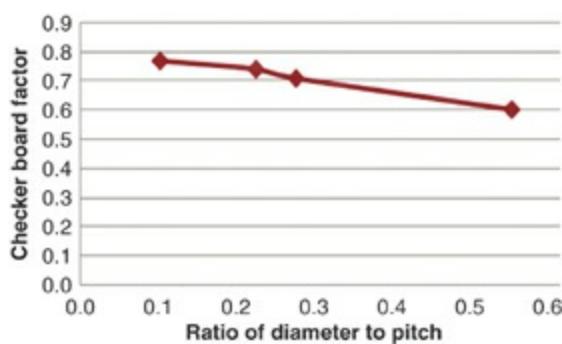
normalized inductance per pair greater than the twin lead loop inductance. Sometimes clumping of similar pins is necessary for layout considerations but results in less inductance improvement than might be expected from the parallel pin count.

The checkerboard factor is essentially a fudge factor that accounts for the pin configuration because inductance is estimated for a number of cylindrical structures in parallel. [Figure 10.5](#) shows the calculated checkerboard factor as the number of pin pairs increases distributed in the arrays shown in [Figure 10.4](#). This is for the special case when the center to pin diameter is 25% of the center-to-center spacing. The asymptotic value is 0.7 for this special case.



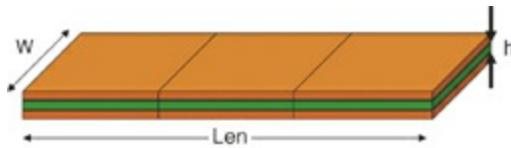
**Figure 10.5** The checkerboard factor calculated for the special case of the pin diameter 25% of the center-to-center spacing, as the number of pin pairs in the array increases.

If the center-to-center spacing decreases compared to the pin diameter, so the pins get closer together, the mutual inductance extends to more pins and the asymptotic value for the checkboard factor decreases. [Figure 10.6](#) shows the calculated checkerboard factor as the ratio of pin diameter to center spacing increases.



**Figure 10.6** Asymptotic value of the checkerboard factor as the pins are brought closer together and the pin diameter-to-center spacing increases.

Like vertical structures, horizontal structures also have inductance and resistance that we must estimate. In Chapter 4, you saw how to estimate the spreading inductance from sheet inductance from the number of squares. Figure 10.7 reviews loop inductance of a section made from a length of two planes.



**Figure 10.7** Illustration of two wide conductors with a thin dielectric between them.

The loop inductance from one far edge to the other is

$$L_{\text{loop}} = (\mu_0 \times h) \times \frac{Len}{w} = L_{\text{sq}} \times n \quad (10.27)$$

where

$L_{\text{loop}}$  = the loop inductance

$h$  = the dielectric thickness

$Len$  = the length of the uniform section of planes

$w$  = the width of the uniform section of planes

$L_{\text{sq}}$  = the sheet inductance in nH/square

$n$  = the number of squares down the length

We call the first term in parentheses the *sheet inductance* or the *loop inductance per square*. It is the loop inductance,  $L_{\text{sq}}$ , of one square of planes. The

second term is the number of squares,  $n$ , which is just the ratio of the length to the width of the strip.

**Tip**

This relationship points out again the importance of using as thin a dielectric as practical between the adjacent power and ground planes. This results in the lowest sheet inductance and the lowest spreading inductance between elements connected by the planes.

Equation 10.27 is a powerful formalism. The sheet inductance of a path made from a pair of planes only depends on the dielectric thickness between the two planes. All we need to know is the sheet inductance and the number of squares in series that makes up the interconnect and we can estimate the loop inductance of the path.

Likewise, we calculate the sheet resistance with

$$R = \left( \frac{1}{t\sigma} \right) \times \frac{Len}{w} \quad (10.28)$$

where

$t$  = the thickness of the trace

$\sigma$  = the conductivity of the copper

The first term is the sheet resistance and the second term is the number of squares. The sheet resistance, in  $\Omega$  per square, is the resistance from edge to edge of a piece of conductor shaped like a square. It is independent of the dimensions of the square.

The total resistance of a trace is just the sheet resistance times the number of squares in series. In the case of the Vdd and Vss traces, there are two traces in series, so the series resistance of the section of the planes is really twice this resistance to account for both the Vdd and Vss paths.

As with the vertical structure, we determine the frequency of the resonant peak of interest and use the skin depth limited resistance at this frequency in the estimate of the series resistance.

## 10.7 ANALYZING TYPICAL BOARD AND PACKAGE GEOMETRIES FOR INDUCTANCE

We implement these calculations in the spreadsheet via the “extraction” tab. We have set up a very specific example to exercise the loop inductance calculations as the default case. This example uses C4 balls on the chip that are 30  $\mu\text{m}$  in diameter and on a 200  $\mu\text{m}$  pitch. The BGA balls are 0.5 mm in diameter on a 1 mm pitch. The board vias to the nearest power and ground plane are assumed to be 0.5 mm deep in the board stackup.

In this configuration, it is interesting to note the relative loop inductance contributions from all the vertical and horizontal sources.

If capacitors are placed on the bottom side of the board, the mounting inductance to the board power planes would be about 1.9 nH. If the capacitors are mounted on the top of the board, they would have a via loop inductance of about 0.37 nH per capacitor.

The contribution from the package vertical inductance path is on the order of 29 pH, compared to the parallel combination of 18 BGA board via pairs to the board’s power and ground cavity of 19 pH.

The largest source of loop inductance that contributes to the Bandini Mountain is the horizontal inductance in the PCB cavity. Assuming a thickness between the Vdd and Vss planes that make up the board cavity of 76  $\mu\text{m}$ , the thinnest typically available, the sheet inductance is

$$L_{\text{sq}} = (\mu_0 \times h) = 0.4 \pi \frac{\text{pH}}{\mu\text{m}} \times 76 \mu\text{m} = 95 \frac{\text{pH}}{\text{square}} \quad (10.29)$$

With one square effectively in the path from the BGA vias to the capacitor vias, there is 95 pH of loop inductance. This amount plus the vertical loop inductance results in a total loop inductance of 111 pH in the PCB path and about 30 pH in the package path for a total of 141 pH.

Tables 10.4 and 10.5 are examples of spreadsheets that make calculations of PDN parameters from geometries and materials. It uses all the closed-form equations discussed thus far in the chapter to calculate RLC element parameter values to be used in the assumed PDN topology shown in the next sections.

1	Extraction of Parameters from Geometries and Materials			Gray cells are inputs					
2	Vertical	PCB	PCB	PCB	Package	Package	Package	Package	Units
3		BGA vias	Caps top	Caps bottom	Balls	Micro vias	PTH vias	Micro vias	Bumps
4	Material	Copper	Copper	Copper	Solder	Copper	Copper	Copper	Solder
5	Pitch	1.00	1.00	1.00	1.000	0.200	0.450	0.200	0.200 mm
6	Diameter (OD)	0.304	0.304	0.304	0.500	0.125	0.200	0.125	0.030 mm
7	Diameter (ID)	0.253	0.253	0.253	0.000	0.000	0.100	0.000	0.000 mm
8	Cross-sectional area	0.0221	0.0221	0.0221	0.1963	0.0123	0.0236	0.0123	0.0007 mm²
9	Conductivity	5.80E + 007	5.80E + 007	5.80E + 007	5.20E + 006	5.80E + 007	5.80E + 007	5.20E + 006	1/(Ω·m)
10	Skin depth at 100 MHz	0.0066	0.0066	0.0066	0.022	0.0066	0.0066	0.0066	0.022 Mm
11	Cross-sectional area at 100 MHz	0.00617	0.00617	0.00617	0.03314	0.00246	0.00402	0.00246	0.00071 mm²
12	Per Unit Length (mm)								
13	Loop resistance at DC	1.557	1.557	1.557	1.959	2.810	1.463	2.810	544.120 mΩ/mm
14	Loop resistance at 100 MHz	5.589	5.589	5.589	11.606	14.029	8.588	14.029	544.120 mΩ/mm
15	Loop inductance/ length	744	744	744	527	419	580	419	1,034 pH/mm

16	I Loop								
17	Length	0.500	0.500	2.500	0.500	0.105	0.800	0.105	0.065 mm
18	I Loop Inductance	372	372	1861	263	44	464	44	67 pH
19	I Loop Resistance at DC	0.78	0.78	3.89	0.98	0.30	1.17	0.30	35.37 mΩ
20	I Loop Resistance at 100 MHz	2.79	2.79	13.97	5.80	1.47	6.87	1.47	35.37 mΩ
21	Pairs								
22	Number of pairs	18	1	1	18	36	36	36	144
23	Checkerboard factor	0.9	1.0	1.0	0.9	0.9	0.8	0.9	0.8
24	Loop inductance	19	372	1861	13.3	1.1	10.7	1.1	0 pH
25	Loop resistance at DC	0.043	0.778	3.892	0.054	0.008	0.033	0.008	0.246 mΩ
26	Skin effect on-set frequency	6.81	6.81	6.81	0.78	1.12	1.75	1.12	216 MHz
27	Loop resistance at resonance	0.103	0.778	3.892	0.214	0.027	0.127	0.027	0.246 mΩ

**Table 10.4** PDN Resonance Calculator (PRC) section detailing the loop inductance elements of the vertical and horizontal interconnect structures.

28	Horizontal (planar)	PCB	Package	Units
29		Power planes	Shape	
30	Dielectric thickness	0.0762	0.035	mm
31	Conductor thickness	0.036	0.036	mm
32	Conductivity	5.80E + 007	5.80E + 007	1/(Ω-m)
33	Skin depth at 100 MHz	0.0066	0.0066	mm
34	Loop inductance per square	96	44	pH
35	Loop resistance per square—DC	0.970	0.970	mΩ
36	Loop resistance per square—100 MHz	5.218	5.218	mΩ
37	Total	PCB	Package	Units
38	Vertical inductance	19	26.7	pH
39	Vertical DC resistance	0.043	0.349	mΩ
40	Vert resistance at resonance	0.103	0.641	mΩ
41	Number of squares	1	1	
42	Number of paths		18	
43	Horizontal inductance	96	2	pH
44	Horizontal DC resistance at DC	0.970	0.054	mΩ
45	Skin effect on-set frequency	3.45	3.45	MHz
46	Horizontal resistance at resonance	0.970	0.192	mΩ
47	Total path inductance	115	29	pH
48	Total path DC resistance	1.013	0.403	mΩ
49	Path resistance at resonance	1.073	0.833	mΩ
50	Peak 1 resonant frequency	44.1		MHz
51	Peak 2 resonant frequency	2.0		MHz

**Table 10.5** Section of the PRC detailing the summary of the RLC components for each peak.

## 10.8 THE THREE LOOPS OF THE PDN RESONANCE CALCULATOR (PRC) SPREADSHEET

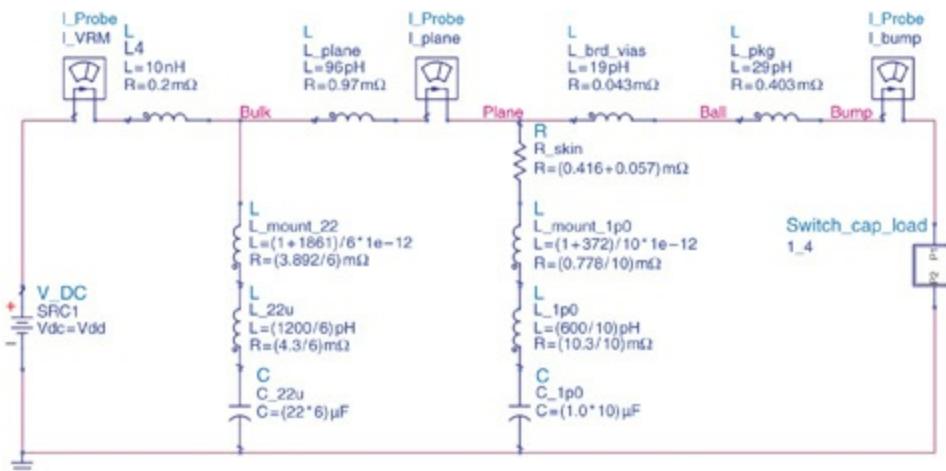
We designed this spreadsheet to analyze a PDN with three distinct peaks in the impedance profile. This commonly occurs when significant inductance separates the interconnect elements. The higher inductance and the increasingly larger capacitance further away from the die results in loops with lower parallel resonant frequencies. Of course, when the PDN impedance profile is more complicated, this simple spreadsheet analysis may not apply and a full-circuit simulation is required. This simplification offers significant insight into the direction to head to optimize the PDN.

In particular, the most important impedance peak is the Bandini Mountain parallel resonance. This is the highest frequency and highest impedance peak, and the hardest to bring below the target impedance. Analysis of its features, its fundamental limits, and the design decisions that influence the performance figures of merit are perhaps the most important aspects in PDN design. This is an important contribution of the PRC spreadsheet.

**Tip**

The PRC spreadsheet is well suited to analyze the Bandini Mountain features.

Figure 10.8 shows the circuit elements that describe the three peaks and the loops associated with each peak.



**Figure 10.8** Equivalent circuit model for the three loops described in the PRC and all the contributing circuit elements.

The highest frequency and most important peak is the Bandini Mountain, created by the on-die decoupling capacitance and package lead inductance in the loop with some associated MLCC capacitor mounting inductance.

Loop interaction of the MLCC capacitors and the bulk capacitor inductance creates the next lower frequency

peak. The interaction of the effective inductance of the VRM and the bulk capacitor creates the lowest frequency peak.

**Tip**

As long as the resonant frequencies are separated by at least an order of magnitude in frequency, their elements do not interact very much and we can analyze each parallel resonance independently. This is how the PRC is designed.

If the resonant frequencies are not separated by a decade, interaction occurs between the resonances. The PRC loses accuracy and circuit simulation is necessary for the lower frequency peaks. Calculations for the Bandini Mountain are still pretty good if the bump-loop inductance includes both high-frequency and bulk capacitor loops.

The important contributors to the R, L, and C elements for each of the three peaks included in the PDN Resonance Calculator are estimated in this section of the spreadsheet. For each peak, we calculate the equivalent loop inductance, capacitance, and damping terms. From these, we calculate the most important figures of merit of the impedance profile in the frequency domain and the transient response to the three important waveforms in the time domain.

Specific geometries and materials were assumed in the default design as a starting place to estimate PDN circuit parameters. You can drop the extraction portion of the spreadsheet if you use software extraction tools to obtain inductance and resistance parameters. Software tools require a design database that might not be available until late in the product cycle. You can replace the spreadsheet circuit parameters by more accurate values from software extraction to estimate the frequency and time domain performance figures of

merit (impedance peak, q-factor, voltage droops, and so on). The PRC is very useful at this point to figure out what you must change on a design that is not producing a PDN with acceptable performance.

Table 10.6 shows the section of the PRC analyzing the figures of merit for the three peaks.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
26	Extract	Package series inductance	29			pH
27	Extract	R-pkg-dc—in the power current path	0.403			mΩ
28	Extract	R-pkg-ac at resonant frequency (additional)	0.430			mΩ
29	Extract	Board series inductance or VRM	19	96	10,000	pH
30	Extract	R-board-dc—in the power current path	0.043	0.97	0.2	mΩ
31	Extract	R-board-ac at resonant frequency (additional)	0.060	0.0		mΩ
32	Input	Number of board caps	10	6		
33		Discrete capacitor parameters (partial loop)				
34	Input	Capacitance	1.0	22		µF
35	Result	ESR	10.3	4.3		mΩ
36	Input	Partial inductance associated with cap body	600	1,200		pH
37		Capacitor mount properties (partial loop)				
38	Extract	Mounting resistance from vias	0.778	3.892		mΩ
39	Input	Horizontal pad or trace inductance	1	1		pH
40	Extract	Vertical inductance from vias	372	1,861		pH
41		Parallel mounted capacitor loop properties				
42	Result	Capacitance	10,000	132,000		nF
43	Result	Resistance	0.6	1.4		mΩ
44	Result	Inductance	84	510		pH

**Table 10.6** Spreadsheet showing the calculated inductance and resistance parameters for the package and board, die properties, discrete capacitor properties, and calculated q-factor parameters.

**Line 26 is the package series inductance,** extracted from the vertical and horizontal structures in

the package.

**Lines 27 and 28 are the package series resistance at DC and the value at the resonant frequency of each peak.** This takes into account the skin depth effect. Calculating the AC resistance uses the resonant frequencies from line 55 farther in the spreadsheet, shown later in Table 10.7. The larger of the two values is used in the calculation for resistive damping.

**Line 29 is the series inductance associated with the board vias and spreading inductance.** In the case of the lowest frequency peak, it also includes the effective output inductance of the VRM.

**Lines 30 and 31 are the series resistance of these circuit paths in the board.** The AC resistance is calculated as the skin depth resistance at each loop resonant frequency. Only the larger of the two is used to calculate the damping.

**Line 32 is the number of discrete capacitors used as either MLCC or bulk capacitors.** Their inductances are used in the higher frequency peak; their capacitances are used in the lower frequency peak.

**Line 34 is the value of the capacitor used on the board.** In this spreadsheet, we assume only one value of capacitance is used. We would have to use a simulation tool to explore multiple capacitor values to provide a flat impedance profile.

**Line 35 is the calculated ESR of the capacitor, assuming a 0402 body size and an MLCC capacitor.** Chapter 5 discussed that we can model the ESR of many MLCC capacitors with a simple relationship based on just the capacitance:

$$\text{ESR} = \frac{0.20 \Omega}{(C[\text{nF}])^{0.43}} \quad (10.30)$$

where

C = the capacitance of the capacitor in nF

ESR= the equivalent series resistance in  $\Omega$ s

***Line 36 is the partial self-inductance of the capacitor body itself.*** The model used to describe the ESL of the capacitor is a simple total loop inductance. We can use this term to assign a minimum loop inductance for the capacitor, usually associated with the body of the capacitor located some distance above the top of the cavity. It varies depending on the location of the cavity in the stackup and the thickness of the dielectric fill inside the capacitor.

***Line 38 is the series resistance of the vias in the board from the capacitor mounting pads to the top of the cavity.*** This is extracted based on the information in the stackup.

***Line 39 is the inductance contribution based on the surface pads connecting the capacitor to the vias.*** This is input based on the depth of the cavity and the number of squares of trace. In this default example, via-in-pad is assumed so this value is very small.

***Line 40 is the loop inductance contribution from the vias in the board extracted from the extraction spreadsheet.*** This is calculated from the extraction sheet shown in Table 10.4.

***Lines 42, 43, and 44 are the final results for the calculated RLC values of the decoupling capacitors.*** A simple series RLC circuit that takes their parallel combination into account is used to model the capacitors.

## 10.9 THE PERFORMANCE FIGURES OF MERIT

The next section of the PRC calculates the important

figures of merit for each impedance peak based on the input information described in the last section. Table 10.7 shows this section of the PRC.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
45	Result	Resonant loop capacitance	99.0	9,382	142,100	nF
46	Result	Resonant loop resistance (excluding ODC ESR)	1.548	2.954	1.573	mΩ
47	Result	Resonant loop inductance	132	690	10,510	pH
48	Result	$Z_0$ , Reactance at resonance	36	8.6	8.6	mΩ
49	Result	q-factor (combined from contributors)	2.5	2.4	4.0	
50	Result	q-factor from leakage	9.1	39	39	
51	Result	q-factor from load loss	5.5	23.3	23.3	
52	Result	q-factor from on-die capacitance ESR	15			
53	Result	q-factor from loop resistance (excluding ODC ESR)	24	2.9	5.5	

54		PDN Figures of Merit				
55	FD result	Peak frequency	44.1	1.98	0.130	MHz
56	FD result	Peak impedance	91	21	34	mΩ
57	FD result	PDN ratio (ratio of Z to Z target)	14	3.3	5.5	
58	TD result	Clock-edge droop (impulse response)	45			mV
59	TD result	Step response droop	292	69	69	mV
60	TD result	Resonance response (peak to peak)	922	211	348	mV
61	DC result	DC resistance from VRM to circuits	3.1			mΩ
62	DC result	DC power loss for max current	312			mW

**Table 10.7** Snapshot of the PRC spreadsheet showing the most significant figures of merit for the three loops.

Any impedance peak in the frequency domain has five important performance figures of merit, each described in a line of the PRC:

***Line 55, the resonant frequency of each peak***

***Line 56, the peak impedance of each peak***

***Line 57, the PDN ratio: the ratio of the peak impedance to the target impedance***

## **Line 48, the characteristic impedance of each peak**

### **Line 49, the q-factor associated with each peak**

We calculate each of these terms from the equivalent L, C, and q-factors using the expressions summarized at the beginning of this chapter.

The features of the parallel resonance affect the time domain voltage noise for the three important time domain current waveform stimulations: impulse, step, and resonant.

**Line 58, the clock-edge droop from a single impulse of current from one clock edge.** In a single clock edge, there is an impulse of dynamic current causing the voltage on the die pads to droop. This voltage droop is the “clock-edge droop.” It is fundamentally related to the amount of charge required to charge up the switching capacitance compared to the total on-die capacitance and we find it with

$$V_{\text{clock-edge droop}} = \frac{\Delta Q_{\text{switched-capacitance}}}{C_{\text{ODC}}} = \frac{V_{\text{dd}} \times C_{\text{switching}}}{C_{\text{ODC}}} \quad (10.31)$$

**Line 59, the voltage droop from a fast step transient of current at the maximum transient current.** When the full amount of transient current turns on in a timeframe short compared to the period of the resonant peak frequency, the voltage on the die pads droops by a much larger amount than the impulse response. This step response voltage droop depends on the characteristic impedance of the resonant peak and the step transient current. We find the droop with

$$V_{\text{step edge droop}} = I_{\text{transient}} \times Z_0 = I_{\text{transient}} \times \sqrt{\frac{L}{C}} \quad (10.32)$$

### **Line 60, the peak-to-peak voltage response of**

**a resonant square wave of current.** The third important transient response is when a square wave of transient current stimulation is driven at the peak resonant frequency. This is generally the worst-case voltage on the PDN. As we showed in [Chapter 9](#), the peak voltage is reached after the current load has a number of square wave cycles approximately equal to the q-factor, driven at the resonant frequency.

We find the peak voltage, after a square wave of transient current at the resonant frequency, applied for at least a q-factor of cycles as

$$V_{pk-pk} = I_{pk-pk} Z_{peak} = \frac{4}{\pi} I_{transient} \times \text{q-factor} \times Z_0 \quad (10.33)$$

In general, a PDN topology with three loops produces three impedance peaks. This assumes that a significant amount of inductance separates the capacitive branches. The significant horizontal inductance, in the direction of power flow from the ideal voltage source to the load, produces the three distinct impedance peaks, in this case about a decade apart.

The PDN Resonance Calculator is useful to estimate individual impedance peaks when they are well-separated. The three distinct frequency domain peaks give rise to a first, second, and third droop in the time domain.

The first time domain droop is associated with the highest frequency impedance peak; the second droop is associated with the middle frequency peak; and the third droop is associated with the lowest frequency peak. This can happen in systems that have significant package inductance and have a significantly inductive path from the VRM to the high-frequency board capacitors.

Next, we begin an analysis by looking at a poorly

optimized PDN system. This is useful to make some important points about resonances, q-factors, and transient current rise times.

Later in this chapter we will optimize the three-peak PDN by placing additional capacitive branches between power and ground to break up some of the significant inductances between the branches. This is essentially the FDTIM (frequency domain target impedance method) for making the PDN impedance flat over a broad frequency range.

With the additional resonant loops, the impedance peaks become blurred together and form the desired flat impedance profile. When this happens, the PRC system-level spreadsheet becomes less useful and you should use a circuit simulator to evaluate the PDN.

**Tip**

Regardless of the flatness of the rest of the PDN, generally, for economic reasons, there will be a Bandini mountain between the on-die capacitance and next capacitive branch. This sets up a resonance between the bump-loop inductance and the on-die capacitance. The PRC spreadsheet predicts well this most important impedance peak and its impact on the stimulated transient voltages.

## 10.10 SIGNIFICANCE OF DAMPING AND Q-FACTORS

The damping that comes from PDN power losses is often the hardest part of getting good model-to-hardware correlation. As discussed in [Chapter 8](#), we can often measure or ascertain the on-die capacitance from the SPICE models of the on-die transistor-level circuitry.

We can estimate inductance by approximations or by 3D field solver tools based on the specific geometry. With some effort, we can estimate and check the inductance and capacitance elements for a PDN by the

measured resonant frequency. This section concentrates on loss, damping, and q-factor. This is important because it determines the height of the impedance peak, which is simply the product of characteristic impedance and the q-factor:

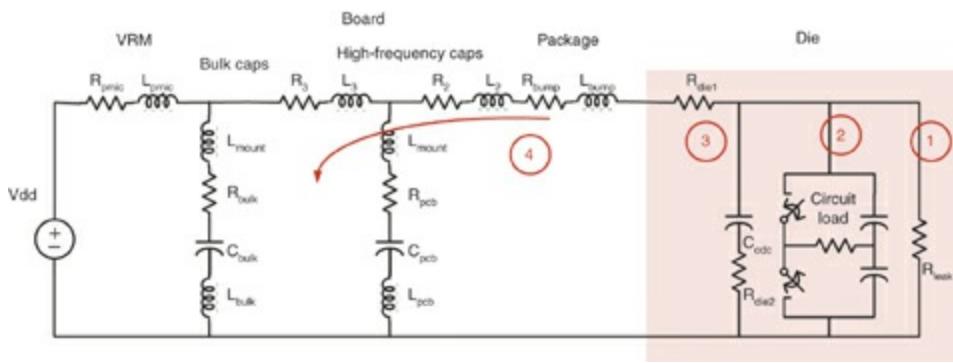
$$Z_{\text{peak}} = \text{q-factor} \times Z_0 \quad (10.34)$$

Note that the peak impedance is directly proportional to the q-factor. A larger q-factor means a higher peak impedance, which is undesirable. Generally, we seek to engineer lower q-factors to keep peak impedances low.

We identify four major sources of damping as illustrated in Figure 10.9:

- Leakage
- Load loss
- ESR for the on-die capacitance
- Bump-loop resistance

If these mechanisms provide insufficient damping (too large a q-factor), we can add more damping by intentionally placing resistance in series with on-die capacitance to absorb resonant power.



**Figure 10.9** Circuit model identifying the four sources of damping contributing to q-factors: leakage, load loss, ESR of the on-die capacitance, and bump-loop resistance.

Lines 49 through 53 of the PDN Resonance Calculator, as shown in Table 10.8, deal with q-factor

and damping for these mechanisms. Peak 1 (Bandini Mountain) is the most important impedance peak so we will concentrate there. We calculate, evaluate, and simulate the q-factor contribution for each of these independent mechanisms one at a time. This enables us to identify and quantify the dominant q-factor. This is important because it helps us focus on the most fruitful area for effort and expense when managing the overall q-factor.

<b>25</b>	<b>Type</b>	<b>Peak Analysis</b>	<b>Loop 1 (Peak 1)</b>	<b>Loop 2 (Peak 2)</b>	<b>Loop 3 (Peak 3)</b>
49	Result	q-factor (combined from contributors)	2.5	2.4	4.0
50	Result	q-factor from leakage	9.1	39	39
51	Result	q-factor from load loss	5.5	23.3	23.3
52	Result	q-factor from on-die capacitance ESR	15		
53	Result	q-factor from loop resistance (excluding ODC ESR)	24	2.9	5.5

**Table 10.8** Section of the PRC spreadsheet showing the calculated q-factors from the four different sources for the Bandini Mountain. (A smaller value is better.)

To quantify individual q-factors, we have to determine whether the loss mechanism is in series or parallel with the resonant circuit.

To evaluate the appropriate q-factors for the several loss mechanisms, we first have to identify the resonant loop. The Bandini peak comes from the on-die capacitance resonating with the bump-loop inductance. The resonant mechanism involves electric field energy being stored in the on-die capacitance for some period of time as voltage. Then current flows and transfers some of this electric field energy into magnetic field energy in the loop during another period of time. Because current is flowing around this loop, it is a series circuit. The loss mechanism is from current flowing through the series loop resistance. Two of our loss

mechanisms reside here.

We choose to separate them into the die loss associated with the ESR of the on-die capacitance and the bump-loop resistance found in the rest of the series path. The loop includes copper material resistance, skin effect losses, and on-die capacitor ESR. By separating mechanisms in this manner, we can assign a loss value to the die and a loss value to the package/board.

When the resistive loss term is in parallel with the reactive elements, the q-factor is

$$q_n = \frac{R_n}{Z_0} \quad (10.35)$$

where

$q_n$  = the q-factor from each source

$Z_0$  = the characteristic impedance of the loop

$R_n$  = the equivalent parallel resistance of the loss mechanism

When the resistive loss term is in series with the reactive elements, so resonant current flows through the resistance, we get the q-factor with

$$q_n = \frac{Z_0}{R_n} \quad (10.36)$$

where

$q_n$  = the q-factor from each source

$Z_0$  = the characteristic impedance of the loop

$R_n$  = the equivalent series resistance of the loss mechanism

The parallel resistance (conductance) of the leakage element is in parallel with the capacitance and inductance of this resonant circuit. The q-factor associated with the leakage loss is simply the leakage

resistance divided by  $Z_0$ . The leakage current goes as the cube of the PDN voltage so we have to use the dynamic resistance (slope) evaluated at the specific PDN voltage:

$$q_1 = \frac{R_{\text{leakage}}}{Z_0} = \frac{1}{G_{\text{leakage}} Z_0} \quad (10.37)$$

where

$q_1$  = the q-factor from the parallel, on-die leakage resistance

$Z_0$  = the characteristic impedance of the Bandini Mountain

$R_{\text{leakage}}$  = the equivalent parallel resistance of the on-die leakage resistance

$G_{\text{leakage}}$  = the conductance of the leakage resistance

The load conductance is also in parallel with the resonant loop. The q-factor associated with the load loss is the load resistance divided by  $Z_0$ :

$$q_2 = \frac{R_{\text{load}}}{Z_0} = \frac{1}{G_{\text{load}} Z_0} \quad (10.38)$$

where

$q_2$  = the q-factor from the parallel, load loss resistance

$Z_0$  = the characteristic impedance of the Bandini Mountain

$R_{\text{load}}$  = the equivalent parallel resistance of the load loss resistance

$G_{\text{load}}$  = the conductance of the load loss resistance

Higher current drawn by the circuits on the die means more PDN load current and a lower parallel resistance. This results in a lower q-factor. This is an important loss mechanism. With more current flowing in the PDN, the q-factor is lower.

The on-die series resistance and the series resistance

of the loop resistance from the mounting interconnects are both in series. Their q-factors are

$$q_3 = \frac{Z_0}{R_{ODC-ESR}} \quad \text{and} \quad q_4 = \frac{Z_0}{R_{loop-ESR}} \quad (10.39)$$

where

$q_3$  = the q-factor from the on-die capacitor's ESR

$q_4$  = the q-factor from the die-attach bump package lead loop series resistance

$Z_0$  = the characteristic impedance of the loop

$R_{ODC-ESR}$  = the equivalent series resistance of the on-die capacitor's resistance

$R_{loop-ESR}$  = the equivalent series resistance of the chip-package mounting loop

Now that we have evaluated the q-factors associated with the independent loss mechanisms, we need to combine them to get an overall q-factor. Q-factors behave like resistors in parallel. The overall q-factor is 1 over the sum of the q-factor reciprocals. This means the overall q-factor is dominated by the lowest value q-factor:

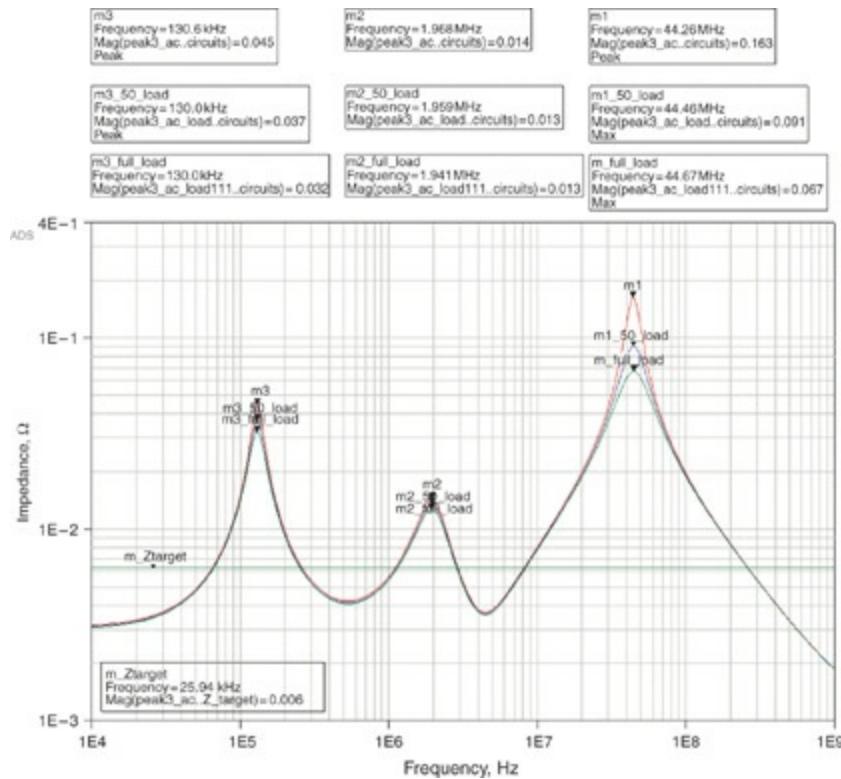
$$q_{all} = \frac{1}{\frac{1}{q_1} + \frac{1}{q_2} + \frac{1}{q_3} + \frac{1}{q_4} \dots} \quad (10.40)$$

Looking at the q-factor values in the table, the load damping is the lowest and dominates. The second most important contributor to q-factor is leakage. These two loss mechanisms are often overlooked when simulating impedance peaks in the frequency domain, yet they are the most influential. In this example we would have overlooked the two most important loss mechanisms if we did not include the load loss and leakage loss in a frequency domain simulation.

### Tip

The two most dominant sources of loss and lower q-factor for this PDN are load loss due to intentional PDN current, and leakage current, an unintentional PDN current sink. Yet, these two terms are often left out of PDN simulations.

**Figure 10.10** is a frequency domain simulation for the three-peak PDN using the same parameters as in the PRC spreadsheet. Peak 1, the Bandini Mountain, is most prominent at 44 MHz. We performed the simulation with and without the load to establish correlation with the PDN Resonance Calculator.



**Figure 10.10** Simulated impedance profiles of the three peaks with the parameters from the PDN resonance calculator spreadsheet using Keysight ADS. The higher peaks are based on ignoring the load loss q-factors. The lower peak heights are based on using a more realistic q-factor that is appropriate for a fully resonating PDN.

Note the very close agreement between the circuit simulation peak heights and the PRC spreadsheet results.

In this simulation, we selected three different load conditions to illustrate the importance of load loss on q-factor and impedance peak height:

- No load damping
- Maximum current load of 9 A
- Maximum transient current of 8 A, 1 A leakage current, and 50% duty cycle

First, let's consider the impedance profile without the benefit of damping from the load. This is the highest impedance curve, with a peak value of  $0.163 \Omega$ . Table 10.9 gives the calculated q-factors and the expected impedance peak parameters for this higher q-factor case. We have forced the q-factor from load loss to be 1,000 to make it an insignificant contributor to q-factor calculations.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
49	Result	q-factor (combined from contributors)	4.5	2.4	4.0	
50	Result	q-factor from leakage	9.1	39	39	
51	Result	q-factor from load loss	1000	23.3	23.3	
52	Result	q-factor from on-die capacitance ESR	15			
53	Result	q-factor from loop resistance (excluding ODC ESR)	24	2.9	5.5	
54		<b>PDN Figures of Merit</b>				
55	FD result	Peak frequency	44.1	1.98	0.130	MHz
56	FD result	Peak impedance	165	21	34	$m\Omega$

**Table 10.9** The q-factor values and the PRC predicted peak frequencies and peak impedances for each of the three loops with no load damping.

The calculated resonant frequencies and impedance peak heights line up remarkably well with the markers on the top curve of the ADS simulation. The 44.10 MHz resonant frequency from the PRC is nearly the same as the 44.26 MHz simulated peak. There is excellent agreement between the PRC peak height of  $165 m\Omega$  compared to the simulated value of  $163 m\Omega$ . To get this level of agreement, we must consider the inductive and resistive paths of the high frequency and bulk caps in

parallel.

Next, we placed a  $0.111\ \Omega$  ( $1\ \text{V}/9\ \text{A}$ ) load resistor in the load position in parallel to the on-die capacitance for the frequency domain simulation. As shown in [Table 10.10](#), the q-factor from the steady  $9\ \text{A}$  dynamic load is 3.0 and totally dominates the overall q-factor, bringing it down to 1.8. This is less than half of the no-load q-factor. The PRC predicted impedance height is  $66\ \text{m}\Omega$  and the simulated impedance peak is  $67\ \text{m}\Omega$ . Once again, the PRC calculated values for the impedance peak frequency and height compare favorably with the markers in the ADS simulation.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
49	Result	q-factor (combined from contributors)	1.8	2.4	4.0	
50	Result	q-factor from leakage	9.1	39	39	
51	Result	q-factor from load loss	3.0	23.3	23.3	
52	Result	q-factor from on-die capacitance ESR	15			
53	Result	q-factor from loop resistance (excluding ODC ESR)	24	2.9	5.5	
54		PDN Figures of Merit				
55	FD result	Peak frequency	44.1	1.98	0.130	MHz
56	FD result	Peak impedance	66	21	34	$\text{m}\Omega$

**Table 10.10** The q-factor values and the PRC predicted peak frequencies and peak impedances for each of the three loops with a full-current load of  $9\ \text{A}$ .

However, a constant, full  $9\ \text{A}$  load has no transient current so a low q-factor is not relevant. A more interesting case is when  $8\ \text{A}$  of transient current ( $9\ \text{A} - 1\ \text{A}$ ) is consumed as shown in the original PRC spreadsheet. This is in addition to the  $1\ \text{A}$  of leakage current. When the  $8\ \text{A}$  transient current is repeated at the PDN resonant frequency, the q-factor for damping is very important.

With a 50% duty cycle, the time average current is

used to get the equivalent damping for the dynamic load of  $1 \text{ V}/((9 \text{ A} + 1 \text{ A})/2) = 0.200 \Omega$ . This gives a q-factor of 5.5 for the load contribution and an overall q-factor of 2.5 as repeated in [Table 10.11](#). The PRC and simulated heights for the 50% duty cycle impedance peak are both 91 mΩ.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
49	Result	q-factor (combined from contributors)	2.5	2.4	4.0	
50	Result	q-factor from leakage	9.1	39	39	
51	Result	q-factor from load loss	5.5	23.3	23.3	
52	Result	q-factor from on-die capacitance ESR	15			
53	Result	q-factor from loop resistance (excluding ODC ESR)	24	2.9	5.5	
54		<b>PDN Figures of Merit</b>				
55	FD result	Peak frequency	44.1	1.98	0.130	MHz
56	FD result	Peak impedance	91	21	34	mΩ

**Table 10.11** The q-factor values and the PRC predicted peak frequencies and peak impedances for each of the three loops with a 50% duty cycle of 8 A transient current. This is the q-factor simulated in the circuit simulation, showing good agreement with the PRC prediction.

So far, good correlation has been established between the PDN Resonance Calculator and frequency domain simulation for unloaded, 50%, and fully loaded impedance profiles. This is an example of how to bring the properties of a very non-linear die load into the frequency domain by time averaging the current. This allows us to do frequency domain analysis on a die that is switching capacitive loads as a function of time.

#### Tip

This exercise illustrates the value of using simple assumptions and a spreadsheet analysis to accurately predict the expected figures of merit of a frequency domain simulation.

Clearly the load damping is important and depends greatly on the load current, which varies with time. The assumptions for the current profiles have a large influence on the load damping, more than a factor of two. Truly understanding the effects of load damping requires a time domain simulation.

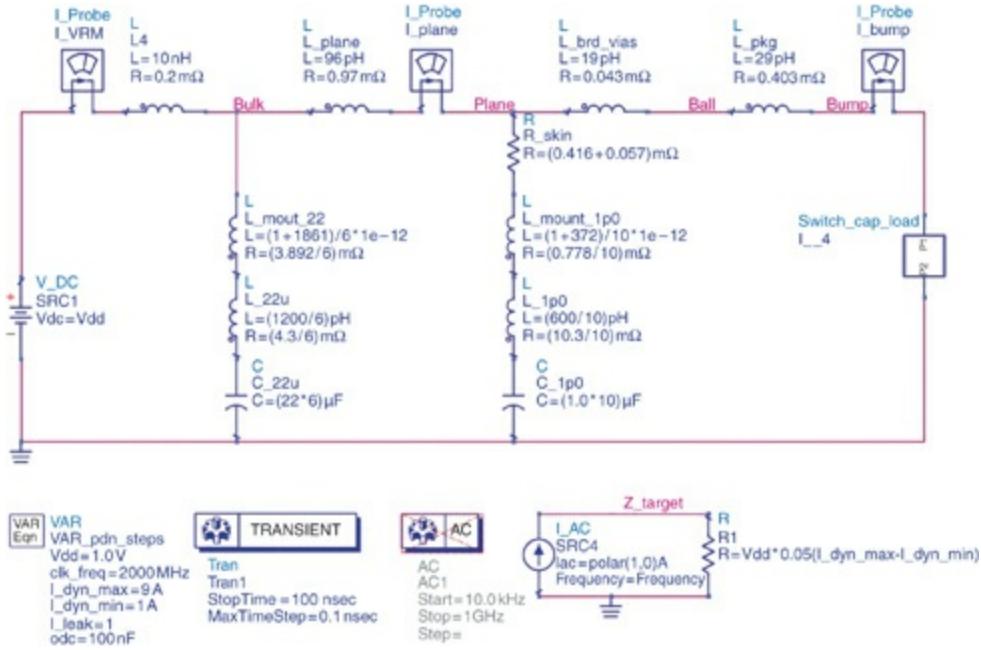
Next, we will establish time domain simulation correlation with PRC, and then return to a discussion on q-factor that involves correlation in both the frequency and time domains with the PRC. The time averaging of loss for frequency domain analysis is validated by time domain analysis with a switched capacitor load. We will evaluate q-factors for individual loss mechanisms identified in the PRC one at a time. Knowing the contributions from the individual loss mechanisms when attempting to manage the overall loss and q-factor is important.

## **10.11 USING A SWITCHED CAPACITOR LOAD MODEL TO STIMULATE THE PDN**

The preceding discussion pointed out the importance of including damping in estimating the peak impedances and the resulting transient responses. In the initial frequency domain analysis, we used a resistor to model the load for several transient currents. The load reduced the impedance peak by more than a factor of two compared to when it was not included. As we showed in the last chapter, the chip load is not really resistive; it is dynamic. A more realistic model of the load is a pair of switched capacitors. We can simulate this by using a more sophisticated switched capacitor load model in the time domain.

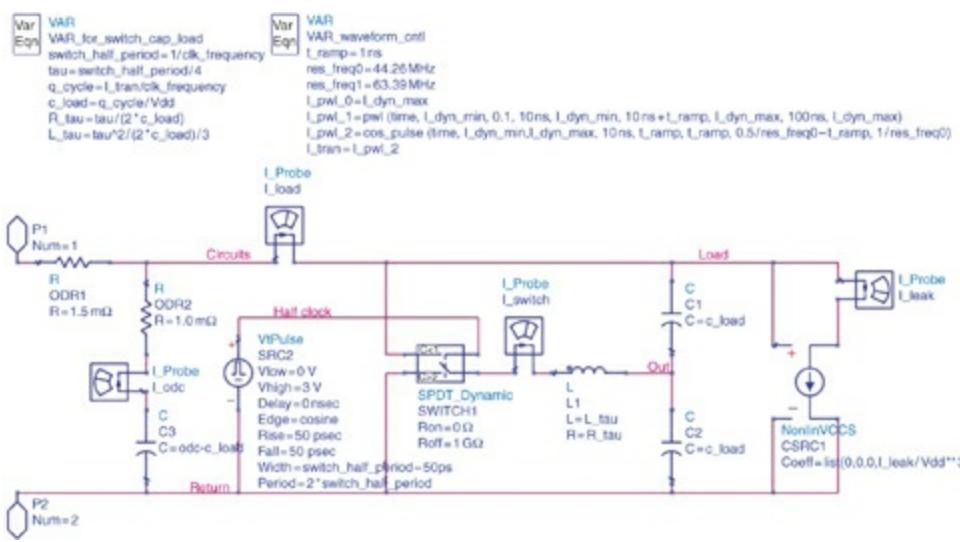
We have simulated the same PDN—whose system-level parameters we developed in the PDN Resonance Calculator spreadsheet and simulated in the frequency

domain—in the time domain with ADS. We use the circuit parameters from the PRC to estimate the frequency and time domain performance (impedance peak, q-factor, voltage droops, and so on). Figure 10.11 shows the circuit topology for the system parameters.



**Figure 10.11** Top-level circuit model used in ADS to simulate the switched capacitor model for the load. This circuit has three loops with parameter values based on the specific condition illustrated in the default values of the PDN resonant calculator.

For convenience, we separated the die from the package and board and show it as a subcircuit called switch\_cap\_load on the right side of the top-level diagram. Figure 10.12 shows the circuit schematic for the switched capacitor load used in this analysis. It contains all the on-die capacitance and associated parasitic resistance, which is shown on the left side of the schematic.



**Figure 10.12** Circuit used to simulate the switched capacitance transient current from the die. This is the subcircuit that represents the load in the complete PDN circuit.

As discussed in [Chapter 9](#), the switched load capacitance borrows some capacitance from the on-die capacitance and uses it to draw charge impulses from the PDN during each clock cycle. Zero switched capacitance draws zero dynamic current. A greater switched load capacitance draws more dynamic current. The switch factor is the amount of switched capacitance load expressed as a percentage of the total on-die capacitance.

Building a simple circuit to emulate the actual, complex current profile of switching gates on die requires a few tricks. In this circuit, L<sub>1</sub> is a fictitious inductor that is there to optimize the shape of the current impulses. The L<sub>tau</sub> and R<sub>tau</sub> parameters are calculated so that an impulse waveform completes just barely before the clock cycle period expires.

The variables defined under VAR\_for\_switch\_cap\_load adjust the parameters of this pulse shaping circuit to fit within the specified clock frequency. This causes the switched capacitor load to draw the dynamic current specified in the top-level schematic by generating charge impulses at the clock

frequency.

We use the variables under VAR\_waveform\_cntl to adjust the transient current profile shaping. We define two piece-wise-linear (PWL) waveforms, one for step response and the other for resonance response. In general, we can define the current ramp rate and any general current waveform by PWL equations in this section.

The I\_tran variable is a function of time and causes the value of c\_load to be a function of time. Many circuit simulators including ADS complain about this but go ahead and do it as intended in this circuit.

Also included in the die and the switched capacitor load circuit is a leakage element. Leakage is sometimes represented by a shunt resistor that gives a leakage current that is proportional to PDN voltage. However, leakage is often a much stronger function of voltage. Some recent technology nodes have leakage that is approximately proportional to the voltage cubed. The coefficients for the voltage controlled current source are set up to for this, which is important for damping.

## **10.12 IMPULSE, STEP, AND RESONANCE RESPONSE FOR THREE-PEAK PDN: CORRELATION TO TRANSIENT SIMULATION**

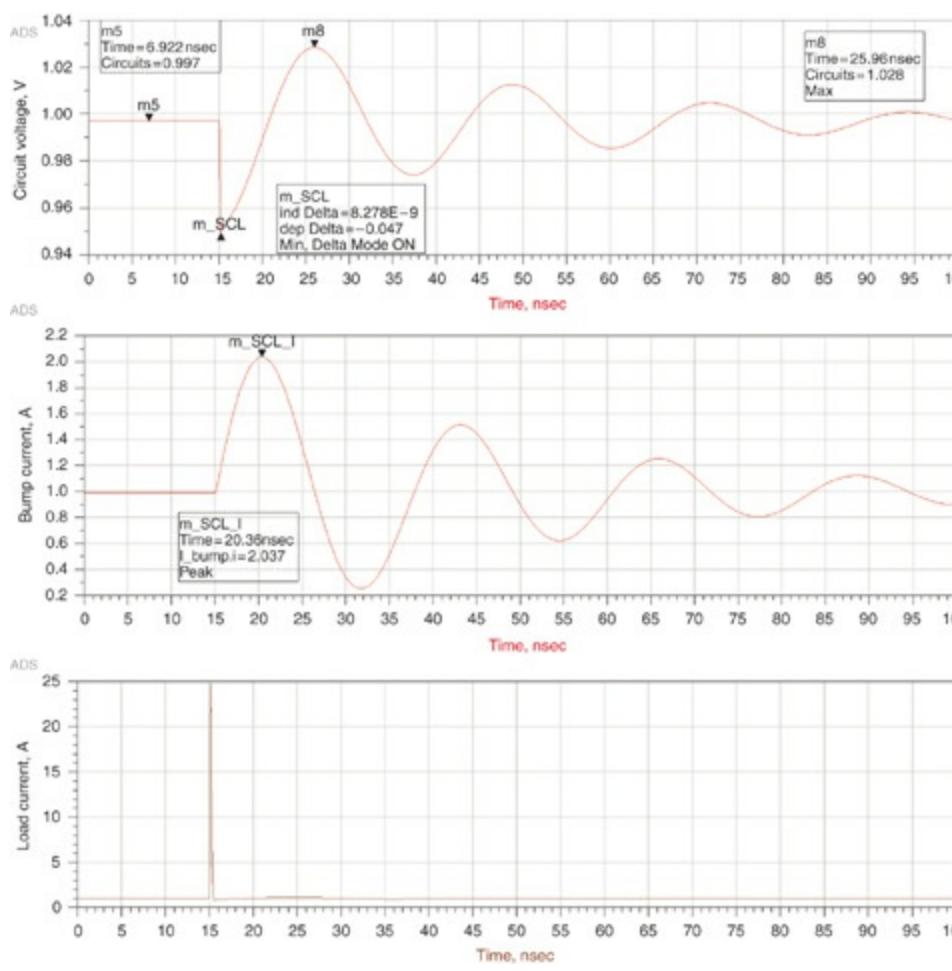
In this section we examine the three time domain waveforms discussed in [Chapter 9](#) in conjunction with the three-peak PDN: impulse, step, and resonance response. [Table 10.12](#) shows the time domain figures of merit predicted by the PRC.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
58	TD result	Clock-edge droop (impulse response)	45			mV
59	TD result	Step response droop	292	69	69	mV
60	TD result	Resonance response (peak to peak)	922	211	348	mV

**Table 10.12** Summary of the PRC terms for the time domain response to the impulse, step, and resonant response for each of the three loops.

The load damping assumption for these terms is 50% the duty cycle of 8 A, which is the maximum resonant current. The load damping is about half of what it is for full current, but full current does not have any transient current. It is more important to consider the case where resonant current is maximum, which means that the load damping is about half of what it is for full current. This is the default condition for the spreadsheet and represents the worst thing that can happen for this PDN.

Figure 10.13 shows the simulated impulse response using the switched capacitor load circuit. The load has been used to draw a current impulse of 4.5 nC as calculated in line 15 of the PRC. This is the impulse of current the PDN draws at 15 ns into the simulation.



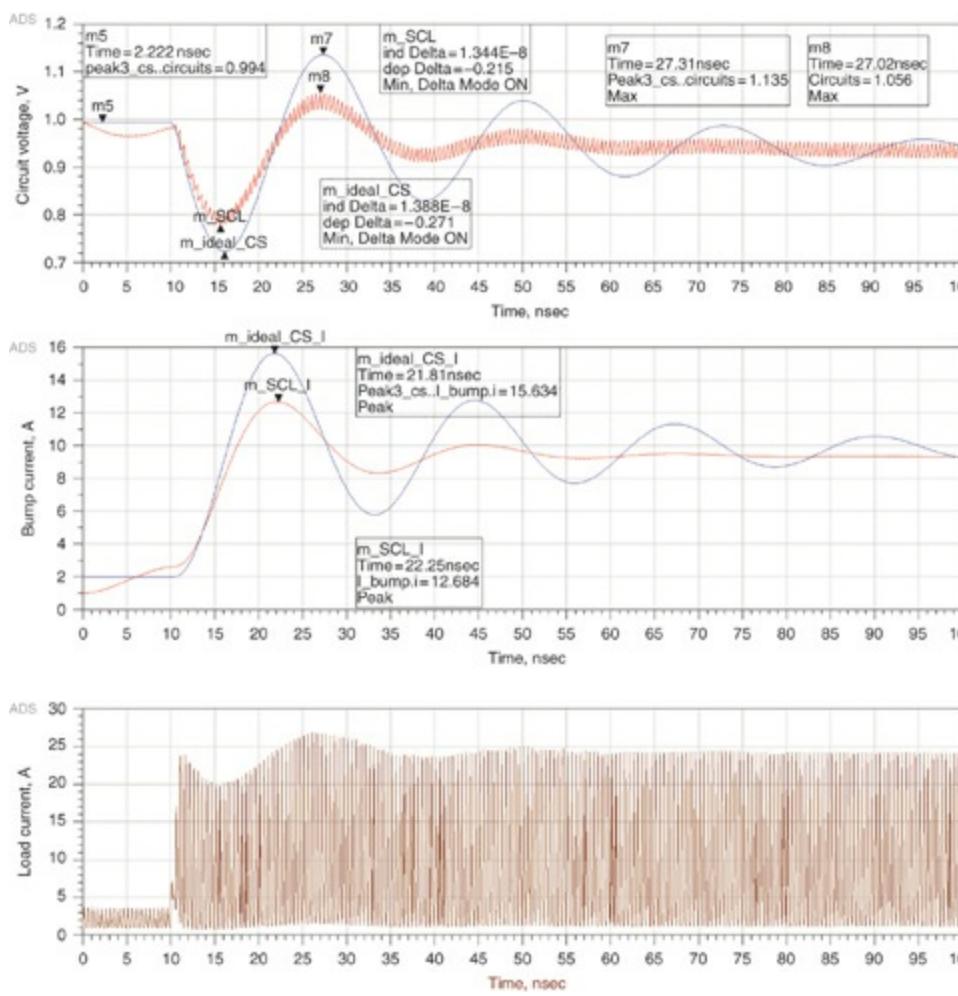
**Figure 10.13** Simulated response for an impulse of current generated by the switched capacitor load from one clock edge. **Top trace:** The simulated voltage on the die pads from the impulse of dynamic current drawn from the die. **Middle trace:** The simulated current flowing through the package and from the board-level PDN elements. Note the filtered response and much lower peak current. **Bottom trace:** The single clock edge of current drawn by the die from the PDN circuit 15 ns into the simulation. This has a 25 A current peak!

The current profile from the on-die capacitance peaks out at 25 A and completes within 0.5 ns as shown in the bottom panel of the figure. The middle panel shows the PDN current response measured in the die bump branch. The on-die capacitance and the bump-loop inductance have filtered this waveform. It peaks at 2 A, 5 ns after the impulse event and dips to 0.2 A before ringing out in the characteristic damped sinusoid. Leakage current is nominally 1 A but varies with the PDN voltage.

The top panel shows the die voltage for the impulse event. The voltage reaches its maximum droop 0.5 ns after the impulse event. At that time, all the 4.5 nF of charge drawn by the load has been consumed from the on-die capacitance. The droop predicted in line 58 of the PRC is 45 mV and the simulated droop is 47 mV, good correlation. The remainder of the voltage curve is the ring out of the PDN impulse response and clearly shows the PDN resonant frequency and damping.

The ringing has pretty much died out after four cycles and confirms the 4.5 q-factor shown on line 49 of the no-load snippet of the PRC in [Table 10.9](#). The no-load q-factor is used because after the clock edge, no load current is flowing and no damping exists in the transient response from this term.

[Figure 10.14](#) shows the step response. This is when the clock turns on after an idle state and the maximum transient current suddenly turns on in just 1 ns. This is the stimulation of the Bandini Mountain. The step response also stimulates other impedance peaks with longer simulated time.



**Figure 10.14** Step response for the three-peak PDN, comparing the stimulated response by an ideal current source and by a switched capacitor load. **Top trace:** Voltage stimulated on the die pads from the two different current models flowing through the same PDN model. **Middle:** Current flowing from the circuit board through the package into the die for the two different current models. **Bottom:** The transient load current drawn by the switched capacitor load. The ideal current source is just a step edge.

The lower panel shows the current impulses consumed by the switched capacitor load. The impulse current profile as a function of die voltage is obvious. As the die voltage changes, due to the ringing response of the PDN impedance profile, the load current also changes because the on-die capacitance is charged up to a voltage profile in time and stores a charge that is a function of time.

The middle panel shows the current in the bump

branch, which the ODC and bump-loop inductance has filtered. [Figure 10.14](#) shows the waveforms for both the switched capacitor load and an ideal current source load. The switched capacitor load current peaks at 12 A. The profile is more damped because of load loss and the q-factor appears to be 2 or less. The waveform produced by the ideal current source load peaks at 15 A and does not benefit from load damping. It rings out with a q-factor of about 4.

**Tip**

This comparison clearly shows the impact of the more realistic switched capacitor load model in providing more damping than assuming a constant current step. This means that the actual voltage noise on the die pads is probably going to be less than that simulated based on a simple ideal current step. This is the source of some additional design margin built into the PDN.

The final value of the switched capacitor load current is a little less than the ideal current source because DC IR drop has reduced the die voltage. Slightly less average current is consumed because less charge is consumed by the capacitive load with less PDN voltage.

The top panel shows the voltage waveforms for both loads. The ideal current source produces a deeper droop than the switched capacitor load as expected because the ideal current does not reduce at reduced voltage. Just like the current waveforms, the switched capacitor load has more damping than the ideal current source load.

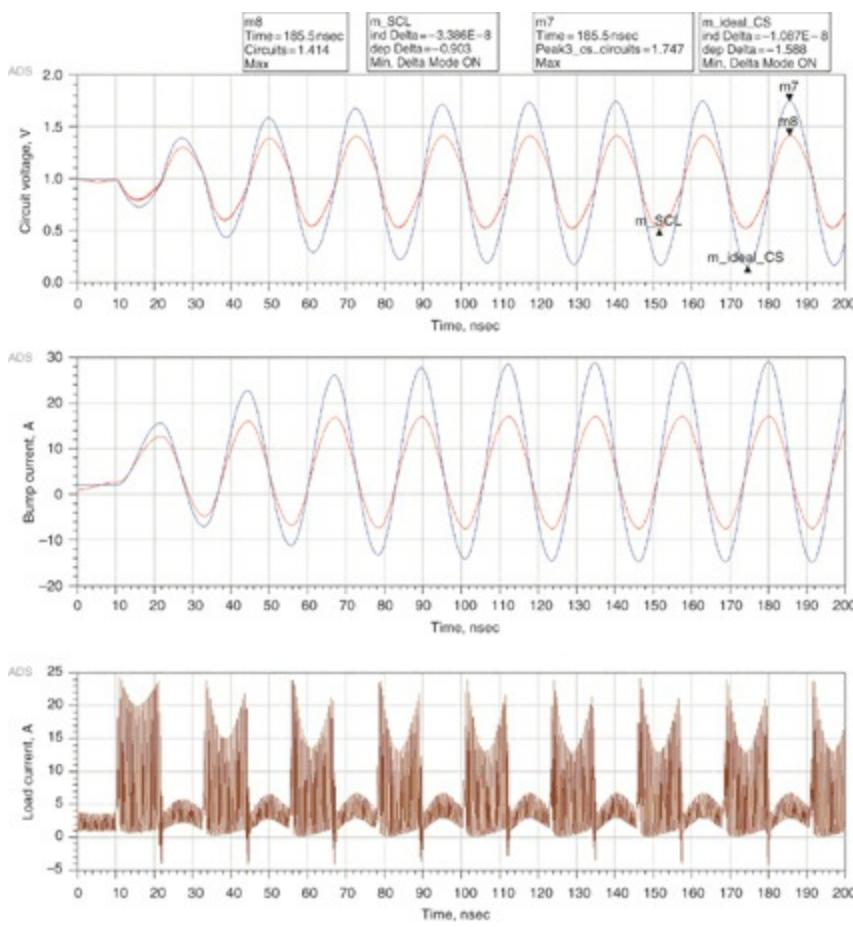
The step response droop of 292 mV calculated in the PRC is for the full transient current step consumed by the ideal current source. Therefore, we should compare the PRC to the simulated ideal current source droop, which was 271 mV. An 8 A transient current was assumed. The switched capacitor load circuit will not produce the full 8 A transient because of PDN voltage droop. The ideal current source simulated droop is

somewhat less than the PRC predicted droop because of the leakage load, which draws current proportional to the voltage cubed. It consumes significantly less current as the PDN droops, leading to reduced step current.

**Tip**

These interactions of the instantaneous voltage affecting the leakage current and the charge on the die and the resulting transient current are too complicated for a spreadsheet; we must analyze them in a circuit simulator.

Finally, [Figure 10.15](#) shows the third significant current waveform response, the resonance response. The transient current is nominally  $9 \text{ A} - 1 \text{ A} = 8 \text{ A}$ . The lower panel shows the profile of current impulses, which are clearly influenced by the PDN voltage when the switched capacitor load is used. As the resonance grows, the impulse profile is affected. In the high-current periods (8 A), the switched capacitor load current sags because the PDN voltage sags. In the low-current periods (1 A) the current peaks up because the PDN voltage peaks up and leakage current increases.



**Figure 10.15** Transient response from a resonant excitation of the three-peak PDN stimulated by an ideal current source and a switched capacitor load. **Top:** Stimulated voltage on the die pads from the two different current models. The switched capacitor load model, which includes the dynamic damping, shows a smaller peak height. **Middle:** The current flowing from the circuit board through the package leads and die pads into the die, filtered by the Bandini Mountain parallel resonance. The larger peak current is from the ideal current source. **Bottom:** The load current switching on-die with a capacitive load that changes in a square wave.

The middle panel shows the current in the bump branch. As the resonance builds up periods of time occur where the current is negative, indicating that current flows both into and out of the package in certain time periods. Electric field energy is stored and released from the on-die capacitance and magnetic field energy is stored and released from the package loop inductance in an alternating fashion as is common in any parallel resonance. A larger current waveform builds up for the

ideal current source load because it does not benefit from load damping the way the switched capacitor load does.

The top panel shows the die voltage waveform. As expected, the switched capacitor load produces less p-p noise because of the damping from load loss. The PRC spreadsheet predicted 922 mV p-p and we should compare it to the switch capacitor load simulation, which is 903 mV. The q-factor for  $9 \text{ A} - 1 \text{ A} = 8 \text{ A}$  transient was used in the PRC calculation. The agreement between the simple estimate in the spreadsheet and the circuit simulation is very good. The ideal current source load with no load damping produces a whopping 1.588 V p-p.

Finally, Table 10.13 shows all the PDN figures of merit.

25	Type	Peak Analysis	Loop 1 (Peak 1)	Loop 2 (Peak 2)	Loop 3 (Peak 3)	Units
54		PDN Figures of Merit				
55	FD result	Peak frequency	44.1	1.98	0.130	MHz
56	FD result	Peak impedance	91	21	34	mΩ
57	FD result	PDN ratio (ratio of Z to Z target)	14	3.3	5.5	
58	TD result	Clock-edge droop (impulse response)	45			mV
59	TD result	Step response droop	292	69	69	mV
60	TD result	Resonance response (peak to peak)	922	211	348	mV
61	DC result	DC resistance from VRM to circuits	3.1			mΩ
62	DC result	DC power loss for max current	312			mW

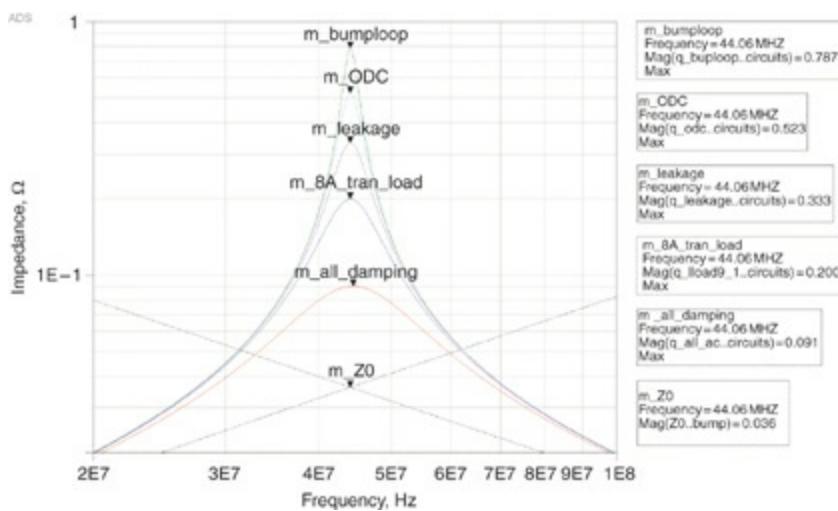
**Table 10.13** Summary of the figures of merit for the PDN as calculated in the PRC for each of the three loops.

## 10.13 INDIVIDUAL Q-FACTORS IN BOTH THE FREQUENCY AND TIME DOMAINS

In this section we evaluate the impact from the various q-factors in both the frequency and time domain. We first isolate each of the four damping mechanisms: the

bump-loop resistance, the ODC resistance, the leakage current, and the switched capacitor load damping. One at a time, each mechanism is included in the circuit model with the on-die capacitance and package-bump-loop inductance to evaluate the resulting peak impedance. We do this by reducing all series damping resistors to zero and increasing all parallel resistors to a very high number, except for the one under consideration. Finally, we include all four damping mechanisms together. We expect that a smaller q-factor and more damping will lead toward lower impedance peak heights.

Figure 10.16 shows the frequency domain simulation of the impedance profile when each source of damping is individually included. The crossing of the inductive and capacitive reactances at the characteristic impedance  $Z_0$  is, of course, the same for each condition and is shown in the bottom of the figure. In the simulation, the characteristic impedance is extracted as  $36 \text{ m}\Omega$  compared to the PRC value of  $36 \text{ m}\Omega$ . We simulated the reactive impedance crossing by disconnecting the on-die capacitance from the inductive bump-loop circuitry and evaluating each separately. The individual q-factors are always the ratio of the impedance peak to  $Z_0$ .



**Figure 10.16** Simulated impedance profiles for the same ODC and bump-loop inductance, but with each damping mechanism evaluated individually. Also included are the characteristic impedance and the impedance with all the damping terms included.

Table 10.14 compares the calculated impedance peak from the PRC with the simulated peak. The appropriate series resistance has been zeroed out and the parallel resistance raised to a very high number except for the mechanism under consideration. This is very similar to what was done in simulation. The agreement is excellent, especially for the lower impedance peaks. Probably some loss mechanisms not completely turned off in the simulation slightly lowered the impedance peaks.

Individual Damping Mechanism	PRC Z Peak ( $\text{m}\Omega$ )	Simulated Z Peak ( $\text{m}\Omega$ )
Leakage	333	333
Load loss	200	200
On-die capacitor ESR	530	523
PDN loop resistance	854	787
All mechanisms	91	91

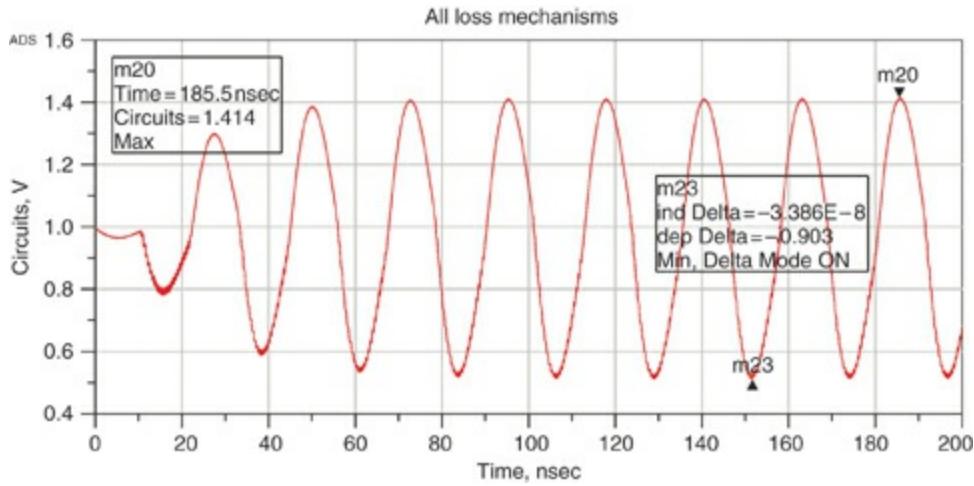
**Table 10.14** Impedance peak predicted by PRC compared to ADS simulation of individual damping mechanisms.

With all damping mechanisms present, the impedance peak is  $91 \text{ m}\Omega$ . This compares exactly to the PRC prediction of  $91 \text{ m}\Omega$ . As expected from the PRC, the

lowest individual damping impedance peak is associated with the load damping and is  $200 \text{ m}\Omega$  for the time averaged transient current of  $9 \text{ A} - 1 \text{ A} = 8 \text{ A}$ . The next higher damped peaks are associated with leakage, ODC, and then bump-loop loss mechanisms. The relative importance of the several damping mechanisms often changes from PDN to PDN and according to the process, voltage, and temperature (PVT) conditions. The combined q-factor from frequency domain simulation is 2.5 and the same as the PRC value of 2.5.

$$\text{q-factor} = \frac{Z_{\text{peak}}}{Z_0} = \frac{91 \text{ m}\Omega}{36 \text{ m}\Omega} = 2.5 \quad (10.41)$$

**Figure 10.17** shows the time domain simulation of the resonant waveform with all damping mechanisms. In this example, we used an 8 A peak-to-peak current, generated from a switched capacitor load model.



**Figure 10.17** The time domain simulation for resonant excitation with all q-factor damping terms included.

The waveform nearly reaches its p-p value after just two complete cycles corresponding to the q-factor of 2.5. The markers indicate that the p-p waveform in the first 200 ns is 0.903 mV. We can use this information to calculate the time domain q-factor. From **Chapter 9**, we know that the p-p voltage at resonance is

$$V_{\text{pk-pk}} = \frac{4}{\pi} I_{\text{transient}} \times Z_{\text{peak}} \quad \text{and} \quad Z_{\text{peak}} = \frac{V_{\text{pk-pk}}}{I_{\text{transient}}} \frac{\pi}{4} \quad (10.42)$$

For this simulation, the resonant forcing function was an ideal 8 A p-p square wave. From this equation and knowledge of the p-p voltage and the transient current, we calculate the  $Z_{\text{peak}}$  to be 89 mΩ. The ratio of the time domain  $Z_{\text{peak}}$  to  $Z_0$  indicates that the q-factor is 2.5, which is the same as the frequency domain and PRC values.

We have now confirmed the q-factor from three different approaches: the PRC, a frequency domain simulation, and a time domain simulation. In the PRC, the resistance and the reactance were used to calculate  $Z_0$ . The calculated  $Z_0$  was used along with the q-factor to predict the impedance peak. In frequency domain simulation, we used the crossing of the reactances to find  $Z_0$  and we found the q-factor from the ratio of the simulated peak to  $Z_0$ . We found the time domain impedance peak from the p-p voltage and back-calculating from the resonant noise prediction, equation 10.42.

#### Tip

These three approaches demonstrate that we can calculate the q-factor from spreadsheet, frequency domain, and time domain techniques with good agreement. They are all self-consistent, reinforcing support for this simple relationship among  $Z_0$ , q-factor, the impedance peak, and p-p time domain resonance noise.

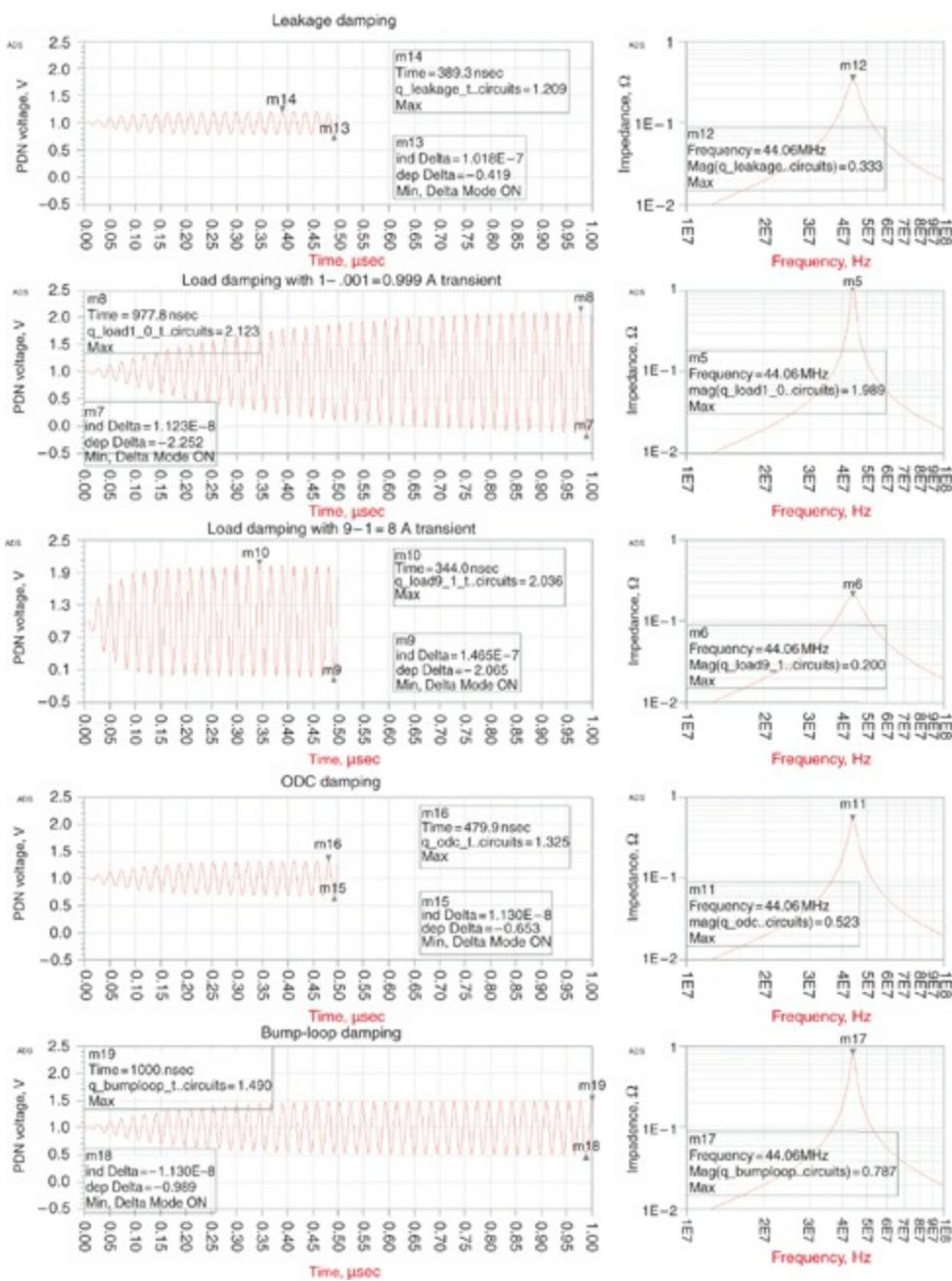
We now examine the individual q-factors mentioned in the PRC discussion in the time domain. We zeroed out all the lumped loss elements of the ADS circuit, eliminating all damping except for the one mechanism under consideration. In these simulations, we used a 1 A peak-to-peak square wave ideal current source as the

stimulus, except when evaluating the load loss term.

The p-p voltage is simulated.

Knowing the transient current, we calculated the time domain impedance peak. We determined the time domain q-factor by dividing the time domain impedance peak by  $Z_0$ .

Figure 10.18 shows both the time domain and frequency domain simulation for one damping mechanism at a time. We accomplished load damping in the time domain with the switched capacitor load using an 8 A peak-to-peak current. To eliminate load damping for the rest of the simulations, we used an ideal square wave current source of 1 A peak to peak rather than a switched capacitor load. The ideal current has no loss because the load current does not depend on PDN voltage.



**Figure 10.18** Transient simulation with a square wave of current excitation at the resonant frequency for RLC circuits including one loss mechanism at a time. The transient response and peak impedance response are very consistent for the individual damping mechanisms.

By examining the individual q-factors in both the frequency and time domains, on the same scale factors, we get a visual image of the importance of each contributor to overall q-factor. We observe that sharp, high impedance peaks are associated with time domain resonant waveforms that slowly build up to high voltages. Voltages in circuits with low q-factor resonances do not build up.

The top panel shows the voltage response with damping from leakage alone. A non-linear source draws current according to the PDN voltage cubed. The time domain simulation uses a 0 to 1 A ideal current source to generate a square wave at the Bandini Mountain frequency, 44.06 MHz. The resonance response rises up to 419 mV p-p. The frequency domain simulation shows an impedance peak of 333 mΩ.

The second panel shows damping from the switched capacitor load. The transient current was between 0.001 A and 1 A because the switched capacitors cannot be completely turned off. The resonant waveform builds up to 2252 mV p-p over 1 us. Clearly this one has a high q-factor because of a small amount of loss with the low load current. The frequency domain simulation uses a 1.998 Ω resistor. We use the time average current of approximately 0.5 A with the die voltage of 1 V to calculate approximately 2 Ω equivalent resistance. As expected, the impedance peak is 1.989 Ω, very close to 2 Ω. We show this panel for reference to demonstrate the large difference that load damping can make.

The third panel shows damping from the switched capacitor load when the transient current is between 1 A and 9 A (8 A transient current). This is consistent with the calculations in the full PRC. The resonant waveform builds up quickly to 2065 mV p-p. There is much more loading in this case compared to the 1 A transient current case and the q-factor is much lower. The interesting thing is that the magnitude of the noise peak is similar to the 1 A transient current case. This is because the noise amplitude is the product of the impedance peak and noise current. The impedance peak is about 8 times higher for the 1 A case compared to the 8 A case. We do the frequency domain simulation with the 200 Ω resistor because the time average dynamic

current is  $(9 + 1)/2 = 5$  A. The frequency domain impedance peak is  $0.200 \Omega$  as expected.

**Tip**

Note that when just including the damping from the current load *only*, the resulting time domain peak-to-peak voltage noise is mostly independent of the current load. Although a low-current load has less driving force, it also sees a higher peak impedance. A high-current load has a high driving force, but the lower q-factor creates a lower peak impedance. In both cases, the product of the current and impedance is about the same.

The fourth panel shows damping from the ESR associated with the on-die capacitance alone. We assume a 250 ps time constant for the RC product. This gives  $2.5 \text{ m}\Omega$  for our 100 nF ODC. The time domain simulation with the ideal current source load builds up to 653 mV p-p over 500 ns. The frequency domain peak from ODC ESR is 523 m $\Omega$ .

The fifth panel shows the damping from the bump-loop alone. This is mostly dominated by the parallel board cap ESR but also includes skin effect losses from the board and package metal. The ideal current source load causes the resonance to build up to 989 mV p-p over 1,000 ns. The frequency domain peak is 787 m $\Omega$ . Note that the bump-loop loss, which involves the board capacitors, is the least important damping mechanism.

We simulated each of the individual loss mechanisms in frequency and time domains. These values compare closely with the PRC calculations. In [Table 10.15](#), we compare the equivalent series or parallel resistance and q-factor from each approach for each individual damping mechanism.

		PRC		ADS FD		ADS TD			
Damping Mechanism	Type	Resistance		Z_peak		I_tran	V_p-p	Z_peak	
q-factor source		mΩ	q-factor	mΩ	q-factor	A	mV	mΩ	q-factor
Leakage resistance	Parallel	333	9.3	333	9.3	1	419	329	9.1
Load resistance: 0.001 to 1 A (switch cap load)	Parallel	1998	55.5	1989	55.3	0.999	2252	1770	49.2
Load resistance: 1 to 9 A (switch cap load)	Parallel	200	5.6	200	5.6	8	2065	203	5.6
On-die capacitance	Series	2.5	14.4	523	14.5	1	653	513	14.2
Bump-loop resistance	Series	1.5	23.3	787	21.9	1	989	777	21.6
Combined q-factor			2.5	91	2.5	8	903	89	2.5
Z <sub>o</sub> (reactance at resonance) mΩ	36.0								

**Table 10.15** Comparing the loss terms from three different analysis approaches: PRC, ADS frequency domain, and ADS time domain. The agreement is remarkable.

The key to many of these calculations is the characteristic impedance, Z<sub>o</sub>. It was calculated to be 36 mΩ in the PRC and simulated to be 36 mΩ in ADS. The ratio of resistance to reactance was used for the PRC q-factor calculations. We calculated the ADS frequency domain q-factor from the height of the impedance peak divided by Z<sub>o</sub>. We found the ADS time domain impedance peak by dividing the peak-peak voltage by the transient current and Fourier coefficient to get the impedance peak. We then divided the time domain impedance peak by Z<sub>o</sub> to find the q-factor, just like the frequency domain.

The table gives the q-factors from the three different methods in the shaded area. The load resistance for 1 A transient current line is shown just for reference. The contrast between 1 A and 8 A load damping

demonstrates the importance of load damping when currents become high. The combined q-factors involve the 8 A transient load in simulation and the 200 mΩ resistor from current calculations. The agreement between PRC, frequency domain, and time domain simulation is very good.

**Tip**

This analysis supports the approach that we can consider each individual loss mechanism one at a time in spreadsheet format, frequency domain simulation, or time domain simulation. We can combine the individual q-factors to find the overall q-factor.

Working with q-factors and identifying the strongest damping mechanism is a powerful technique for managing the height of the impedance peak.

## 10.14 RISE TIME AND STIMULATION OF IMPEDANCE PEAK

In the preceding examples, the transient current turned on in about 1 clock cycle. This means it contains very wide signal bandwidth, from a few times the clock frequency to DC, or as long as we choose to look. This current transient has frequency content that excites all resonances in the PDN impedance profile. However, what if the rise time of the current step doesn't have enough frequency content to excite a specific resonance? The current rise time has a dramatic impact on the stimulated voltage response.

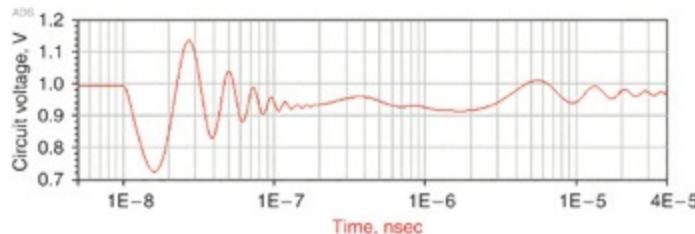
For example, we estimate the bandwidth of a signal with a 1 ns rise time using:

$$BW = \frac{0.35}{RT} = \frac{0.35}{1\text{ nsec}} = 0.35\text{ GHz} = 350\text{ MHz} \quad (10.43)$$

An important consideration is whether the rise time of the current load has sufficient frequency content to

stimulate the resonance. Shorter rise times can stimulate higher frequency resonances; longer rise times will not.

Figure 10.19 shows the voltage profile when the entire 8 A transient current is drawn from the three-peak PDN in 1 ns beginning at 10 ns. The rise time is fast enough to stimulate all three impedance peaks. The 44 MHz Bandini Mountain peak creates a droop at about 16 ns. The 2 MHz peak makes its droop at about 180 ns and is a little hard to see because of the leftover ringing from the Bandini peak. The 130 kHz peak makes its droop at about 2  $\mu$ s. We plotted the waveform on an unusual log time scale to see the effect of each of the three impedance peaks on the same plot. We demonstrate the rise times that stimulate each individual peak by using custom rise times on three different time scales.

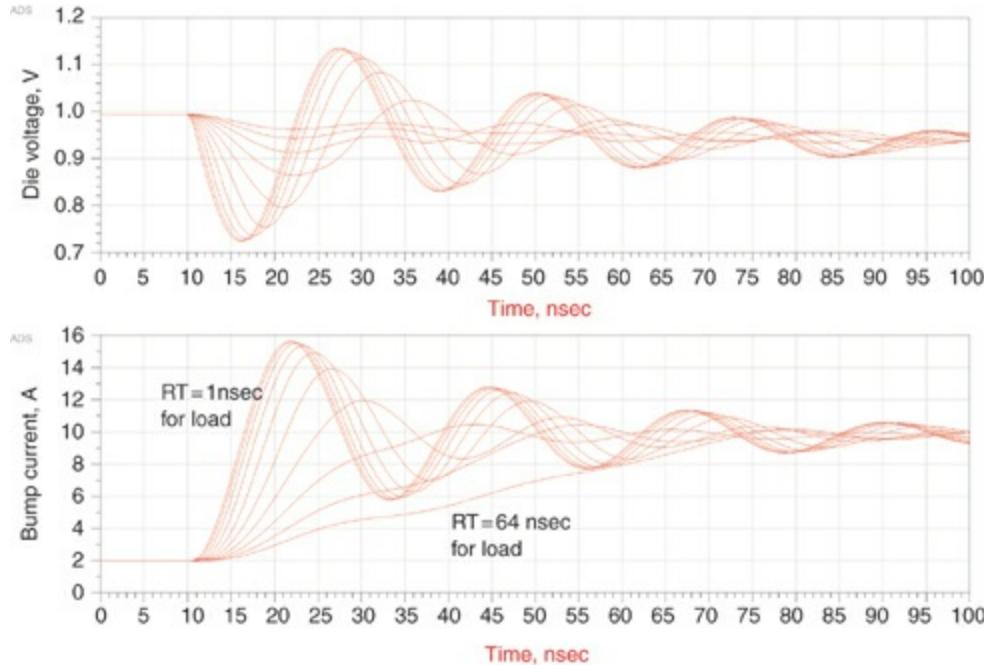


**Figure 10.19** Time domain waveform of the three-peak PDN stimulated with a 1 ns rise time current step plotted on a log time scale. The droop from the Bandini high-frequency peak is at 16 ns, the droop from the second highest frequency peak is at 180 ns, and the droop from the third peak is at 2  $\mu$ s.

First, we choose the rise time of an ideal current step edge to increase from 1 ns to 63 ns and use it to stimulate the three-peak PDN. The Bandini Mountain for this PDN is at 44.1 MHz. This is the highest frequency peak and is said to be the first peak. The droop associated with the first peak is known as the first droop.

Using the bandwidth estimate of equation 10.43, we expect stimulation of the impedance peak to drop off

when the bandwidth of the signal drops below the peak frequency, or the rise time is longer than  $0.35/0.0441$  GHz = 7.9 ns. **Figure 10.20** shows the simulation results. The top panel shows the die voltage and the bottom panel shows the bump current, which is a filtered version of the load current.



**Figure 10.20** Impact on the simulated PDN voltage when we change the rise time of the ideal transient step current, and the bandwidth of the current response drops below the peak frequency. This example used an ideal constant current source with different rise times. **Top:** The stimulated voltage on the die pads for different rise time current edges. Longer rise times do not stimulate the high-frequency impedance peak. **Bottom:** The step current response through the package.

The frequency content of the increasing rise time diminishes gradually so there is no sharp transition. The slowest five rise times are longer than 8.4 ns and the fastest five rise times are shorter than 7.9 ns. By observation in the figure, this is about the break point where the rise times no longer stimulate the Bandini Mountain. There is a gradual transition between rise times that do stimulate the resonance and those that do not. For the fastest rise time, the deepest part of the

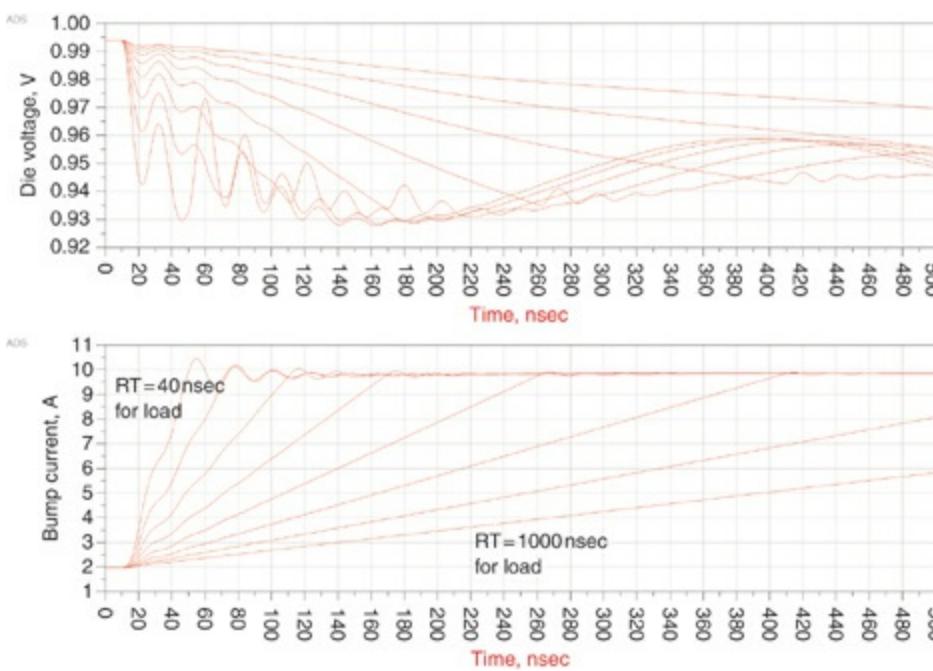
droop seems to come about 8.4 ns after the beginning of the current transient, so it makes sense that rise times longer than 8.4 ns have a diminished effect on the impedance peak.

**Tip**

Droop reduction with increasing rise time is an important observation. If we can increase the rise time of the current load beyond the point where it can stimulate the important impedance peak, we can much improve the PDN voltage droop performance.

Some digital applications have pipelines that take a pre-determined amount of time to fill up and a pre-determined amount of time to empty out. If the rise and fall times for the current drawn from the PDN can be guaranteed to be longer than a certain threshold, the impedance peak will not be stimulated because there is insufficient frequency content to do so.

We performed the same analysis on the second peak of the three-peak PDN. The droop associated with the second peak is known as the second droop. For this PDN, the second peak comes at 1.98 MHz. Using the frequency content estimate from [equation 10.43](#), we expect the second droop to be stimulated by rise times shorter than  $0.35/1.98 \text{ MHz} = 177 \text{ ns}$ . We also expect the second droop to occur at about 177 ns after the transient event. [Figure 10.21](#) shows the simulation with the rise time swept at 40, 63, 100, 158, 251, 398, 631, and 1,000 ns. The shorter rise times still have some frequency content at the 42 MHz of the first peak so they are a little lumpy in the beginning.

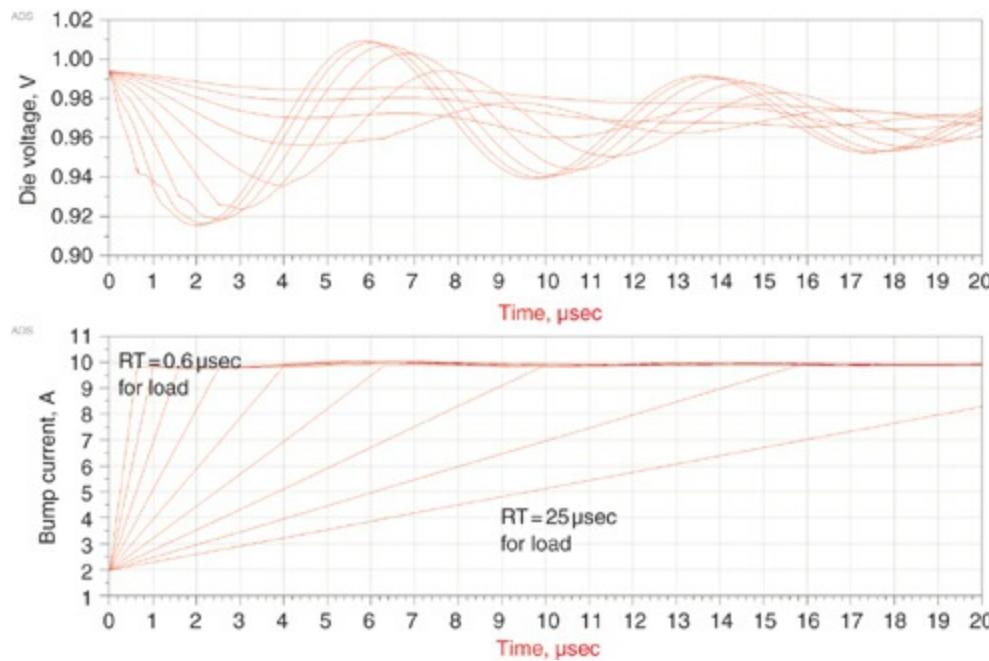


**Figure 10.21** Simulated voltage noise on the die pads when excited with ideal step transient currents with different rise times from 40 ns to 1,000 ns, corresponding to bandwidths that are above the second peak impedance and below. **Top:** Simulated voltage on the die pads. Note, the short rise time current sources are able to excite the first resonant peak, giving the initial ripples. **Bottom:** Transient current load waveforms with different rise times.

From the figure, it is observed that rise times longer than 177 ns have a diminished effect on the second peak and a diminished second droop. These rise times are so long that the filtering of the on-die capacitance and bump-loop inductance have very little effect on the bump currents. The long rise time current waveform in the second panel are almost straight with little high-frequency ripple.

Finally, Figure 10.22 shows the third droop, which is associated with the third peak of the three-peak PDN. The frequency of the third peak is 130 kHz and we expect to stimulate it with rise times shorter than  $0.35/130 \text{ kHz} = 2.69 \mu\text{s}$ . This peak is a little higher and the q-factor is a little bigger than the second peak's. Rise times longer than  $2.69 \mu\text{s}$  show a diminished stimulation of the third peak and diminished third

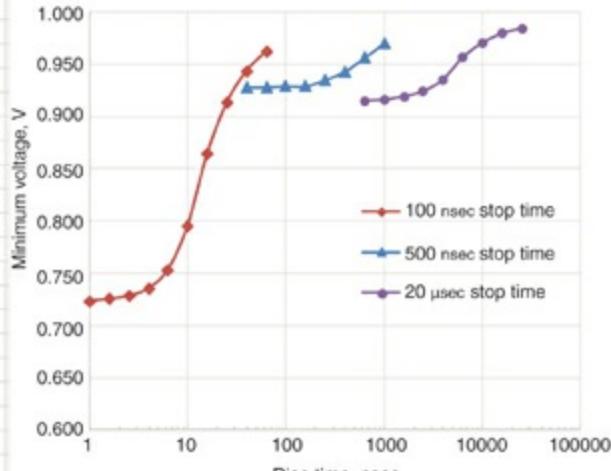
droop.



**Figure 10.22** Simulated voltage noise on the die pads when excited with ideal step transient currents with different rise times from  $0.6 \mu\text{s}$  to  $25 \mu\text{s}$ , corresponding to bandwidths that are above the third peak impedance and below. **Top:** Simulated voltage on the die pads. Note: the short rise time current sources are able to excite the second resonant peak, giving the initial ripples. **Bottom:** Transient current waveforms with different rise times.

**Figure 10.23** summarizes the results of the rise time simulations. The droop voltages are recorded in tabular and graphical format. Clearly, the first droop (from the Bandini Mountain) does the most damage to the PDN voltage if it can possibly be stimulated.

Stop time	Rise time	Droop	Impedance peak	1	2	3	
100ns	1	0.723	Time constant (sqrt(LC))	3.6	80	1,222	nsec
	2	0.725	2 Time constants	7.2	161	2,444	nsec
	3	0.728	5 Time constants	18	402	6,110	nsec
	4	0.735					
	6	0.753					
	10	0.795					
	16	0.864					
	25	0.913					
	40	0.943					
	63	0.962					
1,000ns	40	0.928					
	63	0.928					
	100	0.929					
	158	0.929					
	251	0.935					
	398	0.943					
	631	0.956					
	1,000	0.970					
	631	0.915					
	1,000	0.916					
20,000ns	1,585	0.919					
	2,512	0.924					
	3,981	0.935					
	6,310	0.956					
	10,000	0.970					
	15,849	0.979					
	25,119	0.984					



**Figure 10.23** Summary of the voltage droop values for each peak for different rise times. If the rise time is increased enough, the step current will not stimulate a peak, dramatically reducing the voltage droop on the PDN.

Each resonant peak is created by a parallel combination of an L and a C. We find the period of one cycle of the resonant frequency with

$$T_{\text{cycle}} = 2\pi\sqrt{LC} \quad (10.44)$$

As a rough figure of merit for the response time of an LC circuit, we define the time constant of the resonance as

$$T_{\text{time constant}} = \frac{T_{\text{cycle}}}{2\pi} = \sqrt{LC} = \frac{1}{\omega_{\text{resonance}}} = \frac{1}{2\pi f_{\text{resonance}}} \quad (10.45)$$

If a signal were to have a rise time that was n times the time constant, its bandwidth would be roughly

$$\text{BW} = \frac{0.35}{n \times T_{\text{time constant}}} = \frac{0.35 \times 2\pi}{n \times T_{\text{cycle}}} \approx \frac{2}{n} \times f_{\text{resonance}} \quad (10.46)$$

The deepest voltage droop for a short rise time current step occurs about one-fourth of a cycle into the

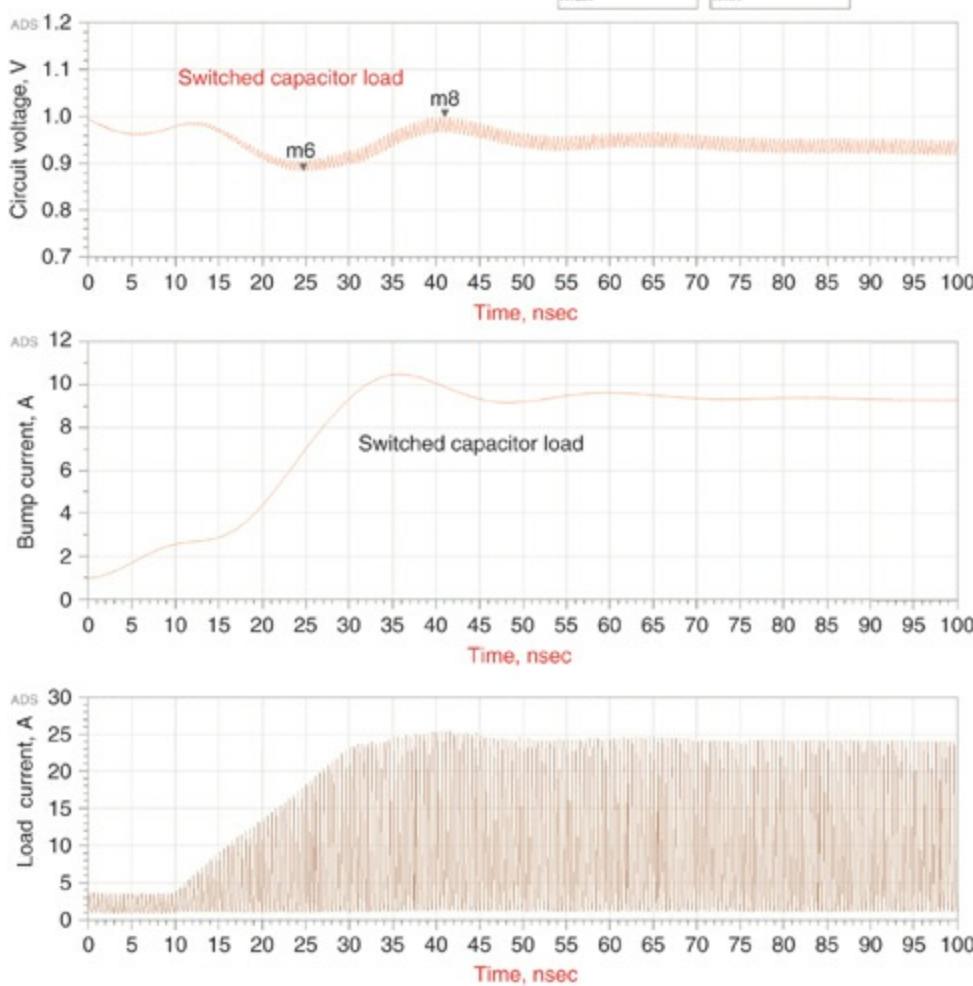
resonance, which is about two time constants after the start of the transient current. As quantified in [equation 10.43](#), the impact from the impedance peak is almost gone when the bandwidth of the current step is significantly lower than the peak resonance. This is roughly when the bandwidth is less than half the peak resonance frequency, or a rise time longer than about five time constants. This is also equivalent to a rise time equal to roughly the period of the resonant frequency.

**Tip**

An important way to mitigate the effects of an impedance peak is to prevent the current rise time to be shorter than five time constants of the resonance. Doing this is easy in concept but difficult in practice because the current rise times are usually dependent on the microcode and product architecture and are not easily changed.

The rise time simulations in this section used an ideal current step source where it was easy to change the rise time. We can easily control the current rise time with the switched capacitor load by modifying the ramp rate as determined in the PWL equations. [Figure 10.24](#) shows a simulation involving the switched capacitor load where the rise time has been limited by the ramp rate to be 20 ns. This is five times the time constant of the first resonance. The first droop has almost completely vanished. The second and third droops expected at about 200 ns and 2000 ns would dominate the voltage response if the simulation were carried out that long.

m8 Time = 41.02 nsec Circuits = 0.999 Max	m6 Time = 24.66 nsec Circuits = 0.885 Min
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**Figure 10.24** The transient step current response when using the switched capacitor load model and a rise time of 20 ns. **Top:** The stimulated voltage on the die pads showing the dramatically reduced first droop. **Middle:** The bump current showing the absence of resonant response. **Bottom:** The switching current from the on-die capacitance.

## 10.15 IMPROVEMENTS FOR A THREE-PEAK PDN: REDUCED LOOP INDUCTANCE OF THE BANDINI MOUNTAIN AND SELECTIVE MLCC CAPACITOR VALUES

The three-peak PDN, as created in the default conditions of the spreadsheet, does not even come close to meeting performance objectives based on the target impedance of  $6.3 \text{ m}\Omega$ . As we see in line 54 of the PRC, the Bandini Mountain impedance peak is 15 times the target impedance. Even its characteristic impedance is 6 times above the target impedance.

As expected from the PRC figure of merit calculations, the step response and resonance response droops greatly exceed the 5% tolerance that was used in the target impedance calculation. Power integrity engineers often encounter this difficult situation. This section offers some suggestions for improvement and management of this dilemma. Several of these improvements carry consequences such as cost increase and performance and power impact. The improvements we discuss include

- Addition of a package capacitor
- Optimizing midfrequency board capacitors
- Extra damping in the VRM model
- Reduction of transient current
- Increase of the transient current rise time (reduction of frequency content)
- When all else fails, raise up the PDN voltage to cover over the voltage droops

For core circuits, we are usually interested in Fmax, the maximum clock frequency where the core runs error free at a given PDN voltage. Any further reduction in PDN voltage will likely cause a set-up time violation leading to a functional failure. IO and communication circuits are often more concerned about jitter than about setup and hold time failures. They are often more sensitive to  $dV/dT$  than to the minimum functional voltage.

The biggest problem is the Bandini Mountain where the die capacitance and package inductance reactances cross. The impedance peak impedance,  $91\text{ m}\Omega$  is way above the target impedance,  $6.3\text{ m}\Omega$  (lines 10 and 56 of PRC). The most obvious solutions are to increase the on-die capacitance or reduce bump-package-circuit board loop inductance to lower the crossing point and

the characteristic impedance.

**Tip**

On-die capacitance requires either more silicon area for thin oxide capacitance or extra mask steps for MIM (metal insulator metal) capacitance. Although both of these solutions are very effective, they are also very expensive. A high cost is associated with increasing the ODC.

Line 19 of the PRC indicates that we already have 100 nF of on-die capacitance. The evaluation of clock-edge noise on lines 13–17 indicates that the switch factor is 4.5%, which is very reasonable. The expected clock-edge droop in line 58 is 45 mV and not excessive. The major problem here is that the clock frequency has gotten pretty fast at 2 GHz and leads to high power density. This is common as we move to more advanced technology nodes and makes a strong case for investing in MIM capacitance. For some products in some markets this is acceptable but for others it is not. The other choice is to work on the inductance side.

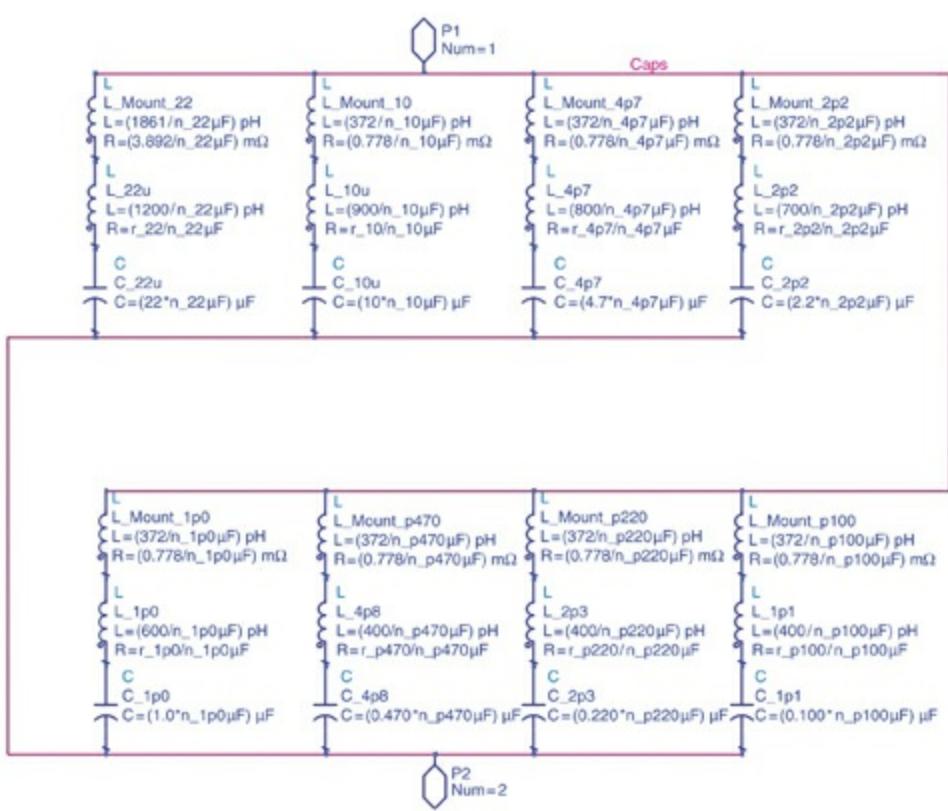
In the default design, the bump-loop inductance involves the package, balls, PCB vias, power planes, and mounted board caps. The extraction and resonance calculation page of the PDN resonance calculator gives good insight into the inductance contributors. Out of the 132 pH loop inductance on line 47, 84 pH of it is coming from the mounted capacitors. The remainder includes 29 pH in the package and 19 pH in the board BGA vias. Clearly the mounted capacitors dominate. Doubling the number of high-frequency capacitors from 10 to 20 brings the 84 pH down to 45 pH. Doubling the number again brings the inductance of the mounted capacitors down to 23 pH. At this point we have reached the point of diminishing returns because the 23 pH is less than half of the 48 pH for the package and board BGA vias.

We have increased the number of board high-frequency capacitors from 10 to 20 and then to 40. To double the board caps again would bring us to 80 capacitors but only give a reduction to 12 pH for board caps, which is in series with the 48 pH for the board vias and package. For this design, using more than ~40 board capacitors does not bring a good return on investment and one can argue that even 40 is too many.

**Tip**

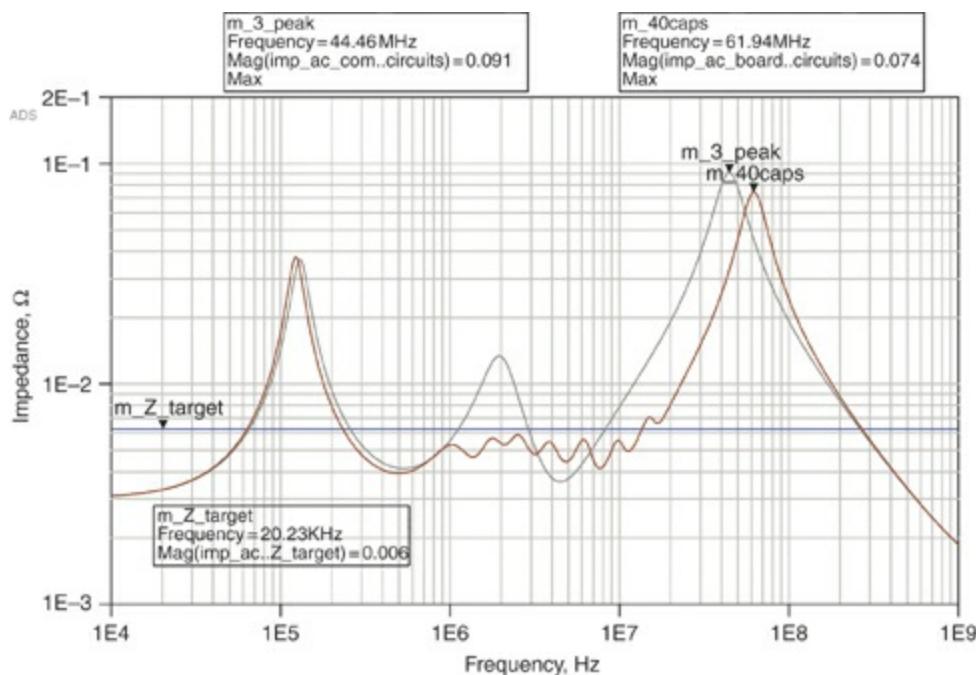
After the equivalent parallel inductance of the board mounted capacitors drops below the remaining series inductance (package, board vias, board planes, and so on), adding more capacitors does not result in a significant reduction in loop inductance. This sets a convenient cost-effective limit for the number of board-level MLCC capacitors to target.

Figure 10.25 shows the simulation schematic for the board caps. Originally for the three-peak PDN, there were  $10 \times 1 \mu\text{F}$  capacitors. Changing to a distribution of capacitor values of  $1 \times 10 \mu\text{F}$ ,  $1 \times 4.7 \mu\text{F}$ ,  $2 \times 2.2 \mu\text{F}$ ,  $4 \times 1 \mu\text{F}$ ,  $6 \times 470 \text{ nF}$ ,  $10 \times 220 \text{ nF}$ , and  $16 \times 100 \text{ nF}$  (40 total caps) marginally improves the PDN. The circuit element parameters for each capacitor branch have a multiplier or divider number so that we can easily tune the number of caps in each branch in the simulation.



**Figure 10.25** Circuit model for an array of capacitors with a distribution of values. Eight different values are selected, each with its own ESR, ESL, and number, ranging in capacitor value: 22  $\mu$ F, 10  $\mu$ F, 4.7  $\mu$ F, 2.2  $\mu$ F, 1.0  $\mu$ F, 470 nF, 220 nF, and 100 nF. The number of capacitors determines the effective mounting inductance, capacitor inductance, ESR, and capacitance.

Figure 10.26 shows the expected improvement when we increase 10 identical board caps to 40 with distributed values. We carefully selected the 40 caps to provide a flat impedance over a broad frequency range, just below the target impedance. This has eliminated the second resonance peak and the second droop discussed earlier.



**Figure 10.26** PDN improvement by adding a distribution of board capacitor values. We increased the original 10 board capacitors to 40 and optimize them to make the impedance as flat as possible. The second resonance peak is gone. The improvement of the Bandini Mountain peak comes primarily from reduced inductance of mounted capacitors. Further increase in the number of capacitors has marginal return because other parts of the board inductance dominate.

Although we eliminated the second impedance peak, the Bandini Mountain impedance peak only dropped from 91 mΩ to 74 mΩ. Most of the improvement was gained by increasing from 10 to 20 well-selected caps. Only a marginal improvement came from the next 20 capacitors. Doubling the number of capacitors again is fruitless because the board vias and package dominate the inductance.

#### Tip

For board designers who have control of the board but no influence on the package or die, this is all that you can do. A limit exists to the impact possible on the Bandini Mountain without influence on the package lead inductance and on-die capacitance. This is because the Bandini Mountain characteristic impedance is so high.

The preceding discussion illustrates one of the primary values of the PRC spreadsheet: It is easy to see the contribution of the several inductive structures. This guides us into the most cost-effective area for improvement by showing the relative importance of each contributor. It also lets us know when we have reached the point of diminishing returns and need to look elsewhere for improvements.

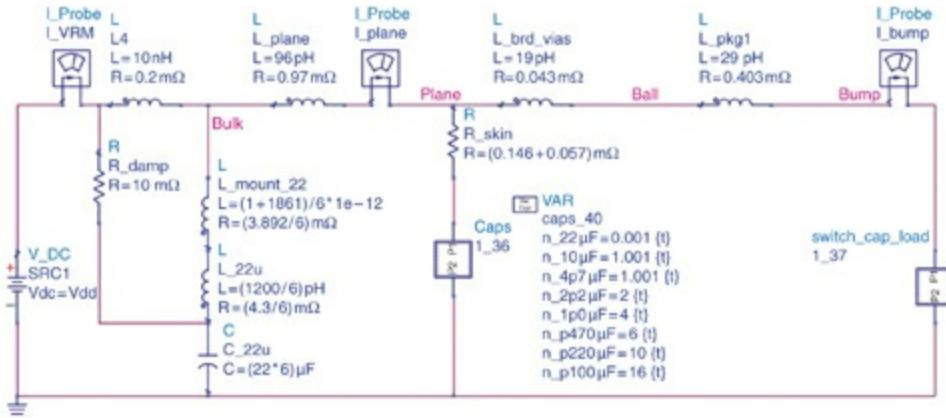
## **10.16 IMPROVEMENTS FOR A THREE-PEAK PDN: A BETTER SMPS MODEL**

Now it is apparent that we have two major peaks, one from the Bandini Mountain and the other from the VRM. The VRM peak may not be real. A typical switch mode power supply (SMPS) has an impedance peak at perhaps 100 kHz but it does not have a high q-factor and is not this tall or sharp as predicted by the impedance curve when properly designed and compensated. This assumes that the feedback loop, control system, and bulk capacitor are well-managed. Accurate SMPS simulation can only be done in the time domain because the circuit topology varies with time and is very nonlinear.

The SMPS response time for a rising current transient is often different from that of a falling current transient. This violates many of the assumptions behind frequency domain analysis. Having said that, we still need some kind of a linear model for the VRM for our frequency domain simulations. We cannot directly connect an ideal voltage source to our board caps. It would be completely unrealistic. On the other hand, the circuit model for the SMPS must be sufficiently simple that it does not consume a lot of simulation time and computer memory to simulate useful time scales.

A good workaround is an appropriate resistor ( $10 \text{ m}\Omega$ )

connected as closely as possible to shunting the bulk capacitance to the ideal voltage source as shown in the schematic of [Figure 10.27](#).  $R_{\text{damp}}$  is added to emulate realistic damping in the SMPS VRM but is not a realistic system resistor. The VRM inductor still controls the impedance at low frequency. The fictitious  $R_{\text{damp}}$  simply puts a limit on the VRM impedance peak.



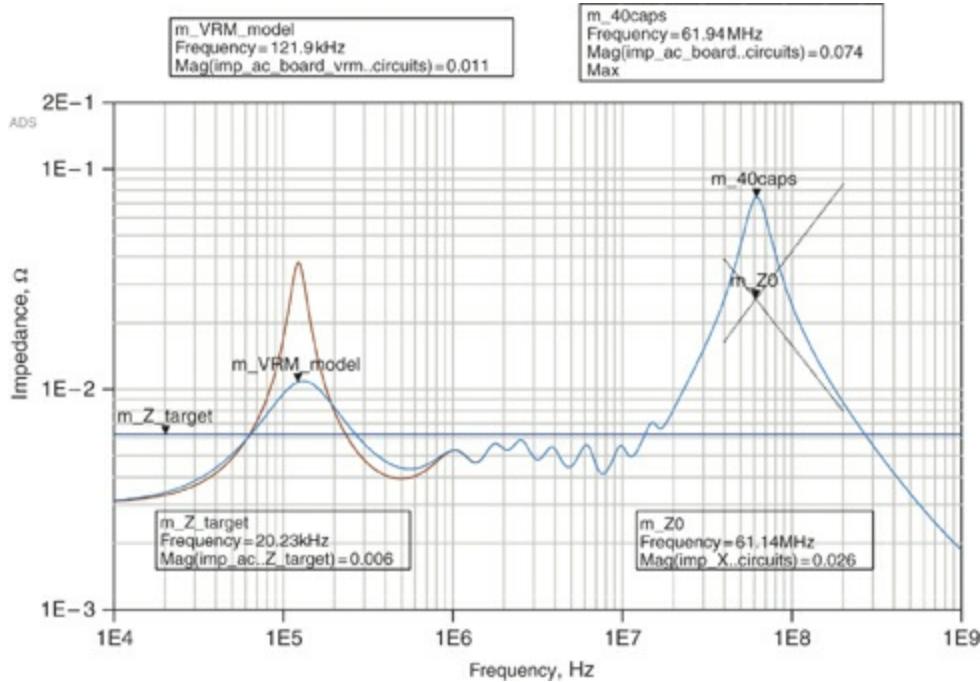
**Figure 10.27** Improved circuit model of the SMPS using  $R_{\text{damp}}$ , an artificial  $10\text{ m}\Omega$  damping resistor. The  $10\text{ nH}$  series inductance is selected to match the transient response of the VRM. Included is the bulk decoupling capacitor. Also shown in the  $\text{caps\_40}$  variable is the number of individual capacitors that make up the 40 board capacitors.

The resistor is sized to give the expected VRM voltage droop at the full transient current. The VRM inductor is sized to give the right time constant for the VRM droop and appropriate DC voltage drop. Once again, this is not an accurate or even physical VRM model but it does allow us to proceed with frequency and time domain simulation and set a PDN voltage with an ideal voltage source at the far side of the VRM inductor. Simulations with this model will not be accurate below the bulk capacitor series resonant frequency or for time domain simulations longer than several microseconds.

[Figure 10.28](#) shows the frequency domain simulation of the improved VRM model along with the 40 board capacitors. The impedance profile below 1 MHz has

changed but above 1 MHz shows little difference. This enables us to continue with PDN simulation in the frequency bands and time windows where power integrity engineers are most concerned without being disrupted by an unrealistic SMPS impedance peak.

The Bandini peak for 40 board capacitors has  $Z_{peak} = 74 \text{ m}\Omega$  and  $Z_0 = 26 \text{ m}\Omega$ . The q-factor is  $74/26=2.85$ .



**Figure 10.28** Simulation of the improved VRM model to capture approximate VRM behavior with a simple model and including the 40 capacitors.

The dominant peak is still the Bandini Mountain and deserves the most attention.

#### Tip

After reducing the MLCC capacitors' loop inductance below the package loop inductance, we can do little to affect the Bandini Mountain at the board level.

## 10.17 IMPROVEMENTS FOR A THREE-PEAK PDN: ON-PACKAGE DECOUPLING (OPD) CAPACITORS

An effective way of reducing the Bandini Mountain is by adding on-package decoupling (OPD) capacitors. These

will effectively reduce the bump-loop inductance that resonates with the on-die capacitance (ODC) and manage q-factors. Three types (locations) of package capacitors have become popular:

- Top side of the package at the same level as the die and die bumps
- Embedded capacitors that are located in the package substrate underneath the die
- Bottom-side capacitors that are located underneath the package where they usually displace several balls

If a package capacitor is to be used, package resources must be consumed to hook it up with a low inductance connection in order to make it effective. After all, the reason it is there is to reduce the loop inductance seen by the bumps when looking out into the rest of the system. The most important property of a package capacitor is its mounted loop inductance.

**Tip**

The loop inductance of the on-package capacitors integrated into the package PDN is the most important property influencing their effectiveness.

The second most important property of the package capacitor is its ESR. This often becomes the dominant loss mechanism for the overall q-factor of the Bandini Mountain.

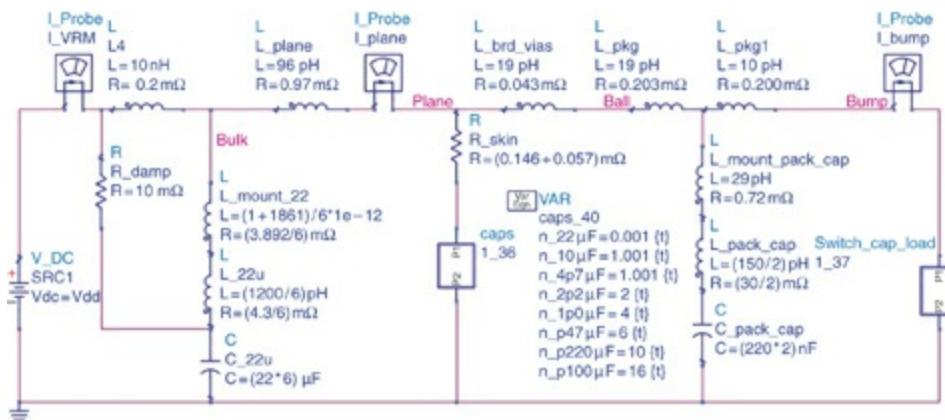
**Tip**

The package capacitor is effective at both reducing the characteristic impedance for the PDN step response through reduced inductance and reducing the q-factor height of the impedance peak for the PDN resonance response by increasing resistive losses.

Interestingly enough, the least important property of

the package capacitor is its capacitance. It generally just needs to be about five times the on-die capacitance to be effective. Above this, further increases in capacitance have little impact because the series combination of the on-package and on-die capacitances is what matters against the impedance peak. However, a larger package capacitance reduces the requirements on the effective board inductance.

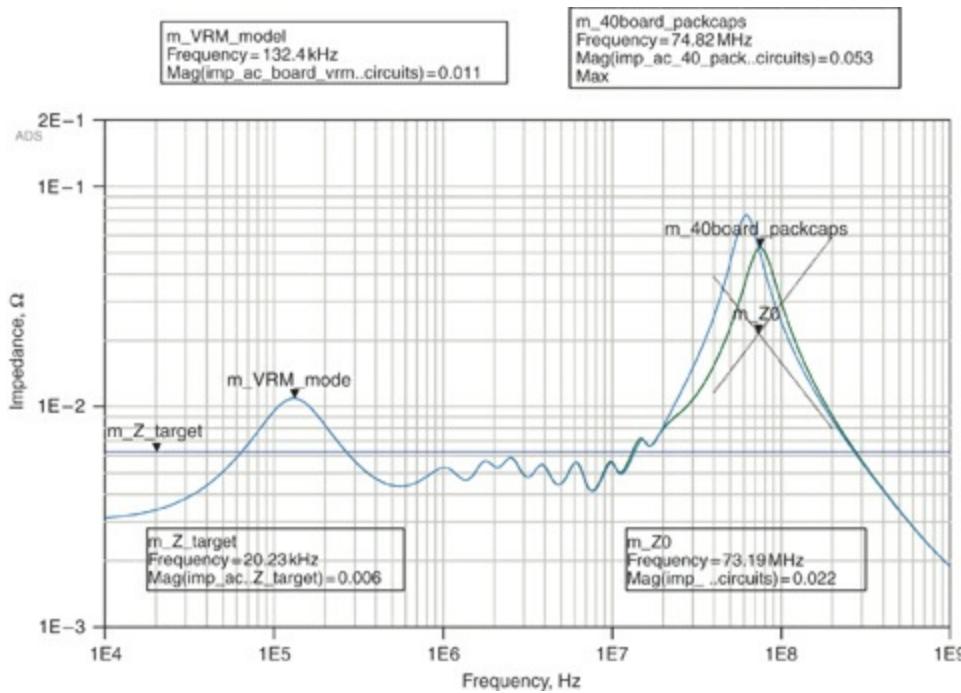
Figure 10.29 shows the schematic of the improved PDN with two 220 nF capacitors added to the package, as an example. At this point, many engineering tradeoffs need to be made concerning the physical size of the capacitors, the ability to fit them in the ball space underneath the package, the ability to embed them within the substrate, the ability to hook them up with a low inductance connection, and the electrical properties of parallel package capacitors.



**Figure 10.29** Improved PDN circuit model that includes the more realistic VRM model, multiple value MLCC capacitors, on-package capacitors, and the switched capacitor load model.

The impact of adding on-package capacitors is to split the Bandini Mountain. Of course, the features of the resulting impedance profile depend strongly on the capacitors selected and how they are integrated into the package. In this example, we assume two 220 nF capacitors with 150 pH of mounting inductance each.

**Figure 10.30** is the resulting impedance profile, compared with not having any on-package capacitors.



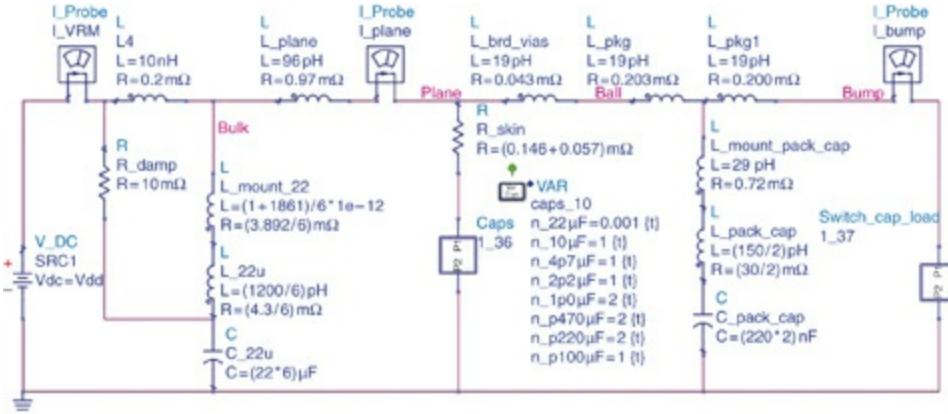
**Figure 10.30** PDN impedance profile with two 220 nF on-package capacitors added. Note the reduction in the Bandini Mountain peak impedance. The ESR of the on-package capacitors also provides more damping.

The Bandini Mountain impedance peak has moved up in frequency from 62 MHz to 75 MHz because of reduced inductance with the package capacitors. The impedance peak has also moved down in height from 74 mΩ to 53 mΩ. This is partially from the reduction of characteristic impedance  $Z_0$  and partially from better damping. The  $Z_0$  for 40 board caps plus package caps is 22 mΩ. The q-factor is  $53/22=2.41$ .

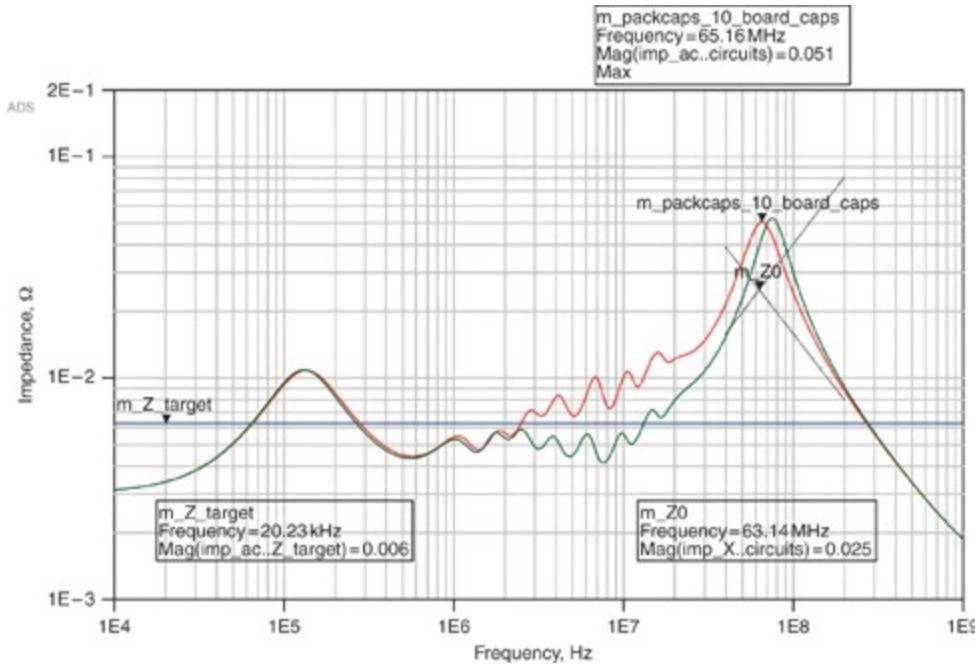
At this point, the PDN has 40 MLCC capacitors. This adds cost to the board. When trying to balance cost and performance, we can sometimes back off slightly on performance for a significant cost reduction. To evaluate this, we explore the impact of reducing the number of MLCC capacitors, now that we included the on-package capacitors.

For example, suppose we reduce the number of MLCC

capacitors from 40 back to 10, but optimized in value, rather than all the same value. Figure 10.31 shows the schematic with 10 board capacitors. Figure 10.32 shows the resulting PDN impedance profile for this case. This is the final improvement we include in the PDN.



**Figure 10.31** Final physical improvements for the three-peak PDN. We've reduced board caps from 40 to 10 optimum values. On-package decoupling capacitors are present as well as VRM model improvement.



**Figure 10.32** The PDN impedance profile with two on-package capacitors, comparing 40 board capacitors with 10 board capacitors with optimized values. The 10 board caps actually give a slightly lower Bandini Mountain impedance peak. This is due to a combination of the increased board inductance forcing more current through the higher ESR of the package and the higher ESR provided by fewer MLCC board-level capacitors in parallel.

The loop inductance is increased leading to a reduction in resonant frequency from 74 to 65 MHz. Interestingly, the impedance peak reduces in height from 53 to 51 mΩ. There are two reasons for this. First, the board inductance is higher, which causes a higher percentage of the load current at resonance to be drawn from the package, cap which has higher ESR. Second, the board ESR is higher because of fewer parallel capacitor ESRs. Both mechanisms increase the damping resistance and loss for the load current. The  $Z_0$  for a Bandini Mountain with 10 board capacitors plus two package capacitors is 25 mΩ and is more than it was with all 40 board caps (22 mΩ). The q-factor with these 10 capacitors is  $51/25=2.04$ .

**Tip**

Interestingly, reducing the q-factor of the Bandini Mountain from 2.41 to 2.04 due to the fewer board capacitors is more important than the increase in bump-loop inductance.

Both bump-loop inductance and damping have increased with fewer board capacitors and the net effect has been to reduce the height of the impedance peak. This result is somewhat unexpected and surprising. It underscores the necessity to manage both inductance (where lower is better) and losses (where higher is better, at least from a resonance standpoint). The only way to sort this out is with a simulation tool and accurate models.

With fewer board capacitors, the midfrequency band between 2 MHz and 65 MHz is somewhat higher impedance. However, the midfrequency peak of ~13 mΩ of the original three-peak PDN has been reduced to nearly 10 mΩ and is close to the target impedance with just 10 optimized board capacitors.

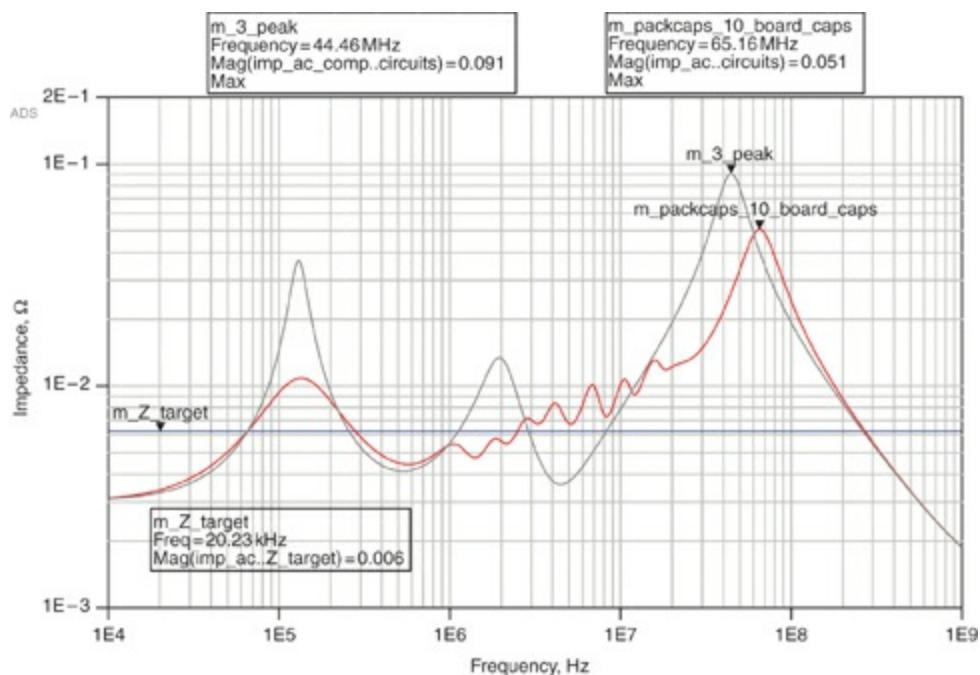
At this point, it is hard to say whether the 40 board capacitors or 10 capacitors are electrically better. It depends on the frequency content of the load. If the 65 or 74 MHz Bandini Mountain impedance peak can be stimulated by resonant load current, then the reduced number of board capacitors with their lower Bandini Mountain peak may actually have slightly better performance, at lower cost.

**Tip**

Fewer board capacitors can sometimes reduce the impedance peak. The q-factor is reduced by the ESR losses in the package capacitors in parallel with the higher ESR associated with fewer board capacitors even though there is more bump-loop inductance.

The step response voltage droop, which is related to the characteristic impedance of the Bandini Mountain, is better with the 40 board capacitors. The resonant response, driven by the height of the impedance peak, is better with 10 board capacitors. At this point, knowledge of the load current is required to determine which solution has better performance, but clearly the board cost, area, and complexity is lower with fewer capacitors.

Figure 10.33 gives the impedance profile of the improved PDN compared to the original three-peak PDN. We used the two package capacitors and 10 optimized board capacitors to bring the impedance peak down from  $91 \text{ m}\Omega$  to  $51 \text{ m}\Omega$  and  $Z_0$  from  $36 \text{ m}\Omega$  to  $25 \text{ m}\Omega$ .



**Figure 10.33** PDN impedance profile comparing the original three-peak impedance profile using the default conditions, and after making improvements in the VRM model, the MLCC capacitors, and the on-package capacitors.

A simple estimate of the q-factor from the two on-package capacitors, each with  $30\text{ m}\Omega$  of ESR, suggests a parallel resistance of  $15\text{ m}\Omega$  and could possibly make an individual q-factor of  $26/15 = 1.7$ , which would be really good for damping. However, the circuit simulation results for Figure 10.32 indicate that the q-factor is 2.04. Unfortunately, the simple estimates break down because the resonant current splits. Some of it goes to the package capacitors and some of it goes to the board capacitors.

#### Tip

As the complexity of the PDN topology increases with additional parallel paths for PDN current, simple estimates and spreadsheet calculations do not capture the subtle effects. We must use a circuit simulator.

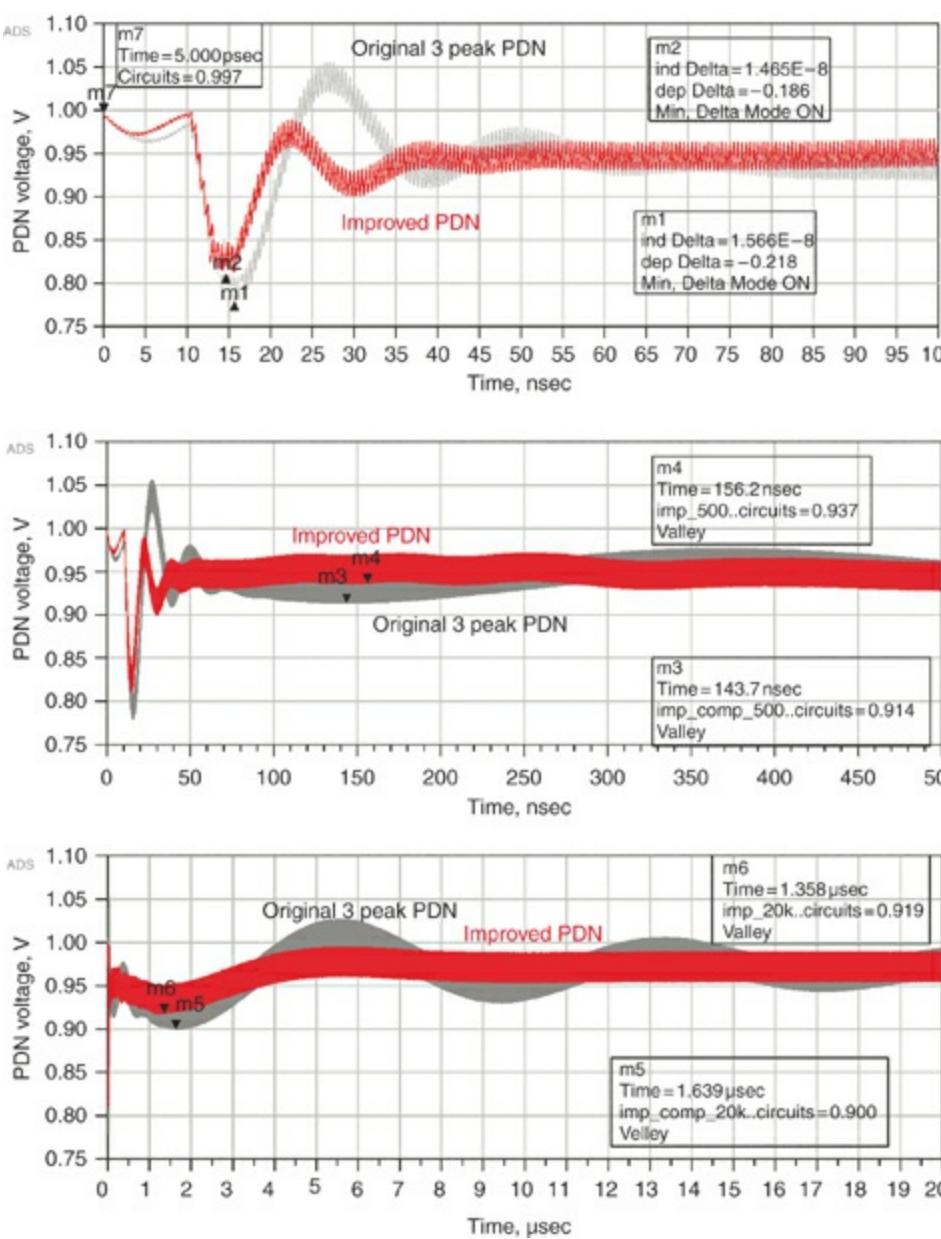
The preceding exercise illustrates the typical process flow for improving a PDN, but it still does not meet performance requirements. Significant improvements to

PDN performance usually come at a cost. Increased capacitance and reduced inductance are the most effective ways to improve a PDN. We might have used more package capacitors to further improve the PDN but fitting them all into the package and hooking them up with an effective low inductance connection becomes a greater challenge with more physical capacitors. The on-die capacitance probably has the most effect on the PDN and we could have increased it. But on-die capacitance directly increases the die area or die layers and is very expensive and is usually not considered, at least on consumer products.

### **10.18 TRANSIENT RESPONSE OF THE PDN: BEFORE AND AFTER IMPROVEMENT**

We evaluate improvements in the PDN first in the frequency domain. Based on the features of the peaks and their characteristic impedance, we estimate the expected step current transient response and resonant frequency transient response. By making the improvements in the peak and characteristic impedances, we expect to see reduced voltage droop and peak voltage noise.

Figure 10.34 shows time domain simulations for the improved PDN compared to the three-peak PDN. We made improvements to all three impedance peaks so we need to show this on three different time scales in the time domain. The top panel shows the improvement in the first dip because of the reduction of first peak, the Bandini Mountain. We reduced the deepest droop, at about 15 ns, from 218 mV to 186 mV.



**Figure 10.34** Time domain step response of the original three-peak PDN compared with the improved PDN. We see package capacitor improvements for the Bandini

Mountain at about 15 ns in the top panel, board capacitor improvements at about 150 ns in the second panel, and VRM model improvements at about 2  $\mu$ s in the bottom panel.

We have chosen the 10 board capacitors that are more effective at increasing the damping and reducing the height of the impedance peak for this simulation. This is one reason why there was not a great improvement in the step response in the top panel. Forty board caps would have reduced the characteristic impedance from  $36 \text{ m}\Omega$  to  $22 \text{ m}\Omega$  and given a marginally bigger improvement for the step response. We settled for  $Z_0$  of

$25\text{ m}\Omega$ . Also, the expected big droop from the three-peak PDN is somewhat mitigated by the switched capacitor load. As the PDN voltage falls, the load draws less current so some self-correction occurs in both the simulation and the physical product. The q-factor reduction is evident in the waveform signature and this shows up as reduced peak-to-peak noise at resonance.

The second panel shows the improvement in the second droop, which occurs at about 150 ns. With the improved PDN, the droop is gone, but clearly the “DC” voltage is reduced from its initial value. We might be tempted to call this DC IR drop, but the current in this frequency band is coming from the board capacitors, not the VRM.

**Tip**

In time scales that sample the mid-band frequency ranges, where the PDN impedance profile is relatively flat, the voltage response to the step transient current looks like a DC offset. This is not due to IR drops but to the step current through this flat impedance profile.

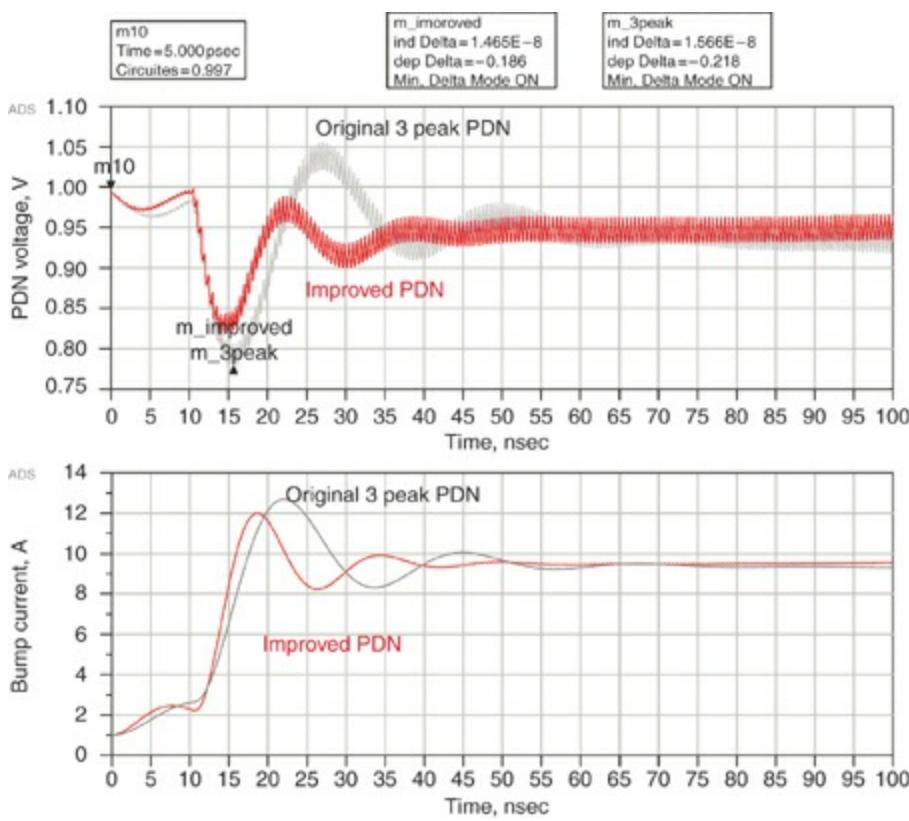
The board capacitor ESR is responsible for this voltage drop that is relatively flat over time. The PDN impedance is relatively flat but does not quite meet the target impedance based on 5% voltage tolerance in the 3 MHz to 30 MHz band. So it is no surprise that the voltage is more than 50 mV (5%) down in the 50 ns to 500 ns time window (middle panel). If we were to achieve a perfectly flat PDN impedance right at the target impedance, we should expect the voltage response to a step current to be right at the lower voltage tolerance for a long period of time.

The third panel shows the third droop that comes from the improvement of the VRM model with proper damping. The system is now overdamped at 130 kHz

and so there is no ringing. There is a slight droop at 1.5  $\mu$ s, which is typical time domain performance expected from the VRM. The capacitor ESR and resonances between board capacitors sets the PDN impedance out to several  $\mu$ s where the VRM regulation loop takes over.

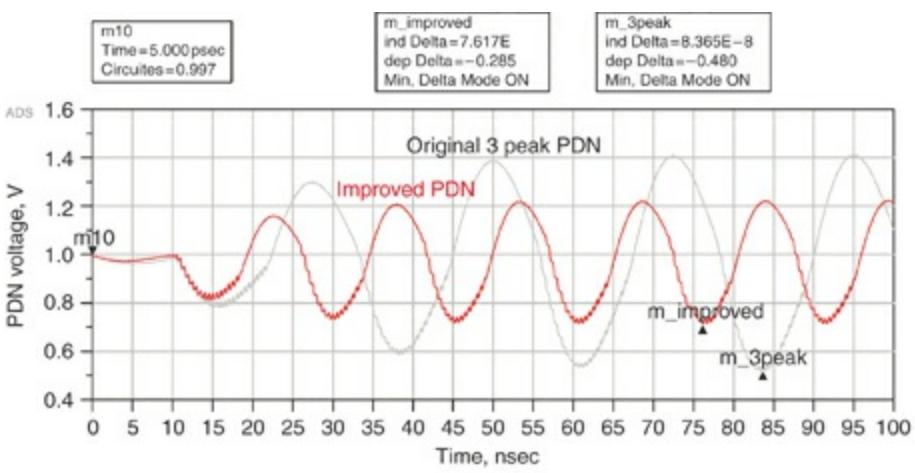
The long term voltage settles in at  $10 \text{ A} \times 3.1 \text{ m}\Omega = 31 \text{ mV}$  down from the initial voltage of 1 V. This is the DC IR drop. The thickness in the voltage trace is primarily due to clock-edge noise. The DC power lost in the PDN is 312 mW as shown in lines 61 and 62 of the PRC.

Figure 10.35 shows the bump current along with the voltage response to step load current. Once again, the bump current is a low-pass filtered version of the load current because of the on-die capacitance and bump-loop inductance. The current ramps up quicker in the improved PDN compared to the three-peak PDN because there is less bump-loop inductance. There is more  $di/dt$  (small signal, slope) because  $V/L$  is bigger. The current profiles also show the higher resonant frequency and increased damping in the improved PDN compared to the original three-peak PDN. The step response droop has improved from 218 mV to 186 mV.



**Figure 10.35** Current step response in the bump branch along with the voltage response for the original three-peak PDN and improved PDN.

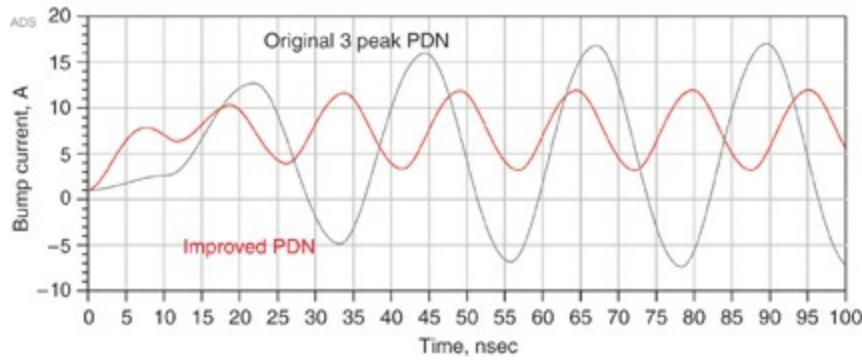
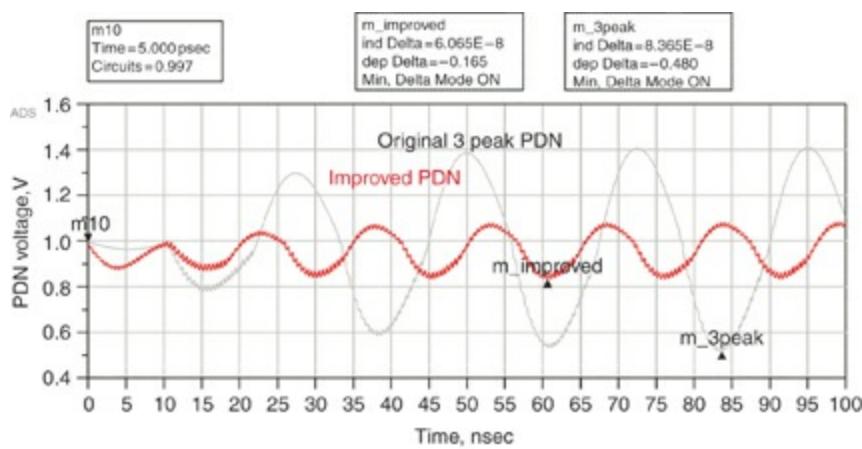
Figure 10.36 shows the resonance response of the improved PDN compared to the three-peak PDN. The initial droop is the same as the step response. As time goes on and the PDN responses from the load current cycles superimpose upon each other, the peak-to-peak voltage builds up. The biggest droop in the improved PDN is 285 mV compared to 480 mV in the original three-peak PDN. Although this is a substantial improvement, the droop is still more than five times the voltage tolerance specified for the target impedance. We have done as much as we can with the physical PDN. We now need to look elsewhere if improvements are still required.



**Figure 10.36** Resonance response of improved PDN (package cap, board caps, VRM damping). We use the switched capacitor load to make repetitive 8 A transients.

## 10.19 RE-EXAMINING TRANSIENT CURRENT ASSUMPTIONS

For the PDN analysis so far we have assumed that the biggest transient current ( $I_{\max} - I_{\min}$ ) from changes in dynamic current is as high as 8 A. However, the probability of having these transients repeat over and over at the resonant frequency is often very low. From knowledge of the load, a power integrity engineer might argue that the maximum repeating transient current at the resonant frequency is only half of the transient current. In this case, we might argue that the PDN should be designed to tolerate repeating transients between 5 A and 9 A. The transient current would be reduced from 8 A to 4 A if we can make this assumption. We simulated the reduced transient current case; Figure 10.37 shows the results. We reduced the maximum droop to 165 mV.



**Figure 10.37** PDN performance improves when we reduce the repetitive transient current from 8 A to 4 A (between 5 A and 9 A). This moves the target impedance up to 12.6 mΩ in the resonance band.

It is highly likely that the transient current will be a function of frequency. It generally takes a fair amount of time to go from the minimum dynamic current to the maximum dynamic current and back again. Repeating this at a very high frequency is difficult. We intuitively expect less transient current repetitions at higher frequency. The reduced transient current (half) at resonant frequency is a special case of this. Because the transient current is a function of frequency, the target impedance is also a function of frequency. In this case, we have effectively increased the target impedance in the resonance band from 6.3 mΩ to 12.6 mΩ. It may be entirely possible for the load to draw the full transient current in lower frequency bands but not possible to repeat the transients at a higher repetition rate.

**Tip**

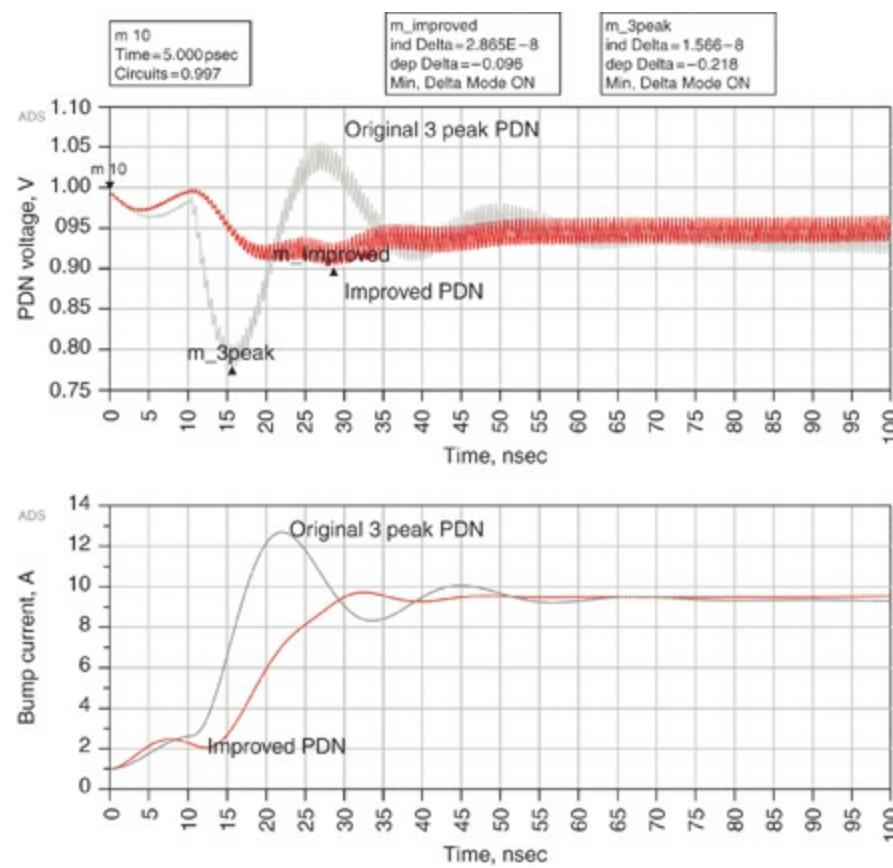
In-depth knowledge of the product and microcode controlling the product is the guide to knowing how to set the target impedance as a function of frequency. Measured data on previous products with similar architecture is a good indication for this. This is where power integrity engineers make cost, performance, and risk tradeoffs.

Having the PDN impedance meet the target impedance at resonant frequency, or even having the characteristic impedance meet the target impedance, is often prohibitively expensive. Now we have to evaluate the transient current versus frequency profile and the level of risk that we are willing to take in raising up the target impedance at higher frequency.

We now return to the step response for a final improvement consideration and ask the question about rise time. As illustrated in [section 10.14](#), if the rise time of the current load is long enough, it will not stimulate a given impedance peak. Some digital products have pipelines that take time to fill and complete. As data enters the pipeline, one latch might release data in the first clock cycle, two latches in the second clock cycle, and in a similar fashion, 20 latches release data in the twentieth clock cycle. This gives a smooth current ramp up and ramp down on both the leading and trailing current edges. Pipelines are a good reason to argue that the transient current is reduced at higher frequencies; therefore, the PDN impedance peak requirements can be relaxed.

[Figure 10.38](#) shows the PDN response to a current step with a 17 ns long ramp. This is more than five times the PDN time constant of the Bandini Mountain impedance peak and does not significantly stimulate this resonant peak. The maximum droop is 96 mV. Having the current slowly ramp up in 17 ns dramatically

reduces the step response.



**Figure 10.38** PDN performance improvement by controlling rise time. Switched capacitor load is ramped up in 17 ns (five time constants of the Bandini Mountain peak). This figure compares the original improved PDN designs with the longer time constant of the step response.

By looking at this waveform, we know that the primary voltage droop contributors are the ESR of capacitors that are delivering current in this frequency band, the clock-edge noise, and some small reactive effects because the voltage profile is not entirely flat near 100 nsec. This represents a vast improvement from where we started. Some product architectures have reliable pipelines and current rise times are expected to be well behaved. However, a risk always exists from unexpected events, recovery from cache misses, and so on. Once again, intimate product knowledge is required to know if current rise times will be well behaved in all cases at all times. In general, long pipelines greatly

diminish the amount of transient current at the resonant frequency.

## **10.20 PRACTICAL LIMITATIONS: RISK, PERFORMANCE, AND COST TRADEOFFS**

We started with a three-peak PDN that did not come even close to meeting the target impedance. We physically improved the PDN by careful selection of board capacitors and the addition of package capacitors. We improved the linear-circuit-element VRM model by adding resistance for damping. We then considered the actual transient current at resonant frequency, the current rise time, and the possibility of shaping the target impedance versus frequency from knowing the load rise-time characteristics.

By these considerations, we reduced the expected PDN voltage droop from an astounding 497 mV (50% of the nominal PDN voltage!) to 96 mV. The droop is still much bigger than our 5%, 50 mV tolerance. This represents a significant risk that functional failures will occur because the PDN exceeded the voltage tolerance. The circuits might not run as fast as required. These risks might be acceptable in consumer product markets but unacceptable in aviation, automotive, medical, and applications where human lives are at stake.

The final solution is not a PDN improvement or even an analysis improvement, but it is often done as a final act of desperation. The VRM voltage might have to be raised up by 50 mV. The dynamic power consumption, which is proportional to the square of the voltage, will go up 10%. The leakage current, which is often proportional to the cube of the voltage, may go up 15%. Thermal profiles are obviously affected. Reliability might be impacted as circuits spend more time at higher voltage.

**Tip**

Raising the VRM voltage has several downsides to the product as well as the power integrity engineer's career. However, sometimes more risk is accepted to meet the performance, cost, and schedule constraints. This is where judgement based on analyzing the performance of similar architecture products is so important.

**Tip**

The more we know about the performance of older, well-characterized products, the farther up the learning curve we start for the next design.

## 10.21 REVERSE ENGINEERING THE PDN FEATURES FROM MEASUREMENTS

In this section, we use the principles introduced in conjunction with the PRC spreadsheet to reverse engineer the PDN properties of an Altera test chip from the measured transient responses. This Altera FPGA test chip data was measured and first presented at the Custom Integrated Circuit Conference and DesignCon conference [3][4]. The authors want to thank and acknowledge Dr. Shishuang Sun for his pioneering efforts with these measurements.

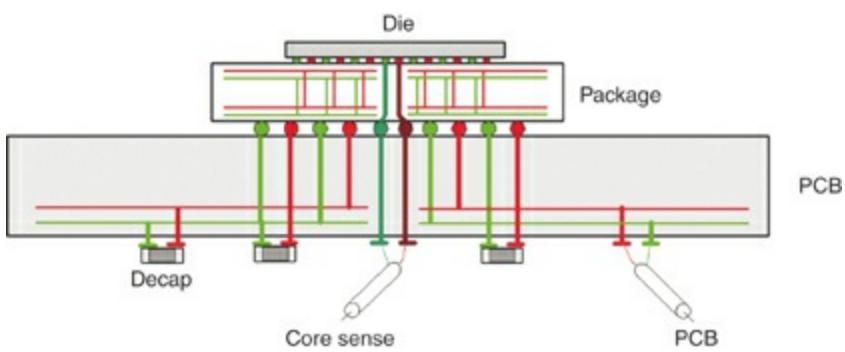
The FPGA was configured to toggle many logic circuits in a way that caused constant current to be drawn during each clock cycle. Although the measured voltages at various nodes were well-documented, the details of the PDN parameters are no longer available. Instead, we use the measured data to reverse engineer the PDN properties that the hardware must have had to generate the measured data. Simulation of the reverse-engineered PDN parameters matches the measured data well.

**Tip**

As shown throughout this book, the PDN impedance, the transient current profiles, and the transient voltage responses measured on the PDN nodes are all interrelated. Knowing any two of them allows us to extract the third. We can use this powerful technique to reverse engineer important features of the PDN.

We can also use the technique to diagnose and establish the root cause when measured PDN waveforms are not behaving as expected based on the design phase analysis.

The measurement fixture involved PDN sense lines into the package, close to the die bumps. The capacitance that is important for the Bandini Mountain impedance peak is on-die. The loop inductance is associated with the die bumps, package planes, vias, and balls, and continues on into the board vias, power planes, and mounted capacitors. The on-die capacitance and the package bump-loop inductance are essentially in parallel with the on-die circuit load. The impulse, step, and resonance responses are generated when the die draws these types of current signatures. This is a typical PDN system with on-die capacitance and package/board inductance and resistance, as depicted in [Figure 10.39](#).



**Figure 10.39** Fixture setup for FPGA PDN

measurements. The capacitance associated with the Bandini Mountain impedance peak is on-die. The loop inductance for the power path involves die bumps, package planes, vias and balls, board vias, planes, and mounted capacitors. The PDN voltage was sensed using nominally  $50\ \Omega$  impedance paths that did not carry PDN current.

Ensuring that the PDN voltage sense lines do not touch the structures that carry PDN current until very close to the die is very important. This is a form of four-point “Kelvin probing” discussed in [Chapter 3](#). The microcode and the functional blocks on the die force the current through the PDN. Non-current carrying structures go all the way to the die to measure and sense the voltage. Very little of the PDN current travels in the voltage sense loop because of the relatively high  $50\ \Omega$  termination at the scope. In this case, the Vdd and Vss sense structures were centered inside a checkerboard pattern of balls, vias, and bumps that brought current in and out of the core load. The package and board via sense structures were equally referenced to Vdd and Vss structures.

At some point in the measurement setup, Vss must be subtracted from Vdd. If the Vdd and Vss sense structures were measured with respect to board ground, Vdd would initially sag down and Vss would initially peak up as the power supply voltage on-die collapses. This happens because the sense structures are referenced to both Vdd and Vss structures.

If both Vdd and Vss sense structures were referenced to Vss, only the Vdd sense line would show noise. Conversely, if both sense structures were referenced only to Vdd, only the Vss sense line would show noise. This is a good physical example of the non-uniqueness of voltages and inductance matrices. [5] The PDN system behaves the way it does because of loop inductance. The partial inductances of PDN Vdd and Vss structures are not unique any more than the Vdd sense and Vss sense voltages are unique.

All PDN measurements of this nature must involve Vdd and Vss sense structures that are differential in nature and equally influenced by whatever return path or reference structures that happen to be nearby. Only the loop inductance is unique and only the difference of  $V_{DD} - V_{SS}$  is unique.

The most straightforward way to measure  $V_{DD} - V_{SS}$  is by subtraction on the instrument. Scopes do this well but spectrum analyzers have trouble with it. We can use  $50\ \Omega$  board traces attached to the board sense structures to bring the Vdd and Vss traces to measurement pads on the board at some convenient location several inches from the DUT. We can use SMA connectors to connect the board trace to  $50\ \Omega$  cables that go directly to an oscilloscope. We must take care to terminate the  $50\ \Omega$  cables with  $50\ \Omega$  termination at the scope to prevent transmission line ringing. All waveforms from the DUT are absorbed by the scope termination and there are no reflections back to the DUT. We can use the scope to subtract Vss sense from Vdd sense to give a proper representation of  $V_{DD} - V_{SS}$  at the die.

A severe impedance mismatch exists at the DUT with the PDN being a few  $m\Omega$  compared to the  $50\ \Omega$  measurement environment. This is good because the measurement structure is  $\sim 1,000$  times higher

impedance than the DUT.

Using high-impedance probes is unnecessary; in fact, they just get in the way. The measurement system described is impedance matched and well-terminated at the scope. Because the PDN sense structures are referenced equally to both Vdd and Vss structures inside the board and package, we should expect an equal amount of PDN noise on the Vdd and Vss sense lines, but opposite polarity. In this configuration, we use the scope to subtract the Vss sense line from the Vdd sense line to get an accurate representation of the on-die voltage. The cables and board traces must be equal length.

An alternative and often more convenient method to subtract Vss from Vdd is by transmission line subtraction. We connect Vdd to the inner conductor of the coax cable and Vss to the outer conductor. There is no DC problem because both the scope ground and the die end of the Vss sense line are at zero volts. However, an AC voltage waveform is on the Vss sense structure that is the opposite polarity in an unknown magnitude compared to the Vdd sense structure.

The difference voltage between Vdd sense and Vss sense is launched into the  $50 \Omega$  coax and the subtraction of Vss from Vdd is accomplished. We must terminate the  $50 \Omega$  coax at the instrument. The transmission line subtraction method is appropriate for spectrum analyzers as well as scopes. The core sense line shown in the [Figure 10.39](#) is set up for transmission line subtraction. The PCB sense line is with respect to board ground. The sense structures leading into the  $50 \Omega$  coax must be electrically short when we use transmission line subtraction, meaning that they must be a small fraction of the wavelength of the highest frequency of interest.

A major source of error when using a  $50\ \Omega$  measurement environment is probe resistance. The probes form a voltage divider with the  $50\ \Omega$  scope termination. If there are  $2\ \Omega$ s loop resistance in a socket contact or die-level metal, a 4% attenuation error will be measured at the scope because of the resistive voltage divider. It is usually better for the sense lines to contact PDN metal on the package side of the bump rather than use dedicated bumps with significant redistribution layer (RDL) metal resistance on the die.

Table 10.16 shows a summary of the FPGA measured data, which is also shown graphically in Figures 10.42, 10.44, and 10.45.

	FPGA PDN Example	Measured	Inputs	Units
1	Vdd	1.1	1.1	V
2	Leakage current	3	3	A
3	Total current at 266 MHz	11	11	A
4	Total current at 533 MHz	19	19	A
5	$f_{clock}$	533	533	MHz
6	Clock-edge noise (impulse response)	105	105	mV
7	Resonant frequency	33	33	MHz
8	100 nsec droop on board, fclk=266 MHz	30	30	mV

**Table 10.16** Summary of the important features measured on the Altera test chip.

The bench power supply voltage and the bench current are measured under three clock conditions:

- The leakage current is 3 A with no clock (line 2)
- The total DC current is 11 A with a 266 MHz clock (line 3)
- The total DC current is 19 A with a 533 MHz clock (line 4)

Normally, the clock would be at 533 MHz so we know that the dynamic current impulse will have completed in less than 2 ns. Line 6 shows the clock-edge noise of 105 mV. It is measured when the clock is slowed way down

to perhaps 10 MHz. The impulse response from a single clock edge is used to estimate the Bandini Mountain resonant frequency at 33 MHz as shown on line 7. Time periods between the damped sinusoid patterns establish the resonant frequency.

Finally, line 8 shows the voltage droop of 30 mV measured 100 ns after a current step. This is almost everything we need to figure out the PDN properties and develop simulated waveforms to compare with measured waveforms.

From the preceding measured data, we calculate the primary PDN properties as summarized in Table 10.17.

	FPGA PDN Example	Calculations	Units
9	Dynamic current at 266 MHz	8	A
10	Dynamic current at 533 MHz	16	A
11	Charge per clock cycle ( $q_{cycle}$ )	30	nC
12	Capacitance that switched	27	nF
13	Capacitance that did not switch	286	nF
14	On-die capacitance	313	nF
15	Switch factor	9%	
16	PDN loop inductance	74	pH
17	PDN $Z_0$	15.4	mΩ
18	Board loop resistance	3.75	mΩ
19	Ball/socket resistance		mΩ
20	Bump-loop resistance	4.35	mΩ

**Table 10.17** Summary of the extracted values of PDN based on the measured transient current features.

After subtracting out the leakage current, the dynamic current is 8 A and 16 A at 266 MHz and 533 MHz, respectively. We use the 533 MHz dynamic current to calculate the charge per clock cycle as

$$q_{cycle} = \frac{I_{dynamic}}{f_{clk}} = \frac{16A}{0.533 \text{ GHz}} = 30 \text{ nC/cycle} \quad (10.47)$$

This is shown on line 11. From the  $q = CV$  equation we calculate the on-die capacitance that must have switched:

$$C_{\text{switched}} = \frac{q_{\text{switched}}}{V_{\text{dd}}} = \frac{30 \text{ nCoul}}{1.1 \text{ V}} = 27 \text{ nF} \quad (10.48)$$

This is identified on line 12. We also calculate the on-die capacitance that did not switch to be

$$C_{\text{ODC\_ns}} = \frac{dq}{dV} = \frac{q_{\text{switched}}}{V_{\text{droop}}} = \frac{30 \text{ nCoul}}{0.105 \text{ V}} = 286 \text{ nF} \quad (10.49)$$

This is included on line 13. The total on-die capacitance is the sum of the switched and non-switched capacitance and is 313 nF as shown on line 14. The switch factor would then be  $27 \text{ nF}/313 \text{ mF} = 9\%$ , as shown on line 15. Using the resonant frequency from an LC circuit and on-die capacitance, we find that the inductance for the first resonant loop is 74 pH on line 16. The characteristic impedance is calculated to be 15.4 mΩ in line 17.

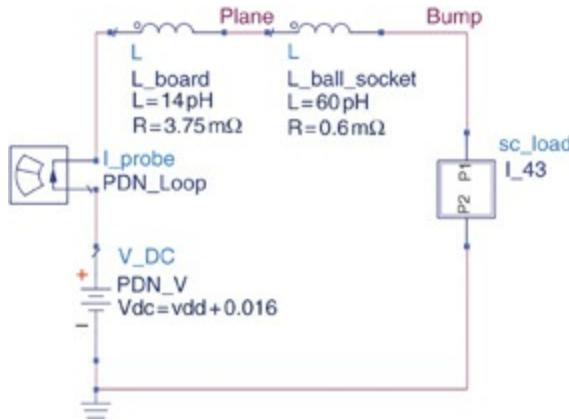
In the FPGA step response measurement, the measured voltage is about 30 mV down ~100 ns after the 8 A current step. This leads to the board resistance calculation on line 18:

$$R_{\text{board}} = \frac{30 \text{ mV}}{8 \text{ A}} = 3.75 \text{ m}\Omega \quad (10.50)$$

This is the board impedance at approximately 3.5 MHz and is mostly due to board decoupling capacitor ESR. There is also some resistance in the package, socket, and board via positions of the PDN. For reasons discussed in the next section on resonance, we chose this to be 0.6 mΩ as shown in line 19. The total bump-loop resistance is 4.35 mΩ.

Lines 9–20 establish the necessary circuit parameters to perform simulation. [Figure 10.40](#) shows the top-level schematic for simulation. We assume the external (off-die) PDN to be just a resistance and inductance. This is sufficient to establish the Bandini Mountain impedance

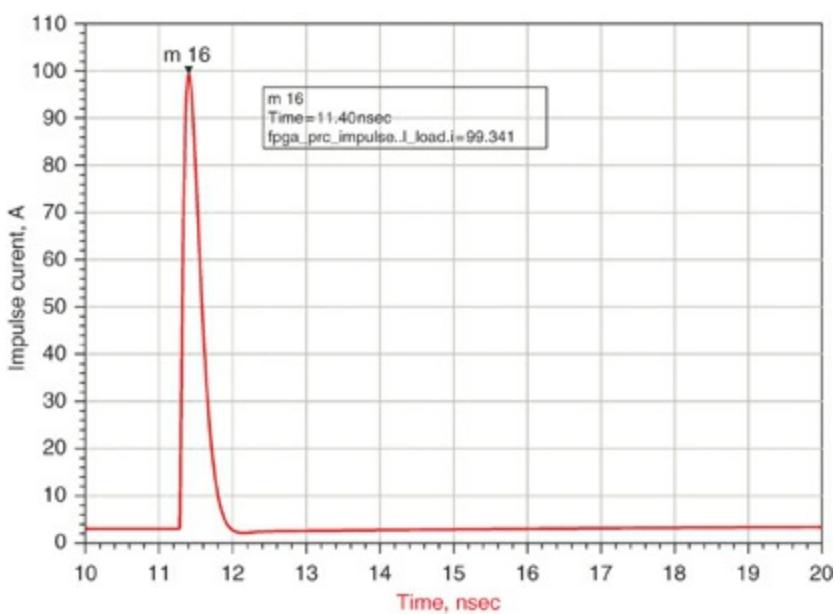
peak including the bump-loop loss for damping. We assume about 80% of the inductance to be in the vertical structures for board vias, socket, package, and so on. We assume most of the resistance to be on the board. Dozens of decoupling capacitors are on the board.



**Figure 10.40** ADS top-level schematic for FPGA model-to-hardware correlation.

The switched capacitor load is similar to what was shown earlier in this chapter. We chose the load capacitance to be 27 nF that draws 30 nC of charge from a 1.1 V PDN each time it is switched. We chose the switch time constant to be 200 ps so that there are almost 10 time constants for the current waveform to decay within the 533 MHz clock period.

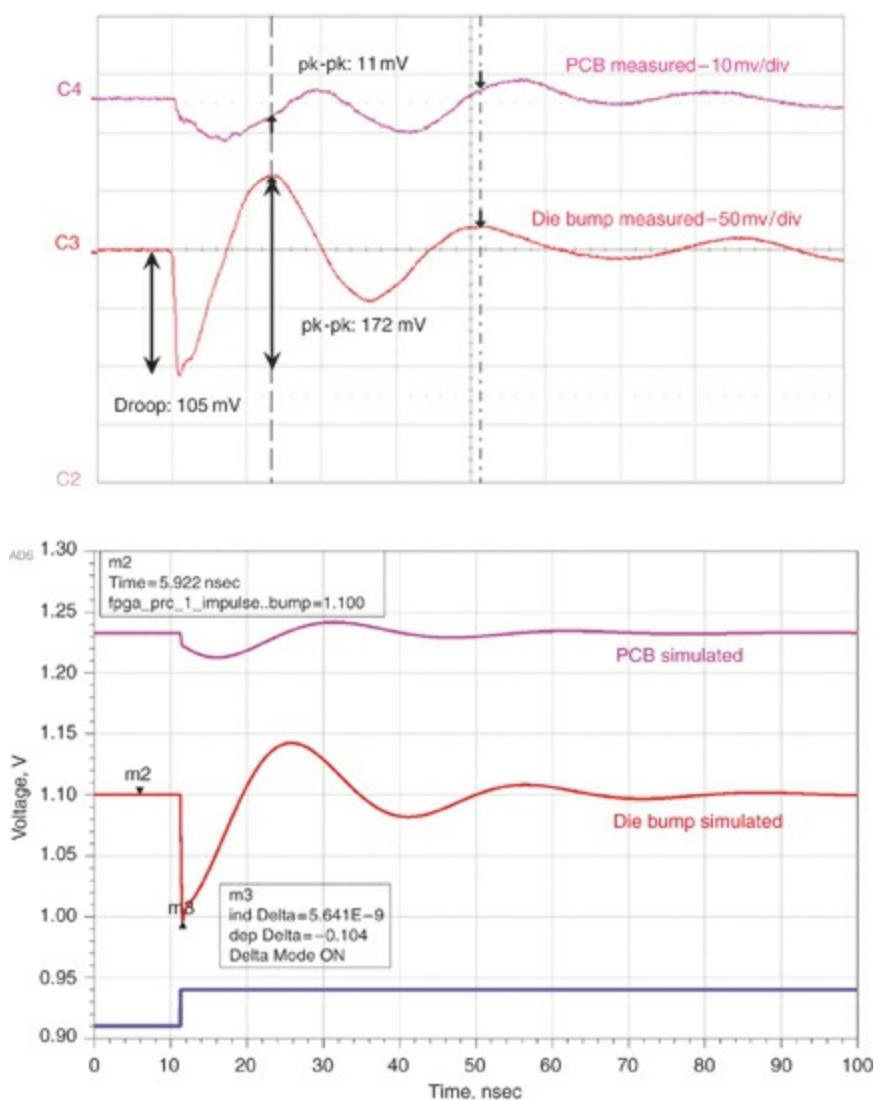
Figure 10.41 shows the current impulse drawn by the switched capacitor load. It reaches a peak of 100 A and has a  $di/dt$  of more than 1,000 A/ns. This is an outrageously fast  $di/dt$  but it is of little consequence because it is delivered from the on-die capacitance. The most important property of this curve is the area under it, which is 30 nC, and causes the impulse response droop. The waveform is riding on top of 3 A of leakage current. The leakage current momentarily drops at about 12 ns because of voltage droop.



**Figure 10.41** The simulated impulse of current drawn by a switched capacitor load. The peak current is 100 A and less than 1 ns wide. The  $di/dt$  is more than 1,000 A/ns but this is of no consequence because it is delivered by the on-die capacitance.

## 10.22 SIMULATION-TO-MEASUREMENT CORRELATION

Figure 10.42 shows the measured data and simulated results for the impulse response. We see the initial impulse response from a single clock edge at 10 ns. The fall time is the width of the 30 nC current impulse and is less than 1 ns. The measured clock-edge droop is 105 mV and the corresponding simulated droop is 104 mV. The assumptions made for the current impulse shape and on-die capacitance ESR make subtle differences in the simulated droop. The chosen 200 ps impulse time constant gives a reasonable tradeoff between clock-edge noise we see in the impulse and step response waveforms. This comparison shows a good match between measured and simulated impulse responses.



**Figure 10.42 Top:** Oscilloscope recording of the measured voltage response on the board and die Vdd rails when one clock edge draws an impulse of transient current. **Bottom:** Simulated board node and on-die node of the PDN response to an impulse of current. Each plot is on the same scale. The agreement is very close.

Before calculating the expected peak impedance, we need to determine the PDN loss at resonant frequency. In Table 10.18, we summarize the contribution from several loss mechanisms: leakage, load, on-die resistance, and bump-loop resistance. The top part of the table shows the resistance for the several loss mechanisms and the bottom part of the table shows the expected q-factors from the individual mechanisms. The calculations for loss mechanisms are similar to those shown previously in this chapter. We calculated the die resistance from the ODC and 250 ps time constant.

	FPGA PDN Example	Calculations	Units
18	Board loop resistance	3.75	mΩ
19	Ball/socket resistance	0.6	mΩ
20	Bump-loop resistance	4.35	mΩ
21	Effective resistance from leakage at Vdd	122	mΩ
22	Load resistance for 16 A resonance	138	mΩ
23	Die resistance	0.80	mΩ
24	q-factor from bump loop	3.54	
25	q-factor from leakage	7.9	
26	q-factor from load	8.9	
27	q-factor from ODR	19.3	
28	Combined q-factor	1.75	

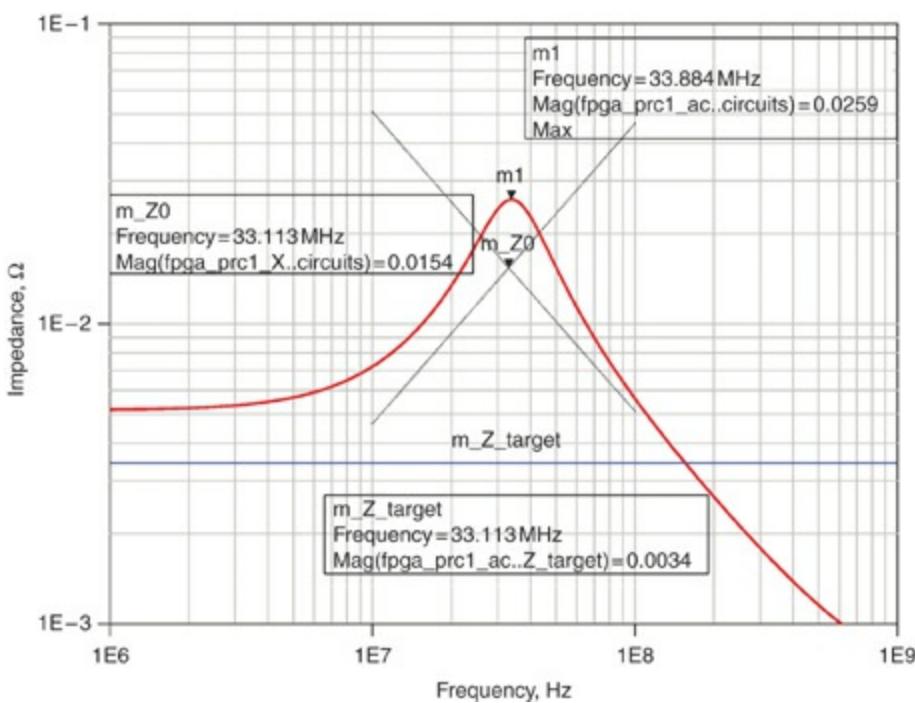
**Table 10.18** Summary of the PDN sources of loss for this measured FPGA example

One thing that stands out in this example compared to the three-peak example is that the q-factor from the bump-loop resistance now dominates. With the previous three-peak PDN, the loss from the load was the dominant damping mechanism. After considering the four individual damping mechanisms, we end up with a combined calculated q-factor of 1.75.

Frequency domain simulation was performed on the assumed PDN topology with the parameters found from time domain measurements. [Figure 10.43](#) shows the results. The frequency peak is 33.88 MHz and 25.9 mΩ. The reactive components were simulated to find the inductive and capacitive reactance at resonance. The two curves cross at the characteristic impedance that is 15.4 mΩ at 33.11 MHz. This is the same as the estimated  $Z_0$  of 15.4 mΩ on line 17. The q-factor from simulation is

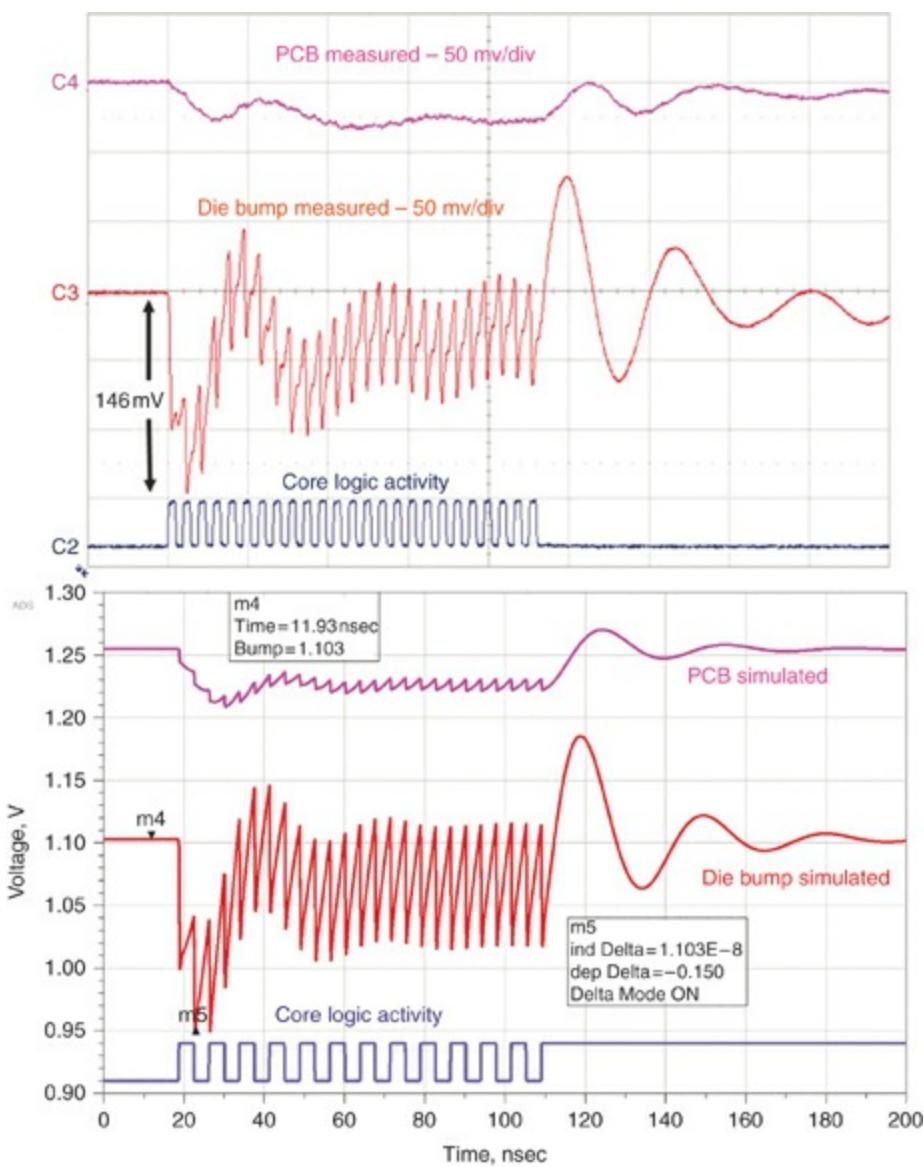
$$\text{q-factor} = \frac{Z_{\text{peak}}}{Z_0} = \frac{25.9}{15.4} = 1.68 \quad (10.51)$$

This is close to the 1.75 predicted on line 28.



**Figure 10.43** Frequency domain simulation results for the FPGA PDN based on measured time domain parameters

So far, the impulse response simulation has matched well with measured data. The frequency domain simulations compare well with the hand calculations in the spreadsheet for resonant frequency, characteristic impedance, q-factor, and impedance peak. Now we move on to the measured step response compared to the simulated step response, as shown in [Figure 10.44](#). The measured data was initiated by 25 cycles of a 266 MHz clock, which generated some core logic activity. The simulated waveforms were initiated by 25 edges of the half clock for the switched capacitor load. This caused 25 current impulses in simulation similar to the 25 current impulses that must have been present in the lab. The measured and simulated PDN noise waveforms are very similar.

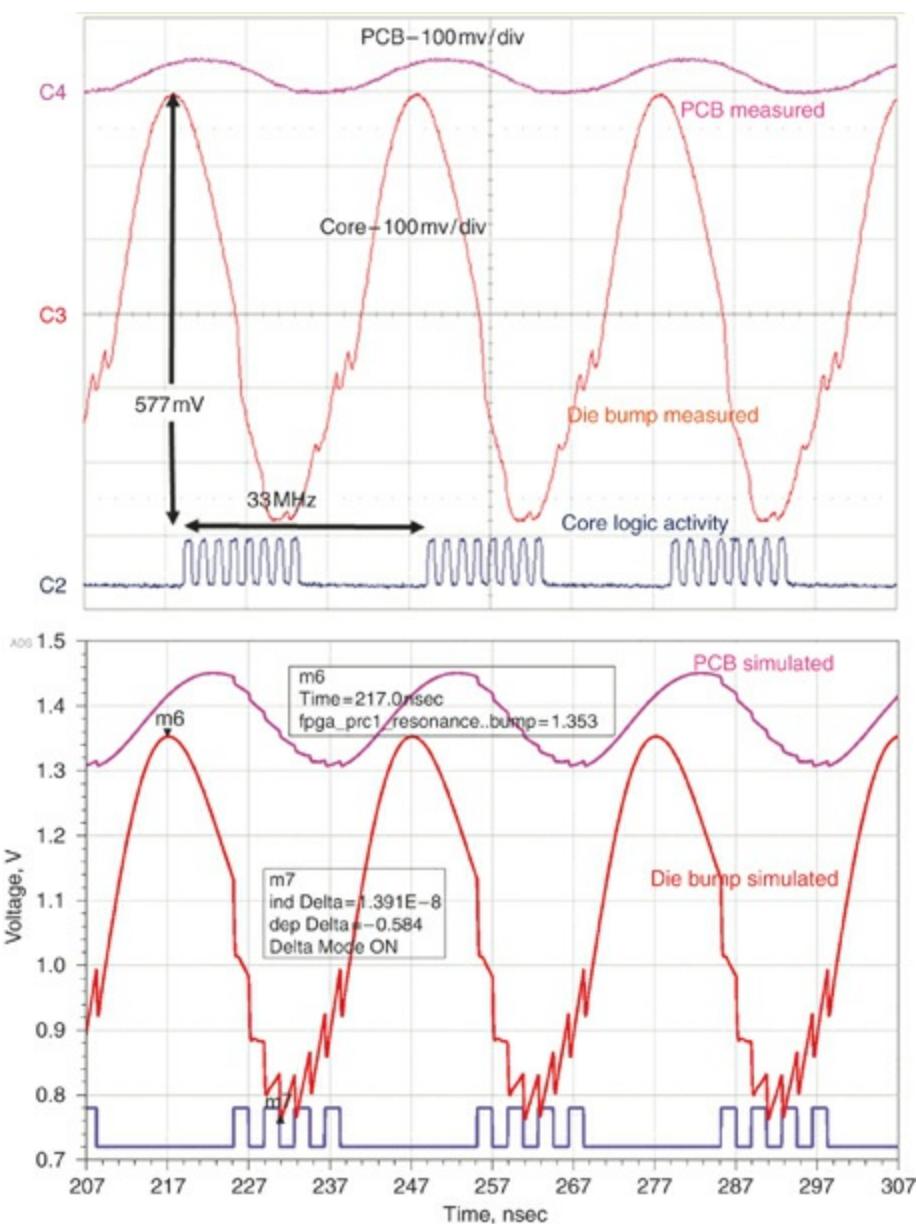


**Figure 10.44 Top:** Measured scope traces for a step transient current. **Bottom:** Simulated step response for the same case.

Clock-edge noise is a major feature for each waveform. The step response droop and signature of the waveforms are similar. The deepest droop from measurement is 146 mV compared to the simulated 150 mV. Clock-edge noise is a little bigger in the simulated data for the step response but is a little smaller in the simulated data for the impulse response. We can increase or decrease the amount of clock-edge noise by manipulating the width of the current impulse. A shorter impulse width makes a deeper droop because of IR drop associated with the ESR of the on-die capacitance. We chose Tau, the switched capacitor

waveform shape parameter, to be 200 ps to obtain reasonable clock-edge noise in both the impulse and step responses. Overall, the measured and simulated step responses match quite well.

Finally, we look at the measured and simulated resonance response, shown in [Figure 10.45](#). The hardware is driven with a 533 MHz clock. The clock waveform is gated (modulated) at the 33 MHz rate to achieve maximum stimulation of the resonant peak. There are eight clock periods with a clock pulse followed by eight clock periods without a clock pulse. This stimulation draws maximum power from the PDN for 15 ns followed by a minimum current for 15 ns. The Bandini Mountain resonance for this PDN is stimulated as much as possible. The measured time domain PDN response is 577 compared to a simulated response of 584 mV p-p.



**Figure 10.45** Measured and simulated resonant stimulation voltages on the board node and the on-die node.

In the development of the simulated resonance response, the initial resonance simulation showed a lot more than 577 mV p-p PDN noise. Because the impulse and step responses match so well, the problem was localized to the q-factor and damping. The p-p resonant voltage should be

$$Z_{\text{peak}} \times \frac{4}{\pi} \times I_{\text{tran}} \quad (10.52)$$

The only explanation is that  $Z_{\text{peak}}$  must have been too high.  $Z_{\text{peak}}$  is the product of the q-factor and the

characteristic impedance. Somehow the loss needed to be greater and the q-factor needed to be lower.

This is often the case with PDN measurements. There is more loss in the system than is accounted for in the initial simulations. In this case, we resolve the situation by adding  $0.6\text{ m}\Omega$  in the ball/socket position of the circuit as shown on line 19 of the spreadsheet. We already had  $3.75\text{ m}\Omega$  for the board as shown on line 18. The additional resistance in the socket position brings the bump-loop resistance up to  $4.35\text{ m}\Omega$ . With this additional damping, the simulated p-p resonant waveform is  $584\text{ mV}$  and closely matches the measured  $577\text{ mV}$  and the spreadsheet calculation of  $588\text{ mV}$ . This is somewhat contrived but is a reasonable way to achieve the losses, q-factor, and impedance peak that the system must have had to produce the measured waveform.

## **10.23 SUMMARY OF THE SIMULATED AND MEASURED PDN IMPEDANCE AND VOLTAGE FEATURES**

In Table 10.19 we summarize the measured data, the inputs, the PDN parameter calculations, and the simulated results. It is a form of the PDN Resonance Calculator. We use the calculated parameters with the assumed simple PDN topology to produce the ADS simulation results.

	FPGA PDN Example	Measured	Inputs	Calculations	Simulated	Units
1	Vdd	1.1	1.1			V
2	Leakage current	3	3			A
3	Total current at 266 MHz	11	11			A
4	Total current at 533 MHz	19	19			A
5	$f_{clock}$	533	533			MHz
6	Clock-edge noise (impulse response)	105	105		104	mV
7	Resonant frequency	33	33		33.11	MHz
8	100 nsec droop on board, $f_{clk}=266\text{MHz}$	30	30			mV
9	Dynamic current at 266 MHz			8		A
10	Dynamic current at 533 MHz			16		A
11	Charge per clock cycle ( $q_{cycle}$ )			30		nC
12	Capacitance that switched			27		nF
13	Capacitance that did not switch			286		nF
14	On-die capacitance			313		nF
15	Switch factor			10%		
16	PDN loop inductance			74		pH
17	PDN $Z_0$			15.4	15.4	$\text{m}\Omega$
18	Board loop resistance			3.75		$\text{m}\Omega$
19	Ball/socket resistance		0.6			$\text{m}\Omega$
20	Bump-loop resistance			4.35		$\text{m}\Omega$
21	Effective resistance from leakage at Vdd			122		$\text{m}\Omega$
22	Load resistance for 16 A resonance			138		$\text{m}\Omega$

23	Die resistance			0.80		$\text{m}\Omega$
24	q-factor from bump loop			3.54	3.05	
25	q-factor from leakage			7.9	7.5	
26	q-factor from load			8.9	8.8	
27	q-factor from ODR			19.3	20.7	
28	Combined q-factor			1.75	1.68	
29	Impedance peak			26.9	25.9	$\text{m}\Omega$
30	$Z_{target}$ for 266 MHz			6.9		$\text{m}\Omega$
31	$Z_{target}$ for 533 MHz			3.4		$\text{m}\Omega$
32	Step response droop	146		123	150	mV
33	Resonance peak-peak noise	577		548	584	mV

**Table 10.19** Summary of all the input terms and extracted terms associated with the Altera test chip, the transient current, and the PDN features.

Lines 30 and 31 show the calculations for the target impedances for 266 MHz and 533 MHz clock speeds and are 6.9 and 3.4 mΩ respectively. The target impedances are far below the characteristic impedance (15.4 mΩ, line 17) and impedance peak (25.9 mΩ, line 29). This might have been expected after observing the large droops associated with the step and resonance responses. The die-package-board PDN is not designed to handle the large currents and transient currents that have been measured in these tests. The FPGA has been pushed well beyond the region where it is normally expected to operate.

The q-factor of 1.68 shown on line 28 is not very high. By most standards, this PDN is well damped. In the initial publication of this data, the simulated q-factor was thought to be 3.9 and the impedance peak was thought to be 63 mΩ. In all likelihood, some of the damping mechanisms (that is, leakage and load loss) were not considered at that time. The calculations and simulated results presented here show that the q-factor and peak impedance were really much smaller.

**Tip**

This exercise drives home the importance of measuring and characterizing PDNs. Real-world systems usually have more loss and damping than initially expected.

This section has demonstrated how to use a few time domain measurements to estimate the parameters for a simple PDN topology. The required measurements were

- The PDN voltage
- The leakage current

- The current at a few clock frequencies
- The impulse response
- The resonant frequency

The impulse response was key because we could measure the clock-edge droop and infer what the on-die capacitance must have been.

We could measure the period of the resonant frequency, which led to an inductance calculation. This was sufficient to get good simulation results for both the impulse and step response.

For the resonance response, we had to put a little more damping into the system than our simple measurements indicated. If the setup were still available, we could have measured the voltage drop from die bumps to board planes to get a more accurate reading on this resistance.

**Tip**

This section has demonstrated a practical process to reverse-engineer an existing PDN to find many of its primary parameters.

## 10.24 THE BOTTOM LINE

1. PDN design is really about managing the peaks in the impedance profile.
2. Every peak has just three terms that characterize it: the resonant frequency, the characteristic impedance, and the q-factor.
3. Three important PDN current waveforms tell us everything the power integrity engineer needs to know about the voltage response of a PDN: the clock edge impulse response, the transient current step response, and the resonant square wave of current response. If you know these voltage responses, you have a good picture of the expected

PDN performance.

4. We described all of these important features, to first order, in a spreadsheet for easy exploration of design space. It is a convenient starting place in PDN design. The most important benefit is to quickly point out the dominant design features that affect the peak impedance features and to estimate the expected PDN performance.
5. Simple analytical approximations in the spreadsheet enable remarkably close agreement to the voltage features simulated in a circuit simulation, confirming a spreadsheet as a great way to start the analysis process.
6. Select capacitors on-board to “do no harm.” Add enough low inductance capacitors so as to make the mounted cap inductance a small part of the Bandini Mountain loop inductance.
7. Optimize capacitor values to add some damping to the Bandini Mountain.
8. Adding on-package decoupling (OPD) capacitors can be a very cost-effective way of reducing the peak impedance of the Bandini Mountain.
9. Although an impedance peak can never be lower than its characteristic impedance, approaching this value is possible by increasing damping. A large contributor to the Bandini Mountain damping is often the load current.
10. When we apply the PDN Resonant Calculator model to a real FPGA system, the agreement between measured voltage waveforms on the die pads is remarkably close to the simulated predictions. This approach to PDN design and analysis really does work.

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# Index

## NUMBERS

- 0th droop. *See* clock edge current
- 1-inch diameter copper loop, measuring impedance of,  
102–105
- 1<sup>st</sup> droop, 661
- 2<sup>nd</sup> droop, 661
- 3D field solver
  - 0th droop, 195–202
  - extracting spreading inductance from, 304–306
- 4-point Kelvin resistance measurement technique,  
93–95
- 182 nF ideal capacitor, 27–29
- 0603 multilayer ceramic chip (MLCC) capacitor, 27

## A

- A<sub>conductor</sub>, 343, 370
- A<sub>dielectric</sub>, 344, 370
- abAmps, 146
- abHenrys, 146
- AC steady state responses, 589–595
- AC tolerance, 660
- ADCs (analog-to-digital converters), 5
- ADS (Advanced Design System), 22, 84–85
- Agilent Technologies, 22
- Ampere's Law, 168
- analog-to-digital converters (ADCs), 5
- approximations, inductance
  - parallel plate approximation for loop inductance, 183
  - round loop inductance, 179–182
  - uniform transmission line inductance, 188–193

artifacts in impedance measurements, [105–109](#)

measured inductance of a via, [109–114](#)

small MLCC capacitor on board, [114–119](#)

$A_{\text{total}}$ , [343](#)

attenuation, modal resonance and, [343–347](#)

## B

B (magnetic field density), [155–159](#)

back emf (electromotive force), [149](#)

ball grid array (BGA), [240](#)

Bandini Fertilizer Company, [448](#)

Bandini Mountain

characteristic impedance, [456–457](#)

frequency, [452–456](#)

intrinsic damping, [456–460](#)

overview of, [447–452](#)

peak impedance, [451–452](#), [494](#)

reduced loop inductance, [718–722](#)

BGA (ball grid array), [240](#)

boundary conditions, [337–338](#)

building PDN (power delivery network) ecology,  
[488–492](#)

bulk capacitance, [225–229](#)

minimum amount of capacitance required, [478–483](#)

optimizing, [483–487](#)

## C

capacitance. *See also* capacitors

bulk capacitance, [225–229](#)

minimum amount of capacitance required, [476–478](#)

optimizing, [483–487](#)

capacitance referenced to both Vss and Vdd rails,  
[558–562](#)

definition of, [138](#)

density, [435](#)

fringe field capacitance

    overview of, [279–285](#)

    in power puddles, [285–289](#)

gate, [430](#)

MLCC (multilayer ceramic chip) capacitors, [220–222](#)

ODC (on-die decoupling capacitance)

    clock edge noise, [431](#)

    ESR (equivalent series resistance), [436–439](#)

    estimating, [431–435](#)

    historic trends in, [435–436](#)

    measuring, [434–435](#)

    relaxation time, [438](#)

    sources of, [430](#)

on-die capacitance

    large on-die capacitance with small package lead

    inductance, [521–527](#)

    measuring impedance of, [120–134](#)

    overview of, [138–140](#)

    parallel plate capacitance, [278–279](#)

capacitor mounting inductance, [401–403](#)

capacitors. *See also* [capacitance](#); [impedance](#); [MLCC](#)

(multilayer ceramic chip) capacitors

bulk capacitors

    minimum amount of capacitance required, [476–478](#)

    optimizing, [483–487](#)

capacitor mounting inductance, [401–403](#)

capacitor/cavity interaction, [325–327](#)

classes of, [222](#)

controlled ESR capacitors, [527–532](#)

damping to suppress parallel resonant peaks,

DC blocking capacitors

number required to suppress cavity resonance,  
387–393

number to carry return current, 393–401  
overview of, 383–386

ESL (equivalent series inductance), 207

ESR (equivalent series resistance), 207, 229–234

FDTIM (Frequency Domain Target Impedance Method)

selecting capacitor values with, 516–521

selecting number of capacitors with, 514–516

location, spreading inductance and, 327–332

lossy transmission line models, 260, 269–272

OPD (on-package decoupling capacitors), 532–539,  
724–731

real versus ideal, 26–30, 206

reverse aspect ratio capacitors, 246

SCL (Switched Capacitor Load)

impulses from, 613–622

PRC (PDN Resonance Calculator) spreadsheet,  
694–696

X2Y capacitors, 248–250

cavity

capacitor/cavity interaction, 325–327

cavity modes in two dimensions, 347–353

definition of, 275

fringe field capacitance

overview of, 279–285

in power puddles, 285–289

impedance profiles, 276–277

long, narrow cavities, loop inductance in, 290–292

modal resonances, 334–340

parallel plate capacitance, [278–279](#)

parameters, [370](#)

PCB cavity

impedance as Seen by die pads, [465–469](#)

role of, [469–476](#)

S-parameters, [461–462](#)

VRM (voltage regulator module), [460–465](#)

peak impedance, [364–367](#)

series LC resonance, [312–314](#)

signal integrity design

capacitor mounting inductance, [401–403](#)

cavity losses and impedance peak reduction,  
[408–411](#)

damping to suppress parallel resonant peaks,  
[403–408](#)

DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity  
resonance, [383–393](#)

lower impedance and higher damping, [367–371](#)

multiple capacitor values, [411–414](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

summary of, [418–419](#)

thin dielectric, [367–371](#)

transmission line circuit models, [419–423](#)

uncontrolled ESR capacitors, [414–417](#)

spreading inductance

capacitor location and, [327–332](#)

between contact points, [317–324](#)

extracting from 3D field solver, [304–306](#)

probing with transfer impedance, [353–360](#)

role of, [327–332](#)

saturating, 332–334

source contact location, 315–317

in wide cavities, 292–304

transmission line properties, 334–340

$C_{\text{bulk}}$ , 226, 480

$C_{\text{cap}}$ , 262

$C_{\text{cavity}}$ , 375, 402, 422

$C_{\text{die}}$ , 50

$C_{\text{down}}$ , 634

cgs units, 146

characteristic impedance, 33, 335

Bandini Mountain, 456–457

calculating, 574, 647

charge, 139. *See also* capacitance

checkerboard reduction factor, 669–671

circuits. *See also* impedance

circuit topology, identifying, 46–52

lumped circuit

PRF (parallel resonant frequency), 307–312

SRF (series resonance frequency), 307–312

models for real capacitors, 206–209

parallel RLC circuits

ESR (equivalent series resistance), 229–237

examples of, 42–46

impedance of, 34–35

impedance profiles, 209

resonant properties of, 36–42

series RLC circuits

examples of, 42–46

impedance of, 30–33

resonant properties of, 36–42

Class 1 capacitors, 222

Class 2 capacitors, [222–223](#)

Class 3 capacitors, [222–223](#)

C<sub>Len</sub>, [298](#)

C<sub>Len-fringe</sub>, [286](#)

C<sub>Len-fringe-image</sub>, [280](#)

C<sub>Len-image</sub>, [280](#)

C<sub>Len-pp</sub>, [286](#)

C<sub>Len-pp-image</sub>, [280](#), [281](#)

C<sub>Len-total</sub>, [286](#)

C<sub>load</sub>, [432](#)

clock edge current

capacitance referenced to both Vss and Vdd rails,  
[558–562](#)

as cause of PDN noise, [565–572](#)

clock edge droop, [579](#), [683–684](#)

clock edge noise, [431](#), [557–558](#), [661–664](#)

example of, [557–558](#)

impulses from SCL (Switched Capacitor Load),  
[613–622](#)

measurement example: embedded controller  
processor, [562–565](#)

waveforms composed of series of clock impulses,  
[622–629](#)

clock edge droop, [579](#), [683–684](#)

clock gating, [629–633](#)

clock swallowing, [629–633](#)

CMEs (coronal mass ejections), [156–157](#)

cobalt, [147](#), [168](#)

CoDC, [432](#), [453](#)

combining capacitors in parallel, [209–211](#)

constant current amplitude, [22–23](#)

constricting resistance, [93](#)

contact points, spreading inductance between, [317–324](#)

contact resistance

constricting, 93

ESR (equivalent series resistance), 118

four-point Kelvin resistance measurement technique,  
93–95

traditional two-wire resistance measurements, 94

controlled ESR capacitors, 238–240, 527–532

copper loop, measuring impedance of, 102–105

core power rails. *See* Vdd rails

coronal mass ejections (CMEs), 156–157

Coulombs, 143

$C_{pp}$ , 284, 286

$C_{pp\text{-image}}$ , 281

$C_{sect}$ , 262

$C_{total}$ , 284

$C_{up}$ , 634

current

clock edge current

capacitance referenced to both Vss and Vdd rails,  
558–562

as cause of PDN noise, 565–572

clock edge droop, 579, 683–684

clock edge noise, 431, 557–558, 661–664

example of, 557–558

impulses from SCL (Switched Capacitor Load),  
613–622

measurement example: embedded controller  
processor, 562–565

waveforms composed of series of clock impulses,  
622–629

current waveforms, 577–579

impulse current waveform, 577, 579–581, 613–629,  
696–702

resonance current waveform, 577, 585–589  
rogue wave effect, 602–613  
step current waveform, 577, 582–584  
inrush current, 633–634  
leakage current, 659  
max current consumed, 659  
maximum dynamic current, 659  
minimum current consumed, 659  
minimum dynamic current, 659  
PRC (PDN Resonance Calculator) spreadsheet, 658–661  
ratio of voltage to. See impedance  
through ideal capacitor, 19  
transient currents  
calculating target impedance with, 550–553  
clock gating, 629–633  
clock swallowing, 629–633  
estimating, 646  
importance of, 547–549  
impulse current waveform, 579–581  
on-die PDN current draw, 553–558  
peak impedance, 595–602  
power gating, 633–638  
PRC (PDN Resonance Calculator) spreadsheet, 731–738  
q-factor, 595–602  
reactive elements, 595–602  
resonance current waveform, 585–589  
rogue wave effect, 602–613  
step current waveform, 582–584  
target impedance, 589–595  
current waveforms, 577–579

impulse current waveform

definition of, [577](#)

impulses from SCL (Switched Capacitor Load),  
[613–622](#)

PDN response to, [579–581](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[696–702](#)

waveforms composed of series of clock impulses,  
[622–629](#)

resonance current waveform

definition of, [577](#)

PDN response to, [585–589](#)

rogue wave effect, [602–613](#)

step current waveform

definition of, [577](#)

PDN response to, [582–584](#)

## D

damping

Bandini Mountain, [456–460](#)

lower impedance and, [367–371](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[685–693](#)

suppressing parallel resonant peaks with, [403–408](#)

dB, [166](#)

DC blocking capacitors

number to carry return current, [393–397](#)

number to suppress cavity resonances, [387–393](#)

overview of, [383–386](#)

suboptimal numbers of DC capacitors, [397–401](#)

$D_{\text{cavity}}$ , [305, 310](#)

decoupling

controlled ESR capacitors, [527–532](#)

OPD (on-package decoupling capacitors), [532–539](#)

density

capacitance density, [435](#)

energy density in magnetic field, [159–162](#)

inductance density, [162](#)

magnetic field density (B), [155–159](#)

power density, [435](#)

density<sub>caps</sub>, [395](#)

density<sub>sig</sub>, [395](#)

design (PDN)

goals of, [643–645](#)

power integrity principles, summary of, [645–653](#)

PRC (PDN Resonance Calculator) spreadsheet

clock edge noise and on-die parameters, [661–664](#)

goal of, [658](#)

impulse, step, and resonance response, [696–702](#)

inductance, analyzing board and package

geometries for, [674–677](#)

input voltage, current, and target impedance

parameters, [658–661](#)

mounting inductance and resistance, [665–673](#)

OPD (on-package decoupling capacitors), [724–731](#)

overview of, [654–658](#)

performance figures of merit, [682–685](#)

q-factors in frequency and time domains, [703–710](#)

reduced loop inductance, [718–722](#)

reverse-engineering of PDN from measurements,

[740–747](#)

rise time and stimulation of impedance peak,

[710–717](#)

risk, performance, and cost tradeoffs, [739](#)

SCL (Switched Capacitor Load) model, [694–696](#)

significance of damping and q-factors, [685–693](#)

simulated and measured PDN impedance and voltage features, [754–757](#)

simulation-to-measurement correlation, [747–754](#)

SMPS (switch mode power supply) model, [722–724](#)

three loops of, [677–682](#)

transient current assumptions, [736–738](#)

transient response of PDN, [731–735](#)

robust design, [8–12](#)

rogue waves and, [610–613](#)

working design, [8–12](#)

device under test (DUT), [70](#)

Df, [229](#)

diamagnetic properties, [146–147](#)

die pads, impedance and, [465–469](#)

dielectric

impact on magnetic field lines, [146–147](#)

thickness of, [367–371](#)

dielectric constant (Dk), [180, 370–371, 376, 422](#)

diffusion junctions, [430](#)

DIP (dual in-line package), two leads in, [81–85](#)

dispersion (material), [288](#)

Dk (dielectric constant), [180, 370–371, 376, 422](#)

D<sub>k</sub><sub>eff</sub>, [189](#)

dl, [166](#)

dL/dv, [161](#)

dL<sub>Loop</sub>, [301](#)

domains

frequency domain, [428–430](#)

FDTIM (Frequency Domain Target Impedance Method), [514–521](#)

impedance in, [18–21](#)

PRC (PDN Resonance Calculator) spreadsheet,

time domain

current through ideal capacitor, 19

impedance in, 19

PRC (PDN Resonance Calculator) spreadsheet,

703–710

driving a resonance, 337

DUT (device under test), 70

D<sub>via</sub>, 305, 310

dynamic current

impulse current waveform

definition of, 577

PDN response to, 579–581

resonance current waveform

definition of, 577

PDN response to, 585–589

rogue wave effect, 602–613

step current waveform

definition of, 577

PDN response to, 582–584, 585–589

## E

e (energy density in magnetic field), 159–162

ecology (PDN). *See PDN (power delivery network)*

ecology

effective dielectric constant, 189

EIA (Electronics Industries Alliance), 223

electromagnetic compatibility (EMC), 364

ElectroMagnetic Units (EMU), 146

Electronics Industries Alliance (EIA), 223

embedded controller processor, measuring clock edge

currents in, 562–565

EMC (electromagnetic compatibility), 364

EMU (ElectroMagnetic Units), [146](#)

energy density in magnetic field, [159–162](#)

equivalent circuit models for real capacitors, [206–209](#)

equivalent series inductance (ESL), [118](#), [207](#)

equivalent series resistance. *See* [ESR \(equivalent series resistance\)](#)

ESL (equivalent series inductance), [118](#), [207](#), [516](#)

ESR (equivalent series resistance), [118](#), [207](#)

calculating, [681](#)

controlled ESR capacitors, [238–240](#), [527–532](#)

effective ESR, [403–408](#)

estimating from spec sheets, [234–237](#)

first and second order models, [229–234](#)

ODC (on-die decoupling capacitance), [436–439](#)

package PDN (power delivery network), [446](#)

estimating

ESR (equivalent series resistance), [234–237](#)

ODC (on-die decoupling capacitance), [431–435](#)

transient currents, [646](#)

external inductance, [167–172](#)

## F

$F_{\text{clock}}$ , [453–454](#)

FDTIM (Frequency Domain Target Impedance Method)

selecting capacitor values with, [516–521](#)

selecting number of capacitors with, [514–516](#)

ferrite materials, [147](#)

ferromagnetic materials, [147](#), [168](#)

field lines, flux of, [144–147](#)

fields, magnetic

energy density in, [159–162](#)

fringe field capacitance

overview of, [279–285](#)

in power puddles, [285–289](#)

## inductance

inductor impedance, [147–150](#)

in long, narrow cavities, [290–292](#)

magnetic field density ( $B$ ), [155–159](#)

principles of, [141–147](#)

quasi-static approximation, [150–155](#)

spreading inductance in wide cavities, [292–304](#)

mutual field lines, [173](#)

self-field lines, [173](#)

fixture, [106](#)

fixture artifacts, [105–109](#)

measured inductance of a via, [109–114](#)

small MLCC capacitor on board, [114–119](#)

flat impedance profiles, [550–553](#)

flux of field lines, [144–147](#)

$f_{\max\_lim}$ , [516](#)

four-point Kelvin resistance measurement technique,

[93–95](#)

frequency

Bandini Mountain, [452–456](#)

FDTIM (Frequency Domain Target Impedance Method)

selecting capacitor values with, [516–521](#)

selecting number of capacitors with, [514–516](#)

frequency domain, [428–430](#)

FDTIM (Frequency Domain Target Impedance Method), [514–521](#)

impedance in, [18–21](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[703–710](#)

peak impedance frequency, [35–36](#), [42](#)

PRF (parallel resonant frequency), [35](#), [307–312](#)

resonance frequencies, [336](#), [347–353](#)

SRF (series resonance frequency), [32–33](#), [307–312](#)

frequency domain

FDTIM (Frequency Domain Target Impedance Method)

selecting capacitor values with, [516–521](#)

selecting number of capacitors with, [514–516](#)

impedance in, [18–21](#)

PRC (PDN Resonance Calculator) spreadsheet, [703–710](#)

$f_{\text{res}}$ , [308](#), [375–376](#), [441](#), [647](#)

fringe field capacitance

overview of, [279–285](#)

in power puddles, [285–289](#)

$f_{\text{VRM-max}}$ , [226](#), [480](#)

## G

gating

clock gating, [629–633](#)

gate capacitance, [430](#)

power gating, [633–638](#)

$G_{\text{leakage}}$ , [688](#)

$G_{\text{Len}}$ , [344](#)

$G_{\text{load}}$ , [689](#)

ground bounce, [571](#)

ground rails. *See* [Vss rails](#)

## H

hacking the interconnect, [85](#)

$h_{\text{cavity}}$ , [422](#)

Henrys, [146](#)

higher bandwidth capacitor models, [258–272](#)

high-frequency range (ODC)

clock edge noise, [431](#)

ESR (equivalent series resistance), [436–439](#)

estimating, [431–435](#)

historic trends in, [435–436](#)

measuring, [434–435](#)

relaxation time, [438](#)

sources of, [430](#)

## I

$I_{\text{clk\_edge}}$ , [557](#)

IDC (interdigitated capacitor), [249](#)

ideal capacitors

current through, [19](#)

impedance, [205–206](#)

versus real capacitors, [26–30, 206](#)

$I_{\text{max-pair}}$ , [444–445, 453–454](#)

$I_{\text{max-transient}}$ , [8](#)

impedance

Bandini Mountain

characteristic impedance, [456–457](#)

frequency of, [452–456](#)

intrinsic damping of, [456–460](#)

overview of, [447–452](#)

peak impedance, [451–452, 494](#)

boundary conditions, [337–338](#)

calculating, [21–26](#)

characteristic impedance, [33, 335](#)

Bandini Mountain, [456–457](#)

calculating, [574, 647](#)

circuit topology, identifying, [46–52](#)

in frequency domain, [18–21](#)

of ideal capacitors, [205–206](#)

impedance matrix, [56–66](#)

self-impedances, [60](#)  
simulating, [64–66](#)  
transfer impedances, [60–64](#)

impedance profiles

controlled ESR capacitors, [527–532](#)  
flat impedance profiles, [550–553](#)  
package PDN (power delivery network), [441](#)  
PCB cavity, [469–474](#)

importance of, [17–18](#)

of inductors, [147–150](#)

input impedance of transmission lines, [340–342](#)

magnitude of, [25](#)

measurement

based on reflection of signals, [71–76](#)  
based on V/I definition of impedance, [70–71](#)  
fixture artifacts, [105–109](#)  
four-point Kelvin resistance measurement  
technique, [93–95](#)  
impedance of one-inch diameter copper loop,  
[102–105](#)  
impedance of small wire loop, [86–89](#)  
impedance of two leads in DIP, [81–85](#)  
importance of, [69](#)  
inductance of via, [109–114](#)  
limitations of measurements at low frequency,  
[89–93](#)  
measurement-based modeling, [85](#)  
MLCC capacitor on board, [114–119](#)  
on-die capacitance, [120–134](#)  
two-port low impedance measurement technique,  
[95–102](#)  
with VNA, [76–93](#)  
parallel resonant peak, [35](#)

parallel RLC circuits

calculating, 34–35

examples of, 42–46

resonant properties of, 36–42

PDN ratio, 12

peak impedance

Bandini Mountain, 451–452, 494

calculating, 650

equations governing, 572–576

frequency, 35–36, 42

limits to, 492–497

at PRF, 215–220

rise time and stimulation of impedance peak,

710–717

phase of, 25

of planes, 276–277

PRC (PDN Resonance Calculator) spreadsheet,

754–757

profiles

engineering, 12–14

parallel RLC circuits, 209

planes, 276–277

sculpting, 12–14

q-factor, 38–42

reactance, 20–21

real capacitors, 42–46

real versus ideal circuit components, 26–30, 206–209

resistance term, identifying, 46–52

as Seen by die pads, 465–469

series RLC circuits

calculating, 30–33

examples of, 42–46

resonant properties of, [36–42](#)

signal integrity design

capacitor mounting inductance, [401–403](#)

cavity losses and impedance peak reduction,  
[408–411](#)

damping to suppress parallel resonant peaks,  
[403–408](#)

DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity  
resonance, [383–393](#)

lower impedance and higher damping, [367–371](#)

lower impedance/higher damping, [367–371](#)

multiple capacitor values, [411–414](#)

peak impedance, [364–367](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

summary of, [418–419](#)

thin dielectric, [367–371](#)

transmission line circuit models, [419–423](#)

uncontrolled ESR capacitors, [414–417](#)

simulating, [21–26](#)

target impedance, [8–11](#), [589–595](#), [660](#)

calculating with flat impedance profiles, [550–553](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[658–661](#)

in time domain

current through ideal capacitor, [19](#)

impedance of capacitor, [19](#)

transfer impedances, [60–64](#), [353–360](#)

transient response, [52–56](#)

VRM (voltage regulator module), [476–478](#)

impedance matrix, [56–66](#)

self-impedances, [60](#)

simulating, [64–66](#)

transfer impedances, [60–64](#)

impedance profiles, [12–14](#)

Bandini Mountain

characteristic impedance, [456–457](#)

frequency of, [452–456](#)

intrinsic damping of, [456–460](#)

overview of, [447–452](#)

peak impedance, [451–452](#), [494](#)

controlled ESR capacitors, [527–532](#)

engineering, [12–14](#)

flat impedance profiles, [550–553](#)

MLCC (multilayer ceramic chip) capacitor, [44–46](#)

package PDN (power delivery network), [441](#)

parallel RLC circuits, [209](#)

PCB cavity, [469–474](#)

peak impedance frequency, [35–36](#), [42](#)

sculpting, [12–14](#)

impulse current waveform

definition of, [577](#)

impulses from SCL (Switched Capacitor Load),  
[613–622](#)

PDN response to, [579–581](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[696–702](#)

waveforms composed of series of clock impulses,  
[622–629](#)

inductance. *See also* [capacitance](#)

capacitor mounting inductance, [401–403](#)

checkerboard reduction factor, [669–671](#)

density, [162](#)

EMU (ElectroMagnetic Units), [146](#)

energy density in magnetic field, [159–162](#)

ESL (equivalent series inductance), [118](#), [207](#)

external, [167–172](#)

flux of field lines, [144–147](#)

higher bandwidth capacitor models, [258–272](#)

importance of, [137–138](#)

inductance density, [162](#)

inductance per square, [183–185](#)

inductor impedance, [147–150](#)

internal, [167–172](#)

International System of Units, [142](#)

loop inductance

approximations for, [176–178](#)

extracting from S-parameters with 3D field solver,  
[195–202](#)

in long, narrow cavities, [290–292](#)

Maxwell's Equations, [163–167](#)

of mounted capacitors, [240–250](#)

package PDN (power delivery network), [441–446](#)

parallel plate approximation for loop inductance,  
[183](#)

versus partial inductance, [172–175](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[674–677](#), [718–722](#)

round loop inductance, approximations for,  
[179–182](#)

rule of thumb for, [194–195](#)

uniform round conductors, [175–178](#)

uniform transmission line inductance,  
approximations for, [188–193](#)

wide conductors close together, [182–187](#)

magnetic field density (B), [155–159](#)

Maxwell's Equations, [163–167](#)  
measurement of, [109–114](#)  
mutual, [172–175](#)  
package lead inductance, [521–527](#)  
partial, [172–175](#), [194](#)  
PRC (PDN Resonance Calculator) spreadsheet,  
[665–673](#)  
principles of, [141–147](#)  
quasi-static approximation, [150–155](#)  
self-inductance, [172–175](#)  
sheet inductance, [183–185](#), [290](#), [673](#)  
skin depth, [167–172](#)  
spreading inductance  
    capacitor location and, [327–332](#)  
    capacitor mounting inductance and, [401–403](#)  
    between contact points, [317–324](#)  
    extracting from 3D field solver, [304–306](#)  
    PCB cavity, [470](#)  
    probing with transfer impedance, [353–360](#)  
    role of, [327–332](#)  
    saturating, [332–334](#)  
    source contact location, [315–317](#)  
    in wide cavities, [292–304](#)  
    via inductance, [109–114](#)  
VRM (voltage regulator module), [478](#)  
inductors, impedance of, [20–21](#), [147–150](#)  
input impedance of transmission lines, [340–342](#)  
input voltage (PRC), [658–661](#)  
inrush current, [633–634](#)  
integrity of signals. *See* [signal integrity design](#)  
interconnect, hacking, [85](#)  
interdigitated capacitor (IDC), [249](#)

internal inductance, 167–172

International System of Units, 142

$I_{pk-pk}$ , 585, 651

iron, 147, 168

$I_{transient}$ , 585, 651

## J-K

jitter, sensitivity to PDN noise, 5

Kelvin resistance measurement technique, 93–95

Kenworthy, Dave, 448

Keysight Technologies' ADS (Advanced System Design),  
22, 84–85

Kramers-Kronig relationship, 25

## L

$L_{blocking\_cap}$ , 387

$L_{bottom}$ , 262–263

$L_{cap}$ , 263

$L_{caps}$ , 401

LDO (low drop out) regulators, 225

leakage current, 659

leakage resistance, 664

$L_{cavity}$ , 422

$L_{Len}$ , 176–178, 298

$L_{Len-via}$ , 387

$L_{loop}$ , 182, 290, 442, 445, 453, 672

$L_{mount}$ , 262–263, 387

$L_{mounting}$ , 327–328

load, 430

loop impedance. *See* impedance

loop inductance

of mounted capacitors, 240–250

package PDN (power delivery network), 441–446

PRC (PDN Resonance Calculator) spreadsheet,

674–677, 718–722

loop inductance per square. *See* sheet inductance

loop resistance (PRC), 665–673

loops. *See also* inductance

measuring impedance of, 95–102

loop resistance, 49

one-inch diameter copper loop, 102–105

small wire loop, 86–89

two-port low impedance measurement technique,  
95–102

PRC (PDN Resonance Calculator) spreadsheet,

677–682

lossy transmission line models, 260, 269–272

low drop out (LDO) regulators, 225

low impedance, measuring

based on reflection of signals, 71–76

based on V/I definition of impedance, 70–71

fixture artifacts, 105–109

measured inductance of a via, 109–114

small MLCC capacitor on board, 114–119

four-point Kelvin resistance measurement technique,

93–95

impedance of one-inch diameter copper loop, 102–105

importance of, 69

measurement-based modeling, 85

MLCC capacitor on board, 114–119

on-die capacitance, 120–134

two-port low impedance measurement technique,  
95–102

via inductance, 109–114

with VNA, 76–80

impedance of small wire loop, 86–89

impedance of two leads in DIP, 81–85

limitations of measurements at low frequency,  
89–93

low-frequency properties of planes

fringe field capacitance

overview of, 279–285

in power puddles, 285–289

parallel plate capacitance, 278–279

$L_{\text{package}}$ , 50

$L_{\text{per-len}}$ , 442, 445, 453–454

$L_{\text{plates}}$ , 262–263

$L_{\text{point-cavity}}$ , 322

$L_{\text{point-point}}$ , 322–324

$L_{\text{sect}}$ , 261

$L_{\text{self}}$ , 194

$L_{\text{spread}}$ , 402

$L_{\text{spreading}}$ , 327

$L_{\text{sq}}$ , 183, 184, 290, 322, 672

$L_{\text{tline}}$ , 266

$L_{\text{total}}$ , 113

lumped circuit

PRF (parallel resonant frequency), 307–312

SRF (series resonance frequency), 307–312

$L_{\text{via}}$ , 295, 375, 387

$L_{\text{VRM}}$ , 480

## M

magnetic field density ( $B$ ), 155–159

magnetic fields

energy density in, 159–162

flux of, 144–147

fringe field capacitance

overview of, 279–285

in power puddles, [285–289](#)

## inductance

inductor impedance, [147–150](#)

in long, narrow cavities, [290–292](#)

magnetic field density ( $B$ ), [155–159](#)

principles of, [141–147](#)

quasi-static approximation, [150–155](#)

spreading inductance in wide cavities, [292–304](#)

mutual field lines, [173](#)

self-field lines, [173](#)

magnitude of impedance, [25](#)

material dispersion, [288](#)

matrix (impedance), [56–66](#)

self-impedances, [60](#)

simulating, [64–66](#)

transfer impedances, [60–64](#)

max current consumed, [659](#)

maximum dynamic current, [659](#)

Maxwells, [142](#)

Maxwell's Equations, [163–167](#)

## measurement

clock edge noise, [562–565](#)

### impedance

based on reflection of signals, [71–76](#)

based on V/I definition of impedance, [70–71](#)

fixture artifacts, [105–109](#)

four-point Kelvin resistance measurement

technique, [93–95](#)

impedance of one-inch diameter copper loop,

[102–105](#)

impedance of small wire loop, [86–89](#)

impedance of two leads in DIP, [81–85](#)

importance of, [69](#)

inductance of via, [109–114](#)

limitations of measurements at low frequency,  
[89–93](#)

measurement-based modeling, [85](#)

MLCC capacitor on board, [114–119](#)

on-die capacitance, [120–134](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[754–757](#)

two-port low impedance measurement technique,  
[95–102](#)

with VNA, [76–93](#)

measurement-based modeling, [85](#)

ODC (on-die decoupling capacitance), [434–435](#)

reverse-engineering of PDN features from, [740–747](#)

simulation-to-measurement correlation, [747–754](#)

metallization, [430, 435](#)

minimum amount of capacitance required, [478–483](#)

minimum current consumed, [659](#)

minimum dynamic current, [659](#)

MLCC (multilayer ceramic chip) capacitors. *See also*  
impedance

bulk capacitance, [225–229](#)

combining in parallel, [209–211](#)

controlled ESR capacitors, [238–240](#)

engineering capacitance of, [220–222](#)

equivalent circuit models for real capacitors, [206–209](#)

ESR (equivalent series resistance)

controlled ESR capacitors, [238–240](#)

estimating from spec sheets, [234–237](#)

first and second order models, [229–234](#)

FDTIM (Frequency Domain Target Impedance  
Method)

selecting capacitor values with, [516–521](#)

selecting number of capacitors with, [514–516](#)

higher bandwidth models, [258–272](#)

impedance

    impedance profiles, [44–46](#)

    measuring, [114–119](#)

importance of, [205–206](#)

one value MLCC capacitor

    impact of, [498–501](#)

    optimizing, [502–507](#)

PRF (parallel resonant frequency)

    calculating, [211–215](#)

    peak impedance at PRF, [215–220](#)

reduced loop inductance of, [718–722](#)

temperature and voltage stability, [222–225](#)

three values of MLCC capacitors

    impact of, [507–511](#)

    optimizing, [511–514](#)

vendor-supplied S-parameter models, [251–258](#)

modal resonance

    attenuation, [343–347](#)

    cavity modal resonances, [334–340](#)

    cavity modes in two dimensions, [347–353](#)

    input impedance and, [340–342](#)

    suppression of

        capacitor mounting inductance, [401–403](#)

        cavity losses and impedance peak reduction,  
[408–411](#)

        damping to suppress parallel resonant peaks,  
[403–408](#)

        DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity resonance, [383–393](#)

lower impedance and higher damping, [367–371](#)

multiple capacitor values, [411–414](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

thin dielectric, [367–371](#)

uncontrolled ESR capacitors, [414–417](#)

modeling

measurement-based, [85](#)

planes with transmission line circuits, [419–423](#)

modes of transmission line, [334–340](#)

mounted capacitors, loop inductance of, [240–250](#)

mounting inductance (PRC), [665–673](#)

multilayer ceramic chip capacitors. *See* [MLCC](#)

(multilayer ceramic chip) capacitors

multiple capacitor values to suppress impedance peak, [411–414](#)

multiple via pair contacts, [460–465](#)

mutual (transfer) impedances, [60–64](#)

mutual field lines, [173](#)

mutual inductance, [172–175](#)

## N

nanoHenrys (nH), [146](#)

narrow cavities, loop inductance in, [290–292](#)

$n_{\text{caps}}$ , [388, 394](#)

n-channel, [560](#)

nH (nanoHenry), [146](#)

nickel, [147, 168](#)

noise, voltage

clock edge current, [431](#)

capacitance referenced to both Vss and Vdd rails,

## 558–562

as cause of PDN noise, 565–572

example of, 557–558

impulses from SCL (Switched Capacitor Load),  
613–622

measurement example: embedded controller  
processor, 562–565

PRC (PDN Resonance Calculator) spreadsheet,  
661–664

waveforms composed of series of clock impulses,  
622–629

peak impedance, 364–367, 595–602

peak-to-peak voltage noise, 585–588, 651

performance and, 3–7

q-factor, 595–602

reactive elements, 595–602

ringing voltage noise, 54–56

rogue wave effect, 602–613

signal integrity design

capacitor mounting inductance, 401–403

cavity losses and impedance peak reduction,

408–411

damping, 367–371

damping to suppress parallel resonant peaks,  
403–408

DC blocking capacitors to carry return current,  
393–397

DC blocking capacitors to suppress cavity  
resonance, 383–393

lower impedance/higher damping, 367–371

peak impedance, 364–367

shorting vias, 372–383

suboptimal numbers of DC capacitors, 397–401

thin dielectric, [367–371](#)

target impedance, [8–11](#)

transient current

calculating target impedance with, [550–553](#)

importance of, [547–549](#)

on-die PDN current draw, [553–558](#)

upper limit of, [5–7](#)

$n_{pairs}$ , [442, 444–445](#)

$n$ -port circuits, impedance in. *See* [impedance matrix](#)

$n_{sig}$ , [394](#)

## O

ODC (on-die decoupling capacitance), [48–52](#)

clock edge noise, [431, 565–572](#)

ESR (equivalent series resistance), [436–439](#)

estimating, [431–435](#)

historic trends in, [435–436](#)

impedance, [120–134](#)

large on-die capacitance with small package lead

inductance, [521–527](#)

measuring, [434–435](#)

relaxation time, [438](#)

sources of, [430](#)

on-die decoupling capacitance. *See* [ODC \(on-die decoupling capacitance\)](#)

on-die parameters (PRC), [661–664](#)

on-die PDN current draw, [553–558](#)

on-die series resistance, [663](#)

one value MLCC capacitor

impact of, [498–501](#)

optimizing single MLCC capacitance value, [502–507](#)

one-inch diameter copper loop, measuring impedance of, [102–105](#)

OPD (on-package decoupling capacitors), [455](#), [532–539](#),  
[724–731](#)

optimization

bulk capacitors, [483–487](#)

MLCC (multilayer ceramic chip) capacitors

single MLCC, [502–507](#)

three values of MLCC capacitors, [511–514](#)

oscilloscopes, [76–77](#)

oxides, [93](#)

## P

package lead inductance, [521–527](#)

package PDN (power delivery network)

components of, [440](#)

ESR (equivalent series resistance), [446](#)

impedance profiles, [441](#)

loop inductance, [441–446](#)

parallel, connecting multiple capacitors in, [209–211](#)

parallel elements, [30](#), [46](#)

parallel plate approximation for loop inductance, [183](#)

parallel plate capacitance, [278–279](#)

parallel resonant frequency (PRF), [35](#)

calculating, [211–215](#)

lumped circuit, [307–312](#)

peak impedance at PRF, [215–220](#)

parallel resonant peaks, [35](#), [403–408](#)

parallel RLC circuits

examples of, [42–46](#)

impedance of, [34–35](#)

peak impedance at PRF, [215–220](#)

PRF (parallel resonant frequency), [211–215](#)

resonant properties of, [36–42](#)

scaled values, [209–211](#)

SRF (series resonance frequency), [211](#)

paramagnetic properties, [146–147](#)

partial inductance, [172–175](#), [194](#)

PCB cavity

impedance as Seen by die pads, [465–469](#)

impedance profile, [469–474](#)

role of, [469–476](#)

S-parameters, [461–462](#)

VRM (voltage regulator module), [460–465](#)

p-channel, [555](#), [560](#)

PDN (power delivery network) design. *See also* [design \(PDN\)](#)

PDN (power delivery network) ecology, [6](#). *See also*

[impedance](#)

Bandini Mountain

characteristic impedance, [456–457](#)

frequency of, [452–456](#)

intrinsic damping of, [456–460](#)

overview of, [447–452](#)

peak impedance, [494](#)

building, [488–492](#)

bulk capacitors

minimum amount of capacitance required,  
[478–483](#)

optimizing, [483–487](#)

controlled ESR capacitors, [527–532](#)

engineering, [5–7](#)

FDTIM (Frequency Domain Target Impedance  
Method)

selecting capacitor values with, [516–521](#)

selecting number of capacitors with, [514–516](#)

frequency domain, [428–430](#)

impedance profile, [12–14](#)

large on-die capacitance with small package lead inductance, [521–527](#)

MLCC (multilayer ceramic chip) capacitors

  impact of one value MLCC capacitor, [498–501](#)

  impact of three values of MLCC capacitors, [507–511](#)

  optimizing single MLCC capacitance value,

[502–507](#)

  optimizing values of three capacitors, [511–514](#)

multiple chips sharing rail, [540–543](#)

ODC (on-die decoupling capacitance)

  clock edge noise, [431](#)

  ESR (equivalent series resistance), [436–439](#)

  estimating, [431–435](#)

  historic trends in, [435–436](#)

  measuring, [434–435](#)

  relaxation time, [438](#)

  sources of, [430](#)

OPD (on-package decoupling capacitors), [532–539](#)

overview of, [1–5](#)

package PDN

  components of, [440](#)

  ESR (equivalent series resistance), [446](#)

  impedance profiles, [441](#)

  loop inductance, [441–446](#)

PCB cavity

  impedance as Seen by die pads, [465–469](#)

  impedance profile, [469–474](#)

  role of, [469–476](#)

  S-parameters, [461–462](#)

VRM (voltage regulator module), [460–465](#)

PDN ratio, [12](#)

peak impedance, limits to, [492–497](#)

power ground planes with multiple via pair contacts,

460–465

power puddles, 476

purpose of, 2

robust design, 8–12

schematic of, 6

VRM (voltage regulator module)

impedance, 476–478

inductance, 478

working design, 8–12

PDN (power delivery network) ratio, 12

PDN (power delivery network) response

to impulse of dynamic current, 579–581

PRC (PDN Resonance Calculator) spreadsheet,  
696–702

to square wave of dynamic current at resonance,  
585–589

to step change in dynamic current, 582–584

target impedance and, 589–595

PDN Resonance Calculator spreadsheet. *See PRC (PDN Resonance Calculator) spreadsheet*

peak impedance

Bandini Mountain, 451–452, 494

calculating, 650

equations governing, 572–576

frequency, 35–36, 42

impact on voltage noise, 595–602

limits to, 492–497

at PRF (parallel resonant frequency), 215–220

rise time and stimulation of impedance peak, 710–717

signal integrity design

capacitor mounting inductance, 401–403

cavity losses and impedance peak reduction,

408–411

damping to suppress parallel resonant peaks,

403–408

DC blocking capacitors to carry return current,

393–397

DC blocking capacitors to suppress cavity

resonance, 383–393

lower impedance/higher damping, 367–371

multiple capacitor values, 411–414

peak impedance, 364–367

shorting vias, 372–383

suboptimal numbers of DC capacitors, 397–401

summary of, 418–419

thin dielectric, 367–371

transmission line circuit models, 419–423

uncontrolled ESR capacitors, 414–417

peak impedance frequency, 35–36, 42

peak-to-peak voltage noise, 585–588, 651

performance figures of merit (PRC), 682–685

permeability, relative, 168

pH (picoHenrys), 146

phase locked loops (PLLs), 5

phase of impedance, 25

picoHenrys (pH), 146

planes, 305. *See also* cavity

impedance, 276–277

loop inductance in long, narrow cavities, 290–292

low-frequency properties

fringe field capacitance, 279–285

fringe field capacitance in power puddles, 285–289

parallel plate capacitance, 278–279

lumped-circuit PRF, 307–312

lumped-circuit SRF, [307–312](#)

modal resonance

attenuation, [343–347](#)

cavity modal resonances, [334–340](#)

cavity modes in two dimensions, [347–353](#)

input impedance and, [340–342](#)

power ground planes with multiple via pair contacts,  
[460–465](#)

role of, [275–277](#)

series LC resonance, [312–314](#)

signal integrity design

capacitor mounting inductance, [401–403](#)

cavity losses and impedance peak reduction,  
[408–411](#)

damping to suppress parallel resonant peaks,  
[403–408](#)

DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity  
resonance, [383–393](#)

lower impedance and higher damping, [367–371](#)

multiple capacitor values, [411–414](#)

peak impedance, [364–367](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

summary of, [418–419](#)

thin dielectric, [367–371](#)

transmission line circuit models, [419–423](#)

uncontrolled ESR capacitors, [414–417](#)

spreading inductance

capacitor location and, [327–332](#)

between contact points, [317–324](#)

extracting from 3D field solver, [304–306](#)

probing with transfer impedance, [353–360](#)

role of, [327–332](#)

saturating, [332–334](#)

source contact location, [315–317](#)

in wide cavities, [292–304](#)

transmission lines

input impedance of, [340–342](#)

properties, [334–340](#)

PLLs (phase locked loops), [5](#)

Poisson profile, [616–617](#)

Polar Instruments SI 9000 2D field solver, [282](#)

ports, [57](#)

definition of, [76](#)

two-port low impedance measurement technique,  
[95–102](#)

power density, [435](#)

power gating, [633–638](#)

power ground planes with multiple via pair contacts,  
[460–465](#)

power integrity principles, summary of, [645–653](#)

power puddles

definition of, [476](#)

fringe field capacitance in, [285–289](#)

power rails, voltage noise on, [3–5](#)

PRBS (pseudo random bit sequence), [5](#)

PRC (PDN Resonance Calculator) spreadsheet

clock edge noise and on-die parameters, [661–664](#)

goal of, [658](#)

impulse, step, and resonance response, [696–702](#)

inductance, analyzing board and package geometries  
for, [674–677](#)

input voltage, current, and target impedance  
parameters, [658–661](#)

mounting inductance and resistance, [665–673](#)  
OPD (on-package decoupling capacitors), [724–731](#)  
overview of, [654–658](#)  
performance figures of merit, [682–685](#)  
q-factors in frequency and time domains, [703–710](#)  
reduced loop inductance, [718–722](#)  
reverse-engineering of PDN from measurements,  
[740–747](#)  
rise time and stimulation of impedance peak, [710–717](#)  
risk, performance, and cost tradeoffs, [739](#)  
SCL (Switched Capacitor Load) model, [694–696](#)  
significance of damping and q-factors, [685–693](#)  
simulated and measured PDN impedance and voltage  
features, [754–757](#)  
simulation-to-measurement correlation, [747–754](#)  
SMPS (switch mode power supply) model, [722–724](#)  
three loops of, [677–682](#)  
transient current assumptions, [736–738](#)  
transient response of PDN, [731–735](#)  
PRF (parallel resonant frequency), [35](#)  
calculating, [211–215](#)  
lumped circuit, [307–312](#)  
peak impedance at PRF, [215–220](#)  
probing spreading inductance, [353–360](#)  
profiles, impedance  
Bandini Mountain  
characteristic impedance, [456–457](#)  
frequency of, [452–456](#)  
intrinsic damping of, [456–460](#)  
overview of, [447–452](#)  
peak impedance, [451–452, 494](#)  
controlled ESR capacitors, [527–532](#)

engineering, 12–14

flat impedance profiles, 550–553

MLCC (multilayer ceramic chip) capacitor, 44–46

package PDN (power delivery network), 441

parallel RLC circuits, 209

PCB cavity, 469–474

peak impedance frequency, 35–36, 42

planes, 276–277

sculpting, 12–14

properties

of planes

fringe field capacitance, 279–285

fringe field capacitance in power puddles, 285–289

parallel plate capacitance, 278–279

of transmission lines, 334–340

pseudo random bit sequence (PRBS), 5

psi, 142–143

puddles (power), fringe field capacitance in, 285–289

pulse swallowing, 629–633

## Q

$Q_{\text{clk\_edge}}$ , 557

q-factor, 38–42, 236–237, 587

Bandini Mountain, 457–459

calculating, 648

impact on voltage noise, 595–602

PRC (PDN Resonance Calculator) spreadsheet

q-factors in frequency and time domains, 703–710

significance of damping and q-factors, 685–693

quasi-static approximation (inductance), 150–155

QUCS (Quite Universal Circuit Simulator), 22, 84–85

## R

$R_{\text{cavity}}$ , [295–296](#)

$R_{\text{dc}}$ , [231](#)

reactance, [20–21](#)

reactive elements, impact on voltage noise, [595–602](#)

real capacitors

equivalent circuit models for, [206–209](#)

ESR (equivalent series resistance), [229–234](#)

versus ideal capacitors, [26–30](#), [206](#)

reduced loop inductance, [718–722](#)

reflection coefficient, [73](#), [79–80](#)

reflection of signals, [71–76](#)

relative permeability, [168](#)

$R_{\text{equivalent}}$ , [50](#)

resistance

constricting, [93](#)

ESR (equivalent series resistance), [118](#), [207](#)

controlled ESR capacitors, [238–240](#)

estimating from spec sheets, [234–237](#)

first and second order models, [229–234](#)

four-point Kelvin resistance measurement technique,  
[93–95](#)

leakage resistance, [664](#)

on-die series resistance, [663](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[665–673](#)

resistance term, identifying, [46–52](#)

sheet resistance, [673](#)

traditional two-wire resistance measurements, [94](#)

resonance

driving, [337](#)

frequencies, [336](#)

modal resonance

attenuation, [343–347](#)

cavity modal resonances, [334–340](#)

cavity modes in two dimensions, [347–353](#)

input impedance and, [340–342](#)

PRF (parallel resonant frequency)

calculating, [211–215](#)

lumped circuit, [307–312](#)

peak impedance at PRF, [215–220](#)

resonance current waveform

definition of, [577](#)

PDN response to, [585–589](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[696–702](#)

series LC resonance, [312–314](#)

signal integrity design

damping, [367–371](#)

shorting vias, [372–383](#)

thin dielectric, [367–371](#)

SRF (series resonance frequency), [209–210, 307–312](#)

transmission line properties, [334–340](#)

resonance current waveform

definition of, [577](#)

PDN response to, [585–589](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[696–702](#)

resonant properties

of parallel RLC circuits, [36–42](#)

of series RLC circuits, [36–42](#)

responses (PDN)

to impulse of dynamic current, [579–581](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[696–702](#)

to square wave of dynamic current at resonance,

585–589

to step change in dynamic current, 582–584

target impedance and, 589–595

return current, DC blocking capacitors needed to carry,

393–401

reverse aspect ratio capacitors, 246

reverse-engineering PDN, 740–747

ringing voltage noise, 54–56

rise time, stimulation of impedance peak and, 710–717

RLC circuits

ESR (equivalent series resistance)

controlled ESR capacitors, 238–240

first and second order models, 229–234

examples of, 42–46

parallel RLC circuits

examples of, 42–46

impedance of, 34–35

impedance profiles, 209

peak impedance at PRF, 215–220

PRF (parallel resonant frequency), 211–215

resonant properties of, 36–42

scaled values, 209–211

SRF (series resonance frequency), 211

series RLC circuits

impedance of, 30–33

resonant properties of, 36–42

R<sub>leads</sub>, 50

R<sub>leakage</sub>, 688

R<sub>Len</sub>, 344, 369

R<sub>load</sub>, 689

R<sub>loop-ESR</sub>, 689

$R_{\text{metalization}}$ , [50](#)

robust PDN design, [8–12](#)

$R_{\text{ODC-ESR}}$ , [689](#)

rogue wave effect, [602–613](#)

round loop inductance, [179–182](#)

$R_{\text{sect}}$ , [262](#)

$R_{\text{series}}$ , [39](#)

$R_{\text{via}}$ , [295–296](#)

## S

saturating spreading inductance, [332–334](#)

scaled values, [209–211](#)

scattering parameter, [78–80](#), [102–103](#)

extracting loop inductance from, [195–202](#)

PCB cavity, [461–462](#)

vendor-supplied S-parameter capacitor models,  
[251–258](#)

SCL (Switched Capacitor Load)

impulses from, [613–622](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[694–696](#)

sculpting PDN impedance profile, [12–14](#)

self-field lines, [173](#)

self-impedances, [60](#)

self-inductance, [172–175](#)

self-resonant frequency (SRF), [307–312](#)

series elements, [30](#), [46](#)

series LC resonance, [312–314](#)

series resonance frequency (SRF), [32–33](#), [209–210](#)

series RLC circuits

examples of, [42–46](#)

impedance of, [30–33](#)

resonant properties of, [36–42](#)

sheet inductance, [183–185](#), [290](#), [673](#)

sheet resistance, [673](#)

shorting vias, cavity resonance suppression with,  
[372–383](#)

SI 9000 2D field solver (Polar Instruments), [282](#)

SI units, [142–143](#)

signal integrity design

capacitor mounting inductance, [401–403](#)

cavity losses, [408–411](#)

damping to suppress parallel resonant peaks,  
[403–408](#)

DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity resonance,  
[383–393](#)

lower impedance and higher damping, [367–371](#)

lower impedance/higher damping, [367–371](#)

multiple capacitor values, [411–414](#)

overview of, [363–364](#)

peak impedance, [364–367](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

summary of, [418–419](#)

thin dielectric, [367–371](#)

transmission line circuit models, [419–423](#)

uncontrolled ESR capacitors, [414–417](#)

signal propagation, [72](#)

signals, reflected, [71–76](#)

Simbeor, extracting loop inductance with, [195–202](#)

simulations

impedance, [21–26](#)

impedance matrix, [64–66](#)

PRC (PDN Resonance Calculator) spreadsheet

simulated and measured PDN impedance and voltage features, [754–757](#)  
simulation-to-measurement correlation, [747–754](#)  
simultaneous switch noise (SSN) problem, [564–565](#)  
sine waves  
    of constant current amplitude, [22–23](#)  
    in frequency domain, [19–20](#)  
    highest expected sine wave frequency, [54](#)  
    scattering parameter, [78–80](#), [102–103](#)  
    sine wave output voltage, [23](#)  
VNA (vector network analyzer) ports and, [78](#)  
skin depth, [167–172](#)  
SMPS (switch mode power supply) model, [722–724](#)  
source contact location, spreading inductance and, [315–317](#)  
S-parameter, [78–80](#), [102–103](#)  
    extracting loop inductance from, [195–202](#)  
    PCB cavity, [461–462](#)  
    vendor-supplied S-parameter capacitor models, [251–258](#)  
spec sheets, estimating ESR from, [234–237](#)  
SpiCAP, [236](#)  
spreading inductance  
    capacitor location and, [327–332](#)  
    capacitor mounting inductance and, [401–403](#)  
    between contact points, [317–324](#)  
    extracting from 3D field solver, [304–306](#)  
    PCB cavity, [470](#)  
    probing with transfer impedance, [353–360](#)  
    role of, [327–332](#)  
    saturating, [332–334](#)  
    source contact location, [315–317](#)

in wide cavities, [292–304](#)

spreading resistance, [93](#)

spreadsheet, PRC (PDN Resonance Calculator), [343](#)

clock edge noise and on-die parameters, [661–664](#)

goal of, [658](#)

impulse, step, and resonance response, [696–702](#)

inductance, analyzing board and package geometries for, [674–677](#)

input voltage, current, and target impedance parameters, [658–661](#)

mounting inductance and resistance, [665–673](#)

OPD (on-package decoupling capacitors), [724–731](#)

overview of, [654–658](#)

performance figures of merit, [682–685](#)

q-factors in frequency and time domains, [703–710](#)

reduced loop inductance, [718–722](#)

reverse-engineering of PDN from measurements, [740–747](#)

rise time and stimulation of impedance peak, [710–717](#)

risk, performance, and cost tradeoffs, [739](#)

SCL (Switched Capacitor Load) model, [694–696](#)

significance of damping and q-factors, [685–693](#)

simulated and measured PDN impedance and voltage features, [754–757](#)

simulation-to-measurement correlation, [747–754](#)

SMPS (switch mode power supply) model, [722–724](#)

three loops of, [677–682](#)

transient current assumptions, [736–738](#)

transient response of PDN, [731–735](#)

SRF (series resonance frequency), [32–33, 209–210, 307–312](#)

SSN (simultaneous switch noise) problem, [564–565](#)

stability, [222–225](#)

step current waveform

definition of, [577](#)

PDN response to, [582–584](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[696–702](#)

suppression of modal resonance

capacitor mounting inductance, [401–403](#)

cavity losses and impedance peak reduction, [408–411](#)

damping to suppress parallel resonant peaks,  
[403–408](#)

DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity resonance,  
[383–393](#)

lower impedance and higher damping, [367–371](#)

multiple capacitor values, [411–414](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

thin dielectric, [367–371](#)

uncontrolled ESR capacitors, [414–417](#)

Svia-via, [376](#)

switch mode power supply (SMPS) model, [722–724](#)

Switched Capacitor Load (SCL)

impulses from, [613–622](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[694–696](#)

## T

tantalum capacitor, [43](#)

target impedance, [8–11](#), [589–595](#), [660](#)

calculating with flat impedance profiles, [550–553](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[658–661](#)

TD (time delay), [188](#), [335](#)

Teledyne LeCroy HDO 12-bit resolution scope, [563](#)

Telegrapher's Equations, [93](#)

temperature (MLCC), [222](#)–[225](#)

thin dielectric, cavity noise reduction via, [367](#)–[371](#)

Thomson, William, [93](#)

three values of MLCC capacitors

impact of, [507](#)–[511](#)

optimizing, [511](#)–[514](#)

three-terminal cap, [248](#)–[250](#)

time delay (TD), [188](#), [335](#)

time domain

current through ideal capacitor, [19](#)

impedance of capacitor in, [19](#)

PRC (PDN Resonance Calculator) spreadsheet,  
[703](#)–[710](#)

topology, identifying, [46](#)–[52](#)

traditional two-wire resistance measurements, [94](#)

transfer impedances, [60](#)–[64](#), [353](#)–[360](#)

transient currents

calculating target impedance with, [550](#)–[553](#)

clock edge current

capacitance referenced to both Vss and Vdd rails,  
[558](#)–[562](#)

as cause of PDN noise, [565](#)–[572](#)

clock edge droop, [579](#), [683](#)–[684](#)

example of, [557](#)–[558](#)

impulses from SCL (Switched Capacitor Load),  
[613](#)–[622](#)

measurement example: embedded controller  
processor, [562](#)–[565](#)

waveforms composed of series of clock impulses,  
[622](#)–[629](#)

clock gating, [629–633](#)  
clock swallowing, [629–633](#)  
current waveforms, [577–579](#)  
estimating, [646](#)  
importance of, [547–549](#)  
impulse current waveform  
    definition of, [577](#)  
    PDN response to, [579–581](#)  
on-die PDN current draw, [553–558](#)  
peak impedance  
    equations governing, [572–576](#)  
    impact on voltage noise, [595–602](#)  
power gating, [633–638](#)  
PRC (PDN Resonance Calculator) spreadsheet  
    transient current assumptions, [736–738](#)  
    transient response of PDN, [731–735](#)  
q-factor, [595–602](#)  
reactive elements, [595–602](#)  
resonance current waveform  
    definition of, [577](#)  
    PDN response to, [585–589](#)  
rogue wave effect, [602–613](#)  
step current waveform  
    definition of, [577](#)  
    PDN response to, [582–584](#)  
target impedance, [589–595](#)  
transient response, [52–56](#), [731–735](#)  
transimpedances, [60–61](#)  
transmission lines  
    circuit models, [419–423](#)  
    input impedance of, [340–342](#)  
    modal resonance

attenuation, 343–347

cavity modal resonances, 334–340

input impedance and, 340–342

properties, 334–340

two leads in DIP, measuring impedance of, 81–85

two-port low impedance measurement technique,

95–102

two-wire resistance measurements, 94

## U

uncontrolled ESR capacitors, 414–417

uniform round conductors, 175–178

uniform transmission line inductance, approximations

for, 188–193

## V

$V_1$ , 56

$V_{dd}$ , 557

$V_{dd-}$  634

Vdd rails

clock edge current, 557–562

clock edge noise, 431

probing configuration for, 120

voltage droop on, 432

voltage noise on, 3–5

$V_{dd+}$ , 634

$V_{ddo}$ , 432

$V_{dd1}$ , 432

vector network analyzer. *See VNA (vector network analyzer)*

vendor-supplied S-parameter models, 251–258

$V(f)$ , 70

$V_i$ , 73

V/I definition of impedance, measurements based on,

vias. *See also* spreading inductance

inductance of, 109–114

power ground planes with multiple via pair contacts,  
460–465

shorting vias, 372–383

$V_{\text{incident}}$ , 79, 96

$V_j$ , 57

VNA (vector network analyzer)

definition of, 76

impedance measurement with, 76–80

impedance of small wire loop, 86–89

impedance of two leads in DIP, 81–85

limitations of measurements at low frequency,  
89–93

$V_{\text{noise}}$ , 8, 394

voltage, definition of, 139

voltage droop, 432

voltage noise. *See also* capacitance; impedance

clock edge current

capacitance referenced to both Vss and Vdd rails,  
558–562

as cause of PDN noise, 565–572

clock edge noise, 431, 661–664

example of, 557–558

impulses from SCL (Switched Capacitor Load),  
613–622

measurement example: embedded controller  
processor, 562–565

waveforms composed of series of clock impulses,  
622–629

current through ideal capacitor, 19

peak impedance, 364–367, 595–602

peak-to-peak voltage noise, [585–588, 651](#)

performance and, [3–5](#)

q-factor, [595–602](#)

reactive elements, [595–602](#)

ringing voltage noise, [54–56](#)

rogue wave effect, [602–613](#)

signal integrity design

capacitor mounting inductance, [401–403](#)

cavity losses and impedance peak reduction,  
[408–411](#)

damping, [367–371](#)

damping to suppress parallel resonant peaks,  
[403–408](#)

DC blocking capacitors to carry return current,  
[393–397](#)

DC blocking capacitors to suppress cavity  
resonance, [383–393](#)

lower impedance/higher damping, [367–371](#)

peak impedance, [364–367](#)

shorting vias, [372–383](#)

suboptimal numbers of DC capacitors, [397–401](#)

thin dielectric, [367–371](#)

transient current

calculating target impedance with, [550–553](#)

importance of, [547–549](#)

on-die PDN current draw, [553–558](#)

upper limit of, [5–7](#)

voltage regulator module. *See* [VRM \(voltage regulator  
module\)](#)

voltage stability, [222–225](#)

$V_{\text{pk-pk}}$ , [651](#)

$V_r$ , [73](#)

$V_{\text{reflected}}$ , [79, 96](#)

VRM (voltage regulator module), [225](#)

    impedance, [476–478](#)

    impedance profile of, [53–54](#)

    inductance, [478](#)

    PCB cavity, [460–465](#)

$V_{sig}$ , [394](#)

Vss rails

    clock edge current, [557–562](#)

    probing configuration for, [120](#)

    voltage noise on, [3–5](#)

$V_{total}$ , [79](#)

## W

waveforms (current), [577–579](#)

    impulse current waveform

        definition of, [577](#)

        impulses from SCL (Switched Capacitor Load),  
[613–622](#)

        PDN response to, [579–581](#)

        waveforms composed of series of clock impulses,  
[622–629](#)

    resonance current waveform

        definition of, [577](#)

        PDN response to, [585–589](#)

    rogue wave effect, [602–613](#)

    step current waveform

        definition of, [577](#)

        PDN response to, [582–584](#)

Webers, [142](#)

Weir, Steve, [448](#)

wide cavities, spreading inductance in, [292–304](#)

wide conductors, loop inductance for, [182–187](#)

Wild River Technologies, [380](#)

wire loop, measuring impedance of, [86–89](#)

working PDN design, [8–12](#)

## X

X (reactance), [20–21](#)

X2Y Attenuators, [114](#)

X2Y capacitors, [248–250](#)

## Y-Z

$Z_C$ , [205](#)

$Z_{DUT}(f)$ , [82](#)

$Z_{peak}$ , [215–220](#)

$Z_{port}$ , [340](#)

$Z_{target}$ , [8](#), [226](#), [480](#), [516](#)