

John H. Lau

# Semiconductor Advanced Packaging

# Semiconductor Advanced Packaging

John H. Lau

# Semiconductor Advanced Packaging



Springer

John H. Lau  
Unimicron Technology Corporation  
Taoyuan, Taiwan

ISBN 978-981-16-1375-3      ISBN 978-981-16-1376-0 (eBook)  
<https://doi.org/10.1007/978-981-16-1376-0>

© The Editor(s) (if applicable) and The Author(s), under exclusive license to Springer Nature Singapore Pte Ltd. 2021

This work is subject to copyright. All rights are solely and exclusively licensed by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, expressed or implied, with respect to the material contained herein or for any errors or omissions that may have been made. The publisher remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

This Springer imprint is published by the registered company Springer Nature Singapore Pte Ltd.  
The registered company address is: 152 Beach Road, #21-01/04 Gateway East, Singapore 189721,  
Singapore

# Preface

Semiconductor industry has identified five main growth engines (applications): (1) mobile such as smartphones, smartwatches, wearables, notebooks, and tablets; (2) high-performance computing (HPC), also known as supercomputing, which is able to process data and perform complex calculations at high speeds on a supercomputer; (3) autonomous vehicle (or self-driving cars); (4) IoT (Internet of things) such as smart factory and smart health; and (5) big data (for cloud computing) and instant data (for edge computing).

The packaging technologists are using various advanced packaging methods such as flip chip; W/PLCSP (wafer/panel-level chip-scale package); FOW/PLP (fan-out wafer/panel-level packaging); PoP (package-on-package); TSV (through-silicon via); 2.1D, 2.3D, 2.5D, and 3D IC integration; HBM (high bandwidth memory), multichip module; system-in-package (SiP); heterogeneous integration; chiplets; and bridges to house (package) the semiconductor devices for those five main applications.

The system-technology drivers such as 5G (5th generation technology standard for broadband cellular networks) and AI (artificial intelligence which is defined as any technique that enables computers to mimic human intelligence) are boosting the growths of these five semiconductor applications. Because of the drive of 5G and AI, the semiconductors' speed increases, density increases, pad-pitch decreases, chip-size increases, and power dissipation increases. All these provide challenges (opportunities) to semiconductor advanced packaging.

Unfortunately, for most of the practicing engineers and managers, as well as scientists and researchers, these advanced packaging methods are not well understood. Thus, there is an urgent need, both in industry and research institute, to create a comprehensive book on the current state of knowledge of these advanced packaging technologies. This book is written so that readers can quickly learn about the basics of problem-solving methods and understand the trade-offs inherent in making system-level decisions.

There are 11 chapters in this book, namely: (1) advanced packaging; (2) system-in-package; (3) fan-in wafer/panel-level chip-scale packages; (4) fan-out wafer/panel-level packaging; (5) 2D, 2.1D, and 2.3D IC integration; (6) 2.5D IC integration; (7) 3D

IC integration and 3D IC packaging; (8) hybrid bonding; (9) chiplets heterogeneous integration; (10) low loss dielectric materials; and (11) advanced packaging trends.

Chapter 1 simply defines semiconductor advanced packaging and lists 16 different kinds of advanced packaging. One example of each kind is given. The relations between drivers, semiconductor, and packaging will also be briefly mentioned.

Chapter 2 presents the system-in-package (SiP) technology and its assembly processes such as SMT (surface mount technology) and flip chip technology. The difference between the SoC (system-on-chip) and SiP will be briefly mentioned first.

Chapter 3 details the fan-in wafer/panel-level chip-scale packages. There are four parts: (1) fan-in wafer-level chip-scale packages, (2) fan-in panel-level chip-scale packages, (3) six-side molded wafer-level chip-scale packages, and (4) six-side molded panel-level chip-scale packages.

Chapter 4 presents the fan-out wafer/panel-level packaging. There are six parts: (1) fan-out (chip-first and face-down) wafer-level packaging, (2) fan-out (chip-first and face-down) panel-level packaging, (3) fan-out (chip-first and face-up) wafer-level packaging, (4) fan-out (chip-first and face-up) panel-level packaging, (5) fan-out (chip-last or RDL-first) wafer-level packaging, and (6) fan-out (chip-last or RDL-first) panel-level packaging.

Chapter 5 simply defines the 2D, 2.1D, and 2.3D IC integration. Examples for each kind of IC integration will be given. Redistribution layers (RDLs) such as organic RDLs, inorganic RDLs, and hybrid RDLs will be briefly mentioned.

Chapter 6 simply defines the 2.5D IC integration or passive TSV-interposer and presents many examples. The recent developments of 2.5D IC integration will also be briefly presented. The origin of 2.5D IC integration will be briefly mentioned first.

Chapter 7 presents the 3D IC integration which includes the 3D IC packaging (without TSVs) and 3D IC integration (with TSVs) or active TSV-interposer. There are many examples. HBM (high bandwidth memory) will also be briefly mentioned.

Chapter 8 discusses the hybrid bonding. Cu-Cu TCB (thermocompression bonding),  $\text{SiO}_2$ - $\text{SiO}_2$  TCB, and room-temperature Cu-Cu TCB will also be presented. Some new developments in hybrid bonding will be briefly mentioned.

Chapter 9 simply defines the chiplets heterogeneous integration, and its advantages and disadvantages will also be briefly presented. DARPA's COSMOS, DAHI, CHIPS, and SHIP programs will be briefly mentioned.

Chapter 10 systematically presents the dielectric material properties of Df and Dk for high speed and frequency applications in the literatures of last three years. Why need low Df and Dk and low coefficient of thermal expansion dielectric materials for 5G applications are briefly mentioned first.

Chapter 11 presents the trends in advanced packaging and their assembly processes. The trends in SoC (system-on-chip) and chiplets will be provided. The impact of COVID-19 on the semiconductor industry will be briefly mentioned first.

For whom is this book intended? Undoubtedly, it will be of great interest to three groups of specialists: (1) those who are active or intend to become active in research and development of advanced packaging such as 2D fan-out (chip-first) IC integration, 2D flip chip IC integration, PoP (package-on-package), SiP (system-in-package) or heterogeneous integration, 2D fan-out (chip-last) IC integration, 2.1D

flip chip IC integration, 2.1D flip chip IC integration with bridges, 2.1D fan-out IC integration with bridges, 2.3D fan-out (chip-first) IC integration, 2.3D flip chip IC integration, 2.3D fan-out (chip-last) IC integration, 2.5D (solder bump) IC integration, 2.5D ( $\mu$ bump) IC integration,  $\mu$ bump 3D IC integration,  $\mu$ bump chiplets 3D IC integration, bumpless 3D IC integration, and bumpless chiplets 3D IC integration; (2) those who have encountered practical advanced packaging problems and wish to understand and learn more methods for solving such problems; and (3) those who have to choose a reliable, creative, high-performance, high-density, low power consumption, and cost-effective advanced packaging technique for their products. This book can also be used as a text for college and graduate students who have the potential to become our future leaders, scientists, and engineers in the electronics and optoelectronics industry.

I hope that this book will serve as a valuable reference source for all those faced with the challenging problems created by the ever-increasing interest in advanced packaging. I also hope that it will aid in stimulating further research and development on key enabling technologies and more sound applications to advanced packaging products. The organizations that learn how to design and manufacture advanced packaging in their semiconductor packaging systems have the potential to make major advances in the electronics and optoelectronics industry and to gain great benefits in performance, functionality, density, power, bandwidth, quality, size, and weight. It is my hope that the information presented in this book may assist in removing roadblocks, avoiding unnecessary false starts, and accelerating the design, materials, process, and manufacturing development of advanced packaging.

Palo Alto, CA, USA

John H. Lau

# Acknowledgments

Development and preparation of Semiconductor Advanced Packaging was facilitated by the efforts of a number of dedicated people. I would like to thank them all, with special mention of Kokila Durairaj, Springer Nature Scientific Publishing Services (P) Ltd., for their unswerving support and advocacy. My special thanks go to Ms. Jasmine Dou, Springer Singapore, who made my dream of this book come true by effectively sponsoring the project and solving many problems that arose during the book's preparation. It has been a great pleasure and fruitful experience to work with all of them in transferring my messy manuscripts into a very attractive printed book.

The material in this book clearly has been derived from many sources, including individuals, companies, and organizations, and I have attempted to acknowledge by citations in the appropriate parts of the book the assistance that I have been given. It would be quite impossible for me to express my thanks to everyone concerned for their cooperation in producing this book, but I would like to extend due gratitude. Also, I would like to thank several professional societies and publishers for permitting me to reproduce some of their illustrations and information in this book, including the American Society of Mechanical Engineers (ASME) conference proceedings (e.g., International Intersociety Electronic Packaging Conference) and transactions (e.g., Journal of Electronic Packaging), the Institute of Electrical and Electronic Engineers (IEEE) conference proceedings (e.g., Electronic Components and Technology Conference and Electronics Packaging and Technology Conference) and transactions (e.g., Components, Packaging, and Manufacturing Technologies), and the International Microelectronics and Packaging Society (IMAPS) conference proceedings (e.g., International Symposium on Microelectronics), and transactions (e.g., International Journal of Microcircuits and Electronic Packaging).

I would like to thank my former employers, ASM (HK), Industrial Technology Research Institute (ITRI), the Hong Kong University of Science and Technology (HKUST), the Institute of Microelectronics (IME), Agilent, and HP, for providing me with excellent working environments that have nurtured me as a human being, fulfilled my need for job satisfaction, and enhanced my professional reputation. Also, I would like to thank Dr. Don Rice (HP), Dr. Steve Erasmus (Agilent), Prof. Dim-Lee Kwong (IME), Prof. Ricky Lee (HKUST), Dr. Ian Yi-Jen Chan (ITRI), and Mr. Lee Wai Kwong (ASM) for their kindness and friendship while I was at their

organizations. Furthermore, I would like to thank Mr. Tzvy-Jang Tseng (Chairman of Unimicron Technology Corporation) for his trust, respect, and support of my work at Unimicron. Finally, I would like to thank the following colleagues for their stimulating discussions and significant contributions to this book: N. Khan, V. Rao, D. Ho, V. Lee, X. Zhang, T. Chai, V. Kripesh, C. Lee, C. Zhan, P. Tzeng, M. Dai, H. Chien, S. Wu, R. Lo, M. Kao, L. Li, Y. Chao, R. Tain, C. Premachandran, A. Yu, C. Selvanayagam, D. Pinjala, C. Ko, M. Li, Q. Li, R. Beica, I. Xu, T. Chan, K. Tan, E. Kuah, Y. Cheung, X. Cao, J. Ran, H. Yang, N. Lee, S. Lim, N. Fan, M. Tao, J. Lo, R. Lee, X. Qing, Z. Cheng, Y. Lei, Z. Li, Y. Chen, M. Lin, V. Sekhar, A. Kumar, P. Lim, X. Ling, T. Lim, P. Ramana, L. Lim, C. Teo, W. Liang, J. Chai, M. Zhang, C. Ko, C. Peng, T. Tseng, K. Yang, T. Xia, P. Lin, E. Lin, L. Chang, H. Liu, C. Lin, Y. Fan, D. Cheng, W. Lu, G. Chen, J. Huang, R. Chou, G. Chen, J. Huang, R. Chou, C. Yang, and W. Choi. Definitely, I would like to thank my eminent colleagues (the enumeration of whom would not be practical here) at Unimicron, ASM, ITRI, HKUST, IME, Agilent, EPS, HP, and throughout the electronics industry for their useful help, strong support, and stimulating discussions. Working and socializing with them has been a privilege and an adventure. I learned a lot about life and semiconductor advanced packaging from them.

Lastly, I would like to thank my daughter Judy and my wife Teresa for their love, consideration, and patience by allowing me to work peacefully on this book. Their simple belief that I am making a contribution to the electronics industry was a strong motivation for me. Thinking that Judy and her supportive husband (Bill) have been doing very well in a semiconductor company and their two lovely kids (Allison and James) have been raising in a happy environment, and Teresa and I are in good health, I want to thank God for His generous blessings.

Palo Alto, CA, USA

John H. Lau

# Contents

<b>1</b>	<b>Advanced Packaging .....</b>	<b>1</b>
1.1	Introduction .....	1
1.2	Semiconductor Applications .....	1
1.3	System-Technology Drivers .....	1
1.3.1	AI .....	2
1.3.2	5G .....	2
1.4	Advanced Packaging .....	4
1.4.1	Kinds of Advanced Packaging .....	4
1.4.2	Groups of Advanced Packaging .....	4
1.5	2D Fan-Out (Chip-First) IC Integration .....	5
1.6	2D Flip Chip IC Integration .....	7
1.7	PoP, SiP, and Heterogeneous Integration .....	7
1.8	2D Fan-Out (Chip-Last) IC Integration .....	9
1.9	2.1D Flip Chip IC Integration .....	9
1.10	2.1D Flip Chip IC Integration with Bridges .....	11
1.11	2.1D Fan-Out IC Integration with Bridges .....	11
1.12	2.3D Fan-Out (Chip-First) IC Integration .....	12
1.13	2.3D Flip Chip IC Integration .....	12
1.14	2.3D Fan-Out (Chip-Last) IC Integration .....	13
1.15	2.5D (C4 Bump) IC Integration .....	13
1.16	2.5D (C2 Bump) IC Integration .....	14
1.17	$\mu$ Bump 3D IC Integration .....	14
1.18	$\mu$ Bump Chiplets 3D IC Integration .....	15
1.19	Bumpless 3D IC Integration .....	15
1.20	Bumpless Chiplets 3D IC Integration .....	17
1.21	Summary and Recommendation .....	18
	References .....	19
<b>2</b>	<b>System-in-Package (SiP) .....</b>	<b>27</b>
2.1	Introduction .....	27
2.2	SoC (System-on-Chip) .....	27
2.3	System-in-Package (SiP) .....	29

2.4	Intention of SiP .....	29
2.5	Actual Applications of SiP .....	29
2.6	SiP Examples .....	29
2.7	SMT .....	32
2.7.1	PCB .....	32
2.7.2	SMDs .....	35
2.7.3	Solder Paste .....	35
2.7.4	Stencil Printing Solder Paste and AOI .....	37
2.7.5	Pick and Place of SMDs .....	40
2.7.6	AOI of SMDs on PCB .....	40
2.7.7	SMT Solder Reflow .....	40
2.7.8	AOI and X-Ray Inspection for Defects .....	42
2.7.9	Re-Work .....	42
2.7.10	Summary and Recommendation .....	43
2.8	Flip Chip Technology .....	45
2.8.1	Wafer Bumping by Stencil Printing .....	46
2.8.2	C4 (Controlled Collapse Chip Connection) Wafer Bumping .....	48
2.8.3	C2 (Chip Connection) Wafer Bumping .....	49
2.8.4	Flip Chip Assembly—Mass Reflow of C4 or C2 Bumps (CUF) .....	50
2.8.5	Underfill for Reliability .....	51
2.8.6	Flip Chip Assembly—TCB with Low-Force of C4 or C2 Bumps (CUF) .....	54
2.8.7	Flip Chip Assembly—TCB with High-Force of C2 Bumps (NCP) .....	55
2.8.8	Flip Chip Assembly—TCB with High-Force of C2 Bumps (NCF) .....	56
2.8.9	An Advanced Flip Chip Assembly—LPC TCB of C2 Bumps .....	56
2.8.10	Summary and Recommendation .....	65
	References .....	66
<b>3</b>	<b>Fan-In Wafer/Panel-Level Chip-Scale Packages .....</b>	<b>75</b>
3.1	Introduction .....	75
3.2	Fan-In Wafer-Level Chip-Scale Packages (WLCSPs) .....	78
3.2.1	The Structure .....	78
3.2.2	WLCSP Key Process Steps .....	79
3.2.3	PCB Assembly of WLCSP .....	81
3.2.4	Thermal Simulation of the WLCSP PCB Assembly .....	81
3.2.5	Summary and Recommendation .....	88
3.3	Fan-In Panel-Level Chip-Scale Packages (PLCSPs) .....	88
3.3.1	Test Chip .....	89
3.3.2	Test Package .....	90

Contents	xiii	
3.3.3	PLCSP Process Flow .....	92
3.3.4	PCB Assembly of the PLCSP .....	98
3.3.5	Drop Test of PLCSP PCB Assembly .....	100
3.3.6	Thermal Cycling Test of PLCSP PCB Assembly .....	101
3.3.7	Thermal Cycling Simulation of the PLCSP PCB Assembly .....	109
3.3.8	Summary and Recommendation .....	114
3.4	<b>Six-Side Molded Wafer-Level Chip-Scale Packages .....</b>	115
3.4.1	eWLCSP by Statschippac .....	116
3.4.2	WLCSP by UTAC .....	117
3.4.3	mWLCSP by SPL .....	117
3.4.4	WLCSP by Huatian .....	118
3.4.5	mWLCSP by SPL and MediaTek .....	118
3.4.6	Summary and Recommendation .....	120
3.5	<b>Six-Side Molded Panel-Level Chip-Scale Packages .....</b>	120
3.5.1	The 6-Side Molded PLCSP Structure .....	121
3.5.2	Cutting and EMC Molding of Wafer from the Front-Side .....	122
3.5.3	Backgrinding and Wafer Backside Molding .....	123
3.5.4	Plasma Etching and Dicing .....	123
3.5.5	Test PCB .....	124
3.5.6	SMT Assembly of the 6-Side Molded PLCSP on PCB .....	126
3.5.7	Thermal Cycling Test of the 6-Side Molded PLCSP .....	126
3.5.8	Thermal Cycling Simulation of the 6-Side Molded PLCSP PCB Assembly .....	133
3.5.9	Summary and Recommendation .....	137
	<b>References .....</b>	138

<b>4</b>	<b>Fan-Out Wafer/Panel-Level Packaging .....</b>	147
4.1	Introduction .....	147
4.2	<b>Fan-Out (Chip-First and Face-Down) Wafer-Level Packaging (FOWLP) .....</b>	147
4.2.1	Test Chips .....	149
4.2.2	Test Package .....	149
4.2.3	Conventional Chip-First (Face-Down) Wafer Process .....	150
4.2.4	New Process for Heterogeneous Integration Package .....	152
4.2.5	Dry-Film EMC Lamination .....	153
4.2.6	Temporary Bonding Another Glass Carrier .....	153
4.2.7	RDLs .....	154
4.2.8	Solder Ball Mounting .....	156
4.2.9	Final De-Bonding .....	156

4.2.10	PCB Assembly .....	158
4.2.11	Reliability (Drop Test) of the Heterogeneous Integration .....	160
4.2.12	Summary and Recommendation .....	163
4.3	Fan-Out (Chip-First and Face-Down) Panel-Level Packaging (FOPLP) .....	163
4.3.1	Heterogeneous Integration of Test Package .....	164
4.3.2	A New Uni-SIP Process .....	165
4.3.3	Dry-Film Lamination of ECM-Panel .....	166
4.3.4	Lamination of Uni-SIP Structure .....	168
4.3.5	Lamination of the New ABF, Laser Drilling, and De-Smearing .....	168
4.3.6	LDI and PCB Cu-Plating .....	171
4.3.7	Summary and Recommendation .....	172
4.4	Fan-Out (Chip-First and Face-Up) Wafer-Level Packaging .....	173
4.4.1	Test Chip .....	173
4.4.2	Process Flow .....	174
4.5	Fan-Out (Chip-First and Face-up) Panel-Level Packaging .....	175
4.5.1	The Structure .....	175
4.5.2	Process Flow .....	175
4.6	Fan-Out (Chip-Last or RDL-First) Wafer-Level Packaging .....	176
4.6.1	IME's RDL-First FOWLP .....	179
4.6.2	Test Structure .....	180
4.6.3	RDL-First Key Process Steps .....	180
4.6.4	RDL-First FOWLP on PCB Assembly .....	181
4.7	Fan-Out (Chip-Last or RDL-First) Panel-Level Packaging .....	182
4.7.1	Test Chips .....	182
4.7.2	Test Package .....	184
4.7.3	RDL-First Panel-Level Packaging for Heterogeneous Integration .....	185
4.7.4	Fabrication of Redistribution-Layer Substrate .....	185
4.7.5	Wafer Bumping .....	189
4.7.6	Chip-to-Substrate Bonding .....	190
4.7.7	Underfilling and EMC Molding .....	191
4.7.8	Panel/Strip Transfer .....	192
4.7.9	Solder Resist Opening and Surface Finishing .....	193
4.7.10	Solder Ball Mounting, Debonding, and Strip Dicing .....	195
4.7.11	PCB Assembly of the RDL-First Panel-Level Package .....	195
4.7.12	Drop Test Results and Failure Analysis .....	197
4.7.13	Thermal-Cycling Test Results and Failure Analysis .....	198
4.7.14	Thermal-Cycling Simulation .....	207
4.7.15	Summary and Recommendation .....	209

4.8	Fan-Out Panel-Level Packaging of Mini-LED RGB Display .....	209
4.8.1	Test Mini—LEDS .....	211
4.8.2	Test Mini-LED RGB Display SMD Package .....	212
4.8.3	RDL and Mini-LED RGB SMD Fabrication .....	214
4.8.4	PCB Assembly .....	217
4.8.5	Drop Test .....	221
4.8.6	Thermal Cycling Simulation .....	222
4.8.7	Summary and Recommendation .....	227
	References .....	229
5	<b>2D, 2.1D, and 2.3D IC Integration .....</b>	239
5.1	Introduction .....	239
5.2	2D IC Integration—Wire Bonging .....	239
5.3	2D IC Integration—Flip Chip .....	239
5.4	2D IC Integration—Wire Bonging and Flip Chip .....	240
5.5	RDLs .....	241
5.5.1	Organic RDLs .....	242
5.5.2	Inorganic RDLs .....	242
5.5.3	Hybrid RDLs .....	242
5.6	2D IC Integration—Fan-Out (Chip-First) .....	242
5.6.1	HTC's Desire 606 W .....	243
5.6.2	Heterogeneous Integration of 4 Chips .....	243
5.7	2D IC Integration—Fan-Out (Chip-Last) .....	245
5.7.1	IME's Fan-Out with Chip-Last .....	245
5.7.2	Amkor's SWIFT .....	246
5.7.3	Amkor's SLIM .....	246
5.7.4	SPIL's Fan-Out on Hybrid RDLs .....	248
5.7.5	Unimicron's Fan-Out with Chip-Last .....	249
5.8	2.1D IC Integration .....	249
5.8.1	Shinko's I-THOP .....	251
5.8.2	Hitachi's 2.1D Organic Interposer .....	253
5.8.3	ASE's 2.1D Organic Interposer .....	254
5.8.4	SPIL's 2.1D Organic Interposer .....	254
5.8.5	JCET's UFOS .....	255
5.8.6	Intel's EMIB .....	255
5.8.7	Applied Materials' Bridge .....	256
5.8.8	TSMC'S LSI .....	257
5.9	2.3D IC Integration .....	257
5.10	2.3D IC Integration with SAP/PCB Method .....	259
5.10.1	Shinko's Coreless Organic Interposer .....	260
5.10.2	Cisco's Organic Interposer .....	262
5.11	2.3D IC Integration with Fan-Out (Chip-First) Method .....	263
5.11.1	Statschippac's 2.3D eWLB .....	263
5.11.2	Mediatek's Fan-Out (Chip-First) .....	265

5.11.3	ASE's FOCoS (Chip-First) .....	266
5.11.4	TSMC's InFO_OS and InFO_MS .....	266
5.12	2.3D IC Integration with Fan-Out (Chip-Last) Method .....	268
5.12.1	SPIL'S NTI .....	268
5.12.2	Samsung's Si-Less RDL Interposer .....	269
5.12.3	ASE's FOCoS (Chip-Last) .....	271
5.12.4	TSMC's Multilayer RDL Interposer .....	273
5.12.5	Shinko's 2.3D Organic Interposer .....	273
5.12.6	Unimicron's 2.3D RDL-Interposer .....	276
5.13	Summary and Recommendation .....	294
	References .....	295
<b>6</b>	<b>2.5D IC Integration .....</b>	<b>299</b>
6.1	Introduction .....	299
6.2	Leti's SoW (the Origin of 2.5D IC Integration) .....	299
6.3	IME's 2.5D IC Integration .....	299
6.3.1	3D Nonlinear Local and Global Analysis of 2.5D IC Integration .....	300
6.3.2	2.5D IC Integration for Electrical and Fluidic Interconnects .....	303
6.3.3	Double Stacked Passive TSV-Interposers .....	305
6.3.4	TSV-Interposer Used as Stress (Reliability) Buffer .....	306
6.4	HKUST's TSV-Interposer with Chips on Both Sides .....	308
6.5	ITRI's 2.5D IC Integration .....	308
6.5.1	Thermal Management of TSV-Interposer with Chips on Both Sides .....	308
6.5.2	TSV-Interposer with Embedded Fluidic Microchannels for LEDs .....	311
6.5.3	TSV-Interposer with SoCs and Memory Cube .....	313
6.5.4	Semi-embedded TSV-Interposer .....	315
6.5.5	TSV-Interposer with Double-Sided Chip Attachments .....	315
6.5.6	TSV-Interposer with Chips on Both Sides .....	317
6.5.7	Through-Silicon Hole-Interposer (TSH-Interposer) .....	318
6.6	TSMC's CoWoS .....	320
6.7	Xilinx/TSMC's 2.5D IC Integration .....	322
6.8	Altera/TSMC's 2.5D IC Integration .....	326
6.9	AMD/UMC's 2.5D IC Integration .....	326
6.10	NVidia/TSMC's 2.5D IC Integration .....	328
6.11	TSMC's CoWoS Roadmap .....	329
6.12	Recent Advances in 2.5D IC Integration .....	329
6.12.1	TSMC's CoWoS with Deep Trench Capacitor (DTC) .....	330

6.12.2	IME's Non-destructive Fault Isolation in 2.5D IC Integration .....	331
6.12.3	Fraunhofer's Photonics Interposer .....	332
6.12.4	Dai Nippon/AGC's Glass Interposer .....	333
6.12.5	Fujitsu's Multilayer Glass Interposer .....	334
6.13	Summary and Recommendation .....	334
	References .....	336
<b>7</b>	<b>3D IC Integration and 3D IC Packaging .....</b>	<b>343</b>
7.1	Introduction .....	343
7.2	3D IC Packaging .....	343
7.2.1	3D IC Packaging—Memory Stack with Wire Bonding .....	344
7.2.2	3D IC Packaging—Face-to-Face Bonding with Wire Bonding to Substrate .....	344
7.2.3	3D IC Packaging—Back-to-Back Bonding with Wire Bonding to Substrate .....	346
7.2.4	3D IC Packaging—Face-to-Face Bonding with Solder Bump/Ball to Substrate .....	346
7.2.5	3D IC Packaging—Face-to-Back .....	352
7.2.6	3D IC Packaging—Embedded Chip (Face-to-Face) in SiP .....	355
7.2.7	3D IC Packaging—PoP with Flip-Chip Technology .....	356
7.2.8	3D IC Packaging—PoP with Fan-Out Technology .....	357
7.2.9	Summary and Recommendation .....	360
7.3	3D IC Integration .....	362
7.3.1	3D IC Integration—HBM Specifications .....	362
7.3.2	3D IC Integration—HBM Assembly .....	364
7.3.3	3D IC Integration—Chip-on-Chip with TSVs .....	365
7.3.4	3D IC Integration—Bumpless Hybrid Bonding of Chip-on-Chip with TSVs .....	368
7.3.5	3D IC Integration—Bumpless Hybrid Bonding of Chip-on-Chip Without TSVs .....	369
7.3.6	Summary and Recommendation .....	371
	References .....	375
<b>8</b>	<b>Hybrid Bonding .....</b>	<b>379</b>
8.1	Introduction .....	379
8.2	Cu–Cu TCB .....	380
8.2.1	Some Fundamental on Cu–Cu TCB .....	380
8.2.2	IBM/RPI's Cu–Cu TCB .....	381
8.3	Cu–Cu TCB at Room Temperature .....	383
8.3.1	Some Fundamental on Cu–Cu TCB at Room Temperature .....	383

8.3.2	NIMS/AIST/Toshiba/University of Tokyo's Cu–Cu TCB at Room Temperature .....	383
8.4	<b>SiO<sub>2</sub>–SiO<sub>2</sub> TCB .....</b>	384
8.4.1	Some Fundamental on SiO <sub>2</sub> –SiO <sub>2</sub> TCB .....	384
8.4.2	MIT's SiO <sub>2</sub> –SiO <sub>2</sub> TCB .....	385
8.4.3	Leti/Freescale/STMicroelectronics' SiO <sub>2</sub> –SiO <sub>2</sub> TCB .....	387
8.5	<b>Low Temperature DBI .....</b>	387
8.5.1	Some Fundamental on Low Temperature DBI .....	387
8.5.2	Sony's CMOS Image Sensors (CIS) with TSVs .....	390
8.5.3	Sony's CIS Without TSV (Hybrid Bonding) .....	391
8.6	<b>Recent Developments of Low Temperature Hybrid Bonding .....</b>	394
8.6.1	IME's Thermo-Mechanical Performance of Hybrid Bonding .....	394
8.6.2	TSMC's Hybrid Bonding .....	399
8.6.3	IMEC's Hybrid Bonding .....	400
8.6.4	Globalfoundries' Hybrid Bonding .....	402
8.6.5	Mitsubishi's Hybrid Bonding .....	404
8.6.6	Leti's Hybrid Bonding .....	404
8.6.7	Intel's Hybrid Bonding .....	406
8.7	<b>Summary and Recommendation .....</b>	407
	<b>References .....</b>	408
<b>9</b>	<b>Chiplet Heterogeneous Integration .....</b>	413
9.1	Introduction .....	413
9.2	DARPA's Efforts in Chiplet Heterogeneous Integration .....	413
9.3	SoC (System-on-Chip) .....	414
9.4	Chiplet Heterogeneous Integration .....	416
9.5	Advantages and Disadvantages of Chiplet Heterogeneous Integration .....	417
9.6	<b>Advanced Packaging for Chiplet Heterogeneous Integration .....</b>	418
9.6.1	2D Chiplet Heterogeneous Integration on Organic Substrate .....	418
9.6.2	2.1D Chiplet Heterogeneous Integration on Organic Substrate .....	419
9.6.3	2.3D Chiplet Heterogeneous Integration on Organic Substrate .....	420
9.6.4	2.5D Chiplet Heterogeneous Integration on Silicon Substrate (Passive TSV-Interposer) .....	421
9.6.5	3D Chiplet Heterogeneous Integration on Silicon Substrate (Active TSV-Interposer) .....	423
9.6.6	Chiplet Heterogeneous Integration on Organic Substrate with Silicon Bridges .....	423

9.6.7	PoP Chiplet Heterogeneous Integration .....	424
9.6.8	Chiplet Heterogeneous Integration on Fan-Out RDL-Substrate .....	425
9.7	AMD's Chiplet Heterogeneous Integration .....	427
9.8	Intel's Chiplet Heterogeneous Integration .....	429
9.9	TSMC's Chiplet Heterogeneous Integration .....	431
9.10	Summary and Recommendation .....	434
	References .....	436
<b>10</b>	<b>Low Loss Dielectric Materials .....</b>	<b>441</b>
10.1	Introduction .....	441
10.2	Why Need Low Dk and Df Dielectric Materials? .....	442
10.3	Why Need Low CTE Dielectric Materials? .....	442
10.4	NAMICS's Dk and Df .....	443
10.5	Arakawa's Dk and Df .....	445
10.6	DuPont's Dk and Df .....	446
10.7	Hitachi/DuPont MicroSystems' Dk and Df .....	447
10.8	JSR's Dk and Df .....	448
10.9	Toray's Dk and Df .....	452
10.10	Fujitsu's Dk and Df .....	452
10.11	Kayaku's Dk and Df .....	453
10.12	Mitsubishi's Dk and Df .....	456
10.13	TAITO INK's Dk and Df .....	457
10.14	Zhejiang University's Dk and Df .....	460
10.15	Summary and Recommendation .....	461
	References .....	463
<b>11</b>	<b>Advanced Packaging Trends .....</b>	<b>465</b>
11.1	Introduction .....	465
11.2	The Impact of COVID-19 on Semiconductor Industry .....	465
11.3	The Impact of COVID-19 on Foundry Industry .....	466
11.4	The Impact of COVID-19 on the Semiconductor Customers .....	466
11.5	The Impact of COVID-19 on Packaging Industry .....	468
11.6	Drivers, Semiconductor, and Advanced Packaging .....	469
11.7	Assembly Process for Advanced Packaging .....	470
11.7.1	Wire Bonding .....	472
11.7.2	SMT .....	473
11.7.3	Wafer Bumping for Flip Chip Technology .....	473
11.7.4	Flip Chip on Organic Substrates .....	474
11.7.5	CoC, CoW, and WoW TCB and Hybrid Bonding .....	475
11.8	Fan-Out Chip-First (Face-up), Chip-First (Face-Down), and Chip-Last .....	477
11.9	Bridges Versus TSV-Interposer .....	478
11.10	SoC Versus Chiplets .....	481
11.11	Material Requirement for HS/HF Applications .....	486

11.12 Summary and Recommendation .....	487
References .....	488
<b>Index .....</b>	<b>491</b>

# About the Author

**John H. Lau, Ph.D., P.E.** has been the CTO of Unimicron in Taiwan since August 2019. Prior to that, he was a Senior Technical Advisor at ASM Pacific Technology in Hong Kong for 5 years; a specialist of the Industrial Technology Research Institute in Taiwan for 4½ years; a Visiting Professor at Hong Kong University of Science and Technology for 1 year; the Director of the Microsystems, Modules, and Components Laboratory at the Institute of Microelectronics in Singapore for 2 years; and a Senior Scientist/MTS at Hewlett-Packard Laboratory/Agilent in California for more than 25 years.

His professional competences are design, analysis, materials, process, manufacturing, qualification, reliability, testing, and thermal management of electronic, opto-electronic, LED, CIS, and MEMS components and systems, with emphases on solder mechanics and manufacturing, RoHS-compliant products, SMT, flip chip, fan-in and fan-out wafer/panel-level packaging, SiP, heterogeneous chiplets integration, TSV, and other enabling technologies for 3D IC integration.

With more than 40 years of R&D and manufacturing experience, he has authored or coauthored more than 500 peer-reviewed technical publications, invented more than 30 issued or pending US patents, and given more than 310 lectures/workshops/keynotes worldwide. He has authored or coauthored 22 textbooks on fan-out wafer-level packaging, 3D IC heterogeneous integration and packaging, TSV for 3D integration, advanced MEMS packaging, reliability of 2D and 3D IC interconnects, flip chip, WLP, MCM, area-array packages, WLCSP, high-density PCB, SMT, DCA, TAB, lead-free materials, soldering, manufacturing, and solder joint reliability.

He earned a Ph.D. degree in theoretical and applied mechanics from the University of Illinois at Urbana–Champaign, an M.A.Sc. degree in structural engineering from the University of British Columbia, a second M.S. degree in engineering mechanics from the University of Wisconsin at Madison, and a third M.S. degree in management science from Fairleigh Dickinson University in New Jersey. He also has a B.E. degree in civil engineering from National Taiwan University.

He has received many awards from the American Society of Mechanical Engineers (ASME), the Institute of Electrical and Electronics Engineers (IEEE), the Society of Manufacturing Engineers (SME), and other societies, including for the best

IEEE/ECTC proceedings paper (1989); outstanding IEEE/EPTC paper (2009); best ASME transactions paper (*Journal of Electronic Packaging*, 2000); best IEEE transactions paper (CPMT, 2010); the ASME/EEP Outstanding Technical Achievement Award (1998); IEEE/CPMT Manufacturing Award (1994); IEEE/CPMT Outstanding Contribution Award (2000); IEEE/CPMT Outstanding Sustained Technical Contribution Award (2010); SME Total Excellence in Electronics Manufacturing Award (2001); Pan Wen Yuan Distinguished Research Award (2011); IEEE Meritorious Achievement in Continuing Education Award (2000); IEEE Components, Packaging, and Manufacturing Technology Field Award (2013); and ASME Worcester Reed Warner Medal (2015). He is an elected ASME Fellow, IEEE Fellow, and IMAPS Fellow, and has been heavily involved in many of ASME's, IEEE's, and IMAPS' technical activities.

# Chapter 1

## Advanced Packaging



### 1.1 Introduction

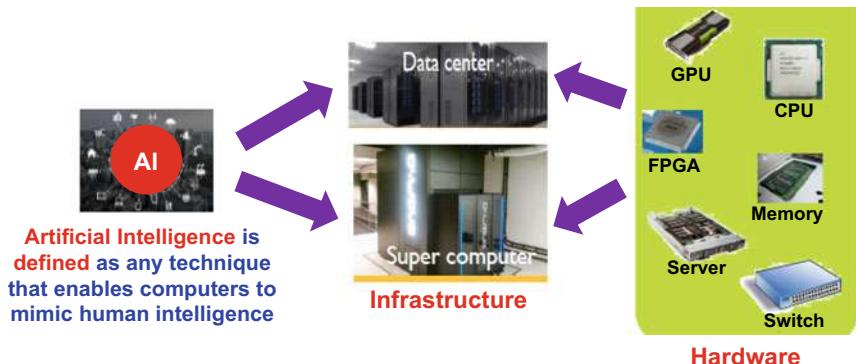
First of all, semiconductor technology is out of the scope of this book and semiconductor advanced packaging technology is the focus. In this chapter, the advanced packaging will be defined and the kinds of advanced packaging will be listed. One example of each advanced packaging will be provided. The relations between drivers, semiconductor, and packaging will be briefly mentioned.

### 1.2 Semiconductor Applications

Semiconductor industry has identified five major growth engines (applications), namely (1) mobile such as smartphones, notebooks, smartwatches, wearables, tablets, etc., (2) high-performance computing (HPC), also known as supercomputing, which is able to process data and perform complex calculations at high speeds on a supercomputer, (3) autonomous vehicle (or self-driving cars), (4) IoTs (internet of things) such as smart factory and smart health, and (5) big data (for cloud computing) and instant data (for edge computing).

### 1.3 System-Technology Drivers

There are many system-technology drivers. In this book, only AI (artificial intelligence) and 5G (5th generation technology standard for broadband cellular networks), which are boosting the growths of the 5 semiconductor applications, will be briefly mentioned.



- The Artificial intelligence (AI) is driving the semiconductor for HPC (high performance computing) application.
- AI needs HPC, whose infrastructure is data center and super computer, where the HPC is performed.
- The hardwares (semiconductor/packaging) for the infrastructure are, e.g., CPU, GPU, FPGA, memory, server, and switch.

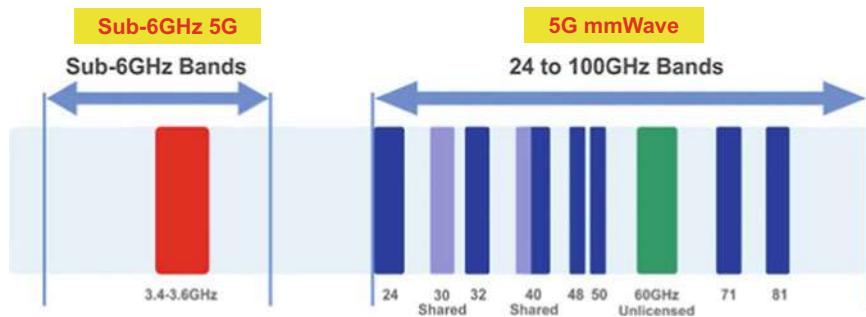
**Fig. 1.1** The relationship between AI, HPC, infrastructure, and hardware

### 1.3.1 AI

AI is defined as any technique that enables computers to mimic human intelligence. For example, AI needs HPC, whose infrastructure is data center and super computer, where the HPC is performed. The hardwares (semiconductor and packaging) for the infrastructure are, e.g., CPU (central processing unit), GPU (graphics processing unit), FPGA (field programmable gate array), memory, server, and switch as shown in Fig. 1.1.

### 1.3.2 5G

According to the US Federal Communications Commission: (a) the mid-band spectrum (also called Sub-6 GHz 5G) is defined as  $900 \text{ MHz} < \text{Frequency} < 6 \text{ GHz}$  and data speeds  $\leq 1 \text{ Gbps}$ , and (b) the high-band spectrum (also called 5G millimeter wave or 5G mmWave) is defined as  $24 \text{ GHz} \leq \text{Frequency} \leq 100 \text{ GHz}$  and  $1 \text{ Gbps} < \text{data speeds} \leq 10 \text{ Gbps}$  (Fig. 1.2). The applications of Sub-6 GHz 5G and LTE (4G) coexist with large distance between antenna and multi-mode RF transceiver. The applications of 28/39 GHz are for, e.g., the antenna of 5G mobile generation, of 60 GHz are for, e.g., high-speed wireless data link, of 77 GHz are for, e.g., automotive radar, and of 94 GHz are for, e.g., radar imaging (Fig. 1.3). In order to meet the



**(a) Mid-band spectrum: It is often referred to as Sub-6GHz 5G**

- Frequency = 2.5GHz, 3.5GHz, and 3.7GHz – 4.2GHz (< 6GHz), but > 900MHz
- Peak data speeds  $\leq$  1Gbps

**(b) High-band spectrum: It is often referred to as 5G millimeter wave (5G mmWave)**

- Frequency  $\geq$  24GHz, such as 24GHz, 28GHz, 37GHz, 47GHz, ...  $\leq$  100GHz
- Peak data speeds  $>$  1Gbps but  $\leq$  10Gbps

Fig. 1.2 US Federal Communications Commission on 5G definitions

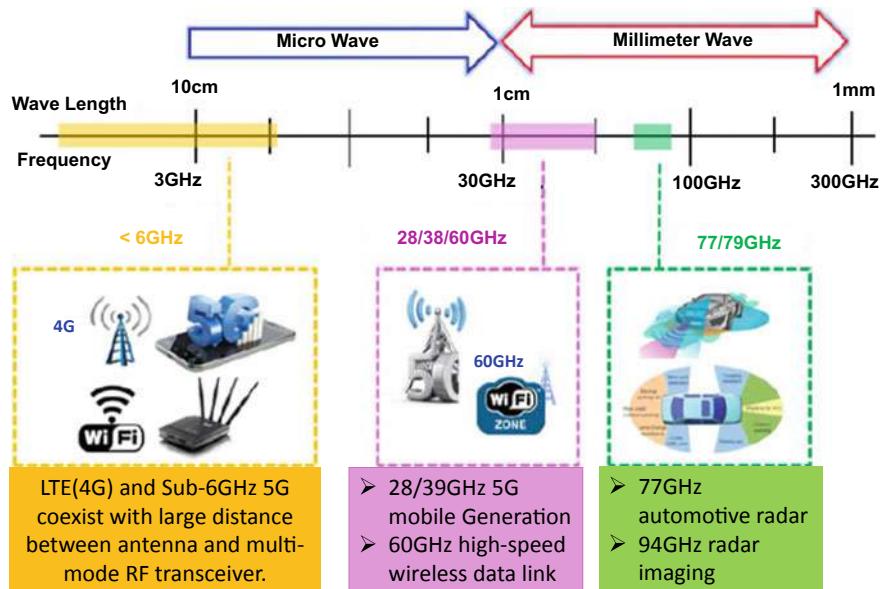


Fig. 1.3 5G applications

requirements for boosting signal transmission speed/rate and managing a huge data flood, advanced development of packaging are necessary.

## 1.4 Advanced Packaging

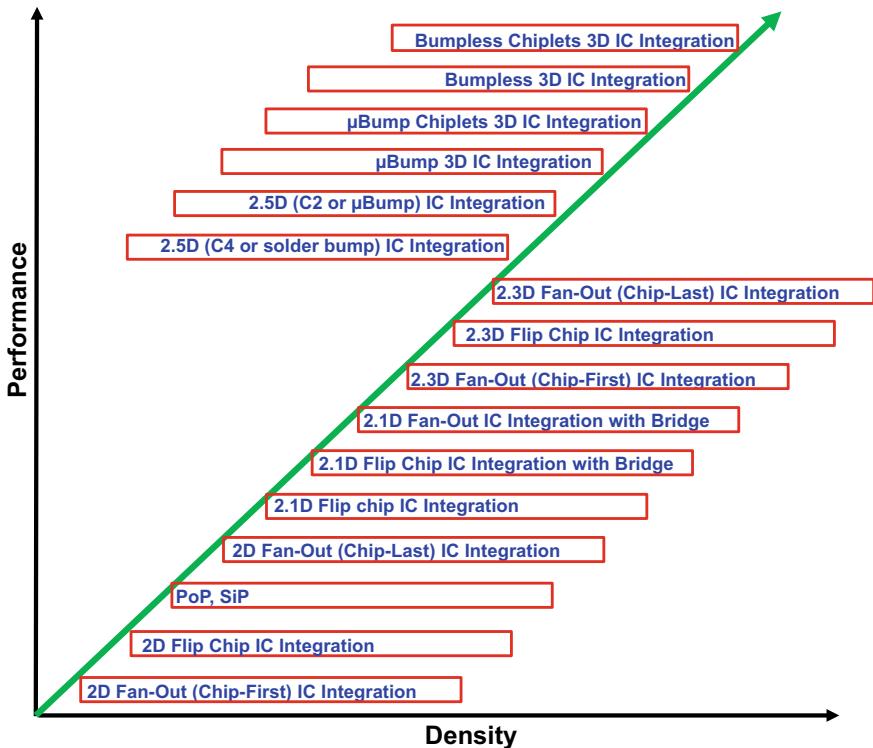
### 1.4.1 *Kinds of Advanced Packaging*

There are many advanced packaging technologies to house the semiconductors such as the 2D fan-out (chip-first) IC integration, 2D flip chip IC integration, PoP (package-on-package), SiP (system-in-package) or heterogeneous integration, 2D fan-out (chip-last) IC integration, 2.1D flip chip IC integration, 2.1D flip chip IC integration with bridges, 2.1D fan-out IC integration with bridges, 2.3D fan-out (chip-first) IC integration, 2.3D flip chip IC integration, 2.3D fan-out (chip-last) IC integration, 2.5D (solder bump) IC integration, 2.5D ( $\mu$ bump) IC integration,  $\mu$ bump 3D IC integration,  $\mu$ bump chiplets 3D IC integration, bumpless 3D IC integration, and bumpless chiplets 3D IC integration. Their performance and density ranges are shown in Fig. 1.4. Figure 1.5 shows the groups of advanced packaging.

### 1.4.2 *Groups of Advanced Packaging*

The simplest packaging method is directly attaching the semiconductor chip on a PCB (printed circuit board) such as COB (chip-on-board) or DCA (direct chip attach) [1–3]. Lead-frame packages such as PQFP (plastic quad flat pack) and SOIC (small outline integrated circuit) are ordinary packages [4]. Even PBGA (plastic ball grid array) and fcCSP (flip chip-chip scale package) for single chip are conventional packages [5]. In this book, advanced packaging is defined (at least) from the 2D IC integration with multichip on a package substrate (this is the minimum criterion). If the build-up package substrate has thin film layer on top, then it is called the 2.1D IC integration. If the build-up package substrate or the EMC (epoxy molding compound) has an embedded bridge, then it is called 2.1D IC integration with bridges. If the multichips are supported by a coreless inorganic/organic TSV-less interposer and then attached on a build-up package substrate, then it is called 2.3D IC integration. If the multichips are supported by a passive TSV-interposer and then attached on a package substrate, then it is called 2.5D IC integration. If the multichips are supported by an active TSV-interposer and then attached on a package substrate, then it is called 3D IC integration as shown in Fig. 1.5.

Throughout this book, all the advanced packaging technologies shown in Fig. 1.4 will be discussed. Assembly methods such as SMT (surface mount technology), wire bond, flip chip, and CoC (chip-on-chip), CoW (chip-on-wafer), and WoW (wafer-on-wafer) TCB (thermocompression bonding) and hybrid bonding will also

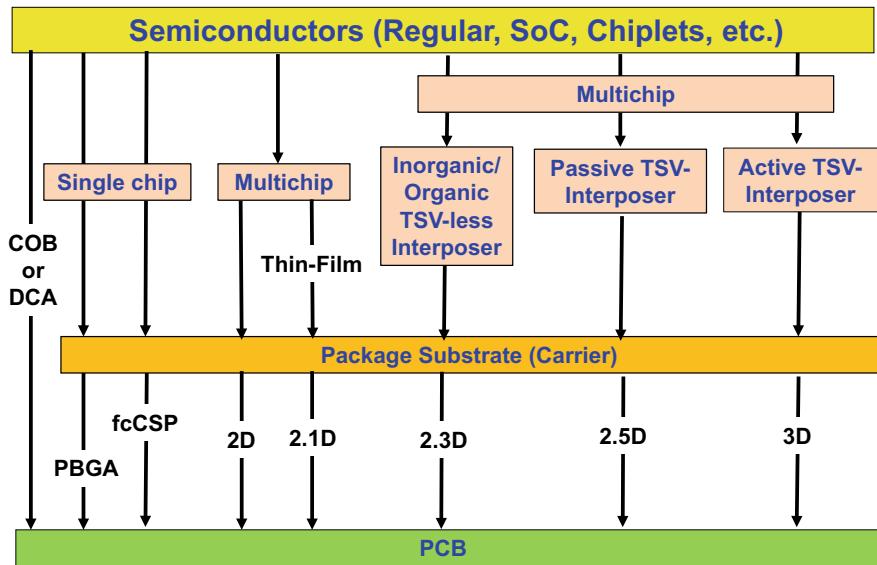


**Fig. 1.4** Density and performance ranges of advanced packaging

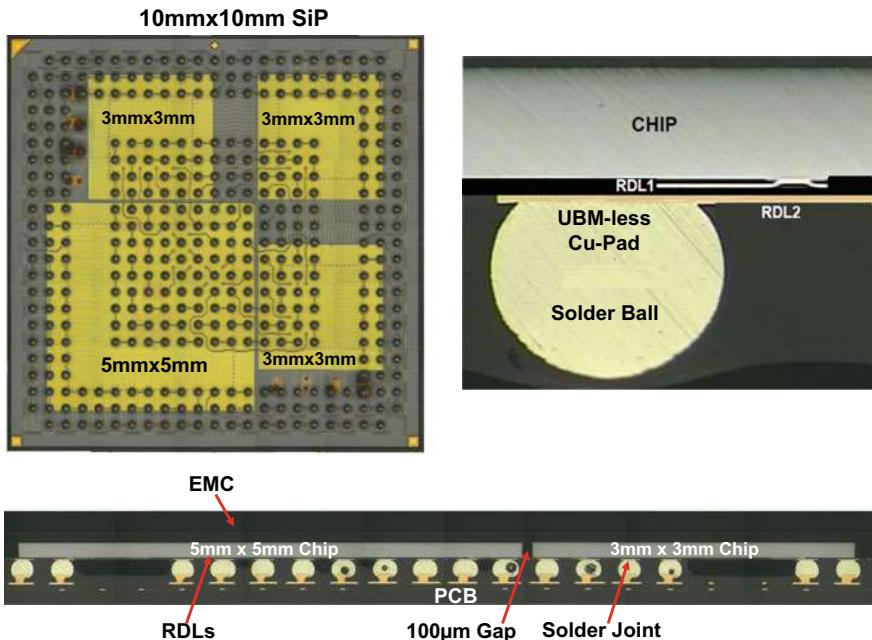
be presented. In this chapter, one example for each of the advanced packaging technologies shown in Fig. 1.4 will be briefly mentioned.

## 1.5 2D Fan-Out (Chip-First) IC Integration

Figure 1.6 shows an example [6–11] of 2D fan-out with chip-first (die face-down) IC integration [12–21]. It can be seen that there are four chips which are first embedded in an EMC (epoxy molding compound) and then fanned out with RDLs (redistribution layers), and finally connected to solder balls. These solder balls are directly attached to the PCB. For more information about fan-out packaging, please read Chap. 4.

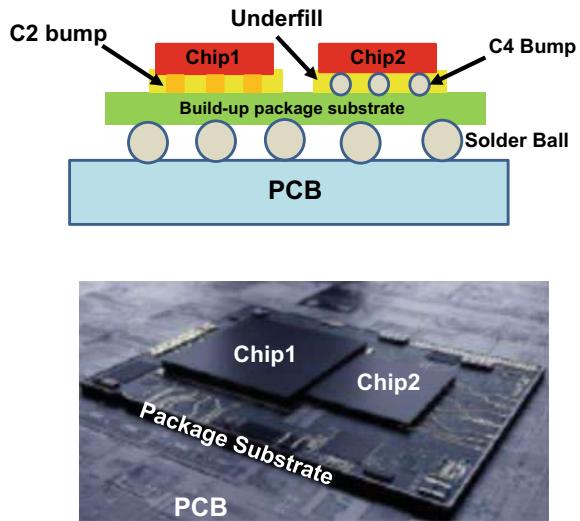


**Fig. 1.5** Advanced packaging: 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration



**Fig. 1.6** 2D fan-out with chip-first of 4 chips IC integration

**Fig. 1.7** 2D flip chip IC integration



## 1.6 2D Flip Chip IC Integration

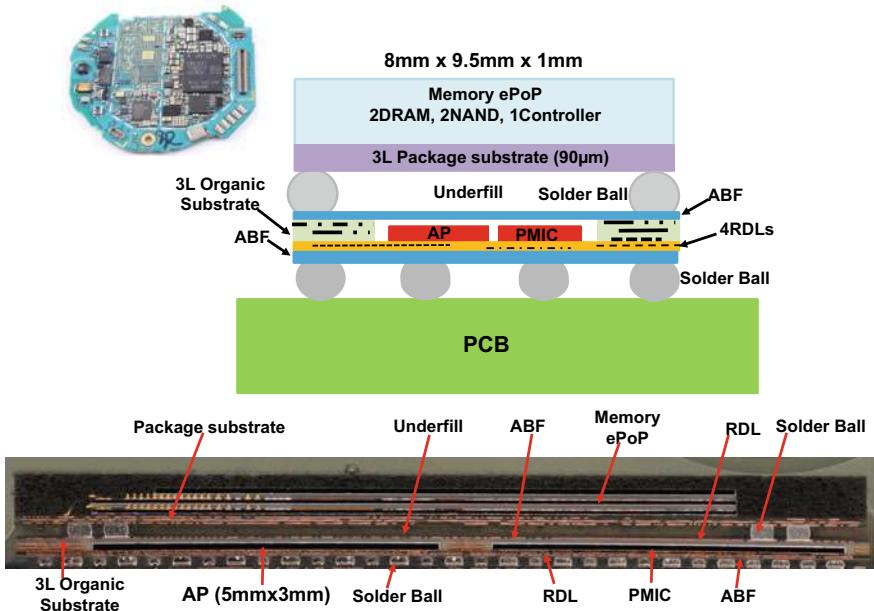
Figure 1.7 shows an example of 2D flip chip IC integration. It can be seen that the chips are flipped (attached) to a build-up package substrate with either C4 (controlled collapse chip connection) bump or C2 (chip connection) bump. Underfill between the chips and the package substrate is usually needed. The package substrate is then attached to the PCB. For more information about 2D flip chip IC integration, please read Chaps. 2 and 5.

## 1.7 PoP, SiP, and Heterogeneous Integration

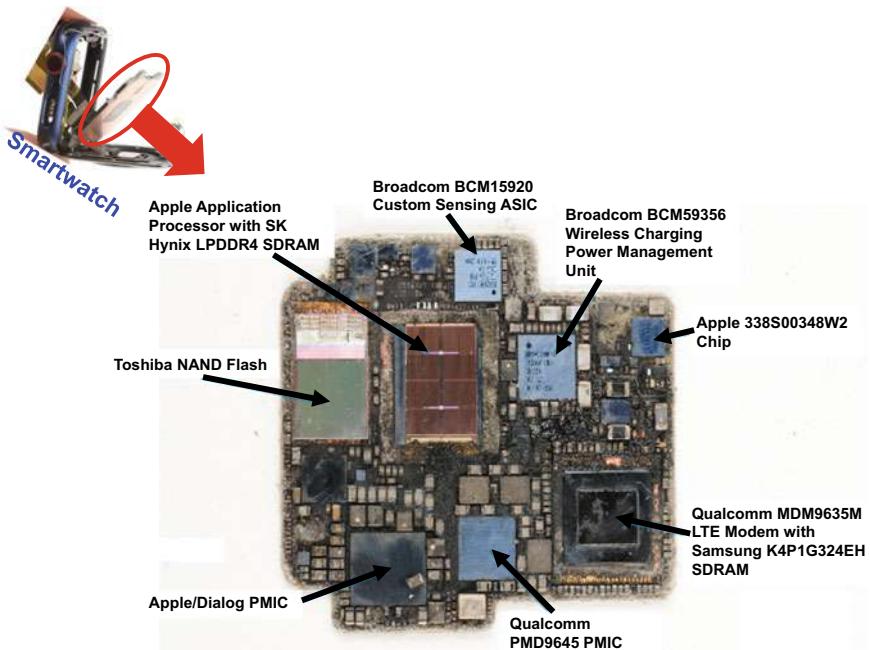
Figure 1.8 shows an example of PoP for a smartwatch provided by Samsung. It can be seen that the bottom package is housing the applied processor (AP) and the power management IC (PMIC) side-by-side with fan-out and chip-first process. The upper package is housing the controller, DRAM (dynamic random-access memory) and NAND (NAND is the short for “NOT AND”, a boolean operator and logic gate).

Figure 1.9 shows an example of SiP for a smartwatch provided by Apple. It can be seen that all the chips and discretes (system) are on (in) a single package substrate (package).

Figure 1.10 shows an example of heterogeneous integration for the IBM 9121 TCM (thermal conduction module). There are 121 chips (about  $8\text{--}10 \text{ mm}^2$ ) on the ceramic substrate which is with 63 layers. The thermal performance is super: up to 10 W dissipation per chip and 600 W dissipation per TCM.



**Fig. 1.8** PoP with 2D fan-out (chip-first) IC integration in the bottom package



**Fig. 1.9** SiP with 2D IC integration

**Fig. 1.10** Heterogeneous integration of 2D (of 121 chips) IC integration on ceramic substrate



#### IBM 9121 TCM (Thermal Conduction Module)

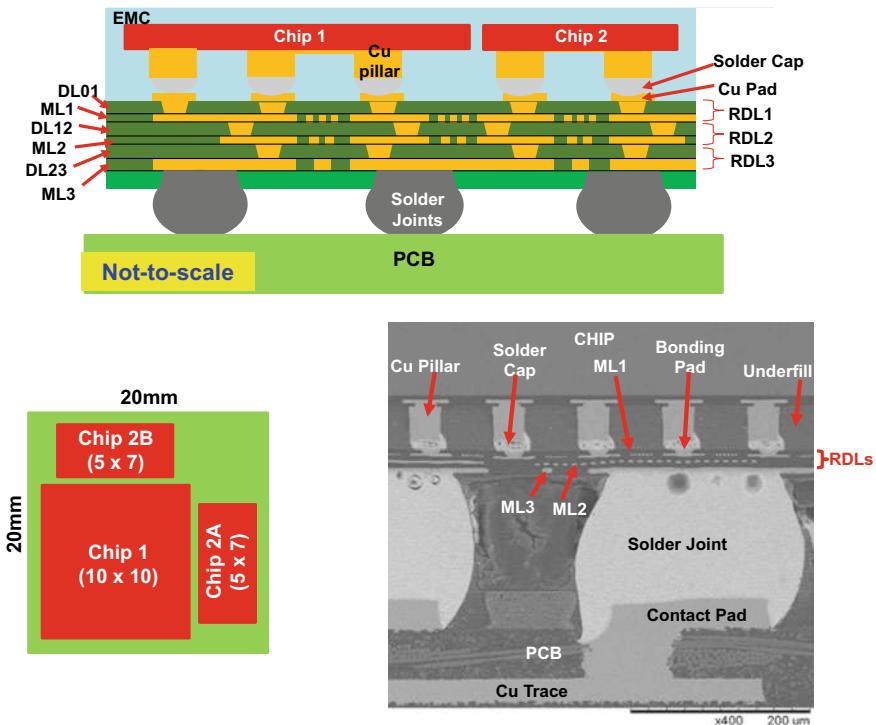
- TCM weighs 2.2Kg
- Contains up to 121 chips about 8-10mm square
- Each chip has a spring-loaded Cu piston to remove heat
- Up to 10W dissipation per chip
- Up to 600W dissipation per TCM
- Ceramic substrate has:
  - 63 layers
  - Up to 400m of wirings
  - Up to 2 million vias
- 5Kg air-cooled heatsink to remove heat from TCM

## 1.8 2D Fan-Out (Chip-Last) IC Integration

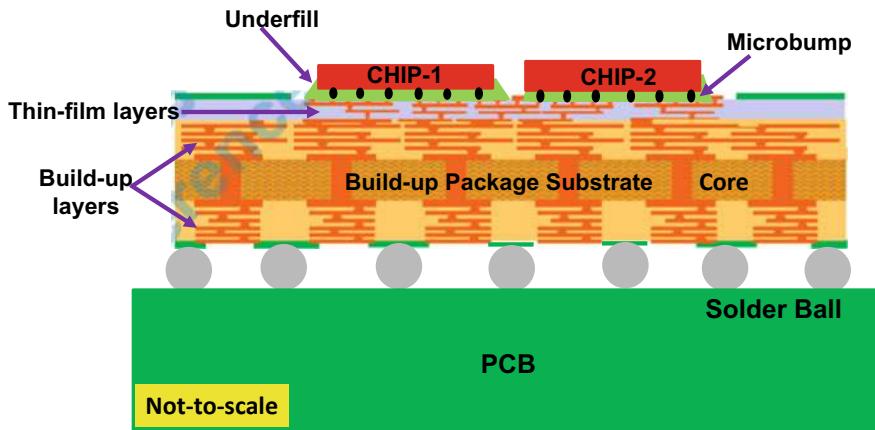
Figure 1.11 shows an example [22, 23] of fan-out with chip-last IC integration [24–40]. It can be seen that the fan-out RDLs with 2/2  $\mu\text{m}$  metal line width and spacing (L/S) are first fabricated. Then, it is followed by chips to RDL-substrate bonding with microbump (Cu pillar + solder cap) and RDL-substrate to PCB attaching with solder ball. The SEM (scanning electron microscope) image shows one of the chips, microbumps, RDL-substrate, solder joints, and PCB [22, 23]. For more information about fan-out (chip-last) IC integration, please read Chaps. 4 and 5.

## 1.9 2.1D Flip Chip IC Integration

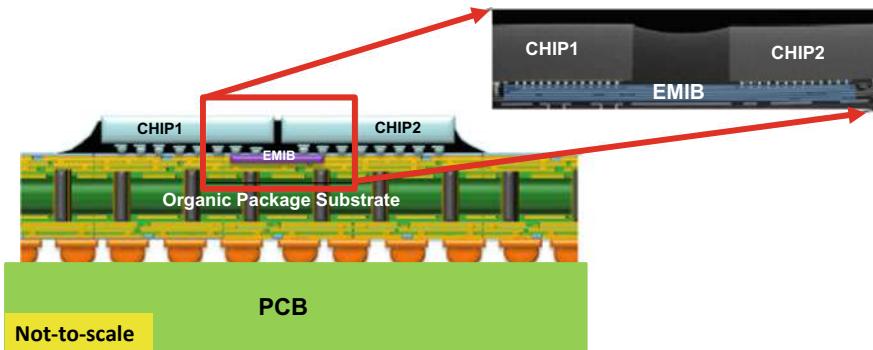
Figure 1.12 shows an example [41, 42] of 2.1D flip chip IC integration [43–46]. It can be seen that thin-film layers are built on top of the build-up package substrate. The metal L/S of the thin-film layers can go down to 2/2  $\mu\text{m}$ , which can support flip chips with microbumps [41, 42]. For more information about 2.1D flip chip IC integration, please read Chap. 5.



**Fig. 1.11** 2D fan-out with chip-last of three chips IC integration



**Fig. 1.12** 2.1D flip chip IC integration



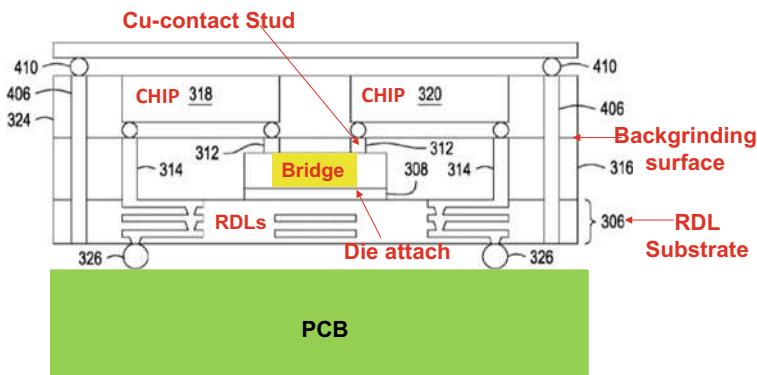
**Fig. 1.13** 2.1D flip chip IC integration with bridge [47, 48]

## 1.10 2.1D Flip Chip IC Integration with Bridges

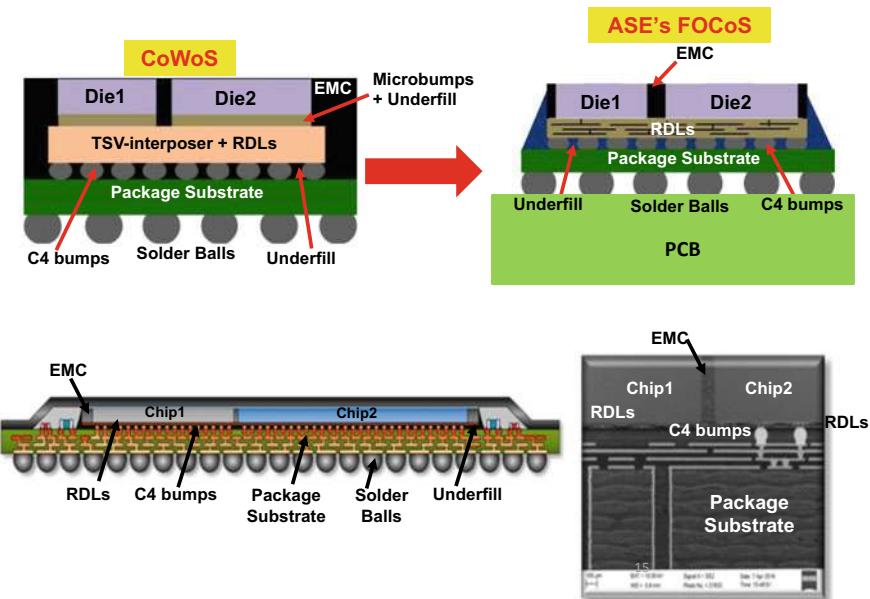
Figure 1.13 shows an example of 2.1D flip chip IC integration with bridges provided by Intel [47, 48]. It can be seen that the **EMIB** (embedded multi-die interconnect bridge) is embedded on the top layer of a build-up package substrate and is supporting the lateral communications between those two flip chips. This packaging technology is meant to replace the **TSV** (through silicon via)-interposer technology. For more information about 2.1D flip chip IC integration with bridges, please read Chap. 5.

## 1.11 2.1D Fan-Out IC Integration with Bridges

Figure 1.14 shows an example of 2.1D fan-out IC integration with bridges provided by Applied Materials [49]. It can be seen that the bridge is embedded in an EMC (epoxy



**Fig. 1.14** 2.1D fan-out IC integration with bridge [49]



**Fig. 1.15** 2.3D fan-out with chip-first IC integration [50]

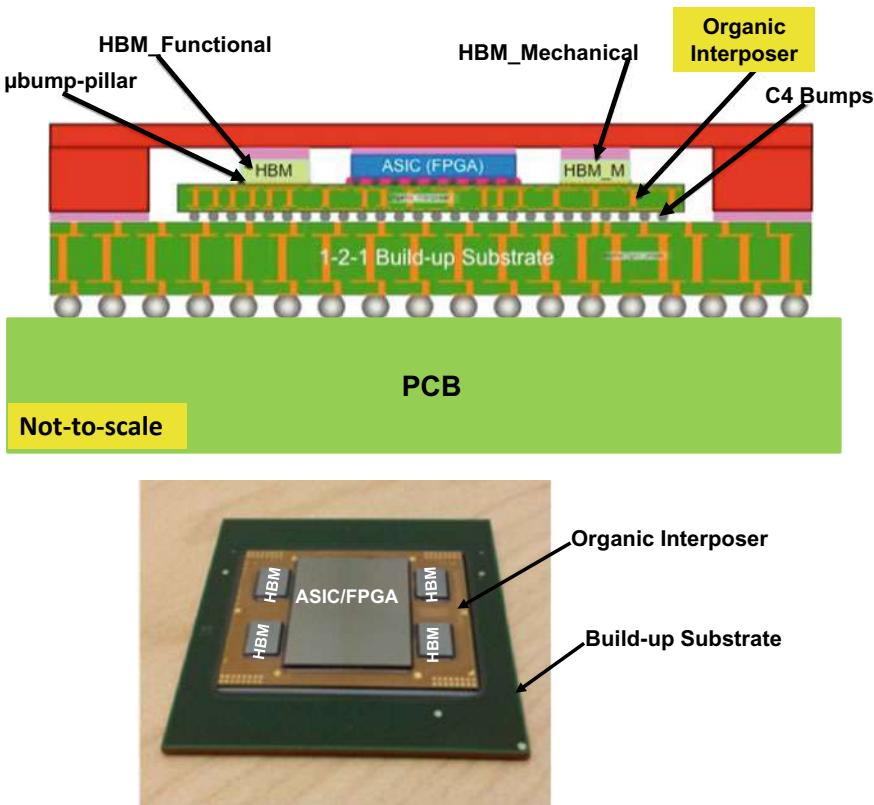
molding compound), instead of a build-up package substrate. For more information about 2.1D fan-out IC integration with bridges, please read Chap. 5.

## 1.12 2.3D Fan-Out (Chip-First) IC Integration

Figure 1.15 shows an example [50] of 2.3D fan-out (chip-first) IC integration [51–55]. It can be seen that the TSV-interposer, microbump, and underfill are replaced by the fan-out RDL-interposer. This technology is scheduled for HVM (high volume manufacturing) by ASE in 2021. For more information about 2.3D fan-out (chip-first) IC integration, please read Chap. 5.

## 1.13 2.3D Flip Chip IC Integration

Figure 1.16 shows an example of 2.3D flip chip IC integration provided by Cisco [56]. It can be seen that the coreless organic substrate (interposer) is built on top of a build-up package substrate and supporting a SoC (system-on-chip) and some HBMs (high-bandwidth memories). For more information about 2.3D flip chip IC integration, please read Chap. 5.



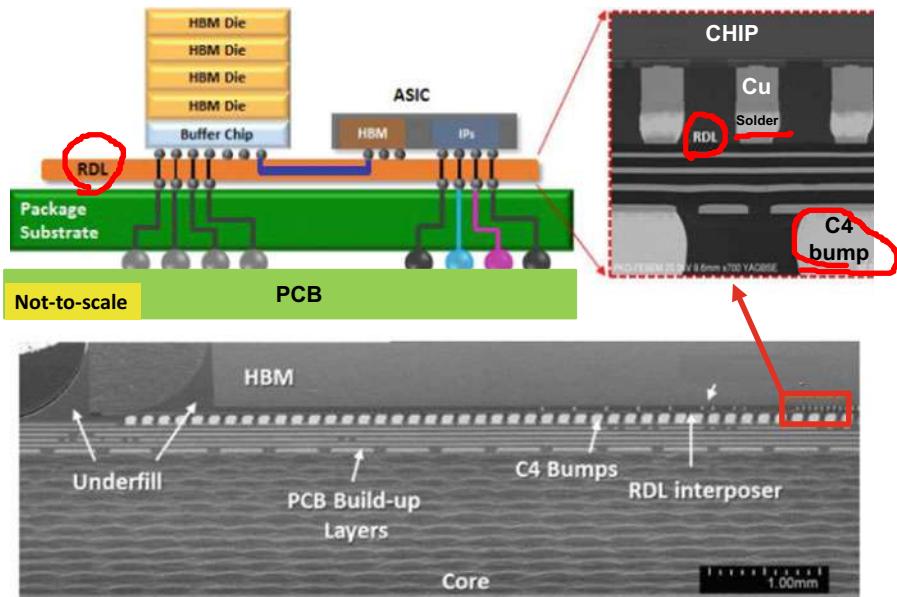
**Fig. 1.16** 2.3D flip chip IC integration [56]

## 1.14 2.3D Fan-Out (Chip-Last) IC Integration

Figure 1.17 shows an example [57, 58] of 2.3D fan-out (chip-last) IC integration [59–66]. It can be seen that an organic interposer is first build by a fan-out packaging method. It is followed by chips-to-organic interposer bonding with microbumps and underfilling. Then, the whole module is attached to the build-up package substrate with C4 bumps. For more information about 2.3D fan-out (chip-last) IC integration, please read Chap. 5.

## 1.15 2.5D (C4 Bump) IC Integration

Figure 1.18 shows an example [67, 68] of 2.5D flip chip (C4 bump) IC integration [69–78]. It can be seen that the RF chip and the logic chip are C4 solder bumped on



**Fig. 1.17** 2.3D fan-out with chip-last IC integration [57]

the passive TSV-interposers (silicon carriers 1 and 2). For more information about 2.5D (C4 bump) IC integration, please read Chap. 6.

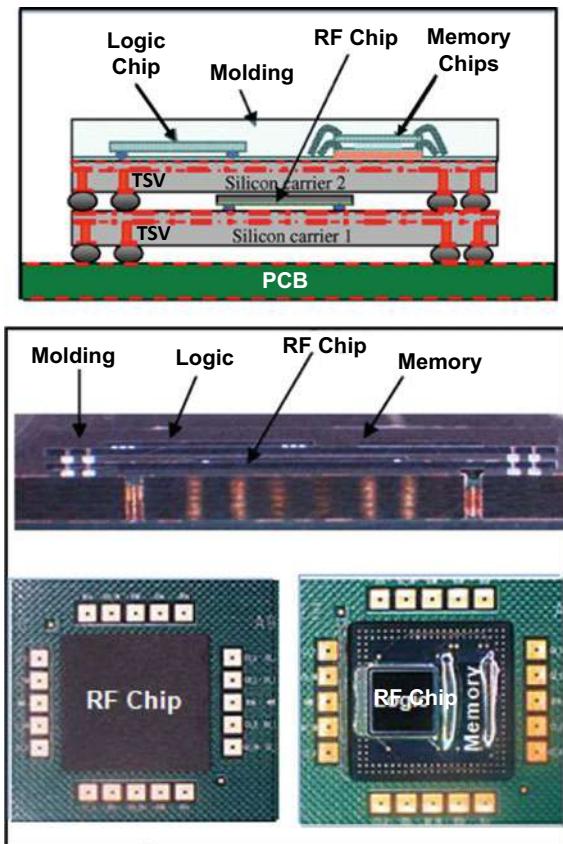
## 1.16 2.5D (C2 Bump) IC Integration

Figure 1.19 shows an example [79] of 2.5D flip chip (C2 bump) IC integration [80–94]. It can be seen that the GPU and the high bandwidth memory (HBM)2 are C2  $\mu$ bumped on the **passive TSV-interposer**. Then, the whole module is attached to a package substrate with C4 bumps. For more information about 2.5D (C2 bump) IC integration, please read [Chap. 6](#).

## 1.17 $\mu$ Bump 3D IC Integration

Figure 1.20 shows an example of 3D IC integration with  $\mu$ bumps provided by IME [95]. It can be seen that the top chip is connected (by  $\mu$ bumps) to the bottom chip with TSVs. Then, the whole module is attached to a package substrate with C4 bumps. For more information about  $\mu$ Bump 3D IC Integration, please read [Chap. 7](#).

**Fig. 1.18** 2.5D flip chip with C4 bump IC integration [79]

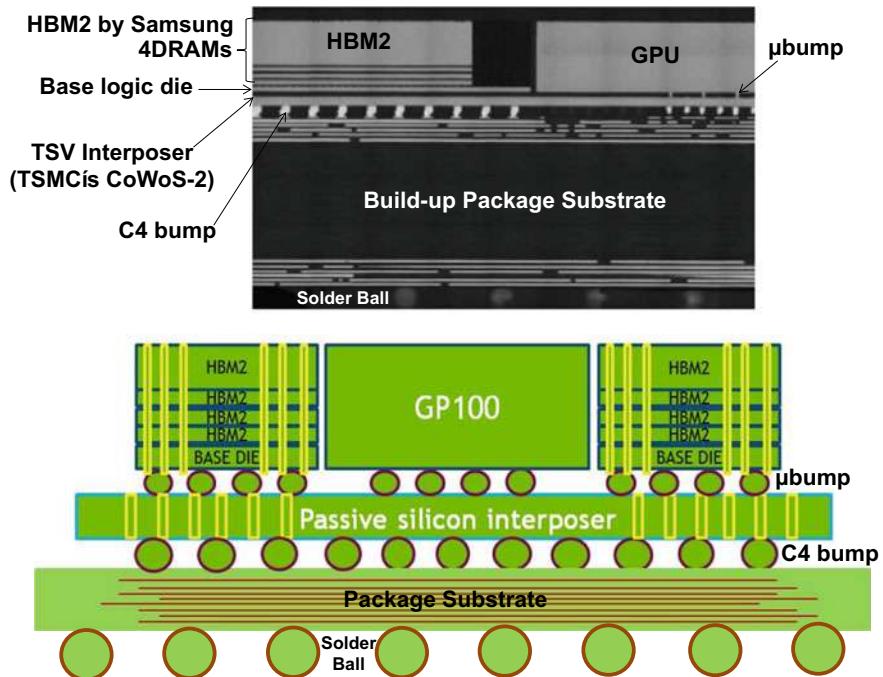


## 1.18 $\mu$ Bump Chiplets 3D IC Integration

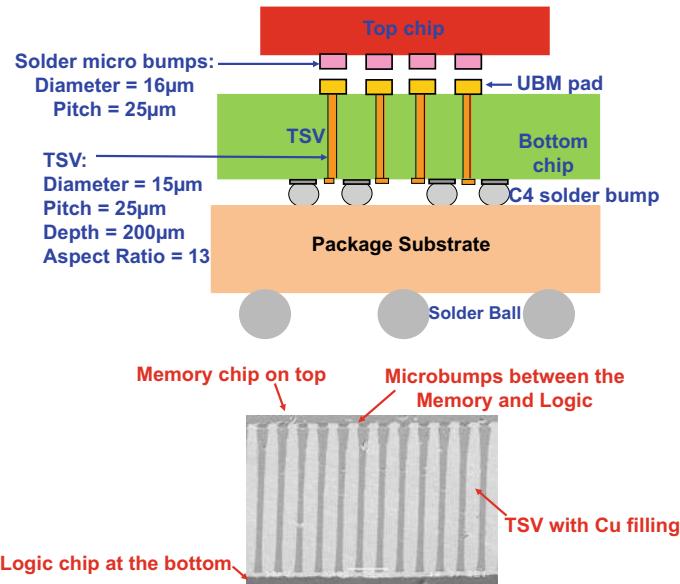
Figure 1.21 shows an example of 3D chiplets IC integration with  $\mu$ bumps provided by Intel [96–98]. It can be seen that the chiplets are face-to-face ( $\mu$ bump) bonded to a base chip with TSVs. Then, the whole module is attached to a package substrate with C4 bumps. For more information about  $\mu$ Bump chiplets 3D IC Integration, please read Chap. 8.

## 1.19 Bumpless 3D IC Integration

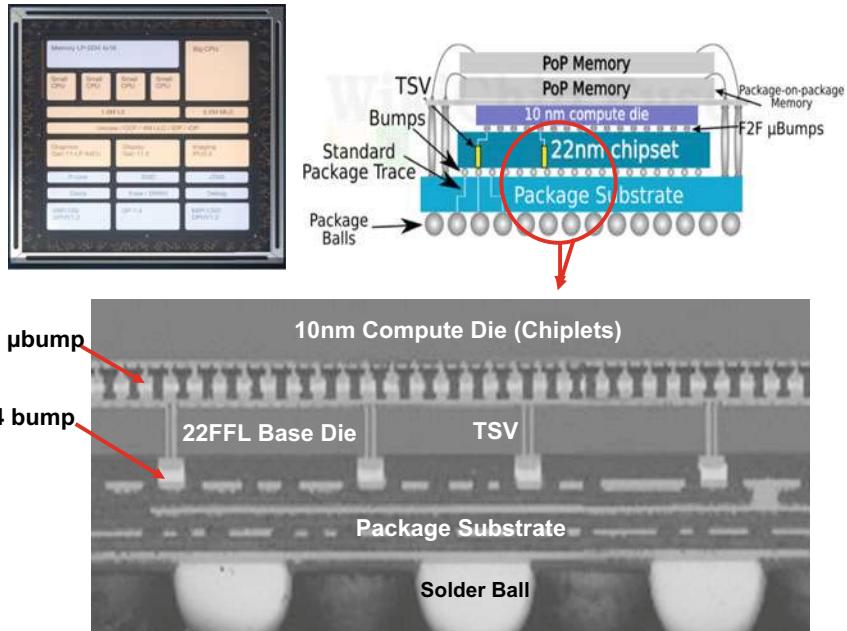
Figure 1.22 shows an example of bumpless 3D IC integration provided by Intel. It can be seen from Fig. 1.22b that with bumpless (hybrid bonding) 3D IC integration the pad-pitch can easily go down to 10  $\mu$ m. For more information about bumpless 3D IC Integration, please read Chap. 8.



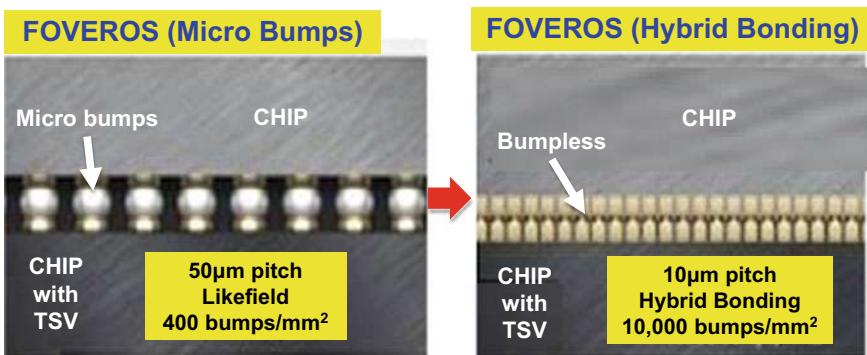
**Fig. 1.19** 2.5D flip chip with microbump IC integration



**Fig. 1.20** 3D IC integration with microbump



**Fig. 1.21** 3D IC chiplets integration with microbump [97]

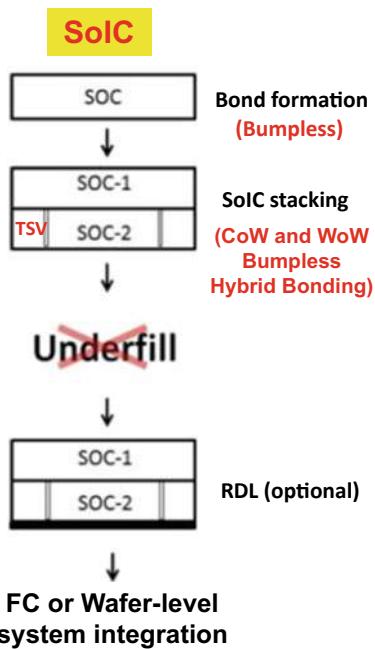


**Fig. 1.22** Bumpless 3D IC integration [98]

## 1.20 Bumpless Chiplets 3D IC Integration

Figure 1.23 shows the announcement of TSMC's SoIC (system on integrated chips) bumpless chiplets 3D IC integration [99–102]. It can be seen that the chiplets (SoC-1 and SoC-2 with TSV) are either CoW (chip-on-wafer) or WoW (wafer-on-wafer) bumpless hybrid bonding. It is scheduled in HVM in 2021. For more information about bumpless chiplets 3D IC Integration, please read Chap. 9.

**Fig. 1.23** Bumpless chiplets  
3D IC integration [101]



## 1.21 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- The Semiconductor industry has identified five major growth engines (applications):
  - Mobile
  - HPC
  - Autonomous vehicle
  - IoTs
  - Big data (for cloud computing) and instant data (for edge computing)
- The following system-technology drivers are boosting the growths of the 5 semiconductor applications:
  - AI
  - 5G
- The advanced packaging technologies to house the semiconductors are:
  - 2D fan-out (chip-first) IC integration
  - 2D flip chip IC integration
  - PoP (package-on-package)
  - SiP (system-in-package) or heterogeneous integration

- 2D fan-out (chip-last) IC integration
- 2.1D flip chip IC integration
- 2.1D flip chip IC integration with bridges
- 2.1D fan-out IC integration with bridges
- 2.3D fan-out (chip-first) IC integration
- 2.3D flip chip IC integration
- 2.3D fan-out (chip-last) IC integration
- 2.5D (C4 solder bump) IC integration
- 2.5D (C2  $\mu$ bump) IC integration
- $\mu$ bump 3D IC integration
- $\mu$ bump chiplets 3D IC integration
- Bumpless 3D IC integration
- Bumpless chiplets 3D IC integration
- The assembly processes are:
  - Wire bonding
  - SMT
  - Flip Chip mass reflow on Organic Substrate
  - CoC, CoW, and WoW TCB and hybrid bonding.

## References

1. Lau, J. H., *Chip On Board Technologies for Multichip Modules*, Van Nostrand Reinhold, New York, March 1994.
2. Lau, J. H., and Y. Pao, *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*, McGraw-Hill, New York, 1997.
3. Lau, J. H., *Low Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies*, McGraw-Hill, New York, 2000.
4. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, Springer, New York, 2020.
5. Lau, J. H., C. P. Wong, J. Prince, and W. Nakayama, *Electronic Packaging: Design, Materials, Process, and Reliability*, McGraw-Hill, New York, 1998.
6. Lau, J. H., M. Li, M. Li, T. Chen, I. Xu, X. Qing, Z. Cheng, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, P. Lo, K. Wu, J. Hao, S. Koh, R. Jiang, X. Cao, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, “Fan-Out Wafer-Level Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, 2018, September 2018, pp. 1544–1560.
7. Lau, J. H., M. Li, Y. Lei, M. Li, I. Xu, T. Chen, Q. Yong, Z. Cheng, K. Wu, P. Lo, Z. Li, K. Tan, Y. Cheung, N. Fan, E. Kuah, C. Xi, J. Ran, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, “Reliability of Fan-Out Wafer-Level Heterogeneous Integration”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 148–162.
8. Ko, CT, H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. W. Lin, T. Chen, I. Xu, C. Chang, J. Pan, H. Wu, Q. Yong, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, K. Wu, J. Hao, R. Beica, M. Lin, Y. Chen, Z. Cheng, S. Koh, R. Jiang, X. Cao, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, “Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, September 2018, pp. 1561–1572.

9. Ko, C. T., H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. Lin, C. Chang, J. Pan, H. Wu, Y. Chen, T. Chen, I. Xu, P. Lo, N. Fan, E. Kuah, Z. Li, K. Tan, C. Lin, R. Beica, M. Lin, C. Xi, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, "Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 141–147.
10. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1–27.
11. Lau, J. H., "Recent Advances and Trends in Heterogeneous Integrations", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 16, April 2019, pp. 45–77.
12. Hedler, H., T. Meyer, and B. Vasquez, "Transfer wafer level packaging," *US Patent 6,727,576*, filed on Oct. 31, 2001; patented on April 27, 2004.
13. Lau, J. H., "Patent Issues of Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 19, November/December 2015, pp. 42–46.
14. Brunnbauer, M., E. Furgut, G. Beer, T. Meyer, H. Hedler, J. Belonio, E. Nomura, K. Kiuchi, and K. Kobayashi, "An Embedded Device Technology Based on a Molded Reconfigured Wafer", *IEEE/ECTC Proceedings*, May 2006, pp. 547–551.
15. Brunnbauer, M., E. Furgut, G. Beer, and T. Meyer, "Embedded Wafer Level Ball Grid Array (eWLB)", *IEEE/EPTC Proceedings*, May 2006, pp. 1–5.
16. Keser, B., C. Amrine, T. Duong, O. Fay, S. Hayes, G. Leal, W. Lytle, D. Mitchell, and R. Wenzel, "The Redistributed Chip Package: A Breakthrough for Advanced Packaging", *Proceedings of IEEE/ECTC*, May 2007, pp. 286–291.
17. Kripesh, V., V. Rao, A. Kumar, G. Sharma, K. Houe, X. Zhang, K. Mong, N. Khan, and J. H. Lau, "Design and Development of a Multi-Die Embedded Micro Wafer Level Package", *IEEE/ECTC Proceedings*, May 2008, pp. 1544–1549.
18. Khong, C., A. Kumar, X. Zhang, S. Gaurav, S. Vempati, V. Kripesh, J. H. Lau, and D. Kwong, "A Novel Method to Predict Die Shift During Compression Molding in Embedded Wafer Level Package", *IEEE/ECTC Proceedings*, May 2009, pp. 535–541.
19. Sharma, G., S. Vempati, A. Kumar, N. Su, Y. Lim, K. Houe, S. Lim, V. Sekhar, R. Rajoo, V. Kripesh, and J. H. Lau, "Embedded Wafer Level Packages with Laterally Placed and Vertically Stacked Thin Dies", *IEEE/ECTC Proceedings*, 2009, pp. 1537–1543. Also, *IEEE Transactions on CPMT*, Vol. 1, No. 5, May 2011, pp. 52–59.
20. Kumar, A., D. Xia, V. Sekhar, S. Lim, C. Keng, S. Gaurav, S. Vempati, V. Kripesh, J. H. Lau, and D. Kwong, "Wafer Level Embedding Technology for 3D Wafer Level Embedded Package", *IEEE/ECTC Proceedings*, May 2009, pp. 1289–1296.
21. Lim, Y., S. Vempati, N. Su, X. Xiao, J. Zhou, A. Kumar, P. Thaw, S. Gaurav, T. Lim, S. Liu, V. Kripesh, and J. H. Lau, "Demonstration of High Quality and Low Loss Millimeter Wave Passives on Embedded Wafer Level Packaging Platform (EMWLP)", *IEEE/ECTC Proceedings*, 2009, pp. 508–515. Also, *IEEE Transactions on Advanced Packaging*, Vol. 33, 2010, pp. 1061–1071.
22. Lau, J. H., C. Ko, T. Peng, K. Yang, T. Xia, P. Lin, J. Chen, P. Huang, T. Tseng, E. Lin, L. Chang, C. Lin, and W. Lu, "Chip-Last (RDL-First) Fan-Out Panel-Level Packaging (FOPLP) for Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 17, No. 3, October 2020, pp. 89–98.
23. Lau, J. H., C. Ko, K. Yang, C. Peng, T. Xia, P. Lin, J. Chen, P. Huang, H. Liu, T. Tseng, E. Lin, and L. Chang, "Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125–1137.
24. Bu, L., F. Che, M. Ding, S. Chong, and X. Zhang, "Mechanism of Moldable Underfill (MUF) Process for Fan-Out Wafer Level Packaging", *IEEE/EPTC Proceedings*, 2015, pp. 1–7.
25. Che, F., D. Ho, M. Ding, and D. Woo, "Study on Process Induced Wafer Level Warpage of Fan-Out Wafer Level Packaging", *IEEE/ECTC Proceedings*, 2016, pp. 1879–1885.
26. Rao, V., C. Chong, D. Ho, D. Zhi, C. Choong, S. Lim, D. Ismael, and Y. Liang, "Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multilayer Fine Pitch RDL for Mobile Applications", *IEEE/ECTC Proceedings*, 2016, pp. 1522–1529.

27. Chen, Z., F. Che, M. Ding, D. Ho, T. Chai, V. Rao, "Drop Impact Reliability Test and Failure Analysis for Large Size High Density FOWLP Package on Package", *IEEE/ECTC Proceedings*, 2017, pp. 1196–1203.
28. Lim, T., and D. Ho, "Electrical design for the development of FOWLP for HBM integration", *IEEE/ECTC Proceedings*, 2018, pp. 2136–2142.
29. Ho, S., H. Hsiao, S. Lim, C. Choong, S. Lim, and C. Chong, "High Density RDL build-up on FO-WLP using RDL-first Approach", *IEEE/EPTC Proceedings*, 2019, pp. 23–27.
30. Boon, S., D. Wee, R. Salahuddin, and R. Singh, "Magnetic Inductor Integration in FO-WLP using RDLfirst Approach", *IEEE/EPTC Proceedings*, 2019, pp. 18–22.
31. Hsiao, H., S. Ho, S. S. Lim, W. Ching, C. Choong, S. Lim, H. Hong, and C. Chong, "Ultra-thin FO Packageon-Package for Mobile Application", *IEEE/ECTC Proceedings*, 2019, pp. 21–27.
32. Lin, B., F. Che, V. Rao, and X. Zhang, "Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging (FOPLP)", *IEEE/ECTC Proceedings*, 2019, pp. 1152–1158.
33. Sekhar, V., V. Rao, F. Che, C. Choong, and K. Yamamoto, "RDL-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging", *IEEE/ECTC Proceedings*, 2019, pp. 2126–2133.
34. Huemoeller, R. and C. Zwenger, "Silicon wafer integrated fan-out technology," *Chip Scale Review*, Mar/Apr 2015, pp. 34–37.
35. Hiner, D., M. Kelly, R. Huemoeller, and R. Reed, "Silicon interposer-less integrated module - SLIM," *IMAPS/Device Packaging*, March 2015.
36. Hiner, D., M. Kolbehdari, M. Kelly, Y. Kim, W. Do, J. Bae, "SLIM™ advanced fan-out packaging for high performance multi-die solutions," *IEEE/ECTC Proceedings*, May 2017, pp. 575–580.
37. Kim, Y., J. Bae, M. Chang, A. Jo, J. Kim, S. Park, et al., "SLIM™, high density wafer-level fan-out package development with sub-micron RDL," *IEEE/ECTC Proceedings*, May 2017, pp. 18–13.
38. Zwenger, C., G. Scott, B. Baloglu, M. Kelly, W. Do, W. Lee, and J. Yi, "Electrical and Thermal Simulation of SWIFT™ High-density Fan-out PoP Technology", *IEEE/ECTC Proceedings*, May 2017, pp. 1962–1967.
39. Scott, G., J. Bae, K. Yang, W. Ki, N. Whitchurch, M. Kelly, C. Zwenger, J. Jeon, and T. Hwang, "Heterogeneous Integration Using Organic Interposer Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 885–892.
40. Ma, M., S. Chen, P. I. Wu, A. Huang, C. H. Lu, A. Chen, C. Liu, and S. Peng, "The development and the integration of the 5  $\mu\text{m}$  to 1  $\mu\text{m}$  half pitches wafer level Cu redistribution layers", *IEEE/ECTC Proceedings*, May 2016, pp. 1509–1514.
41. Shimizu, N., W. Kaneda, H. Arisaka, N. Koizumi, S. Sunohara, A. Rokugawa, and T. Koyama, "Development of Organic Multi Chip Package for High Performance Application", *IMAPS Proceedings of International Symposium on Microelectronics*, October 2013, pp. 414–419.
42. Oi, K., S. Otake, N. Shimizu, S. Watanabe, Y. Kunimoto, T. Kurihara, T. Koyama, M. Tanaka, L. Aryasomayajula, and Z. Kutlu, "Development of New 2.5D Package with Novel Integrated Organic Interposer Substrate with Ultra-fine Wiring and High Density Bumps", *IEEE/ECTC Proceedings*, May 2014, pp. 348–353.
43. Uematsu, Y., N. Ushifusa, and H. Onozeki, "Electrical Transmission Properties of HBM Interface on 2.1-D System in Package using Organic Interposer", *IEEE/ECTC Proceedings*, May 2017, pp. 1943–1949.
44. Chen, W., C. Lee, M. Chung, C. Wang, S. Huang, Y. Liao, H. Kuo, C. Wang, and D. Tarng, "Development of novel fine line 2.1 D package with organic interposer using advanced substrate-based process", *IEEE/ECTC Proceedings*, May 2018, pp. 601–606.
45. Huang, C., Y. Xu, Y. Lu, K. Yu, W. Tsai, C. Lin, C. Chung, "Analysis of Warpage and Stress Behavior in a Fine Pitch Multi-Chip Interconnection with Ultrafine-Line Organic Substrate (2.1D)", *IEEE/ECTC Proceedings*, May 2018, pp. 631–637.
46. Islam, N., S. Yoon, K. Tan, and T. Chen, "High Density Ultra-Thin Organic Substrate for Advanced Flip Chip Packages", *IEEE/ECTC Proceedings*, May 2019, pp. 325–329.

47. Chiu, C., Z. Qian, and M. Manusharow, "Bridge interconnect with air gap in package assembly," *US Patent No. 8,872,349*, 2014.
48. Mahajan, R., R. Sankman, N. Patel, D. Kim, K. Aygun, Z. Qian, et al., "Embedded multi-die interconnect bridge (EMIB) – a high-density, high-bandwidth packaging interconnect," *IEEE/ECTC Proceedings*, May 2016, pp. 557–565.
49. Hsiung, C., and a. Sundarrajan, "Methods and Apparatus for Wafer-Level Die Bridge", US 10,651,126 B2, Filed on December 8, 2017, Granted on May 12, 2020.
50. Lin, Y., W. Lai, C. Kao, J. Lou, P. Yang, C. Wang, and C. Hsieh, "Wafer warpage experiments and simulation for fan-out chip on substrate," *IEEE/ECTC Proceedings*, May 2016, pp. 13–18.
51. Pendse, R., "Semiconductor Device and Method of Forming Extended Semiconductor Device with Fan-Out Interconnect Structure to Reduce Complexity of Substrate", US 9,484,319 B2, Filed: December 23, 2011, Granted: November 1, 2016.
52. Yoon, S., P. Tang, R. Emigh, Y. Lin, P. Marimuthu, and R. Pendse, "Fanout Flipchip eWLB (Embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions", *IEEE/ECTC Proceedings*, 2013, pp. 1855–1860.
53. Chen, N., "Flip-Chip Package with Fan-Out WLCSP", US 7,838,975 B2, Filed: February 12, 2009, Granted: November 23, 2010.
54. Chen, N. C., T. Hsieh, J. Jinn, P. Chang, F. Huang, J. Xiao, A. Chou, B. Lin, "A Novel System in Package with Fan-out WLP for high speed SERDES application", *IEEE/ECTC Proceedings*, May 2016, pp. 1496–1501.
55. Yu, D., "Advanced system integration technology trends," *SiP Global Summit*, SEMICON Taiwan, Sept. 6, 2018.
56. Li, L., P. Chia, P. Ton, M. Nagar, S. Patil, J. Xue, J. DeLaCruz, M. Voicu, J. Hellings, B. Isaacson, M. Coor, and R. Havens, "3D SiP with Organic Interposer for ASIC and Memory Integration", *IEEE/ECTC Proceedings*, May 2016, pp. 1445–1450.
57. Suk, K., S. Lee, J. Kim, S. Lee, H. Kim, S. Lee, P. Kim, D. Kim, D. Oh, and J. Byun, "Low Cost Si-less RDL Interposer Package for High Performance Computing Applications", *IEEE/ECTC Proceedings*, May 2018, pp. 64–69.
58. You, S., S. Jeon, D. Oh, K. Kim, J. Kim, S. Cha, G. Kim, "Advanced Fan-Out Package SI/PI/Thermal Performance Analysis of Novel RDL Packages", *IEEE/ECTC Proceedings*, May 2018, pp. 1295–1301.
59. Kwon, W., S. Ramalingam, X. Wu, L. Madden, C. Huang, H. Chang, et al., "Cost-effective and high-performance 28 nm FPGA with new disruptive silicon-less interconnect technology (SLIT)," *Proc. of Inter. Symp. on Micro.*, October 2014, pp. 599–605.
60. Liang, F., H. Chang, W. Tseng, J. Lai, S. Cheng, M. Ma, et al., "Development of non-TSV interposer (NTI) for high electrical performance package," *IEEE/ECTC Proceedings*, May 2016, pp. 31–36.
61. Lin, Y., M. Yew, M. Liu, S. Chen, T. Lai, P. Kavle, C. Lin, T. Fang, C. Chen, C. Yu, K. Lee, C. Hsu, P. Lin, F. Hsu, and S. Jeng, "Multilayer RDL Interposer for Heterogeneous Device and Module Integration", *IEEE/ECTC Proceedings*, May 2019, pp. 931–936.
62. Chang, K., C. Huang, H. Kuo, M. Jhong, T. Hsieh, M. Hung, C. Wang, "Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity", *IEEE/ECTC Proceedings*, May 2019, pp. 41–46.
63. Lai, W., P. Yang, I. Hu, T. Liao, K. Chen, D. Tarn, and C. Hung, "A Comparative Study of 2.5D and Fan-out Chip on Substrate: Chip First and Chip Last", *IEEE/ECTC Proceedings*, May 2020, pp. 354–360.
64. Fang, J., M. Huang, H. Tu, W. Lu, P. Yang, "A Production-worthy Fan-Out Solution – ASE FOCoS Chip Last", *IEEE/ECTC Proceedings*, May 2020, pp. 290–295.
65. Miki, S., H. Taneda, N. Kobayashi, K. Oi, K. Nagai, T. Koyama, "Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder", *IEEE/ECTC Proceedings*, May 2019, pp. 1599–1604.
66. Murayama, K., S. Miki, H. Sugahara, and K. Oi, "Electro-migration evaluation between organic interposer and build-up substrate on 2.3D organic package", *IEEE/ECTC Proceedings*, May 2020, pp. 716–722.

67. Khan, N., V. Rao, S. Lim, H. We, V. Lee, X. Zhang, E. Liao, R. Nagarajan, T. C. Chai, V. Kripesh, and J. H. Lau, "Development of 3-D Silicon Module With TSV for System in Packaging", *IEEE/ECTC Proceedings*, May 2008, pp. 550–555.
68. Khan, N., V. Rao, S. Lim, H. We, V. Lee, X. Zhang, E. Liao, R. Nagarajan, T. C. Chai, V. Kripesh, and J. H. Lau, "Development of 3-D Silicon Module With TSV for System in Packaging", *IEEE Transactions on CPMT*, Vol. 33, No. 1, March 2010, pp. 3–9.
69. Selvanayagam, C., J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, "Nonlinear Thermal Stress/Strain Analyses of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps", *IEEE Transactions on Advanced Packaging*, Vol. 32, No. 4, November 2009, pp. 720–728.
70. Khan, N., L. Yu, P. Tan, S. Ho, N. Su, H. Wai, K. Vaidyanathan, D. Pinjala, J. H. Lau, T. Chuan, "3D Packaging with Through Silicon Via (TSV) for Electrical and Fluidic Interconnections", *IEEE/ECTC Proceedings*, May, 2009, pp. 1153–1158.
71. Yu, A., N. Khan, G. Archit, D. Pinjala, K. Toh, V. Kripesh, S. Yoon, and J. H. Lau, "Fabrication of Silicon Carriers With TSV Electrical Interconnections and Embedded Thermal Solutions for High Power 3-D Packages", *IEEE Transactions on CPMT*, Vol. 32, No. 3, September 2009, pp. 566–571.
72. Tang, G. Y., S. Tan, N. Khan, D. Pinjala, J. H. Lau, A. Yu, V. Kripesh, and K. Toh, "Integrated Liquid Cooling Systems for 3-D Stacked TSV Modules", *IEEE Transactions on CPMT*, Vol. 33, No. 1, March 2010, pp. 184–195.
73. Khan, N., H. Li, S. Tan, S. Ho, V. Kripesh, D. Pinjala, J. H. Lau, and T. Chuan, "3-D Packaging With Through-Silicon Via (TSV) for Electrical and Fluidic Interconnections", *IEEE Transactions on CPMT*, Vol. 3, No. 2, February 2013, pp. 221–228.
74. Zhang, X., T. Chai, J. H. Lau, C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, et al., "Development of Through Silicon Via (TSV) Interposer Technology for Large Die (21x21mm) Fine-pitch Cu/low-k FCBGA Package", *IEEE/ECTC Proceedings*, May 2009, pp. 305–312.
75. Chai, T. C., X. Zhang, J. H. Lau, C. S. Selvanayagam, D. Pinjala, et al., "Development of Large Die Fine-Pitch Cu/low-k FCBGA Package with through Silicon via (TSV) Interposer", *IEEE Transactions on CPMT*, Vol. 1, No. 5, May 2011, pp. 660–672.
76. Lau, J. H., S. Lee, M. Yuen, J. Wu, C. Lo, H. Fan, and H. Chen, "Apparatus having thermal-enhanced and cost-effective 3D IC integration structure with through silicon via interposer". US Patent No: 8,604,603, Filed Date: February 19, 2010, Date of Patent: December 10, 2013.
77. Lau, J. H., Y. S. Chan, and R. S. W. Lee, "3D IC Integration with TSV Interposers for High-Performance Applications", *Chip Scale Review*, Vol. 14, No. 5, September/October, 2010, pp. 26–29.
78. Chien, H. C., J. H. Lau, Y. Chao, R. Tain, M. Dai, S. T. Wu, W. Lo, and M. J. Kao, "Thermal Performance of 3D IC Integration with Through-Silicon Via (TSV)", *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 9, 2012, pp. 97–103.
79. Hou, S., W. Chen, C. Hu, C. Chiu, K. Ting, T. Lin, W. Wei, W. Chiou, V. Lin, V. Chang, C. Wang, C. Wu, and D. Yu, "Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology", *IEEE Transactions on Electron Devices*, October 2017, pp. 4071–4077.
80. Banijamali, B., S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced Reliability Study of TSV Interposers and Interconnects for the 28 nm Technology FPGA", *Proceedings of IEEE/ECTC*, May 2011, pp. 285–290.
81. Kim, N., D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer Design Optimization for High Frequency Signal Transmission in Passive and Active Interposer using Through Silicon Via (TSV)", *IEEE/ECTC Proceedings*, May 2011, pp. 1160–1167.
82. Banijamali, B., S. Ramalingam, N. Kim, C. Wyland, N. Kim, D. Wu, J. Carrel, J. Kim, and Paul Wu, "Ceramics vs. low-CTE Organic packaging of TSV Silicon Interposers", *IEEE/ECTC Proceedings*, May 2011, pp. 573–576.
83. Chaware, R., K. Nagarajan, and S. Ramalingam, "Assembly and Reliability Challenges in 3D Integration of 28 nm FPGA Die on a Large High Density 65 nm Passive Interposer", *Proceedings of IEEE/ECTC*, May 2012, San Diego, CA, pp. 279–283.

84. Banijamali, B., S. Ramalingam, H. Liu and M. Kim, "Outstanding and Innovative Reliability Study of 3D TSV Interposer and Fine Pitch Solder Micro-bumps", *Proceedings of IEEE/ECTC*, San Diego, CA, May 2012, pp. 309–314.
85. Kim, N., D. Wu, J. Carrel, J. Kim, and P. Wu, "Channel Design Methodology for 28 Gb/s SerDes FPGA Applications with Stacked Silicon Interconnect Technology", *IEEE/ECTC Proceedings*, May 2012, pp. 1786–1793.
86. Banijamali, B., C. Chiu, C. Hsieh, T. Lin, C. Hu, S. Hou, et al., "Reliability evaluation of a CoWoS-enabled 3D IC package," *IEEE/ECTC Proceedings*, May 2013, pp. 35–40.
87. Hariharan, G., R. Chaware, L. Yip, I. Singh, K. Ng, S. Pai, M. Kim, H. Liu, and S. Ramalingam, "Assembly Process Qualification and Reliability Evaluations for Heterogeneous 2.5D FPGA with HiCTE Ceramic", *IEEE/ECTC Proceedings*, May 2013, pp. 904–908.
88. Kwon, W., M. Kim, J. Chang, S. Ramalingam, L. Madden, G. Tsai, S. Tseng, J. Lai, T. Lu, and S. Chin, "Enabling a Manufacturable 3D Technologies and Ecosystem using 28 nm FPGA with Stack Silicon Interconnect Technology", *IMAPS Proceedings of International Symposium on Microelectronics*, Orlando, FL, October 2013, pp. 217–222.
89. Banijamali, B., T. Lee, H. Liu, S. Ramalingam, I. Barber, J. Chang and M. Kim, and L. Yip, "Reliability Evaluation of an Extreme TSV Interposer and Interconnects for the 20 nm Technology CoWoS IC Package", *IEEE/ECTC Proceedings*, May 2015, pp. 276–280.
90. Hariharan, G., R. Chaware, I. Singh, J. Lin, L. Yip, K. Ng, and S. Pai, "A Comprehensive Reliability Study on a CoWoS 3D IC Package", *IEEE/ECTC Proceedings*, May 2015, pp. 573–577.
91. Chaware, R., G. Hariharan, J. Lin, I. Singh, G. O'Rourke, K. Ng, S. Pai, C. Li, Z. Huang, and S. Cheng, "Assembly Challenges in Developing 3D IC Package with Ultra High Yield and High Reliability", *IEEE/ECTC Proceedings*, May 2015, pp. 1447–1451.
92. Xu, J., Y. Niu, S. Cain, S. McCann, H. Lee, G. Ahmed, and S. Park, "The Experimental and Numerical Study of Electromigration in 2.5D Packaging", *IEEE/ECTC Proceedings*, May 2018, pp. 483–489.
93. McCann, S., H. Lee, G. Ahmed, T. Lee, S. Ramalingam, "Warpage and Reliability Challenges for Stacked Silicon Interconnect Technology in Large Packages", *IEEE/ECTC Proceedings*, May 2018, pp. 2339–2344.
94. Wang, H., J. Wang, J. Xu , V. Pham, K. Pan, S. Park, H. Lee, and G. Ahmed, "Product Level Design Optimization for 2.5D Package Pad Cratering Reliability during Drop Impact", *IEEE/ECTC Proceedings*, May 2019, pp. 2343–2348.
95. Yu, A. B., J. H. Lau, S. Ho, A. Kumar, W. Hnin, W. Lee, M. Jong, et al., "Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects", *IEEE Transactions on CPMT*, Vol. 1, No. 9, September 2011, pp. 1336–1344.
96. Ingerly, D., S. Amin, L. Aryasomayajula, A. Balankutty, D. Borst, A. Chandra, K. Cheemalapati, C. Cook, R. Criss, K. Enamul1, W. Gomes, D. Jones, K. Kolluru, A. Kandas, G. Kim, H. Ma, D. Pantuso, C. Petersburg, M. Phen-givoni, A. Pillai, A. Sairam, P. Shekhar, P. Sinha, P. Stover, A. Telang, and Z. Zell, "Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices", *IEEE/IEDM Proceedings*, December 2019, pp. 19.6.1–19.6.4.
97. Gomes, W., S. Khushu, D. Ingerly, P. Stover, N. Chowdhury, F. O'Mahony, etc., "Lakefield and Mobility Computer: A 3D Stacked 10 nm and 2FFL Hybrid Processor System in 12 × 12 mm<sup>2</sup>, 1 mm Package-on-Package", *IEEE/ISSCC Proceedings*, February 2020, pp. 40–41.
98. WikiChip, "A Look at Intel Lakefield: A 3D-Stacked Single-ISA Heterogeneous Penta-Core SoC", <https://en.wikichip.org/wiki/chiplet>, May 27, 2020.
99. Chen, M. F., C. S. Lin, E. B. Liao, W. C. Chiou, C. C. Kuo, C. C. Hu, C. H. Tsai, C. T. Wang and D. Yu, "SoIC for Low-Temperature, Multi-Layer 3D Memory Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.
100. Chen, Y. H., C. A. Yang, C. C. Kuo, M. F. Chen, C. H. Tung, W. C. Chiou, and D. Yu, "Ultra High Density SoIC with Sub-micron Bond Pitch", *IEEE/ECTC Proceedings*, May 2020, pp. 576–581.

101. Chen, F., M. Chen, W. Chiou, D. Yu, “System on Integrated Chips (SoIC<sup>TM</sup>) for 3D Heterogeneous Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 594–599.
102. Chen, M., C. Lin, E. Liao, W. Chiou, C. Kuo, C. Hu, C. Tsai, C. Wang and D. Yu, “SoIC for Low-Temperature, Multi-Layer 3D Memory Integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.

# Chapter 2

## System-in-Package (SiP)



### 2.1 Introduction

System-in-package (SiP) technology has been used extensively on consumer products such as smartwatches, smartphones, tablets, notebooks, TWS (true wireless stereo), etc. The key assembly processes of SiP technology are basically SMT (surface mount technology) and flip chip technology, which will be presented and discussed in this chapter. The difference between the SoC (system-on-chip) and SiP, the intention and actual applications of SiP, and some examples in using SiP technology to manufacture consumer products will be briefly mentioned first.

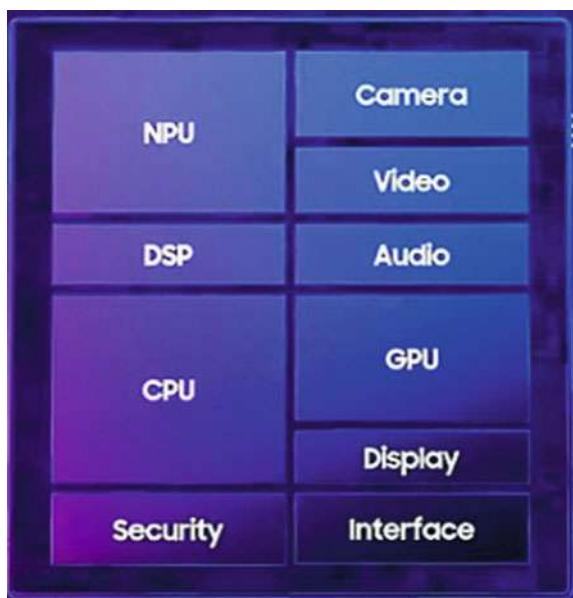
### 2.2 SoC (System-on-Chip)

Due to the drive of Moore's law, compounded with the demands of mobile products such as smartphones, tablets, notebooks, and wearables, SoC (system-on-chip) has been very popular in the past 10 + years. SoC integrates ICs with different functions such as CPU (central processing unit), GPU (graphic processing unit), memory, etc. into a single chip for a system or subsystem. Figure 2.1 schematically shows Qualcomm's Snapdragon 888 5G processor. Figure 2.2 schematically shows Samsung's Exynos 990 5G processor. Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC.

**Fig. 2.1** SoC: Qualcomm's application processors



**Fig. 2.2** Samsung's application processors



## 2.3 System-in-Package (SiP)

System-in-package (SiP) [1–109] contrasts with SoC. SiP uses packaging technology to integrate dissimilar chips such as CPU, GPU, memory, etc., photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. SiP is very similar to heterogeneous integration [1–109], except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance.

## 2.4 Intention of SiP

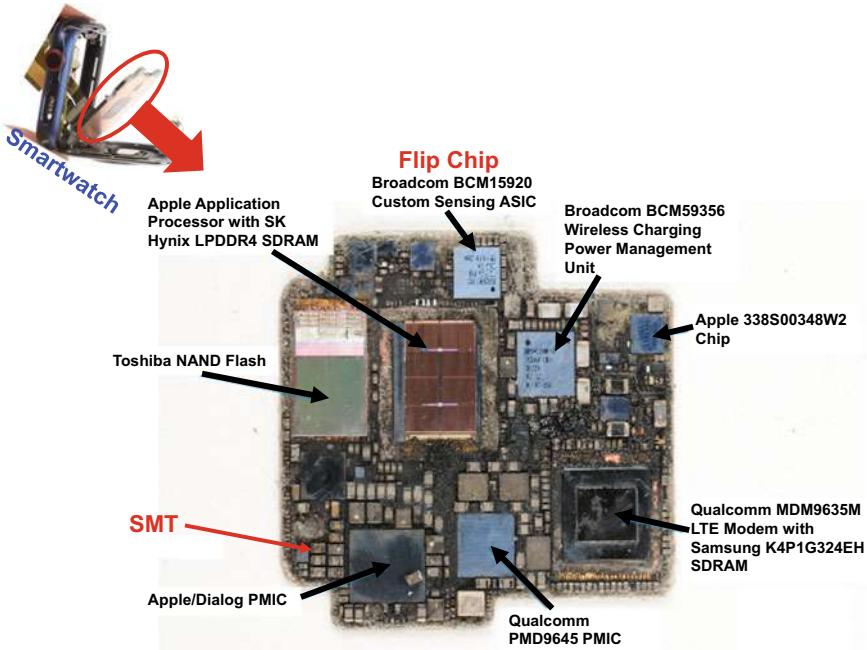
More than 10 years ago, the intention of SiP was to integrate different chips and discrete components, as well as 3D chip stacking of either packaged chips or bare chips such as the wide-bandwidth memory cubes and memory on logic with TSVs (through-silicon vias) side-by-side on a common (either silicon, ceramic, or organic) substrate to form a system or subsystem for smartphones, tablets, notebooks, etc. applications. It was expected that SiP technology performs horizontal as well as vertical integrations, so called vertical-MCM (multichip module) or 3D-MCM.

## 2.5 Actual Applications of SiP

Unfortunately, because of the high cost of TSV technology [110, 111] for smartphones and tablets, it never materialized. Most SiPs that went into HVM (high volume manufacturing) in the past 10 years are actually MCM-L (MCM on laminated substrate) for applications such as smartphones, tablets, smart watches, medical, wearable electronics, gaming systems, consumer products, and internet of things (IoT)-related products such as smart homes, smart energy, and smart industrial automation. Most actual applications of SiPs by OSATs (outsourced semiconductor assembly and test) integrate two or more dissimilar chips, components, and discrete components on a common laminated organic substrate.

## 2.6 SiP Examples

For examples, in the case of Apple, a major consumer electronics manufacturer, pursuing advanced semiconductor and packaging technology that is light, thin, small, and low-cost, SiP plays an indispensable role. Since Apple launched the Apple Watch in 2015 with the SiP technology, the cumulative global shipments of this series of



**Fig. 2.3** Apple's smartwatch: SiP

products have been close to 100 million. Figure 2.3 shows the SiP for Apple Watch series 4. In 2019, Apple's AirPods Pro also used SiP technology (Fig. 2.4). The 5G mmWave AiP (antenna-in-package) of the iPhone 12 (2020) is shown in Fig. 2.5. The AiP module (Fig. 2.5) that integrates multiple array antennas, beamforming circuits, and various RF components is actually based on the SiP concept.

There are more examples on SiP other than Apple. In 2019 Qualcomm shipped their QSiP (Qualcomm SiP) which integrates some components commonly found in Snapdragon mobile platforms, such as processors, power management, RF front-ends, and audio transcoders, into a single package, providing more internal space for cameras, batteries and other components.

Since SiP technology can help TWS (true wireless stereo) products such as the AirPods Pro meet the market demand characteristics of multiple functions, small size, and long standby time, it has attracted the attention of other non-Apple customers/manufacturers. It is understood that the first non-Apple TWS product suing SiP technology is expected to come out in the first half of 2021.

The major assembly processes of SiP technology are by SMT [112, 113] and flip chip technology [115–118] as shown in Figs. 2.3, 2.4, 2.5 and 2.6. Thus SMT and flip chip technology will be presented and discussed in this chapter.

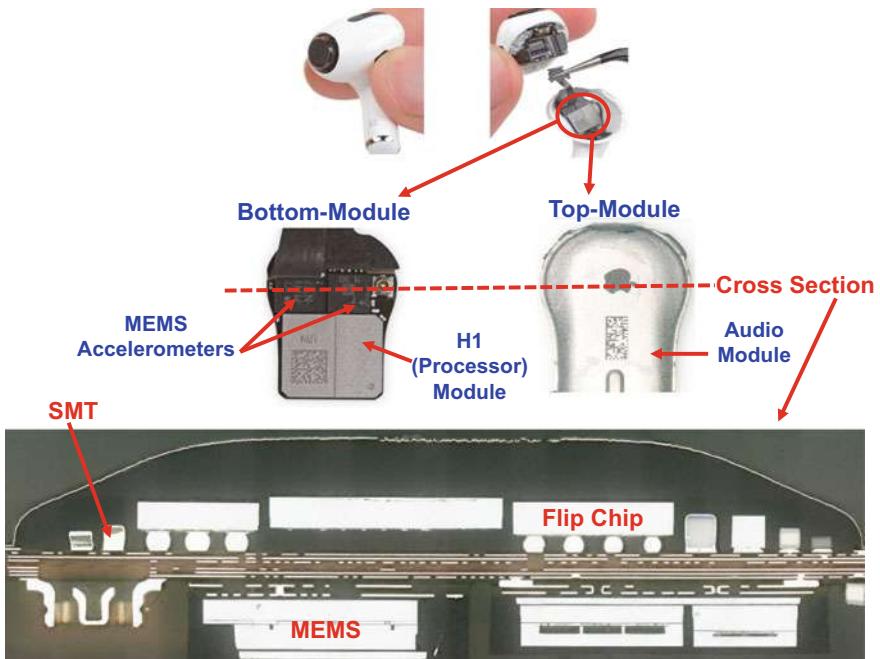


Fig. 2.4 Apple's TWS (true wireless stereo) AirPods Pro

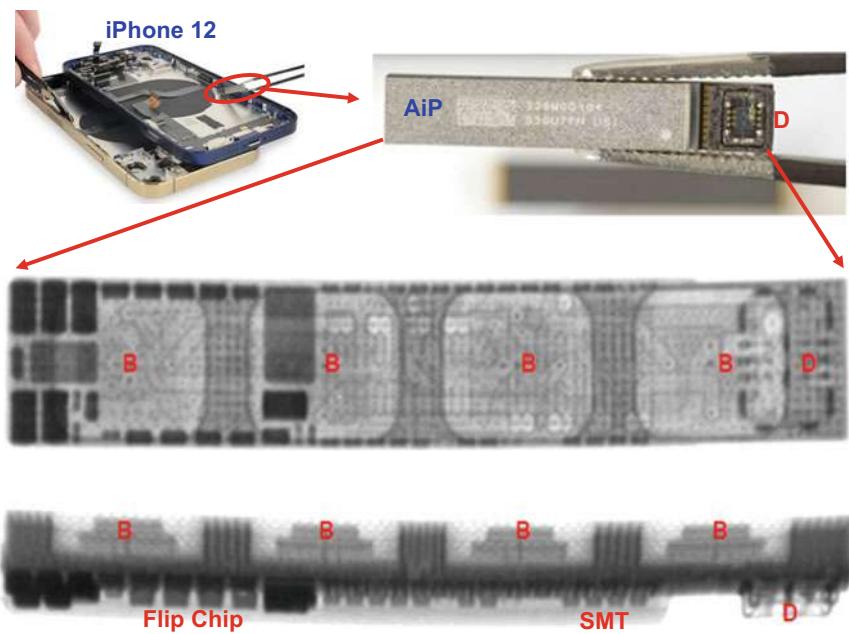
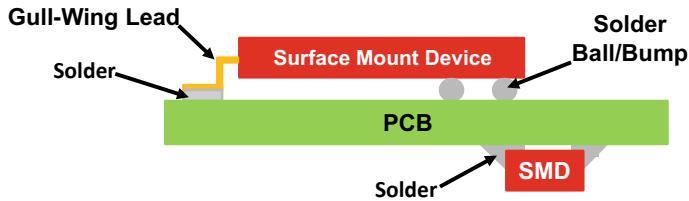


Fig. 2.5 SiP: AiP in iPhone 12



**Fig. 2.6** Schematic of an SMT assembly (two-side assembly)

## 2.7 SMT

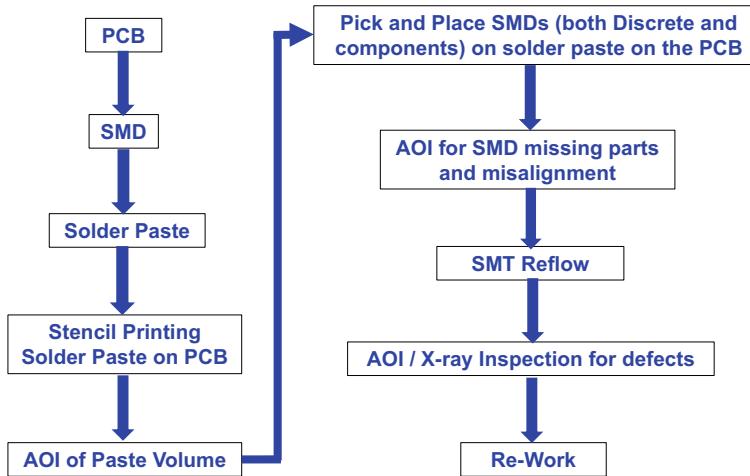
As mentioned earlier, SMT is one of the major assembly technologies for SiP. SMT is a very mature technology [112, 113]. SMT allows placement of more SMD (surface mount devices) into smaller and tighter printed circuit board (PCB) areas. The increased density means increased performance and power in smaller packaging system, and allows manufacturing of smaller and higher performance products at lower cost. Also, SMT allows two-side assembly. Figure 2.6 schematically shows a SMT assembly and Fig. 2.7 shows an actual SMT PCB assembly. Figure 2.8 shows the key elements and process steps in SMT and they will be discussed in the following sections.

### 2.7.1 PCB

A typical PCB is shown in Fig. 2.9a. Most of the PCBs are made from the FR (flame retardant)-4, which is a composite material composed of woven fiberglass cloth with an epoxy resin binder [glass-reinforced epoxy resin laminate as shown in Fig. 2.9b] that is flame resistant. A PCB consists of conductor, trace, track, route, etc.

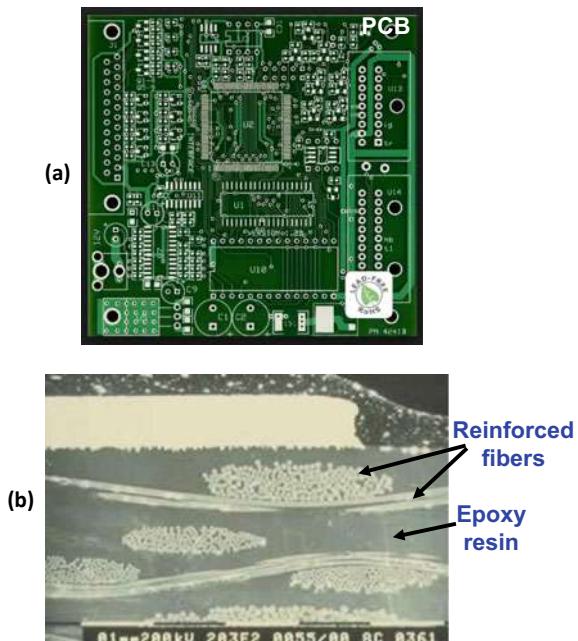


**Fig. 2.7** Typical example of PCB assembly



**Fig. 2.8** Key elements in SMT

**Fig. 2.9** Printed circuit boards



as shown in Fig. 2.10. There are microstrip lines which lay on the surface of the PCB and strip lines which lay in the interior (internal layers) of a PCB. Figure 2.11 shows various kinds of PCB structures such as the single-side, double-sides, multilayers, etc.

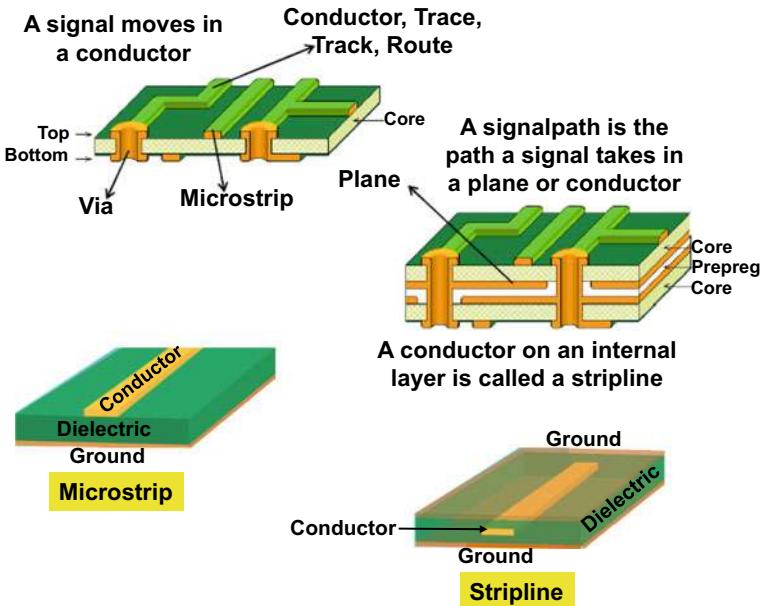
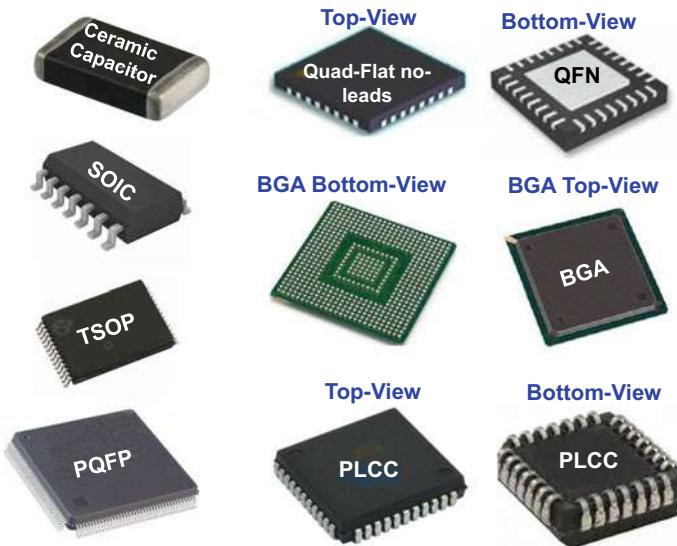


Fig. 2.10 Conductor, trace, track, route, etc. on a PCB

Pattern	Layer	Schematic
Single-sided	One signal layer	
Double-sided	Two signal layers	
Multilayer	Two signal layers and two power layers	
Multilayer	Four signal layers and two power layers	
Multilayer	Two signal layer and two power layer	

Fig. 2.11 Cross sections of PCB



**Fig. 2.12** Examples of SMDs

Nowadays, it is not uncommon to have a PCB with more than 100 layers. However, usually 30–60 layers are the maximum.

### 2.7.2 SMDs

There are many SMDs [113]. Figure 2.12 shows some of the common SMDs. The discrete components such as the capacitors and resistors are the most used SMDs in an electronic product. Today, the smallest capacitor is  $0.25 \text{ mm} \times 0.125 \text{ mm} \times 0.125 \text{ mm}$ . The SOIC (small outline integrated circuit), TSOP (thin small outline package), and PQFP (plastic quad flat pack) are with gull-wing leads. The pitch of the SOIC is 1.27 mm, of the TSOP is 0.65 mm, and of the PQFP is 0.4 mm. The PLCC (plastic leaded chip carrier) is with J-leads and the pitch is 1.27 mm. PBGA (plastic ball grid array) is with an organic package substrate and solder balls. The ball-pitch is going down to 0.35 and even 0.3 mm. The QFN (quad-flat no-leads) is no leads and the pitch is 0.5 mm.

### 2.7.3 Solder Paste

A solder paste consists of powdered metal solder suspended in a thick medium called flux as shown in Fig. 2.13. Flux is added to act as a temporary adhesive, holding the



**Fig. 2.13** Solder paste

components until the soldering process melts the solder and makes a stronger physical connection.

According to JEDEC standard J-STD-004 “Requirements for Soldering Fluxes”, solder pastes are classified into three types based on the flux types. Rosin based pastes are made of rosin, a natural extract from pine trees. These fluxes need to be cleaned after the soldering process using a solvent (potentially including chlorofluorocarbons). Rosin fluxes are no longer predominant. Water soluble fluxes are made up of organic materials and glycol bases. There is a wide variety of cleaning agents for these fluxes. No-clean flux is made with resins and various levels of solid residues. No-clean pastes save not only cleaning costs, but also capital expenditures and floor space. However, these pastes need a very clean assembly environment and may need an inert re-flow environment.

According to IPC standard J-STD-005, the types of solder pastes are classified based on the solder metal powder (particle) size as shown in Table 2.1. For example, the powder size of Type 4 will have less than 0.5% of the nominal diameter are larger than 50  $\mu\text{m}$ , no more than 10% of the nominal diameter are between 38 and 50  $\mu\text{m}$ , more than 80% of the nominal diameter are between 20 and 38  $\mu\text{m}$ , and no more than 10% of the nominal diameter are less than 20  $\mu\text{m}$ . Today, types 3, 4, and 5, especially type 4 are the most common used solder pastes.

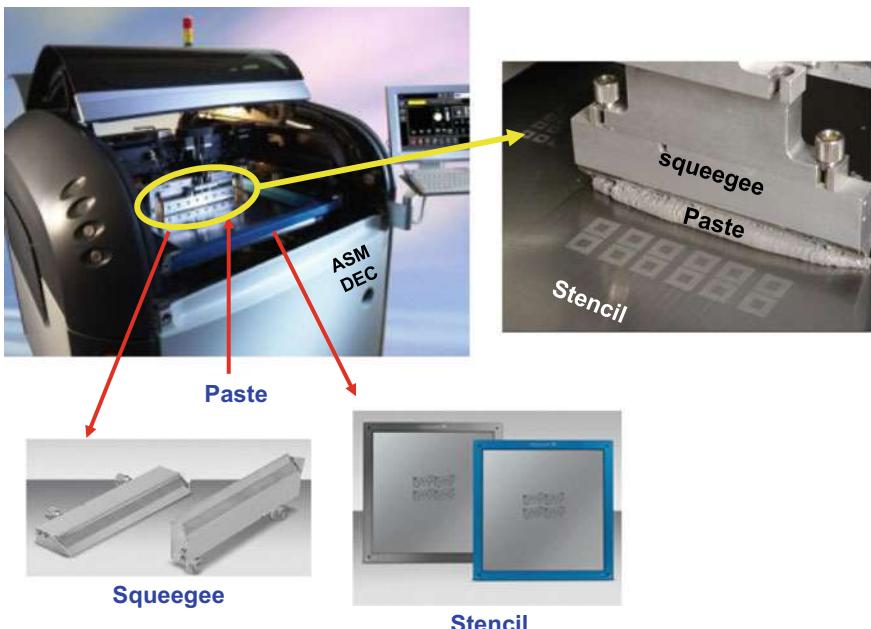
**Table 2.1** Types of solder paste

Type	Less than 0.5% larger than	10% max between	80% min between	10% max less than
1	160	150–160	75–150	75
2	80	75–80	45–75	45
3	60	45–60	25–45	25
4	50	38–50	20–38	20
5	40	25–40	15–25	15
6	25	15–25	5–15	5
7	15	11–15	2–11	2

The units in columns 2–4 are in  $\mu\text{m}$

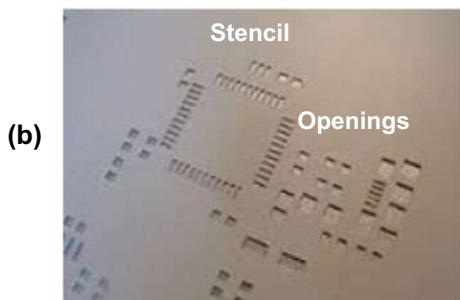
#### 2.7.4 Stencil Printing Solder Paste and AOI

For SMT, stencil printing solder paste on PCB is a very important process step. Figure 2.14 shows a stencil printing system which consists of the solder paste, stencil, and squeegee. Figures 2.15a, b show the stencils, which are made of stainless steel with openings. Figure 2.16a shows the solder paste printed on the pads of a 0.3 mm-pitch PQFP on PCB. Figure 2.16b shows the solder paste printed on the pads of a 0.4 mm-pitch PBGA on PCB.

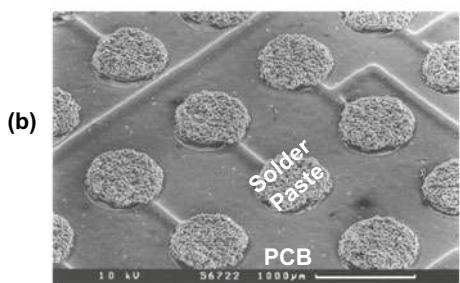
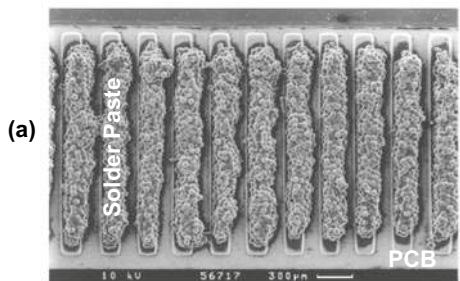


**Fig. 2.14** Typical stencil printing system

**Fig. 2.15** Typical stencils



**Fig. 2.16** **a** Solder paste on the pads of a 0.3 mm-pitch PQFP on PCB. **b** Solder paste on the pads of a 0.4 mm-pitch PBGA on PCB



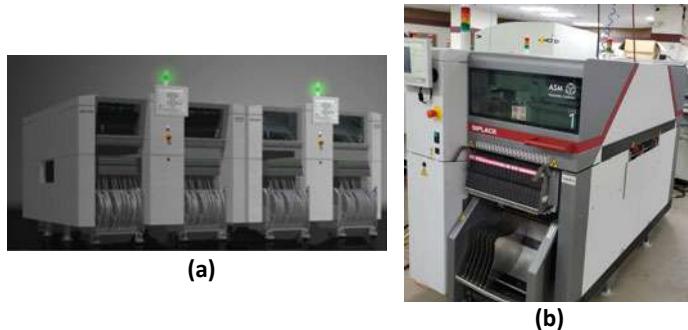
**Table 2.2** Solder paste volumes for various PBGA pad pitches

Pitch (mm)	Spot/pad size μm (mils)	Volume (mil <sup>3</sup> )			
		Stencil/height			
		2 mil (50 μm)	3 mil (75 μm)	4 mil (100 μm)	5 mil (125 μm)
0.5	300 (11.8)	218	327	436	545
0.5	275 (10.8)	184	276	368	460
0.4	250 (9.8)	150	225	300	450
0.35	200 (7.8)	96	144	192	288
0.3	188 (7.5)	89	133.2	177.6	222
0.25	150 (5.9)	55	82	109	137

The effect of stencil thickness (height) on the solder paste volume on PBGA with various pad pitches has been calculated by Intel [114] and is shown in Table 2.2. It can be seen that for a PBGA with 0.4 mm-pitch the stencil thickness should be 100 μm in order to have a solder paste volume ( $300 > 250$  m<sup>3</sup>). Intel showed that from a solder joint quality/reliability points of view, as the PBGA solder ball pitch decreases the contribution of the solder joint quality/reliability from solder paste increases. Thus, beside in design for solder joint quality/reliability, automated optical inspection (AOI) to control the solder paste volume is also very important. Figure 2.17 shows an AOI machine for solder volume inspection.

There are many functions of the AOI for solder paste volume. If most of the printed solder paste volumes don't meet the specification by AOI, then the solder paste on the PCB should be washed away, cleaned, dried, and do the stencil printing of the solder paste on the PCB again. On the other hand, if there are only a few SMDs

**Fig. 2.17** A typical AOI system for solder volume inspection



**Fig. 2.18** **a** A chip shooter. **b** A SMD components pick and place machine

don't meet the paste volume specification, then tell the computer system (next AOI or x-ray inspection) to pay special attention to these few SMDs after pick & place and reflow.

### 2.7.5 *Pick and Place of SMDs*

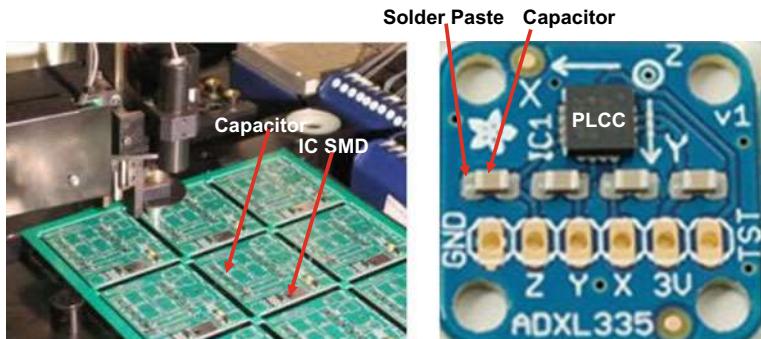
Usually, there are two groups of SMDs, one is the discrete SMDs such as the capacitors and resistors, and the other is the IC components such as the PQFP, PBGA, QFN, etc. Usually, the discrete SMDs are pick and placed (P&P) by a high-speed chip shooter as shown in Fig. 2.18a and the IC components are P&P by high-speed placement machine as shown in Fig. 2.18b.

### 2.7.6 *AOI of SMDs on PCB*

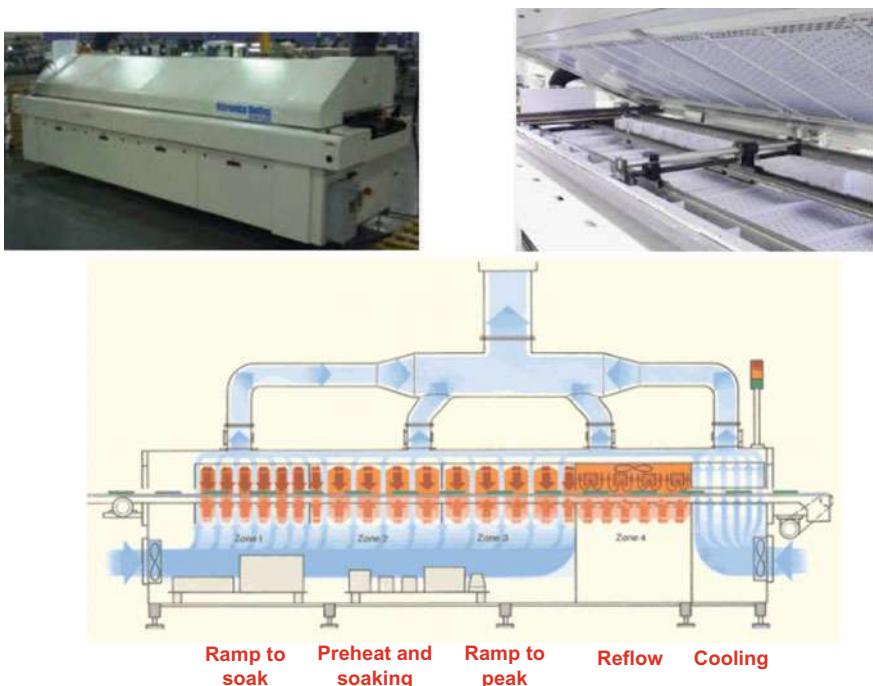
After the P&P of SMDs on the solder paste on the pads of SMDs on the PCB as shown in Fig. 2.19, another AOI should be performed. This is for the missing SMDs, misplacing, and off-placement SMDs. These data are very important for the AOI and x-ray inspection after solder reflow.

### 2.7.7 *SMT Solder Reflow*

SMT solder reflow is the most important process step in SMT. Figure 2.20 shows a typical solder reflow oven, which comes with 6 heating-zones, 8-zone, 10-zone, or 12-zone. According to IPC/JEDEC J-STD-020C Lead-Free Reflow Profile, the functions of a solder reflow oven are to: (a) ramp to soak the SMDs, solder paste,



**Fig. 2.19** Typical PCBs with solder paste and SMD components



**Fig. 2.20** Typical reflow oven

and PCB, (b) preheat and soak the SMDs, solder paste, and PCB, (c) ramp up the temperature to the peak, (d) reflow the solder paste, and (d) cool down the solder joint, SMDs, and PCB. Figure 2.21 shows the temperature profile versus time when the PCB assembly is in the oven. It can be seen that the temperature is ramping up from room temperature to 150 °C to soak the SMDs, solder paste, and PCB. Then, the temperature is increasing from 150 to 200 °C to preheat and soak the SMDs,

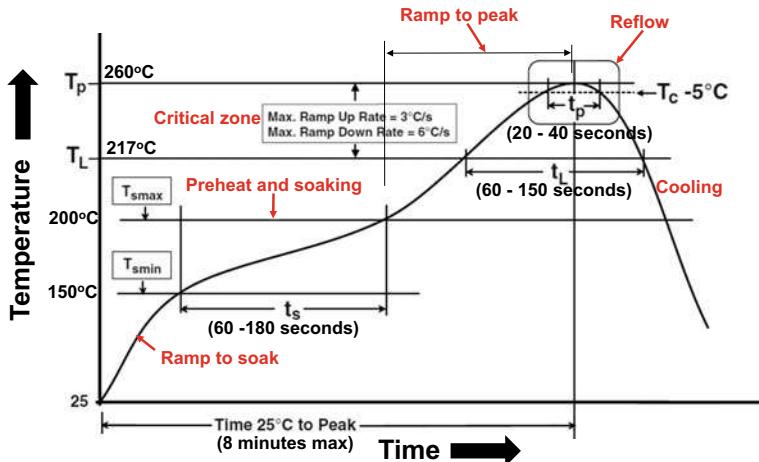


Fig. 2.21 IPC/JEDEC J-STD-020C Lead-Free Reflow Profile

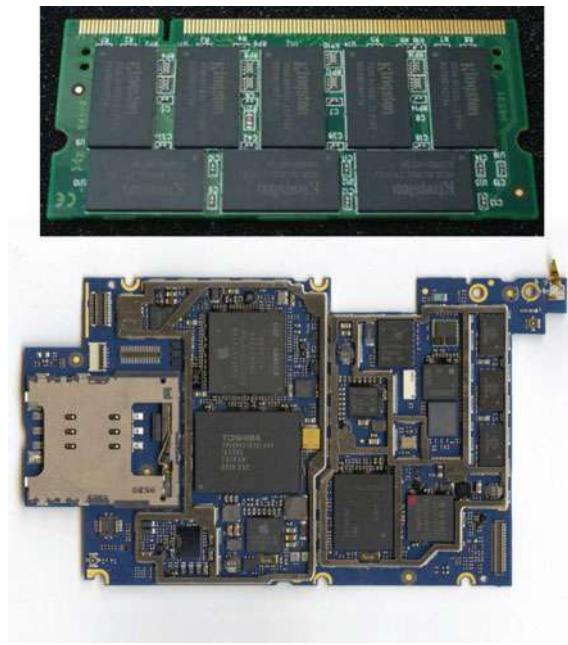
solder paste, and PCB. It is followed by ramping the temperature from 200 °C to the peak (260 maximum) at a maximum rate = 3 °C/s, then solder reflow. After that, the temperature is cooling down from 260 to 217 °C to let the solder joint solidify at a maximum ramp down rate = 6 °C/s. The total time for the PCB assembly in the oven from room temperature to the peak temperature is no more than 8 min. Figure 2.22 shows some PCB assembly.

### 2.7.8 AOI and X-Ray Inspection for Defects

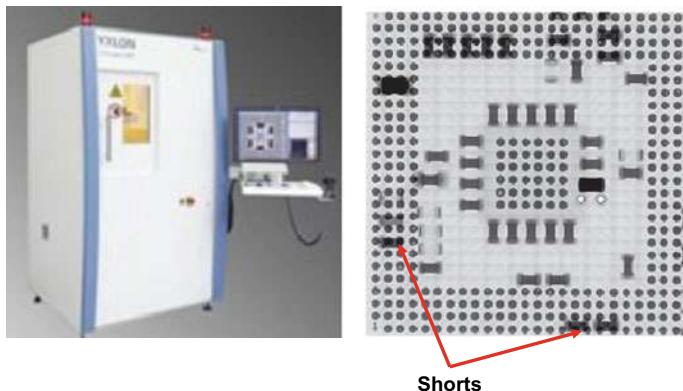
After solder reflowed, it is time to perform a quick AOI for the missing SMDS and off-placement SMDs and a detailed X-ray inspection (Fig. 2.23) for the defects shown in Fig. 2.24. Usually, the x-ray inspection can find out at least 6 different defects, namely open, excess solder, insufficient reflow, short, void, and misalignment.

### 2.7.9 Re-Work

The PCB assembly with defects is re-worked at a re-work station such as the SRT Summit 2100RD shown in Fig. 2.25. It can be seen that the bottom and top heaters reflow solder to remove components with PBGA, gull wing leaded PQFPs, and bottom termination components. Also, the paste dispenser allows placement of precise paste dots.



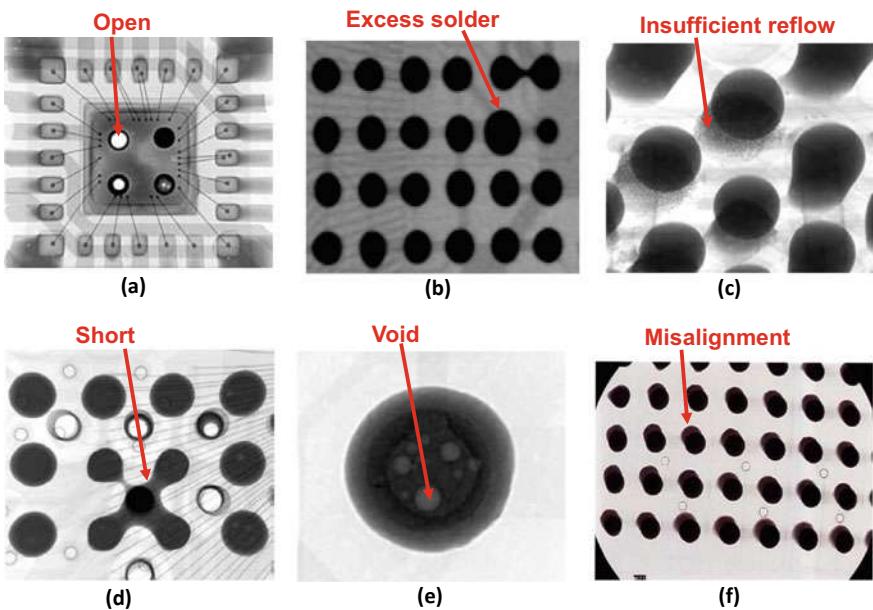
**Fig. 2.22** Typical examples of reflowed PCB assemblies



**Fig. 2.23** X-ray inspection

### 2.7.10 Summary and Recommendation

Some important result and recommendation are summarized in the follows.



**Fig. 2.24** Possible solder joint defects inspected by x-ray machine

**Fig. 2.25** Typical re-work station



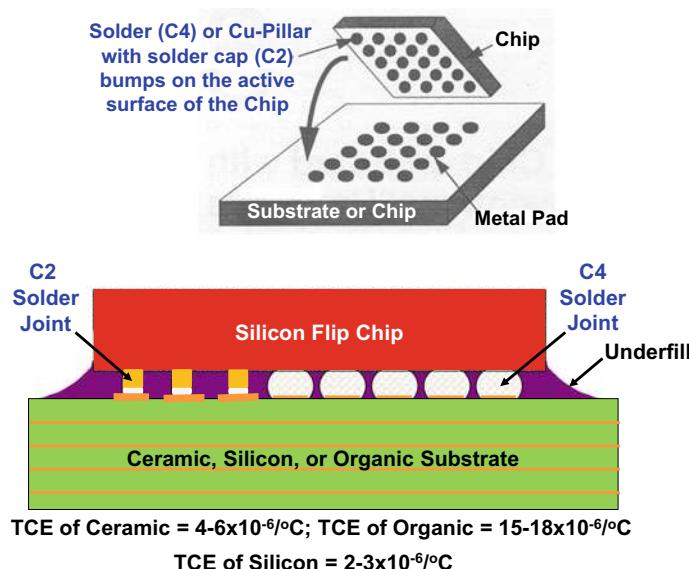
- The major elements and process steps such as PCB, SMD, solder paste, stencil printing solder paste and AOI, P&P of SMDs, SMT solder reflow, AOI and x-ray inspection for defects, and rework in SMT have been provided.
- SMT has been given the designers of modern consumer, commercial, and military electronic systems a remarkable flexibility/convenience to interconnect electronic components. The characteristics of SMT have facilitated board assembly choices

that have fueled creative applications to advance technology. SMT is one of God's gives to electronic industry.

- The trends of SMT are automation, miniaturization, performance, reliability, efficiency, and environmental friendly.

## 2.8 Flip Chip Technology

As mentioned earlier, flip chip technology is one of the major assembly technologies for SiP. Flip chip technology is a very mature technology [115–120]. It was introduced by IBM in the early 1960s for their solid logic technology, which became the logical foundation of the IBM System/360 computer line [119]. The so-called C4 (controlled-collapse chip connection) technology [120] utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the (ceramic, silicon, or organic) substrate, and all solder joints are made simultaneously by reflowing the solder as shown in Fig. 2.26. In this book, for flip chips, even the solder bumps are not made from high-lead solder; we also call them C4 technology. In this section, four different flip chip assembly processes will be briefly discussed. Also, a high throughput thermal compression bonding flip chip process will be provided. Since wafer bumping is the mother of flip chip technology, wafer bumping by stencil printing and electroplating will be briefly mention first.

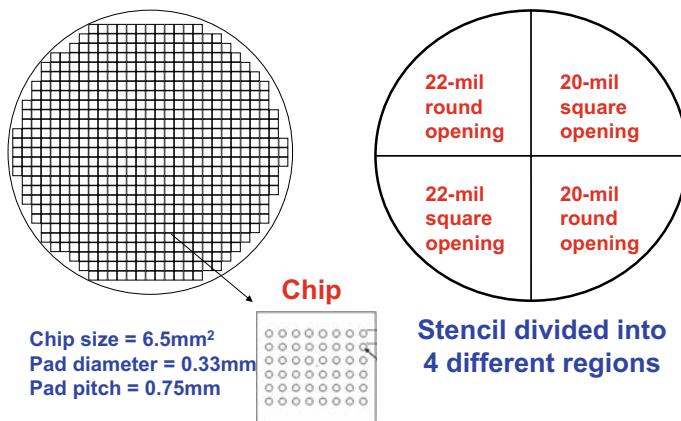


**Fig. 2.26** Flip chip assembly with C4 bumps and/or C2 bumps

### 2.8.1 Wafer Bumping by Stencil Printing

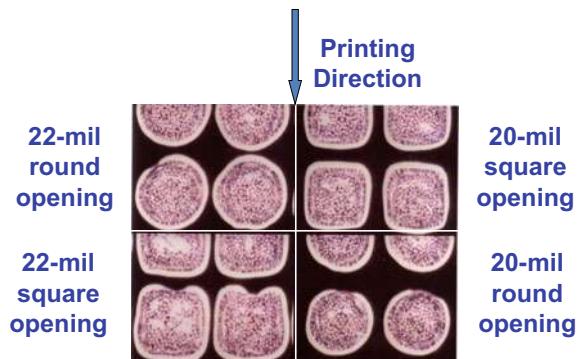
Wafer bumping by stencil printing is the simplest method and will be briefly mentioned [121]. The wafer used is an 8" (200 mm) wafer which is shown in Fig. 2.27. It can be seen that there are 48 pads for each chip and the pad pitch is 0.75 mm. The pad diameter is 0.33 mm with a Cu-stud about 60  $\mu\text{m}$  tall. The stencil is an 8 mil (0.2 mm) thick stainless steel sheet drilled with a phase-quadrupled Nd:YAG laser system made by LPKF. The stencil is then electro-polished in a 30% potassium hydroxide solution as shown in Fig. 2.27. It can be seen that the first quadrant is with 20 mil square opening, the second quadrant is with 20 mil round opening, the third quadrant is with 22 mil square opening, and the fourth quadrant is with 22 mil round opening. The targeted solder-bump height on the wafer is 13 mils (0.33 mm).

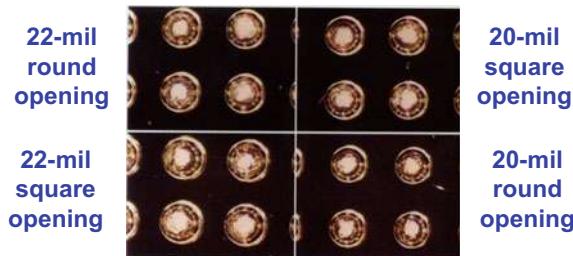
The typical printed solder paste results in each quadrant are shown in Fig. 2.28. The solder pastes on the wafers are reflowed in a DIMA reflow oven with the SMT



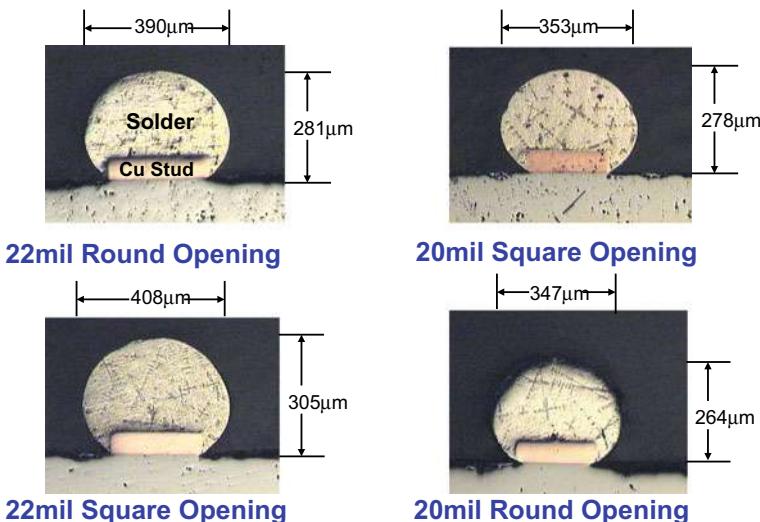
**Fig. 2.27** Wafer bumping with stencil printing

**Fig. 2.28** The printed solder paste on a wafer





**Fig. 2.29** The printed solder paste on a wafer after reflowed

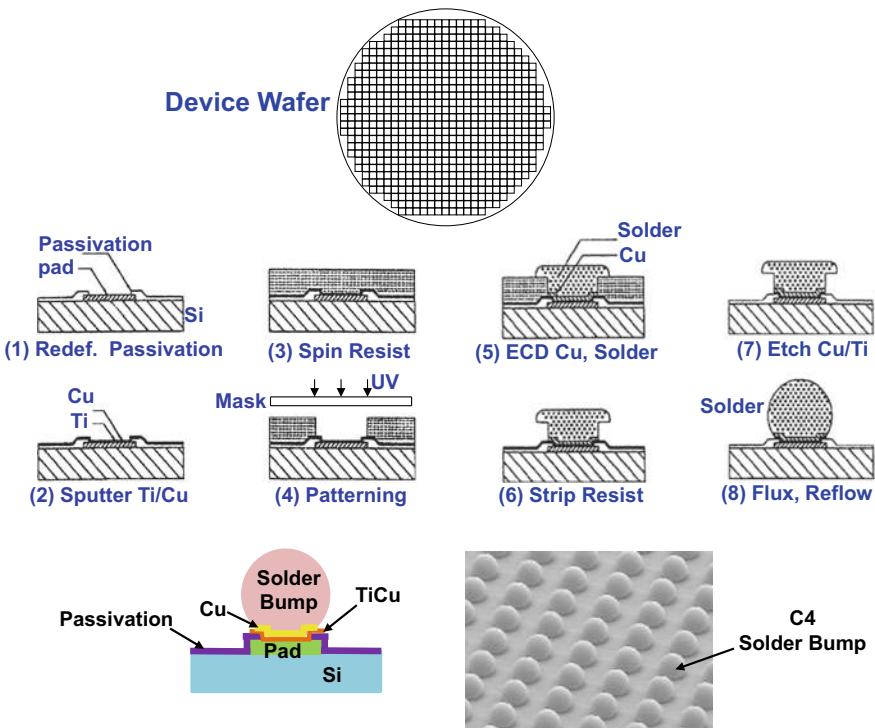


**Fig. 2.30** Cross sections of the reflowed solder bumps by stencil printing

compatible reflow temperature profile. Figure 2.29 shows the solder bumps with different stencil openings, while Fig. 2.30 shows their cross sections. It can be seen that the largest cross sections are from the stencil with 22 mil square openings and the smallest cross sections are from the stencil with 20 mil round openings. The cross sections are about the same for both the 22 mil round openings and the 20 mil square openings. Data analysis of the L4 and L8 Taguchi experiments can be found in [121].

### 2.8.2 C4 (Controlled Collapse Chip Connection) Wafer Bumping

Figure 2.31 shows the C4 wafer bumping process by electroplating. Usually the pad size is equal to 100  $\mu\text{m}$  and the target bump height is equal to 100  $\mu\text{m}$ . After redefining the passivation opening (usually it is not required), either Ti or TiW (0.1–0.2  $\mu\text{m}$ ) are sputtered over the entire surface of the wafer first, followed by 0.3–0.8  $\mu\text{m}$  of Cu. Ti–Cu and TiW–Cu are called under bump metallurgy (UBM). In order to obtain 100  $\mu\text{m}$  bump height, a 40  $\mu\text{m}$  layer of resist is then overlaid on the Ti–Cu or TiW–Cu and a solder bump mask is used to define (ultraviolet exposure) the bump pattern as shown in steps (1)–(4) in Fig. 2.31. The opening in the resist is 7–10  $\mu\text{m}$  wider than the pad opening in the passivation layer. A 5  $\mu\text{m}$  layer of Cu is then plated over the UBM, followed by electroplating the solder. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the target (100  $\mu\text{m}$ ), the solder is plated over the resist coating by about 15  $\mu\text{m}$  to form a mushroom shape. The resist is then stripped off and the Ti–Cu or TiW–Cu is removed with a hydrogen peroxide or plasma etching. The

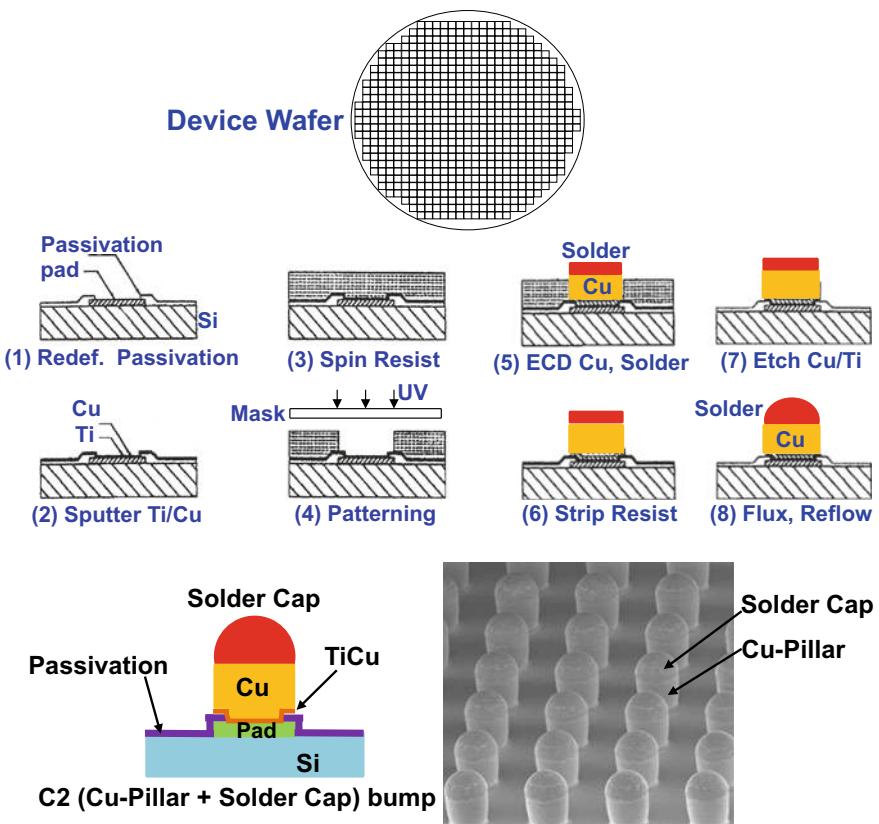


**Fig. 2.31** C4 wafer bumping with electroplating

wafer is then reflowed with flux, which creates smooth truncated spherical solder C4 bumps as shown in Fig. 2.31.

### 2.8.3 C2 (Chip Connection) Wafer Bumping

Because of higher pin-count and tighter pitch (smaller spacing between pads), there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [122] and Cu-pillar with solder cap [123, 124] can be a solution. The fabrication process is basically the same as that of the C4 bumps except electroplating the Cu instead of solder as shown in step (5) of Fig. 2.32. It is followed by electroplating the solder cap and then reflowing the solder with flux, which creates the C2 (Cu-pillar + solder cap) bumps as shown in Fig. 2.32. Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the

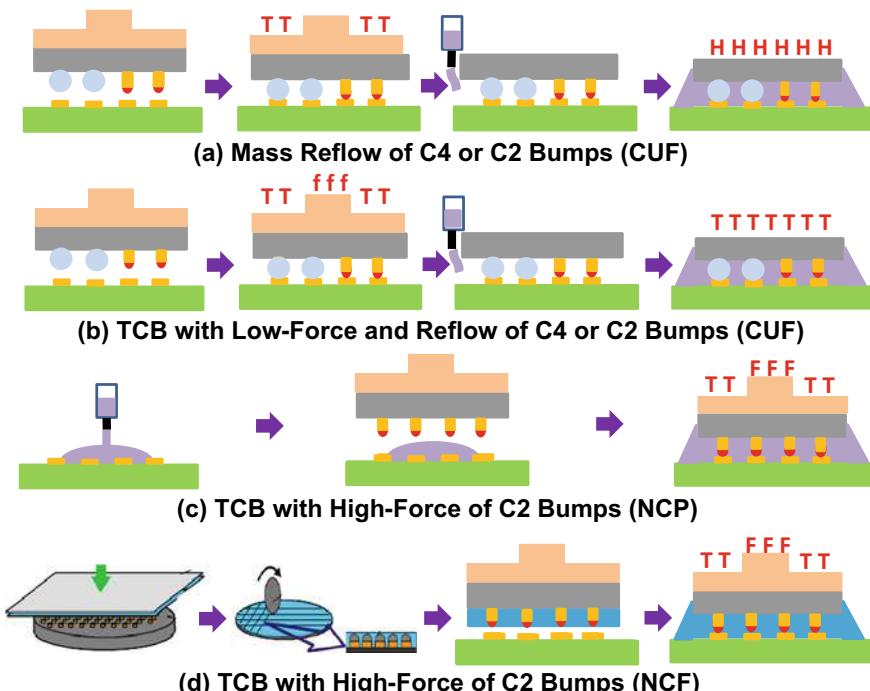


**Fig. 2.32** C2 wafer bumping with electroplating

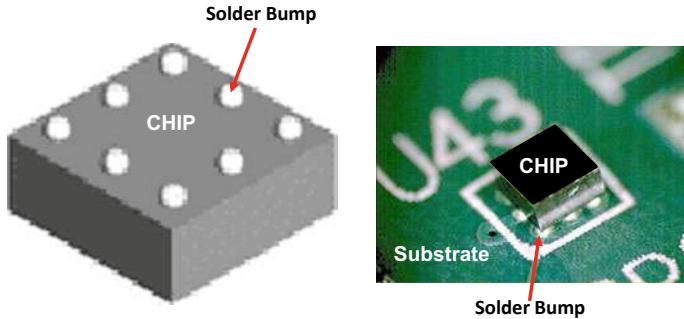
Cu pillar with the solder cap bump and therefore, it is called a C2 (chip connection) bump. Besides being able to handle finer pitch, C2 bumps also provide better thermal and electrical performances than C4 bumps. This is because the thermal conductivity ( $\text{W/m K}$ ) and electrical resistivity ( $\mu\Omega\text{m}$ ) of Cu (400 and 0.0172) are superior to those (55–60 and 0.12–0.14) of solder.

#### 2.8.4 Flip Chip Assembly—Mass Reflow of C4 or C2 Bumps (CUF)

Figure 2.33 shows four different processes in assembling flip chips on mainly organic substrate. Figure 2.33a shows the flip chip assemblies with mass reflow of C4 or C2 solder bumps. This is the most employed flip chip assembly process. First, use a lookup and look-down camera to identify the location of the bumps on the chip and the pads on the substrate; second, apply flux on either the C4 bumps, or the substrate, or both; and third, pick and place the C4 bumped chips on the substrate, then mass



**Fig. 2.33** Flip chip assembly processes (mainly on organic substrate): **a** mass reflow of C4 or C2 bumps (CUF), **b** TCB with low-force and reflow of C4 or C2 bumps (CUF), **c** TCB with high-force of C2 bumps (NCP), and **d** TCB with high-force of C2 bumps (NCF)



**Fig. 2.34** Flip chip assembly with mass reflow of C4 bumps

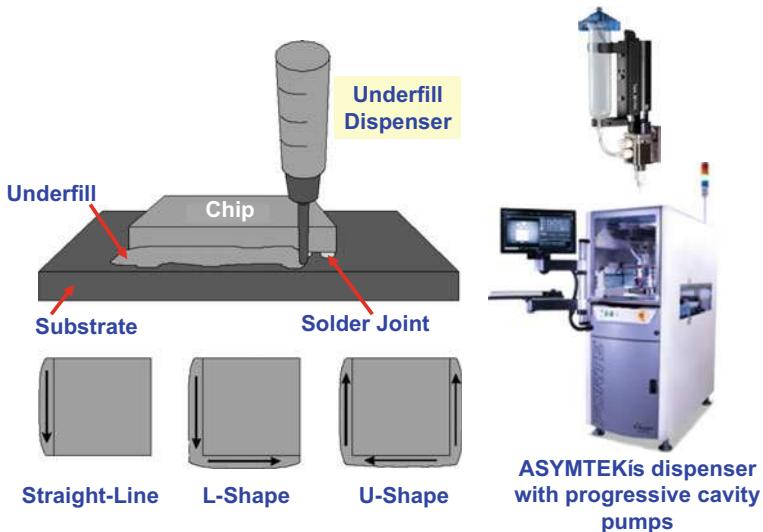
reflow with temperature T-profile such as the that shown in Fig. 2.21. Because of the surface tension of the C4 solder bumps during reflow, the process is very robust (self-alignment) as shown in Fig. 2.34.

In the past few years, solder mass reflow of C2 (Cu-pillar with solder cap) bumped chips on organic package substrates has been tried for high pin-count and fine-pitch flip-chip assemblies. The assembly process, Fig. 2.33a, is exactly the same as that of the C4 bumps, but the self-alignment characteristic is nowhere near the same.

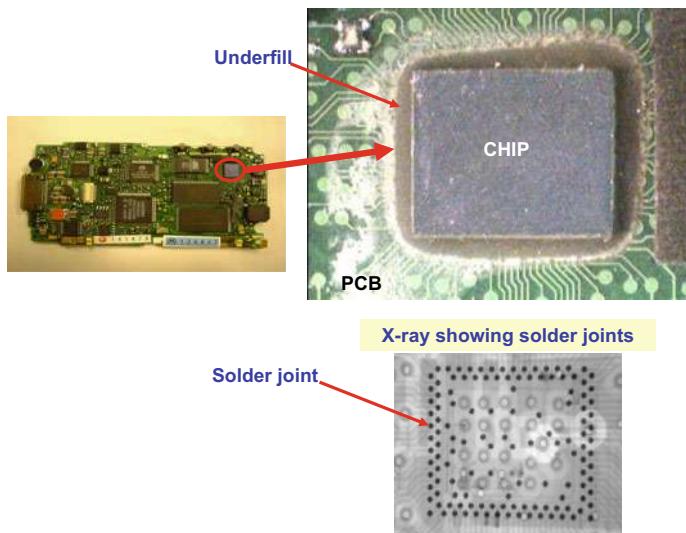
### 2.8.5 Underfill for Reliability

The reliability of flip chip solder joints is enhanced by the application of underfill [125–148], especially on organic substrate. Most underfills consist of low-expansion fillers such as fused silica ( $\text{SiO}_2$ ) and a liquid prepolymer such as thermosetting resin (adhesive) that can be cured to a solid composite. In 1987, Hitachi showed that with underfill, the thermal fatigue life of the flip chip solder joints on ceramic substrate increased [125]. In 1992, IBM at Yasu proposed the use of the low-cost organic substrate instead of the high-cost ceramic substrate for flip chip assemblies [126–128]. They showed that with underfill, the large thermal expansion mismatch between the silicon chip ( $2.5 \times 10^{-6}/^\circ\text{C}$ ) and the organic substrate ( $15\text{--}18 \times 10^{-6}/^\circ\text{C}$ ) is reduced substantially and the solder joints are reliable for most applications.

Figure 2.35 shows the application of underfill dispensing and the equipment. It can be seen that the underfill can be dispensed from the needle of the equipment. The underfill can be dispensed to one side, two sides, or three sides of the chip and wait for the underfill to flow through the gap between the chip and the substrate by capillary action. That's why this is also called CUF (capillary underfill). Don't apply the underfill to four sides of the chip because it will create a central void between the chip and the substrate. Today, in many applications, people only dispense underfill on one side and wait for the underfill to come out from the opposite side and then dispense the underfill again on the opposite side. Figures 2.36 and 2.37 show some

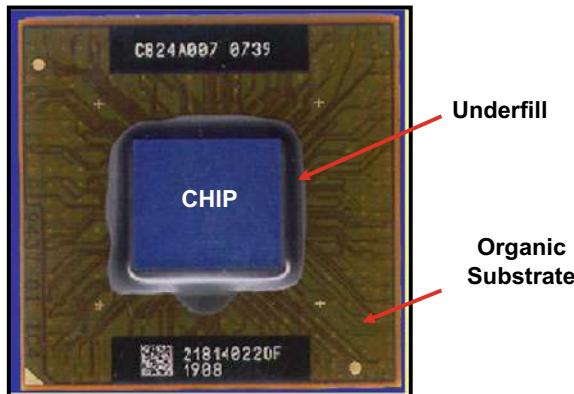


**Fig. 2.35** Underfill dispensing process and equipment

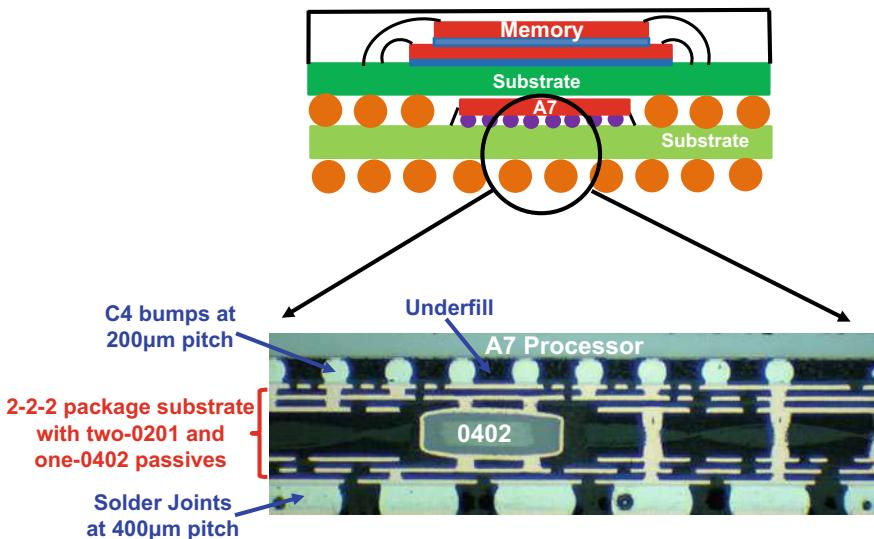


**Fig. 2.36** Flip chip assembly with mass reflow of C4 bumps and underfill

examples of underfilled chips after cured. Figure 2.38 shows the cross section of iPhone 6 Plus (September 2015). It can be seen that the A7 application processor is housed in a PoP (package-on-package) format and the solder bumped flip chip is mass reflowed and underfilled on a 2-2-2 organic package substrate.



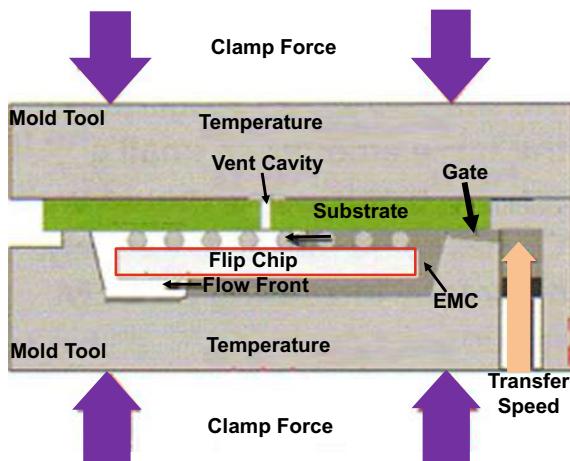
**Fig. 2.37** Flip chip assembly with C4 bumps and underfill



**Fig. 2.38** Flip chip assembly of Apple's application processor with C4 bumps and underfill

Besides CUF, there is the molded underfill (MUF), which was first proposed by Cookson Electronics [149] in 2000 and later by, e.g., Dexter [150], Intel [151], Amkor [152], STATSChipPAC [153], and LETI/STMicroelectronics [154]. For MUF, the modified epoxy molding compound (EMC) is transferred molding the chip and filling the gap between the chip, solder joints, and the substrate of the flip chip assembly as shown in Fig. 2.39. The encapsulant of the chip and the underfill are formed at the same time, which will increase the throughputs. However, the challenges of MUF are: (a) the flow of MUF between the chip and the substrate is usually assisted by vacuum, (b) the size of the silica filler of the EMC must be very small for flowability,

**Fig. 2.39** Schematic of molded underfill(MUF)



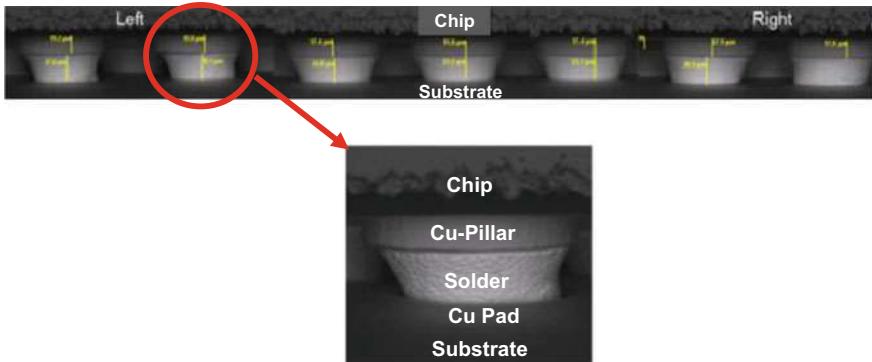
(c) the cost of EMC for MUF is much higher than that for package molding, (d) package warpage is an issue due to the thermal expansion mismatch between the EMC, chip, and substrate, (e) the molding temperature is limited by the melting point of the solder joints, and (f) the standoff-height and pitch of the solder joints cannot be too small.

Another method to increase the throughputs of CUF and avoid the drawbacks of MUF is to design a stencil for printing (instead of dispensing) the underfill material for flip chip assemblies. This topic is out of the scope of this book and the readers can go to [155] for more information.

### 2.8.6 *Flip Chip Assembly—TCB with Low-Force of C4 or C2 Bumps (CUF)*

Recently, because of the requirements of higher functionalities of the chips and shrinking the chips' area, the number of pin-outs of the processors, ASICs (application specific integrated circuits), and memories increases and their pitch (or the spacing between the pin-out pads) decreases. Also, because of the trends of smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and lower profile package substrates lead to the necessity of the thermocompression bonding (TCB) method for flip-chip assemblies.

Figure 2.33b shows the TCB with low-force of flip chip assembly of C4 or C2 bumps with CUF. First, use the look-up and look-down camera to locate the position of the C4 or C2 bumps on the chip and their corresponding pads on the substrate; second, apply flux on the solder bump (or solder cap) or on the substrate or both;



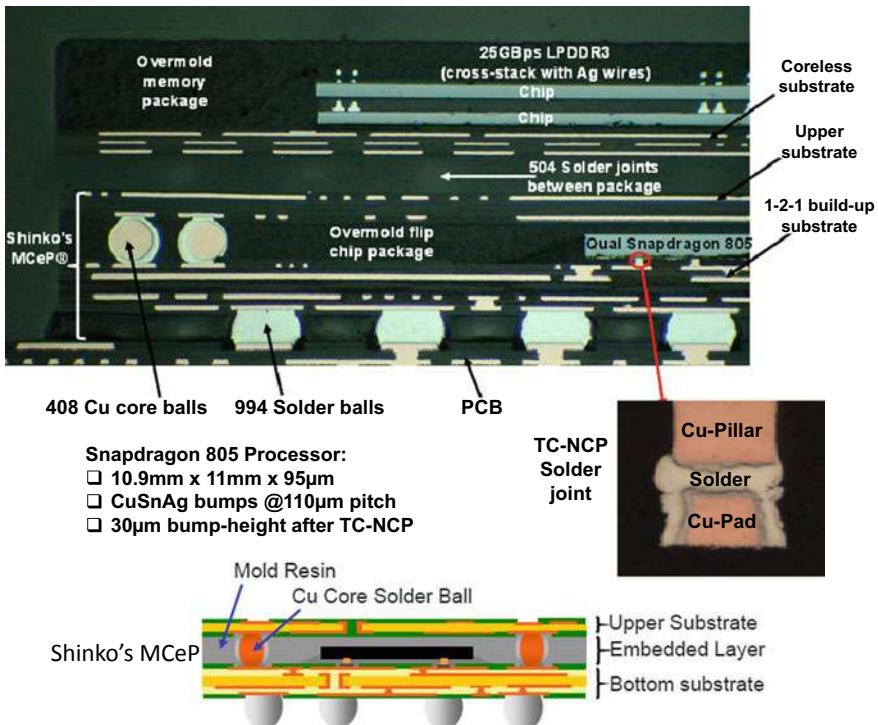
**Fig. 2.40** Flip chip assembly with TCB with low-force and reflow of C2 bumps (CUF) [156]

and third, pick-and-place the chip on the substrate and then apply temperature ( $T$ ) to melt the solder and a low force ( $f$ ) to hold the chip at a certain distance from the substrate. Finally, dispense and cure the CUF. The above procedure is done one chip at a time and therefore, the throughput is low in comparison with the C4 (or C2) solder mass reflow process. Figure 2.40 shows a typical cross section of a flip chip assembly with TCB with low force on C2 bumps [156].

Both mass reflow of C4 or C2 bumps (CUF) and TCB with low-force and mass reflow of C4 or C2 bumps (CUF) are examples of post-assembly underfill, i.e., the application of underfill is after the flip chip assembly.

### 2.8.7 *Flip Chip Assembly—TCB with High-Force of C2 Bumps (NCP)*

Figure 2.33c shows the TCB with high-force of C2 bumps with NCP (non-conductive paste). For pre-assembly underfill, the application of underfill is either on the substrate or chip and is before the flip-chip assembly. High-bonding force TCB of the C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate, Fig. 2.33c was first studied by Amkor [157] and has been used to assemble Qualcomm's SNAPDRAGON application processor for Samsung's Galaxy smartphone as shown in Fig. 2.41. The NCP underfill can be spun on, dispensed by a needle, or vacuum assisted.



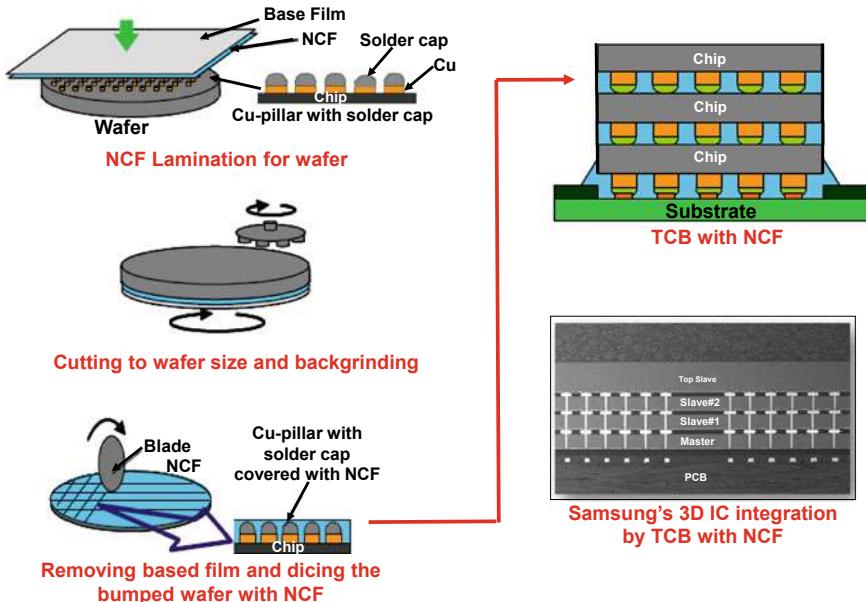
**Fig. 2.41** Flip chip assembly with TCB with high-force of C2 bumps (NCP) [157]

### 2.8.8 *Flip Chip Assembly—TCB with High-Force of C2 Bumps (NCF)*

Another example of pre-assembly underfill is shown in Fig. 2.33d, which use TCB with high-force of flip chip with C2 bumps and with NCF (non-conductive film). Figure 2.42 shows the lamination of NCF on the C2 (Cu-pillar with a solder cap) bump wafer. High-bonding force TCB of the individual C2 chips with NCF (after singulation from the laminated wafer) has been in production for 3D IC integration by Samsung on its TSV-based double data rate type 4 dynamic random access memory (DRAM) as shown in Fig. 2.42.

### 2.8.9 *An Advanced Flip Chip Assembly—LPC TCB of C2 Bumps*

TCB with either low-force, Fig. 2.33b, or high-force, Fig. 2.33c, is very effective for flip chips with fine-pitch, high-pincount, thin-chip, and thin-substrate packages.



**Fig. 2.42** Flip chip assembly with TCB with high-force of C2 bumps (NCF)

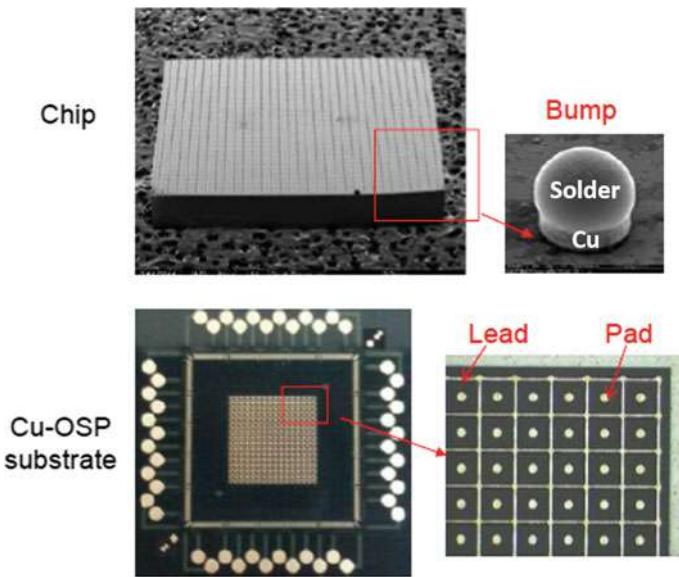
However, low throughput is an issue. In this section, a new TCB-flux process, namely liquid phase contact (LPC) TCB approach is presented [158]. The significant difference between the LPC TCB process and the traditional TCB-flux process is that the solder cap on the copper pillar of the C2 bump is heated to a molten state before contacting the bond pad/lead on the substrate under a small force. The bonding cycle time for LPC TCB process with or without bond head (BH) cooling step is greatly reduced compared with the traditional TCB-flux process, therefore a high throughput assembly process could be achieved. Another advantage of LPC TCB process is that the solder joint thickness (stand-off height) after assembly could be precisely controlled, which is very important for the solder joint reliability.

#### (A) Test Vehicles

Two kinds of test vehicles, namely CoS (chip-on-substrate) and CoC (chip-on-chip) bonding, as summarized in Table 2.3 are used for the study. For CoS bonding, the chip size is  $5.0\text{ mm} \times 5.0\text{ mm} \times 0.15\text{ mm}$  and there are  $31 \times 31$  area array of C2 (Cu pillar with SnAg solder cap) bumps as shown in Fig. 2.43. The Cu pillar diameters are 40 or  $60\text{ }\mu\text{m}$  and the heights for pillar and solder cap are  $25\text{ }\mu\text{m}$  and  $27\text{ }\mu\text{m}$ , or  $25\text{ }\mu\text{m}$  and  $17\text{ }\mu\text{m}$ , respectively. The bump pitch is  $160\text{ }\mu\text{m}$ . The solder composition is 97.5%Sn2.5%Ag. The BT (bismaleimide triazine) substrate has a CuOSP surface finishing with both BOP (bump-on-pad) and BOL (bump-on-lead) structures. The pad diameter is  $80\text{ }\mu\text{m}$ , while the lead width is  $18\text{ }\mu\text{m}$ .

**Table 2.3** Test vehicles: CoS and CoC

	Chip-on-substrate (CoS)	Chip-on-chip (CoC)
Chip	Bump diameter = $\phi 60 \mu\text{m}$ Height = 25 $\mu\text{m}$ Cu + 27 $\mu\text{m}$ solder Bump pitch = 160 $\mu\text{m}$	Bump diameter = $\phi 40 \mu\text{m}$ Height = 25 $\mu\text{m}$ Cu + 17 $\mu\text{m}$ solder Bump pitch = 160 $\mu\text{m}$
	Bump diameter = $\phi 40 \mu\text{m}$ Height = 25 $\mu\text{m}$ Cu + 17 $\mu\text{m}$ solder Bump pitch = 160 $\mu\text{m}$	
Substrate	BT metallization = CuOSP Cu lead width = 18 $\mu\text{m}$ Cu pad diameter = $\phi 80 \mu\text{m}$ ; Cu lead/pad thickness = 15 $\mu\text{m}$	Surface finish = Cu Cu pad diameter = $\phi 60 \mu\text{m}$ Cu pad thickness = 10 $\mu\text{m}$
		Surface finish = SOP Cu pad diameter = $\phi 40 \mu\text{m}$ Cu pad thickness = 10 $\mu\text{m}$

**Fig. 2.43** Chip-on-substrate (CoS) test vehicle

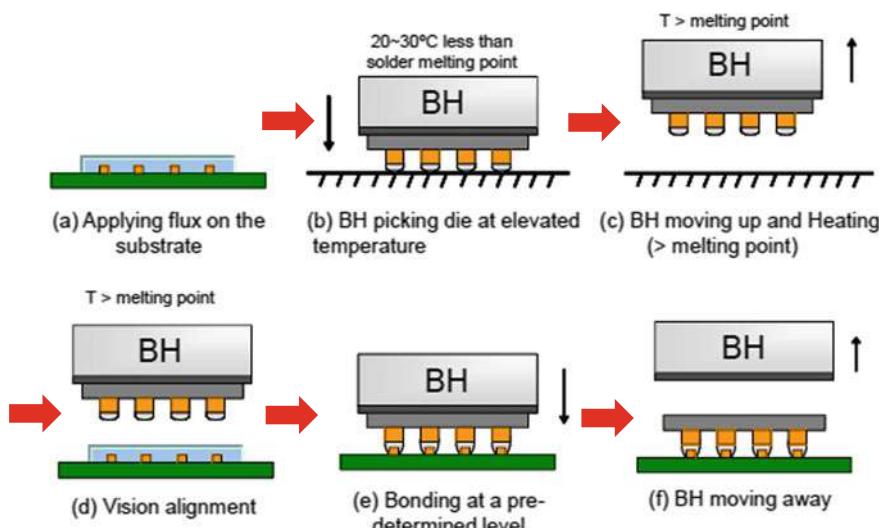
For CoC bonding, the top chip has 40  $\mu\text{m}$  Cu pillar diameter with 25  $\mu\text{m}$  pillar height and 17  $\mu\text{m}$  solder height. The bottom chip has two surface metallizations: bare Cu and solder-on-pad (SOP). For the chip with Cu finish, the pad diameter is 60  $\mu\text{m}$  and the pad thickness is 10  $\mu\text{m}$ . For the chip with SOP finish, the pad diameter is 40  $\mu\text{m}$  and the solder height is 17  $\mu\text{m}$ .

### (B) LPC TCB Process

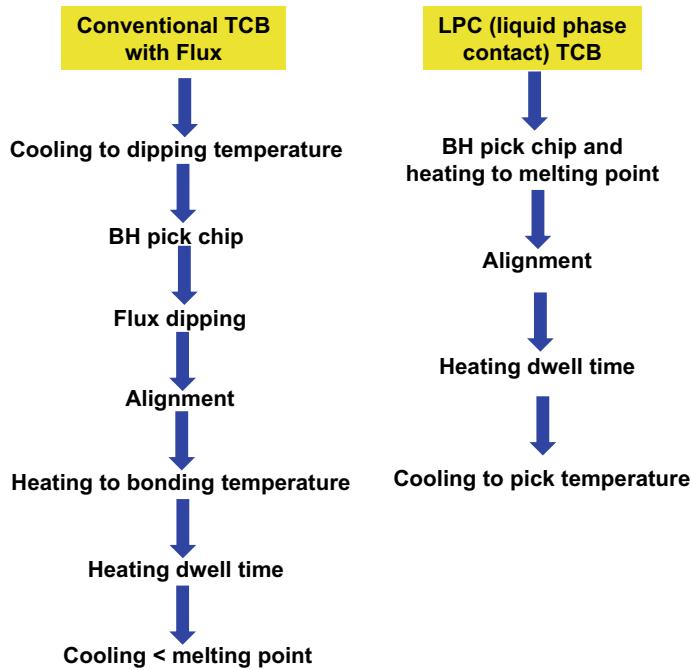
The LPC TCB process is schematically shown in Fig. 2.44, which has the following operation sequences.

- (a) Flux is printed or sprayed on the substrate.
- (b) BH picked up a chip from the carrier at an elevated temperature, which is (20–30 °C) below the solder melting point.
- (c) The BH heats up to a temperature higher than the solder melting point.
- (d) The chip is aligned with respect to the substrate.
- (e) After the vision alignment, the chip is contacted and wetted on the substrate at a predetermined bonding level.
- (f) After a certain bonding time, the BH could move away at the bonding temperature or cooled down to a temperature below the melting point of solder.

Figure 2.45 compares the bonding steps between the conventional TCB-flux process and LPC TCB process. For the conventional TCB-flux process, the flux is applied on the chip by a flux dipping method. The dipping temperature is lower than 100 °C due to the flux wicking and evaporation issues under high temperatures. A large temperature increase, such as from 100 to 250 °C for SnAg solder, is required after the chip contacting with the substrate. The heating time needed depends on the heating capacity/heating rate of the heater. On the other hand, for the LPC TCB process, the standby temperature of the BH is relatively high, only 20 ~ 30 °C lower than the solder melting point. The temperature heating up could occur during the BH moving up and the vision alignment. The whole bonding cycle for LPC TBC process could be less than 4 s. In some circumstances, if the required stand-off height



**Fig. 2.44** Key process flow of LPC TCB



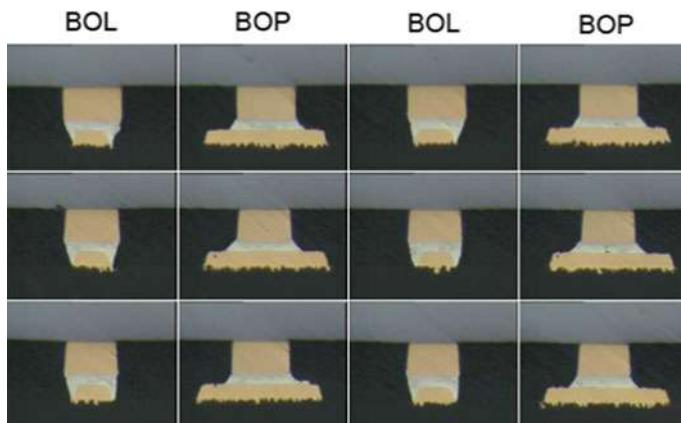
**Fig. 2.45** Bonding step differences between the conventional TCB-flux and LPC TCB

is near the solder equilibrium level, the cooling step could be omitted. The bonding cycle could be further reduced to 3 s or even less. The UPH (unit per hour) could be as high as 1,200 for a single BH configuration, compared with UPH of ~600 for a conventional TCB-flux process.

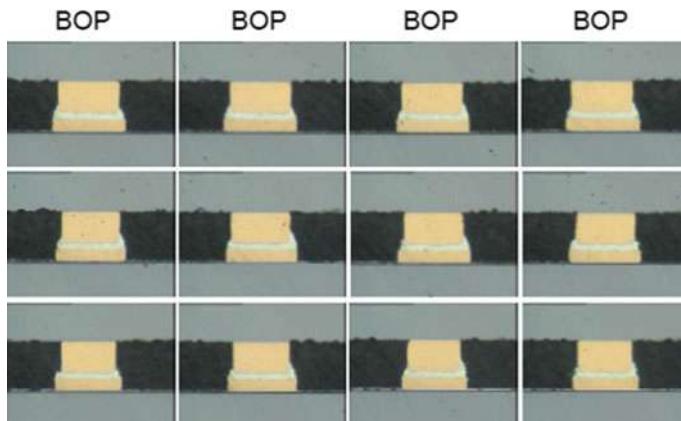
### (C) Bonding Quality Evaluation

Bonding temperature, bonding force, bonding time, bonding level, and cooling step are major process parameters for TCB LPC process, which need to be optimized. Cross sections of CoS and CoC bonded samples (Figs. 2.46 and 2.47, respectively) show excellent solder wetting with a solder thickness variation less than 2  $\mu\text{m}$ . It is noted that higher temperatures for both BH and work holder (WH) are required for CoC bonding. This is because silicon has a higher thermal conductivity (149 W/m K) than BT organic materials (0.35 W/m K). For CoC bonding, the heat from the BH could be dissipated rapidly into the bonding stage by the bottom silicon chip. The amount of additional heat required is controlled by the thickness and size of the bottom chip.

The solder joints obtained from the LPC TCB process are evaluated together with the samples assembled using mass reflow (MR) and conventional TCB-flux processes. Figure 2.48 shows the interfacial microstructure using these three bonding processes. For as-bonded condition, a very thin intermetallic compound (IMC) layer,



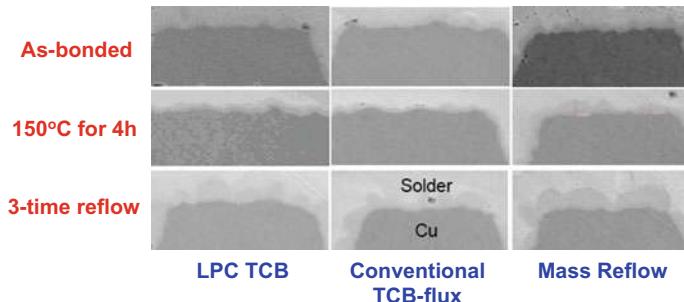
**Fig. 2.46** Cross section images of CoS flip chip assemblies. Stand-off height = 45.6  $\mu\text{m}$  (left); 46.2  $\mu\text{m}$  (center); and 46.4  $\mu\text{m}$  (right). Bonding conditions: WH = 80  $^{\circ}\text{C}$ , BH = 260  $^{\circ}\text{C}$ , BT = 1 s)



**Fig. 2.47** Cross section images of CoC flip chip assemblies. Stand-off height = 38.4  $\mu\text{m}$  (left); 37.6  $\mu\text{m}$  (center); and 38.1  $\mu\text{m}$  (right). Bonding conditions: WH = 120  $^{\circ}\text{C}$ , BH = 350  $^{\circ}\text{C}$ , BT = 1 s)

about 1  $\mu\text{m}$ , could be detected for both LPC TCB and conventional TCB-flux processes. For the MR process, IMC is relatively thick, about 2.0  $\mu\text{m}$ . This is due to the longer liquidus time during mass reflow process.

Short thermal aging and 3 times reflow tests are performed to examine the IMC growth behavior. After thermal aging at 150  $^{\circ}\text{C}$  for 4 h, the IMC growth is limited, only 0.1 ~ 0.2  $\mu\text{m}$ , while significant IMC growth (3  $\mu\text{m}$  for LPC TCB and traditional TCB-flux processes, and 4  $\mu\text{m}$  for mass reflow process) is observed after 3 times reflow. The scallop-like  $\text{Cu}_6\text{Sn}_5$  could be found at the bonding interfaces for all three bonding processes.



**Fig. 2.48** Interfacial microstructure for LPC TCB, conventional TCB-flux and mass reflow processes

Die shear test is also performed to evaluate the solder joint integrity. High values of shear force, ranged from 13 to 15 kgf are obtained for all these three processes under as-bonded conditions. The fracture occurs inside the solder layer. Compared with as-bonded condition, there is only a little change in shear force after thermal aging at 150 °C for 4 h. A relatively large drop in shear force is detected after multiple reflow (shear force after reflow: 10–13 kgf). The present results on interfacial microstructure, shear strength and failure mode indicate that LPC TCB process could lead to an excellent solder joint.

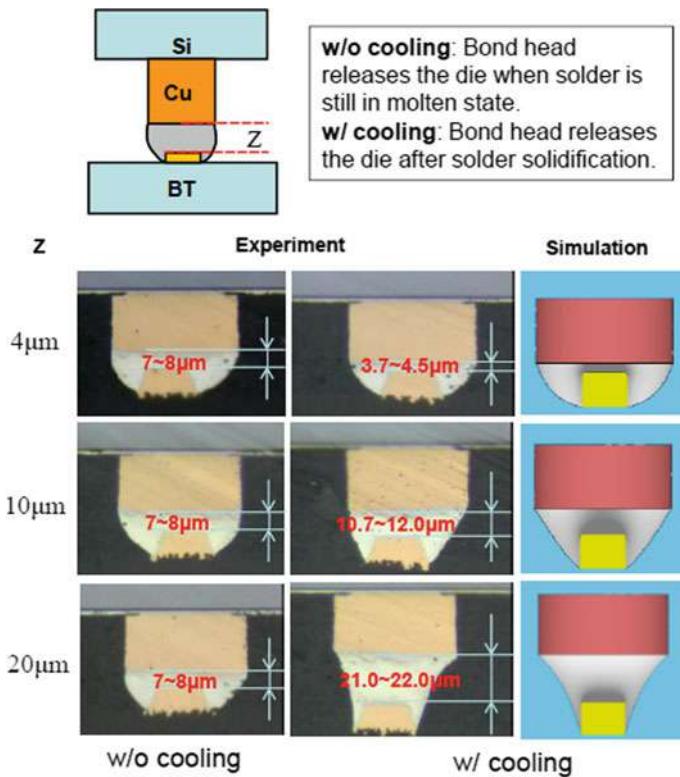
#### (D) Solder Joint Stand-off Height Control

Solder joint stand-off height control is important to facilitate the subsequent underfill process and to achieve excellent joint reliability. Coplanarity adjustment, precise position control and thermal management are the key controlling factors. Compared to the conventional TCB-flux process, there is no bonding tool heat-up step after the chip contacted with the substrate for the LPC TCB process. Thermal expansion induced by the bonding tools could be neglected. Because of the relatively short bonding time, the substrate temperature is low, hence the thermal expansion of the substrate is also less than that in the conventional TCB-flux process.

In addition, only a small bonding force (<1 kg) is required in the LPC TCB process since the solder is in the molten state during bonding. The small bonding force could also minimize the elastic deformation of the substrate to maintain an accurate stand-off height. In the following sections, effects of two bond parameters (cooling step and bonding temperature) on the solder height are reported and discussed.

#### (E) Effect of Cooling Step

As explained previously, after bonding the BH could move away from the chip at the bonding temperature (without a cooling step), or the BH cools down to a temperature below the solder melting point before moving away (with a cooling step). Different solder height values could be obtained under these two conditions. The pictures on



**Fig. 2.49** Cooling effect on solder height at different bonding levels for CoS flip chip assembly

the left in Fig. 2.49 show that without a cooling step the final solder height is almost the same for the samples bonded at different pre-determined bonding levels (from 4 to 20  $\mu\text{m}$ ), while the solder heights are consistent with the bonding levels if the BH cools down to 200  $^{\circ}\text{C}$  before releasing (the pictures in the middle), which are also in good agreement with the simulation results predicted using Surface Evolver model (the pictures on the right).

In order to understand how the restoring force driving the molten solder to the equilibrium height after BH is removed at the temperature above the solder melting point, Surface Evolver model is used to calculate the force generated by the surface tension of liquid solder. Based on the principle of virtual work, the restoring force at z-direction is the rate of change of energy with respect to the solder thickness [159]. In this study, the central difference scheme is used for calculating the restoring force. Figure 2.50 shows the relationship between the restoring force and the solder thickness. When the solder is compressed the force is repulsive, while if the solder is elongated it is attractive. There is one equilibrium point, at which the net force is zero. This point is the equilibrium solder thickness without any external force exertion. If the pre-determined bonding level is 4  $\mu\text{m}$ , the chip moves up to the equilibrium

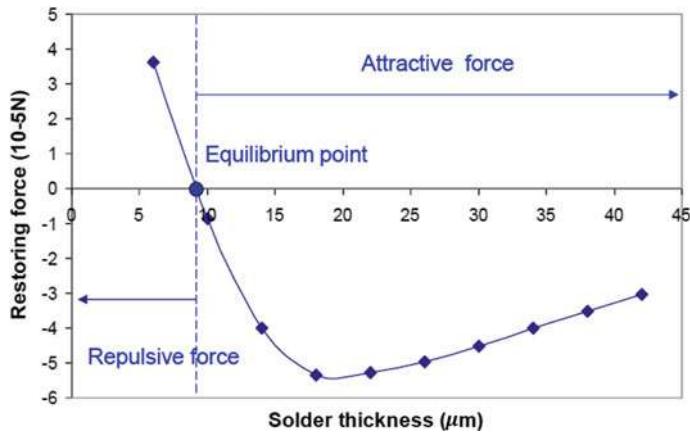


Fig. 2.50 Restoring force versus solder thickness

height driven by the repulsive force after the BH moving away from the chip top. While for the samples bonded at bonding levels of  $10\ \mu\text{m}$  and  $20\ \mu\text{m}$ , the chip moves down to the equilibrium height by the attractive force. That's why the solder height maintained the same regardless the bonding level.

#### (F) Effect of Bonding Temperature

It should be noted that in the aforementioned cases the bonding temperature is high enough that no solder solidification occurs during the bonding process. If the bonding temperature is relatively low, the molten solder might solidify, or partially solidify, as the BH contacting with the substrate. The final stand-off height at the low bonding temperature could be higher than that at the high bonding temperature. As shown in the Fig. 2.51,  $8\ \mu\text{m}$  and  $15\ \mu\text{m}$  solder heights are obtained for bonding temperatures at  $280\ ^\circ\text{C}$  and  $250\ ^\circ\text{C}$ , respectively. Similar phenomenon is also observed for CoC bonding as shown in Fig. 2.52.

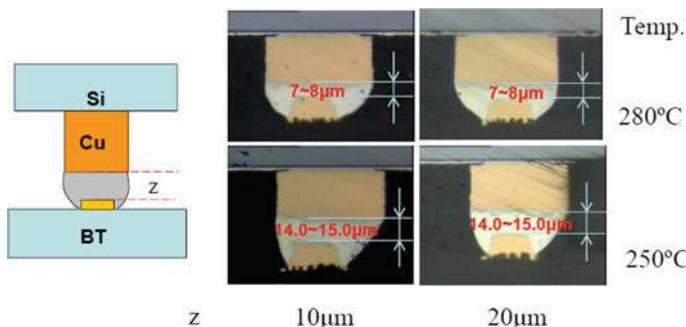
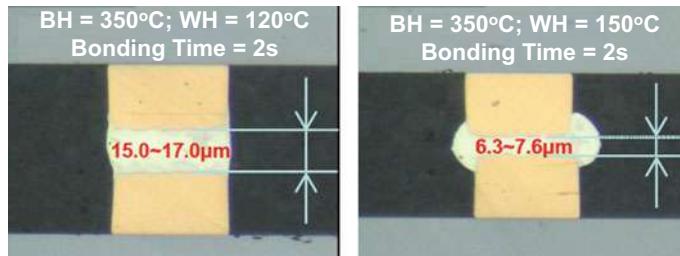


Fig. 2.51 Temperature effect on solder height for CoS flip chip assembly (w/o cooling)



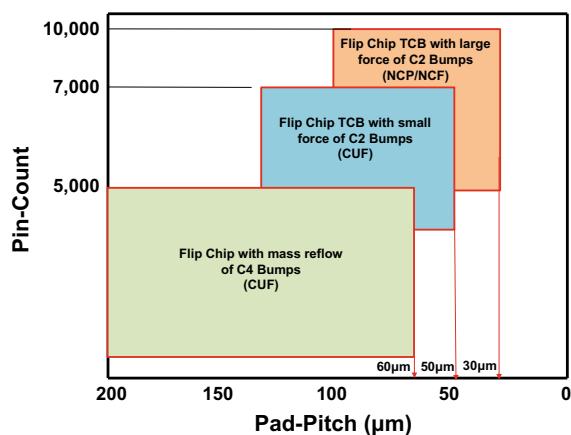
**Fig. 2.52** Temperature effect on solder height for CoC flip chip assembly (w/o cooling)

### 2.8.10 Summary and Recommendation

Some important result and recommendation are summarized in the follows.

- More than 75% of the flip chip applications will be on organic substrates.
- Flip chip with mass reflow of C4 bumps and capillary underfill (CUF) on organic substrates is and still used the most. The pin-count can be as high as 5000 and the pitch can go down to 60  $\mu\text{m}$  (Fig. 2.53).
- Because of the popularity of thin chips and thin organic package substrates, flip chip TCB with small force of C2 bumps and CUF and flip chip TCB with large force of C2 bumps and NCP/NCF are getting traction. The pin-count and pad-pitch of the flip chip TCB with small force of C2 bumps and CUF can be, respectively as high as 7,000 and as low as 50  $\mu\text{m}$ , and of the flip chip TCB with large force of C2 bumps and NCP/NCF can be as high as 10,000 and as low as 30  $\mu\text{m}$  (Fig. 2.53).
- For more information on SMT, please read [113].
- For more information on flip chip technology, please read [115–118].

**Fig. 2.53** Flip chip mass reflow of C4 bumps on organic substrate with CUF, flip chip TCB with small force of C2 bumps on organic substrate with CUF, and flip chip TCB with large force of C2 bumps on organic substrate with NCP/NCF



## References

1. Tsai, M., R. Chiu, D. Huang, F. Kao, E. He, J. Chen, S. Chen, J. Tsai and Y. Wang, "Innovative Packaging Solutions of 3D Double Side Molding with System in Package for IoT and 5G Application", *IEEE/ECTC Proceedings*, May 2019, pp. 700–706.
2. Liu, C., J. Chien, Y. Tseng, K. Liao, A. Chan, D. Chen, M. Shih, and M. Gerber, "Enhanced Reliability of a RF-SiP with Mold Encapsulation and EMI Shielding", *IEEE/ECTC Proceedings*, May 2019, pp. 1902–1908.
3. Milton, B., A. Shah, H. Xu, O. Kwon, G. Schulze, I. Qin, and N. Wong, "Smart Wire Bond Solutions for SiP and Memory Packages", *IEEE/ECTC Proceedings*, May 2019, pp. 55–62.
4. Talebbeydokhti, P., S. Dalmia, T. Thai, S. Tal, and R. Sover, "Ultra Large Area SIPs and Integrated mmW Antenna Array Module for 5G mmWave Outdoor Applications", *IEEE/ECTC Proceedings*, May 2019, pp. 294–299.
5. Dalmia, S., K. Nahalingam, S. Vijayakumar, and P. Talebbeydokhti, "A Zero Height Small Size Low Cost RF Interconnect Substrate Technology for RF Front Ends for M.2 Modules and SiP", *IEEE/ECTC Proceedings*, pp. 1666–1671.
6. Chen, J., X. Yong, D. Trombley, and R. Murugan, "System Co-Design of a 600 V GaN FET Power Stage with Integrated Driver in a QFN System-in-Package (QFN-SiP)", *IEEE/ECTC Proceedings*, pp. 1221–1226.
7. Lee, J., C. Chen, D. Lee, and J. Chen, "Moisture Effect on Physical Failure of Plastic Molded SiP Module", *IEEE/ECTC Proceedings*, May 2020, pp. 2124–2132.
8. Li, J., M. Tsai, R. Chiu, E. He, A. Hsieh, M. Tsai, F. Chu, J. Chen, S. Jian, S. Chen, and Y. Wang, "EMI Shielding Technology in 5G RF System in Package Module", *IEEE/ECTC Proceedings*, May 2020, pp. 931–937.
9. Ouyang, E., Y. Jeong, J. Kim, S. Lin, J. Vang, and A. Yang, "Warpage and Void Simulation of System in Package", *IEEE/ECTC Proceedings*, May 2020, pp. 2066–2071.
10. Chuang, P., M.-L. Lin, S.-T. Hung, Y.-W. Wu, D.-C. Wong, M.-C. Yew, C.-K. Hsu, L.-L Liao, P.-Y. Lai, P.-H. Tsai, S.-M. Chen, S.-K. Cheng, and S.-P. Jeng, "Hybrid Fan-out Package for Vertical Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 333–338.
11. Fettke, M., T. Kubsch, A. Kolbasow, V. Bejugam, A. Frick, T. Teutsch, "Laser-assisted bonding (LAB) and de-bonding (LAdB) as an advanced process solution for selective repair of 3D and multi-die chip packages", *IEEE/ECTC Proceedings*, May 2020, pp. 1016–1024.
12. Scott, G., J. Bae, K. Yang, W. Ki, N. Whitchurch, M. Kelly, C. Zwenger, J. Jeon, and T. Hwang, "Heterogeneous Integration Using Organic Interposer Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 885–892.
13. Chun, S., T. Kuo, H. Tsai, C. Liu, C. Wang, J. Hsieh, T. Lin, T. Ku, and D. Yu, "InFO\_SoW (System-on-Wafer) for High Performance Computing", *IEEE/ECTC Proceedings*, May 2020, pp. 1–6.
14. Peng, C., P. Lin, C. Ko, C. Wang, O. Chuang, and C. Lee, "A Novel Warpage Reinforcement Architecture with RDL Interposer for Heterogeneous Integrated Packages", *IEEE/ECTC Proceedings*, May 2020, pp. 526–531.
15. Liu, P., J. Li, H. van Zeijl, and G. Zhang "Wafer Scale Flexible Interconnect Transfer for Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 817–823.
16. Ali, M., A. Watanabe, T. Kakutani, P. Raj, R. Tummala, and M. Swaminathan1, "Heterogeneous Integration of 5G and Millimeter-Wave Diplexers with 3D Glass Substrates", *IEEE/ECTC Proceedings*, May 2020, pp. 1376–1382.
17. Martins, A., M. Pinheiro, A. Ferreira, R. Almeida, F. Matos, J. Oliveira, H. Santos, M. Monteiro, H. Gamboa, and R. Silva, "Heterogeneous Integration Challenges Within Wafer Level Fan-Out SiP for Wearables and IoT", *IEEE/ECTC Proceedings*, May 2018, pp. 1485–1492.
18. Ko, CT, H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, et al., "Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2018, pp. 355–363.

19. Ko, CT, H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J.W. Lin, T. Chen, I. Xu, C. Chang, J. Pan, H. Wu, Q. Yong, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, K. Wu, J. Hao, R. Beica, M. Lin, Y. Chen, Z. Cheng, S. Koh, R. Jiang, X. Cao, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, "Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, September 2018, pp. 1561–1572.
20. Hsu, F., J. Lin, S. Chen, P. Lin, J. Fang, J. Wang, and S. Jeng, "3D Heterogeneous Integration with Multiple Stacking Fan-Out Package", *IEEE/ECTC Proceedings*, May 2018, pp. 337–342.
21. Lin, Y., S. Wu, W. Shen, S. Huang, T. Kuo, A. Lin, T. Chang, H. Chang, S. Lee, C. Lee, J. Su, X. Liu, Q. Wu, and K. Chen, "An RDL-First Fan-out Wafer Level Package for Heterogeneous Integration Applications", *IEEE/ECTC Proceedings*, May 2018, pp. 349–354.
22. Lau, J. H., M. Li, M. Li, T. Chen, I. Xu, X. Qing, Z. Cheng, et al., "Fan-Out Wafer-Level Packaging for Heterogeneous Integration", *Proceedings of IEEE/ECTC*, May 2018, pp. 2354–2360.
23. Lau, J. H., M. Li, M. Li, T. Chen, I. Xu, X. Qing, Z. Cheng, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, P. Lo, K. Wu, J. Hao, S. Koh, R. Jiang, X. Cao, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, "Fan-Out Wafer-Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, 2018, September 2018, pp. 1544–1560.
24. Knickerbocker, J., R. Budd, B. Dang, Q. Chen, E. Colgan, L.W. Hung, S. Kumar, K.W. Lee, M. Lu, J. W. Nah, R. Narayanan, K. Sakuma, V. Siu, and B. Wen, "Heterogeneous Integration Technology Demonstrations for Future Healthcare, IoT, and AI Computing Solutions", *IEEE/ECTC Proceedings*, May 2018, pp. 1519–1522.
25. Lau, J. H., "Fan-Out Wafer-Level Packaging for 3D IC Heterogeneous Integration", *Proceedings of CSTIC*, March 2018, pp. VII\_1–6.
26. Lau, J. H., "Heterogeneous Integration with Fan-Out Wafer-Level Packaging", *Proceedings of IWLPC*, October 2017, pp. 1–25.
27. Panigrahi, A., C. Kumar, S. Bonam, B. Paul, T. Ghosh N. Paul, S. Vanjari, and S. Singh, "Metal-Alloy Cu Surface Passivation Leads to High Quality Fine-Pitch Bump-Less Cu-Cu Bonding for 3D IC and Heterogeneous Integration Applications", *IEEE/ECTC Proceedings*, May 2018, pp. 1555–1560.
28. Faucher-Courchesne, C., D. Danovitch, L. Brault, M. Paquet, and E. Turcotte, "Controlling Underfill Lateral Flow to Improve Component Density in Heterogeneously Integrated Packaging Systems", *IEEE/ECTC Proceedings*, May 2018, pp. 1206–1213.
29. Lau, J. H., "3D IC Heterogeneous Integration by FOWLP", *Chip Scale Review*, Vol. 22, January/February 2018, pp. 16–21.
30. Hu, Y., C. Lin, Y. Hsieh, N. Chang, A. J. Gallegos, T. Souza, W. Chen, M. Sheu, C. Chang, C. Chen, K. Chen, "3D Heterogeneous Integration Structure Based on 40 nm- and 0.18  $\mu\text{m}$ -Technology Nodes", *Proceedings of IEEE/ECTC*, May 2015, pp. 1646–1651.
31. Bajwa, A., S. Jangam, S. Pal, N. Marathe, T. Bai, T. Fukushima, M. Goorsky, and S. S. Iyer, "Heterogeneous Integration at Fine Pitch ( $\leq 10 \mu\text{m}$ ) using Thermal Compression Bonding", *IEEE/ECTC Proceedings*, May 2017, pp. 1276–1284.
32. Dittrich, M., A. Heinig, F. Hopsch, and R. Trieb, "Heterogeneous Interposer Based Integration of Chips with Copper Pillars and C4 Balls to Achieve High Speed Interfaces for ADC Application", *Proceedings of IEEE/ECTC*, Mat 2017, pp. 643–648.
33. Chuang, Y., C. Yuan, J. Chen, C. Chen, C. Yang, W. Changchien, C. Liu, and F. Lee, "Unified Methodology for Heterogeneous Integration with CoWoS Technology", *IEEE/ECTC Proceedings*, May 2013, pp. 852–859.
34. Ko, C., H. Yang, J. H. Lau, M. Li, M. Li, et al., "Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration", *Proceedings of IMAPS Symposium*, October 2018, pp. TP2\_1–7.
35. Lau, J. H., M. Li, Y. Lei, M. Li, I. Xu, T. Chen, Q. Yong, Z. Cheng, et al., "Reliability of Fan-Out Wafer-Level Heterogeneous Integration", *Proceedings of IMAPS Symposium*, October 2018, pp. WA2\_1–9.

36. Beal, A., and R. Dean, "Using SPICE to Model Nonlinearities Resulting from Heterogeneous Integration of Complex Systems", *IMAPS Proceedings*, October 2017, pp. 274–279.
37. Lau, J. H., M. Li, Y. Lei, M. Li, I. Xu, T. Chen, Q. Yong, Z. Cheng, et al., "Reliability of Fan-Out Wafer-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue 4, October 2018, pp. 148–162.
38. Ko, C. T., H. Yang, and J. H. Lau, "Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue 4, October 2018, pp. 141–147.
39. Hanna, A., A. Alam, T. Fukushima, S. Moran, W. Whitehead, S. Jangam, S. Pal, G. Ezhilarasu, R. Irwin, A. Bajwa, and S. Iyer, "Extremely Flexible (1 mm Bending Radius) Biocompatible Heterogeneous Fan-Out Wafer-Level Platform with the Lowest Reported Die-Shift (<6  $\mu\text{m}$ ) and Reliable Flexible Cu-Based Interconnects", *IEEE/ECTC Proceedings*, May 2018, pp. 1505–1511.
40. Kyozuka, M., T. Kiso, H. Toyazaki, K. Tanaka, and T. Koyama, "Development of Thinner POP base Package by Die Embedded and RDL Structure", *IMAPS Proceedings*, October 2017, pp. 715–720.
41. Yoon, S., J. Caparas, Y. Lin, and P. Marimuthu, "Advanced Low Profile PoP Solution with Embedded Wafer Level PoP (eWLB-PoP) Technology", *IEEE/ECTC Proceedings*, 2012, pp. 1250–1254.
42. Yoon, S., P. Tang, R. Emigh, Y. Lin, P. Marimuthu, and R. Pendse, "Fanout Flipchip eWLB (Embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions", *IEEE/ECTC Proceedings*, 2013, pp. 1855–1860.
43. Lin, Y., W. Lai, C. Kao, J. Lou, P. Yang, C. Wang, and C. Hsieh, "Wafer Warpage Experiments and Simulation for Fan-Out Chip on Substrate", *IEEE/ECTC Proceedings*, May 2016, pp. 13–18.
44. Lau, J. H., *Fan-Out Wafer-Level Packaging*. Springer Book Company, 2018.
45. Lau, J. H., et al, "Apparatus Having Thermal-Enhanced and Cost-Effective 3D IC Integration Structure with Through Silicon via Interposer". US Patent No: 8,604,603, Date of Patent: December 10, 2013.
46. Chiu, C., Z. Qian, and M. Manusharow, "Bridge Interconnect with AirGap in Package Assembly". US Patent No. 8,872,349, 2014.
47. Mahajan, R., R. Sankman, N. Patel, D. Kim, K. Ayyun, Z. Qian, et al., "Embedded Multi-die Interconnect Bridge (EMIB)—A High-Density, High-Bandwidth Packaging Interconnect", *IEEE/ECTC Proceedings*, May 2016, pp. 557–565.
48. Suk, K., S. Lee, J. Kim, S. Lee, H. Kim, S. Lee, P. Kim, D. Kim, D. Oh, and J. Byun, "Low Cost Si-less RDL Interposer Package for High Performance Computing Applications", *IEEE/ECTC Proceedings*, May 2018, pp. 64–69.
49. Podpod, A., J. Slabbekoorn, A. Phommahaxay, F. Duval, A. Salahouedlhadj, M. Gonzalez, K. Rebibis, R. A. Miller, G. Beyer, and E. Beyne, "A Novel Fan-Out Concept for Ultra-High Chip-to-Chip Interconnect Density with 20- $\mu\text{m}$  Pitch", *IEEE/ECTC Proceedings*, May 2018, pp. 370–378.
50. Lau, J. H., C. Lee, C. Zhan, S. Wu, Y. Chao, M. Dai, R. Tain, H. Chien, et al., "Low-Cost Through-Silicon Hole Interposers for 3D IC Integration", *IEEE Transactions on CPMT*, Vol. 4, No. 9, September 2014, pp. 1407–1419.
51. Souriau, J., O. Lignier, M. Charrier, and G. Poupon, "Wafer Level Processing Of 3D System in Package for RF and Data Applications", *IEEE/ECTC Proceedings*, 2005, pp. 356–361.
52. Henry, D., D. Belhachemi, J-C. Souriau, C. Brunet-Manquat, C. Puget, G. Ponthenier, J. Vallejo, C. Lecouvey, and N. Sillon, "Low Electrical Resistance Silicon Through Vias: Technology and Characterization", *IEEE/ECTC Proceedings*, 2006, pp. 1360–1366.
53. Khan, N., V. Rao, S. Lim, H. We, V. Lee, X. Zhang, E. Liao, R. Nagarajan, T. C. Chai, V. Kripesh, and J. H. Lau, "Development of 3-D Silicon Module With TSV for System in Packaging", *IEEE Proceedings of Electronic, Components & Technology Conference*, Orlando, FL, May 27–30, 2008, pp. 550–555. Also, *IEEE Transactions on CPMT*, Vol. 33, No. 1, March 2010, pp. 3–9.

54. Lau, J. H., C.-J. Zhan, P.-J. Tzeng, C.-K. Lee, M.-J. Dai, H.-C. Chien, Y.-L. Chao, et al., “Feasibility Study of a 3D IC Integration System-in-Packaging (SiP) from a 300 mm Multi-Project Wafer (MPW)”, *IMAPS International Symposium on Microelectronics*, October 2011, pp. 446–454. Also, *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 8, No. 4, Fourth Quarter 2011, pp. 171–178.
55. Zhan, C., P. Tzeng, J. H. Lau, M. Dai, H. Chien1, C. Lee, S. Wu, et al., “Assembly Process and Reliability Assessment of TSV/RDL/IPD Interposer with Multi-Chip-Stacking for 3D IC Integration SiP”, *IEEE/ECTC Proceedings*, San Diego, CA, May 2012, pp. 548–554.
56. Che, F., M. Kawano, M. Ding, Y. Han, and S. Bhattacharya, “Co-design for Low Warpage and High Reliability in Advanced Package with TSV-Free Interposer (TFI)”, *Proceedings of IEEE/ECTC*, May 2017, pp. 853–861.
57. Hou, S., W. Chen, C. Hu, C. Chiu, K. Ting, T. Lin, W. Wei, W. Chiou, V. Lin, V. Chang, C. Wang, C. Wu, and D. Yu, “Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology”, *IEEE Transactions on Electron Devices*, October 2017, pp. 4071–4077.
58. Selvanayagam, C., J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, “Nonlinear Thermal Stress/Strain Analysis of Copper Fill TSV (Through Silicon Via) and Their Flip-Chip Microbumps”, *IEEE/ECTC Proceedings*, May 27–30, 2008, pp. 1073–1081.
59. Selvanayagam, C., J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, “Nonlinear Thermal Stress/Strain Analyses of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps”, *IEEE Transactions on Advanced Packaging*, Vol. 32, No. 4, November 2009, pp. 720–728.
60. Lau, J. H., and G. Tang, “Thermal Management of 3D IC Integration with TSV (Through Silicon Via)”, *IEEE/ECTC Proceedings*, May 2009, pp. 635–640.
61. Lau, J. H., Y. S. Chan, and R. S. W. Lee, “3D IC Integration with TSV Interposers for High-Performance Applications”, *Chip Scale Review*, Vol. 14, No. 5, September/October, 2010, pp. 26–29.
62. Lau, J. H., “TSV Manufacturing Yield and Hidden Costs for 3D IC Integration”, *IEEE/ECTC Proceedings*, May 2010, pp. 1031–1041.
63. Zhang, X., T. Chai, J. H. Lau, C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, et al., “Development of Through Silicon Via (TSV) Interposer Technology for Large Die (21 × 21 mm) Fine-pitch Cu/low-k FCBGA Package”, *IEEE Proceedings of ECTC*, May, 2009, pp. 305–312.
64. Chai, T. C., X. Zhang, J. H. Lau, C. S. Selvanayagam, D. Pinjala, et al., “Development of Large Die Fine-Pitch Cu/low-k FCBGA Package with Through Silicon Via (TSV) Interposer”, *IEEE Transactions on CPMT*, Vol. 1, No. 5, May 2011, pp. 660–672.
65. Chien, H. C., J. H. Lau, Y. Chao, R. Tain, M. Dai, S. T. Wu, W. Lo, and M. J. Kao, “Thermal Performance of 3D IC Integration with Through-Silicon Via (TSV)”, *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 9, 2012, pp. 97–103.
66. Chaware, R., K. Nagarajan, and S. Ramalingam, “Assembly and Reliability Challenges in 3D Integration of 28 nm FPGA Die on a Large High-Density 65 nm Passive Interposer”, *IEEE/ECTC Proceedings*, May 2012, pp. 279–283.
67. Banijamali, B., S. Ramalingam, K. Nagarajan, and R. Chaware, “Advanced Reliability Study of TSV Interposers and Interconnects for the 28 nm Technology FPGA”, *IEEE/ECTC Proceedings*, May 2011, pp. 285–290.
68. Banijamali, B., S. Ramalingam, H. Liu, and M. Kim, “Outstanding and Innovative Reliability Study of 3D TSV Interposer and Fine-Pitch Solder Micro-Bumps”, *IEEE/ECTC Proceedings*, May 2012, pp. 309–314.
69. Banijamali, B., C. Chiu, C. Hsieh, T. Lin, C. Hu, S. Hou, et al., “Reliability Evaluation of a CoWoS-Enabled 3D IC Package”, *IEEE/ECTC Proceedings*, May 2013, pp. 35–40.
70. Xie, J., H. Shi, Y. Li, Z. Li, A. Rahman, K. Chandrasekar, et al., “Enabling the 2.5D Integration”, *Proceedings of IMAPS International Symposium on Microelectronics*, October 2012, pp. 254–267.
71. Li, L., P. Su, J. Xue, M. Brillhart, J. H. Lau, P. Tzeng, C. Lee, C. Zhan, et al., “Addressing Bandwidth Challenges in Next Generation High Performance Network Systems with 3D IC Integration”, *IEEE/ECTC Proceedings*, May 2012, pp. 1040–1046.

72. Lau, J. H., P. Tzeng, C. Zhan, C. Lee, M. Dai, J. Chen, Y. Hsin, et al., “Large Size Silicon Interposer and 3D IC Integration for System-in-Packaging (SiP)”, *Proceedings of the 45<sup>th</sup> IMAPS International Symposium on Microelectronics*, September 2012, pp. 1209–1214.
73. Wu, S. T., J. H. Lau, H. Chien, Y. Chao, R. Tain, L. Li, P. Su, et al., “Thermal Stress and Creep Strain Analyses of a 3D IC Integration SiP with Passive Interposer for Network System Application”, *Proceedings of the 45<sup>th</sup> IMAPS International Symposium on Microelectronics*, September 2012, pp. 1038–1045.
74. Chien, H., J. H. Lau, T. Chao, M. Dai, and R. Tain, “Thermal Management of Moore’s Law Chips on Both sides of an Interposer for 3D IC integration SiP”, *IEEE ICEP Proceedings*, Japan, April 2012, pp. 38–44.
75. Chien, H., J. H. Lau, T. Chao, M. Dai, R. Tain, L. Li, P. Su, et al., “Thermal Evaluation and Analyses of 3D IC Integration SiP with TSVs for Network System Applications”, *IEEE/ECTC Proceedings*, San Diego, CA, May 2012, pp. 1866–1873.
76. Ji, M., M. Li, J. Cline, D. Seeker, K. Cai, J. H. Lau, P. Tzeng, et al., “3D Si Interposer Design and Electrical Performance Study”, *Proceedings of Design Con*, Santa Clara, CA, January 2013, pp. 1–23.
77. Wu, S. T., H. Chien, J. H. Lau, M. Li, J. Cline, and M. Ji, “Thermal and Mechanical Design and Analysis of 3D IC Interposer with Double-Sided Active Chips”, *IEEE/ECTC Proceedings*, Las Vegas, NA, May 2013, pp. 1471–1479.
78. Tzeng, P. J., J. H. Lau, C. Zhan, Y. Hsin, P. Chang, Y. Chang, J. Chen, et al., “Process Integration of 3D Si Interposer with Double-Sided Active Chip Attachments”, *IEEE/ECTC Proceedings*, Las Vegas, NA, May 2013, pp. 86–93.
79. Stow, D., Y. Xie, T. Siddiqua, and G. H. Loh, “Cost-Effective Design of Scalable High-Performance Systems Using Active and Passive Interposers”, *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2017, pp. 728–735.
80. Hwang, T., D. Oh, E. Song, K. Kim, J. Kim, and S. Lee, “Study of Advanced Fan-Out Packages for Mobile Applications”, *IEEE/ECTC Proceedings*, May 2018, pp. 343–348.
81. Hong, J., K. Choi, D. Oh, S. Park, S. Shao, H. Wang, Y. Niu, and V. Pham, “Design Guideline of 2.5D Package with Emphasis on Warpage Control and Thermal Management”, *IEEE/ECTC Proceedings*, May 2018, pp. 682–692.
82. You, S., S. Jeon, D. Oh, K. Kim, J. Kim, S. Cha, and G. Kim, “Advanced Fan-Out Package SI/PI/Thermal Performance Analysis of Novel RDL Packages”, *IEEE/ECTC Proceedings*, May 2018, pp. 1295–1301.
83. Miao, M., L. Wang, T. Chen, X. Duan, J. Zhang, N. Li, L. Sun, R. Fang, X. Sun, H. Liu, and Y. Jin, “Modeling and Design of a 3D Interconnect Based Circuit Cell Formed with 3D SiP Techniques Mimicking Brain Neurons for Neuromorphic Computing Applications”, *IEEE/ECTC Proceedings*, May 2018, pp. 490–497.
84. Borel, S., L. Duperrex, E. Deschaseaux, J. Charbonnier, J. Cleidière, R. Wacquez, J. Fournier, J.-C. Souriau, G. Simon, and A. Merle, “A Novel Structure for Backside Protection against Physical Attacks on Secure Chips or SiP”, *IEEE/ECTC Proceedings*, May 2018, pp. 515–520.
85. Lee, E., M. Amir, S. Sivapurapu, C. Pardue, H. Torun, M. Bellaredj, M. Swaminathan, and S. Mukhopadhyay, “A System-in-Package Based Energy Harvesting for IoT Devices with Integrated Voltage Regulators and Embedded Inductors”, *IEEE/ECTC Proceedings*, May 2018, pp. 1720–1725.
86. Li, J., S. Ma, H. Liu, Y. Guan, J. Chen, Y. Jin, W. Wang, L. Hu, and S. He, “Design, Fabrication and Characterization of TSV Interposer Integrated 3D Capacitor for SiP Applications”, *IEEE/ECTC Proceedings*, May 2018, pp. 1968–1974.
87. Ki, W., W. Lee, I. Lee, I. Mok, W. Do, M. Kolbehdari, A. Copia, S. Jayaraman, C. Zwenger, and K. Lee, “Chip Stackable, Ultra-thin, High-Flexibility 3D FOWLP (3D SWIFT® Technology) for Hetero-Integrated Advanced 3D WL-SiP”, *IEEE/ECTC Proceedings*, May 2018, pp. 580–586.
88. Lee, J., C. Lee, C. Kim, and S. Kalchuri, “Micro Bump System for 2nd Generation Silicon Interposer with GPU and High Bandwidth Memory (HBM) Concurrent Integration”, *IEEE/ECTC Proceedings*, May 2018, pp. 607–612.

89. Lim, Y., X. Xiao, R. Vempati, S. Nandar, K. Aditya, S. Gaurav, T. Lim, V. Kripesh, J. Shi, J. H. Lau, and S. Liu, "High Quality and Low Loss Millimeter Wave Passives Demonstrated to 77-GHz for SiP Technologies Using Embedded Wafer-Level Packaging Platform (EMWLP)", *IEEE Transactions on Advanced Packaging*, Vol. 33, 2010, pp. 1061–1071.
90. Manessis, D., L. Boettcher, A. Ostmann, R. Aschenbrenner, and H. Reichl, "Chip Embedding Technology Developments Leading to the Emergence of Miniaturized System-in-Packages", *Proceedings of IEEE/ECTC*, May 2010, pp. 803–810.
91. Lau, J. H., M. S. Zhang, and S. W. R. Lee, "Embedded 3D Hybrid IC Integration System-in-Package (SiP) for Opto-Electronic Interconnects in Organic Substrates", *ASME Transactions, Journal of Electronic Packaging*, Vol. 133, September 2011, pp. 1–7.
92. Lau, J. H., C.-J. Zhan, P.-J. Tzeng, C.-K. Lee, M.-J. Dai, H.-C. Chien, et al., "Feasibility Study of a 3D IC Integration System-in-Packaging (SiP) from a 300 mm Multi-Project Wafer (MPW)", *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 8, No. 4, Fourth Quarter 2011, pp. 171–178.
93. Lau, J. H., and G. Y. Tang, "Effects of TSVs (through-silicon vias) on Thermal Performances of 3D IC Integration System-in-Package (SiP)", *Journal of Microelectronics Reliability*, Vol. 52, Issue 11, November 2012, pp. 2660–2669.
94. Ahmad, M., M. Nagar, W. Xie, M. Jimarez, and C. Ryu, "Ultra Large System-in-Package (SiP) Module and Novel Packaging Solution for Networking Applications", *Proceedings of IEEE/ECTC*, May 2013, pp. 694–701.
95. Wu, H., D. S. Gardner, C. Lv, Z. Zou, and H. Yu, "Integration of Magnetic Materials into Package RF and Power Inductors on Organic Substrates for System in Package (SiP) Applications", *Proceedings of IEEE/ECTC*, May 2014, pp. 1290–1295.
96. Qian, R., and Y. Liu, "Modeling for Reliability of Ultra-Thin Chips in a System in Package", *Proceedings of IEEE/ECTC*, May 2014, pp. 2063–2068.
97. Hsieh, C., C. Tsai, H. Lee, T. Lee, H. Chang, "Fan-out Technologies for WiFi SiP Module Packaging and Electrical Performance Simulation", *Proceedings of IEEE/ECTC*, May 2015, pp. 1664–1669.
98. Li, L., P. Chia, P. Ton, M. Nagar, S. Patil, J. Xue, J. DeLaCruz, M. Voicu, J. Hellings, B. Isaacson, M. Coor, and R. Havens, "3D SiP with organic interposer of ASIC and memory integration", *Proceedings of IEEE/ECTC*, May 2016, pp. 1445–1450.
99. Tsai, M., A. Lan, C. Shih, T. Huang, R. Chiu, S. L. Chung, J. Y. Chen, F. Chu, C. Chang, S. Yang, D. Chen, and N. Kao, "Alternative 3D Small Form Factor Methodology of System in Package for IoT and Wearable Devices Application", *Proceedings of IEEE/ECTC*, May 2017, pp. 1541–1546.
100. Das, R., F. Egitto, S. Rosser, E. Kopp, B. Bonitz, and R. Rai, "3D Integration of System-in-Package (SiP) using Organic Interposer: Toward SiP-Interposer-SiP for High-End Electronics", *IMAPS Proceedings*, September 2013, pp. 531–537.
101. Chien, H., C. Chien, M. Dai, R. Tain, W. Lo, Y. Lu, "Thermal Characteristic and Performance of the Glass Interposer with TGVs (Through-Glass Via)", *IMAPS Proceedings*, September 2013, pp. 611–617.
102. Vincent, M., D. Mitchell, J. Wright, Y. Foong, A. Magnus, Z. Gong, S. Hayes, and N. Chhabra, "3D RCP Package Stacking: Side Connect, An Emerging Technology for Systems Integration and Volumetric Efficiency", *IMAPS Proceedings*, September 2013, pp. 447–451.
103. Renaud-Bezot, N., "Size-Matters—Embedding as an Enabler of Next-Generation SiPs", *IMAPS Proceedings*, September 2013, pp. 740–744.
104. Couderc, P., Noiray, J., and C. Val, "Stacking of Known Good Rebuilt Wafers for High Performance Memory and SiP", *IMAPS Proceedings*, September 2013, pp. 804–809.
105. Lim, J., and V. Pandey, "Innovative Integration Solutions for SiP Packages Using Fan-Out Wafer Level eWLB Technology", *IMAPS Proceedings*, October 2017, pp. 263–269.
106. Becker, K., M. Minkus, J. Pauls, V. Bader, S. Voges, T. Braun, G. Jungmann, H. Wieser, M. Schneider-Ramelow, and K.-D., "Non-Destructive Testing for System-in-Package Integrity Analysis", *IMAPS Proceedings*, October 2017, pp. 182–187.

107. Lee, Y., and D. Link, "Practical Application and Analysis of Lead-Free Solder on Chip-On-Flip-Chip SiP for Hearing Aids", *IMAPS Proceedings*, October 2017, pp. 201–207.
108. Milton, B., O. Kwon, C. Huynh, I. Qin, and B. Chylak, "Wire Bonding Looping Solutions for High Density System-in-Package (SiP)", *IMAPS Proceedings*, October 2017, pp. 426–431.
109. Morard, A., J. Riou, and G. Pares, "Flip Chip Reliability and Design Rules for SiP Module", *IMAPS Proceedings*, October 2017, pp. 754–760.
110. Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill Book Company, New York, 2016.
111. Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, McGraw-Hill Book Company, New York, 2013.
112. Lau, J. H., *Handbook of Fine Pitch Surface Mount Technology*, Van Nostrand Reinhold, New York, 1994.
113. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, Springer, New York, 2020.
114. Prasad, A., L. Pymento, S. Aravamudhan, and C. Periasamy, "Advancement of Solder Paste Inspection (SPI) Tools to Support Industry 4.0 & Package Scaling", *SMTA International Proceedings*, October 2018, pp. 1–5.
115. Lau, J. H., *Flip Chip Technologies*, McGraw-Hill Book Company, New York, 1996.
116. Lau, J. H., and Y. Pao, *Solder Joint Reliability of Flip Chip Assemblies*, McGraw-Hill Book Company, New York, 1997.
117. Lau, J. H., *Low Cost Flip Chip Technologies*, McGraw-Hill Book Company, New York, 2000.
118. Lau, J. H., "Recent Advances and New Trends in Flip Chip Technology", *ASME Transactions, Journal of Electronic Packaging*, September 2016, Vol. 138, Issue 3, pp. 1–23.
119. Davis, E., Harding, W., Schwartz, R., and Corning, J., "Solid Logic Technology: Versatile, High Performance Microelectronics," *IBM J. Res. Dev.*, 8(2), 1964, pp. 102–114.
120. Totta, P., and Sopher, R., "SLT Device Metallurgy and Its Monolithic Extension," *IBM J. Res. Dev.*, 13(3), 1969, pp. 226–238.
121. Lau, J. H., and C. Chang, "Taguchi Design of Experiment for Wafer Bumping by Stencil Printing", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 21, No. 3, July 2000, pp. 219–225.
122. Love, D., Moresco, L., Chou, W., Horine, D., Wong, C., and Eilin, S., "Wire Interconnect Structures for Connecting an Integrated Circuit to a Substrate," *U.S. Patent No. 5,334,804*, filed Nov. 17, 1992 and issued Aug. 2, 1994.
123. Tung, F., "Pillar Connections for Semiconductor Chips and Method of Manufacture," *U.S. Patent No. 6,578,754*, filed Apr. 27, 2000 and issued June 17, 2003.
124. Tung, F., "Pillar Connections for Semiconductor Chips and Method of Manufacture," *U.S. Patent No. 6,681,982*, filed June 12, 2002 and issued Jan. 27, 2004.
125. Nakano, F., Soga, T., and Amagi, S., "Resin-Insertion Effect on Thermal Cycle Resistivity of Flip-Chip Mounted LSI Devices," *International Symposium on Microelectronics*, Minneapolis, MN, Sep. 28–30, 1987, pp. 536–541.
126. Tsukada, Y., Tsuchida, S., and Mashimoto, Y., "Surface Laminar Circuit Packaging," *IEEE/ECTC Proceedings*, May 1992, pp. 22–27.
127. Tsukada, Y., and Tsuchida, S., "Surface Laminar Circuit, a Low Cost High Density Printed Circuit Board," *SMTA International Conference*, Aug. 1992, pp. 537–542.
128. Tsukada, Y., "Solder Bumped Flip Chip Attach on SLC Board and Multichip Module," *Chip on Board Technologies for Multichip Modules*, J. H. Lau, ed., Van Nostrand Reinhold, New York, 1994, pp. 410–443.
129. Lau, J. H., and Chang, C., "Characteristics and Reliability of Fast-Flow, Snap-Cure, and Reworkable Underfills for Solder Bumped Flip Chip on Low-Cost Substrates," *IEEE Trans. Electron. Packag. Manuf.*, 25(3), 2002, pp. 231–230.
130. Lau, J. H., and Lee, R., "Fracture Mechanics Analysis of Low Cost Solder Bumped Flip Chip Assemblies With Imperfect Underfills," *ASME J. Electron. Packag.*, 222(4), 2000, pp. 306–310.
131. Lau, J. H., Lee, R., and Chang, C., "Effects of Underfill Material Properties on the Reliability of Solder Bumped Flip Chip on Board With Imperfect Underfill Encapsulants," *IEEE Trans. CPMT*, 23(2), 2000, pp. 323–333.

132. Lau, J. H., and Lee, S. W., "Effects of Underfill Delamination and Chip Size on the Reliability of Solder Bumped Flip Chip on Board," *IMAPS Trans. Int. J. Microcircuit Electron. Packag.*, 23(1), 2000, pp. 33–39.
133. Lau, J. H., Chang, C., and Chen, C., "Characteristics and Reliability of No-Flow Underfills for Solder Bumped Flip Chip Assemblies," *IMAPS Trans. Int. J. Microcircuit Electron. Packag.*, 22(4), 1999, pp. 370–381.
134. Lau, J. H., and Chang, C., "How to Select Underfill Materials for Solder Bumped Flip Chips on Low Cost Substrates?" *IMAPS Trans. Int. J. Microelectron. Electron. Packag.*, 22(1), 1999, pp. 20–28.
135. Lau, J. H., and Chang, C., "Characterization of Underfill Materials for Functional Solder Bumped Flip Chips on Board Applications," *IEEE Trans. CPMT, Part A*, 22(1), 1999, pp. 111–119.
136. Lau, J. H., Chang, C., and Ouyang, C., "SMT Compatible No-Flow Underfill for Solder Bumped Flip Chip on Low-Cost Substrates," *J. Electron. Manuf.*, 8(3–4), 1998, pp. 151–164.
137. Lau, J. H., Chang, C., and Chen, R., "Effects of Underfill Encapsulant on the Mechanical and Electrical Performance of a Functional Flip Chip Device," *J. Electron. Manuf.*, 7(4), 1997, pp. 269–277.
138. Lau, J. H., and Wun, B., "Characterization and Evaluation of the Underfill Encapsulants for Flip Chip Assembly," *J. Inst. Interconnect. Technol.*, 21(1), 1995, pp. 25–27.
139. Lau, J. H., Schneider, E., and Baker, T., "Shock and Vibration of Solder Bumped Flip Chip on Organic Coated Copper Boards," *ASME J. Electron. Packag.*, 118(2), 1996, pp. 101–104.
140. Lau, J. H., 1998, "Flip Chip on PCBs With Anisotropic Conductive Film," Advanced Packaging, July/Aug., pp. 44–48.
141. Lau, J. H., Chang, C., and Lee, R., "Failure Analysis of Solder Bumped Flip Chip on Low-Cost Substrates," *IEEE Trans. Electron. Packag. Manuf.*, 23(1), 2000, pp. 19–27.
142. Lau, J. H., Lee, R., Pan, S., and Chang, C., "Nonlinear Time-Dependent Analysis of Micro Via-In-Pad Substrates for Solder Bumped Flip Chip Applications," *ASME J. Electron. Packag.*, 124(3), 2002, pp. 205–211.
143. Lau, J. H., Q. Zhang, M. Li, K. Yeung, Y. Cheung, N. Fan, Y. Wong, M. Zahn, and M., and M. Koh, "Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Assemblies," *IEEE/ECTC Proceedings*, May 2015, pp. 168–174.
144. Wong, C. P., Baldwin, D., Vincent, M. B., Fennell, B., Wang, L. J., and Shi, S. H., "Characterization of a No-Flow Underfill Encapsulant During the Solder Reflow Process," *IEEE/ECTC Proceedings*, May 25–28, 1998, pp. 1253–1259.
145. Lau, J. H., Krulevitch, T., Schar, W., Heydinger, M., Erasmus, S., and Gleason, J., "Experimental and Analytical Studies of Encapsulated Flip Chip Solder Bumps on Surface Laminar Circuit Boards," *Circuit World*, 19(3), 1993, pp. 18–24.
146. Wun, B., and Lau, J. H., "Characterization and Evaluation of the Underfill Encapsulants for Flip Chip Assembly," *Circuit World*, 21(3), 1995, pp. 25–32.
147. Zhang, Z., and C. P. Wong, "Recent Advances in Flip-Chip Underfill: Materials, Process, and Reliability", September 2004, *IEEE Transactions on Advanced Packaging*, 27(3), pp. 515–524.
148. Cremaldi, J., Gaynes, M., Brofman, P., Pesika, N., and Lewandowski, E., "Time, Temperature, and Mechanical Fatigue Dependence on Underfill Adhesion," *IEEE/ECTC Proceedings*, May 2014, pp. 255–262.
149. Gilleo, K., Cotterman, B., and Chen, I. A., "Molded Underfill for Flip Chip in Package," *Proceedings of High Density Interconnects*, 2000, pp. 28–31.
150. Rector, L. P., Gong, S., Miles, T. R., and Gaffney, K., "Transfer Molding Encapsulation of Flip Chip Array Packages," *Int. J. Microcircuits Electron. Packag.*, 23(4), 2000, pp. 401–406.
151. Lai, Y. M., Chee, C. K., Then, E., Ng, C. H., and Low, M. F., "Capillary Underfill and Mold Encapsulation Method and Apparatus," U.S. Patent No. 7,262,077, filed Sep. 30, 2003 and issued Aug. 28, 2007.
152. Lee, J. Y., Oh, K. S., Hwang, C. H., Lee, C. H., and Amand, R. D. S., "Molded Underfill Development for FlipStack CSP," *IEEE/ECTC Proceedings*, May 2009, pp. 954–959.

153. Joshi, M., Pendse, R., Pandey, V., Lee, T. K., Yoon, I. S., Yun, J. S., Kim, Y. C., and Lee, H. R., “Molded Underfill (MUF) Technology for Flip Chip Packages in Mobile Applications,” *IEEE/ECTC Proceedings*, June 2010, pp. 1250–1257.
154. Ferrandon, C., Jouve, A., Joblot, S., Lamy, Y., Schreiner, A., Montmeat, P., Pellat, M., Argoud, M., Fournel, F., Simon, G., and Cheramy, S., “Innovative Wafer-Level Encapsulation and Underfill Material for Silicon Interposer Application,” *IEEE/ECTC Proceedings*, May 2013, pp. 761–767.
155. Lau, J. H., Zhang, Q., Li, M., Yeung, K., Cheung, Y., Fan, N., Wong, Y., Zahn, M., and Koh, M., “Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Substrates,” *IEEE Trans. CPMT*, 5(7), 2015, pp. 1027–1035.
156. Eitan, A., and Jing, K., “Thermo-Compression Bonding for Fine-Pitch Copper-Pillar Flip Chip Interconnect—Tool Features as Enablers of Unique Technology,” *IEEE/ECTC Proceedings*, May 2015, pp. 460–464.
157. Lee, M., Yoo, M., Cho, J., Lee, S., Kim, J., Lee, C., Kang, D., Zwenger, C., and Lanzone, R., “Study of Interconnection Process for Fine Pitch Flip Chip,” *IEEE/ECTC Proceedings*, May 2009, pp. 720–723.
158. Li, M., D. Tian, Y. Cheung, L. Yang, and J. H. Lau, “A High Throughput and Reliable Thermal Compression Bonding Process for Advanced Interconnections”, *IEEE/ECTC Proceedings*, May 2015, pp. 603–608.
159. Brakke, K. A., *Surface Evolver Manual version 2.70*, Susquehanna University, 2013.

# Chapter 3

## Fan-In Wafer/Panel-Level Chip-Scale Packages



### 3.1 Introduction

First of all, as the name “fan-in wafer/panel-level chip-scale packages” indicates that packages are fabricated on a wafer or panel, i.e., wafer/panel-level packaging (simply WLP) as shown in Fig. 3.1. This is very different from the wire bonding technology and flip chip technology (Fig. 3.2), in which, the device wafer is first diced into individual chips and then either wirebond or flip the individual chip on a package substrate (chip-in-package) or on a printed circuit board, i.e., COB (chip-on-board) and DCA (direct chip attach).

On July 13, 1998, Elenius and Hollack [1] of Flip Chip Technologies (now Flip Chip International, a subsidiary of Huatian Technology), proposed the use of redistribution layers (RDLs) to fan-in the original peripheral bond pads of a chip on a wafer and of solder balls (or bumps) to connect to a printed circuit board (PCB) or a package substrate (Figs. 3.1 and 3.3). In some applications such as memory chips, the original pads are along a center-line of the chip and the RDLs are fanning out from the original pads to the entire chip on a wafer as shown in Fig. 3.3. The RDL is connecting the electrical contact on the original bond pad to the solder ball (or bump) pad. Large solder balls can be fabricated within the chip on a wafer. Lead frame, substrate, and underfill may be eliminated.

It should be pointed out that the concept of fan-in WLP was first proposed by Flip Chip International [1, 8, 12]. However, the knowledge in this area has been mentioned/demonstrated by many others such as Mitsubishi [2, 6], Marcus [3], Sandia [4], ShellCase [5], Fraunhofer IZM [7, 9], DiStefano [10], and EPIC [11]. The packages made by the fan-in WLP technology are called wafer-level chip-scale packages (WLCSPs) and one of the most famous is UltraCSP [13] developed and patented by Flip Chip International [1].

In 2001, Amkor led the outsourced semiconductor assembly and tests (OSATs) and foundries to license the UltraCSP, and the WLP era began. In the past 20 years,

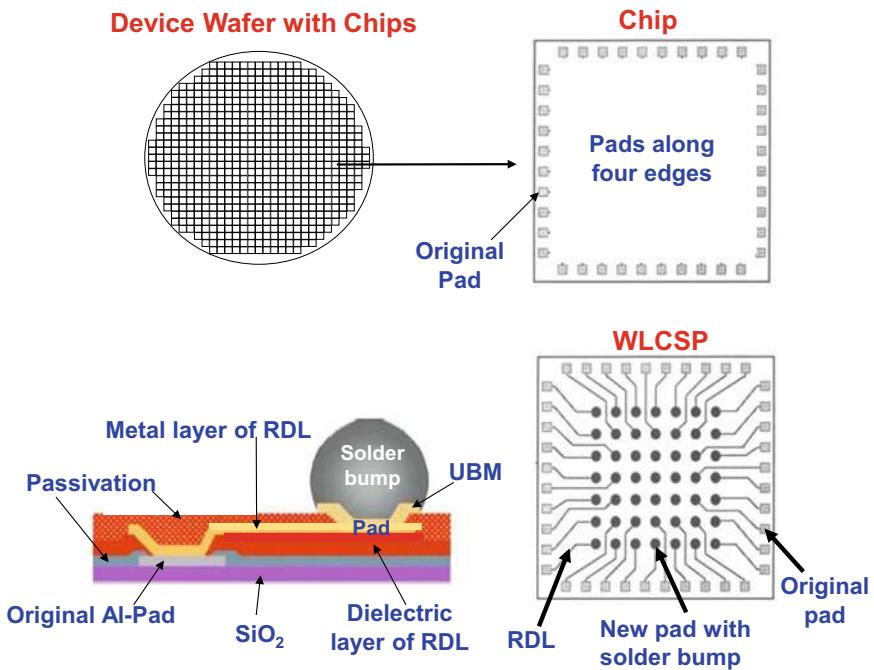


Fig. 3.1 Fan-in wafer-level chip-scale packages (WLCSP)

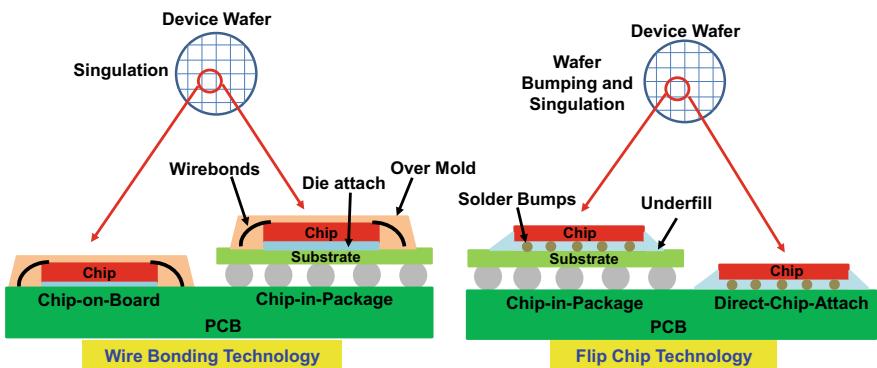
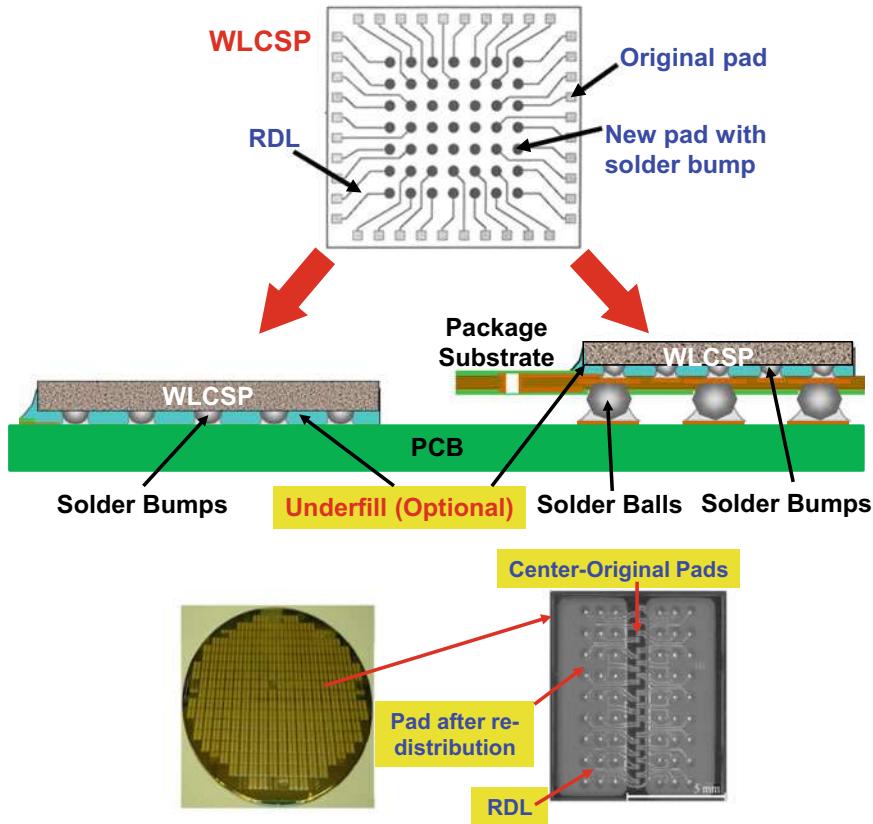


Fig. 3.2 Wire bonding technology and flip chip technology

WLCSPs have been extensively used for low-cost, low-end, low-profile, low-pincount, small form-factor, and high-volume applications such as mobile (smart-watches, smartphones, and tablets) and portable (digital cameras and notebooks) products, and have been researched especially in their solder joint reliability [14–130]. It should be emphasized that WLP is a high-throughput packaging technology.



**Fig. 3.3** WLCSP on board or on substrate

At one shot, all the chips on the wafer are packaged. In the first part of this chapter, the fabrication of RDLs on a wafer and one WLCSP example are presented.

Panel level is a very high-throughput packaging technology. This is because, in addition to area utilization (10–20% less silicon-area wastes with rectangular chips on rectangular panels than on circular wafers), the size of the temporary panel carrier (e.g., 508 mm × 508 mm) is usually larger than the standard-size wafer, e.g., 300 mm, i.e., the area increases by 3.65 times. In the second part of this chapter a method of utilizing the existing sizes of temporary PCB panel carriers and the corresponding PCB equipment for making panel level chip scale package (PLCSP) is presented.

Recently, because: (a) of the delamination of the dielectric layer in the front-side of the WLCSP, which is particularly true for advanced nodes (<14 nm process technology) products with fragile polyimides, (b) of the back-side chipping and sidewall cracking due to the mechanical blade dicing the wafer, (c) of the concern of the handling and SMT (surface mount technology) pick and place to damage the chip, and (d) in automotive electronics, the trends are driving lead-free solder

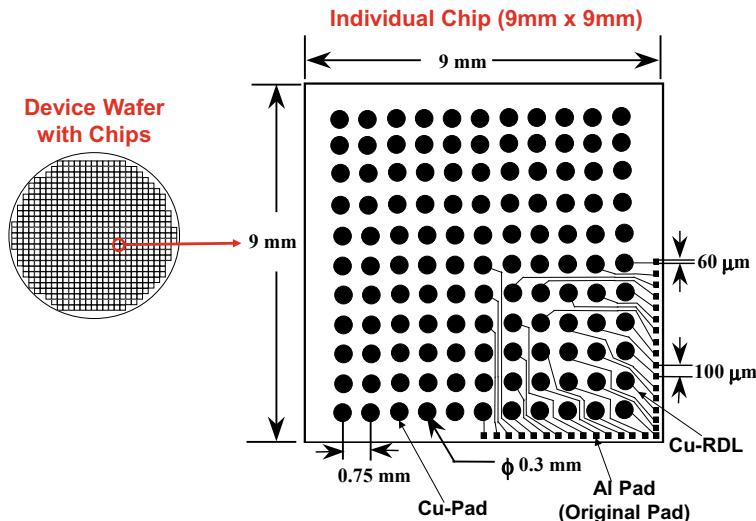
joint reliability for new functions such as the advanced driver-assistance systems (ADAS), under-the-hood operations often require high sustained heating/cooling temperatures, a higher-cost 5-side or 6-side molded WLCSPs are getting traction. In the third part of this chapter various 5-side or 6-side molded WLCSPs will be presented.

In the fourth part of this chapter, the design, materials, process, assembly, and reliability of a 6-side molded PLCSP is presented. Emphasis is placed on the fabrication of the RDLs of the PLCSP on a large temporary panel with multiple device wafers. After the fabrication of RDLs; then debond the wafers from the PCB panel and fabricate the 6-side protection (molding) of the PLCSP. Reliability assessments of the PLCSP are performed by a drop test and a thermal cycling test and simulation.

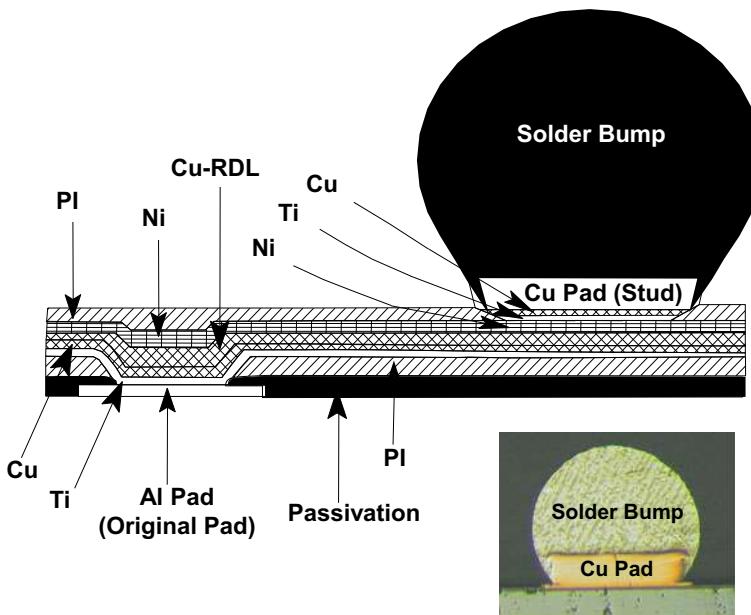
## 3.2 Fan-In Wafer-Level Chip-Scale Packages (WLCSPs)

### 3.2.1 The Structure

Figure 3.4 shows a 300 mm wafer with many  $9 \times 0.51$  mm chips. The dimensions of the 121 original peripheral pads of the chip are  $60 \mu\text{m} \times 60 \mu\text{m}$  with a spacing of  $100 \mu\text{m}$ . By adding an additional metal layer on top of the wafer, the fine-pitch original peripheral-arrayed pads on the chip can be redistributed to a much larger pitch and area-array pads in the interior of the chip. In this case, the pitch is  $0.75 \text{ mm}$  and the pad size is  $0.3 \text{ mm}$  in diameter. Figure 3.5 shows the details of redistribution. It can



**Fig. 3.4** An example on WLCSP



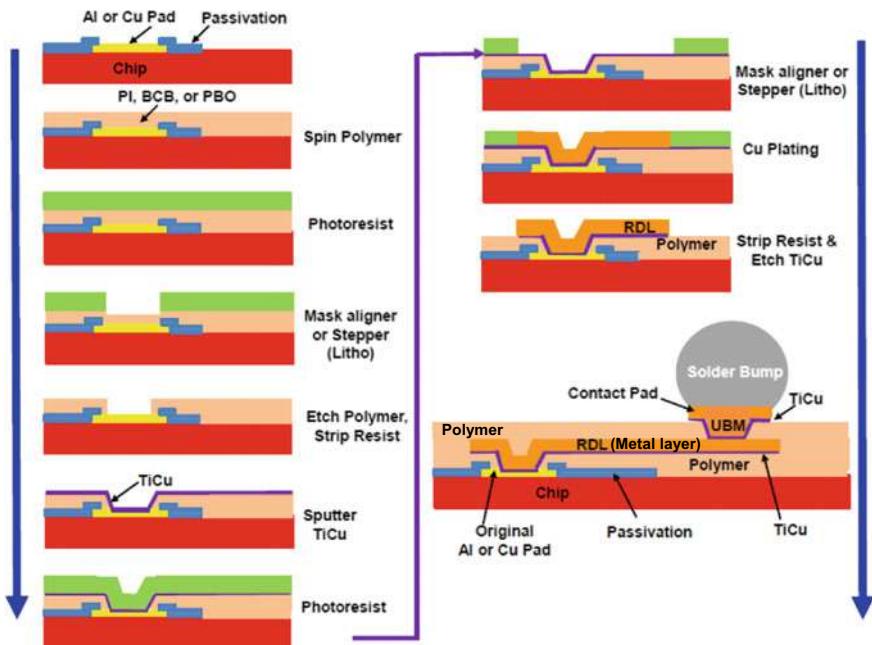
**Fig. 3.5** RDL on a WLCSP

be seen that the solder bump (or ball) is supported by a Cu stud, which is connected to the redistributed Cu/Ni pad through the Cu/Ti UBM (under bump metallurgy). The redistributed metal layer is made of Cu/Ni.

### 3.2.2 WLCSP Key Process Steps

The key process steps (Fig. 3.6) for fabricating the RDL of the WLCSP (Fig. 3.4 and 3.5) are briefly discussed as follows.

1. Ultrasonic clean the wafer
2. Spin the polymers such as polyimide (PI), benzocyclobutene (BCB), or polybenzo-bisoxazole (PBO) on the wafer and cure for 1 h. This will form a 4–7  $\mu\text{m}$ -thick dielectric layer.
3. Apply photoresist.
4. Mask aligner or stepper.
5. Then use photolithography techniques (align and expose) to open vias of the resist.
6. Etch the PI, BCB, or PBO.
7. Strip off the photoresist.
8. Sputter Ti and Cu over the entire wafer.

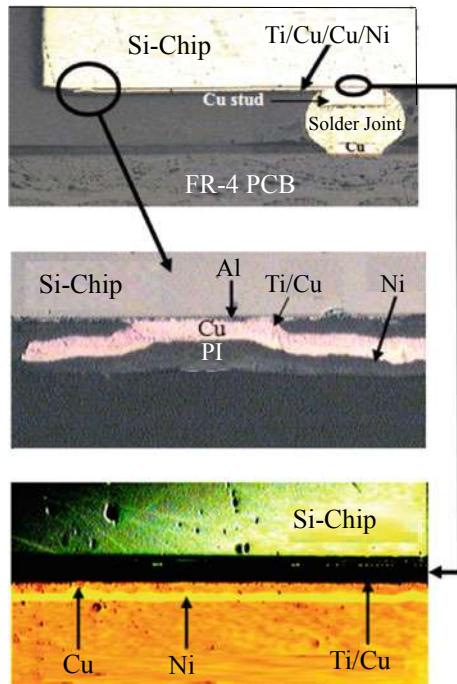


**Fig. 3.6** Key process steps of a WLCSP

9. Apply photoresist and mask aligner or stepper and then use photolithography techniques to open the redistribution traces locations.
10. Electroplate Cu in photoresist openings.
11. Electroplate Ni (optional).
12. Strip off the photoresist.
13. Etch off the Ti/Cu to obtain the RDL.
14. Same as Step 2 (for UBM).
15. Apply photoresist and mask and then use photolithography techniques to open vias on the photoresist for the desired bump pads and cover the redistribution traces.
16. Etch the PI, BCB, or PBO.
17. Strip off the photoresist.
18. Sputter Ti and Cu over the entire wafer.
19. Apply photoresist and mask and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
20. Electroplate the Cu core.
21. Electroplate solder.
22. Strip off the photoresist.
23. Etch off the Ti/Cu.
24. Apply flux and Reflow the solder.

If a photosensitive polyimide is used, then Steps 3, 5, and 7 are not necessary.

**Fig. 3.7** Images of WLCSP on PCB without underfill

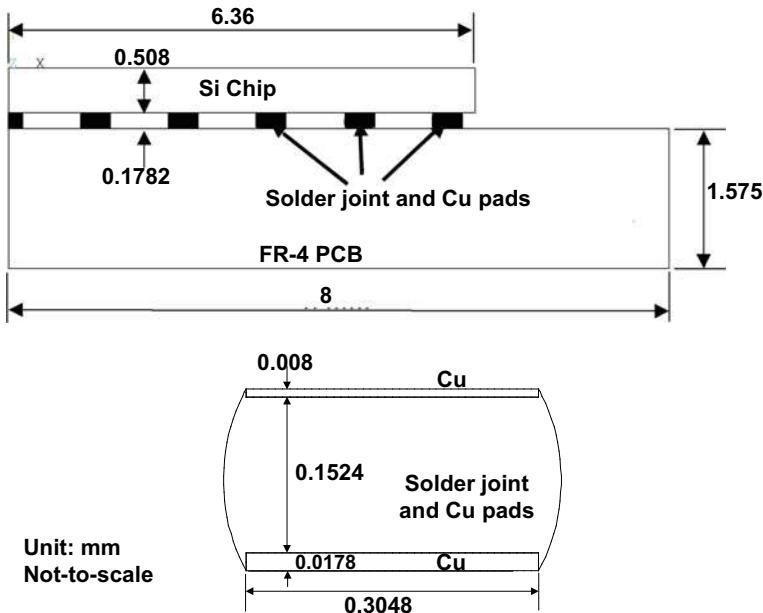


### 3.2.3 PCB Assembly of WLCSP

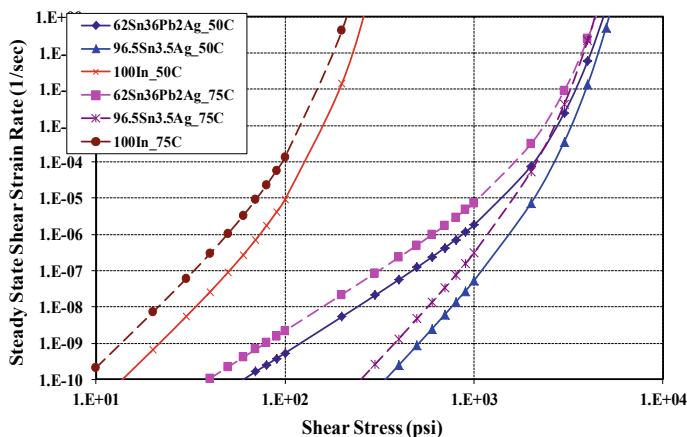
It is very easy to assemble the WLCSP on a PCB. After the solder bumped WLCSP is aligned with the PCB with a look-up camera and a look-down camera, then the WLCSP is placed face-down on the PCB with flux and a very minimum force. After chip placement, it is placed in the oven for reflow. A typical cross section of the WLCSP PCB assembly is shown in Fig. 3.7. It can be seen that the Ti/Cu on the Al pad are supporting the redistribution trace (Cu/Ni) which is protected by the polyimide. At the solder joint, the Cu core on the Ni/Cu pad is connected by the Cu/Ti UBM, which is isolated from the Si chip with a layer of polyimide dielectric.

### 3.2.4 Thermal Simulation of the WLCSP PCB Assembly

Figure 3.8 schematically shows the PCB assembly of the lead-free solder bumped WLCSP. It can be seen that the PCB is 1.575 mm thick and is made of FR-4 epoxy glass. The copper pad thickness is 0.018 mm as shown in Fig. 3.8. The solder joint height is 0.1524 mm and is made of lead-free (96.6Sn3.5Ag and 100In) and 62Sn36Pb2Ag solder alloys. The shear stress versus steady state shear strain rate of these solder alloys is shown in Fig. 3.9 [29].

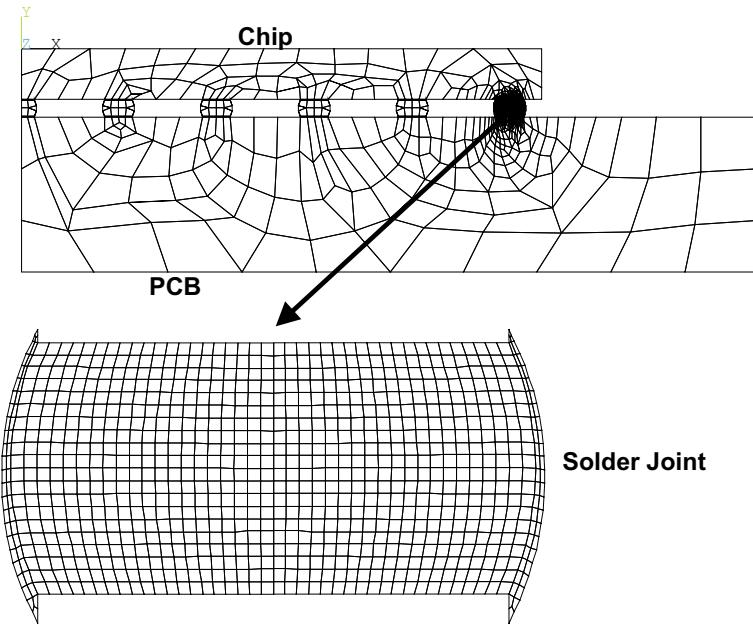


**Fig. 3.8** WLCSP for simulation



**Fig. 3.9** Creep material property of various solder alloys

Figure 3.10 shows a typical finite element model for creep analysis of the lead-free solder bumped WLCSP on PCB assemblies. Due to symmetry, only one-half of the structure (along the diagonal) is modeled and it is a 2-D analysis. Since the focus is on the corner solder joint, finer meshes are used to model it. The finite element code used is ANSYS. It can solve boundary-value problems with Garofalo-Arrhenius



**Fig. 3.10** Finite element modeling of the WLCSP PCB assembly

constitutive equation as shown in Table 3.1 and Fig. 3.9. The material properties of the silicon chip, FR-4 PCB, copper, and underfill are shown in Table 3.2.

The temperature loading imposed on the solder bumped WLCSP on PCB assemblies is shown in Fig. 3.11. It can be seen that for each cycle (60 min) the temperature is between  $-20$  and  $+110$   $^{\circ}\text{C}$ , with 15 min ramp, 20 min hold at hot, and 10 min hold at cold. Five full cycles are executed.

Figures 3.12a through e show the deformed shapes (50X) of the 62Sn2Ag36Pb solder bumped WLCSP on PCB assembly at the instants of 588, 4188, 7788, 11388, and 14988 s (Fig. 3.12). It can be seen and expected that, due to the thermal expansion mismatch between the silicon ( $2.8$   $\text{ppm}/^{\circ}\text{C}$ ) chip and the FR-4 epoxy glass ( $18$

**Table 3.1** Garofalo-Arrhenius constitute equations for various solder alloys  $\frac{d\varepsilon}{dT} = C_1[\sinh(C_2\sigma)]^{C_3} \exp\left(-\frac{C_4}{T}\right)$

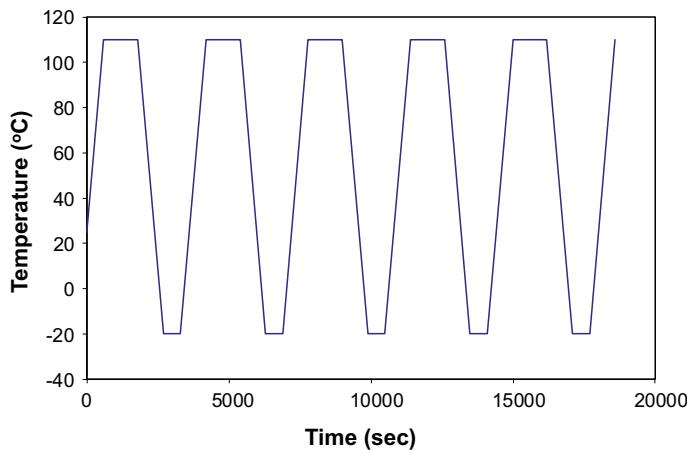
Solder alloys	$C_1$ (1/s)	$C_2$ (1/psi)	$C_3$	$C_4$ ( $^{\circ}\text{K}$ )
62Sn36Pb2Ag	$462(508 - T)/T$	$1/(5478 - 10.79T)$	3.3	6360
96.5Sn3.5Ag	$18(553 - T)/T$	$1/(6386 - 11.55T)$	5.5	5802
100In	$40647(593 - T)/T$	$1/(274 - 0.47T)$	5	8356
96.5Sn3Ag0.5Cu	500000	0.01	5	5800

Note  $T$  is absolute temperature in  $^{\circ}\text{K}$  and  $\sigma$  is in psi, except Sn3Ag0.5Cu which is in MPa

**Table 3.2** Material properties for various solder alloys

Materials	Young's modulus (MPa)	Poisson's ratio ( $\nu$ )	CTE ( $\alpha$ ) ppm/ $^{\circ}$ C
62Sn36Pb2Ag	34,441-152T	0.35	24.5
96.5Sn3.5Ag	52,708-67.14T-0.0587T <sup>2</sup>	0.4	21.85 + 0.02039T
100In	2,200	0.4	32.1
Underfill	9,292-35.4T	0.35	31.04 + 0.0923T
Si	131,000	0.3	2.8
FR4	22,000	0.28	18
Copper	76,000	0.35	17
Build-up resin	20,000	0.3	50

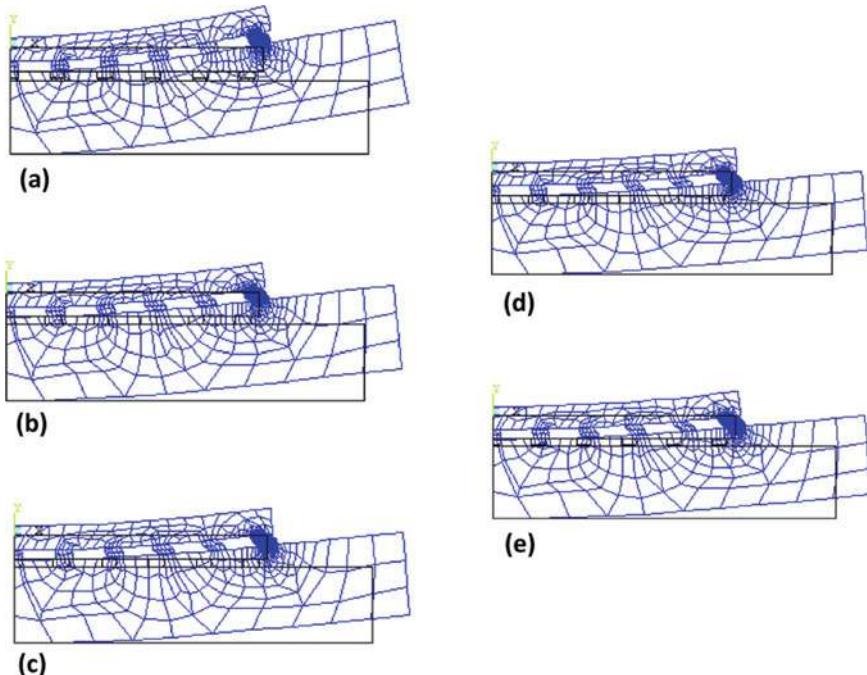
Note T is temperature ( $^{\circ}$ C). The electroplated copper is assumed to be elastic-plastic

**Fig. 3.11** Temperature profile (boundary condition)

$\times 10^{-6}/^{\circ}$ C) PCB, the solder joints are subjected to very large shear deformation (especially the corner solder joint). Also, the whole structure is deformed into a concave shape at these time instants (temperature  $\sim 110$   $^{\circ}$ C).

Figures 3.13a through e and 3.14a through e show, respectively, the effective creep strain contours and the effective stress contours in the corner solder joint of the 62Sn2Ag36Pb solder bumped WLCSP on PCB assembly at the instants of 588, 4188, 7788, 11388, and 14988 s.

It is interesting to note that at 588 s, the maximum deflection of the assembly is 0.028 mm and at that instant the maximum effective creep strain and stress in the corner solder joint are 0.05 and 15.01 MPa, respectively. However, at 4188 s, the maximum deflection of the assembly is reduced (by 21%) to 0.022 and at that instant the maximum effective creep strain in the corner solder joint is increased (by 78%) to 0.088 and the maximum effective stress is decreased (by 17.5%) to 12.39 MPa.



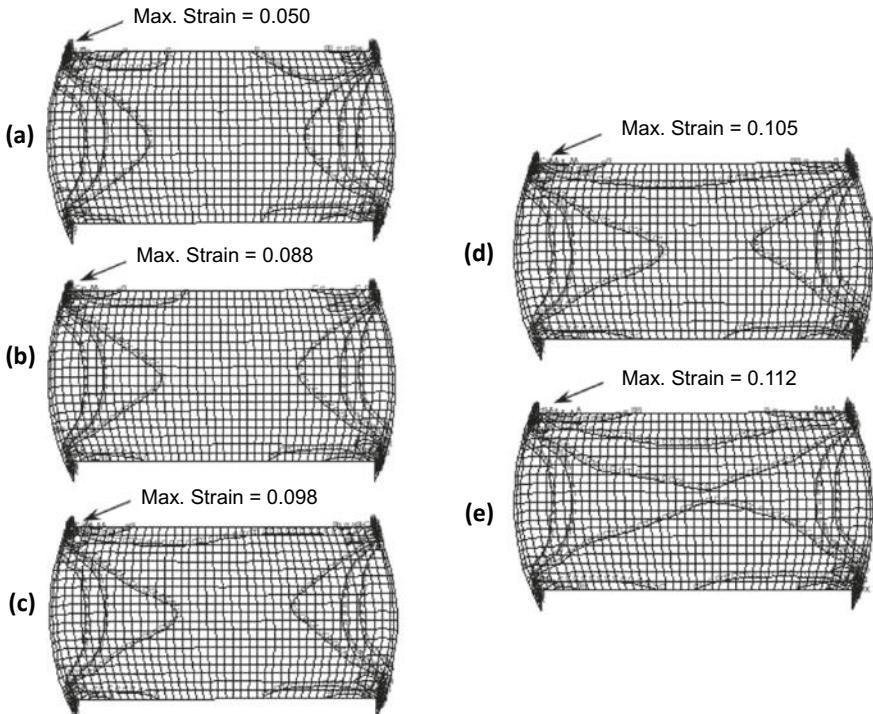
**Fig. 3.12** Deformed shape and undeformed shape

This is because of the increasing deformation of the solder joints which makes the chip and the PCB less bonding together.

At 7788 s, the maximum deflection of the assembly is reduced (by 5%) to 0.021 and at that instant the maximum effective creep strain in the corner solder joint is increased (by 11%) to 0.098 and the maximum effective stress is decreased (by 3%) to 11.97 MPa. At 11388 s, the maximum deflection of the assembly is reduced (by 4.7%) to 0.020 and at that instant the maximum effective creep strain in the corner solder joint is increased (by 7%) to 0.105 and the maximum effective stress is decreased (by 1.8%) to 11.76 MPa.

At 14988 s, the maximum deflection of the assembly is reduced (by 2%) to 0.0196 and at that instant the maximum effective creep strain in the corner solder joint is increased (by 4.7%) to 0.11 and the maximum effective stress is decreased (by 0.03%) to 11.76 MPa. Based on the foregoing results, it can be seen that: (1) the stress and creep strain are quite stabilized after the first thermal cycle, and (2) the present analysis is converged after the third thermal cycles. Similar results for the WLCSP PCB assemblies with 96.5Sn3.5Ag and 100In lead free solder joints.

The shear-stress history at the corner solder joint made by the 62Sn36Pb2Ag, 96.5Sn3.5Ag, and 100In solder alloys is shown in Fig. 3.15. It can be seen that: (1) at this location, the shear-stress history of all these solder alloys follows the imposed thermal cycling condition; (2) the shear stress range of 100In is much smaller than that



**Fig. 3.13** Creep strain contours in the corner solder joint

of 62Sn36Pb2Ag and 96.5Sn3.5Ag; and (3) the shear stress range of 96.5Sn3.5Ag is slight higher than that of 62Sn36Pb2Ag and this is because the stiffness (Young's modulus) of SnAg is higher than that of SnPb.

The shear-creep-strain history at the corner solder joint made by the 62Sn36Pb2Ag, 96.5Sn3.5Ag, and 100In solder alloys is shown in Fig. 3.16. It can be seen that: (1) at this location, just like the shear-stress history, the shear-creep-strain history of all these solder alloys follows the imposed thermal cycling condition; (2) the shear-creep-strain range of 100In is much larger than that of 62Sn36Pb2Ag and 96.5Sn3.5Ag and it is because of the creep rate of In is much larger than that of SnAg and SnPb; and (3) the shear-creep-strain range of 96.5Sn3.5Ag is slight smaller than that of 62Sn36Pb2Ag.

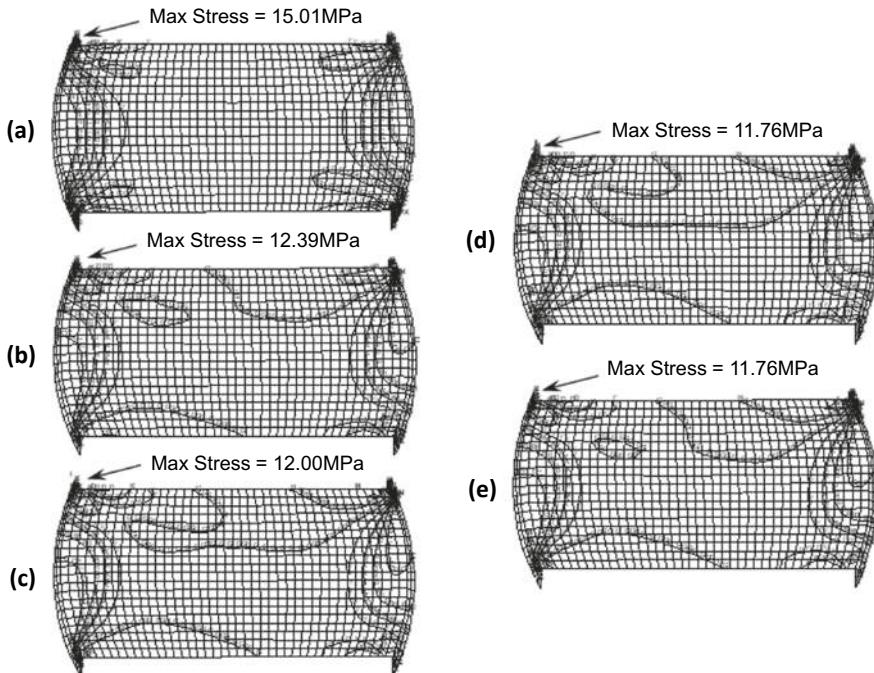


Fig. 3.14 Stress contours in the corner solder joint

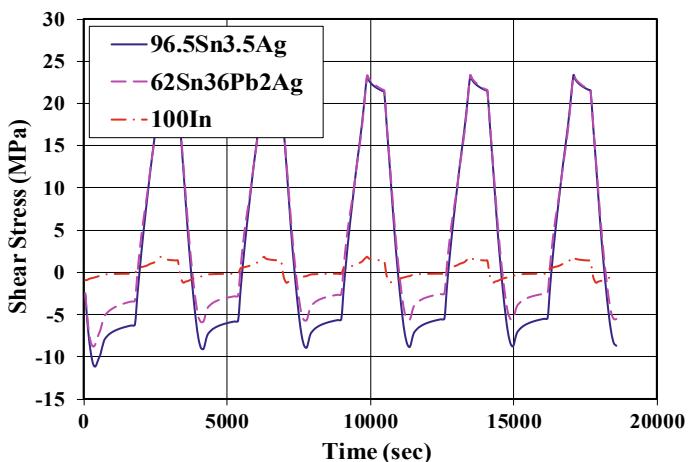
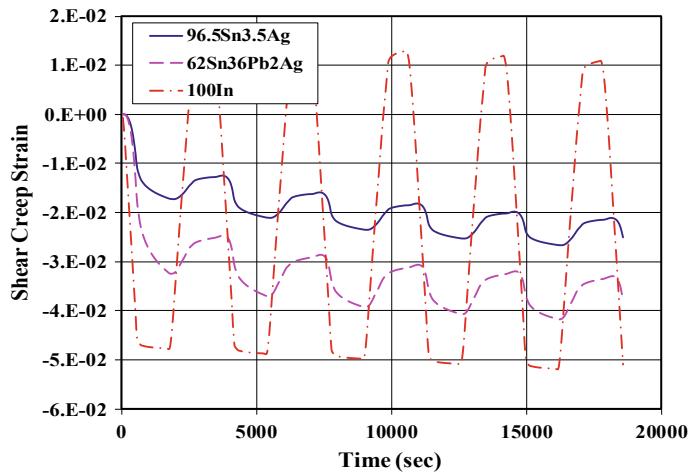


Fig. 3.15 Shear stress versus time in the corner solder joint for various solder alloy



**Fig. 3.16** Shear creep strain versus time in the corner solder joint for various solder alloy

### 3.2.5 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- The key process steps in fabricating the RDL of WLCSP have been provided.
- A non-linear, time and temperature dependent 3D finite element simulation has been performed for a WLCSP PCB assembly with three different solder alloys: 96.5Sn3.5Ag, 100In, and 62Sn36Pb2Ag.
- The creep shear strain range of 100In is larger than that of 62Sn36Pb2Ag and 96.5Sn3.5Ag. Also the creep shear strain range of 96.5Sn3.5Ag is slightly smaller than that of 62Sn36Pb2Ag.
- The shear stress of 100In is much smaller than that of 62Sn36Pb2Ag and 96.5Sn3.5Ag, and the shear stress of 96.5Sn3.5Ag is slightly higher than that of 62Sn36Pb2Ag.
- The 100In is suitable for joining brittle materials, such as GaAs, Si, and glass, and for lower temperature applications. On the other hand, 96.5Sn3.5Ag is for tough materials, such as ceramics and for higher temperature applications such as under the hood of automobile.

## 3.3 Fan-In Panel-Level Chip-Scale Packages (PLCSPs)

Panel level assembly and fabrication is a very high-throughput packaging technology. This is because, in addition to area utilization (10–20% less silicon-area wastes with rectangular chips on rectangular panels than on circular wafers), the size of the

temporary panel carrier is usually larger than the standard-size wafer, e.g., 300 mm [131–140].

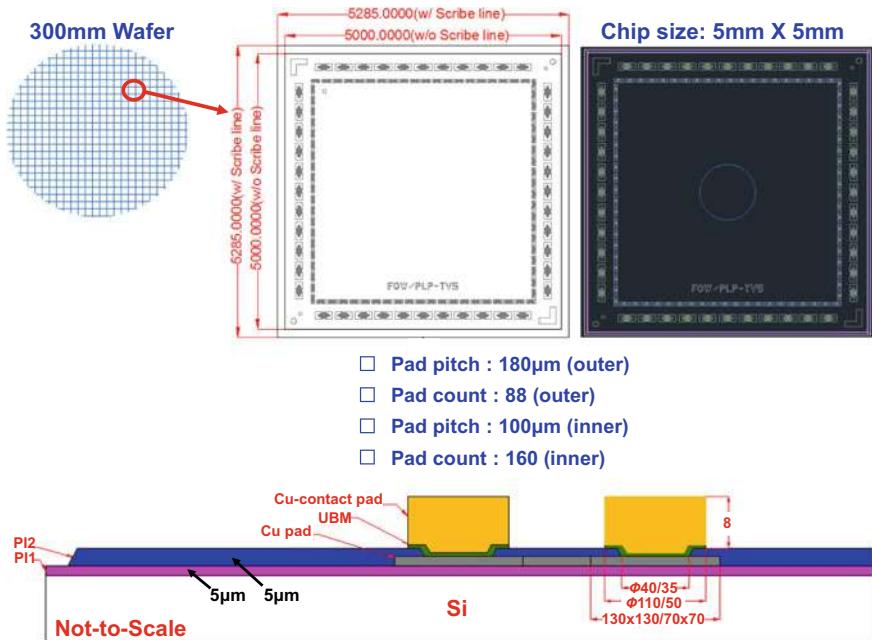
Panel level with multiple wafers could be an even higher (depends on the number of wafers) throughput packaging technology. This is due to, in addition to larger panel size, the saving of dicing the device wafers into individual dies, and pick and place (P&P) time of the dies to the temporary large panel carrier. One of the bottlenecks of panel level with multiple wafers packaging is the availability of equipment and method to fabricate the key elements of the packages such as the RDLs and micro vias on the large temporary panels.

In this section, a method of utilizing the existing sizes of temporary PCB panel carriers and the corresponding PCB equipment for multiple wafers is presented [85, 86]. Since most of the panel sizes are in rectangular shapes, we dice some or all of the round wafers (with orientation flat or not) into two or more pieces. The ratio of dicing of the wafer (the size of each piece) depends on the wafer size, and the available panel size and the corresponding PCB equipment. The feasibility of this method is demonstrated on a 20" × 20" (508 mm) temporary panel carrier with the corresponding PCB equipment for making the RDLs. The 300-mm wafer is diced in two pieces and four pieces.

In this study, the process steps are first laminating a two-side thermal release film (tape) on a 20" × 20" PCB panel carrier. It is followed by making cavities on another PCB panel and attaching it to the PCB with tape. Then, attach the diced and undiced wafers (face-up) through the cavities on the PCB panel with tape. It is followed by laminating an Ajinomoto build-up film (ABF), laser drilling, desmearing, electroless Cu, dry film lamination, laser direct imaging (LDI) and development, PCB Cu plating, and etching and then, solder-mask and pad-finishing formations. Finally, debond the wafers from the temporary panel, mount the solder balls, and dice the wafers into individual ordinary panel-level chip-scale packages (PLCSPs). The present process is not only very high throughput but very low cost because it uses a large PCB panel and all PCB (without any semiconductor) equipment. Reliability assessments such as the drop test and thermal cycling test of the PLCSP PCB assembly are performed and the results including failure analysis are presented and discussed.

### 3.3.1 Test Chip

Figure 3.17 shows the test chip under consideration. It can be seen that the chip size is 5 mm × 5 mm on a 300 mm wafer (a total of 2,324 chips). The chip thickness is 798 μm. There are two rows of peripheral pads; namely, one is with 88 outer pads which are on a 180 μm pitch, and the other is with 160 inner pads which are on a 100 μm pitch. It can also be seen from Fig. 3.17 that: (1) for the outer peripheral pads: the Cu pad size is 130 μm × 130 μm, the Ti/Cu (0.1/0.2 μm) UBM pad size is 110 μm in diameter, the passivation (PI2) opening is 40 μm in diameter, and the Cu-contact pad size is 110 μm in diameter and 8 μm in thickness, and (2) for the inner peripheral pads: the Cu pad size is 70 μm × 70 μm, the UBM pad size is 50 μm

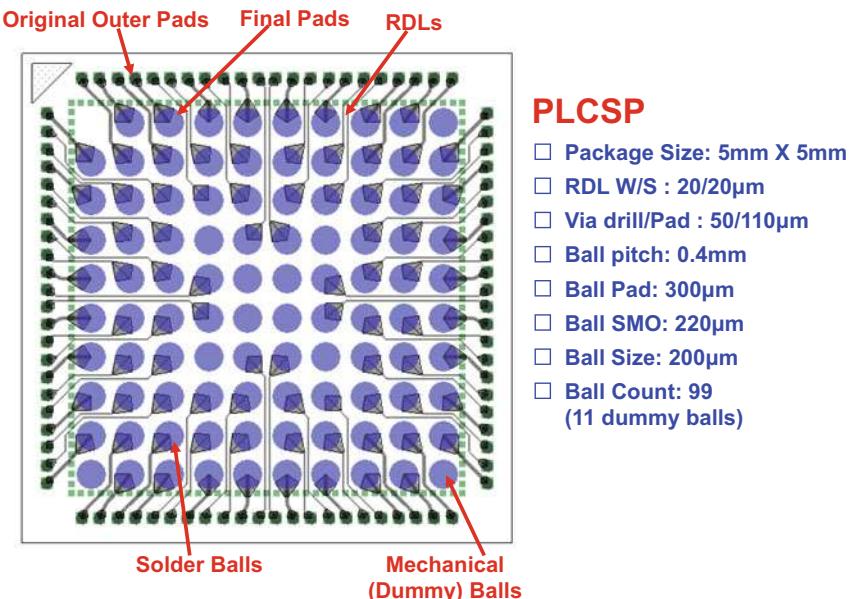


**Fig. 3.17** Top view and cross section view of the test chip

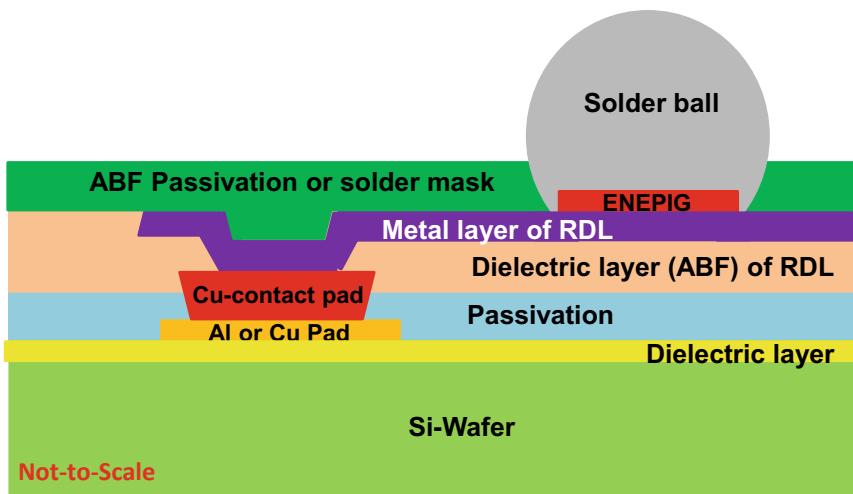
in diameter, the passivation (PI2) opening is 35  $\mu\text{m}$  in diameter, and the Cu-contact pad size is 50  $\mu\text{m}$  in diameter and 8  $\mu\text{m}$  in thickness. For both cases, the Cu pads are daisy chained with a 3- $\mu\text{m}$ -thick copper.

### 3.3.2 Test Package

Figure 3.18 schematically shows the test package under consideration. It can be seen that, in this study, only the outer rows of peripheral pads are redistributed (fan-in) to the interior of the chip. The new (final) pad size is 300  $\mu\text{m}$  in diameter with a solder mask opening of 220  $\mu\text{m}$  in diameter. There are 99 pads and solder balls (11 are dummy). The solder ball size is 200  $\mu\text{m}$  and is on a 0.4-mm pitch. Figure 3.19 schematically shows the cross-sectional view of the test package. It can be seen that there is one RDL which consists of the dielectric insulation layer and the metal conductor layer. The thickness of the dielectric layer and metal layer is 20  $\mu\text{m}$ . The metal linewidth and spacing of the RDL are 20/20  $\mu\text{m}$ . The via opening of the dielectric layer of the RDL is 50  $\mu\text{m}$ .



**Fig. 3.18** Schematic of the test package



**Fig. 3.19** Schematic of the cross section of the test package

### 3.3.3 PLCSP Process Flow

#### (A) Panel and Wafer Preparation

Before making the RDL for the PLCSP, the diced and undiced wafers have to be placed in two temporary panels as shown schematically in Figs. 3.20 and 3.21. First, a PCB panel is laminated with a two-side thermal release film (tape) at room temperature. Then, make cavities (e.g., 300, 15 mm in diameter) on another PCB panel and attach them to the PCB with the tape. It is followed by attaching the diced and undiced wafers (face-up) through the cavities on the PCB panel with the tape. These are the first three steps of the process flow shown in Fig. 3.22a. Figure 3.23 shows the  $20'' \times 20''$  panels with one 12" (300 mm) wafer, two one-half 12" wafers, and one one-fourth 12" wafer. Now, it is ready to make the RDL for the ordinary PLCSP.

#### (B) RDL Fabrication

First, laminate a  $20\text{-}\mu\text{m}$  ABF on the whole panel with wafers (Fig. 3.23a). The ABF is an electrical insulation (dielectric) of complex circuit on PCB/package substrate [85, 86]. It functions just like the polyimide for the dielectric layer of the RDLs of

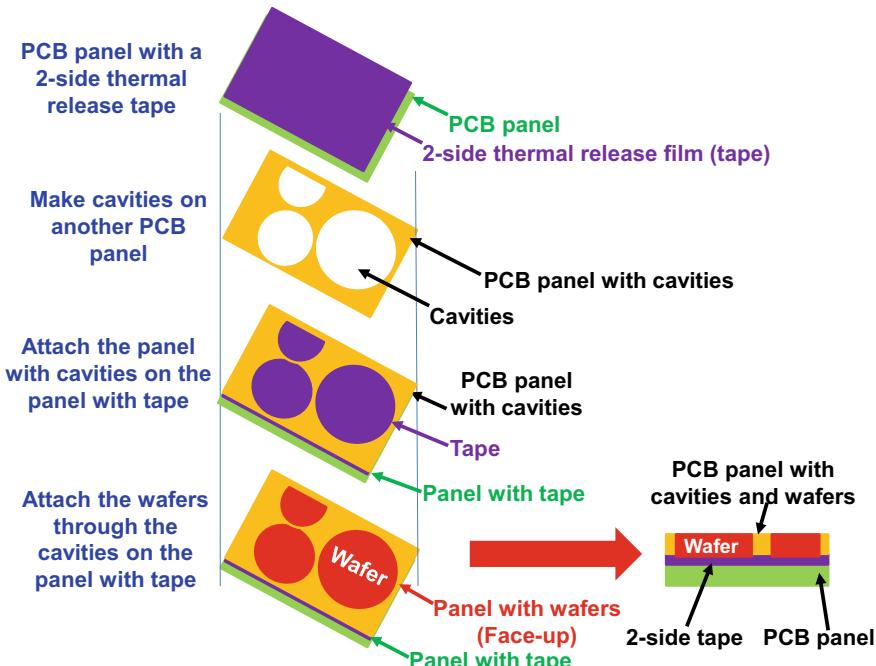
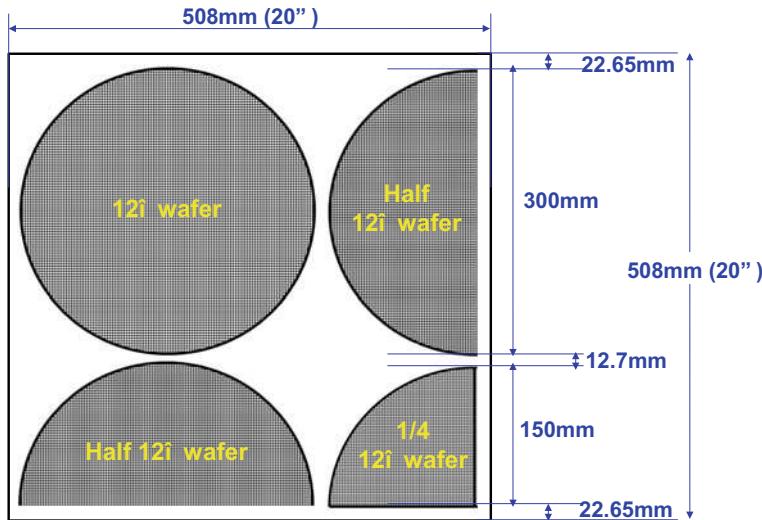


Fig. 3.20 PLCSP made from the chips on a panel with diced and undiced wafers



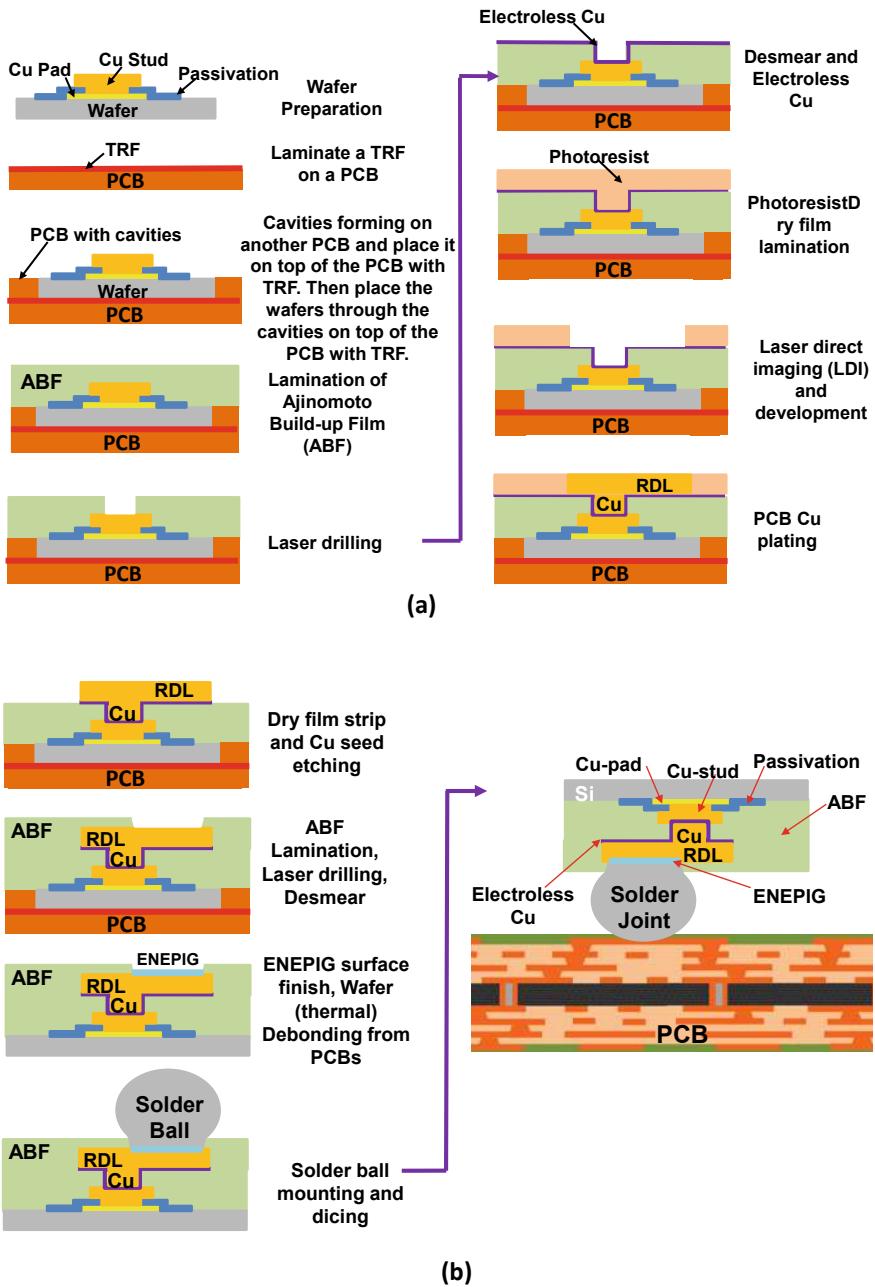
**Fig. 3.21** Layout of the 20" × 20" panel with diced and undiced wafers. The packages are made from the chips on a panel with multiple wafers

WLCSP. ABF is of lower cost than polyimide. However, the line thickness, width, and spacing of the conductor layer with ABF are much larger than those with polyimide. There are two operating stages of the ABF: (1) at the first stage, the temperature is 120 °C for 30 s at vacuum condition and then press (0.68 MPa) for 30 s with the temperature and vacuum on, and (2) at the second stage, the temperature is 100 °C and press (0.58 MPa) for 60 s.

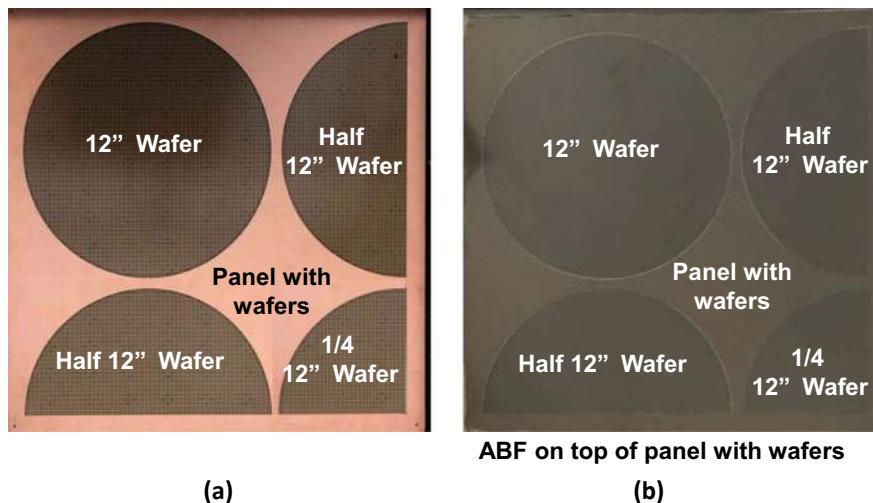
Figure 3.23a shows the panel with the diced and undiced wafers without the ABF, while Fig. 3.23b shows the one with the ABF. Then laser drill the vias on the ABF and the results are shown in Fig. 3.24. The typical diameter of the top via is 63 μm, the bottom via is 43 μm, and the via thickness is 18 μm. The target values are via diameter = 50 μm and via thickness = 20 μm. It is followed by desmearing, electroless Cu for seed layers, photoresist dry film lamination, LDI and development, and PCB Cu plating. Then, strip off the dry film and etch off the seed layer to obtain the RDL as shown in Fig. 3.25. The typical metal linewidth of the RDL is between 16 and 25 μm. The target value is 20 μm. Thus, there are rooms for improvements.

### (C) Solder Resist Opening and Solder Ball Mounting

Next, laminate a 20-μm ABF on the whole panel (for the solder mask), laser drill, desmear, and surface finish with an electroless nickel electroless palladium immersion gold (ENEPIG) as shown in Figs. 3.26 and 3.27. The diameter of the solder resist opening (SRO) is targeted for 0.22 mm. First, we try ultraviolet (UV) laser. However, since the energy of UV laser is too big, the laser passes through the Cu



**Fig. 3.22** **a** PLCSP process steps with diced/undiced wafers. **b** PLCSP process steps (continue)



**Fig. 3.23** Temporary panel with diced and undiced wafers. **a** Without ABF. **b** With ABF

pad (Fig. 3.26a). Then, we try the carbon dioxide (CO<sub>2</sub>) laser and the results (top via diameter = 199.3 μm, bottom via diameter = 157.1 μm, and the via thickness = 20 μm) are acceptable and shown in Fig. 3.26b. The desmear condition is sweller at 60 °C for 2 min/KMnO<sub>4</sub> at 80 °C for 8 min. The results are shown in Figs. 3.26c–e. It can be seen that: (1) 3 μm of ABF is etched off after SRO desmear; (2) most of via bottoms are cleaned; and (3) the top via diameter is 202.6 μm, the bottom via diameter is 165.2 μm, and the via thickness is 17 μm.

The chemicals and operating conditions such as temperature and time used for making the ENEPIG surface finishing are shown in Fig. 3.27. It can be seen that the target thickness of the electronless Ni is 5  $\mu\text{m}$ , the electroless Pd is 0.05  $\mu\text{m}$ , and the immersion Au is 0.05  $\mu\text{m}$ . Then, thermal (230 °C for 10 min) debond the wafers from the panels and mount the solder balls on the wafers. Figure 3.28 shows the fixture for solder ball mounting for half of a 300-mm wafer. It consists of two stencils (one for fluxing and the other for solder ball mounting), vacuum, and wafer holder. It is followed by dicing the wafer into individual PLCSps. Figure 3.29 shows an individual ordinary PLCSp.

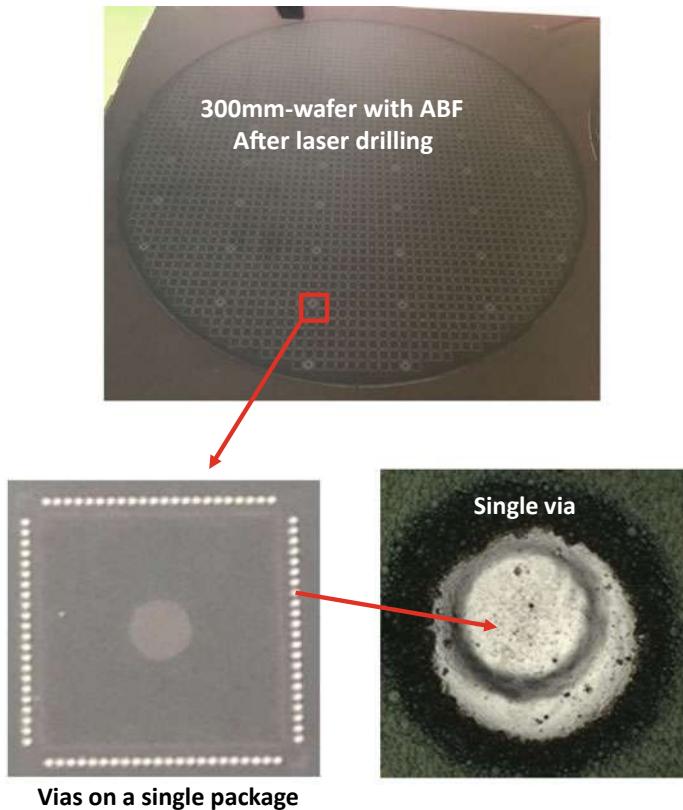


Fig. 3.24 Laser-drilled vias on ABF

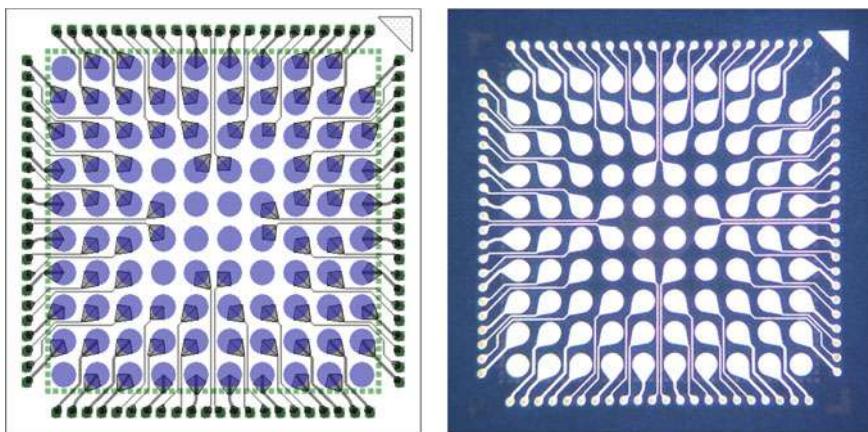
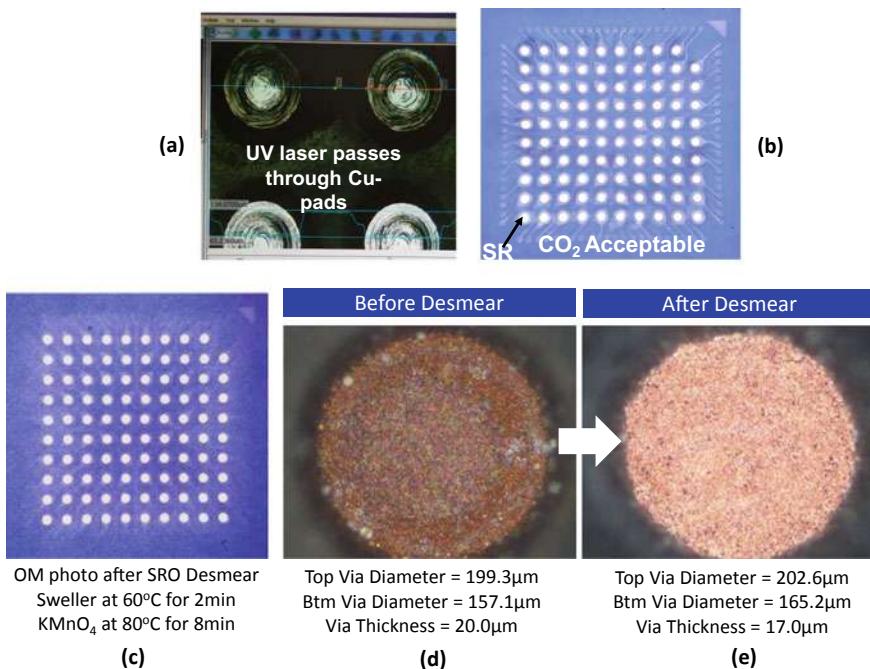


Fig. 3.25 RDL on a PLCSP



**Fig. 3.26** SRO by UV laser and CO<sub>2</sub> laser. Before and after desmear. **a** UV-laser passes through Cu-pad. **b** CO<sub>2</sub>-laser is acceptable. **c** Photo of SRO after desmear. **d** Close-up: before desmear. **e** Close-up: after desmear

Process	Cleaner	Micro-etching	Acid dip	Pre dip	Activator	EL-Ni	EL-Pd	I-Au
Chemical	ACL-738	SPS	H <sub>2</sub> SO <sub>4</sub>	H <sub>2</sub> SO <sub>4</sub>	MFD-5	NPR-4	TPD-21	TWX-40
Temp.(°C)	50	30	R.T	R.T	30	80	50	80
Thickness Target	NA	0.3-0.5μm	NA	NA	NA	5μm	0.05μm	0.05μm
Dipping time (min)	1	0.5	1	1	1	25	10	15

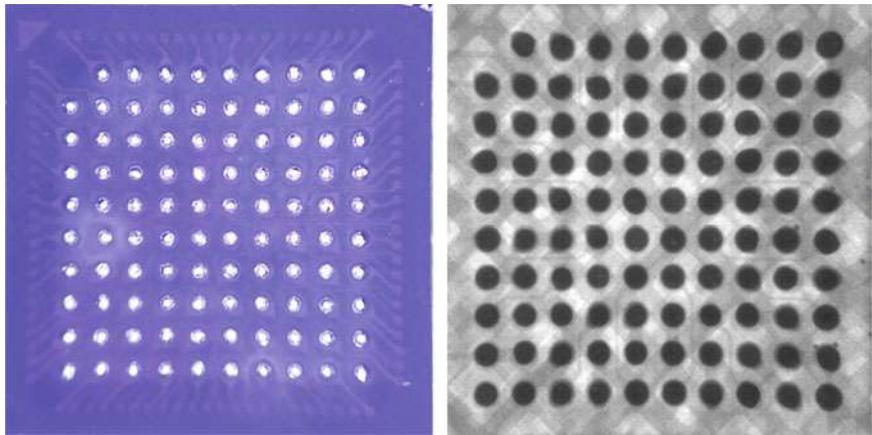
Unit's OM photo after ENEPIG

Via's OM photo before & after ENEPIG

**Fig. 3.27** ENEPIG surface finishing



**Fig. 3.28** Solder ball mounting fixtures for half of a wafer

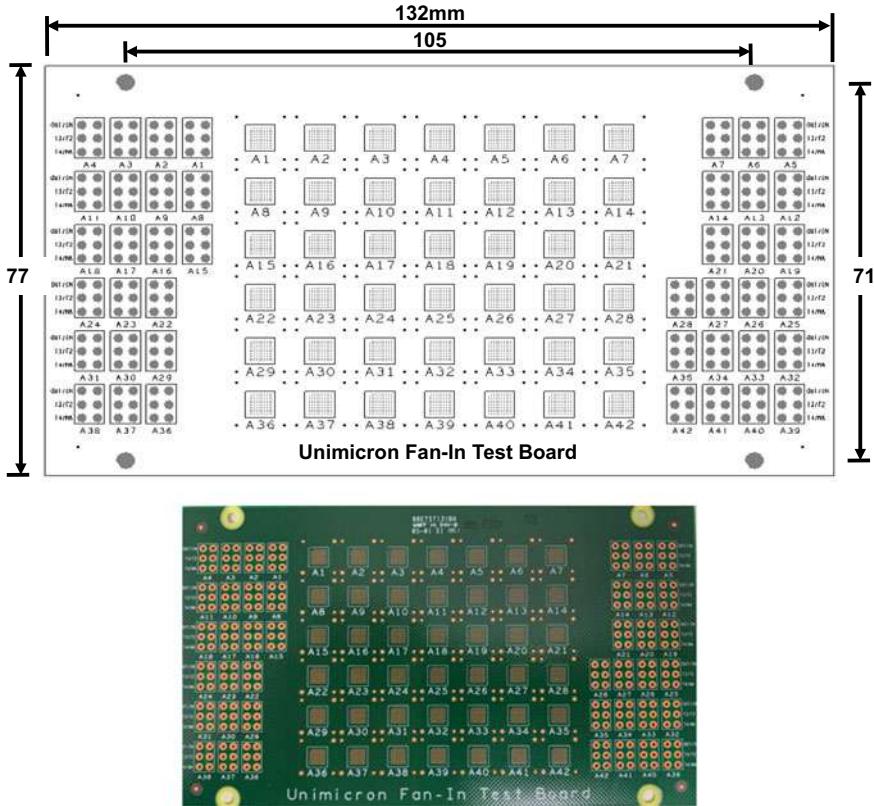


**Fig. 3.29** Individual PLCSP

### 3.3.4 PCB Assembly of the PLCSP

#### (A) PCB

The PCB for the fan-in panel-level package is made of FR-4 and is shown in Fig. 3.30 [85, 86]. It can be seen that there are  $6 \times 7 = 42$  PLCSP sites on the board. The

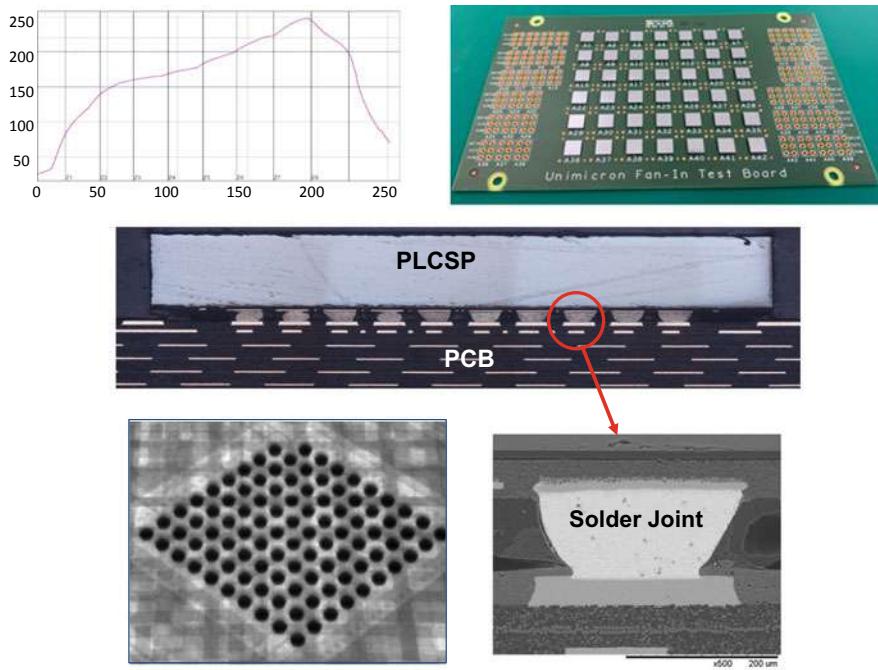


**Fig. 3.30** Test board for PLCSP

dimensions of the PCB are  $132 \text{ mm} \times 77 \text{ mm} \times 0.65 \text{ mm}$ , and there are six layers. There are 99 pads (with a pitch = 0.4 mm) for each PLCSP. The pad with a diameter equal to 0.3 mm is non-solder mask defined, and its surface finish is an organic solderability preservative (OSP).

### (B) SMT of the PLCSP on PCB

A standard lead-free surface-mount technology (SMT) process [99] is used to assemble the PLCSPs on the test PCB. Figure 3.31 shows the reflow temperature profile, the PCB assembly, the X-ray image of a single-package PCB assembly, the cross section, and a solder joint. It can be seen that the ordinary PLCSP PCB assembly is properly done and passes the electrical continuity test.



**Fig. 3.31** PLCSP PCB reflow temperature profile and assembly, X-ray image, and its cross section

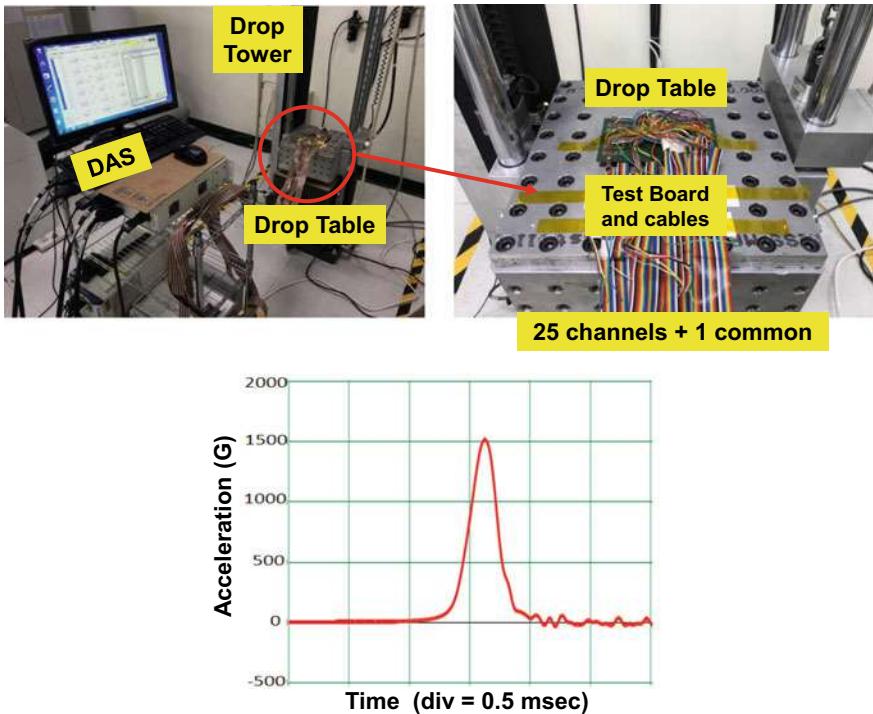
### 3.3.5 Drop Test of PLCSP PCB Assembly

#### (A) Drop Test Setup and Spectrum

The reliability assessment of the ordinary PLCSP on PCB assembly without underfill is by a shock (drop) test. The test setup is according to the JEDEC Standard JESD22-B111, as shown in Fig. 3.32. It consists of a drop tower, a drop table for the PCB with samples. There are 25 channels plus one common, and a DAS (data acquisition system). The height of the drop table is 69.85 mm, which yields the drop spectrum with 1500 G/ms (1500 Gs, 0.5 ms half-sine pulse), as shown in Fig. 3.32. The drop condition is 30 drops. The failure criterion is when the measured resistance during the drop test reaches  $1000\Omega$  as shown in Fig. 3.33b. Less than that, it is considered no failure as shown in Fig. 3.33a.

#### (B) Drop Test Results and Failure Analysis

After 30 drops, there is not any failure, i.e., the measurement resistance data ( $<1000\Omega$ ) are like those shown in Fig. 3.33a. Thus, the ordinary PLCSP assembly passes the drop test. However, cross section of some of the un-failed samples shows that actually

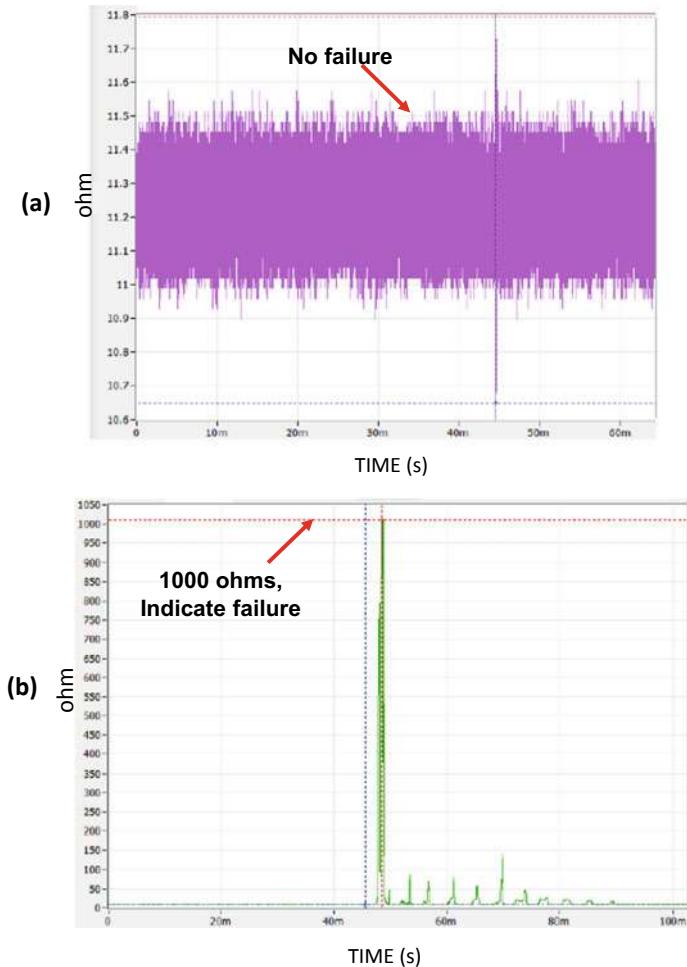


**Fig. 3.32** Drop test setup and the drop spectrum

there are some small cracks as shown in Fig. 3.34. The test continues to 50 drops and there is one failure at 31 drops, i.e., the measurement resistance date ( $>1000\Omega$ ) is like that shown in Fig. 3.34b. Cross section of the failed sample shows that the solder joint is totally cracked (opened) as shown in Fig. 3.35.

### 3.3.6 Thermal Cycling Test of PLCSP PCB Assembly

The PCB assembly of the ordinary PLCSP is put into a thermal cycling chamber as shown in Figs. 3.36 and 3.37 [123]. The temperature in the chamber during test is measured through a thermal couple (in air) and is shown in Fig. 3.38. It can be seen that the temperature profile is basically  $-55 \Leftarrow 125^\circ\text{C}$  at 50-min cycle. The sample size of the ordinary PLCSP is 48.



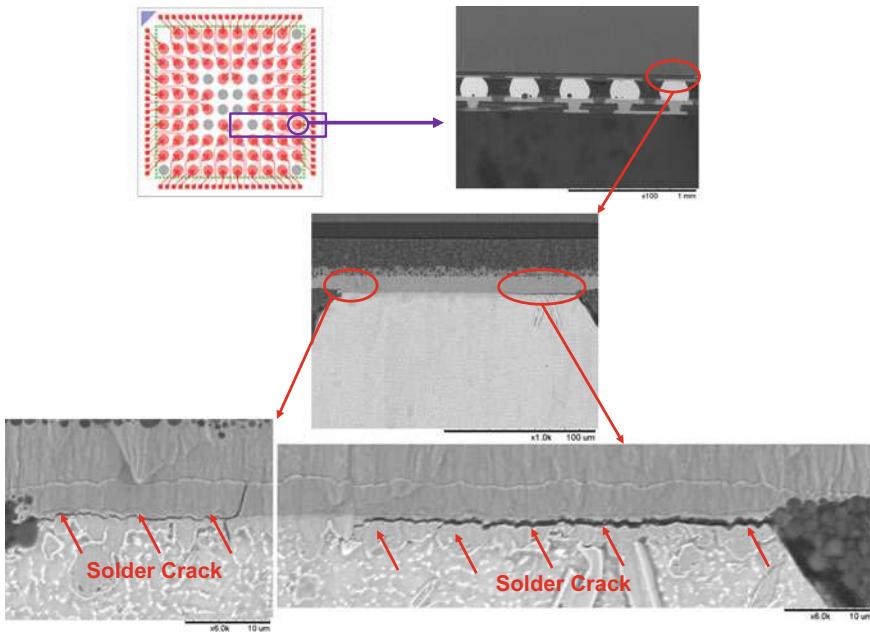
**Fig. 3.33** Failure criteria. **a** No failure. **b** Sample failed

#### (A) Failure Criterion

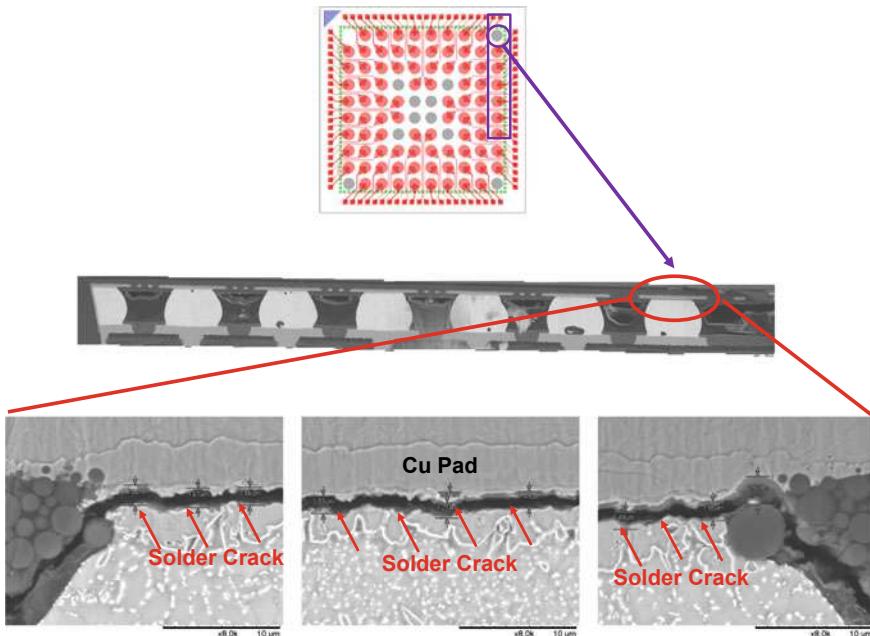
The failure criterion is when the resistance of the daisy chain of the ordinary PLCSP PCB assembly increases by 50%. The cycle at which the first solder joint of a PLCSP failed is considered as the cycle-to-failure of the PLCSP.

#### (B) Test Results of the PLCSP PCB Assembly

The thermal cycling test results of the ordinary PLCSP PCB assembly are tableted in Table 3.3. It can be seen that there are 48 failures. The median (50%) rank [99] are determined from  $F(x) = (j - 0.3)/(n + 0.4)$ , where  $j$  = failure order number and  $n$



**Fig. 3.34** The DAS show there is no failure, but actually there are small cracks of the solder joint



**Fig. 3.35** The DAS show there is a failure and actually the solder joint is totally opened (cracked)

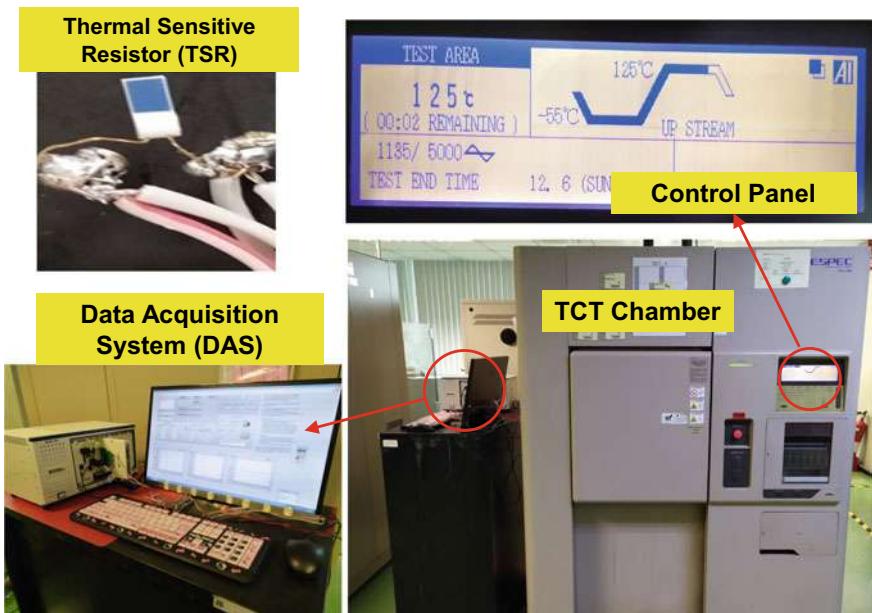


Fig. 3.36 Thermal cycling chamber, thermal couple, and data acquisition system

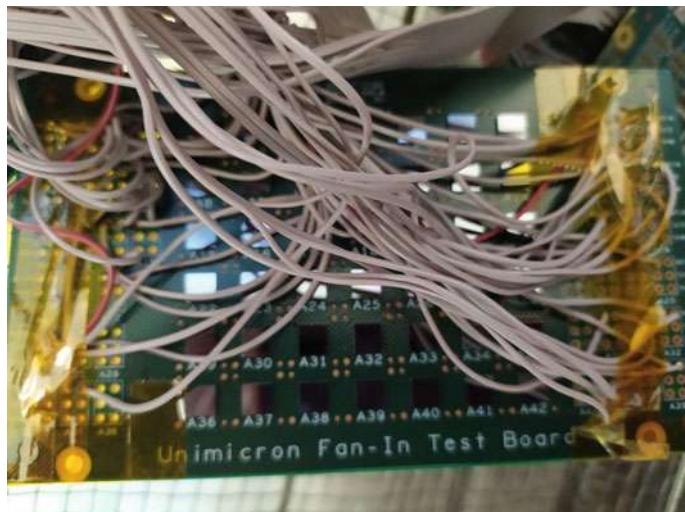
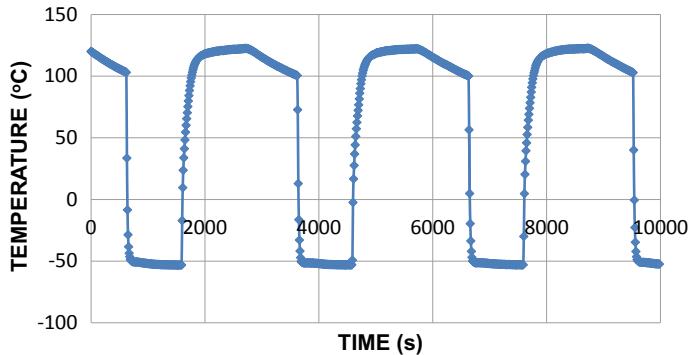


Fig. 3.37 Test boards with ordinary PLCSPIs inside thermal cycling chamber



**Fig. 3.38** Thermal cycling temperature profile

= sample size = 48. These data are plotted into a Weibull distribution and is shown in Fig. 3.39. It can be seen that the characteristic life ( $\theta$ ) (63.2% failed) = 368 cycles and the Weibull slope ( $\beta$ ) is = 3.34.

There are a few reasons for the low reliability of the ordinary PLCSP. First, this is the very first time to use a panel as temporary carrier with multiple diced and un-diced wafers. Second, this is the very first time to use all PCB equipment. Third, the thickness of the ordinary PLCSP is too thick (0.79 mm), i.e., too much thermal expansion mismatch between the silicon chip ( $2.5 \times 10^{-6}/^{\circ}\text{C}$ ) and the FR-4 PCB ( $18.5 \times 10^{-6}/^{\circ}\text{C}$ ).

For other required ranking ( $G$ ), the percent rank ( $z$ ) can be determined by ( $z$  is the percent rank of the  $j$ th value in  $n$  samples) [99]:

$$1 - (1 - z)^n - nz(1 - z)^{n-1} - \frac{n(n-1)}{2!}z^2(1 - z)^{n-2} - \dots - \frac{n(n-1) \cdots (n-j+1)}{(j-1)!}z^{j-1}(1 - z)^{n-j+1} = G$$

For 90% confidence level, we need the 5% rank ( $G = 5\%$ ) and 95% rank ( $G = 95\%$ ) and they are also listed in Table 3.3. For examples, with  $n = 48$  and  $G = 5\%$ , the percent failure rank ( $z$ ) is 0.11 for  $j = 1$  and is 0.75 for  $j = 2$ . Another examples, with  $n = 48$  and  $G = 95\%$ , the percent failure rank ( $z$ ) is 6.05 for  $j = 1$  and is 9.51 for  $j = 2$ .

Confidence is defined as the probability that a given interval determined from the test data will contain the population parameters, such as (using Weibull as an example) the characteristic life and Weibull slope. Confidence applies to the test itself and reliability applies to the product!

Figure 3.40 shows the Weibull plot of the solder joints of the PLCSP PCB assemble at 90% confidence. It can be seen that the true characteristic life ( $\theta_t$ ) at 90% confidence is  $326 \leq \theta_t \leq 403$  cycles. cycles.

**Table 3.3** Thermal cycling test results of the ordinary PLCSP at median rank, 5% rank, and 95% rank

Failure Order	Cycles-to-Failure	F(x)		
		Median (50%) rank	90% confidence	
			5% rank	95% rank
1	155	1.44	0.11	6.05
2	177	3.51	0.75	9.51
3	180	5.57	1.73	12.54
4	186	7.64	2.90	15.37
5	193	9.70	4.20	18.06
6	195	11.77	5.59	20.66
7	199	13.84	7.05	23.19
8	200	15.90	8.57	25.65
9	203	17.97	10.15	28.07
10	205	20.04	11.76	30.44
11	213	22.10	13.42	32.77
12	213	24.17	15.10	35.07
13	250	26.23	16.83	37.34
14	250	28.30	18.57	39.57
15	250	30.37	20.35	41.78
16	250	32.43	22.15	43.97
17	250	34.50	23.98	46.13
18	250	36.56	25.83	48.27
19	300	38.63	27.70	50.38
20	300	40.70	29.59	52.48
21	300	42.76	31.50	54.55
22	300	44.83	33.43	56.60
23	300	46.90	35.39	58.63
24	300	48.96	37.36	60.65
25	350	51.03	39.35	62.64
26	350	53.09	41.37	64.61
27	350	55.16	43.40	66.57
28	350	57.23	45.45	68.50
29	350	59.29	47.52	70.41
30	350	61.36	49.62	72.30
31	400	63.43	51.73	74.17
32	400	65.49	53.87	76.02
33	400	67.56	56.03	77.85

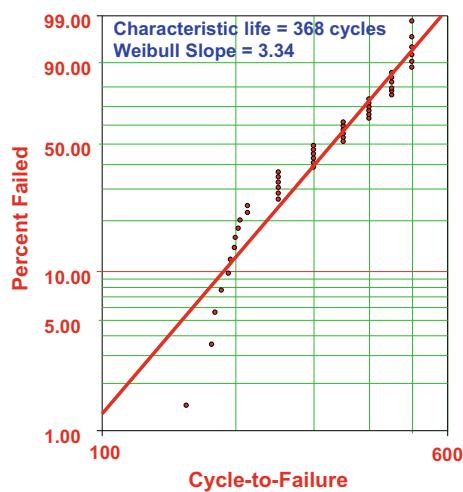
(continued)

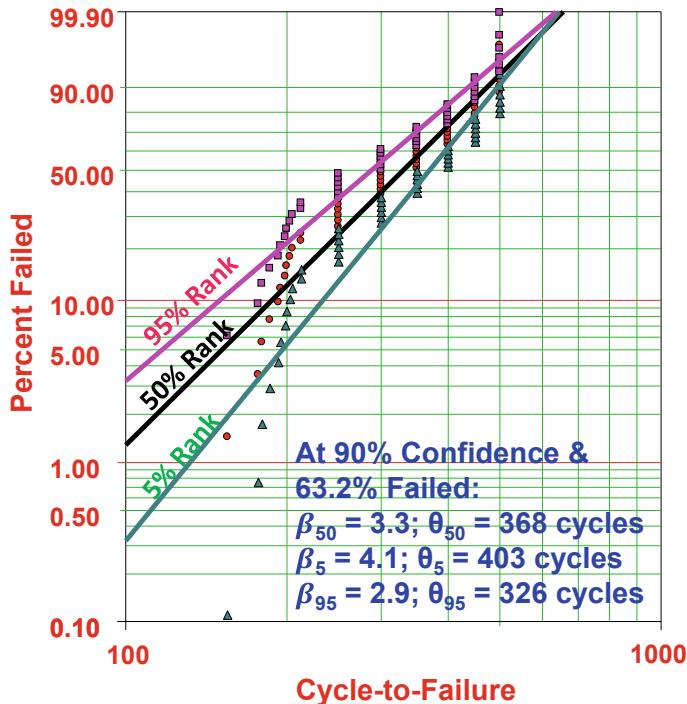
**Table 3.3** (continued)

Failure Order	Cycles-to-Failure	F(x)	90% confidence	
			Median (50%) rank	5% rank
34	400	69.62	58.22	79.65
35	400	71.69	60.43	81.43
36	400	73.76	62.66	83.17
37	450	75.82	64.93	84.90
38	450	77.89	67.23	86.58
39	450	79.16	69.56	88.24
40	450	82.02	71.93	89.85
41	450	84.09	74.35	91.43
42	450	86.15	76.81	92.95
43	500	88.22	79.4	94.41
44	500	90.29	81.94	95.80
45	500	92.35	84.63	97.10
46	500	94.42	87.46	98.27
47	500	96.48	90.49	99.25
48	500	98.55	93.95	99.89

Sample size = 48

**Fig. 3.39** Weibull plot of the ordinary PLCSP solder joint at median rank



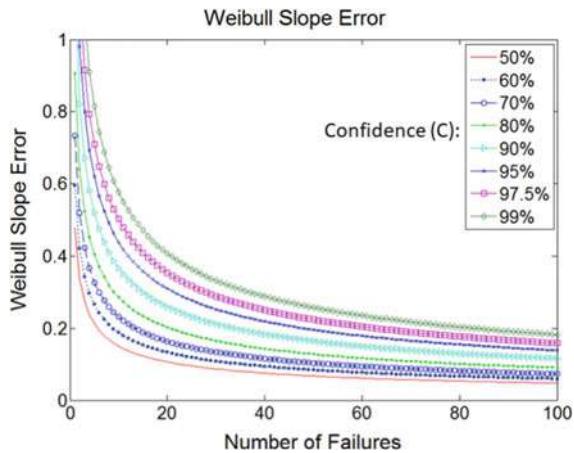


**Fig. 3.40** Weibull plot of the ordinary PLCSP solder joint at 90% confidence

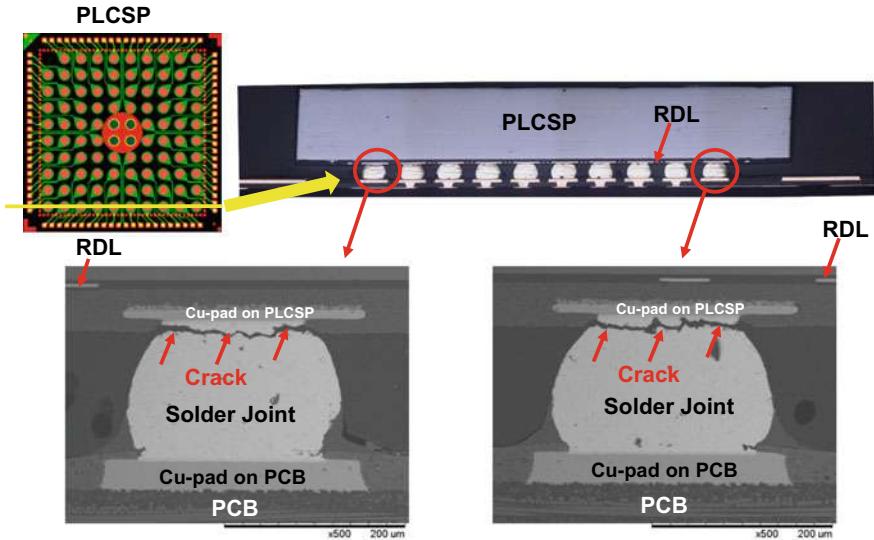
To predict the true Weibull slope ( $\beta_t$ ) of the population, it is necessary to estimate the Weibull slope error in relation to the sample size and the required confidence level. The error ( $E$ ) in the Weibull slope depends on the number of failures ( $N$ ) and the required confidence level ( $C$ ), which can be estimated from Fig. 3.41 [99]. In the case of the ordinary PLCSP,  $C = 90\%$  and  $N = 48$ , then  $E = 0.22$ . Thus, the true Weibull slope is  $2.6 \leq \beta_t \leq 4.1$ .

### (C) Failure Location and Failure Mode of the Ordinary PLCSP PCB assembly

The failure location and failure mode of the ordinary PLCSP solder joints are shown in Fig. 3.42. It can be seen that the failure location of the PLCSP assembly occurs along the outer rows near the corners of solder joints. The failure mode of the PLCSP PCB assembly is the cracking of solder near the interface between the chip and the bulk solders.



**Fig. 3.41** Weibull slope error

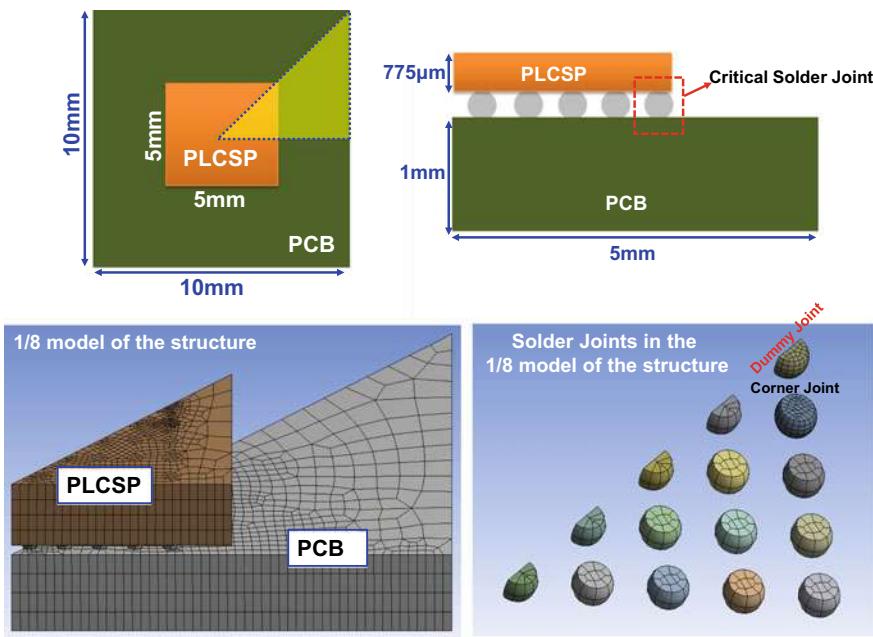


**Fig. 3.42** Failure location and failure mode of the ordinary PLCSP solder joints

### 3.3.7 Thermal Cycling Simulation of the PLCSP PCB Assembly

#### (A) Structure and Kinematic Boundary Conditions

The PCB assembly of the PLCSP is schematically shown in Fig. 3.43. Because of the symmetry about the  $x$ -axis, the  $y$ -axis, and the diagonal axes, only one-eighth of



**Fig. 3.43** PCB assembly of the ordinary PLCSP and its modeling

the structure is modeled. From the concept of distance to neutral point (DNP) [99], the corner solder joint does not carry any power/ground/signal but functions as a dummy (mechanical) solder joint used for absorbing the maximum stress and strain. Despite the overall economy of elements in the one-eighth of model, selective mesh refinement is used to concentrate highly refined elements in the solder joints where failure is anticipated. In the present PCB assembly, failure would be predicted in the solder joints with the greatest DNP and near the chip corners as shown in Fig. 3.43. Thus, highly refined meshes are applied to these solder joints. The other joints are coarsely meshed. The 3-D Solid186 element of ANSYS 2019 is used.

### (B) Material Properties

The material properties of the PLCSP PCB assembly are given in Table 3.4. All the material properties are assumed to be constant except for those of the solder. The Sn<sub>3</sub>Ag<sub>0.5</sub>Cu is assumed to obey the generalized Garofalo creep equation as shown in Table 3.1.

**Table 3.4** Material properties of the ordinary and 6-side molded PLCSPs

Materials	CTE ( $10^{-6}/^{\circ}\text{C}$ )	Young's modulus (GPa)	Poisson's ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Silicon	2.8	131	0.278
Solder	$21 + 0.017T$	$49 - 0.07T$	0.3
ABF	7.0	7.0	0.3

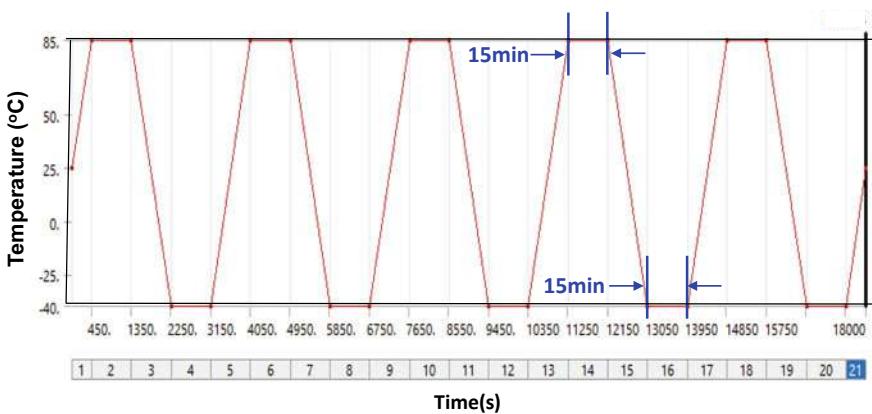
*T* is in Celsius

### (C) Kinetic Boundary Condition

The temperature profile shown in Fig. 3.44 is to be imposed on the PLCSP PCB assembly. Five temperature cycles are executed. It can be seen that the temperature condition is from  $-40$  to  $85$   $^{\circ}\text{C}$ . The cycle time is 60 min and the ramp-up, ramp-down, dwell-at-hot, and dwell-at-cold are each 15 min.

### (D) Thermal Cycling Simulation Results

The deformed shape (color contours) and the undeformed shape (dark lines) of the PLCSP PCB assembly are shown in Fig. 3.45a at 450 s ( $85$   $^{\circ}\text{C}$ ) and in Fig. 3.45b at 2250 s ( $-40$   $^{\circ}\text{C}$ ). It can be seen that: (1) at  $85$   $^{\circ}\text{C}$ , the PCB expanges more than the silicon chip and curves outward; the solder joint (especially the corner one with the largest DNP) is subjected to mainly shear deformation and the structure is deformed to a concave shape (smiling face) and (2) at  $-40$   $^{\circ}\text{C}$ , the PCB shrinks more than the silicon chip and curves inward; the structure is deformed to a convex shape (crying



**Fig. 3.44** Temperature profile for simulation

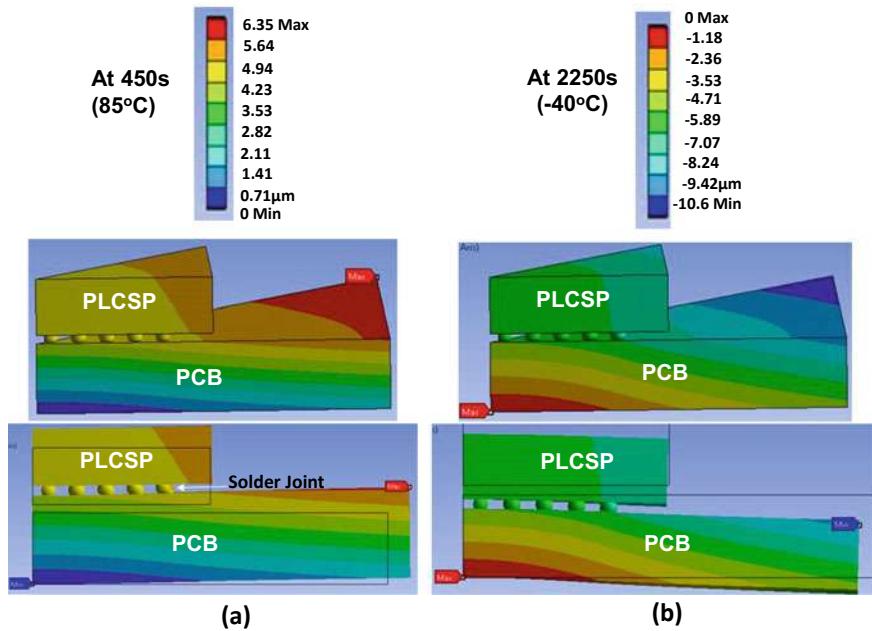


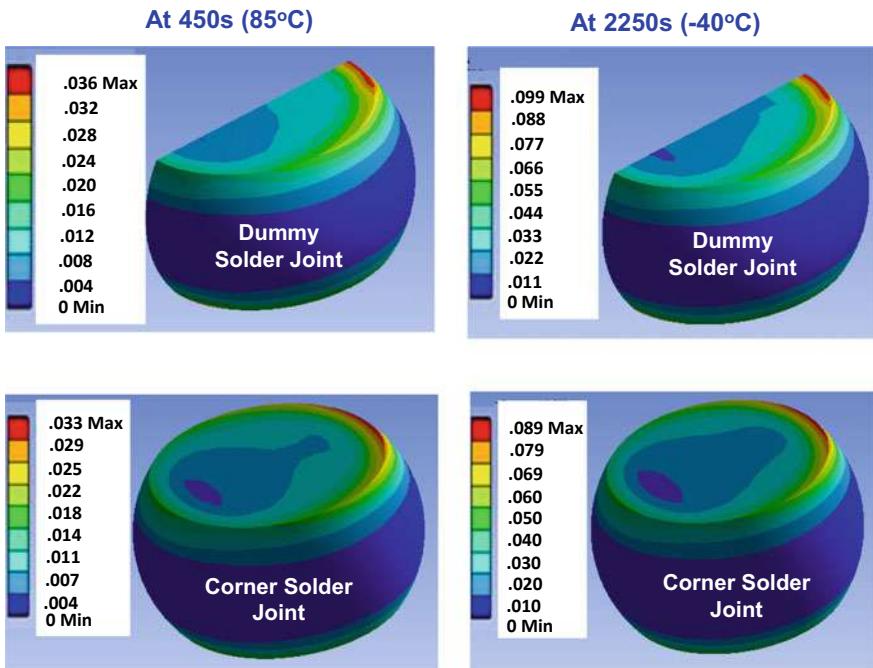
Fig. 3.45 Deformed and undeformed shapes. **a** At 450 s (85 °C). **b** At 2250 s (-40 °C)

face). These results show that the kinematic and kinetic boundary conditions of the modeling structure are not wrongly prescribed.

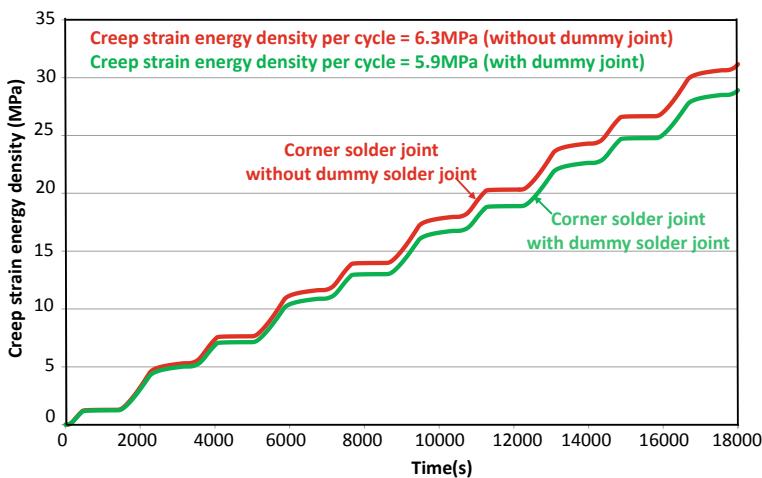
The largest accumulated creep strain occurs (the failure location) at the dummy solder joint and corner solder joint (Fig. 3.43). Figure 3.46 shows the maximum accumulated creep strain contours at 450 s (85 °C) and 2250 s (-40 °C). The following has been observed.

- For both the dummy solder joint and corner solder joint, the maximum accumulated creep strain occurs near the interface between the chip and the bulk solder of the solder joint and it is the driving force for cracking (the failure mode) of the solder joint. Thus, any failure should occur at this location.
- The maximum accumulated creep strain per cycle at the dummy solder joint (0.063) is larger than that (0.056) at the corner solder joint. Thus, it is better to leave the dummy solder joint there to absorb the maximum stress and strain and to prolong the life of the corner solder joint (Fig. 3.42).
- The creep strain energy density time history at the dummy solder joint and corner solder joint is shown in Fig. 3.44. It can be seen that the creep strain energy density per cycle (6.9 MPa) at the dummy solder joint is larger than that (5.9 MPa) at the corner solder joint.

As a matter of fact, Fig. 3.47 shows the comparison of the creep strain energy density time history between the cases with and without the dummy solder joint. It



**Fig. 3.46** Accumulated creep strain contours in the dummy and corner solder joints at 450 s ( $85\text{ }^{\circ}\text{C}$ ) and 2250 s ( $-40\text{ }^{\circ}\text{C}$ )



**Fig. 3.47** Creep strain energy density time history in the dummy and corner solder joints

can be seen that the creep strain energy density at the corner solder joint is larger without the dummy solder joint.

### ***3.3.8 Summary and Recommendation***

Some important results and recommendations are summarized as follows.

- A very high-throughput and low-cost packaging method for fabricating the fan-in chip-scale package has been developed. This method utilizes the existing PCB panel and the corresponding PCB equipment. Since the PCB panel is in a rectangular shape, some of the device wafers have been diced into two or more pieces so the panel is fully utilized.
- A test chip has been designed and the test-chip wafer has also been fabricated.
- A PLCSP has been designed and demonstrated.
- The panel and wafer preparations of the ordinary PLCSP are very simple. First, laminate a two-side thermal release tape on a panel. Then make cavities on another panel and attach them to the panel with the tape. It is followed by attaching the diced and undiced wafers with dies facing upward through the cavities on the panel with the tape.
- The RDL for the PLCSP has been fabricated by an all PCB process and equipment. The dielectric layer of the RDL has been made by an ABF, the vias have been made by laser drilling and desmearing, and the metal layer of the RDL has been made by electroless Cu for the seed layer, photoresist and LDI, and then PCB Cu plating. The typical metal linewidth and spacing of the RDL of the PLCSP were between 16 and 25  $\mu\text{m}$ . The target value was 20  $\mu\text{m}$ . Thus, there are rooms for improvements.
- For the solder mask of the PLCSP, we used ABF. For the SRO, we recommend the CO<sub>2</sub> laser, because the power of the UV laser is too big and will pass through the Cu pad. The surface finishing was ENEPIG.
- For solder ball mounting of the PLCSP, the fixtures have been designed and fabricated. It consists of vacuum, holders, and two stencils; one is for fluxing and the other is for solder ball mounting.
- A PCB with daisy chains has been designed and fabricated for the assembly of the PLCSPs and for their reliability testing.
- SMT assembly of the PLCSPs on the reliability test PCB has been successfully done and passed the electrical continuity test.
- Failure analysis of the thermal cycling test results indicated the failure location of the PLCSP is along the outer row (near the corner) of solder joints. The failure mode is the cracking of solder near the interface between the chip and the bulk solders.
- The simulation of the PLCSP PCB assembly showed that the maximum accumulated creep strain occurs near the interface between the chip and the bulk solders.

Thus, any failure should occur (initiate) at this location. This confirms with the failure mode from the thermal cycling test results.

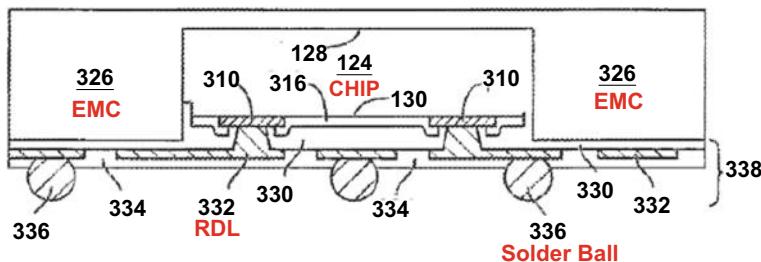
### 3.4 Six-Side Molded Wafer-Level Chip-Scale Packages

Recently, because: (a) of the delamination of the dielectric layer in the front-side of the WLCSP, which is particularly true for advanced nodes (<14 nm process technology) products with fragile polyimides, (b) of the back-side chipping and sidewall cracking due to the mechanical blade dicing the wafer, (c) of the concern of the handling and SMT (surface mount technology) pick and place to damage the chip, and (d) in automotive electronics, the trends are driving lead-free solder joint reliability for new functions such as the advanced driver-assistance systems (ADAS), under-the-hood operations often require high sustained heating/cooling temperatures, a higher-cost 5-side or 6-side molded WLCSPs are getting tractions [87–98, 123].

The 5-side molded WLCSP was first patented (e.g., US8456002) [87] in 2011 (Fig. 3.48) and published [56, 88–90] by Statschippac and is called eWLCSP (encapsulated WLCSP). The backside and the four side walls of the chip are protected by molding. Basically, this is the eWLB (embedded wafer-level ball grid array) or chip-first (face-down) fan-out wafer-level packaging method [141].

In 2015, UTAC published a paper on 6-side protected WLCSP [91]. The four side-walls and the front-side of the chip are protected by molding and the backside of the chip is protected by a conventional method such as the lamination of a tape (film). In 2016, SPIL published a similar paper on 5-side protected (four side walls and the front side of the chip) and called it mWLCSP (molded WLCSP) [92]. They also proposed a 6-side protection by laminating an epoxy film at the backside of the chip.

Since 2018, Huatian Technology have been publishing a series of papers on 5-side or 6-side molded WLCSP [93–95]. They actually make the 6-side molded WLCSP. Their process is very similar to that of UTAC and SPIL, except they mold the backside of the chip instead of using the (conventional) lamination of a film.



**Fig. 3.48** Statschippad's patent on 5-side molded WLCSP [87]

In 2020, MediaTek and SPIL published a paper [96] on 5-side and 6-side molded WLCSPs. Their process is similar (by using a temporary carrier) to that of Statschippac but there are some differences.

In this section, the 5-side or 6-side molded WLCSPs by Statschippad, UTAC, SPIL, Huatian, and MediaTek will be briefly mentioned.

### 3.4.1 eWLCSP by Statschippac

Figure 3.49 shows the images of Statschippac's eWLCSP [88–90], which can be seen that basically it is the fan-out chip-first with face-down method. They test and then dice the original device wafer into KGDs (known good dies), pick and place the individual KGDs on a temporary wafer carrier, and then compression mold an EMC (epoxy molding compound) on the re-constituted wafer as shown in Fig. 3.49. It is followed by debonding the temporary carrier, fabricating the redistribution-layer (RDL), solder ball mounting, and dicing the re-constituted wafer into individual eWLCSPs (Fig. 3.49) [88–90]. It can be seen that the backside and four sides of the chip are protected by EMC.

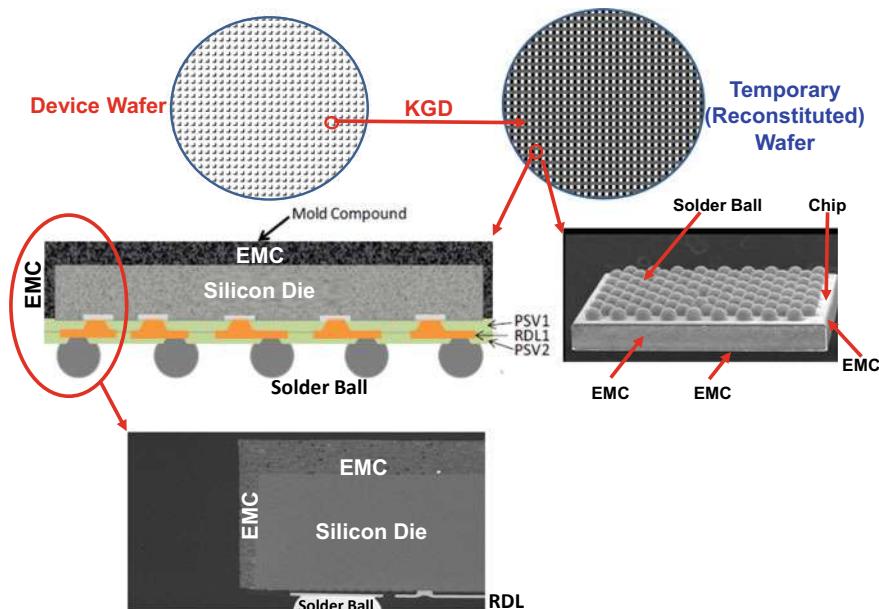
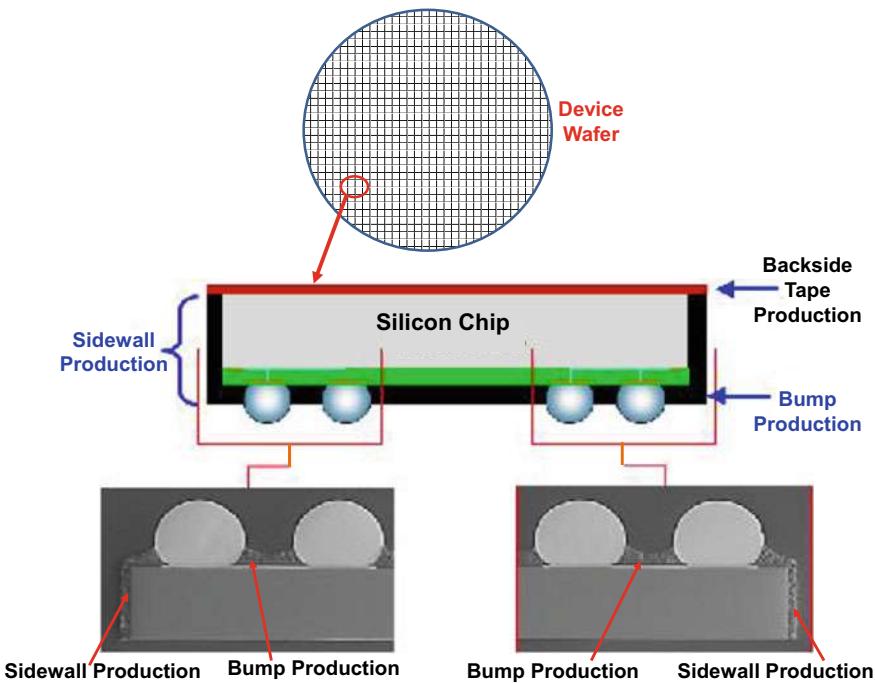


Fig. 3.49 Statschippad's eWLCSP [88]



**Fig. 3.50** UTAC's WLCSP

### 3.4.2 WLCSP by UTAC

UTAC's method [91] in making the 5-side molded WLCSP is very different from that of Statschippac. They use the original device wafer (without dicing and P&P of the KGDs on a temporary wafer) to make the RDL; solder ball mounting, dicing, molding and then grinding. It is followed by dicing the device wafer into individual WLCSPs (Fig. 3.50).

### 3.4.3 mWLCSP by SPIL

SPIL's method on 5-side protected (four side walls and the front side of the chip) is very similar to that of UTAC. They called it mWLCSP (molded WLCSP) [92] (Fig. 3.51). SPIL also proposed a 6-side protection by laminating an epoxy film at the backside of the chip.

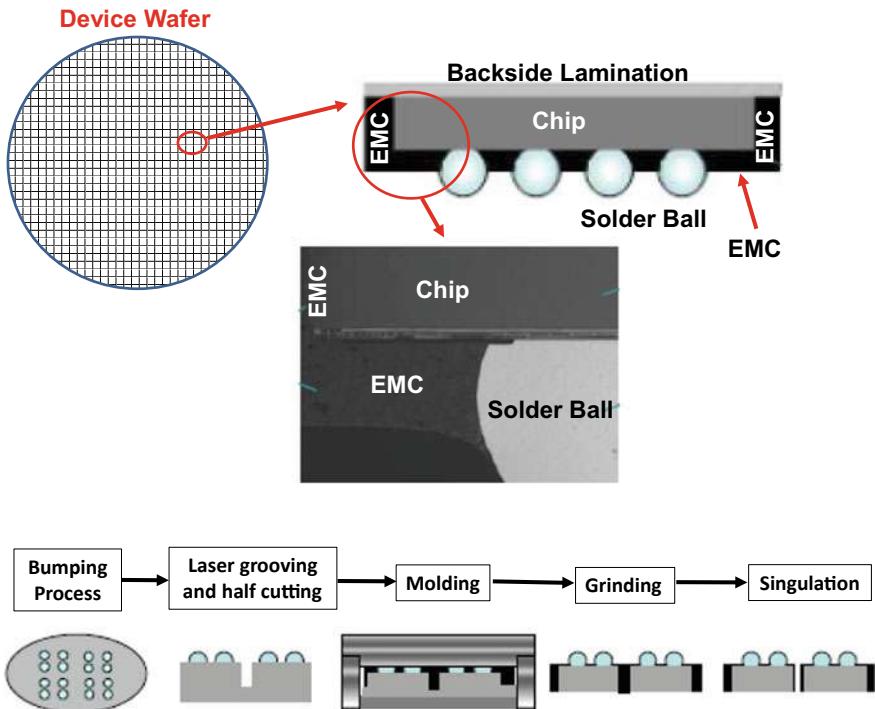


Fig. 3.51 SPIL's mWLCSP [92]

### 3.4.4 WLCSP by Huatian

Huatian's method [93–95] in making the 6-side molded WLCSP (four side walls, front side, and back side of the chip) is very similar to that of UTAC [91] and SPIL [92]. Their structure is shown in Fig. 3.52 and process flow is shown in Fig. 3.53. With laser dicing such as those given by ASM [101–103], the saw street can be as little as 60  $\mu\text{m}$ .

### 3.4.5 mWLCSP by SPIL and MediaTek

Figure 3.54 shows the 5-side molded mWLCSP and 6-side molded mWLCSP by SPIL and MediaTEK [96]. The process for the 5-side molded WLCSP is shown in Fig. 3.55 and for the 6-side molded WLCSP is shown in Fig. 3.56. Similar to Statschippac [88–90], which use a temporary carrier, but their process is quite different [96].

For the 5-side molded WLCSP, it can be seen from Fig. 3.55 that on the device wafer, they make the RDL (metal layer and dielectric layer) and UBM and then dice

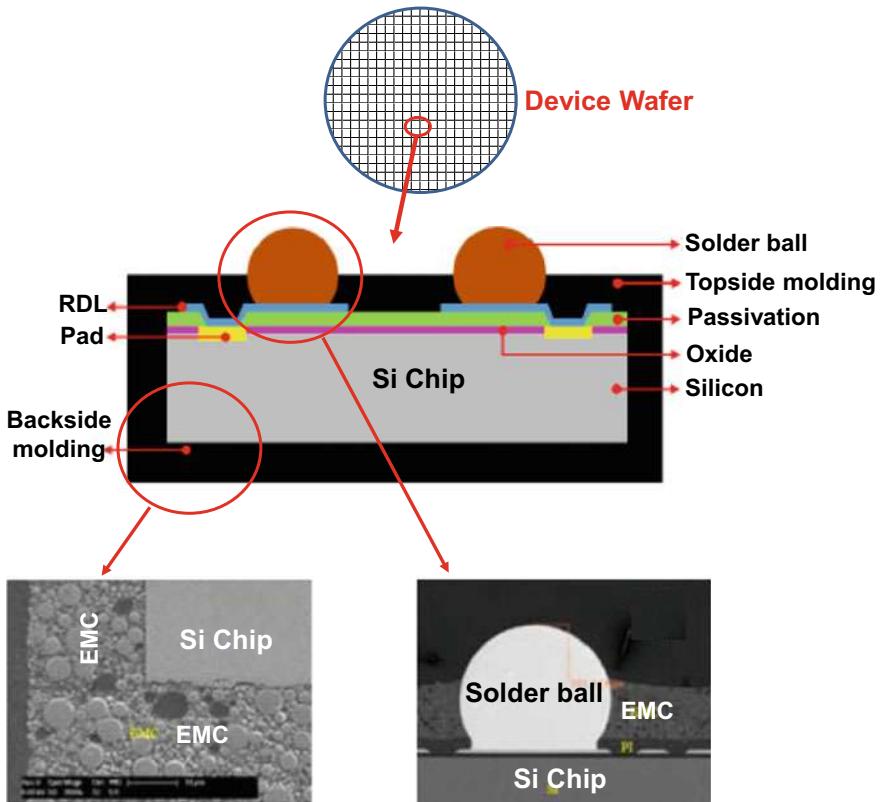
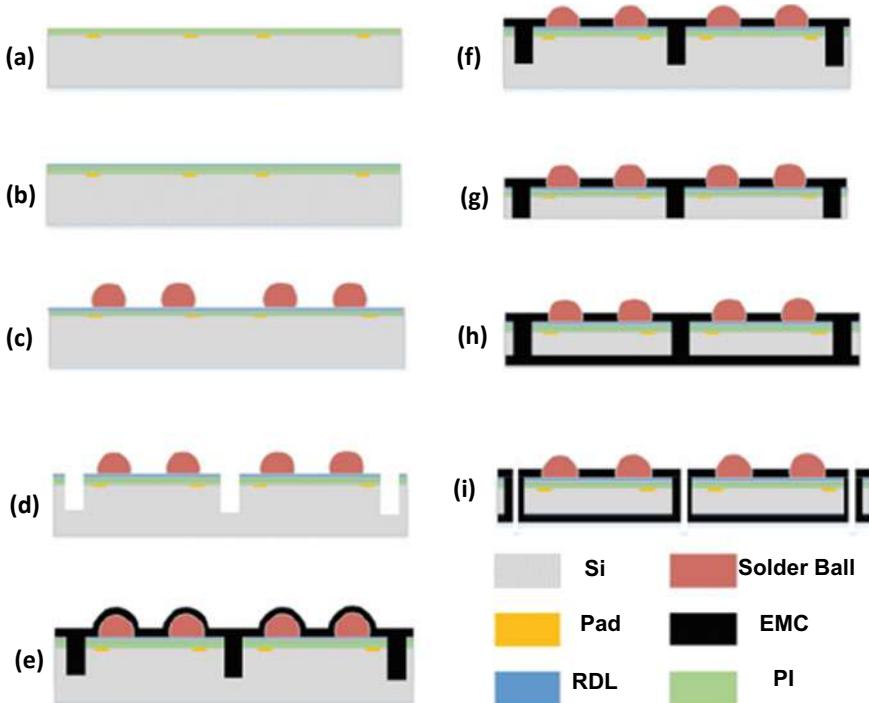


Fig. 3.52 Huatian's WLCSP [95]

the wafer into individual chips. It is followed by P&P the chips (face-down) on a temporary carrier and molded with an EMC. Then remove the temporary carrier and mount the solder balls. Finally, dice the reconstituted wafer into individual 5-side molded WLCSPs [96].

For the 6-side molded WLCSP, it can be seen from Fig. 3.56 that on the device wafer, they make the RDL and then dice the wafer into individual chips. It is followed by P&P the chips (face-up) on a temporary carrier and then molded with an EMC. Then backgrind the EMC to expose the contact pad of the chips. It is followed by debonding the temporary carrier, making the passivation, UBM, and solder balling. Then, backgrind the backside of the chip with EMC and perform backside lamination. Finally, dice the reconstituted wafer into individual 6-side molded mWLCSPs [96].



**Fig. 3.53** Key process steps in Huatian's WLCSP [95]

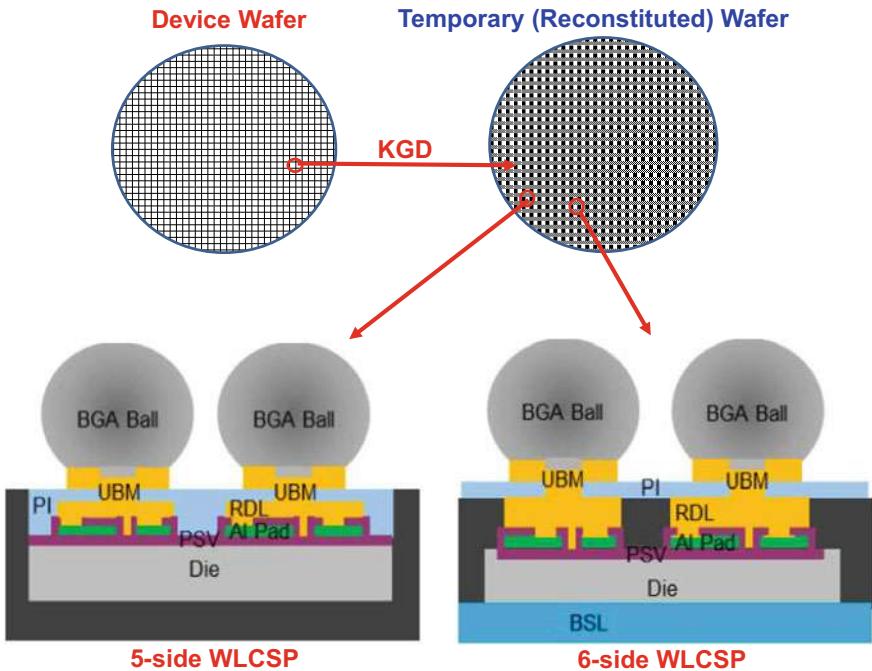
### 3.4.6 Summary and Recommendation

Some important results and recommendation are summarized as follows.

- The 5-side or 6-side molded WLCSP from various companies have been briefly mentioned.
- Basically, there are two different methods to make the molded WLCSP. One is by using a temporary wafer carrier for the individual KGDs and the other is working directly on the device wafer.

## 3.5 Six-Side Molded Panel-Level Chip-Scale Packages

In this section, the ordinary PLCSP fabricated in Sect. 3.3 is further to be fabricated into a 6-side molded PLCSP.



**Fig. 3.54** SPIL/MediaTEK's 5-side and 6-side molded mWLCSP [96]

### 3.5.1 The 6-Side Molded PLCSP Structure

The cross-sectional view of the test package is shown in Fig. 3.57 [97, 98]. It can be seen the ordinary PLCSP is protected (molded) in all 6 sides; front-side, back-side, and four side walls of the chip. There is one RDL which consists of the dielectric layer and the metal layer and their thickness is 20  $\mu\text{m}$ . The metal linewidth and spacing of the RDL are 20/20  $\mu\text{m}$ . The via opening of the dielectric layer of the RDL is 50  $\mu\text{m}$ .

The key process steps in fabricating the 6-side molded PLCSP are shown in Fig. 3.58a, b. In Sect. 3.3 we have completed most of the steps. In this section, we first thermal (230 °C for 10 min) debond the wafers from the panels and mount the solder balls on the wafers as shown in Figs. 3.59a, b. Figure 3.59c shows an x-ray image of the ordinary PLCSP. The average solder ball height is equal to 150  $\mu\text{m}$ .

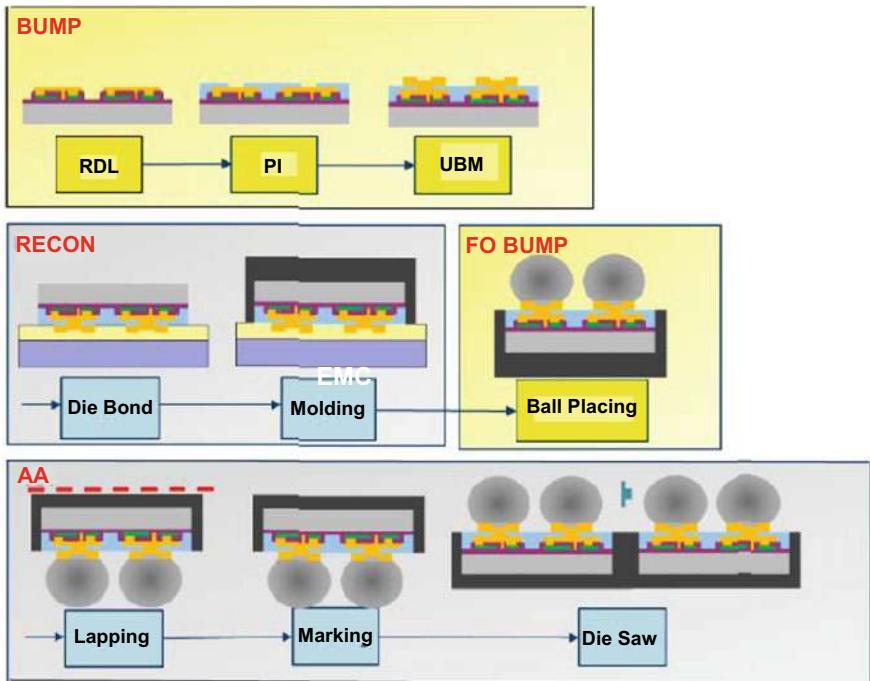


Fig. 3.55 SPIL/MediaTEK's 5-side molded mWLCSP key process steps [96]

### 3.5.2 Cutting and EMC Molding of Wafer from the Front-Side

Next, the wafer with RDL and solder balls is half-cut from its front-side with a mechanical dicing saw, Fig. 3.60a. Laser grooving [101–103] is better but optional. The average trench width is equal to  $170 \mu\text{m}$  and the average depth is equal to  $394 \mu\text{m}$  as shown in Fig. 3.60.

Then, it is followed by laminating an EMC (ABF) with  $200 \mu\text{m}$ -thickness on the front-side of the wafer, Fig. 3.60b. Because of the lamination pressure, the EMC is filled in the trench as shown in Fig. 3.60b. It can be seen that the thickness of the EMC is about  $150 \mu\text{m}$  (not  $200 \mu\text{m}$ , because some of the EMC materials go to fill the trenches in the saw streets), which is equal to the total height of EMC ( $202.4 \mu\text{m}$ ) minus the (solder mask + dielectric =  $50 \mu\text{m}$ ) thickness.

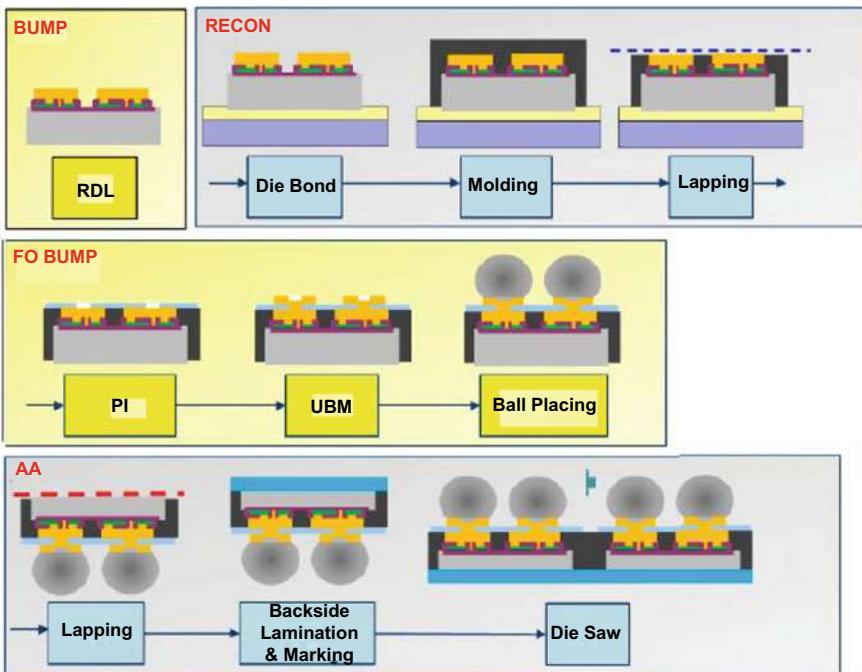


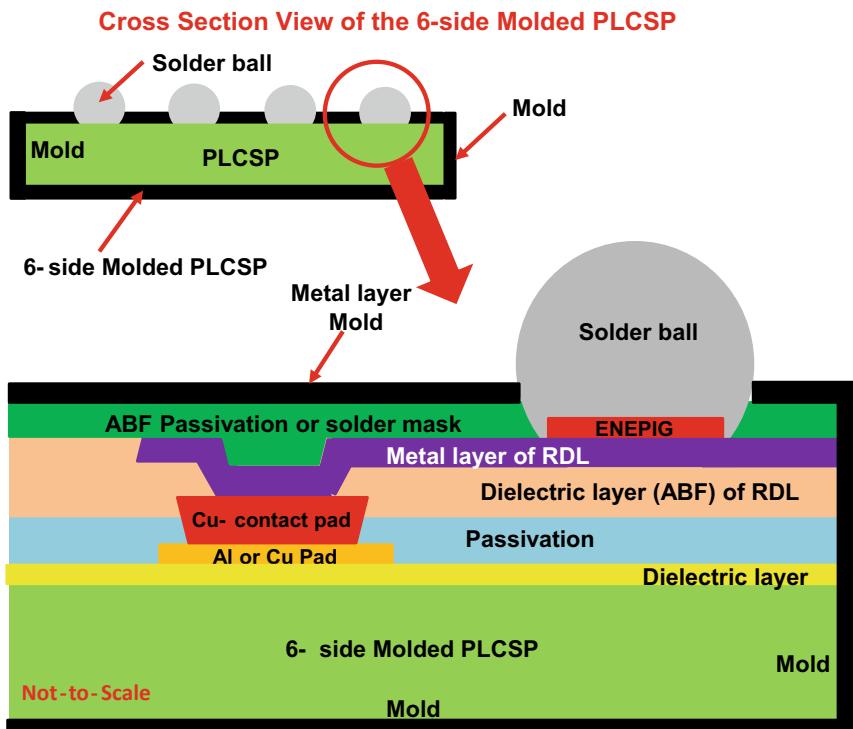
Fig. 3.56 SPIL/MediaTEK's 6-side molded mWLCSP key process steps [96]

### 3.5.3 Backgrinding and Wafer Backside Molding

Now, it is time to perform the backgrinding of the wafer from its backside. This continues until the EMC in the trench is seen (about  $390\ \mu\text{m}$ ) as shown in Fig. 3.61. Thus, the chip thickness of the 6-side molded PLCSP becomes  $390\ \mu\text{m}$ . Next, a  $25\text{-}\mu\text{m}$  EMC (ABF) is laminated at the backside of the wafer.

### 3.5.4 Plasma Etching and Dicing

Next, it is time for plasma etching to remove some of the EMC from the solder balls as shown in Fig. 3.58b. The plasma conditions are: temperature =  $132\ ^\circ\text{C}$ , power =  $2700\ \text{W}$ , pressure =  $0.33\ \text{torr}$ , and  $\text{O}_2/\text{CF}_4 = 2000\ \text{sccm}$ . The etch rate is about  $1.76\ \mu\text{m}/\text{min}$ . Figure 3.62a shows the ordinary PLCSP. Figure 3.62b shows the 6-side molded PLCSP with front-side EMC molding. Figure 3.62c shows the solder joint of the 6-side molded PLCSP after plasma etching. The average solder ball height of an ordinary PLCSP is  $148\ \mu\text{m}$ , Fig. 3.62d, and the average solder ball height of a 5-side or 6-side molded PLCSP is  $103\ \mu\text{m}$ , Fig. 3.62e.



**Fig. 3.57** Unimicron's 6-side molded PLCSP

Then, dice the wafer into individual 6-side molded PLCSPs. The 3D view and the cross-sectional view of the 6-side molded PLCSP are shown, respectively in Figs. 3.63a and 3.64b. It can be seen that the average side wall molding is  $\sim 78 \mu\text{m}$ , the average front-side molding is  $\sim 53 \mu\text{m}$ , and the average standoff height of the solder ball is  $\sim 100 \mu\text{m}$ . The chip thickness is  $390 \mu\text{m}$ .

### 3.5.5 Test PCB

The PCB for the 6-side molded PLCSP is the same as that for the PLCSP and is shown in Fig. 3.64. The dimensions of the PCB are  $132 \text{ mm} \times 77 \text{ mm} \times 0.65 \text{ mm}$ , and there are six layers. There are 99 pads (with a pitch =  $0.4 \text{ mm}$ ) for each PLCSP. The pad with a diameter equal to  $0.3 \text{ mm}$  is non-solder mask defined, and its surface finish is an organic solderability preservative (OSP).

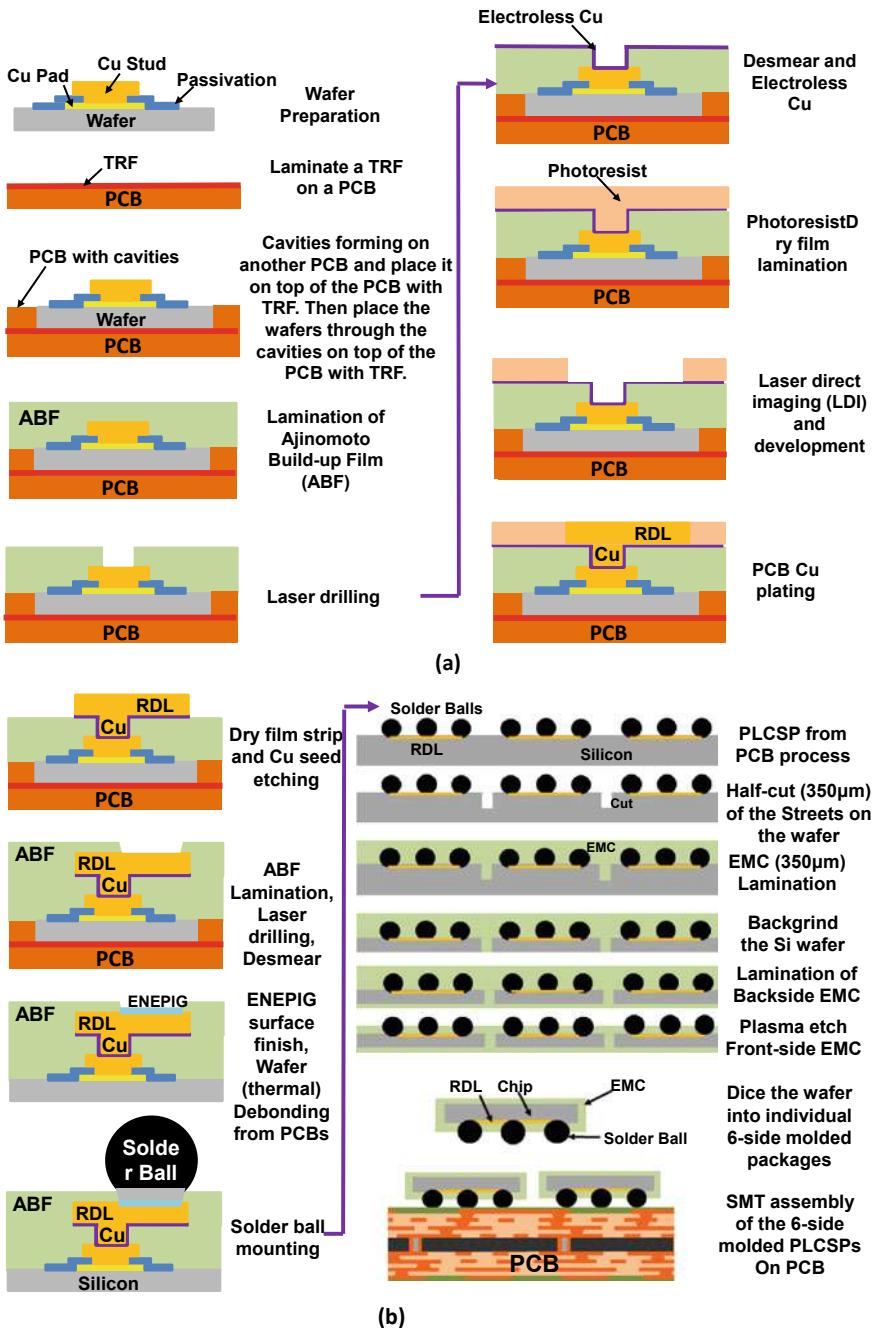
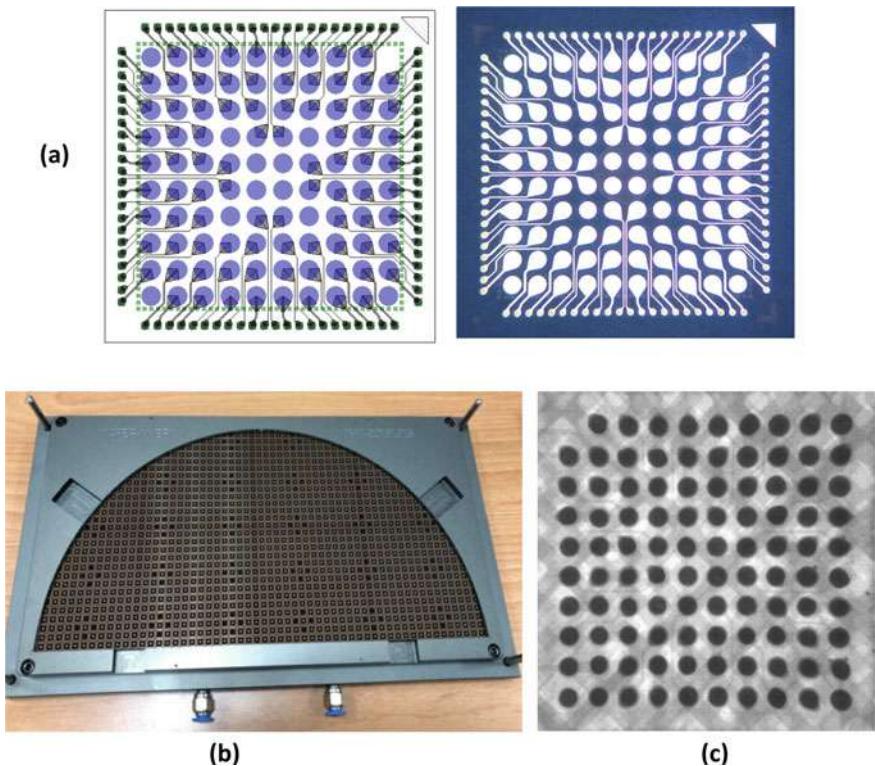


Fig. 3.58 a Key process steps of Unimicron's 6-side molded PLCSP. b Continue



**Fig. 3.59** **a** Fabricated PLCSP from a  $508 \times 508$  mm panel. **b** Solder ball mounting equipment. **c** X-ray image of PLCSP with solder balls

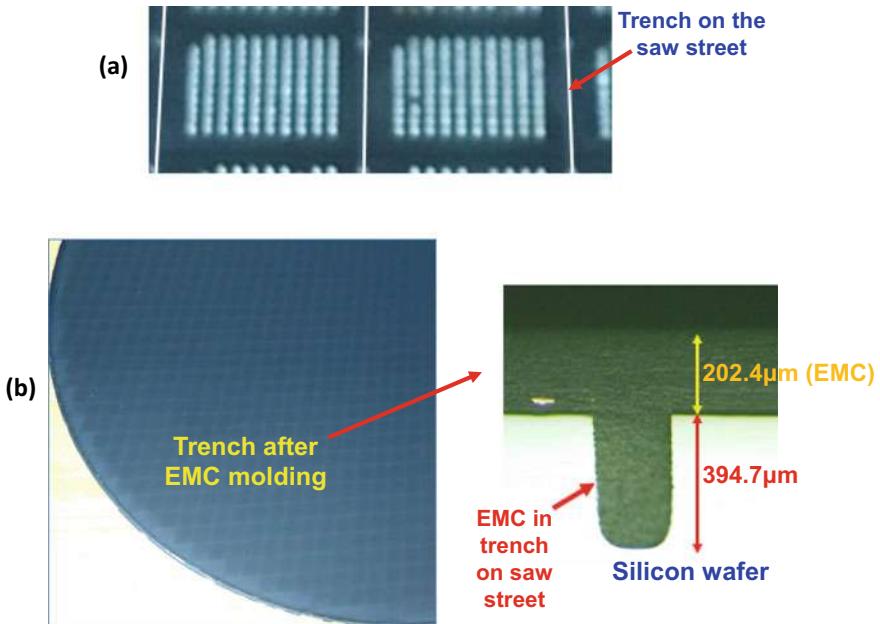
### 3.5.6 SMT Assembly of the 6-Side Molded PLCSP on PCB

A lead-free surface-mount technology (SMT) process is used to assemble the 6-side molded PLCSPs on the test PCB. Figure 3.64a shows the reflow temperature profile. Figure 3.64b shows the PCB assembly of the ordinary PLCSP and Fig. 3.59c shows the PCB assembly of the 6-side molded PLCSP.

### 3.5.7 Thermal Cycling Test of the 6-Side Molded PLCSP

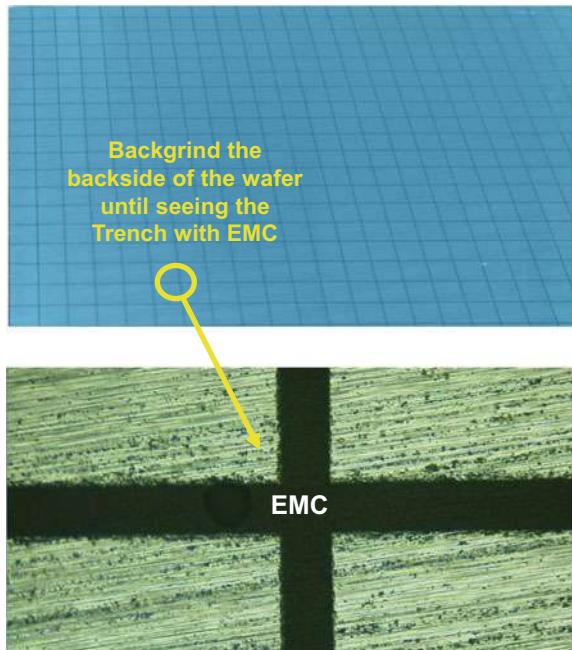
The PCB assembly of the 6-side molded PLCSP is put into a thermal cycling chamber as shown in Fig. 3.36 and 3.37 [123]. The temperature cycling profile is shown in Fig. 3.38. The sample size of the 6-side molded PLCSP is 24.

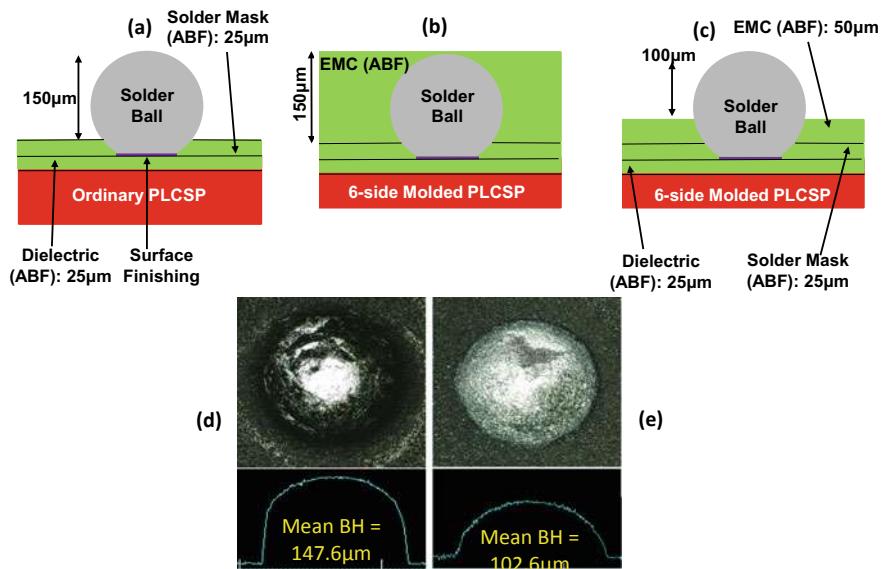
#### (A) Failure Criterion



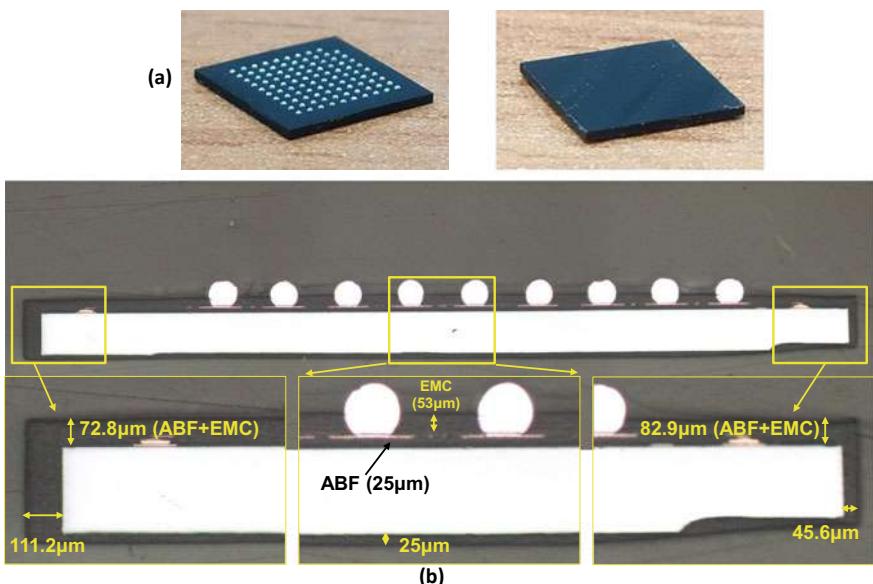
**Fig. 3.60** **a** Dicing the front-side of the wafer. **b** After EMC molding of the front-side of the wafer

**Fig. 3.61** Backgrind the backside of the wafer until seeing the EMC on the trench of the saw street

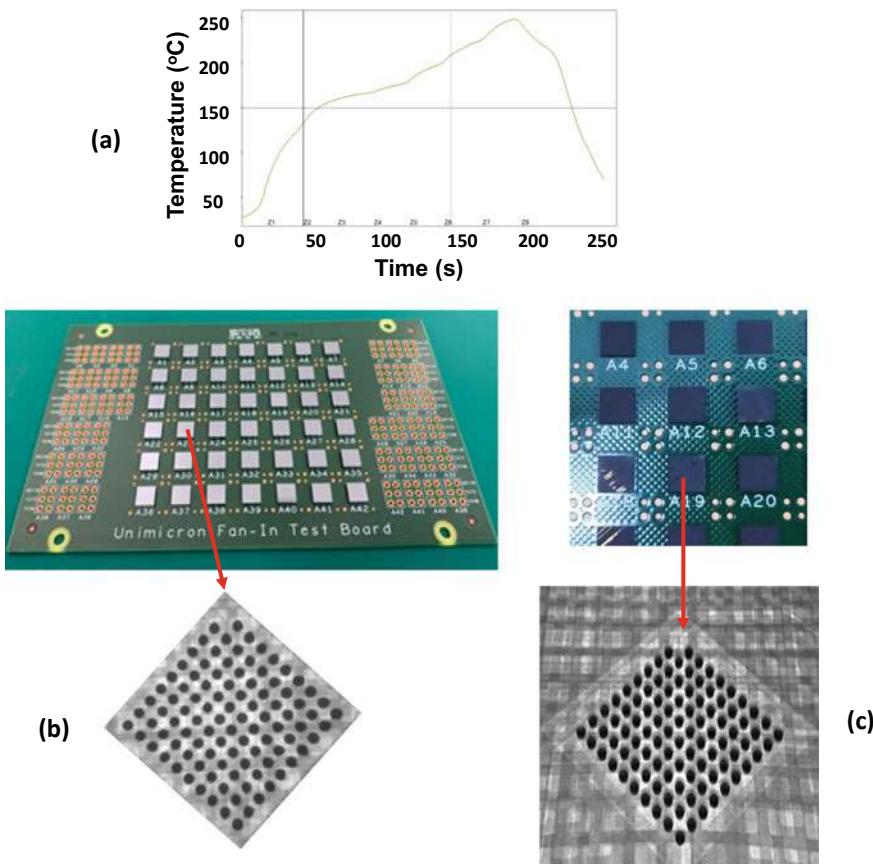




**Fig. 3.62** Solder ball height. **a** Ordinary PLCSP. **b** Right after front-side molding. **c** Right after plasma etching. **d** Ordinary PLCSP solder ball image. **e** 5-side or 6-side molded PLCSP solder ball image



**Fig. 3.63** **a** 3D-view. **b** Cross section view of the 6-side molded PLCSP



**Fig. 3.64** SMT assembly of the 6-side molded PLCSP. **a** Reflow profile. **b** Ordinary PLCSP PCB assembly. **c** 6-side molded PLCSP PCB assembly

In this study, the failure criterion is when the resistance of the daisy chain of the 6-side molded PLCSP PCB assembly increases by 50%. The cycle at which the first solder joint of a 6-side molded PLCSP failed is considered as the cycle-to-failure of the 6-side molded PLCSP.

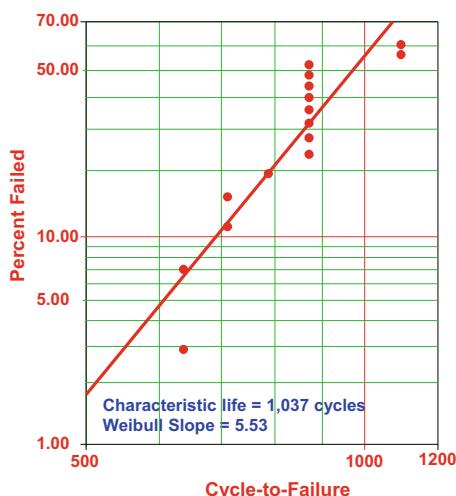
#### (B) Test Results of the 6-Side Molded PLCSP

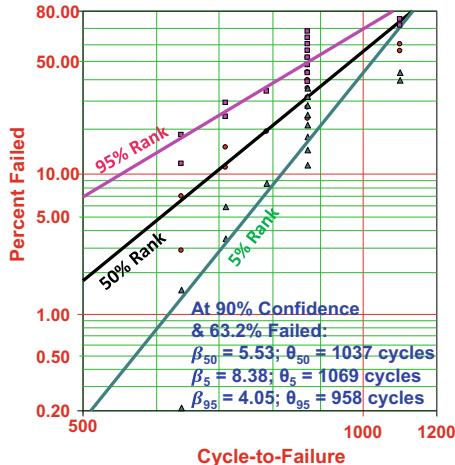
The thermal cycling test results of the 6-side molded PLCSP are tabulated in Table 3.5. It can be seen that there are 15 failures. The median (50%) rank, 5% rank, and 95% rank are also tabulated in Table 3.5. These data are plotted into a Weibull distribution at median rank and is shown in Fig. 3.65. It can be seen that the characteristic life ( $\theta$ ) (63.2% failed) = 1,037 cycles and the Weibull slope ( $\beta$ ) is = 5.53. Figure 3.66 shows the Weibull plot of the 6-side molded PLCSP at 90% confidence. It can be seen that the true characteristic life ( $\theta_t$ ) at 90% confidence is  $958 \leq \theta_t \leq 1,069$  cycles.

**Table 3.5** Thermal cycling test results of the 6-side molded PLCSP at median rank, 5% rank, and 95% rank

Failure order	Cycles-to-failure	$F(x)$	90% confidence		
			Median (50%) rank	5% rank	95% rank
1	638	2.88	0.21	11.73	
2	638	6.98	1.50	18.29	
3	712	11.08	3.50	23.98	
4	712	15.17	5.90	29.23	
5	788	19.27	8.59	34.18	
6	872	23.37	11.49	38.91	
7	872	27.46	14.57	43.47	
8	872	31.56	17.80	47.87	
9	872	35.66	21.26	52.14	
10	872	39.75	24.64	56.29	
11	872	43.85	28.24	60.32	
12	872	47.95	31.94	64.24	
13	872	52.04	35.76	68.06	
14	1096	56.14	39.68	71.76	
15	1096	60.24	43.71	75.36	

Sample size = 24

**Fig. 3.65** Weibull plot of the 6-side molded PLCSP solder joint at median rank



**Fig. 3.66** Weibull plot of the 6-side molded PLCSP solder joint at 90% confidence

By using Fig. 3.41 with  $C = 90\%$  and  $N = 15$ , then  $E = 0.29$ . Thus, the true Weibull slope is  $3.93 \leq \beta_t \leq 7.13$ .

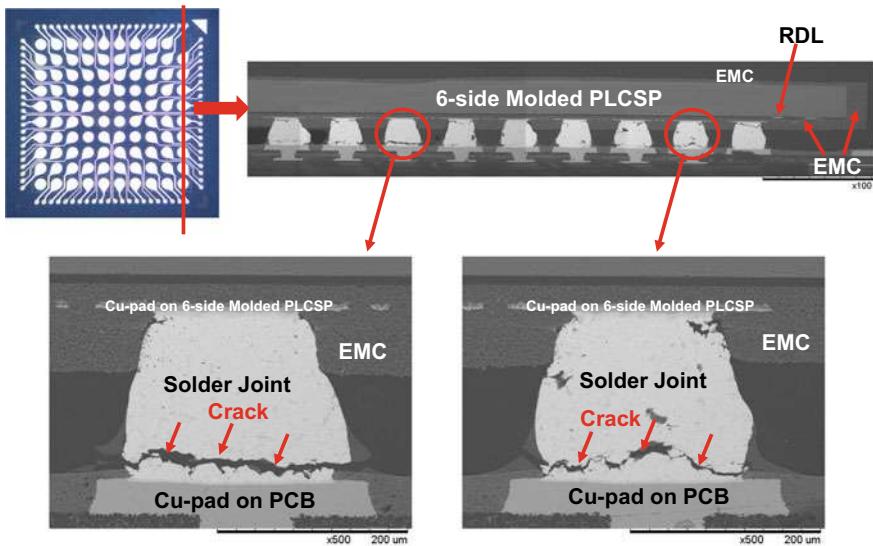
#### (C) Failure Location and Failure Mode of the 6-side Molded PLCSP PCB Assembly

The typical failure location occurs at the outer lows (near the corners) of the solder joints of the 6-side molded PLCSP as shown in Fig. 3.67. Most of the failure modes are the cracking of the solder near the interface between the PCB and the bulk solder as shown in Fig. 3.67. This failure mode of the 6-side molded PLCSP is very different from that of the ordinary PLCSP (Fig. 3.42). More on this characteristic will be elaborated in the thermal cycling simulation section.

#### (D) Comparison of the Mean-Life of Solder Joints between the 6-side Molded PLCSP and the Ordinary PLCSP

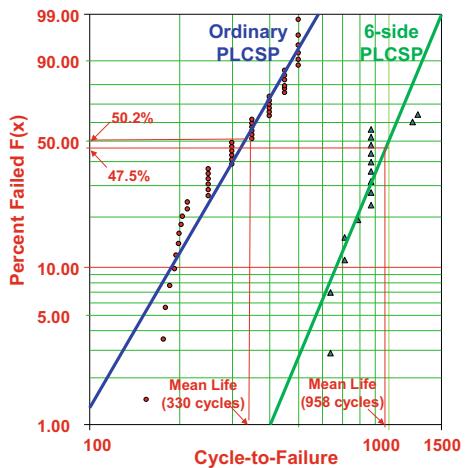
The Weibull plots of the solder joints of the 6-side molded PLCSP and the ordinary PLCSP at median rank are shown in Fig. 3.68. From these plots, it is obvious that the characteristic life of the 6-side molded (1,037 cycles) PLCSP is better than that (368 cycles) of the ordinary PLCSP. Also, the mean life of the 6-side molded PLCSP (958 cycles) is better than that (330 cycles) of the ordinary PLCSP. [Mean life =  $\theta\Gamma(1 + 1/\beta)$ ].

If one product is found to be superior to another from testing, how CONFIDENT ( $P$ ) can it be that the same is true of their populations? Herein, a simple approach is used to determine whether the mean life of one product is better than the other, without inquiring what the actual differences are [99].



**Fig. 3.67** Failure location and failure mode of the 6-side molded PLCSP solder joints

**Fig. 3.68** Comparison between the 6-side Molded PLCSP and the Ordinary PLCSP solder joints



$$P = \frac{1}{1 + \frac{\log 1/q}{\log 1/(1-q)}}$$

where

$$q = 1 - \frac{1}{\left[1 + \left(\frac{t+4.05}{6.12}\right)^5\right]^{40/7}}$$

$$t = \frac{\sqrt{1 + \sqrt{T}}(\rho - 1)}{\rho \Omega_2 + \Omega_1}$$

$$\rho = \frac{M_2}{M_1}$$

$$T = (r_1 - 1)(r_2 - 1)$$

$$\begin{aligned}\Omega_1 &= \sqrt{\frac{\Gamma(1 + 2/\beta_1)}{\Gamma^2(1 + 1/\beta_1)} - 1} \\ \Omega_2 &= \sqrt{\frac{\Gamma(1 + 2/\beta_2)}{\Gamma^2(1 + 1/\beta_2)} - 1}\end{aligned}$$

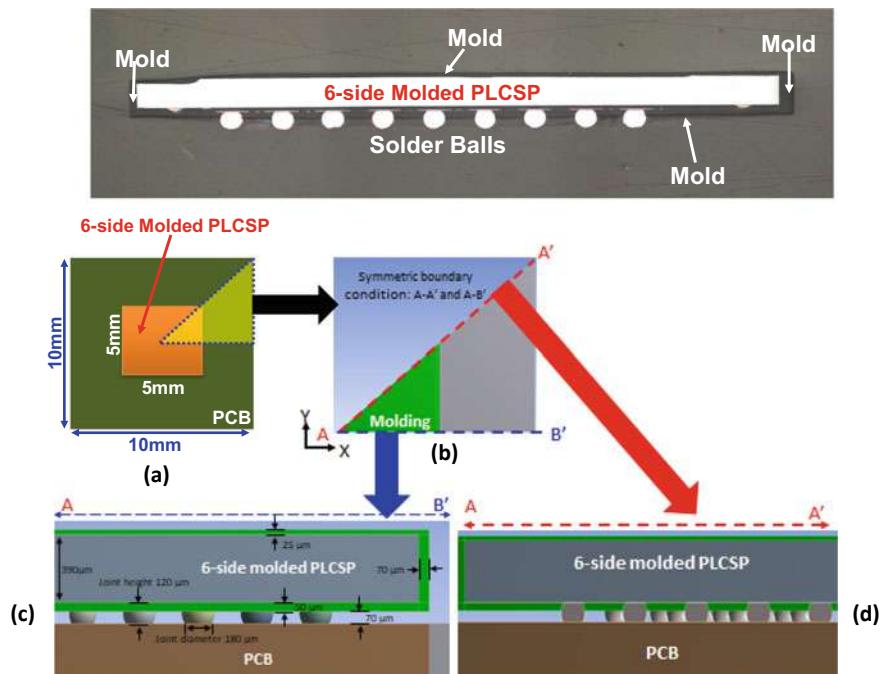
and  $M_1$  is the mean life of Simple 1 (S1),  $M_2$  is the mean life of Simple 2 (S2),  $r_1$  is the number of failures in S1,  $r_2$  is the number of failures in S2,  $\beta_1$  is the Weibull slope of S1, and  $\beta_2$  is the Weibull slope of S2. In our case,  $M_1 = 958$ ,  $M_2 = 330$ ,  $S1 = 24$ ,  $S2 = 48$ ,  $r_1 = 15$ ,  $r_2 = 48$ ,  $\beta_1 = 5.53$ , and  $\beta_2 = 3.34$ . A simple calculation yields  $M_1/M_2 = 2.9$  and  $P = 0.999$ , i.e., in 999 out of one thousand cases the mean life of the 6-side molded PLCSP solder joint is superior (by 2.9 times) to the ordinary PLCSP.

### 3.5.8 Thermal Cycling Simulation of the 6-Side Molded PLCSP PCB Assembly

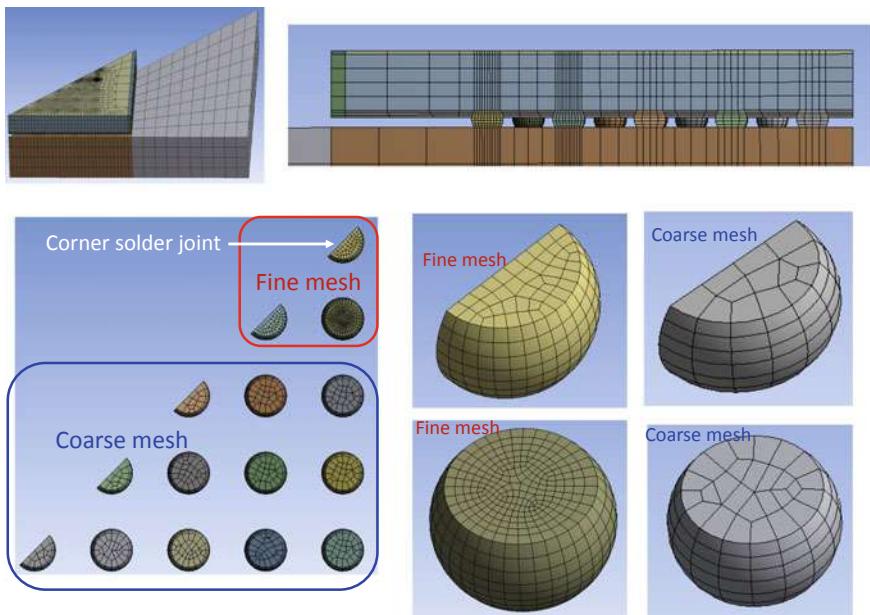
#### (A) Structure and Kinematic Boundary

The PCB assembly of the 6-side molded PLCSP is schematically shown in Fig. 3.69. Because of the symmetry about the  $x$ -axis, the  $y$ -axis, and the diagonal axes, only one-eighth of the structure is modeled. From the concept of distance to neutral point (DNP) [99], the corner solder joint does not carry any power/ground/signal but functions as a dummy (mechanical) solder joint used for absorbing the maximum stress and strain.

Despite the overall economy of elements in the one-eighth model, selective mesh refinement is used to concentrate highly refined elements in the solder joints where failure is anticipated. In the present PCB assembly, failure would be predicted in the solder joints with the greatest DNP and near the chip corners as shown in Fig. 3.70. Thus, highly refined meshes are applied to these solder joints. The other joints are coarsely meshed. The 3-D Solid186 element of ANSYS 2020 is used.



**Fig. 3.69** Geometry of the 6-side molded PLCSP and boundary-value problem



**Fig. 3.70** Finite element model for simulations

### (B) Material Properties

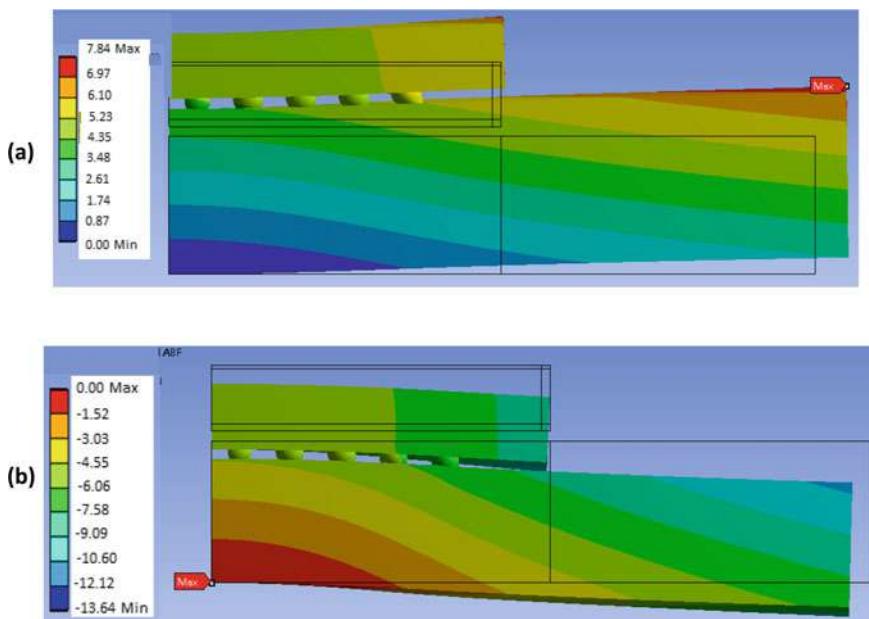
The material properties of the 6-side molded PLCSP PCB assembly are given in Tables 3.1 and 3.4. All the material properties are assumed to be constant except for those of the solder. The Sn3Ag0.5Cu is assumed to obey the generalized Garofalo creep equation [99]. The coefficient of thermal expansion (CTE) and Young's modulus of the solder are  $21 + 0.017T$  and  $49 - 0.07T$ , respectively, and  $T$  is the temperature in Celsius.

### (C) Kinetic Boundary Condition

The temperature profile shown in Fig. 3.44 is to be imposed on the 6-side molded PLCSP PCB assembly. Five temperature cycles are executed. It can be seen that the temperature condition is from  $-40$  to  $85$  °C. The cycle time is 60 min; the ramp-up and ramp-down are 15 min, and the dwell-at-hot and dwell-at-cold are each 15 min.

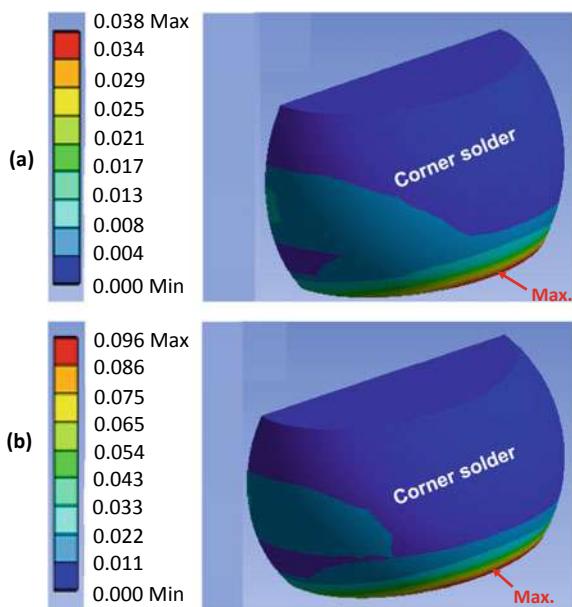
### (D) Thermal Cycling Simulation Results

The deformed shape (color contours) and the undeformed shape (dark lines) of the 6-side molded PLCSP PCB assembly are shown in Fig. 3.71a at 450 s ( $85$  °C) and in Fig. 3.71b at 2,250 s ( $-40$  °C). It can be seen that: (a) at  $85$  °C, the PCB expanges more



**Fig. 3.71** Deformed and undeformed shapes of the 6-side molded PLCSP. **a** At 450 s ( $85$  °C). **b** At 2,250 s ( $-40$  °C)

**Fig. 3.72** Accumulated creep strain at the corner solder joint of the 6-side molded PLCSP PCB assembly. **a** At 85 °C (450 s). **b** At –45 °C (2,250 s)



than the 6-side molded silicon chip and curves outward; the solder joint (especially the corner one with the largest DNP) is subjected to mainly shear deformation and the structure is deformed to a concave shape (smiling face), and (b) at –40 °C, the PCB shrinks more than the molded silicon chip and curves inward; the structure is deformed to a convex shape (crying face).

The largest accumulated creep strain occurs (the failure location) at the corner solder joint (Fig. 3.72) of the 6-side molded PLCSP assembly. Figure 3.72a shows the distribution of accumulated creep strain contours at 450 s (85 °C) and Fig. 3.72b at 2,250 s (–40 °C) in the corner solder joint. It can be seen that the maximum accumulated creep strain occurs near the interface between the PCB and the bulk solder of the corner solder joint and it is the initial driving force for cracking (the failure mode) of the solder joint. Thus, any failure should occur (initiate) at this location. However, the maximum accumulated creep strain only occurs in a very small (red) volume of the whole corner solder joint. Actually, the accumulated creep strains in most of the (blue) volume of the corner solder joint (especially near the interface between the chip and the bulk solder) are very small. This is because the upper portion (about 50  $\mu\text{m}$ ) of the corner solder joint is embedded in the EMC.

An ordinary PLCSP PCB assembly subjected to the same boundary conditions has also been analyzed (Sect. 3.3.7). The largest accumulated creep strain also occurs at the corner solder joint (the same failure location as in the 6-side molded case). However, the distribution of the accumulated creep strain (failure mode) in the corner solder (Fig. 3.46) is very different from that of the 6-side molded PLCSP (Fig. 3.72).

First of all, the site of the maximum accumulated creep strain in the corner solder joint has been switched from the interface between the chip and the bulk solder for

the ordinary PLCSP (Fig. 3.46) to the interface between the PCB and the bulk solder for the 6-side molded PLCSP (Fig. 3.72). This is because there are more local thermal expansion mismatch between the silicon chip and the bulk solder for the ordinary PLCSP. (The local thermal expansion mismatch between the 6-side molded silicon chip and the bulk solder is smaller.) Also, the upper portion (about 50  $\mu\text{m}$ ) of the 6-side molded solder joint is embedded in the EMC.

Second, the corner solder joint failure mode is different between the ordinary PLCSP and the 6-side molded PLCSP. For the ordinary PLCSP, the crack should initiate at the interface between the chip and the bulk solders (Figs. 3.42 and 3.46). On the other hand, for the 6-side molded PLCSP, the crack should initiate at the interface between the PCB and the bulk solders (Fig. 3.67 and 3.72).

A simple thermal fatigue life prediction model of lead-free solder joint is given by [142, 143]:

$$N_f = \sum_j \alpha_j \left[ \frac{\sum_i \Delta W_i \times V_i}{\sum_i V_i} \right]^{\beta_j}$$

where  $N_f$  is the thermal fatigue life, and  $\alpha_j$  and  $\beta_j$  are constants to be determined by experiments (usually isothermal fatigues) for a specific component/package and solder joint.  $\Delta W_i$  is the creep (or inelastic) strain energy density (or accumulated equivalent creep strain) per cycle in the  $i$ th element determined from finite element simulations.  $V_i$  is the volume of that  $i$ th element.

In the present simulations, the corner solder joint consists of 320 elements. Some of the elements of the 6-side molded PLCSP corner solder joint have similar maximum values (0.038 at 85 °C and 0.96 at -45 °C) of the accumulated creep strain ( $\Delta W_i$ ) as the ordinary PLCSP corner solder joint (0.036 at 85 °C and 0.99 at -45 °C), but the number of elements are very small, i.e., only a very small volume of the corner solder joint. On the other hand, most of elements (volume) of the 6-side molded PLCSP corner solder joint have lower values of  $\Delta W_i$  than the ordinary PLCSP solder joint. Thus, it is reasonable to estimate that the thermal fatigue life of the 6-side molded PLCSP corner solder joint lasts longer than that of the ordinary PLCSP corner solder joint. Unfortunately, since the  $\alpha_j$  and  $\beta_j$  are not available, thus, the thermal fatigue life of these two solder joints cannot be predicted.

### 3.5.9 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- The feasibility of the design, materials, process, fabrication, and reliability of a 6-side molded PLCSP has been demonstrated.
- The RDL of the PLCSP has been fabricated on a 508 mm × 508 mm panel with diced and un-diced 2.25 times of 300 mm device wafers. It is a very high throughput process.

- The RDL of the PLCSP has been fabricated with an all PCB process and equipment on the large panel with diced and un-diced device wafers. It is a very low cost process.
- After RDL fabrication, the wafers have been debonded from the panel. Then, solder ball mounting, half-cutting the wafer from the front-side to make the trenches on the saw streets, wafer front-side EMC laminating, backgrinding the backside of the wafer until the EMC on the trenches was seen, backside laminating of EMC plasma etching some of the EMC to expose portion of the solder ball, then dicing the wafer into individual 6-side molded PLCSPs.
- Based on the JEDEC Standard JESD22-B111, a drop test of the ordinary PLCSP on PCB assembly has been performed. All the samples passed 30 drops, thus the PLCSP passed the drop test.
- The failure location of the 6-side molded PLCSP is along the outer row (near the corner) of solder joints. The failure mode is the cracking of solder near the interface between the PCB and the bulk solders.
- By comparing the mean life between the 6-side molded PLCSP solder joint (958 cycles) with the ordinary PLCSP solder joints (330), it has been determined that in 999 out of one thousand cases, the mean life of the 6-side molded PLCSP is 2.9 times of the ordinary PLCSP.
- A non-linear time and temperature dependent 3D finite element simulation of the 6-side molded PLCSP PCB assembly showed that the maximum accumulated creep strain occurs near the interface between the PCB and the bulk solders. Thus, any failure should occur (initiate) at this location. This confirms with the failure mode from the thermal cycling test results.
- The reason for the switch of the failure mode from the interface between the PCB and the bulk solders (for the 6-side molded PLCSP) to the interface between the chip and the bulk solders (ordinary) is because there is protection of the upper solder joint from the EMC molding.
- The maximum values of the accumulated creep strain ( $\Delta W_i$ ) in the corner solder joint for the 6-side molded PLCSP and the ordinary PLCSP are about the same. However, this maximum values only occurred at a very small volume of the 6-side molded PLCSP solder joint. The accumulated creep strain in most of the volumes of the 6-side molded solder joint is smaller than those in the ordinary PLCSP solder joins. Thus, the thermal-fatigue life of the 6-side molded PLCSP should be longer than that of the ordinary PLCSP.

## References

1. Elenius, P., and H. Hollack, "Method for forming chip scale package," *US patent 6,287,893*, filed on July 13, 1998; patented on September 11, 2001.
2. Yasunaga, M., "Chip-scale package: a lightly dressed LSI chip," *Proc. of IEEE/CPMT IEMTS*, 1994, pp. 169–176.

3. Marcoux, P., "A minimal packaging solution for known good die and direct chip attachment," *Proc. Of SMTA*, 1994, pp. 19–26.
4. Chanchani, R., "A new mini ball grid array (m-BGA) multichip module technology," *Proc. Of NEPCON West*, 1995, pp. 938–945.
5. Badihi, A., "Shellcase—a true miniature integrated circuit package," *Proc. of International FC, BGA, Adv. Packaging Symp.*, 1995, pp. 244–252.
6. Baba, S., et al., "Molded chip-scale package for high pin count," *Proc. of IEEE/ECTC*, 1996, 1251–1257.
7. Topper, M., "Redistribution technology for chip scale package using photosensitive BCB," *Future Fab International*, 1996, pp. 363–368.
8. Elenius, P., "FC2SP-(Flip Chip-Chip Size Package)," *Proc. of NEPCON West*, 1997, pp. 1524–1527.
9. Auersperg, J., "Reliability evaluation of chip-scale packages by FEA and microDAC," *Proc. of Symp. On Design and Reliability of Solder and Solder Interconnections*, TMS Annual Meeting, 1997, pp. 439–445.
10. DiStefano, T., "Wafer-level fabrication of IC packages," *Chip Scale Review*, 1997, pp. 20–27.
11. Kohl, J. E., "Low-cost chip scale packaging and interconnect technology," *Proc. of the CSP Symp.*, 1997, pp. 37–43.
12. Elenius, P., "Flip-chip bumping for IC packaging contractors," *Proc. of NEPCON West*, 1998, pp. 1403–1407.
13. Lau, J. H., and S. W. R. Lee, *Chip Scale Package*, McGraw-Hill Book Company, New York, 1999.
14. Lau, J. H., T. Chung, R. Lee, C. Chang, and C. Chen, "A Novel and Reliable Wafer-Level Chip Scale Package (WLCSP)", *Proceedings of the Chip Scale International Conference*, SEMI, September 1999, pp. H1–8.
15. Lau, J. H., S. W. R. Lee, and C. Chang, "Solder Joint Reliability of Wafer Level Chip Scale Packages (WLCSP): A Time-Temperature-Dependent Creep Analysis", *ASME Transactions, Journal of Electronic Packaging*, Vol. 122, No. 4, May 2000, pp. 311–316.
16. Lau, J. H., "Critical Issues of Wafer Level Chip Scale Package (WLCSP) with Emphasis on Cost Analysis and Solder Joint Reliability", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 25, No. 1, 2002, pp. 42–50.
17. Lau, J. H., and R. Lee, "Effects of Build-Up Printed Circuit Board Thickness on the Solder Joint Reliability of a Wafer Level Chip Scale Package (WLCSP)," *IEEE Transactions on Components & Packaging Technologies*, Vol. 25, No. 1, March 2002, pp. 3–14.
18. Lau, J. H., S. Pan, and C. Chang, "A New Thermal-Fatigue Life Prediction Model for Wafer Level Chip Scale Package (WLCSP) Solder Joints", *ASME Transactions, Journal of Electronic Packaging*, Vol. 124, September 2002, pp. 212–220.
19. Lau, J. H., and R. Lee, "Modeling and Analysis of 96.5Sn-3.5Ag Lead-Free Solder Joints of Wafer Level Chip Scale Package (WLCSP) on Build-Up Microvia Printed Circuit Board," *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 25, No. 1, 2002, pp. 51–58.
20. Lau, J. H., R. Lee, S. Pan, and C. Chang, "Nonlinear Time-Dependent Analysis of Micro Via-in-Pad Substrates for Solder Bumped Flip Chip Applications," *ASME Transactions, Journal of Electronic Packaging*, Vol. 124, September 2002, pp. 205–211.
21. Lau, J. H., C. Chang, and R. Lee, "Solder Joint Crack Propagation Analysis of Wafer-Level Chip Scale Package on Printed Circuit Board Assemblies," *IEEE Transactions on Components & Packaging Technologies*, Vol. 24, No. 2, 2001, pp. 285–292.
22. Lau, J. H., and R. Lee, "Computational Analysis on the Effects of Double-Layer Build-Up Printed Circuit Board on the Wafer Level Chip Scale Package (WLCSP) Assembly with Pb-Free Solder Joints." *International Journal of Microcircuits & Electronic Packaging, IMAPS Transactions*, Vol. 24, No. 2, 2001, pp. 89–104.
23. Lau, J. H., and R. Lee, "Effects of Microvia Build-Up Layers on the Solder Joint Reliability of a Wafer Level Chip Scale Package (WLCSP)," *IEEE Proceedings of Electronic Components & Technology Conference*, May 29–June 1, Orlando, Florida, U.S.A., 2001, pp. 1207–1215.

24. Lau, J. H., and R. Lee, "Reliability of 96.5Sn-3.5Ag Lead-Free Solder-Bumped Wafer Level Chip Scale Package (WLCSP) on Build-Up Microvia Printed Circuit Board," *Proceedings of the 2nd International Conference on High Density Interconnect and System Packaging*, April 17–20, Santa Clara, California, U.S.A., 2001, pp. 314–322.
25. Lau, J. H., and R. Lee, "Effects of Build-Up Printed Circuit Board Thickness on the Solder Joint Reliability of a Wafer Level Chip Scale Package (WLCSP)," *Proceeding of the International Symposium on Electronic Materials & Packaging*, November 30–December 2, Kowloon, Hong Kong, 2000, pp. 115–126.
26. Lau, J. H., S. Pan, and C. Chang, "Nonlinear Fracture Mechanics Analysis of Wafer-Level Chip Scale Package Solder Joints with Creaks", *Proceedings of IMAPS Microelectronics Conference*, Boston, MA, September 2000, pp. 857–865.
27. Lau, J. H., and R. Lee, "Reliability of Wafer Level Chip Scale Package (WLCSP) with 96.5Sn-3.5Ag Lead-Free Solder Joints on Build-Up Microvia Printed Circuit Board," *Proceeding of the International Symposium on Electronic Materials & Packaging*, November 30–December 2, Kowloon, Hong Kong, 2000, pp. 55–63.
28. Lau, J. H., S. Pan, and C. Chang, "A New Thermal-Fatigue Life Prediction Model for Wafer Level Chip Scale Package (WLCSP) Solder Joints", *Proceeding of the 12th Symposium on Mechanics of SMT & Photonic Structures*, ASME International Mechanical Engineering Congress & Exposition, November 5–10, Orlando, Florida, USA, 2000, pp. 91–101.
29. Lau, J. H., S. Pan, and C. Chang, "Creep Analysis of Wafer Level Chip Scale Packages (WLCSP) with 96.5Sn-3.5Ag and 100In Lead-Free Solder Joints and Microvia Build-Up Printed Circuit Board", *Proceeding of the 12th Symposium on Mechanics of SMT & Photonic Structures*, ASME International Mechanical Engineering Congress & Exposition, November 5–10, Orlando, Florida, USA, 2000, pp. 79–89.
30. Lau, J. H., C. Chang, and R. Lee, "Solder Joint Crack Propagation Analysis of Wafer-Level Chip Scale Package on Printed Circuit Board Assemblies," *IEEE Proceeding of the 50th Electronic Components & Technology Conference*, Las Vegas, NA, 2000, pp. 1360–1368.
31. Lau, J. H. and R. Lee, "Fracture Mechanics Analysis of Low Cost Solder Bumped Flip Chip Assemblies with Imperfect Underfills," *Proceedings of NEPCON West*, Anaheim, CA, 2000, pp. 653–660.
32. Lau, J. H., T. Chung, T., R. Lee, and C. Chang, "A Low Cost and Reliable Wafer Level Chip Scale Package," *Proceedings of NEPCON West*, Anaheim, CA, 2000, pp. 920–927.
33. Lau, J. H., Lee, S.W.R., Ouyang, C., Chang, C. and Chen, C.C., "Solder Joint Reliability of Wafer Level Chip Scale Packages (WLCSP): A Time-Temperature-Dependent Creep Analysis," ASME Winter Annual Meeting, *ASME Paper No. 99-IMECE/EEP-5*, Nashville, TN, 1999.
34. Lau, J. H., C. Ouyang, and R. Lee, "A Novel and Reliable Wafer-Level Chip Scale Package (WLCSP)", *Proceedings of Chip Scale International Conference*, San Jose, CA, September 1999, pp. H1–H9.
35. Chen, C., K. H. Chen, Y. S. Wu, P. H. Tsao and S. T. Leu, "WLCSP Solder Ball Interconnection Enhancement for High Temperature Stress Reliability", *IEEE/ECTC Proceedings*, May 2020, pp. 1212–1217.
36. Zhang, H., Z. Wu, J. Malinowski, M. Carino, K. Young-Fisher, J. Trewhella, and P. Justison, "45RFSOI WLCSP Board Level Package Risk Assessment and Solder Joint Reliability Performance Improvement", *IEEE/ECTC Proceedings*, May 2020, pp. 2151–2156.
37. Ma, S., Y. Liu, F. Zheng, F. Li, D. Yu, A. Xiao, and X. Yang, "Development and Reliability study of 3D WLCSP for automotive CMOS image sensor using TSV technology", *IEEE/ECTC Proceedings*, May 2020, pp. 461–466.
38. Machani, K., F. Kuechenmeister, D. Breuer, C. Klewer, J. Cho, and K. Fisher, "Chip Package Interaction (CPI) risk assessment of 22FDX® Wafer Level Chip Scale Package (WLCSP) using 2D Finite Element Analysis modeling", *IEEE/ECTC Proceedings*, May 2020, pp. 1100–1105.
39. Chiu, J., K.C. Chang, S. Hsu, P. Tsao and M. J. Lii, "WLCSP Package and PCB Design for Board Level Reliability", *IEEE/ECTC Proceedings*, May 2019, pp. 763–767.

40. Yu, D., Y. Zou, X. Xu, A. Shi, X. Yang, and Z. Xiao, "Development of 3D WLCSP with Black Shielding for Optical Finger Print Sensor for the Application of Full Screen Smart Phone", *IEEE/ECTC Proceedings*, May 2019, pp. 884–889.
41. Zhou, Y. , L. Chen, Y. Liu, and S. Sitaraman, "Thermal Cycling Simulation and Sensitivity Analysis of Wafer Level Chip Scale Package with Integration of Metal-Insulator-Metal Capacitors", *IEEE/ECTC Proceedings*, May 2019, pp. 1521–1528.
42. Chou, P. H. Hsiao, and K. Chiang, "Failure Life Prediction of Wafer Level Packaging using DoS with AI Technology", *IEEE/ECTC Proceedings*, May 2019, pp. 1515–1520.
43. Chen, Z., B. Lau, Z. Ding, E. Leong, C. Wai, B. Han, L. Bu, H. Chang, and T. Chai, "Development of WLCSP for Accelerometer Packaging with Vertical CuPd Wire as Through Mold Interconnection (TMI)", *IEEE/ECTC Proceedings*, May 2018, pp. 1188–1193.
44. Tsao, P. H., T. H. Lu, T. M. Chen, K. C. Chang, C. M. Kuo, M. J. Lii and L. H. Chu, "Board Level Reliability Enhancement of WLCSP with Large Chip Size", *IEEE/ECTC Proceedings*, May 2018, pp. 120–1205.
45. Ramachandran, V., K. C. Wu, C. C. Lee, and K. N. Chiang, "Reliability Life Assessment of WLCSP Using Different Creep Models", *IEEE/ECTC Proceedings*, May 2018, pp. 1017–1022.
46. Sheikh, M., A. Hsiao, W. Xie, S. Perng, E. Ibe, K. Loh, and T. Lee, "Multi-axis loading impact on thermo-mechanical stress-induced damage on WLCSP and components with via-in pad plated over (VIPPO) board design configuration", *IEEE/ECTC Proceedings*, May 2018, pp. 911–915.
47. Tsao, P. H., T. M. Chen, Y. L. Kuo, C. M. Kuo, S. Hsu, M. J. Lii, and L. H. Chu, "Investigation of Production Quality and Reliability Risk of ELK Wafer WLCSP Package", *IEEE/ECTC Proceedings*, May 2017, pp. 371–375.
48. Lin, W., Q. Pham, B. Baloglu, and M. Johnson, "SACQ Solder Board Level Reliability Evaluation and Life Prediction Model for Wafer Level Packages", *IEEE/ECTC Proceedings*, May 2017, pp. 1058–1064.
49. Yang, S., C. Chen, W. Huang, T. Yang, G. Huang, T. Chou, C. Hsu, C. Chang, H. Huang, C. Chou, C. Ku, C. Chen, C. Chen, K. Liu, A. Kalnitsky, and M. Liao, "Implementation of Thick Copper Inductor Integrated into Chip Scaled Package", *IEEE/ECTC Proceedings*, May 2017, pp. 306–311.
50. Lee, T., Y. Chang, C. Hsu, S. Hsieh, P. Lee, Y. Hsieh, L. Wang, and L. Zhang, "Glass Based 3D-IPD Integrated RF ASIC in WLCSP", *IEEE/ECTC Proceedings*, May 2017, pp. 631–636.
51. Hsu, M., K. Chiang, C. Lee, "A Modified Acceleration Factor Empirical Equation for BGA Type Package", *IEEE/ECTC Proceedings*, May 2017, pp. 1020–1026.
52. Jalink, J., R. Roucou, J. Zaa, J. Lesventes, R. Rongen, "Effect of PCB and Package Type on Board Level Vibration using Vibrational Spectrum Analysis", *IEEE/ECTC Proceedings*, May 2017, pp. 470–475.
53. Xu, J., Z. Ding, V. Chidambaram, H. Ji, and Y. Gu, "High Vacuum and High Robustness Al-Ge Bonding for Wafer Level Chip Scale Packaging of MEMS Sensors", *IEEE/ECTC Proceedings*, May 2017, pp. 956–960.
54. Max K., C. Wu, C. Liu, and D. Yu, "UFI (UBM-Free Integration) Fan-In WLCSP Technology Enables Large Die Fine Pitch Packages", *IEEE/ECTC Proceedings*, May 2017, pp. 1154–1159.
55. Takyu, S., Y. Fumita, D. Yamamoto, S. Yamashita, K. Furuta, Y. Yamashita, K. Tanaka, N. Uchiyama, T. Ogiwara, and Y. Kondo, "A Novel Dicing Technologies for WLCSP Using Stealth Dicing through Dicing Tape and Back Side Protection-Film", *IEEE/ECTC Proceedings*, May 2016, pp. 1241–1246.
56. Lin, Y., E. Chong, M. Chan, K. Lim, and S. Yoon, "WLCSP + and eWLCSP in Flex-Line: Innovative Wafer Level Package Manufacturing", *IEEE/ECTC Proceedings*, May 2015, pp. 865–870.
57. Chen, J. H., Y. L. Kuo, P. H. Tsao, J. Tseng, M. Chen, T. M. Chen, Y. T. Lin, and A. Xu, "Investigation of WLCSP Corrosion Induced Reliability Failure on Halogens Environment for Wearable Electronics", *IEEE/ECTC*, May 2015, pp. 1599–1603.

58. Chatinho, V., A. Cardoso, J. Campos, and J. Geraldes, "Development of Very Large Fan-In WLP/ WLCSP for Volume Production", *IEEE/ECTC*, May 2015, pp. 1096–1101.
59. Nomura, H., K. Tachibana, S. Yoshikawa, D. Daily, and A. Kawa, "WLCSP CTE Failure Mitigation via Solder Sphere Alloy", *IEEE/ECTC*, May 2015, pp. 1257–1261.
60. Yang, S., C. Wu, Y. Hsiao, C. Tung, D. Yu, "A Flexible Interconnect Technology Demonstrated on a Wafer-Level Chip Scale Package", *IEEE/ECTC*, May 2015, pp. 859–864.
61. Yang, S., B. Tsai, C. Lin, E. Yen, J. Lee, W. Hsieh, and V. Wu, "Advanced Multi-sites Testing Methodology after Wafer Singulation for WLPs Process", *IEEE/ECTC*, May 2015, pp. 871–876.
62. Keser, B., R. Alvarado, M. Schwarz, and S. Bezuk, "0.35 mm Pitch Wafer Level Package Board Level Reliability: Studying Effect of Ball De-population with Varying Ball Size", *IEEE/ECTC*, May 2015, pp. 1090–1095.
63. Arumugam, N., G. Hill, G. Clark, C. Arft, C. Grosjean, R. Palwai, J. Pedicord, P. Hagelin, A. Partridge, V. Menon, and P. Gupta, "2-die Wafer-level Chip Scale Packaging enables the smallest TCXO for Mobile and Wearable Applications", *IEEE/ECTC*, May 2015, pp. 1338–1342.
64. Liu, Y., Y. Liu, and S. Qu, "Bump Geometric Deviation on the Reliability of BOR WLCSP", *IEEE/ECTC Proceedings*, May 2014, pp. 808–814.
65. Anzai, N., M. Fujita, and A. Fujii, "Drop Test and TCT Reliability of Buffer Coating Material for WLCSP", *IEEE/ECTC Proceedings*, May 2014, pp. 829–835.
66. Cui, T., A. Syed, B. Keser, R. Alvarado, S. Xu, and M. Schwarz, "Interconnect Reliability Prediction for Wafer Level Packages (WLP) for Temperature Cycle and Drop Load Conditions", *IEEE/ECTC Proceedings*, May 2014, pp. 100–107.
67. Keser, B., R. Alvarado, A. Choi, M. Schwarz, and S. Bezuk, "Board Level Reliability and Surface Mount Assembly of 0.35 mm and 0.3 mm Pitch Wafer Level Packages", *IEEE/ECTC Proceedings*, May 2014, pp. 925–930.
68. Xiao, Z., J. Fan, Y. Ren, Y. Li, X. Huang, D. Yu, W. Zhang, "Development of 3D Thin WLCSP Using Vertical Via Last TSV Technology with Various Temporary Bonding Materials and Low Temperature PECVD Process", *IEEE/ECTC Proceedings*, May 2017, pp. 302–309.
69. Zoschke, K., M. Klein, R. Gruenwald, C. Schoenbein, And K. Lang, "LiTaO<sub>3</sub> Capping Technology for Wafer Level Chip Size Packaging of SAW Filters", *IEEE/ECTC Proceedings*, May 2017, pp. 889–896.
70. Kuo, F., J. Chiang, K. Chang, J. Shu, F. Chien, K. Wang and R. Lee, "Studying The Effect Of Stackup Structure Of Large Die Size Fan-in Wafer Level Package At 0.35 mm Pitch With Varying Ball Alloy To Enhance Board Level Reliability Performance", *IEEE/ECTC Proceedings*, May 2017, pp. 140–146.
71. Tsou, C., T. Chang, K. Wu, P. Wu and K. Chiang, "Reliability Assessment using Modified energy based model for WLCSP Solder Joints", *IEEE/ICEP2017*, Yamagata, Japan, April 2017.
72. Rogers, B., and C. Scanlan, "Improving WLCSP Reliability Through Solder Joint Geometry Optimization" *International Symposium on Microelectronics*, October 2013, pp. 546–550,
73. Hsieh, M. C., "Modeling correlation for solder joint fatigue life estimation in wafer-level chip scale packages", *International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, Oct. 2015, pp. 65–68.
74. Hsieh, M. C., and S. L. Tzeng, "Solder joint fatigue life prediction in large size and low cost wafer-level chip scale packages," *IEEE Electronic Packaging Technology (ICEPT)*, November 2015, pp. 496–501.
75. Liu, Y. M., and Y. Liu, "Prediction of board-level performance of WLCSP," *IEEE/ECTC Proceedings*, June 2013, pp. 840–845.
76. Liu, Y., Q. Qian, M. Ring, J. Kim, and D. Kinzer, "Modeling for Critical Design of Wafer Level Chip Scale Package," *IEEE/ECTC Proceedings*, June 2012, pp. 959–964.
77. Chan, Y., S. Lee, F. Song, J. Lo, and T. Jiang, "Effect of UBM and BCB layers on the thermomechanical reliability of wafer level chip scale package (WLCSP)," *Proc. Microsystems, Packaging, Assembly and Circuits Technology Conf. (IMPACT)*, 2009, pp. 407–412.

78. Tee, T., L. Tan, R. Anderson, H. Ng, J. Low, C. Khoo, R. Moody, and B. Rogers “Advanced Analysis of WLCSP Copper Interconnect Reliability under Board Level Drop Test,” *IEEE/ECTC Proceedings*, May 2008, pp. 1086–1095.
79. Fan, X., and Q. Han, “Design and Reliability in Wafer Level Packaging,” *IEEE/ECTC Proceedings*, May 2008, pp. 834–841.
80. Jung, B. Y., et al., “MEMS WLCSP development using vertical interconnection,” *Electronics Packaging Technology Conference (EPTC)*, IEEE 18th, December 2016, pp. 455–458.
81. Ding, M., B. Lau, and Z. Chen, “Molding process development for low-cost MEMS-WLCSP with silicon pillars and Cu wires as vertical interconnections,” *Electronics Packaging Technology Conference (EPTC)*, IEEE 19th, 2017.
82. Zeng, K., and A. Nangia, “Thermal cycling reliability of SnAgCu solder joints in WLCSP,” *Proc. 2014 IEEE 16th Electronics Packaging Technology Conference*, December 2014, pp. 503–511.
83. Peng Sun, “Package & board level reliability study of 0.35 mm fine pitch wafer level package,” *Proc. 2017 18th International Conference on Electronic Packaging Technology*, pp. 322–326.
84. Yeung, T., “Material characterization of a novel lead-free solder material – SACQ,” *IEEE/ECTC Proceedings, May 2014*, pp. 518–522.
85. Lau, J. H., C. Ko, T. Tseng, K. Yang, C. Peng, T. Xia, P. Lin, E. Lin, L. Chang, H. Liu, and D. Cheng, “Fan-In Panel-Level with Multiple Diced Wafers Packaging”, *IEEE/ECTC Proceedings*, May 2020, pp. 1146–1153.
86. Lau, J. H., C. Ko, T. Tseng, K. Yang, C. Peng, T. Xia, P. Lin, E. Lin, L. Chang, H. Liu, and D. Cheng, “Panel-Level Chip-Scale Package with Multiple Diced Wafers”, *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1110–1124.
87. Lin, Y., P. Marimuthu, K. Chen, H. Goh, Y. Gu, I. Shim, R. Huang, S. Chow, J. Fang, and X. Feng, “Semiconductor Device and Method of Forming Insulating layer Disposed Over the Semiconductor Die for Stress Relief”, *US Patent 8,456,002B2*, filling date: December 21, 2011.
88. Strothmann, T., S. Yoon, and Y. Lin, “Encapsulated Wafer Level Package Technology (eWLCSP)”, *Proceedings of IEEE/ECTC*, May 2014, pp. 931–934.
89. Lin, Y., K. Chen, K. Heng, L. Chua, and S. Yoon, “Encapsulated Wafer Level Chip Scale Package (eWLCSP™) for Cost Effective and Robust Solutions in FlexLine™”, *Proceeding of IEEE/IMPACT*, September 2014, pp. 316–319.
90. Lin, Y., K. Chen, K. Heng, L. Chua and S. Yoon, “Challenges and Improvement of Reliability in Advanced Wafer Level Packaging Technology”, *Proceedings of IEEE 23rd International Symposium on the Physical and Failure Analysis (IPFA)*, Singapore, July 2016, pp. 47–50.
91. Smith, L., and J. Dimaano Jr., “Development Approach & Process Optimization for Sidewall WLCSP Protection”, *Proceedings of IWLPC*, October 2015, pp. 1–4.
92. Tang, T., A. Lan, J. Wu, J. Huang, J. Tsai, J. Li, A. Ho, J. Chang, W. Lin, “Challenges of Ultra-thin 5 Sides Molded WLCSP”, *Proceedings of IEEE/ECTC*, May 2016, pp. 1167–1771.
93. Ma, S., T. Wang, Z. Xiao, D. Yu, “Process development of five-and six-side molded WLCSP”, *Proceedings of China Semiconductor Technology International Conference (CSTIC)*, March 2018, pp. 1–3.
94. Zhao, S., F. Qin, M. Yang, M. Xiang, and D. Yu, “Study on warpage evolution for six-side molded WLCSP based on finite element analysis”, *Proceeding of the International Conference on Electronic Packaging Technology (ICEPT)*, August 2019, pp. 1–4.
95. Qin, F., S. Zhao, Y. Dai, M. Yang, M. Xiang, and D. Yu, “Study of Warpage Evolution and Control for Six-Side Molded WLCSP in Different Packaging Processes”, *IEEE Transactions on CPMT*, Vol. 10, No. 4, April 2020, pp. 730–738.
96. Chi, Y., C. Lai, C. Kuo, J. Huang, C. Chung, Y. Jiang, H. Chang, N. Liu, and B. Lin, Board Level Reliability Study of WLCSP with 5-Sided and 6-Sided Protection”, *Proceedings of IEEE/ECTC*, May 2020, pp. 807–810.
97. Lau, J. H., C. Ko, T. Tseng, T. Peng, K. Yang, C. Xia, P. Lin, E. Lin, L.N. Liu, C. Lin, D. Cheng, and W. Lu, “Six-Side Molded Panel-Level Chip-Scale Package with Multiple Diced Wafers”, *IMAPS Proceedings*, October 2020, pp. 1–10.

98. Lau, J. H., C. Ko, T. Tseng, T. Peng, K. Yang, C. Xia, P. Lin, E. Lin, L.N. Liu, C. Lin, D. Cheng, and W. Lu, "Six-Side Molded Panel-Level Chip-Scale Package with Multiple Diced Wafers", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 17, December 2020, pp. 111–120.
99. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, Springer, New York, 2020.
100. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, V. 141, December 2019, pp. 1–27.
101. Borkulo, J., E. Tan, and R. Stam, "Laser Multi Beam Full Cut Dicing of Dicing of Wafer Level Chip-Scale Packages", *Proceedings of IEEE/ECTC*, May 2017, pp. 338–342.
102. Borkulo, J., and R. Stam, "Laser-Based Full Cut Dicing Evaluations for Thin Si wafers", *Proceedings of IEEE/ECTC*, May 2018, pp. 1945–1949.
103. Borkulo, J., R. Evertsen, R. Stam, "A More than Moore Enabling Wafer Dicing Technology", *IEEE/ECTC Proceedings*, May 2019, pp. 423–427.
104. Qu, S., J. Kim, G. Marcus, M. Ring, "3D Power Module with Embedded WLCSP", *IEEE/ECTC Proceedings*, May 2013, pp. 1230–1234.
105. Syed, A., K. Dhandapani, C. Berry, R. Moody, and R. Whiting, "Electromigration Reliability and Current Carrying Capacity of various WLCSP Interconnect Structures", *IEEE/ECTC Proceedings*, May 2013, pp. 714–724.
106. Arfaei1, B., S. Mahin-Shirazi, S. Joshi, M. Anselm1, P. Borgesen, E. Cotts, J. Wilcox, and R. Coyle, "Reliability and Failure Mechanism of Solder Joints in Thermal Cycling Tests", *IEEE/ECTC Proceedings*, May 2013, pp. 976–985.
107. Yang, S., C. Wu, D. Shih, C. Tung, C. Wei, Y. Hsiao, Y. Huang, and D. Yu, "Optimization of Solder Height and Shape to Improve the Thermo-mechanical Reliability of Wafer-Level Chip Scale Packages", *IEEE/ECTC Proceedings*, May 2013, pp. 1210–1218.
108. Hau-Riege, C., B. Keser, Y. Yau, S. Bezuk, "Electromigration of Solder Balls for Wafer-Level Packaging with Different Under Bump Metallurgy and Redistribution Layer Thickness", *IEEE/ECTC Proceedings*, May 2013, pp. 707–713.
109. Lai, Y., C. Kao, Y. Chiu, and B. Appelt, "Electromigration Reliability of Redistribution Lines in Wafer-level Chip-Scale Packages", *IEEE/ECTC Proceedings*, May 2011, pp. 326–331.
110. Darveaux, R., S. Enayet, C. Reichman, C. Berry, and N. Zafar, "Crack Initiation and Growth in WLCSP Solder Joints", *IEEE/ECTC Proceedings*, May 2011, pp. 940–953.
111. Yadav, P., S. Kalchuri, B. Keser, R. Zang, M. Schwarz, and B. Stone, "Reliability Evaluation on Low k Wafer Level Packages", *IEEE/ECTC Proceedings*, May 2011, pp. 71–77.
112. Franke, J., R. Dohle, F. Schüßler, T. Oppert, T. Friedrich, and S. Härtter, "Processing and Reliability Analysis of Flip-Chips with Solder Bumps Down to 30  $\mu\text{m}$  Diameter", *IEEE/ECTC Proceedings*, May 2011, pp. 893–900.
113. Bao, Z., J. Burrell, B. Keser, P. Yadav, S. Kalchuri, and R. Zang, "Exploration of the Design Space of Wafer Level Packaging Through Numerical Simulation", *IEEE/ECTC Proceedings*, May 2011, pp. 761–766.
114. England, L., "Solder Joint Reliability Performance of Electroplated SnAg Mini-Bumps for WLCSP Applications", *IEEE/ECTC Proceedings*, May 2010, pp. 599–604.
115. Walls, J., S. Kuo, E. Gelvin, and A. Rogers, "High-Sensitivity Electromigration Testing of Lead-Free WLCSP Solder Bumps", *IEEE/ECTC Proceedings*, May 2010, pp. 293–296.
116. Zhang, Y., and Y. Xu, "The Experimental and Numerical Investigation on Shear Behaviour of Solder Ball in a Wafer Level Chip Scale Package", *IEEE/ECTC Proceedings*, May 2010, pp. 1746–1751.
117. Liu, Y., Q. Qian, J. Kim, and S. Martin, "Board Level Drop Impact Simulation and Test for Development of Wafer Level Chip Scale Package", *IEEE/ECTC Proceedings*, May 2010, pp. 1186–1194.
118. Chen, L., Y. Hsu, P. Fang, and R. Chen, "Packaging Effect Investigation for MEMS-based Sensors WL-CSP with a Central Opening", *IEEE/ECTC Proceedings*, May 2010, pp. 1689–1695.

119. Okayama, Y., M. Nakasato, K. Saitou, Y. Yanase, H. Kobayashi, T. Yamamoto, R. Usui, and Y. Inoue, "Fine Pitch Connection and Thermal Stress Analysis of a Novel Wafer Level Packaging Technology Using Laminating Process", *IEEE/ECTC Proceedings*, May 2010, pp. 287–292.
120. Chen, L., C. Chen, T. Wilburn, and G. Sheng, "The Use of Implicit Mode Functions to Drop Impact Dynamics of Stacked Chip Scale Packaging", *IEEE/ECTC Proceedings*, May 2011, pp. 2152–2157.
121. Chang, S., C. Cheng, L. Shen, and K. Chen, "A Novel Design Structure for WLCSP With High Reliability, Low Cost, and Ease of Fabrication", *IEEE Transactions on Advanced Packaging*, September 2007, 30(3), pp. 377 – 383.
122. Zhou, T., S. Ma, D. Yu, M. Li, and T. Hang, "Development of Reliable, High Performance WLCSP for BSI CMOS Image Sensor for Automotive Application", *Sensors* 2020, 20(15), July 2020, pp. 4077–4083.
123. Lau, J. H., C. Ko, T. Peng, T. Tseng, K. Yang, T. Xia, B. Lin, E. Lin, L. Chang, H. Liu, C. Lin, Y. Fan, D. Cheng, and W. Lu, "Reliability of 6-side Molded Panel-Level Chip-Scale Packages (PLCSPs)", *IEEE/ECTC Proceeding*, May 2021.
124. Garrou, P., "Wafer level chip scale packaging (WL-CSP): an overview", *IEEE Transactions on Advanced Packaging*, Vol. 23, Issue: 2, May 2000, pp. 198–205.
125. Rogers, B., M. Melgo, M. Almonte, S. Jayaraman, C. Scanlan, and T. Olson, "Enhancing WLCSP Reliability Through Build-up Substrate Improvements and New Solder Alloys", *IWLPC Proceedings*, October 2014, pp. 1–7.
126. Wu, Z., H. Zhang, and J. Malinowski, "Understanding and Improving Reliability for Wafer Level Chip Scale Package: A Study Based on 45 nm RFSOI Technology for 5G Applications", *IEEE Journal of the Electron Devices Society*, September 2020, pp. 1–10.
127. Liu, T., C. Chen, S. Liu, M. Chang, and J. Lin, "Innovative methodologies of circuit edit by focused ion beam (FIB) on wafer-level chip-scale-package (WLCSP) devices", *Journal of Materials Science: Materials in Electronics*, Vol. 22, No. 10, pp. 1536–1541.
128. Rahangdale, U., B. Conjeevaram, A. Doiphode, and S. Kummerl, "Solder ball reliability assessment of WLCSP — Power cycling versus thermal cycling", *IEEE/ITHERM Proceedings*, June 2017, pp. 1361–1368.
129. Hsiao, A., M. Sheikh, K. Loh, E. Ibe, and T. Lee, "Impact of Conformal Coating Induced Stress on Wafer Level Chip Scale Package Thermal Performance", *SMTA Journal*, Volume 33 Issue 2, 2020, pp. 7–13.
130. Hsiao, A., G. Baty, E. Ibe, K. Loh, S. Perng, W. Xie, and T. Lee, "Edgebond and Edgefill Induced Loading Effect on Large WLCSP Thermal Cycling Performance", *SMTA Journal*, Volume 33 Issue 2, 2020, pp. 22–27.
131. Braun, T., K.-F. Becker, O. Hoelck, R. Kahle, M. Wohrmann, L. Boettcher, M. Topper, L. Stobbe, H. Zedel, R. Aschenbrenner, S. Voges, M. Schneider-Ramelow, and K.-D. Lang, "Panel Level Packaging – A View along the Process Chain", *Proceedings of IEEE/ECTC*, May 2019, pp. 70–78.
132. Braun, T., K. Becker, O. Hoelck, S. Voges, R. Kahle, M. Dreissigacker, and M. Ramelow, "Fan-Out Wafer and Panel Level Packaging as Packaging Platform for Heterogeneous Integration", *Micromachines*, May 2019, pp. 1–9.
133. Ueno, K., K. Dohi, Y. Suzuki, and M. Hirose, "Development of Sheet Typemolding Compounds for Panel Level Package", *Proceedings of IEEE/ECTC*, May 2019, pp. 2162–2167.
134. Fujinaga, T., "High rate and low damage etching method as pretreatment of seed layer sputtering for fan out panel level packaging", *Proceedings of IEEE/ECTC*, May 2019, pp. 358–362.
135. Weichert, J., J. Weichert, A. Erhart, and K. Viehweger, "Preconditioning Technologies for Sputtered Seed Layers in FOPLP", *Proceedings of IEEE/ECTC*, May 2019, pp. 1833–1841.
136. Selhofer, H., A. Mayr, and H. Pristauz, "Large Panel Size Bonder with High Performance and High Accuracy", *Proceedings of IEEE/ECTC*, May 2019, pp. 1492–1497.
137. Bu, L., F. X. Che, V. Rao, and X. Zhang, "Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging (FOPLP)", *Proceedings of IEEE/ECTC*, May 2019, pp. 1152–1158.

138. Che, F. X., K. Yamamoto, V. Rao, and V. Sekha, "Study on Warpage of Fan-Out Panel Level Packaging (FO-PLP) using Gen-3 Panel", *Proceedings of IEEE/ECTC*, May 2019, pp. 842–849.
139. Ko, C. T., H. Yang, J. H. Lau, et al., "Chip-First Fan-Out Panel Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, 2018, Vol. 8, Issue 9, September 2018, pp. 1561–1572.
140. Ko, C. T., H. Yang, J. H. Lau, et al., "Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 141–147.
141. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
142. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.
143. Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", *ASME Transactions, Journal of Electronic Package*, Vol. 143, June 2021, pp. 803–1 – 802-36.

# Chapter 4

## Fan-Out Wafer/Panel-Level Packaging



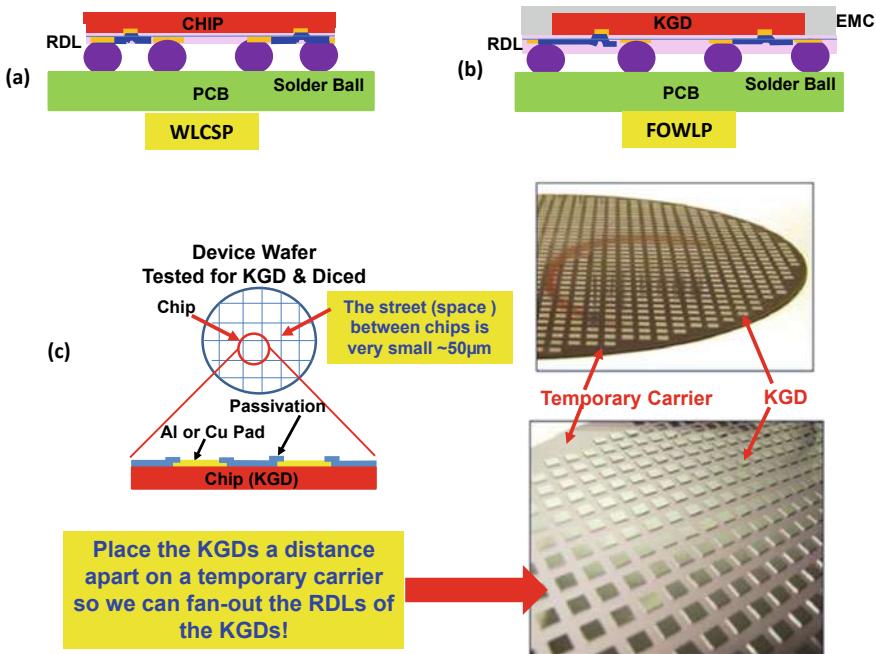
### 4.1 Introduction

First of all, both fan-in wafer/panel-level chip-scale packages (W/PLCSPs or simply WLCSP), Fig. 4.1a, and fan-out wafer/panel-level packaging (FOW/PLP or simply FOWLP), Fig. 4.1b, are wafer/panel-level packaging or simply WLP (wafer-level packaging). The biggest difference between WLCSP and FOWLP is that, FOWLP needs a temporary carrier but WLCSP does not. Why? Because the saw street (spacing) between chips on a device wafer is very small (~50  $\mu\text{m}$ ) and there is not enough space to fan-out the RDLs (redistribution-layers) of the chip. Thus, for FOWLP the device wafer is first tested for KGDs and then the wafer is diced into individual KGDs. It is followed by picking and placing the KGDs on a temporary carrier (either round or rectangular) with certain distance apart as shown in Fig. 4.1c.

There are many fan-out packaging formations [1–150]. However, basically there are three different kinds, namely chip-first (die face-down) [1–72], chip-first (die face-up) [73–94], and chip-last or RDL-first [95–150]. They will be discussed in this chapter with both round (wafer) and rectangular (panel) temporary carriers. At the end of this chapter, the design, materials, process, fabrication, and reliability of mini-LED RGB display by fan-out chip-first and die face-down panel-level packaging will be presented.

### 4.2 Fan-Out (Chip-First and Face-Down) Wafer-Level Packaging (FOWLP)

In this section, chip-first (die face-down) formations will be presented. The first fan-out wafer-level packaging (FOWLP) U.S. patent was filed by Infineon on October 31, 2001 [1, 2], and the first technical papers were also published (at ECTC2006 and EPTC2006) by Infineon and their industry partners: Nagase, Nitto Denko, and Yamada [3, 4]. At that time, they called it embedded wafer-level ball (eWLB) grid

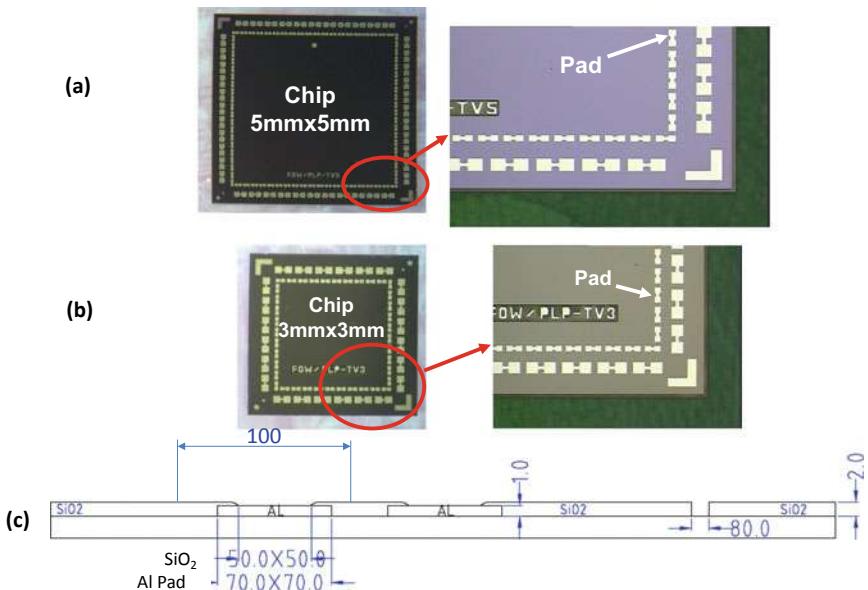


**Fig. 4.1** WLCSP versus FOWLP: FOWLP needs a temporary carrier

array. This technology eliminates wirebonding or wafer bumping and leadframe or package substrate, and potentially leads to a lower cost, better performance, and lower profile package. Alternatively, this technology requires a temporary (reconstituted) carrier for the known-good die (KGD), epoxy molding compound (EMC), molding, and the fabrication of the redistribution layers (RDLs).

During ECTC2007, Freescale presented a similar technology and called it redistributed chip package (RCP) [5]. IME extended the FOWLP technology to multi-die and stacked multi-die in 3-D format and presented at ECTC2008 [6]. During ECTC2009, IME presented four papers on: (1) a novel method to predict die shift during compression molding [7]; (2) laterally placed and vertically stacked thin dies [8]; (3) the reliability of 3-D FOWLP [9]; and (4) the demonstration of high quality and low-loss millimeter-wave passives on FOWLP [10].

In [12–15], it has been demonstrated the chip-first and die facedown fan-out wafer-level packaging for heterogeneous integration. The liquid EMC (epoxy molding compound) was compression molded. The metal line width and spacing of the RDLs (redistributed layers) were 10 and 15 µm. In this section, instead of using compression molding of the liquid EMC reported in [12, 13], herein we use a lamination method of a new dry-film EMC. Also, the minimum metal line width and spacing of the RDLs will be reduced from 10 to 5 µm. Furthermore, in order to save the expensive EMC materials and achieve low profile (thin) package, a special assembly process will be developed.



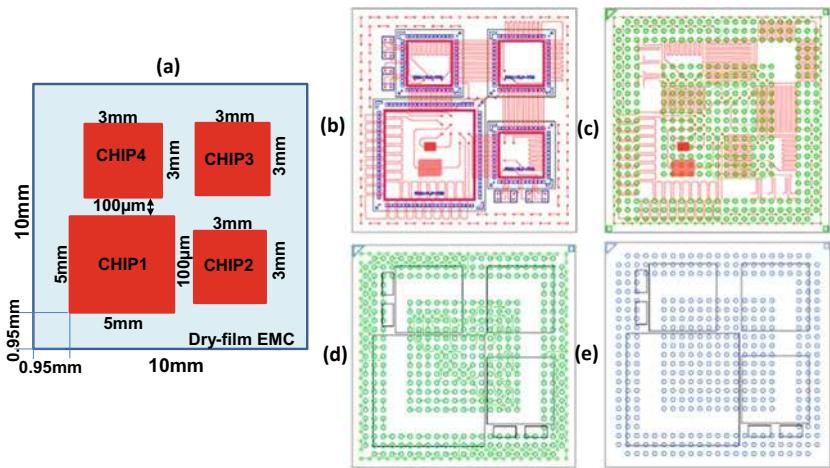
**Fig. 4.2** Top view and cross section view of the test chips

#### 4.2.1 Test Chips

Figure 4.2 shows the test chips under consideration. The layout and the fabricated large test chip are shown in Fig. 4.2a. It can be seen that the large chip sizes are  $5\text{ mm} \times 5\text{ mm} \times 150\text{ }\mu\text{m}$  and there are 160 pads with a pitch =  $100\text{ }\mu\text{m}$  (the inner rows). The SiO<sub>2</sub> passivation opening of the Al-pad is  $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$  and the size of the Al-pad is  $70\text{ }\mu\text{m} \times 70\text{ }\mu\text{m}$ . The dimensions of the small chip are  $3\text{ mm} \times 3\text{ mm} \times 150\text{ }\mu\text{m}$  and the fabricated chip is shown in Fig. 4.2b. It can be seen that there are 80 pads and are on  $100\text{ }\mu\text{m}$ -pitch (inner rows). The cross section and dimensions of the pads of the small chip are the same as those of the large chip.

#### 4.2.2 Test Package

Figure 4.3a schematically shows the test package under consideration. The dimensions of the test package are:  $10\text{ mm} \times 10\text{ mm}$  and it consists of one large chip ( $5\text{ mm} \times 5\text{ mm}$ ) and three small chips ( $3\text{ mm} \times 3\text{ mm}$ ). The spacing (gap) between the large chip and the small chip is  $100\text{ }\mu\text{m}$ . There are two RDLs of the test package. The RDLs between the chips and RDL1 is schematically shown in Fig. 4.3b, between the RDL1 and RDL2 is shown in Fig. 4.3c and between the RDL2 and the PCB is



**Fig. 4.3** Layout schematic (top-view) of the test package

shown in Fig. 4.3d. Figure 4.3e shows the footprint of the test package. These packages are to be made from a 300 mm glass reconstituted temporary wafer and the pitch of the test package on the wafer is 10.2 mm. In real applications, the large chip could be an application processor and the small chips could be memories. This is a very high throughput process. In one shot, 629 (10 mm × 10 mm) heterogeneous integration packages and each with 4 chips can be made.

Figure 4.4 schematically shows the cross-sectional view of the test package. It can be seen that there are 2 RDLs and the metal thickness of RDL1 is 3  $\mu\text{m}$  and RDL2 is 7.5  $\mu\text{m}$ . The metal line width and spacing of RDL1 are 5  $\mu\text{m}$  and those of RDL2 are 10  $\mu\text{m}$ , respectively. The dielectric layer thickness of DL1 and DL2 is 5  $\mu\text{m}$ , and DL3 is 10  $\mu\text{m}$ .

The via (VC1), through the first dielectric layer (DL1); connecting the Cu contact-pad of the test chip to the first RDL (RDL1) is 20–30  $\mu\text{m}$  in diameter. The pad-diameter on the RDL1 is 55  $\mu\text{m}$ , which is connected to RDL2 through the via (V12) with a diameter of 30–40  $\mu\text{m}$ . Similarly, the pad-diameter on the RDL2 is 65  $\mu\text{m}$ . Finally, 220  $\mu\text{m}$  solder-ball Cu pads are formed on RDL2. The opening of the passivation (DL3) is 180  $\mu\text{m}$ . The solder ball size is 200  $\mu\text{m}$  and ball pitch is 0.4 mm.

#### 4.2.3 Conventional Chip-First (Face-Down) Wafer Process

Figure 4.5 shows, in general, the conventional process flow of chip-first with die face-down FOWLP. First, the device wafer is tested for known-good dies (KGDs) and then singulated into individual dies. This is followed by picking up the KGDs and placing them face-down on a temporary carrier (which can be metal, silicon,

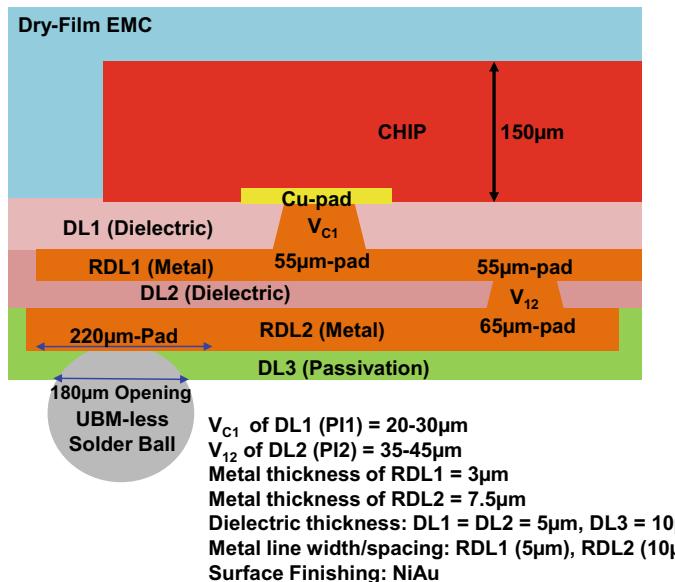


Fig. 4.4 Layout schematic (cross-section view) of the test package

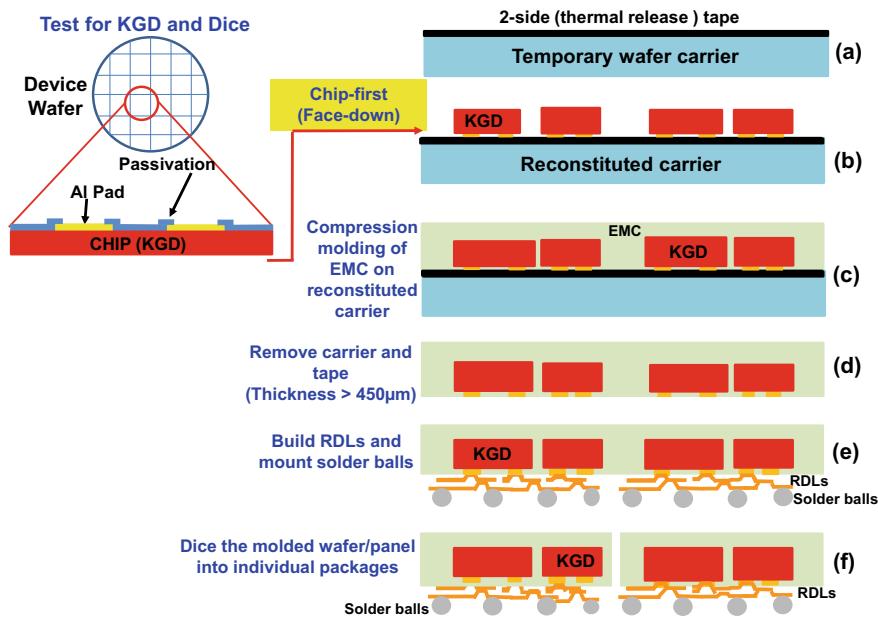
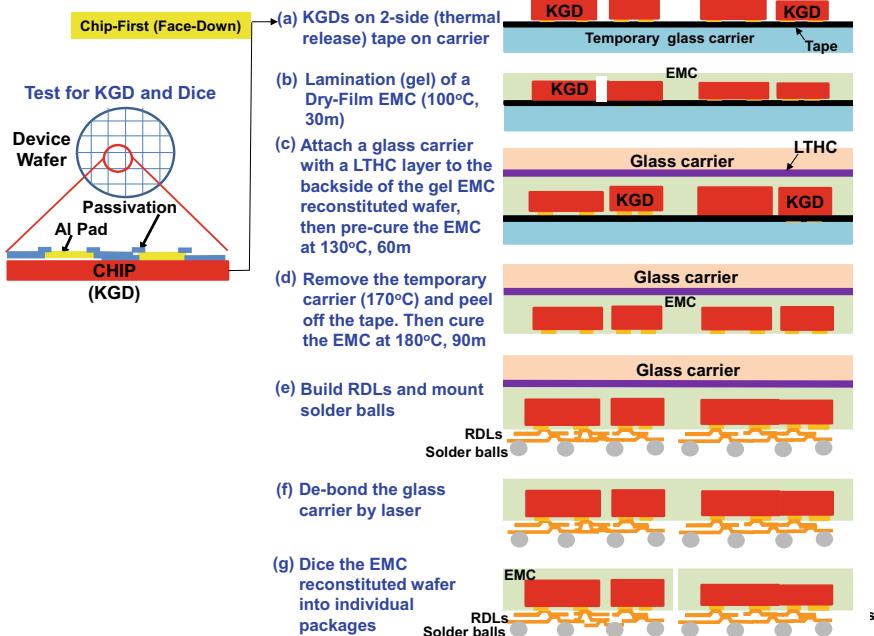


Fig. 4.5 Chip-first (die face-down) conventional key process steps

or glass) that can be round (wafer) or rectangular (panel), Fig. 4.5b, with a double sided thermal release tape, Fig. 4.5a. Then, the reconstituted (temporary) carrier with the KGDs are molded with EMC, Fig. 4.5c, using the compression method + PMC (post mold cure) before removing the carrier and the peeling off the double-sided tape, Fig. 4.5d. Next comes building the RDLs, Fig. 4.5e. Finally, solder balls are mounted and the whole reconstituted carrier (with KGDs, RDLs, and solder balls) is diced into individual packages, Fig. 4.5f.

#### 4.2.4 New Process for Heterogeneous Integration Package

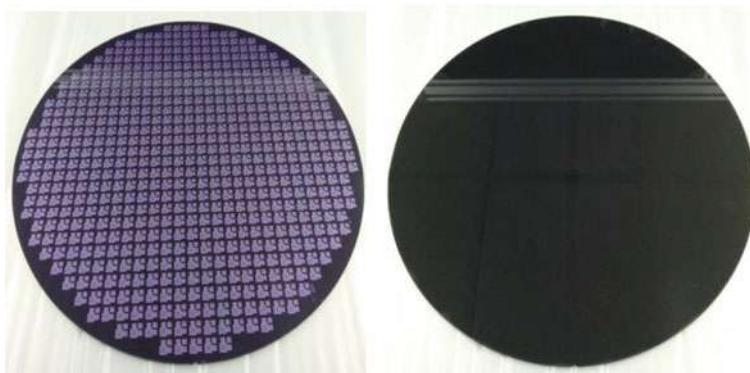
In the present study, we will not use the conventional method such as Fig. 4.5c to compression molding the EMC and Fig. 4.5e to build the RDLs. Instead, we will use the new process shown in Fig. 4.6.



**Fig. 4.6** Chip-first (die face-down) new key process steps

**Table 4.1** Material properties of the dry-film EMC

	Previous	Current
EMC material	Liquid	Dry film
	EMC (R4507)	New EMC
Filler max cut ( $\mu\text{m}$ )	25	5
Filler contents (%)	85	80
Tg (DMA) ( $^{\circ}\text{C}$ )	150	163
CTE 1 (ppm/K)	10	15
CTE 2 (ppm/K)	41	23
Young's modulus (GPa)	19	10



**Fig. 4.7** Right after the step of Fig. 4.6c. (L) Glass-side. (R) Dry-film EMC-side

#### 4.2.5 Dry-Film EMC Lamination

In [22], we had used a liquid EMC and compression molding method. In this study, we will use a new dry-film EMC with material properties shown in Table 4.1 and the EMC molding method is by lamination. After pick and place the KGDs on the carrier, Fig. 4.6a, b, the 200  $\mu\text{m}$ -thick dry-film EMC is laminated (gelled) on the reconstituted wafer at 100  $^{\circ}\text{C}$  for 30 min as shown in Figs. 4.6c and 4.7.

#### 4.2.6 Temporary Bonding Another Glass Carrier

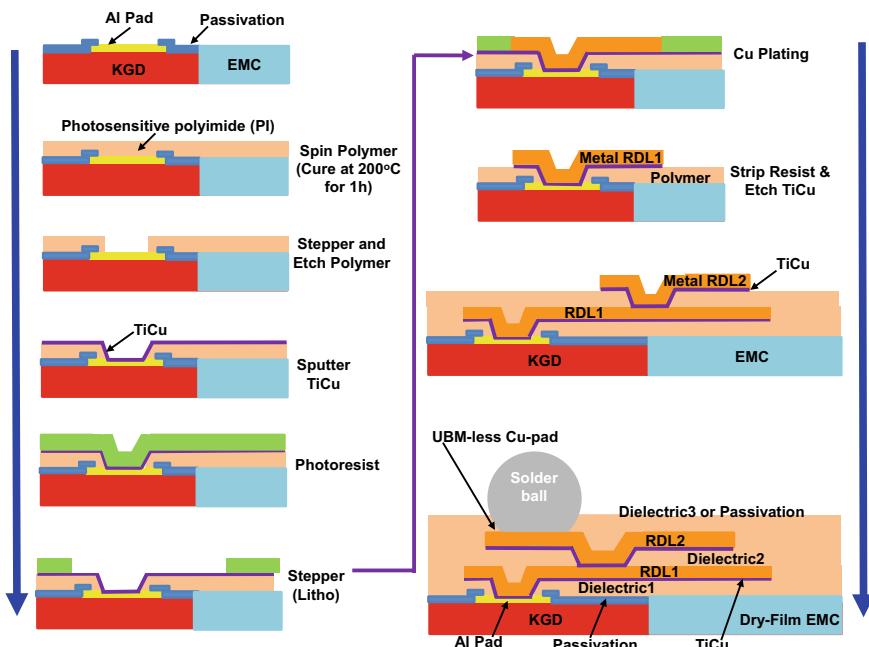
In the conventional FOWLP, after EMC molding, then debond the carrier and peel off the tape, Fig. 4.5d, the total thickness of the reconstituted wafer is usually  $\geq 450 \mu\text{m}$ . It is followed by building the RDLs and mounting the solder balls, Fig. 4.5e. However, in this study, in order to save the expensive EMC materials and have a very low profile (thin) package, the total thickness of our reconstituted wafer without the carrier is

only 300  $\mu\text{m}$ . Thus, the reconstituted wafer is too fragile to fabricate the RDLs and mount the solder balls.

One of the solutions is to attach the thin reconstituted wafer on another 1 mm-thick glass ( $\text{CTE} = 6.4 \times 10^{-6}/^\circ\text{C}$ ) wafer with a coated LTHC (light-to-heat-conversion) layer as shown in Fig. 4.6d. Then, pre-cure the dry-film EMC at 130  $^\circ\text{C}$  for 60 min. Next, remove the first temporary carrier and peel off the tape, Fig. 4.6e. It is followed by curing the dry-film EMC at 180  $^\circ\text{C}$  for 90 min.

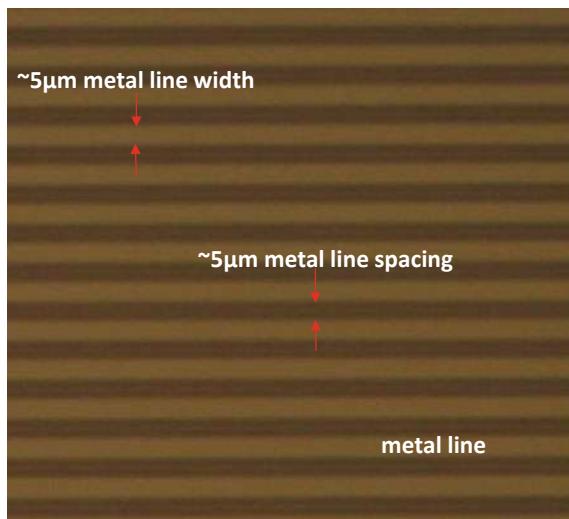
#### 4.2.7 RDLs

Now, it is ready to build the RDLs as shown in Fig. 4.6f. Figure 4.8 shows the key process steps in making the RDLs. First, spin coat a photosensitive polyimide (PI) on the reconstituted wafer. Then apply a stepper (every 4 test packages as a unit) and use photolithography techniques to align, expose, and develop the vias of the PI. Finally, cure the PI at 200  $^\circ\text{C}$  for one hour. This will form a 4 to 5- $\mu\text{m}$ -thick PI layer. (PI development.) It is followed by Sputtering Ti and Cu by physical vapor deposition (175–200  $^\circ\text{C}$ ) over the entire wafer. Apply a photoresist and a stepper and then use photolithography techniques to open the redistribution-traces locations. Then electroplate Cu by electrochemical deposition (at room temperature) on Ti/Cu

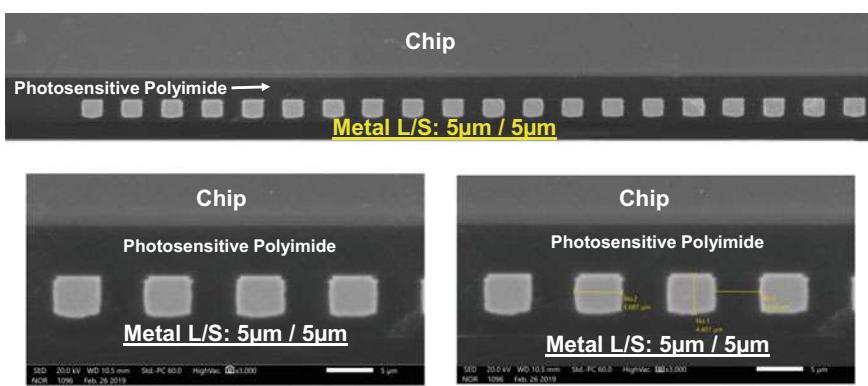


**Fig. 4.8** Key process steps in fabricating the RDLs

in photoresist openings. Strip off the photoresist and etch off the Ti/Cu. (RDL1 is obtained.) Repeat the above steps to obtain RDL2. Figure 4.9 shows the metal line width and spacing of RDL1. It can be seen that the metal line width and spacing of RDL1 are very close to the design value (5  $\mu\text{m}$ ). Figure 4.10 shows the SEM (scanning electron microscope) cross section images of the RDL1. It can be seen that the chip, the photosensitive polyimide, and the RDL1 with metal line width and spacing = 5  $\mu\text{m}$ .



**Fig. 4.9** Top views of the 5  $\mu\text{m}$  metal linewidth and spacing RDL



**Fig. 4.10** Cross section images of the chip, photosensitive polyimide, and RDL1. The metal line width and spacing of RDL1 are 5  $\mu\text{m}$

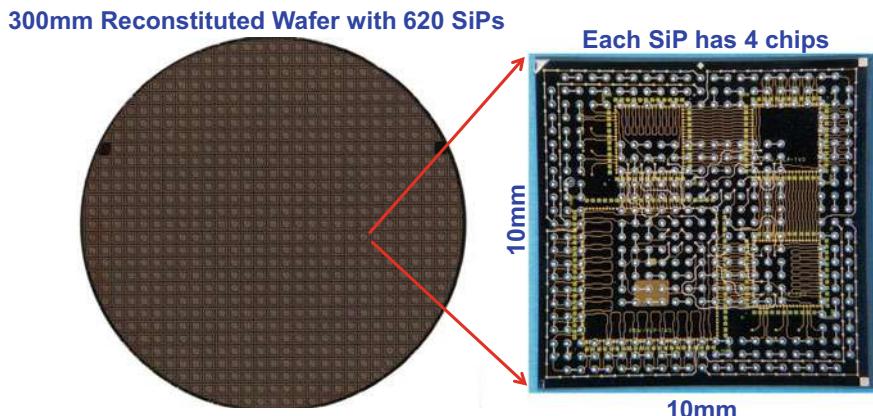
#### 4.2.8 Solder Ball Mounting

There are two different stencils for the solder ball mounting, Fig. 4.6f, one is for stencil printing the flux and the other is for stencil mounting the solder balls. The solder (Sn3wt%Ag0.5 wt%Cu) balls (200  $\mu\text{m}$ -diameter) used are on a 0.4 mm-pitch. The peak temperature for solder reflow is 245 °C.

#### 4.2.9 Final De-Bonding

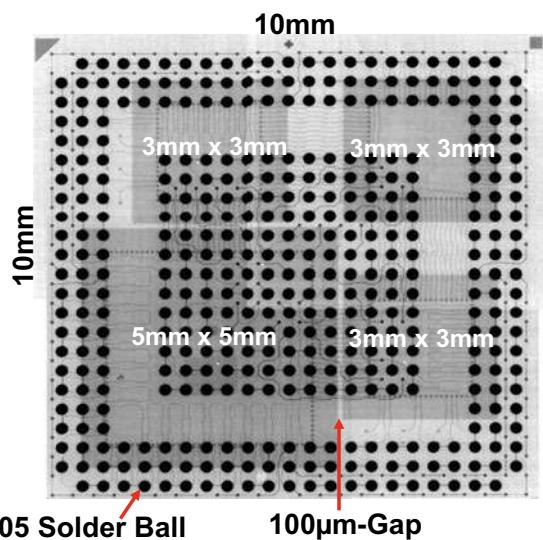
The de-bonding of the glass carrier as shown in Fig. 4.6g is by scanning a laser (355 nm DPSS Nd: YAG UV laser source is used) from the glass carrier side. The laser spot-size is 240  $\mu\text{m}$ , the scanning speed is 500 mm/s and the scanning pitch is 100  $\mu\text{m}$ . When the LTHC layer “sees” the laser light, it converts into powders and the glass carrier is easily removed. It is followed by chemical cleaning. Figure 4.11 shows the reconstituted wafer without any carrier and a closed-up on one of the package. It can be seen that there are 4 chips in a package and they are properly fabricated. The reconstituted wafer is diced, as shown in Fig. 4.6h, into individual packages as shown in the x-ray image in Fig. 4.12, where also shows the RDL1 and RDL2 of the package.

Figure 4.13 shows a typical cross section of the heterogeneous integration package. It can be seen that there are two RDLs. The thickness of the metal layer of RDL2 (7.5  $\mu\text{m}$ ) is thicker than that of RDL1 (3  $\mu\text{m}$ ). The thicker metal layer of RDL2 is for the UBM-less thicker Cu pads to “resist” the Cu consumption from the solder ball reflow and during operation.

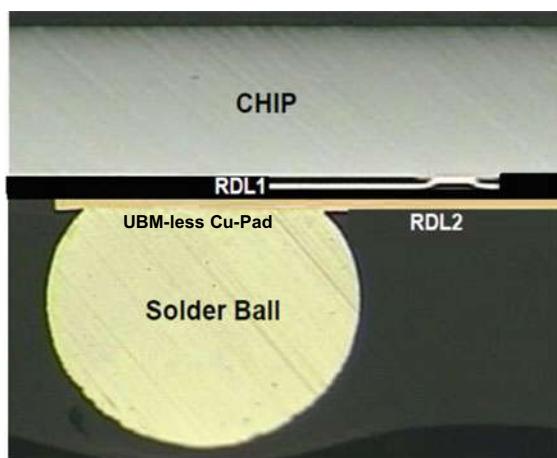


**Fig. 4.11** 300mm reconstituted wafer with 620 good SiPs. Each SiP (10 mm × 10 mm) has one large chip (5 mm × 5 mm) and three small chips (3 mm × 3 mm)

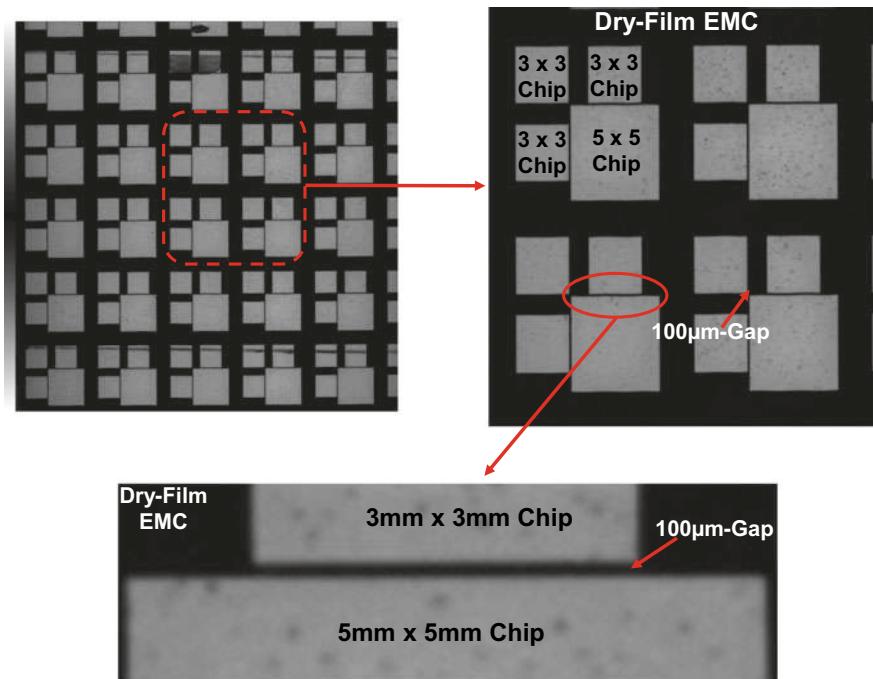
**Fig. 4.12** X-ray images of the heterogeneous integration of one large chip ( $5\text{ mm} \times 5\text{ mm}$ ) and three small chips ( $3\text{ mm} \times 3\text{ mm}$ ). The dimensions of the SiP are  $10\text{ mm} \times 10\text{ mm}$  and there're 405  $200\text{ }\mu\text{m}$ -diameter solder balls on  $0.4\text{ mm}$ -pitch



**Fig. 4.13** Cross section of the individual package



Inspections for dry-film EMC lamination molding voids are carried out by C-SAM (C-mode scanning acoustic microscopy). In order to balance the resolution and signal penetration depth, a transducer of 75 MHz is selected for the voids observation. After a couple of parametric studies, there is not any void in the optimal wafers (EMC as well as gap) as shown in Fig. 4.14.



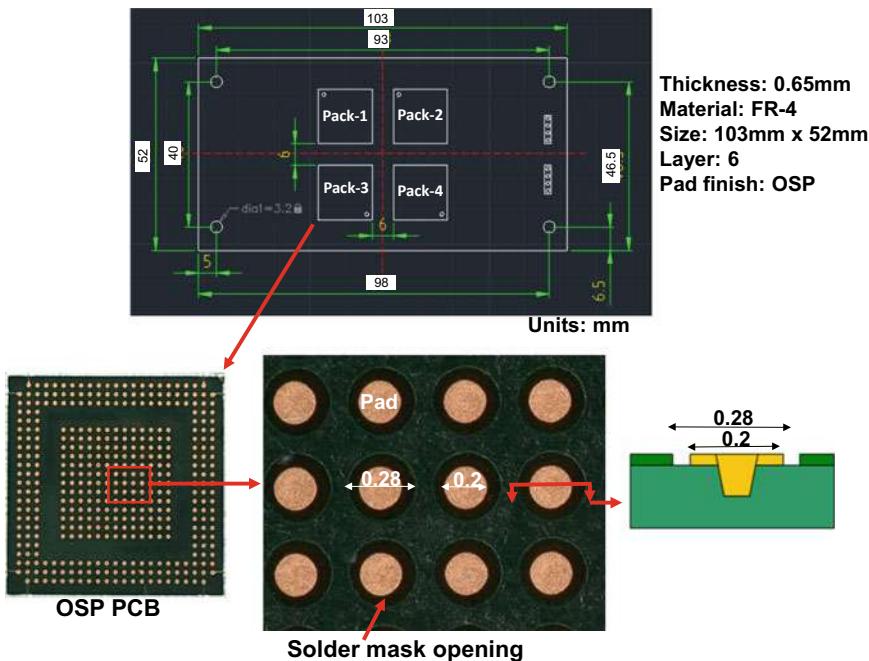
**Fig. 4.14** C-mode SAM image showing there is not any obvious void in the dry-film EMC even in the 100  $\mu\text{m}$ -gap between the large chip and small chips

#### 4.2.10 PCB Assembly

The design of the printed circuit board (PCB) and stencil will be briefly mentioned. The stencil solder paste printing, pick and place, and solder reflow will also be presented. The X-ray images and the cross-sectional images of the PCB assembly are provided.

##### (A) PCB

The PCB for the fan-out panel-level package is made of FR-4 and is shown in Fig. 4.15. It can be seen that there are four package sites on the board. The dimensions of the PCB are 103 mm  $\times$  52 mm  $\times$  0.65 mm, and there are six layers. There are 405 pads (with a pitch = 0.4 mm) for each package. The pad with a diameter = 0.2 mm is non-solder mask defined, and its surface finish is an organic solderability preservative. The solder mask opening diameter is 0.28 mm.



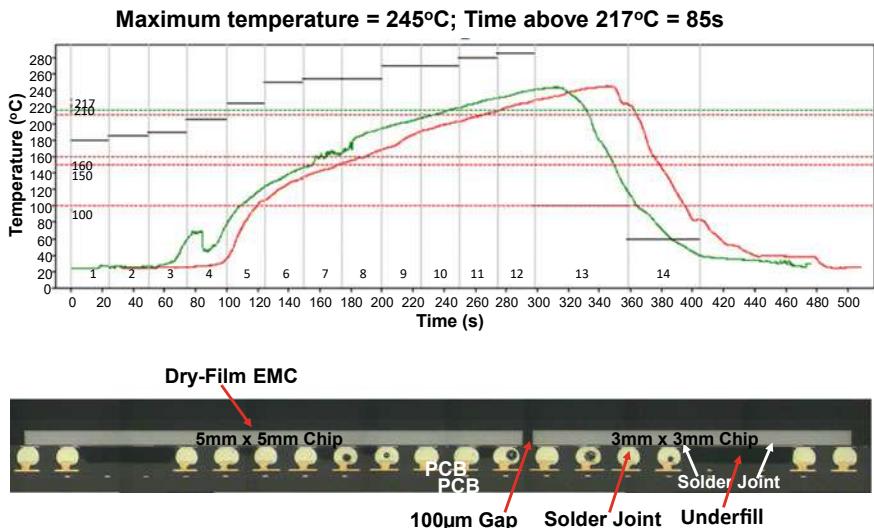
**Fig. 4.15** PCB layout and the fabricated PCB

### (B) Stencil and Printing

The stencil is made of stainless steel with a grain size of  $2 \mu\text{m}$  (which will benefit for the solder paste transfer) and is 0.08 mm thick. The opening is fabricated by laser and electrical/chemical polishing. The solder paste printing is by the DEK Horizon 9.

### (C) Pick and Place and Reflow

The pick and place is by the SiPlace x4s. The 10-temperature zones BYU Pyram nitrogen 150 N is used for the reflow. The temperature profile is shown in Fig. 4.16. It can be seen that the maximum temperature is  $245^\circ\text{C}$ , and the time above  $217^\circ\text{C}$  is 85 s.



**Fig. 4.16** SMT reflow profile. Cross section of the PCB assembly of the heterogeneous integration

#### 4.2.11 Reliability (Drop Test) of the Heterogeneous Integration

The reliability assessment of the PCB assembly of heterogeneous integration of 4 chips by FOWLP with chip-first and face-down as shown in Fig. 4.16 is by drop test.

##### (A) Drop Test Setup

The test setup is according to JEDEC Standard JESD22-B111 as shown in Fig. 4.17. After more than 20 tries, the right height of the drop table is obtained which yields the drop spectrum with 1500G/ms as shown in Fig. 4.18.

##### (B) Drop Test Results

The drop condition is 1,000 drops. There are 24 samples with underfill. All the samples pass 500 drops. The first failure occurs at 550 drops and the failure location is shown in Fig. 4.19. It can be seen that a few corner solder joints near the center of the PCB failed. The failure mode is shown in Fig. 4.20. It can be seen that the solder cracking occurs near the interface between the chip and the bulk solder.

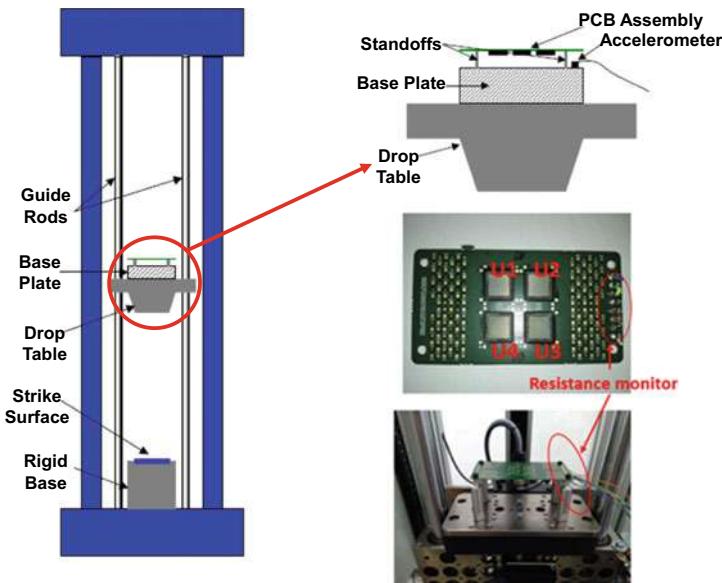


Fig. 4.17 Drop test setup

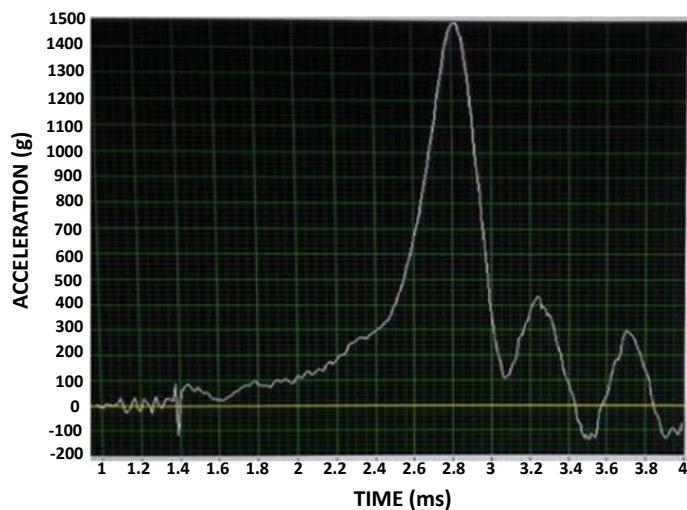


Fig. 4.18 Drop spectrum

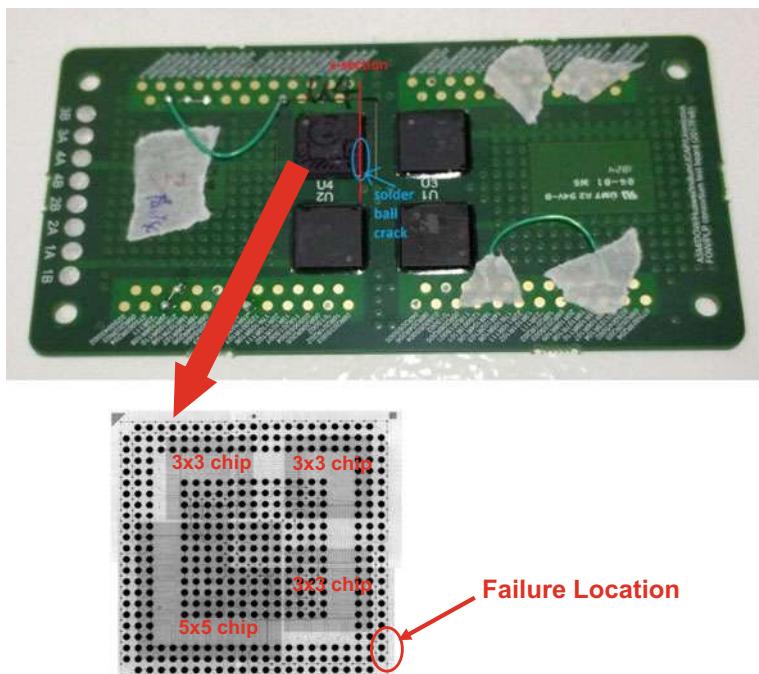


Fig. 4.19 Failure location of the PCB assembly of the heterogeneous integration under drop test

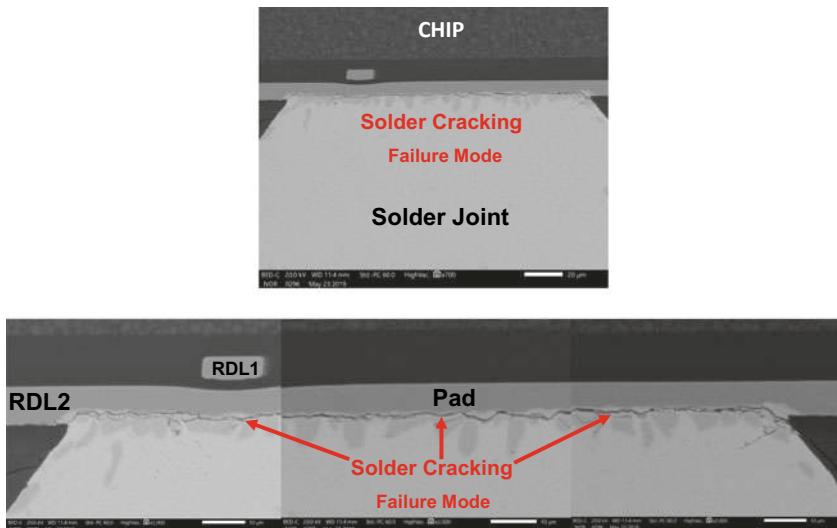


Fig. 4.20 Failure mode of the PCB assembly of the heterogeneous integration under drop test

#### 4.2.12 Summary and Recommendation

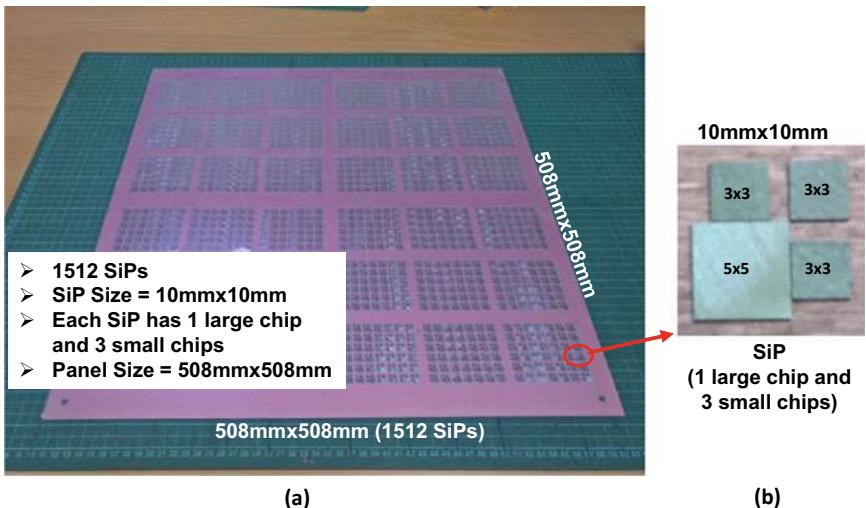
The design, materials, process, and fabrication of a thin heterogeneous integration of 4 chips by a new FOWLP method have been investigated. Some important results and recommendations are summarized as follows [12, 13].

- The minimum metal line width and spacing of the RDLs = 5  $\mu\text{m}$  have been fabricated. The accuracy has been demonstrated by both optical and SEM images.
- The gap between the large chip (5mmx5mm) and the small chip (3mmx3mm) is 100  $\mu\text{m}$ . It has been found by the C-SAM method that there is not any void in the dry-film EMC and the gap.
- A dry-film EMC has been chosen and a lamination method of the dry-film EMC has been developed.
- Both x-ray and optical microscope images verified that the 4 chips have been assembled properly.
- Both x-ray and optical microscope images demonstrated that the RDLs have been properly fabricated.
- The heterogeneous integration package thickness is 300  $\mu\text{m}$  (not including the solder balls). It is not only save expensive EMC cost but leads to a very low-profile (thin) package.
- The proposed assembly process, i.e., by attaching the thin reconstituted molded wafer on another temporary glass wafer with a coated LTHC layer, provided a better warpage control, an opportunity for making supper low-profile package, and a way to save the EMC material.
- The thin heterogeneous integration package has been assembled on a PCB and through a shock (drop) test.

### 4.3 Fan-Out (Chip-First and Face-Down) Panel-Level Packaging (FOPLP)

The same test chips (5 mm  $\times$  5 mm and 3 mm  $\times$  3 mm) used in Sect. 4.2 for FOWLP are used herein for FOPLP study [15]. The size of the package is the same (10 mm  $\times$  10 mm) as that in Sect. 4.2, but the structure of the package is different. Instead of 5 and 10  $\mu\text{m}$  metal line width and spacing in the FOWLP, 10 and 25  $\mu\text{m}$  are used in the present FOPLP. Also, the semiconductor equipment has been used for making the FOWLP; herein the PCB equipment is used for fabricated the FOPLP. Furthermore, the temporary carrier for the FOPLP is a rectangular panel.

In order to have a very high-throughput and low-profile package and save the expensive EMC; a process called uni-substrate-integrated package (Uni-SIP) [15] is used to fabricate the RDLs. The panel dimensions are 508 mm  $\times$  508 mm (Fig. 4.21) and a dry-film EMC is laminated on the reconstituted panel (instead of the liquid EMC with compression molding).

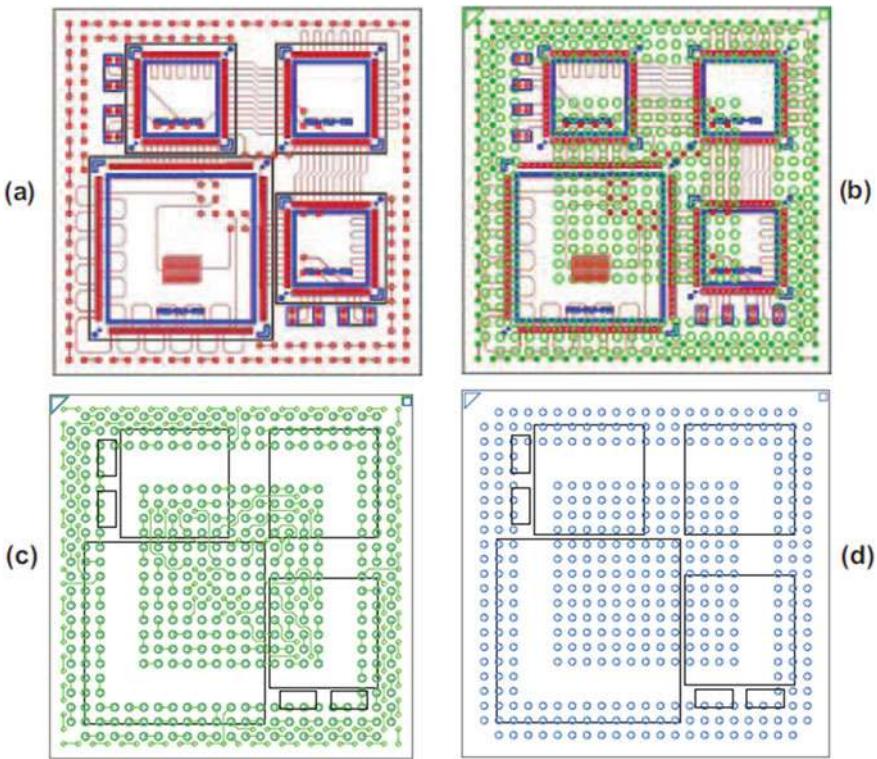


**Fig. 4.21** Reconstituted panel ( $508 \times 508$  mm) with 1512 SiPs, and each SiP with four chips

### 4.3.1 Heterogeneous Integration of Test Package

The test package, Fig. 4.21b, looks the same as that in [12, 13]. However, the major differences are: (1) a new dry-film EMC instead of a liquid EMC is used, (2) the EMC is fabricated by a lamination method instead of a compression method, (3) the metal line width and spacing is reduced from  $20 \mu\text{m}$  to  $10 \mu\text{m}$ , (4) the panel size is increased from  $340 \text{ mm} \times 340 \text{ mm}$  to  $508 \text{ mm} \times 508 \text{ mm}$ , and (5) a new desmear and electroless Cu plating process. The spacing (gap) between the large chip and the small chip is  $100 \mu\text{m}$ . There are two RDLs of the test package. The RDLs between the chips and RDL1 is schematically shown in Fig. 4.22a, between the RDL1 and RDL2 is shown in Fig. 4.22b, and between the RDL2 and the PCB is shown in Fig. 4.22c. Figure 4.22d shows the footprint of the test package. These packages are to be made from a  $508 \text{ mm} \times 508 \text{ mm}$  reconstituted panel as shown in Fig. 4.21a. There are 1,512 heterogeneous integration packages and each one with 4 chips.

Figure 4.23 schematically shows the cross-sectional view of the test package. It can be seen that there are two RDLs, and the thickness of the metal layer of RDL1 and RDL2 is  $10 \mu\text{m}$ . The metal line width and spacing of RDL1 are  $10 \mu\text{m}$  (which is different from  $20 \mu\text{m}$  of [14]), and those of RDL2 are  $25 \mu\text{m}$ . The dielectric layer thickness of DL1, DL2, and DL3 is  $20 \mu\text{m}$ . The via through the first dielectric layer (DL1), connecting the Cu contact pad of the test chips to the first RDL (RDL1) is  $50 \mu\text{m}$  in diameter. The pad diameter on the RDL1 is  $135 \mu\text{m}$ , which is connected to RDL2 through the via with a diameter of  $50 \mu\text{m}$ . Similarly, the pad diameter on the RDL2 is  $135 \mu\text{m}$ . Finally,  $230 \mu\text{m}$  solder-ball Cu pads are formed on RDL2. The opening of the solder mask (DL3) is  $180 \mu\text{m}$ . The solder ball diameter is  $200 \mu\text{m}$ , and the ball pitch is  $0.4 \text{ mm}$ .



**Fig. 4.22** Test package. One  $5 \times 5$  mm chip and three  $3 \times 3$  mm chips. Package dimensions =  $10 \times 10$  mm. **a** The RDLs between the chips and RDL1. **b** The RDL between the RDL1 and RDL2. **c** The RDL between the RDL2 and the PCB. **d** The footprint of the test package

### 4.3.2 A New Uni-SIP Process

Figure 4.24 shows the new Uni-SIP process. The temporary carrier is made of an organic substrate with the coefficient of thermal expansion (CTE) =  $4 \times 10^{-6}/^{\circ}\text{C}$ . The thickness of the organic carrier is 1 mm. The advantages of 1 mm-carrier are: (a) not easy to break when it is cleaned and reused, and (b) to increase the stiffness and resist to bending (warpage) of the reconstituted carrier during pick and place of the chips, the 2-stage vacuum lamination, and post mold cure (PMC) of the dry-film EMC. After a temporary carrier is chosen, then attach the 2-side thermal release tape (REVALPHA) provided by Nitto Denko on top of the carrier, Fig. 4.24a. It is followed by picking and placing the chips on top of the tape, Fig. 4.24b.

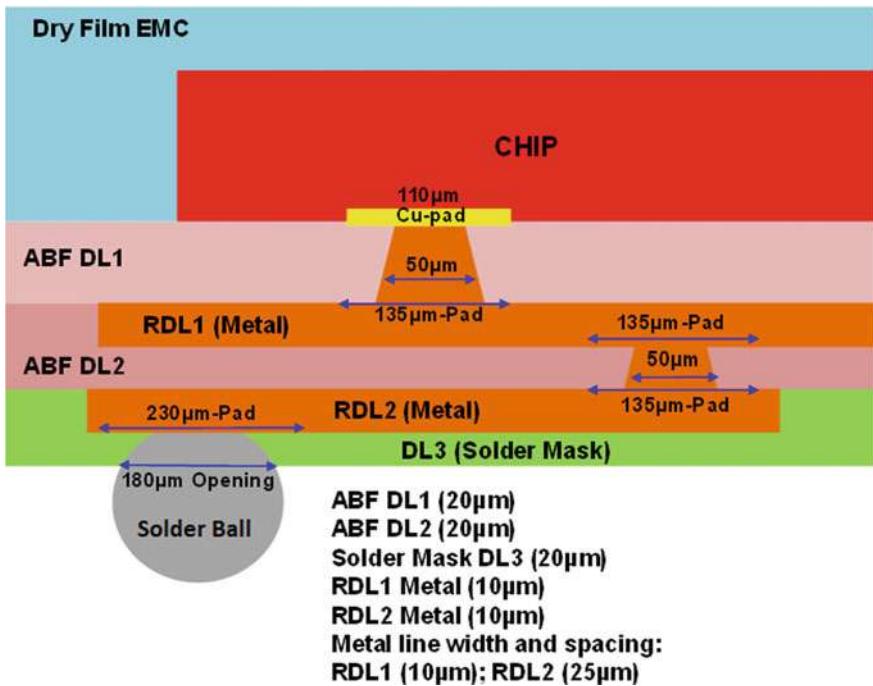


Fig. 4.23 Cross section of the test package

#### 4.3.3 Dry-Film Lamination of ECM-Panel

For large panel size such as the 508 mm × 508 mm, the liquid (previous) EMC is difficult to fill the full panel without flow marks and the EMC total thickness variation (TTV) between the corner and the center of the panel is large. The advantages of dry-film EMC are: (a) better flattening control, (b) more consistent TTV as full panel, (c) PCB process suitable, (d) higher throughput, and (e) less particle pollution. In this study, a dry-film EMC is used.

The material properties of the dry-film EMC are shown in Table 4.1. It can be seen that the filler content is 80% and the maximum size of the filler is 5  $\mu\text{m}$ . The Young's modulus of the EMC is 10GPa and the glass transition temperature ( $T_g$ ) is 163 °C. The dry-film EMC is laminated on top of the carrier and chips, Fig. 4.24c, by a 2-stage vacuum lamination machine as shown in Fig. 4.25. The first stage is vacuum lamination (100 °C and vacuum for 30 s and press (0.68 MPa) for 30 s), which is for the resin of the dry-film EMC to be confirmed. After vacuum lamination, it is followed by the second stage (flattening press: 100 °C for 60 s and press (0.54 MPa)), which is for the surface of the dry-film EMC to be flattened. Then, cure the structure at 150 °C for 1 h + 180 °C for 0.5 h. The structure of Fig. 4.24c is called ECM-panel. (In this study, chips embedded in the dry film EMC are called the ECM-panel).

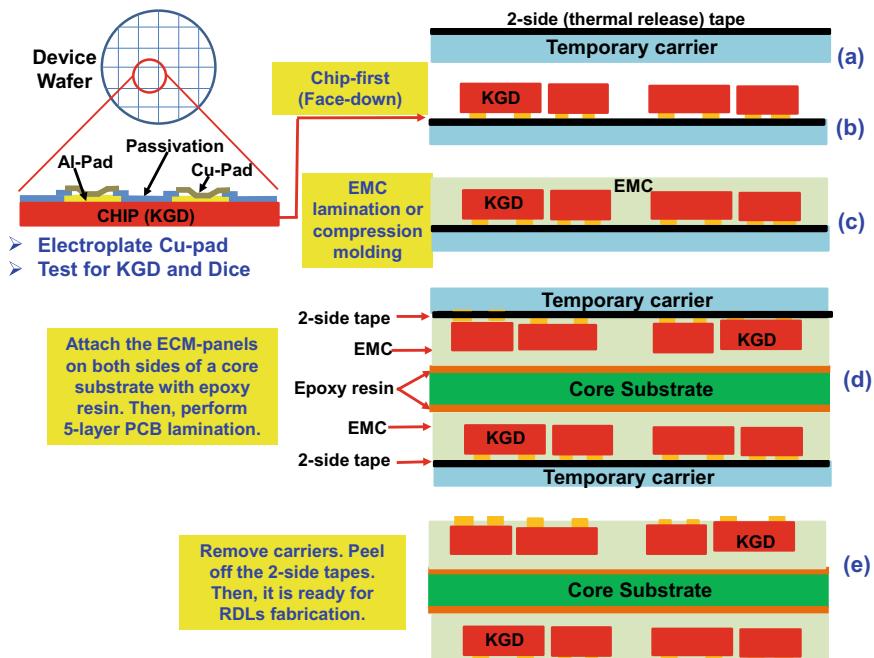


Fig. 4.24 Uni-SIP key process steps

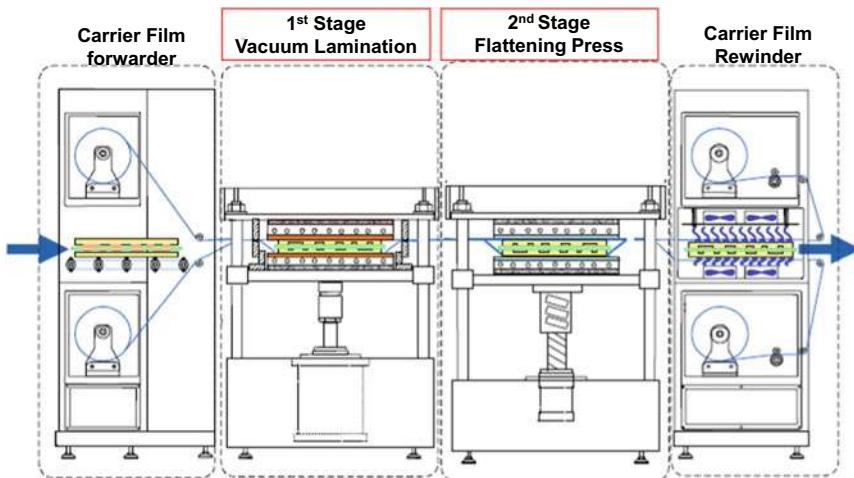


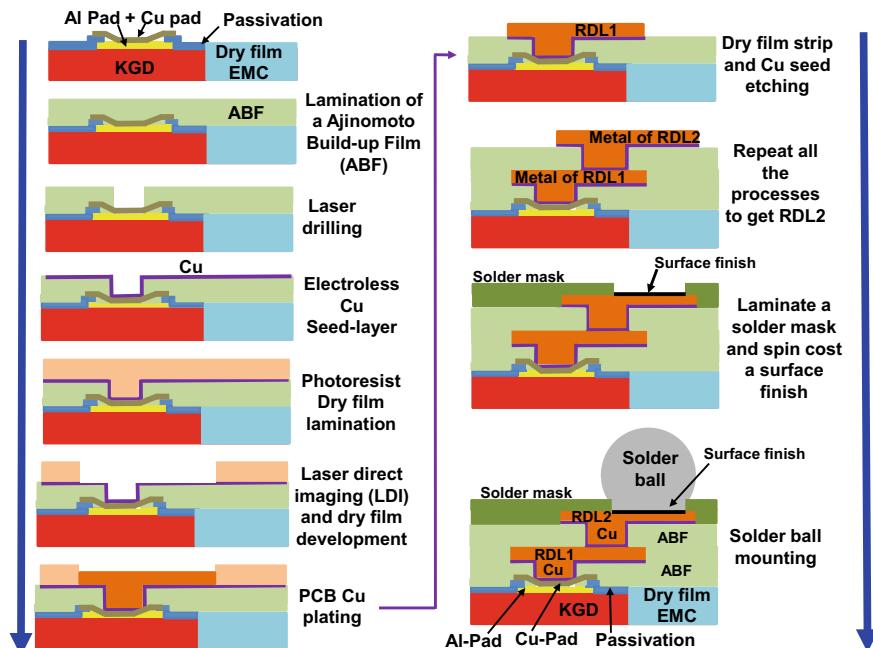
Fig. 4.25 2-stage vacuum lamination machine

#### 4.3.4 Lamination of Uni-SIP Structure

The next step is to attach an epoxy resin on both side of another organic core carrier (substrate). Then, attach the back-side of the ECM-panel to both sides of the core carrier as shown in Fig. 4.24d. It is followed by a 5-layer (ECM-panels on both sides + core) PCB lamination with the same 2-stage vacuum lamination machine as shown in Fig. 4.25 and the conditions are the same as the 2-layer ECM-panel. Then, remove the temporary carrier and peel of the tape, Fig. 4.24e. It is ready for making the RDLs on the pads on both sides of the chips.

#### 4.3.5 Lamination of the New ABF, Laser Drilling, and De-Smeared

Figure 4.26 shows the process steps in fabricating the RDLs from the Cu pads on both sides of the Uni-SIP structure shown in Fig. 4.24e. First, laminate a new ABF (Table 4.2) on both sides of the chips. In order to control the panel warpage, the selection of ABF and EMC materials is an important consideration. The CTE of ABF should be matched to the equivalent one of ECM-panel. Also, for fine metal



**Fig. 4.26** Key process steps in fabricating the RDLs from the Cu pads on both sides of the Uni-SIP structure

**Table 4.2** Material properties of the ABFs

Item	Old ABF	New ABF
Filler max cut ( $\mu\text{m}$ )	15	5
Filler contents (%)	82	80
CTE (30–150 °C) (ppm/K)	7	15
Young's modulus (GPa)	7	10
Dielectric constant (Dk)	3.2	3.3

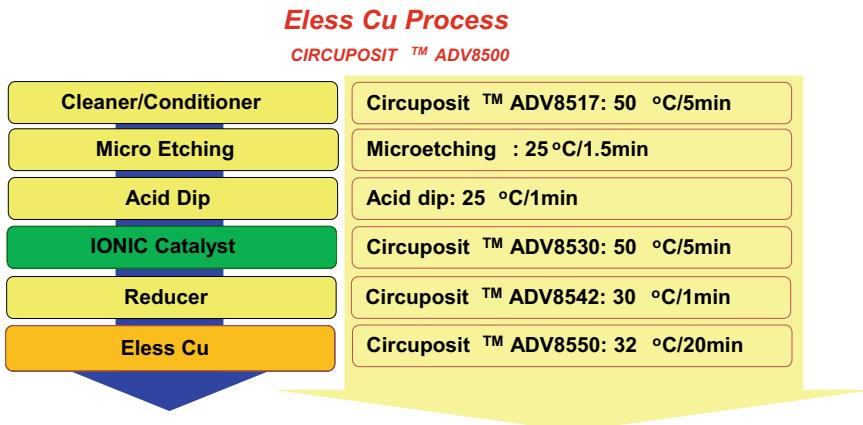
line width and spacing ( $\leq 10 \mu\text{m}$ ) applications, the filler size should be small. In this study, the CTE ( $15 \times 10^{-6}/\text{°C}$ ) of ABF (5  $\mu\text{m}$ ) is significantly smaller. Furthermore, the previous DF (Dry Film) and LDI combination only can get the limit resolution down to 20  $\mu\text{m}$ . The new thinner DF (12  $\mu\text{m}$ ) and more advanced LDI used in this study can get the limit resolution down to 5  $\mu\text{m}$  on glass.

After the lamination of the ABF on both sides of the chips, then laser drill the ABF and stop at the Cu pad (this is the reason for making the Cu pad on the device wafer) as shown in Fig. 4.26. Before metallization, a post laser de-smear of the ABF dielectric is generally required for surface roughening to achieve sufficient adhesion of electroless-Cu to ABF. In this study, DOW's SAP solution—CIRCOPIST 7800 de-smear process (Fig. 4.27) and CIRCUPOSIT ADV 8500 Eless Cu process (Fig. 4.28) with some modified parameters are used for this study. As shown in Fig. 4.29, the surface roughness of the new ABF is smoother than that of the old ABF, which will be beneficial to the fine metal line width/spacing formation on top of the ABF.

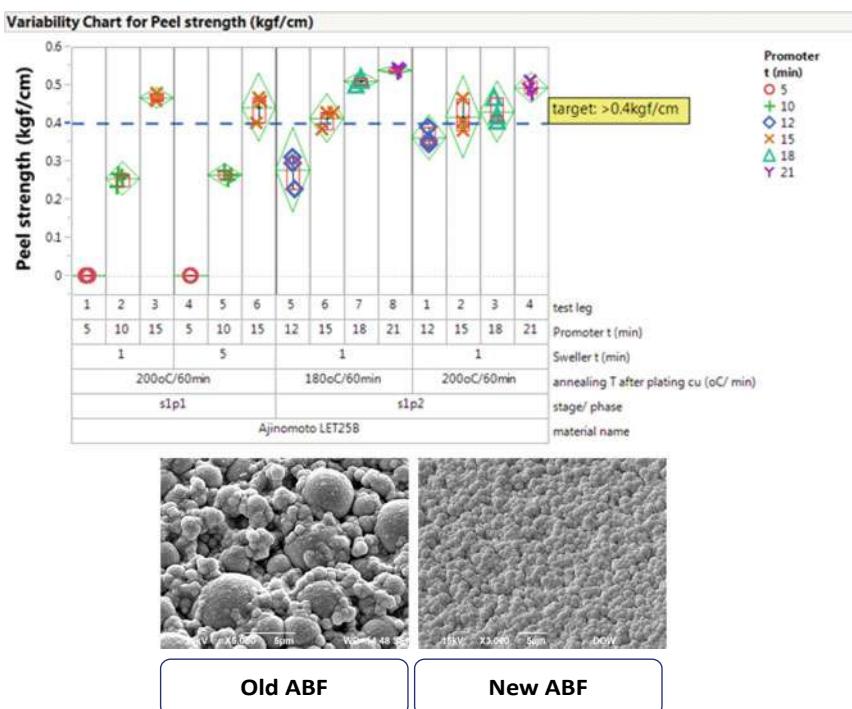
Peel strength is the key on the build-up metallization performance. It can be related to surface roughness (Ra) after de-smear process. There are three modified prominent factors: swelller dwell time, promoter dwell time and annealing time. After a detailed design of experiment performed by DOW, the peel strength results are shown in Fig. 4.30. It shows that 180 °C annealing time with higher than 12-min promoter dwell time leads to better performance—the peel strength is higher than 0.4kgf/cm<sup>2</sup>. Consequently, with the better performance on peel strength, the



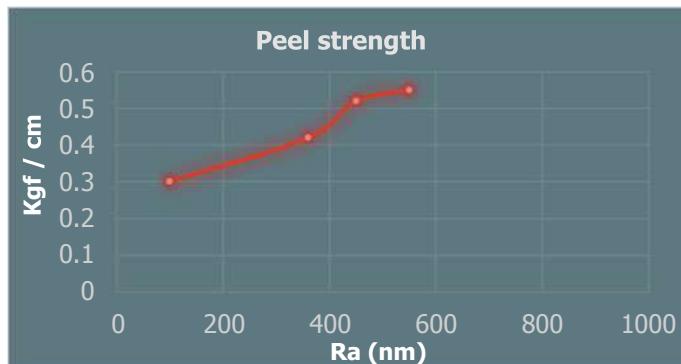
**Fig. 4.27** CIRCOPIST 7800 de-smear process



**Fig. 4.28** CIRCUPOSIT ADV 8500 Eless Cu process



**Fig. 4.29** Surface roughness: old ABF versus new ABF



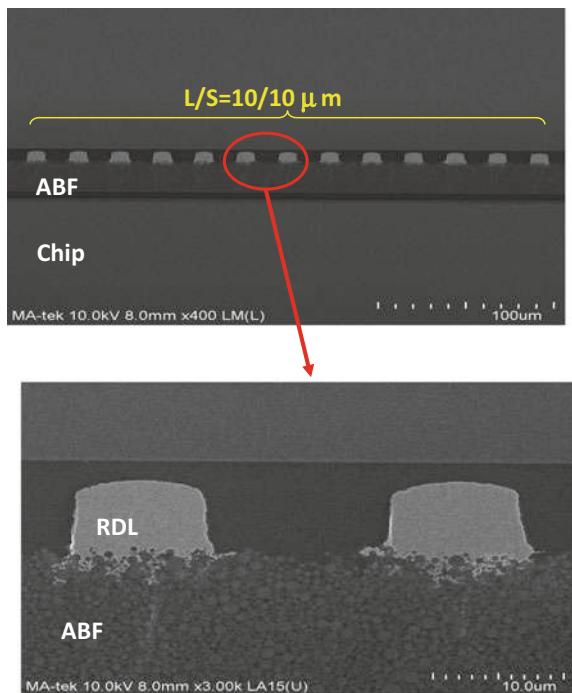
**Fig. 4.30** Peel strength results

new condition is selected for subsequent development in this study. The average thickness of electroless-Cu film is  $0.65 \mu\text{m}$ .

#### 4.3.6 LDI and PCB Cu-Plating

After electroless-Cu on both sides of the chips, laminate a new photoresist dry film with a thickness of  $12 \mu\text{m}$  on both sides of the Uni-SIP structure. It is followed by LDI photolithographic process and dry-film development. The LDI is with a positioning accuracy of  $\pm 5 \mu\text{m}$ . The wavelength of the UV laser is  $365 \text{ nm}$  and the exposure energy is  $200 \text{ mJ/cm}^2$ . Cu plating is carried out using an electrolyte containing  $240 \text{ g/L}$  of  $\text{CuSO}_4$  and  $60 \text{ g/L}$  of  $\text{H}_2\text{SO}_4$ . The Cu film is plated at a constant current density of  $2.0 \text{ ASD}$ . After metallization, these fine traces are formed on the ABF dielectric according to the pre-defined photoresist pattern. Finally, the photoresist is stripped off and Cu seeding layer is etched to form the RDL1. The fabricated metal line width and spacing (on average) is  $10 \mu\text{m}$  according to the top-view measurements of the cross section shown in Fig. 4.31. Repeat all the processes to get RDL2. Figure 4.32 shows the images of the heterogeneous integration package of 4 chips. It can be seen that the gap between the large chip ( $5 \text{ mm} \times 5 \text{ mm}$ ) and the small chip ( $3 \text{ mm} \times 3 \text{ mm}$ ) is  $100 \mu\text{m}$  and there is no void in the dry-film EMC.

Figure 4.33 shows the SiPs fabricated by the FOPLP chip-first and die face-down on a  $508 \text{ mm} \times 508 \text{ mm}$  panel. A cross section of the SiP PCB assembly is shown in the bottom of Fig. 4.33. It can be seen that the SiP has been properly fabricated.

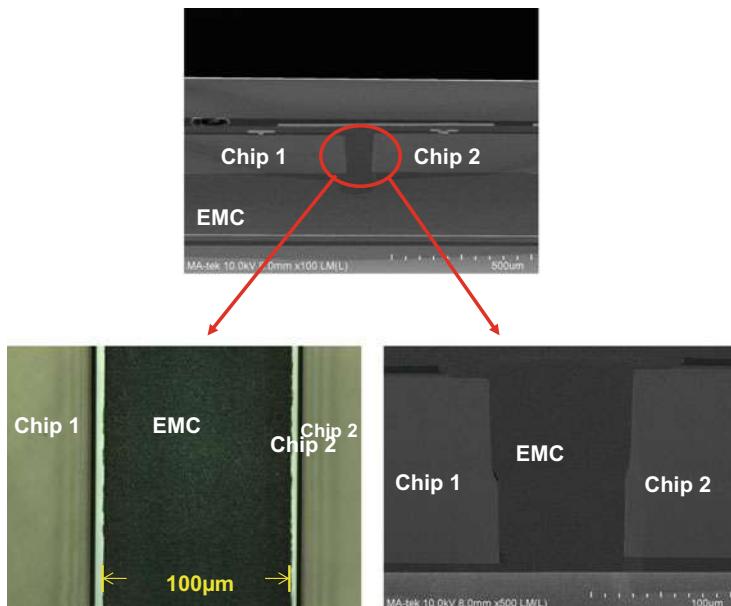


**Fig. 4.31** SEM images of the RDL1 ( $10 \mu\text{m}$  metal line width and spacing)

#### 4.3.7 Summary and Recommendation

The feasibility of design, materials, process, and fabrication of a thin heterogeneous integration of 4 chips by a FOPLP method has been demonstrated. Some important results and recommendations are summarized as follows [15].

- The  $10 \mu\text{m}$  RDL1 of the heterogeneous integration fan-out package has been successfully fabricated by an all PCB SAP and equipment.
- The lamination of a dry-film EMC has been successfully demonstrated on making the ECM-panel in a 2-stage vacuum lamination machine with the given important parameters.
- The lamination of the 5-layer (2 ECM-panel + core substrate) Uni-SIP structure has been successfully fabricated. The debonding of the temporary carriers and removing of the two-side tape have been successfully demonstrated.
- A new ABF with a CTE ( $15 \times 10^{-6}/^\circ\text{C}$ ) which is the same as the dry-film EMC and a very small filler size ( $5 \mu\text{m}$ ) has been selected.



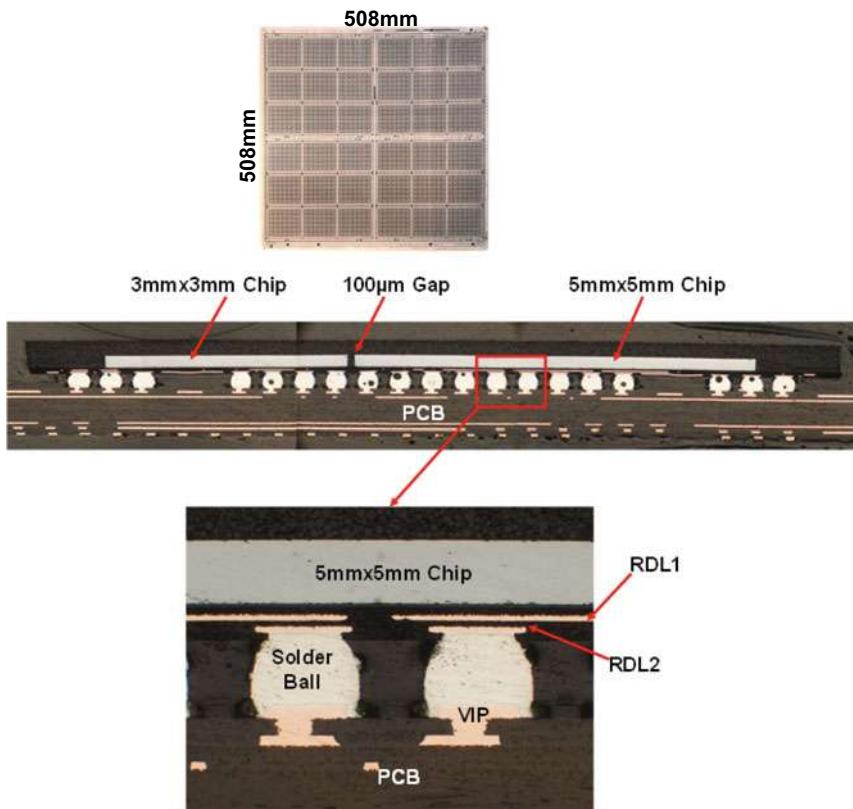
**Fig. 4.32** Images of the test package showing the 100  $\mu\text{m}$  gap between the large chip and small chip and there is no void in the dry-film EMC

- DOW's SAP solution—CIRCOPIST 7800 de-smear process and CIRCUPOSIT ADV 8500 E-less Cu process with some modified parameters have been successfully demonstrated with smooth ABF surface and outstanding peel strength results.
- The present LDI + PCB Cu-plating on fabricating the 10  $\mu\text{m}$  metal line width and spacing of RDL1 have been successfully demonstrated.

## 4.4 Fan-Out (Chip-First and Face-Up) Wafer-Level Packaging

### 4.4.1 Test Chip

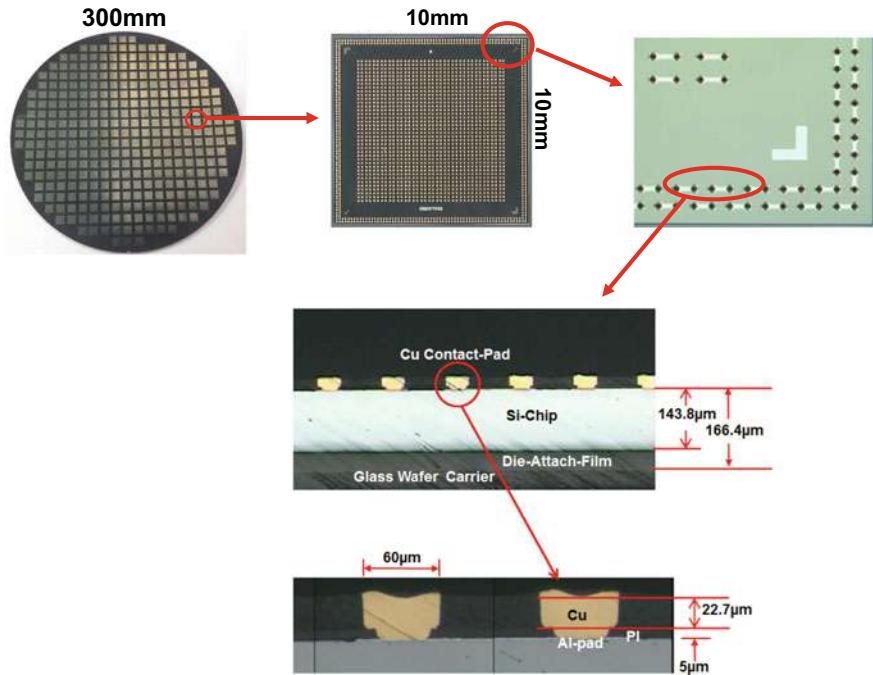
Figure 4.34 shows the test chip ( $10 \text{ mm} \times 10 \text{ mm}$ ) for a fan-out (chip-first and face-up) packaging. It can be seen that a Cu contact-pad (or stud) has been plated up from the Al-pad of the chip.



**Fig. 4.33** (Top) 508 mm × 508 mm panel with SiPs. (Bottom) Cross section view of the SiP assembly

#### 4.4.2 Process Flow

The key process flow in fabricating the fan-out (chip-first and face-up) package is shown in Fig. 4.35 and the cross section of the package is shown in Fig. 4.36. It can be seen that there are three RDLs with the minimum metal linewidth and spacing equal to 5  $\mu\text{m}$ . The design, materials, process, fabrication, and reliability of this package have been reported in [83–86] and will not be elaborated herein.



**Fig. 4.34** Test chip. (Top) Fabricated and close-up look of the test chip. (Bottom) Cross-sectional image of the test chip

## 4.5 Fan-Out (Chip-First and Face-up) Panel-Level Packaging

### 4.5.1 The Structure

For high-volume and low-density applications such as the PMIC (power management integrated circuits), Deca's M-Series [80] as shown in Fig. 4.37 by using a temporary panel carrier can reduce cost. M-Series is a chip-first and die face-up process.

### 4.5.2 Process Flow

Deca's M-Series process flow is reported in [80] and is shown in Fig. 4.38. It can be seen that the KGD is picked and placed face-up on a temporary carrier and then molded over the top in a continuous layer to fully encapsulate and encase the KGD. Cu pillars are electroplated on the device wafer to provide interconnect between the chip and fan-out RDL as shown in Fig. 4.37. This fully molded structure provides

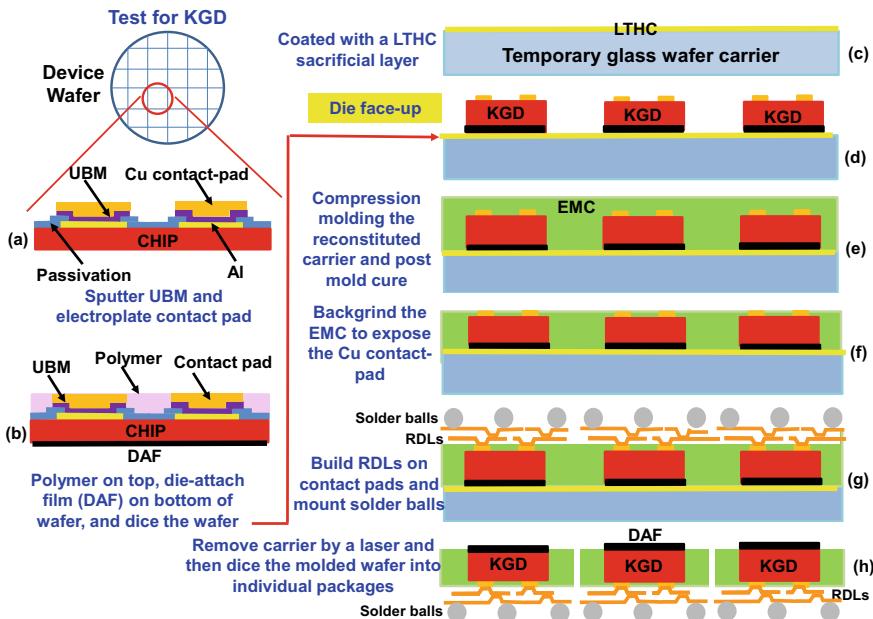
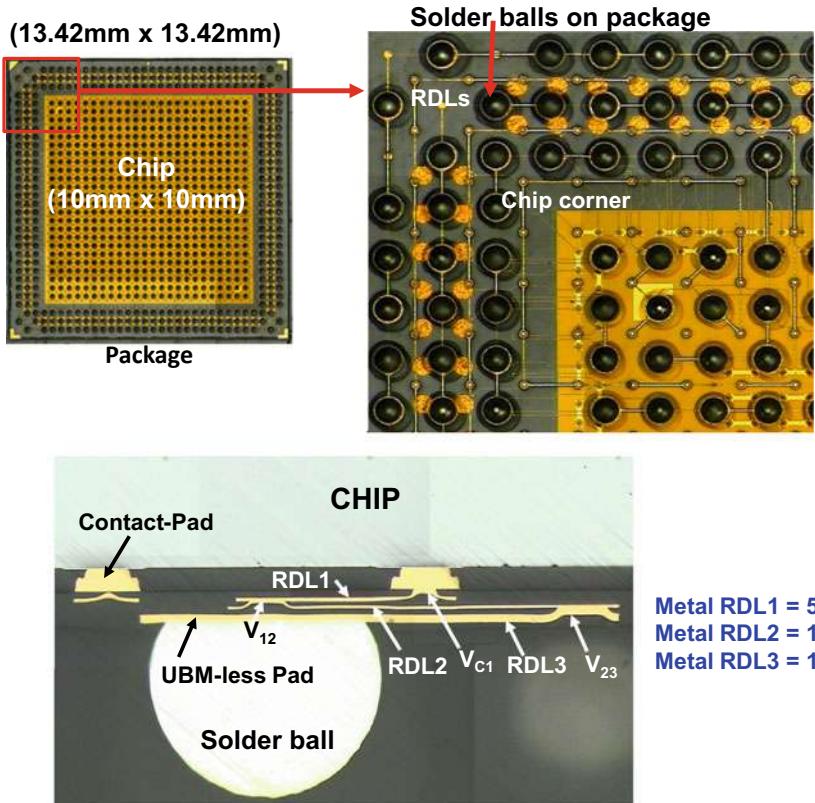


Fig. 4.35 Key process steps of the chip-first (die face-up) fan-out packaging

better mechanical protection for the dielectric layer in the front-side of the chip and provides an additional buffer layer between the KGD and the RDLs. A typical SEM of the cross section of the M-Series fan-out with chip-first and die face-up package is shown in Fig. 4.39 [80].

## 4.6 Fan-Out (Chip-Last or RDL-First) Wafer-Level Packaging

Since 2006, NEC Electronics Corporation (now Renesas Electronics Corporation) has been developing a novel SMArt chip connection with feed through interposer (SMAFTI) packaging technology for inter chip wideband data transfer [95, 96], 3-D stacked memory integrated on logic devices [97–101], system-in wafer-level package (SiWLP) [102], and redistribution-layer (RDL)-first (or chip-last) fan-out wafer-level packaging [103]. The feed through interposer (FTI) used in SMAFTI is a film with ultrafine linewidth and spacing RDLs. The dielectric of the FTI is usually SiO<sub>2</sub> or a polymer, and the conductor wiring of the RDL is Cu. The FTI not only supports the RDL underneath within the chip but it also provides support beyond the edges of the chip. Area array solder balls are mounted at the bottom side of the FTI, which are to be connected to the printed circuit board (PCB). Epoxy molding

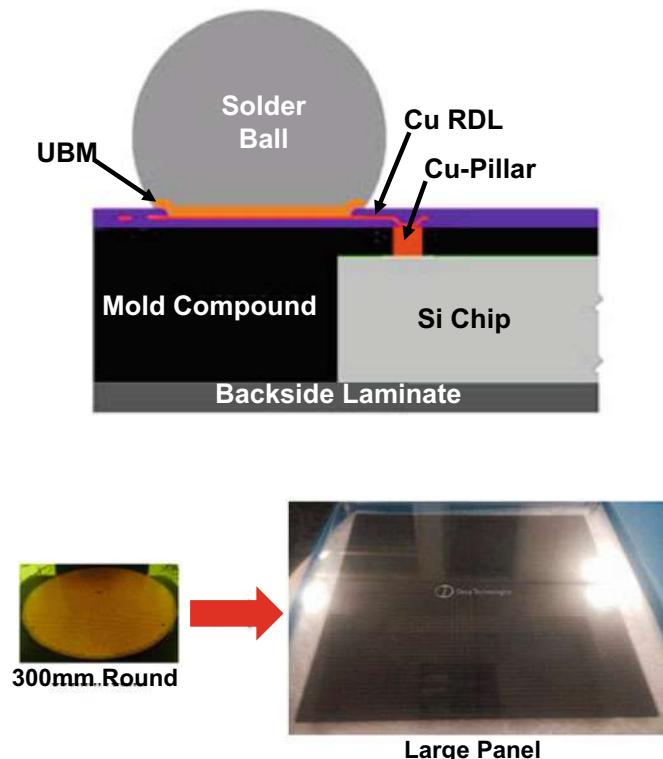


**Fig. 4.36** (Top) Fabricated and close-up look of the chip-first (die face-up) fan-out package. (Bottom) Cross-sectional image of the test package

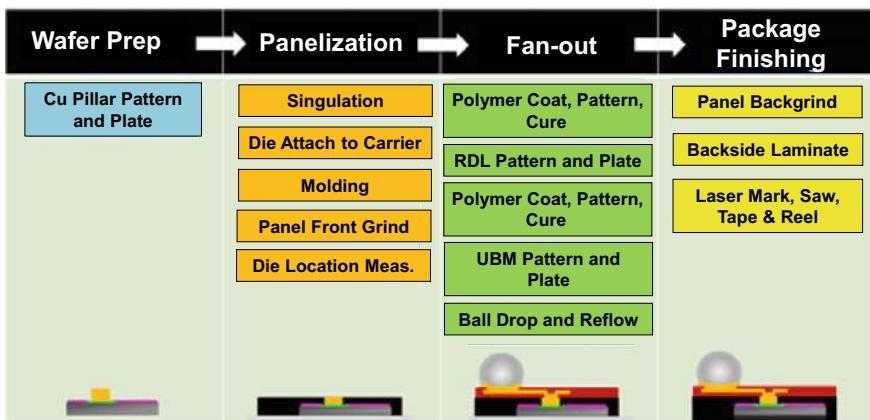
compound (EMC) is used to embed the chip and support the RDL and solder balls [11, 104].

One of the key reasons for the RDL-first (or chip-last) [11, 104] is trying to prevent the loss of the embedded known good die (KGD) during the RDL fabrication of the chip-first process [11]. This is true only if the RDL-first substrate for chip-last [11, 104] can be fully functionally tested at speed before other process steps, such as chip-to-substrate bonding, underfilling, and EMC molding; otherwise, the KGD still have to be thrown away for the case of a not good (NG) RDL-first substrate after a system test. Comparing with the chip-first process, the chip-last process is more complex and higher cost [11, 104]. Besides making the RDL, chip-last also must perform the wafer bumping, chip-to-wafer or panel substrate bonding, and underfilling (or molded underfill.) Thus, in general, RDL-first is meant for high-density fan-out wafer or panel-level packaging (HD FOWLP) or (HD FOPLP).

Since 2015, Amkor has been promoting a very similar RDL-first technology called silicon wafer integrated fan-out technology (SWIFT) [106]. Since 2015, the Institute

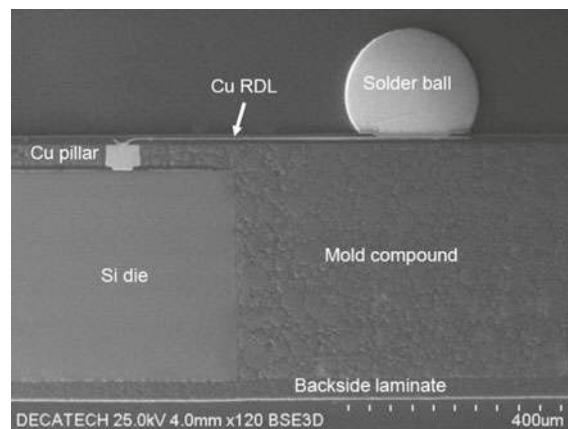


**Fig. 4.37** (Top) M-series chip-first (die face-up) fan-out package. (Bottom) Temporary panel carrier [80]



**Fig. 4.38** M-series process flow

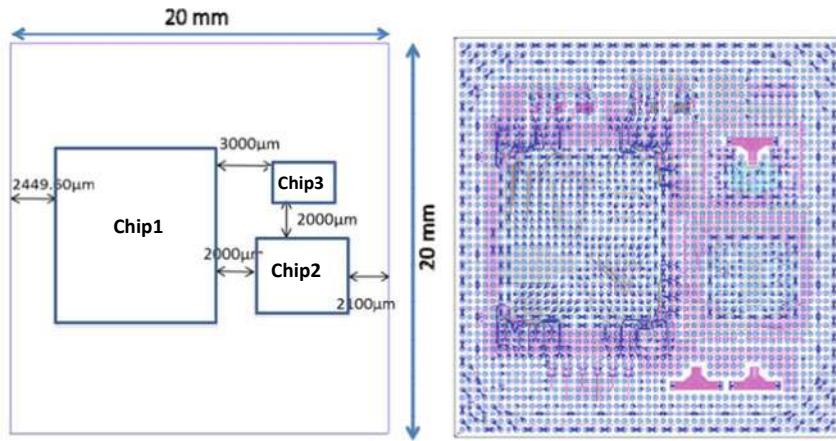
**Fig. 4.39** Cross-sectional image of M-series fan-out package



of Microelectronics (IME) has been publishing a series of research and development papers on chip-last or RDL-first FOWLP and FOPLP [107–116]. In 2016, SPIL demonstrated the first hybrid integration of the fine line plasma-enhanced chemical vapor deposition (PECVD) RDL with  $\text{SiO}_2$  and the RDL with polymeric dielectrics [117]. In 2017, Amkor published a very similar hybrid RDL for its silicon-less integrated module (SLIM) [118, 119]. Also, in 2017, Unimicron published a paper on RDL-first with the minimum linewidth of  $8\ \mu\text{m}$  on a panel size of  $370\ \text{mm} \times 470\ \text{mm}$  [120]. In 2018, Samsung published two papers on using RDL-first to make Si-less RDL for high-performance computing (HPC) applications [121], and system-in-package (SiP) side-by-side (SbS) for advanced mobile applications [122]. Since 2018, ITRI has been publishing research and development papers in RDL-first FOWLP and FOPLP [123–125]. In 2019, ASE used RDL-first for its fan-out chip on substrate (FOCoS) [126], and TSMC used RDL-first to make the RDL-interposer for its high-density heterogeneous large package [127]. Also, in 2019 and 2020, Shinko [128, 129] used RDL-first to make high density organic package substrate, and in 2020 Unimicron published papers [130, 131] on RDL-first with the minimum metal linewidth of  $2\ \mu\text{m}$  on a panel size of  $510\ \text{mm} \times 515\ \text{mm}$ . As of this writing, none of the abovementioned RDL-first FOWLP and FOPLP are in high-volume manufacturing.

#### 4.6.1 IME's RDL-First FOWLP

IME has been publishing many papers on fan-out with chip-last or RDL-first process [107–116]. In this section, IME's chip-last on a round (wafer) temporary carrier will be briefly mentioned.



**Fig. 4.40** Multi-chip FOWLP layout. **a** Chip arrangement layout. **b** Daisy chain and package level bump layout [109]

#### 4.6.2 Test Structure

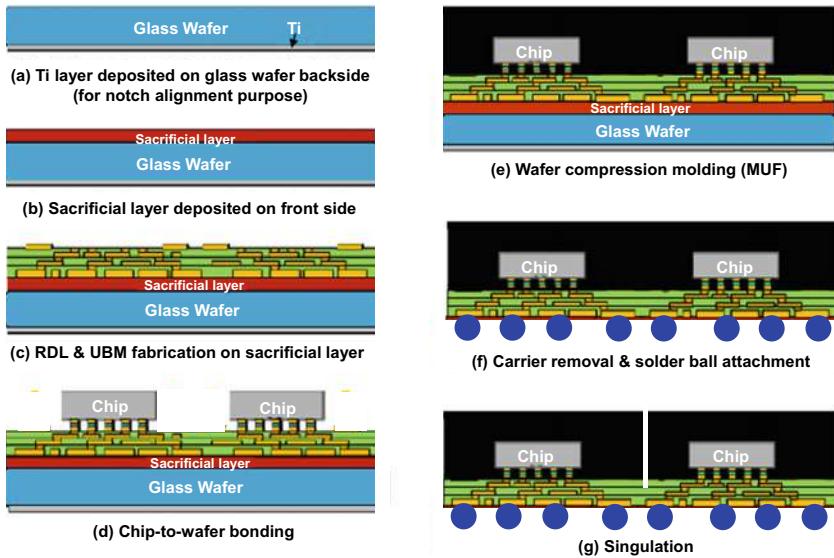
The test structure is shown in Fig. 4.40. It can be seen that there are three test chips: 9.0 × 8.0, 5.0 × 4.0 and 3.0 × 2.0 mm<sup>2</sup>. The bump pitches of the test chips are, respectively 120 μm, 80 μm and 60 μm. The test package size is 20 × 20 mm<sup>2</sup> and there are three RDLs with the metal linewidth and spacing (L/S) are 2 μm/2 μm, 5 μm/5 μm and 10 μm/10 μm respectively. There are about 2400 solder bumps at 400 μm pitch.

#### 4.6.3 RDL-First Key Process Steps

The key process flow for making the fan-out RDL-first package is shown in Fig. 4.41. It can be seen that the temporary carrier is a glass wafer and a laser release material as the sacrificial layer. The fabrication process starts with Ti layer (physical vapor deposition) on the backside of the glass carrier wafer to make the glass wafer surface opaque for handling systems of subsequent processing tools. The sacrificial release layer is coated on the front side of the temporary carrier. Second, the formation of UBM and multi-layer RDL with LS of 10/10, 5/5 and 2/2 μm on the temporary carrier with sacrificial release layer.

In parallel, wafer micro bumping of the device wafer with the standard PVD and ECD Cu and solder process is performed. Then, dice the wafers into individual chips with micro bumps.

Third, the device chips with micro bumps are bonded to the multi-layer RDL film on the temporary carrier using chip-on-wafer (CoW) bonding. The gaps between the



**Fig. 4.41** RDL-First FOWLP fabrication integration flow [109]

chip and the RDL film are filled using capillary underfilling. Fourthly, compression wafer level molding to encapsulate the test chips.

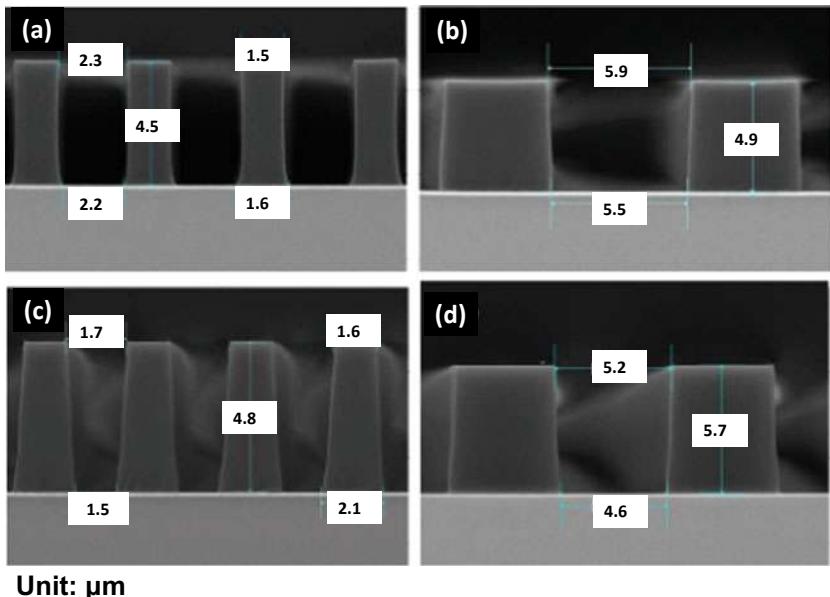
Finally, the temporary carrier is de-bonded and the sacrificial layer material is cleaned to expose the UBM for solder ball mounting. In this integration flow, molding is the last process, therefore it can eliminate die shift and die protrusion and wafer warpage issues during the RDL fabrication, and allows the fabrication of fine pitch RDLs on the temporary carrier.

Figure 4.42 shows the effects of photoresists (PRA and PRB) on the metal L/S of 2/2  $\mu\text{m}$  and 5/5  $\mu\text{m}$  RDLs. It can be seen that the side walls of PRA (Figs. 4.42a, b) are near vertical than those of PRB (Figs. 4.42c, d).

Figure 4.43 shows the effects of photo-dielectrics (PIA and PIB) on the via profile of the RDLs. Both dielectric materials are cured at 200 °C for 1 h and able to open small size vias of 3 and 5  $\mu\text{m}$  diameters with near vertical side-wall profiles as shown in Fig. 4.43.

#### 4.6.4 RDL-First FOWLP on PCB Assembly

The complete integration of RDL-First FOWLP on PCB assembly is shown in Fig. 4.44. It can be seen that all three RDLs are properly done. Also, the chip-to-wafer bonding and the solder joints look very good.



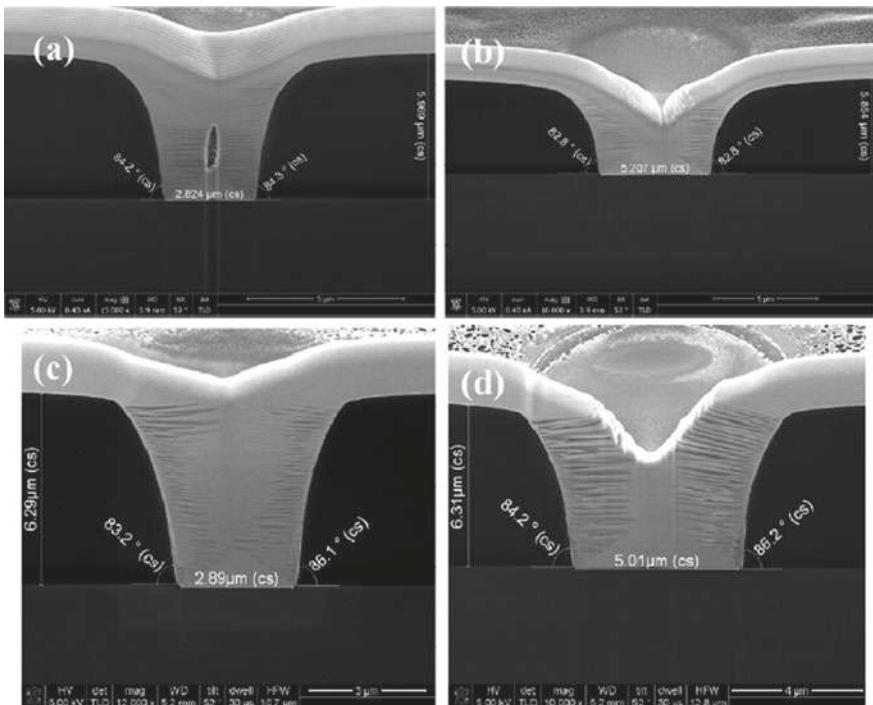
**Fig. 4.42** Cross-section of fine pitch RDL PR patterns profile: **a** and **b** PR material A—RDL patterns of L/S of 2  $\mu\text{m}$ /2  $\mu\text{m}$  and 5  $\mu\text{m}$ /5  $\mu\text{m}$  respectively, **c** and **d** PR material B—RDL patterns of L/S of 2  $\mu\text{m}$ /2  $\mu\text{m}$  and 5  $\mu\text{m}$ /5  $\mu\text{m}$  respectively [109]

## 4.7 Fan-Out (Chip-Last or RDL-First) Panel-Level Packaging

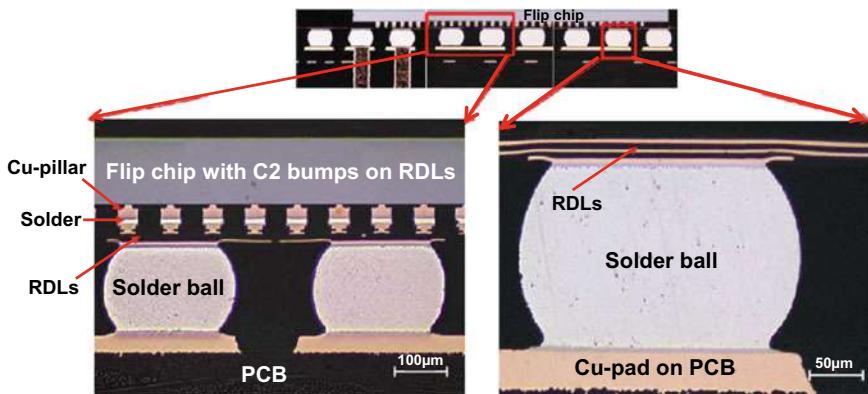
In this section, the materials, process, fabrication, and reliability of the heterogeneous integration of three chips (one large and two small) on a three-layer RDL substrate (with the minimum L/S of the metal layers (MLs) equal to 2/2  $\mu\text{m}$ ) fabricated on a 515  $\times$  510-mm<sup>2</sup> panel are presented [130, 131]. The physical meaning of this structure could be for an application processor chipset; the large chip could be the processor and the smaller chips could be the memories.

### 4.7.1 Test Chips

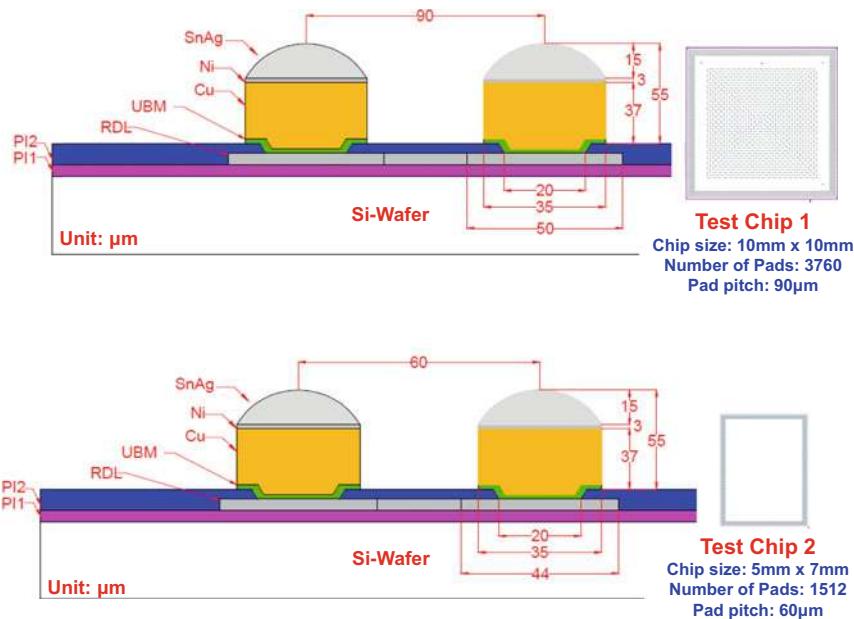
The test chips are shown in Fig. 4.45. The dimensions of the large chip (chip 1) are 10  $\times$  10 mm<sup>2</sup> and of the small chip (chip 2) are 7  $\times$  5 mm<sup>2</sup>. It can be seen that there are 3,760 pads on 90-mm pitch for the large chip and 1,512 pads on 60-mm pitch for the small chip. The micro bump of both chips is the same: (1) the diameter and height of the Cu pillar are, respectively, 35  $\mu\text{m}$  and 37  $\mu\text{m}$ , (2) the Ni barrier layer is 3  $\mu\text{m}$ , and (3) the SnAg solder cap is 15  $\mu\text{m}$ .



**Fig. 4.43** Cross-section of dielectric via profile: **a** and **b** Dielectric material A—via opening of 3  $\mu\text{m}$  and 5  $\mu\text{m}$  diameter respectively, **c** and **d** Dielectric material B—via opening of 3  $\mu\text{m}$  and 5  $\mu\text{m}$  diameter respectively [109]



**Fig. 4.44** Cross-section of assembled FOWLP on PCB [109]

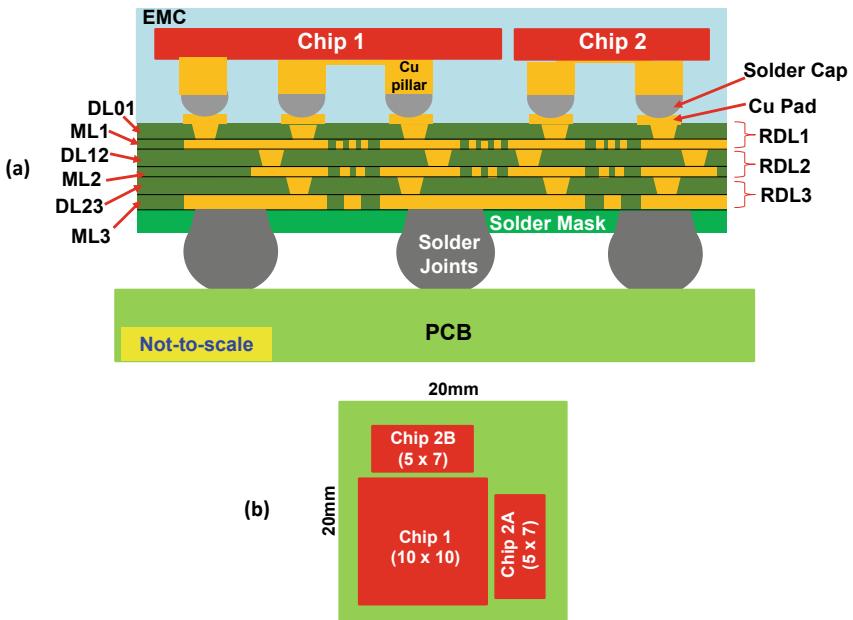


**Fig. 4.45** Cross section of test chips

#### 4.7.2 Test Package

The cross section view and top view of the test package are shown in Fig. 4.46. It can be seen that there are three chips (one large and two small) on a  $20 \times 20\text{-mm}^2$  substrate. The substrate consists of three RDLs and the L/S of the first metal layer (ML1) of RDL1 are  $2/2\text{ }\mu\text{m}$ , of the second metal layer (ML2) of RDL2 are  $5/5\text{ }\mu\text{m}$ , and of the third metal layer (ML3) of RDL3 are  $10/10\text{ }\mu\text{m}$ . The thickness of ML1, ML2, and ML3 are, respectively, 2.5, 2.5, and 8  $\mu\text{m}$ . The thickness of the dielectric layers (DLs) DL01 (DL between the Cu pad and ML1), DL12 (DL between ML1 and ML2), and DL23 (DL between ML2 and ML3) are, respectively, 5, 6.5, and 6.5  $\mu\text{m}$  as shown in Fig. 4.47a. The solder resist (mask) opening and thickness are, respectively, 245  $\mu\text{m}$  and 5  $\mu\text{m}$ .

The top side of the RDL substrate for those three chips is shown in Fig. 4.47b and its bottom side for the solder balls on the PCB is shown in Fig. 4.47c. It can be seen that there are 6,784 pads with 90 and 60- $\mu\text{m}$  pitches on the top side and 2,780 pads with 0.35-mm pitch on the bottom side. The  $20 \times 20\text{-mm}^2$ -RDL substrate is fabricated on a large temporary glass panel with dimensions of  $515 \times 510\text{ mm}^2$  as shown in Fig. 4.48. It can be seen that, at one shot, 396 ( $20 \times 20\text{ mm}^2$ ) RDL substrates can be made. After the RDL substrate fabrication is completed, the panel is then cut into 12 strips ( $240 \times 74\text{ mm}^2$ ) and each strip is with 33 ( $20 \times 20\text{ mm}^2$ ) package substrates. All the remaining assembly and process steps are performed on the strip.



**Fig. 4.46** Test package ( $20\text{ mm} \times 20\text{ mm}$ ). **a** Cross-sectional view. **b** Top view

### 4.7.3 RDL-First Panel-Level Packaging for Heterogeneous Integration

The key process flow steps for fabricating the RDL-first substrate, surface finishing, chip-to-substrate bonding, underfilling, epoxy molding compound (EMC) molding, solder resist opening (SRO) and solder ball mounting, and dicing are shown in Figs. 4.49a, b. Comparing with those process steps in making the RDL substrate in Figs. 4.6a, b of [130], it can be seen that they are very different. The key difference is that in [130], the RDLs are built from the  $2/2\text{ }\mu\text{m}$  metal L/S, whereas in this study, the RDLs are going to be built from the  $10/10\text{ }\mu\text{m}$  metal L/S. Consequently, the vias connecting the MLs are different. Also, there is no need to transfer the RDL substrate to another temporary carrier before the chip-to-substrate bonding.

### 4.7.4 Fabrication of Redistribution-Layer Substrate

First, a released film (sacrificial layer) is slit coated on a temporary glass carrier ( $515 \times 510\text{ mm}^2$ ) and it is followed by slit coating a photoimageable dielectric (PID) for the solder mask (or passivation layer) DL3B as shown in Fig. 4.49a. Then, a Ti/Cu seed layer is formed by physical vapor deposition. It is followed by photoresist, laser

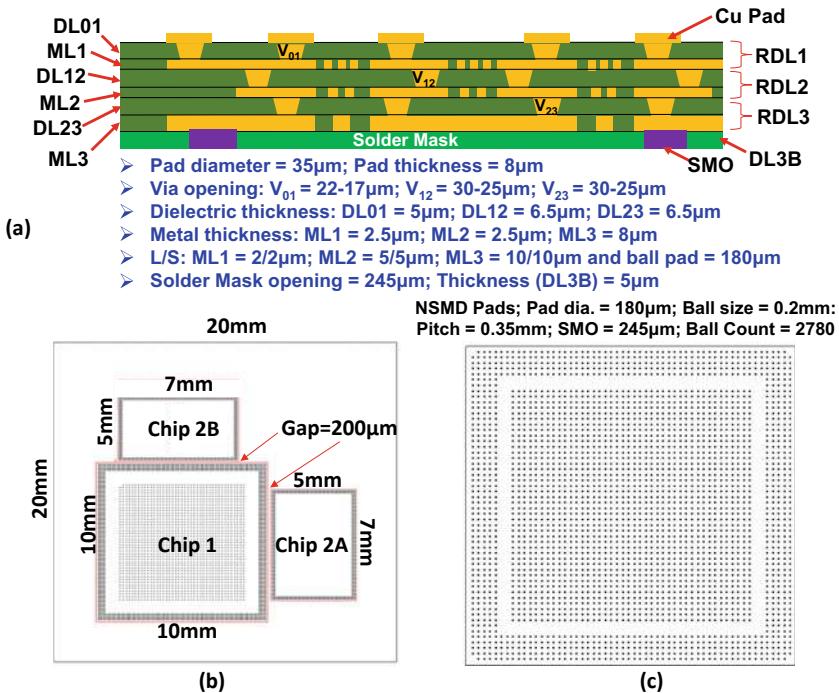


Fig. 4.47 a Three-layer RDL-first substrate. b Top view. c Bottom view

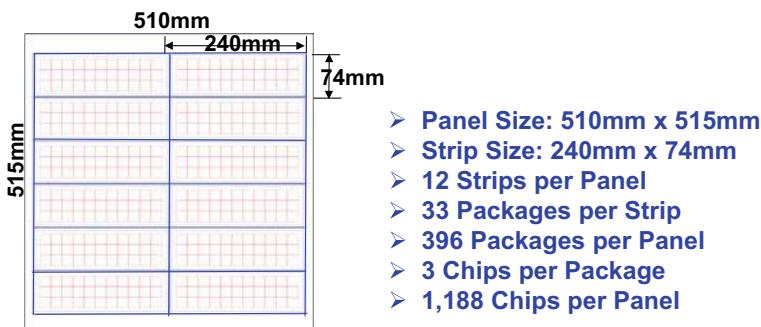
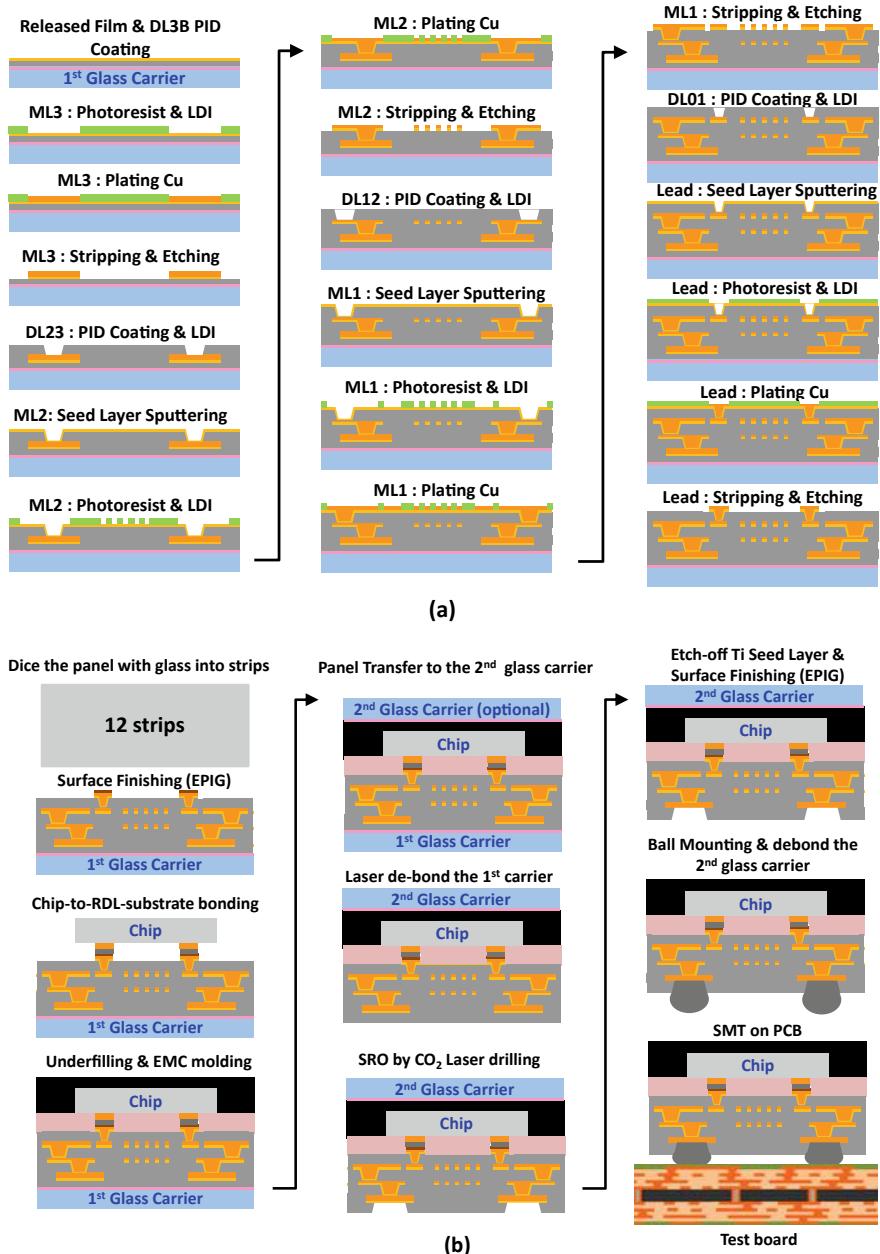


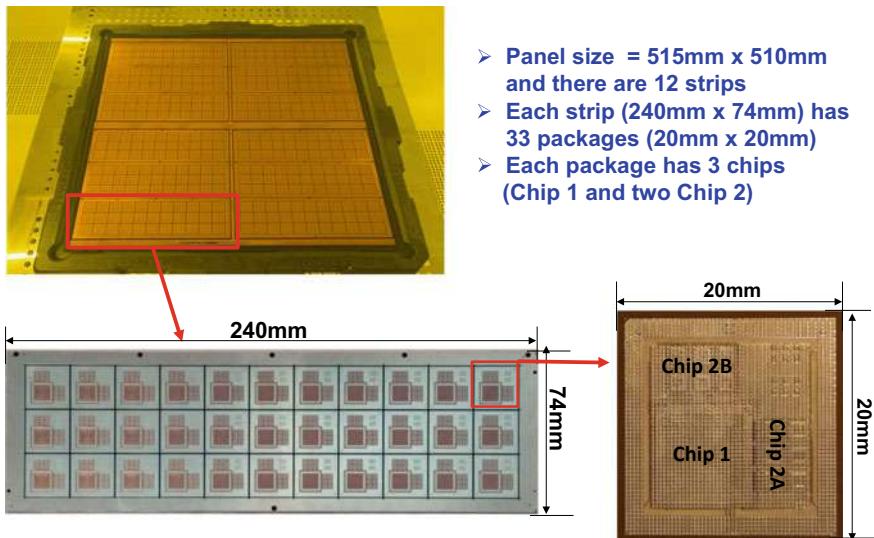
Fig. 4.48 Panel (515 mm × 510 mm) for making the RDL-first substrate

direct imaging (LDI), and development. Then, electrochemical deposition (ECD) Cu and strip off the photoresist and etch off the Ti/Cu to obtain the 10/10 µm ML (ML3) of RDL3.

It is followed by slit coating a PID and LDI to get the DL (DL23) of RDL3. Then, sputter the Ti/Cu seed layer, slit coat the photoresist, LDI and develop, and ECD the Cu. It is followed by stripping off the photoresist and etching off the TiCu seed layer



**Fig. 4.49** **a** Process flow of the fan-out RDL-first panel-level package. **b** Process flow of the fan-out RDL-first panel-level packaging (continue)

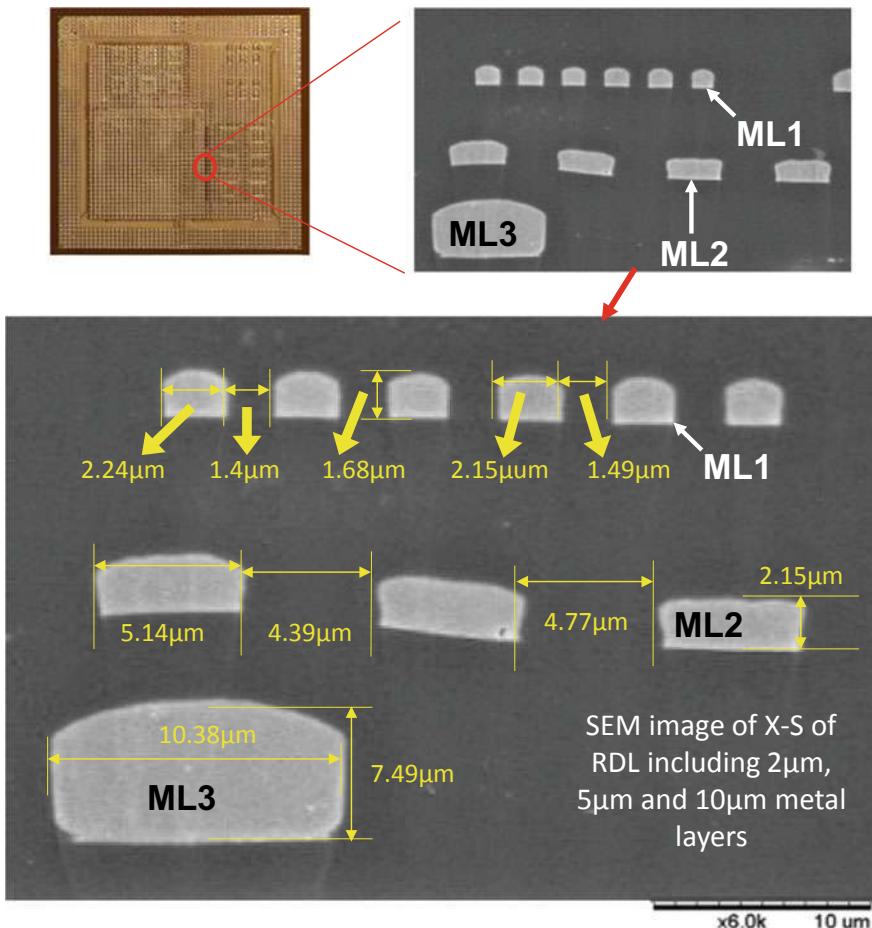


**Fig. 4.50** Fabricated three-layer RDL-first substrate on a 515 mm × 510 mm glass panel carrier

to get the  $5/5 \mu\text{m}$  ML (ML2) of RDL2. It is followed by slit coating a PID and LDI to get the DL (DL12) of RDL2. Repeat the same process steps to obtain the  $2/2 \mu\text{m}$  ML (ML1) and DL (DL01) of RDL1. Then, sputter the Ti/Cu, slit coat the photoresist, LDI and develop, and ECD the Cu. It is followed by stripping off the photoresist and etching off the TiCu to get the bonding pad (lead) for the chips, which is shown in the last step of Fig. 4.49a.

Next, the glass panel ( $515 \times 510 \text{ mm}^2$ ) with the fabricated 396 three-layer RDL substrates is cut into 12 strips. The dimensions of each strip are  $240 \times 74 \text{ mm}^2$ , and each strip has 33 ( $20 \times 20 \text{ mm}^2$ ) RDL substrates. Figure 4.50 shows the panel, the strip, and the individual RDL substrate.

Figure 4.51 shows the SEM images of a typical cross section of the RDL substrate. This cross section is showing (including) all three MLs (ML1, ML2, and ML3) of RDL1, RDL2, and RDL3. A closer look at the bottom SEM image, it can be seen that for RDL1, the linewidth does not meet the  $2-\mu\text{m}$  target but equals  $2.15 \mu\text{m}$ ,  $2.24 \mu\text{m}$ ..., the line spacing does not meet the  $2-\mu\text{m}$  target but equals  $1.4 \mu\text{m}$ ,  $1.49 \mu\text{m}$ ..., and the thickness also does not meet the  $2.5 \mu\text{m}$  target but equals  $1.68 \mu\text{m}$ ... Thus, there are rooms for improvements (such as use better PIDs, higher resolution LDI or a stepper). The linewidth, spacing, and thickness of ML2 are much better, and they are, respectively,  $5.14$ ,  $4.77$ , and  $2.15 \mu\text{m}$ , and the targets are  $5$ ,  $5$ , and  $2.5 \mu\text{m}$ . The linewidth and thickness of ML3 are, respectively,  $10.38 \mu\text{m}$  and  $7.49 \mu\text{m}$ , which are very close to the target values of  $10$  and  $8 \mu\text{m}$ . This is understandable because the smaller the L/S, the larger the error.

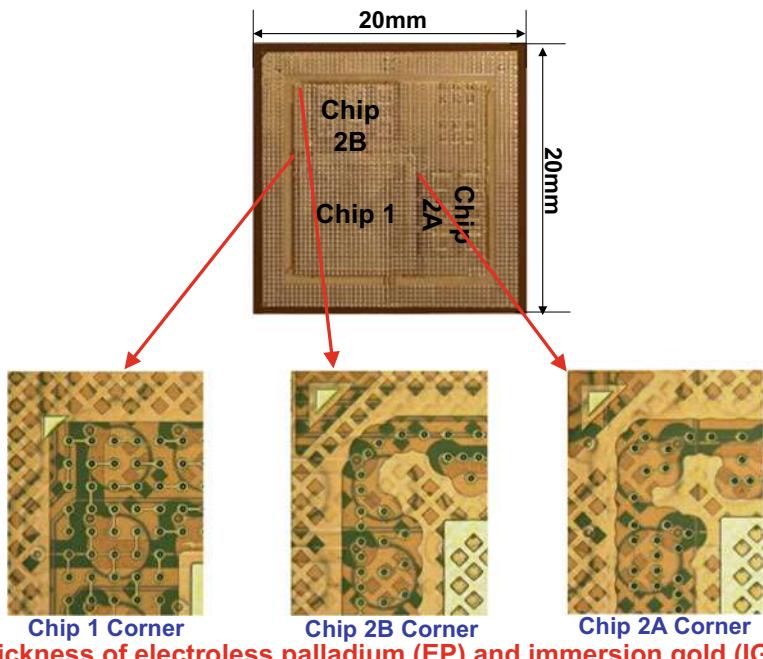


**Fig. 4.51** Cross-sectional view of the RDL-first substrate showing ML1–ML3

The last step on the fabrication of the RDL substrate right before the chips-to-substrate bonding is the surface finishing of the Cu bonding pads. In this study, electroless palladium and immersion gold (EPIG) surface finishing is used. Figure 4.52 shows the results at a few locations of the RDL substrate.

#### 4.7.5 Wafer Bumping

In parallel, the test wafers are bumped with the C2 (chip connection) bumps as shown in Fig. 4.45. After wafer bumping, the wafer is diced into individual chips. For all the bumped test chips, the bump consists of the Cu pillar, Ni barrier, and SnAg cap.



**The thickness of electroless palladium (EP) and immersion gold (IG) are  $0.027\mu\text{m}$  and  $0.054\mu\text{m}$ , respectively.**

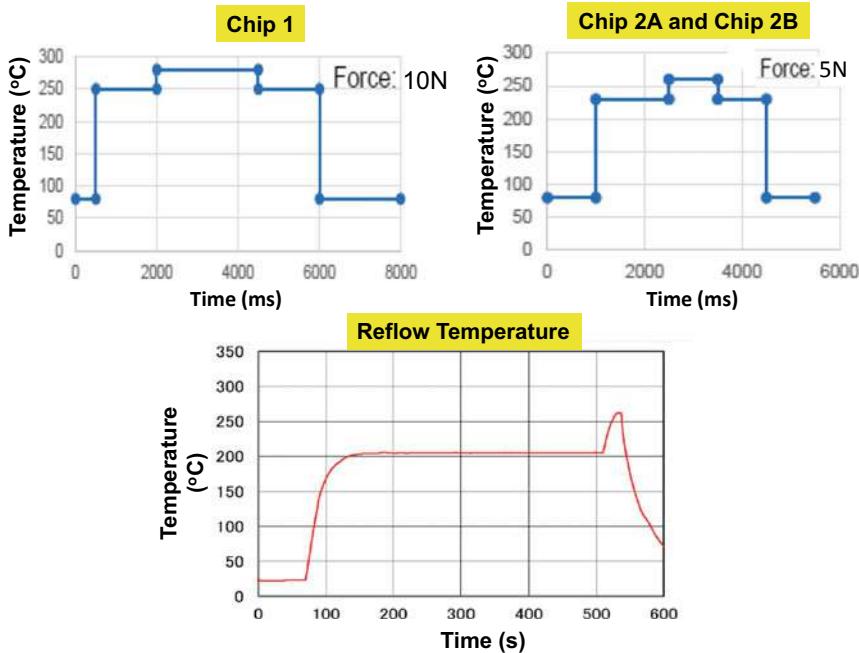
**Fig. 4.52** Surface finishing (EPIG) of the bonding pad (of the RDL-substrate) for the chips

#### 4.7.6 Chip-to-Substrate Bonding

Now, it is ready for chips-to-substrate bonding. Because of the support of the temporary glass carrier, the strip is very stiff and flat for bonding, Fig. 4.49b. Also, because the  $2/2-\mu\text{m}$  ML1 of RDL1 is facing upward, there is no need to transfer the RDL substrate strip to another temporary carrier before chip bonding. This is the biggest difference between the current process and the one from [130].

First, pick and place (P&P) all the chips on the strip, which is operated at room temperature. The P&P head condition for the large chip (chip 1) is shown in Fig. 4.53. It can be seen that the temperature rises very fast from  $75$  to  $250$   $^{\circ}\text{C}$  and then  $275$   $^{\circ}\text{C}$  and stays there for  $2.5$  s, then drops very fast to  $75$   $^{\circ}\text{C}$ . The applied force is small ( $10$  N). The P&P head condition for the small chips (chip 2A and chip 2B) is also shown in Fig. 4.53. It can be seen that the temperature rises very fast from  $75$  to  $225$   $^{\circ}\text{C}$  and then  $260$   $^{\circ}\text{C}$  and stay there for  $1$  s, then drops very fast to  $75$   $^{\circ}\text{C}$ . The applied force is very small ( $5$  N).

After the P&P of all the ( $3 \times 33 = 99$ ) chips on the RDL substrate, it is put into a reflow oven for a solder mass reflow of all the chips. The reflow temperature profile is shown in Fig. 4.53. It can be seen that the maximum temperature is  $250$   $^{\circ}\text{C}$  for the SnAg solder cap. Figure 4.54a shows a strip with  $33$  RDL substrates and

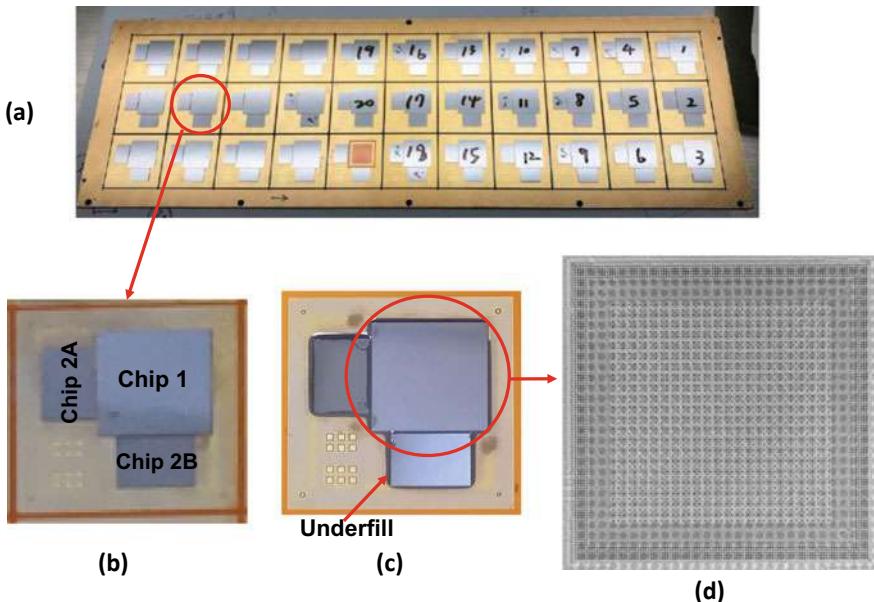


**Fig. 4.53** Chip-to-substrate (temperature vs. time) bonding conditions for the large chip and small chips. Solder mass reflow condition for all the chips

each with 3 chips as shown in Fig. 4.54b. Unlike the process in [1], the chip-to-substrate bonding is by thermocompression (one chip at a time); the current mass reflow process is very high throughout.

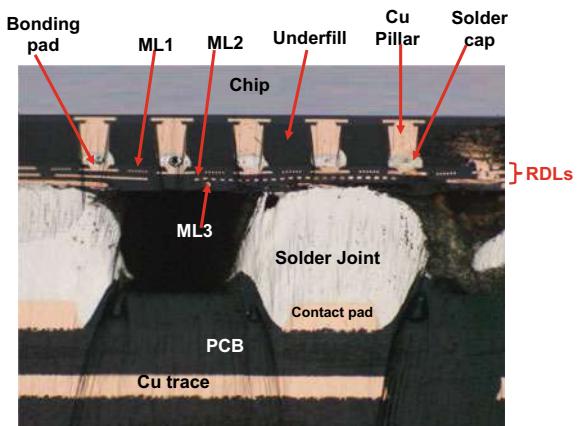
#### 4.7.7 Underfilling and EMC Molding

After chips-to-substrate strip bonding, it is time for underfill dispensing and curing as shown in Fig. 4.49b. The underfill curing condition is 165 °C for 2 h. A typical example is shown in Fig. 4.54c. After underfilling all the packages on the strip, the whole strip is laminated with an EMC (400  $\mu\text{m}$ -thick). The temperature and pressure conditions for the lamination are (1) first stage: 120 °C/vacuum for 30 s and press 5.68 MPa for 30 s and (2) second stage: 100 °C and press 5.58MPs for 60 s. Figure 4.54d shows the X-ray image of one of the large chips. Figures 4.55 and 4.56 show the cross sections of the chip bonded to the RDL substrate. The Cu pillar and solder cap of the chip, the underfill, and the ML1, ML2, and ML3 of the RDL substrate are clearly seen.



**Fig. 4.54** **a** A strip with 33 heterogeneous integration packages after mass reflow. **b** A close-up. **c** After underfill. **d** X-ray image of one of the large chip

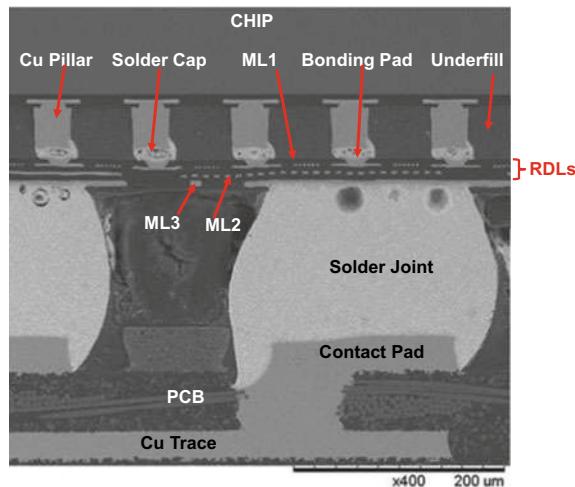
**Fig. 4.55** Cross section image showing the chip-to-RDL-substrate bonding, solder ball mounting, and then SMT reflow on a PCB



#### 4.7.8 Panel/Strip Transfer

Depending on the thickness of the EMC, the strip transfer is optional. If the EMC thickness is thick enough ( $>500 \mu\text{m}$ ), i.e., the stiffness of the strip with EMC embedded heterogeneous integration packages is strong enough to resist large ( $>1 \text{ mm}$ ) warpage after the original temporary glass carrier is removed, then there is

**Fig. 4.56** Cross section image showing the chip-to-RDL-substrate bonding, solder ball mounting, and then SMT reflow on a PCB

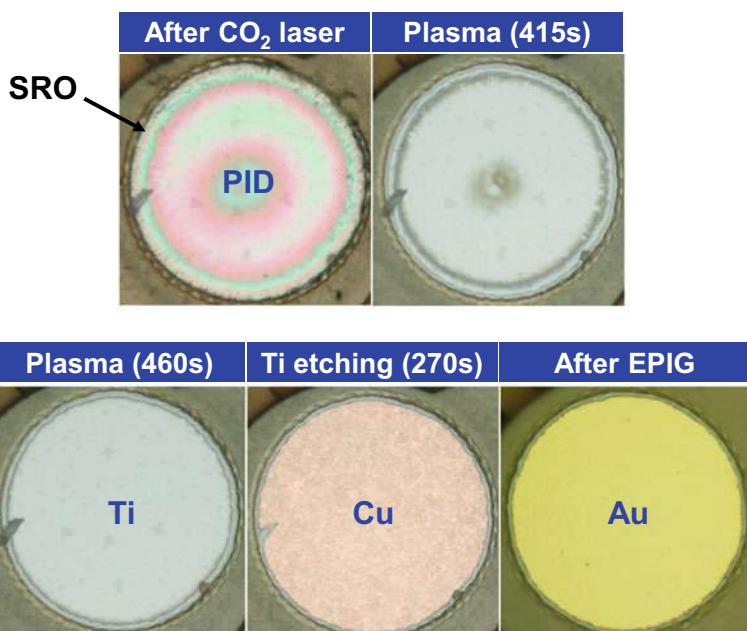
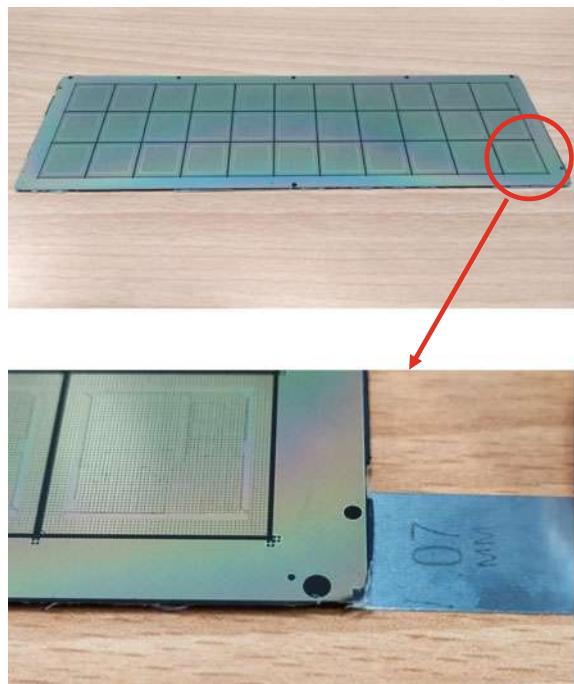


no need to transfer the strip to another temporary carrier. Otherwise, the strip transfer to another glass carrier is necessary for the remaining process steps such as solder ball mounting. In this study, the strip was transferred to another temporary glass carrier and then the original temporary glass carrier was removed so that we can make SRO and surface finishing on the Cu contact pads as shown in Fig. 4.49b. In this study, to save the EMC materials and have a lower profile heterogeneous integration package, the thickness of the EMC is only 400  $\mu\text{m}$ , thus the transfer of the strip to another temporary glass carrier is necessary. Figure 4.57 shows the case of strip transfer to another glass carrier and then remove the first temporary glass carrier. The maximum warpage is 0.7 mm.

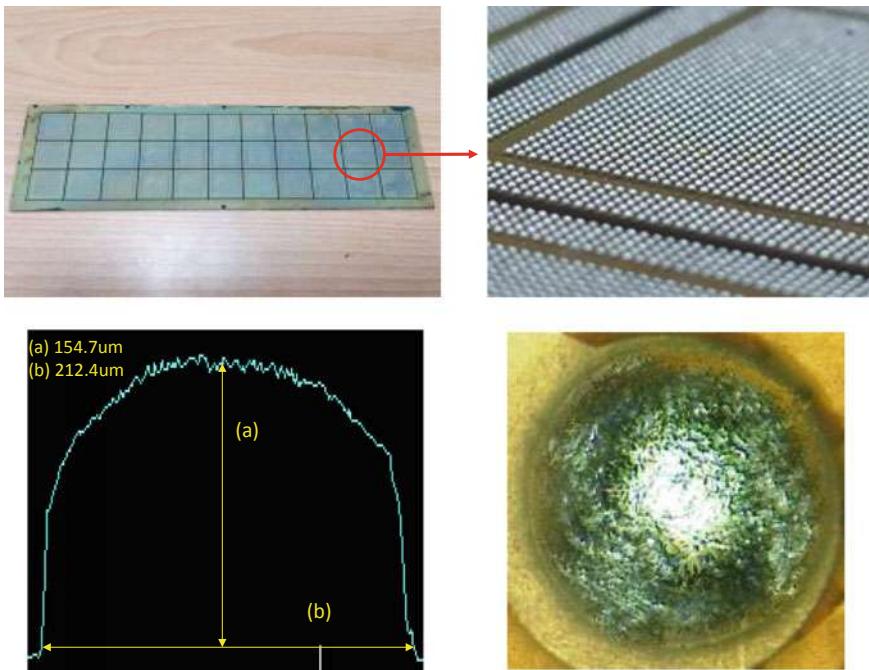
#### 4.7.9 Solder Resist Opening and Surface Finishing

After the removal of the first temporary glass carrier by a laser, it is time to make the SRO and surface finishing as shown in Fig. 4.49b. The 245  $\mu\text{m}$ -diameter SRO is made by a CO<sub>2</sub> laser with four times of pulse. Then, it is followed by plasma etching the PID for 460 s and chemical etching the Ti for 270 s as shown in Fig. 4.58. The surface finishing is by EPIG with the thickness of Pd and Au, respectively, equal to 0.056 and 0.069  $\mu\text{m}$ . The target values are 0.05  $\mu\text{m}$  for both Pd and Au.

**Fig. 4.57** After chip-to-substrate bonding, underfilling, and EMC molding, transfer the strip to another glass carrier and debond the original glass carrier



**Fig. 4.58** Solder resist opening, plasma etching, Ti etching, and EPIG surface finishing



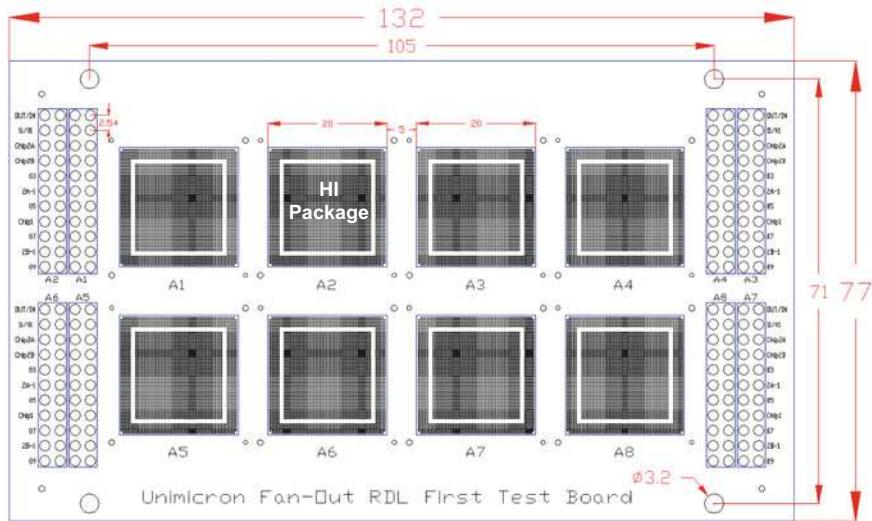
**Fig. 4.59** Solder ball mounting after strip transferred to another temporary glass carrier

#### 4.7.10 *Solder Ball Mounting, Debonding, and Strip Dicing*

After the SRO and EPIG surface finishing, it is time for solder ball mounting. Figure 4.59 shows the solder balls mounted on a strip (the average solder ball height equals to 154.7  $\mu\text{m}$ ) and the size of an individual solder ball. The alloy of the solder ball is Sn3Ag0.5Cu. After solder ball mounting, it is time to remove the second temporary glass carrier from the strip. Finally, the strip is diced into individual heterogeneous integration packages.

#### 4.7.11 *PCB Assembly of the RDL-First Panel-Level Package*

The reliability assessment of the present heterogeneous integration package is performed by the drop test.



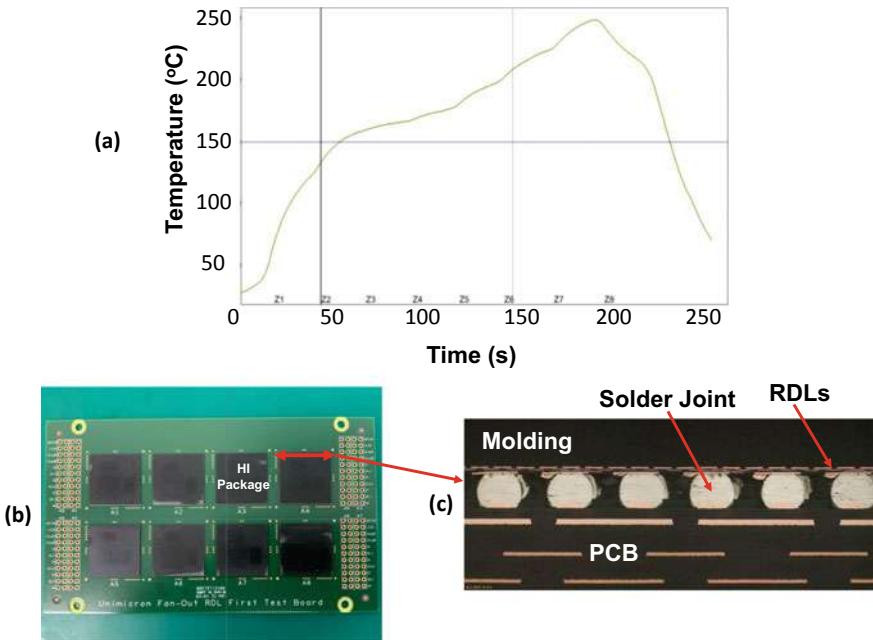
**Fig. 4.60** Reliability test PCB with 8 20 mm × 20 mm heterogeneous integration packages

### A. Printed Circuit Board

The PCB for the heterogeneous integration package is made of FR-4 and is shown in Fig. 4.60. It can be seen that there are eight package sites on the board. The dimensions of the PCB are 132 × 77 × .992 mm<sup>3</sup>, and there are eight layers. There are 2,780 pads (with a pitch = .35 mm) for each package. The pad with a diameter of 0.2 mm is non-solder mask defined, and its surface finish is an organic solderability preservative. The solder mask opening diameter is 0.245 mm and the ball pad diameter is 0.18 mm.

### B. SMT (Surface Mount Technology) Assembly of the Package

The SMT [151] assembly of the heterogeneous integration package on PCB is shown in Fig. 4.61. Figure 4.61a shows the reflow temperature profile, and it can be seen that the maximum temperature is 245 °C. Figure 4.61b shows the assembled PCB with eight heterogeneous integration packages. Figures 4.55, 4.56, and 4.61c show the typical cross sections of the PCB assembly where the chip, Cu pillar and solder cap, EMC, MLs of RDLs, solder joints, and PCB are clearly seen.



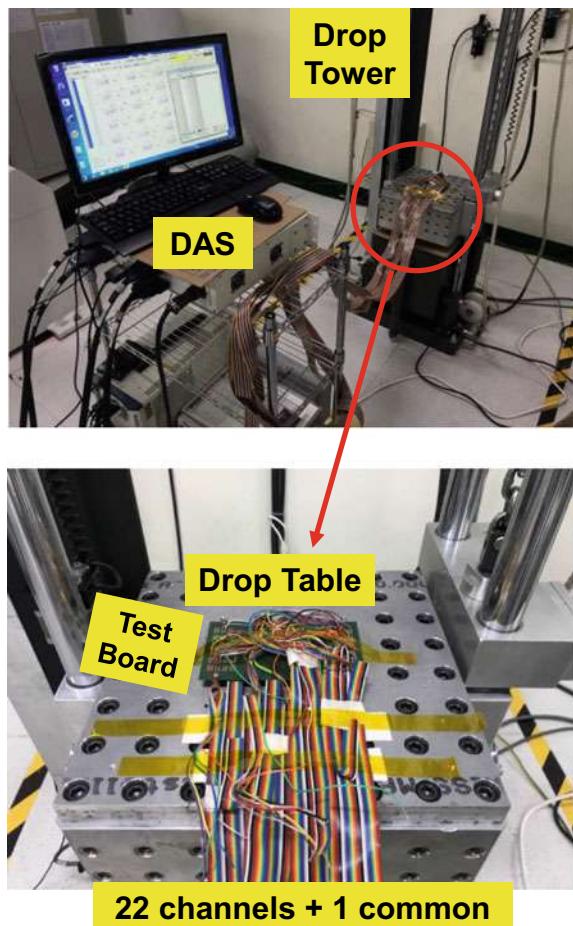
**Fig. 4.61** **a** SMT reflow temperature profile. **b** The assembled test board. **c** Typical cross section of the PCB assembly

#### 4.7.12 Drop Test Results and Failure Analysis

The shock (drop) test setup is according to JEDEC Standard ESD22-B111, as shown in Fig. 4.62. It consists of a drop tower, a drop table for the PCB with samples. There are 22 channels plus one common and a data acquisition system (DAS). The drop spectrum with 1,500 G/ms (1,500-Gs, 0.5-ms half-sine pulse) is shown in Fig. 4.63. The drop condition is 30 drops. The failure criterion is when the measured resistance during the drop test reaches 1,000  $\Omega$  as shown in Fig. 4.64a. Less than that, it is considered no failure, as shown in Fig. 4.64b.

After 30 drops, there is only one failure which occurs after 23 drops. The DAS shows that the second package has failed (Fig. 4.65). Failure analysis by X-ray and cross sections indicates that the failure location of this package occurs near the corner solder joints and the edge near the middle of the PCB as shown in Fig. 4.65. However, this particular solder joint is bad to begin with. It is a head-in-pillow [151] solder joint. Before the drop test, the DAS cannot detect it and think it is a good solder joint. After 23 drops, the head is separated from the pillow, i.e., the solder joint is totally cracked. Thus, this sample should not be counted, and the heterogeneous integration package PCB assembly should be considered passing the drop test. On the other hand, failure analysis on some non-failure samples (the measured resistance is far

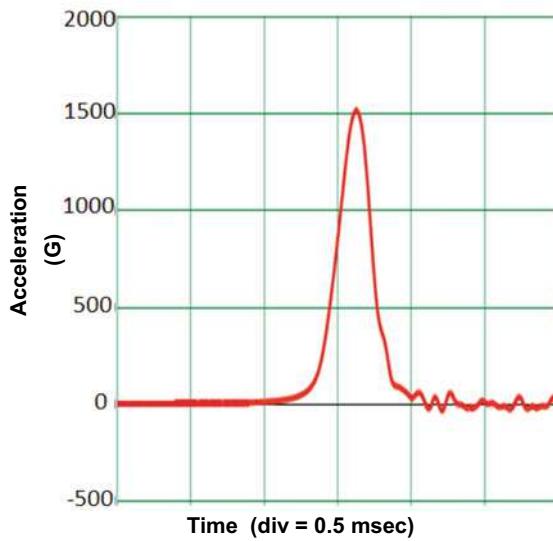
**Fig. 4.62** Drop test set up, DAS, and samples



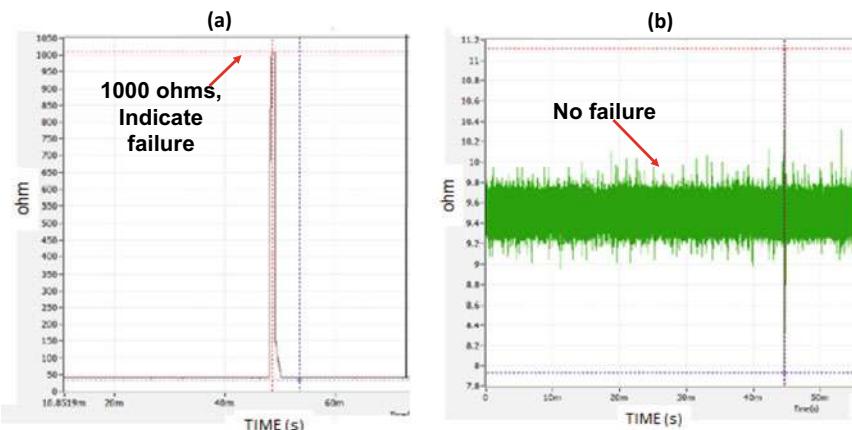
less than  $1,000 \Omega$  as shown in Fig. 4.64b indicates that there are some small cracks in the solder joint as shown in Fig. 4.66.

#### 4.7.13 Thermal-Cycling Test Results and Failure Analysis

The heterogeneous integration package PCB assemblies are put inside a thermal cycling chamber as shown in Figs. 4.67 and 4.68. The temperature in the chamber during test is measured through a thermal couple (in air) and is shown in Fig. 4.69. It can be seen that the temperature profile is basically  $-55 \leftrightarrow 125^\circ\text{C}$  at 50-min cycle. There are 49 channels and each covers certain outer rows of solder joints.



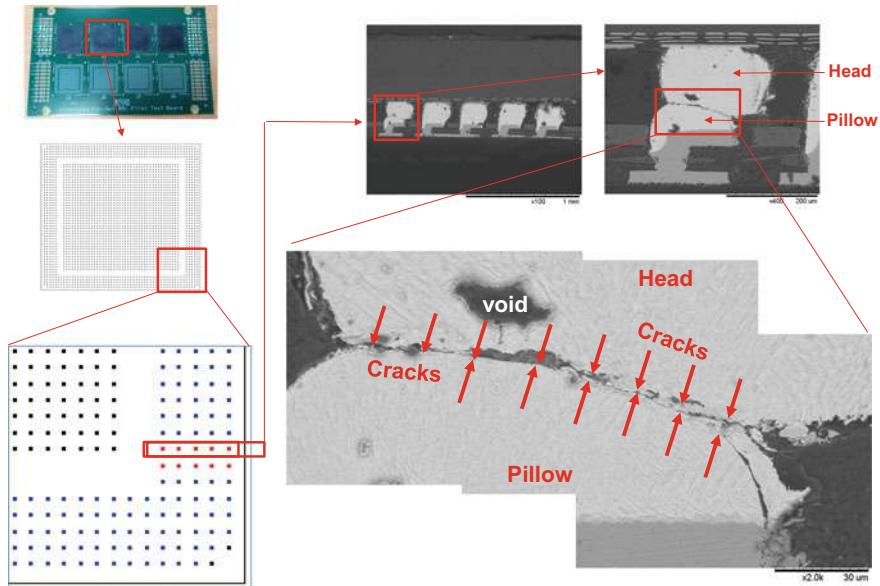
**Fig. 4.63** The drop spectrum



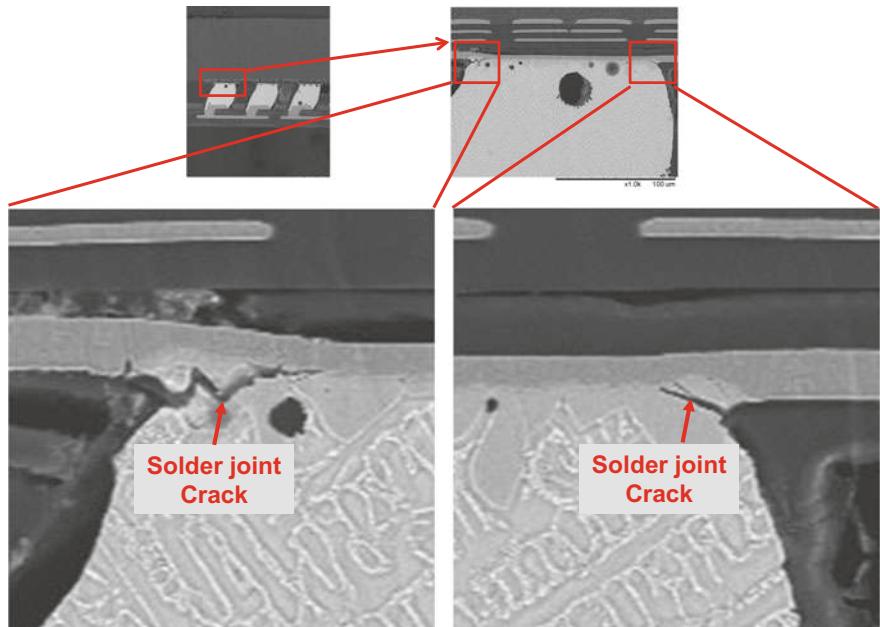
**Fig. 4.64** Failure criterions. **a** When the resistance  $\geq 1000 \Omega$ , it indicates failure. **b** No failure

#### (A) Failure Criterion

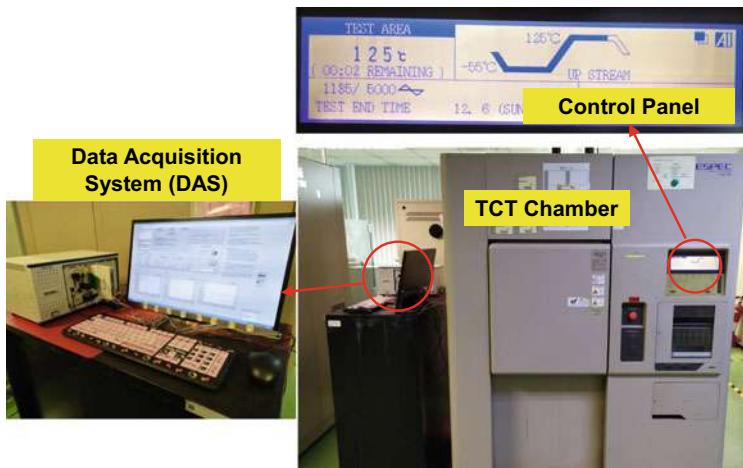
In this study, the failure criterion is when the resistance of the daisy chain of the heterogeneous integration PCB assembly increases by 50%. The cycle at which the first solder joint of a package failed is considered as the cycle-to-failure of the heterogeneous integration package.



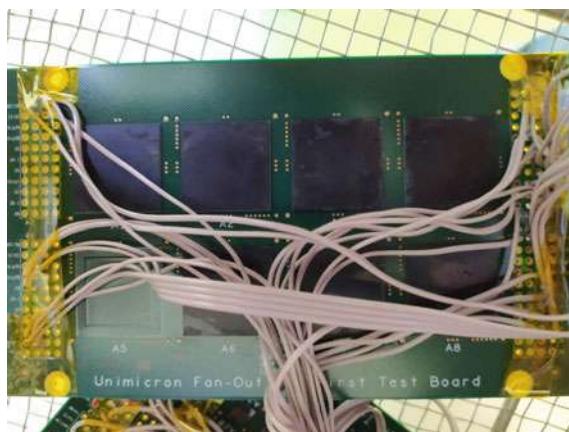
**Fig. 4.65** The failure location and failure mode of the only failure sample under drop test. It turns out the failure sample is bad (head-in-pillow) to begin with



**Fig. 4.66** No-failure sample showing small cracks after drop test



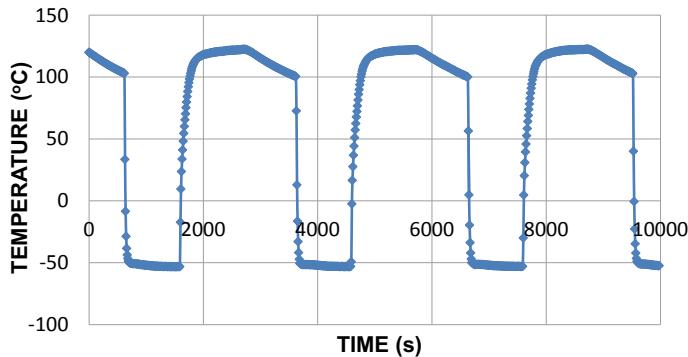
**Fig. 4.67** Thermal cycling chamber and data acquisition system



**Fig. 4.68** Test boards with the packages inside thermal cycling chamber

### (B) Test Results of the Package at Median Rank

The thermal cycling test results of the heterogeneous integration package PCB assembly are tabulated in Table 4.3. It can be seen that there are 12 failures. The median (50%) rank are determined from  $F(x) = (j - 0.3)/(n + 0.4)$ , where  $j$  = failure order number and  $n$  = sample size = 49. These data are plotted into a Weibull distribution and is shown in Fig. 4.70 for the median rank. It can be seen that the characteristic life ( $\theta$ ) (63.2% failed) = 1,702 cycles and the Weibull slope ( $\beta$ ) is = 2.28.



**Fig. 4.69** Thermal cycling temperature profile

**Table 4.3** Thermal cycling test results (sample size = 49) at median rank, 5% rank, and 95% rank

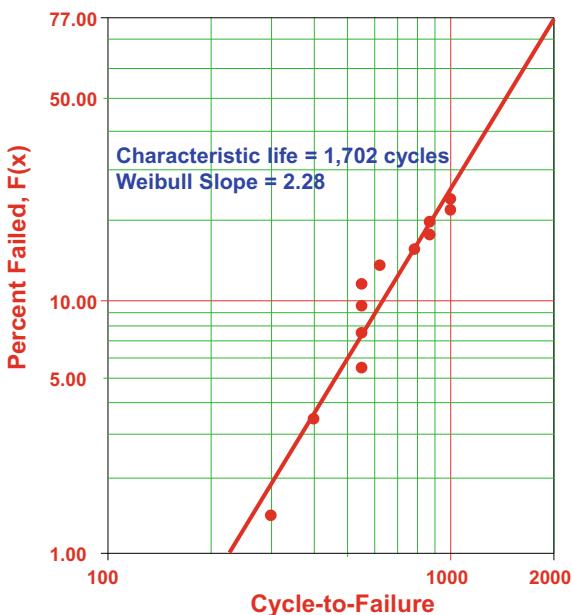
Failure order	Cycles-to-failure	$F(x)$	90% confidence		
			Median (50%) rank	5% rank	95% rank
1	300	1.41	0.1	5.93	
2	400	3.43	0.73	9.32	
3	552	5.46	1.69	12.3	
4	552	7.48	2.84	15.07	
5	552	9.51	4.11	17.71	
6	552	11.53	5.47	20.27	
7	624	13.56	6.9	22.74	
8	788	15.58	8.39	25.16	
9	872	17.6	9.93	27.54	
10	872	19.63	11.51	29.86	
11	1003	21.65	13.13	32.15	
12	1003	23.68	14.78	34.41	

Sample size = 49

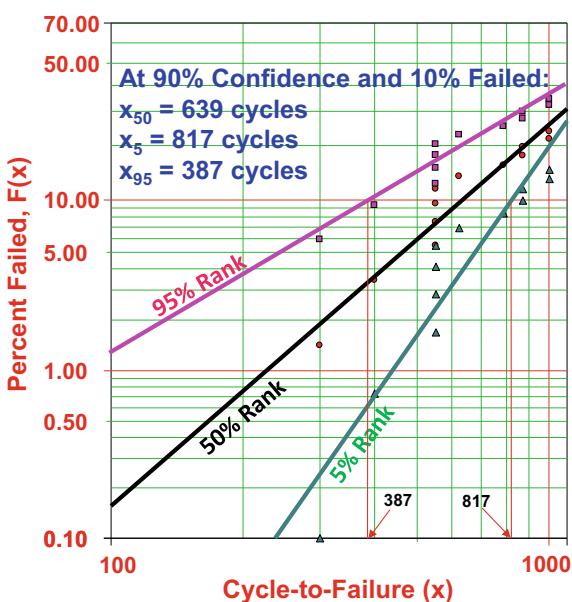
### (C) Test Results of the Package at other Ranks

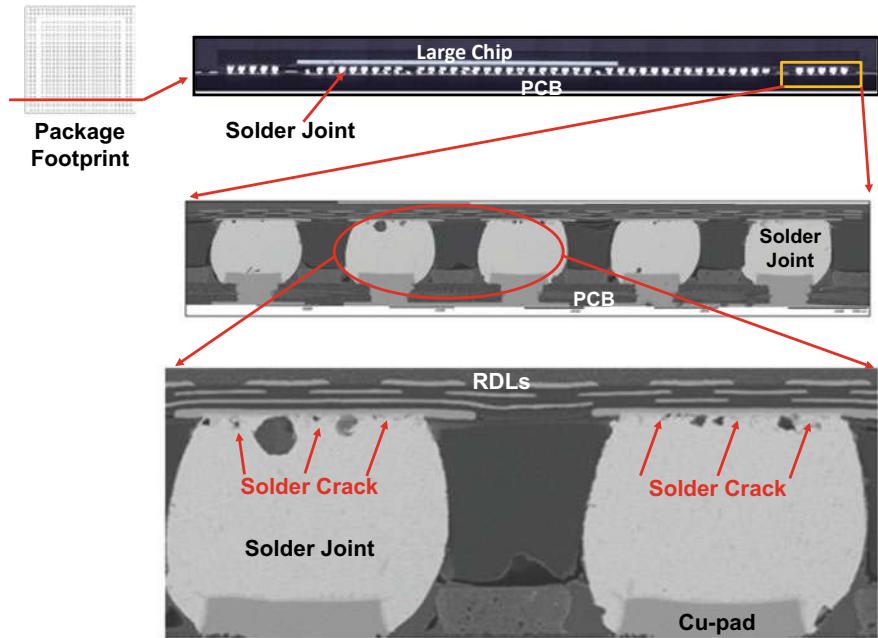
For 90% confidence level, we need the 5% rank ( $G = 5\%$ ) and 95% rank ( $G = 95\%$ ) and they are also listed in Table 4.3. For examples, with  $n = 49$  and  $G = 5\%$ , the percent failure rank ( $z$ ) is 0.1 for  $j = 1$  and is 0.73 for  $j = 2$ . Another examples, with  $n = 49$  and  $G = 95\%$ , the percent failure rank ( $z$ ) is 5.93 for  $j = 1$  and is 9.32 for  $j = 2$ . Figure 4.71 shows the Weibull plot of the solder joints for the heterogeneous integration package PCB assembly at 90% confidence. It can be seen that at 90%

**Fig. 4.70** Weibull plot of the heterogeneous integration solder joints at median rank



**Fig. 4.71** Weibull plot of the heterogeneous integration solder joints at 90% confidence





**Fig. 4.72** Failure location and failure mode

confidence (that is one in ten cases it will happen), the true 10% failed life is  $387 \leq x_t \leq 817$  cycles.

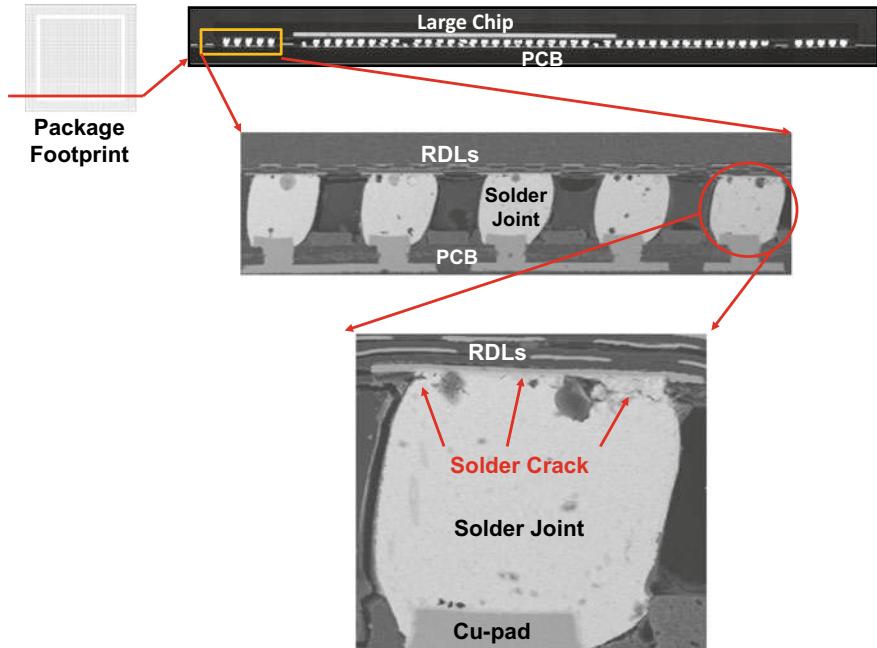
#### (D) Failure Location and Failure Mode of the 6-side Molded PLCCSP PCB Assembly

The typical failure location occurs near the solder joints underneath the Chip 1 and Chip 2A corners as shown in Figs. 4.72 and 4.73. The failure mode is the cracking of the solder near the interface between the RDL-substrate and the bulk solders as shown in Figs. 4.72 and 4.73.

#### (E) True Weibull Slope

Confidence is defined as the probability that a given interval determined from the test data will contain the population parameters, such as (using Weibull as an example) the mean/characteristic life and Weibull slope. Confidence applies to the test itself and reliability applies to the product!

To predict the true Weibull slope ( $\beta_t$ ) of the population, it is necessary to estimate the Weibull slope error in relation to the sample size and the required confidence level. The error ( $E$ ) in the Weibull slope depends on the number of failures ( $N$ ) and the required confidence level ( $C$ ), which can be searched from equation [151]:



**Fig. 4.73** Failure location and failure mode

$$\frac{1}{\sqrt{\pi}} \int_{-\infty}^{E\sqrt{2N}} e^{-\frac{t^2}{2}} dt = \frac{1 + C}{2}$$

This integral cannot be carried out in close-form and is approximated by the following

$$\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{E\sqrt{2N}} e^{-\frac{t^2}{2}} dt = 1 - Z(x)(b_1 t + b_2 t^2 + b_3 t^3 + b_4 t^4 + b_5 t^5) + \varepsilon(x)$$

where

$$Z(x) = \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}}$$

$$t = \frac{1}{1 + px}$$

$$x = E\sqrt{2N}$$

$$\begin{aligned}
p &= 0.2316419, \\
b_1 &= 0.31938153, \\
b_2 &= -0.356563782, \\
b_3 &= 1.781477937, \\
b_4 &= 1.821255978, \\
b_5 &= 1.330274429, |\varepsilon(x)| < 7.5 \times 10^{-8}
\end{aligned}$$

Thus, for a given  $C$  (the confidence level) and  $N$  (the number of failures), the  $E$  (error) can be searched from the above equations. In our case, for 90% confidence, i.e.,  $C = 0.9$ , and  $N = 12$ , we can search that  $E = 0.32$ . Thus, the true Weibull slope  $\beta_t$  of the heterogeneous integration solder joints will be happened in the intervals of  $(2.28 - 0.32 \times 2.28) \leq \beta_t \leq (2.28 + 0.32 \times 2.28)$  or  $1.55 \leq \beta_t \leq 3.01$ .

#### (F) Linear Acceleration Models

There are many linear acceleration models [151] for lead-free solder alloys. Basically, they are based on [152] (a) dwell time and maximum temperature [153], (b) frequency and maximum temperature [154], and (c) frequency and mean temperature [155]. The one proposed by Lall, et al., [154] will be adopted in the present study.

$$\alpha = \left( \frac{\Delta T_t}{\Delta T_o} \right)^{2.3} \left( \frac{f_o}{f_t} \right)^{0.3} \exp \left[ 4562 \left( \frac{1}{T_{\max,t}} - \frac{1}{T_{\max,o}} \right) \right]$$

In this equation,  $T_{\max,t}$ ,  $f_t$ ,  $\Delta T_t$  and  $T_{\max,o}$ ,  $f_o$ ,  $\Delta T_o$ , are the maximum temperature during cycling (in degrees Kelvins), the temperature cycling frequency, and the temperature range (in degree Celsius), respectively, at testing condition and at operating condition. In our case,  $\Delta T_t = 180$  °C,  $T_{\max,t} = 125$  °C, and  $f_t = 28.8$  cycle/day, and we know that the solder joint can survive up to 300 cycles (Table 4.3 and Fig. 4.70). However, we also need to know if this value of 300 cycles is sufficient to meet the 5-year operating condition given by 0 to 80 °C with 1 cycle per day ( $\Delta T_o = 80$  °C,  $T_{\max,o} = 80$  °C, and  $f_o = 1$  cycle/day).

$$\alpha = \left( \frac{180}{80} \right)^{2.3} \left( \frac{1}{28.8} \right)^{0.3} \exp \left[ 4562 \left( \frac{1}{273 + 80} - \frac{1}{273 + 125} \right) \right]$$

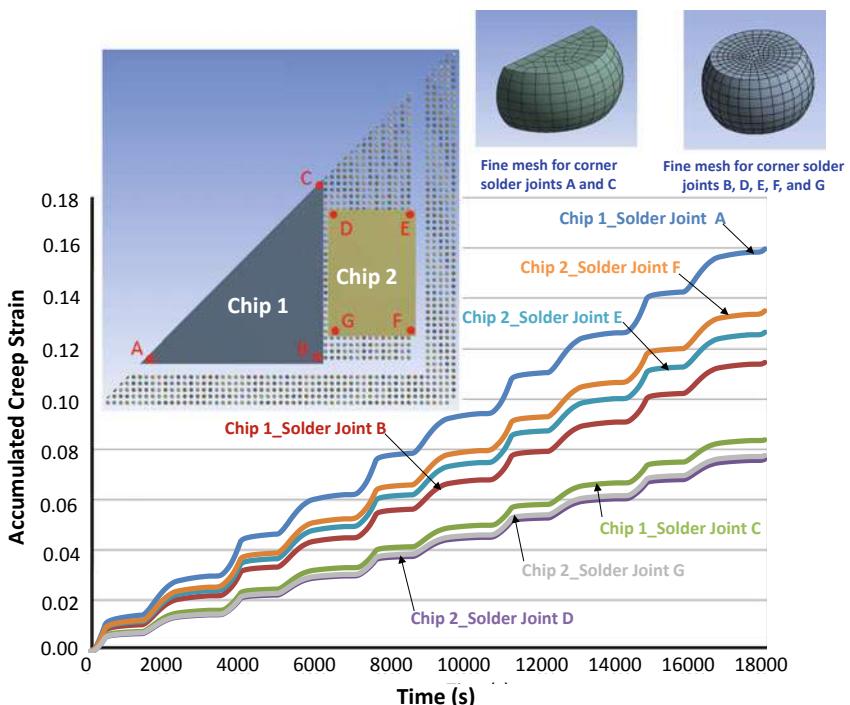
$$\alpha = 10.76$$

The solder joints will survive  $10.76 \times 300$  cycle per day =  $3,228 \div 365 = 8.84$  years > 5 years.

#### 4.7.14 Thermal-Cycling Simulation

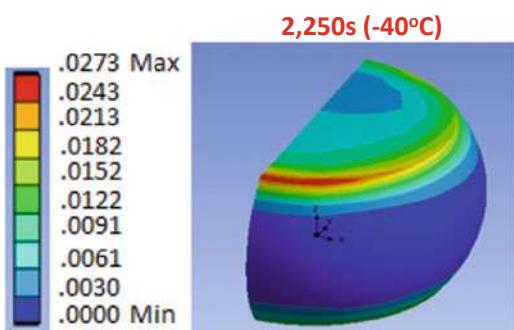
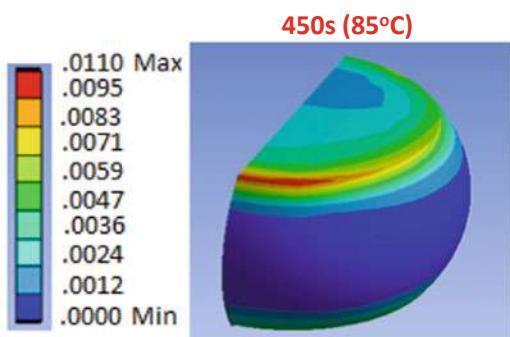
The simulation of the heterogeneous integration PCB assembly has been reported in [130]. The accumulated creep strain time-history at various solder joint locations is shown in Fig. 4.74. It can be seen that the maximum accumulated creep strain occurs at the corner solder joint A underneath the Chip 1 and the second maximum accumulated creep strain occurs at the corner solder joint F underneath Chip 2A. Thus, any solder joint failure should initial at these locations. This confirmed with the failure analysis of thermal cycling test results as shown in Figs. 4.72 and 4.73.

The accumulated creep strain contours at solder joint A and solder joint F at 450 s ( $85^{\circ}\text{C}$ ) and 2,250 s ( $-40^{\circ}\text{C}$ ) are shown in Figs. 4.75 and 4.76, respectively. It can be seen that for both solder joints and at  $85$  and  $-40^{\circ}\text{C}$ , the maximum accumulated creep strain occurs near the interface between the RDL-substrate and the bulk solders. Thus, the failure mode of the solder joints is the cracking of solder near the interface between the RDL and the bulk solders. Again, this failure mode confirms with the thermal cycling test results (Figs. 4.72 and 4.73).

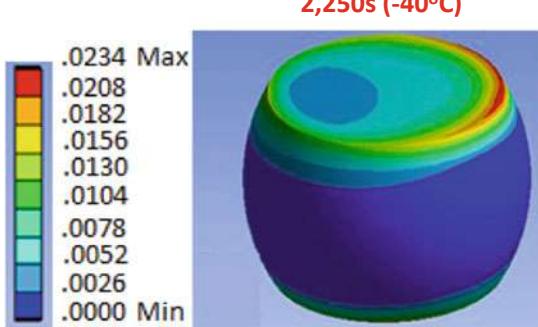
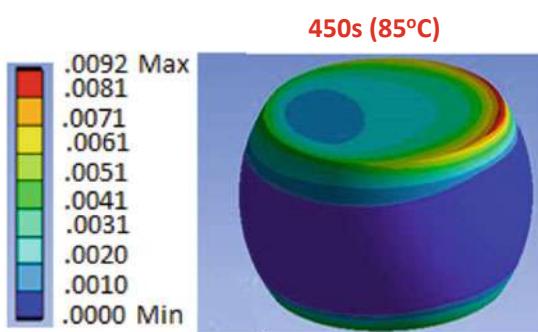


**Fig. 4.74** Accumulated creep strain versus time at various locations of solder joints

**Fig. 4.75** Accumulated creep strain at solder joint A at 450 s (85 °C) and 2,250 s (-40 °C)



**Fig. 4.76** Accumulated creep strain at solder joint F at 450 s (85 °C) and 2,250 s (-40 °C)



#### 4.7.15 Summary and Recommendation

Some important results and recommendation are summarized as follows [131].

- Thermal cycling test of the heterogeneous integration of three chips package PCB assembly has been performed. There were 49 channels and each covered certain outer rows of solder joints. The test condition was  $-55 \leq 125^{\circ}\text{C}$  at 50-min cycle.
- The failure criterion was when the resistance of the daisy chain of the heterogeneous integration PCB assembly increased by 50%. The cycle at which the first solder joint of a channel failed is considered as the cycle-to-failure of the heterogeneous integration package.
- For the median rank, the Weibull slope and the characteristic life of the solder joints of the package assembly are, respectively 2.28 and 1,702 cycles.
- For 90% confidence (in nine out of ten cases) the true Weibull slope is  $1.55 \leq \beta_t \leq 3.01$  and the true 10% life is  $387 \leq x_t \leq 817$  cycles.
- The typical failure location of the heterogeneous integration package PCB assembly occurs near the solder joints underneath the corner (A) of Chip 1 and the corner (F) of Chip 2A.
- The typical failure mode of the heterogeneous integration package PCB assembly is the cracking of solder joint near the interface between the RDL-substrate and the bulk solders.
- For an operating condition (0 to  $80^{\circ}\text{C}$  with 1 cycle per day), the solder joint of the heterogeneous integration of 3-chip package can survive 8.84 years.
- A non-linear, time and temperature dependent 3D finite element simulation of the heterogeneous integration PCB assembly confirmed the failure location and failure mode with the thermal cycling test results.
- For more information on fan-out packaging, please read [16, 104].

### 4.8 Fan-Out Panel-Level Packaging of Mini-LED RGB Display

The feasibility of mini-LED RGB display fabricated by a chip-first fan-out panel-level packaging is investigated. Emphasis is placed on the design, materials, process, fabrication, and reliability of the mini-LED RGB display package on a printed circuit board (PCB). The mini-LEDs under consideration and their sizes are Red ( $125 \times 250 \times 100 \mu\text{m}$ ), Green ( $130 \times 270 \times 100 \mu\text{m}$ ), and Blue ( $130 \times 270 \times 100 \mu\text{m}$ ). The spacing among the RGB mini-LEDs is  $80 \mu\text{m}$ , the pixel-to-pixel spacing is also  $\sim 80 \mu\text{m}$ , and the pixel pitch is  $625 \mu\text{m}$ . The temporary glass panel for making the RDLs of the package is  $515 \times 510 \times 1.1 \text{ mm}$  in size. In order to increase the SMT assembly yield on the PCB, the mini-LEDs are grouped into  $4(2 \times 2 \text{ pixels})$  in one SMD (surface mount device), i.e., a total of 12 R, B, and G mini-LEDs. A PCB ( $132 \text{ mm} \times 77 \text{ mm}$ ) is designed and fabricated for the drop test of the mini-LED

package. Thermal cycling of the mini-LED SMD PCB assembly is also performed by a nonlinear temperature- and time-dependent finite-element simulation.

Light emitting diode (LED) is a specialized semiconductor that glows when current passes through it. When the current is on, it emits light. While the current is off, it goes dark. The average size of a conventional LED is 1 mm [156], of a mini-LED is 75–300  $\mu\text{m}$  [157], and of a micro-LED is  $\leq 75 \mu\text{m}$  [157]. Since the shipment of MSI (Micro-Star International) Creator 17 gaming notebook with mini-LED backlighting liquid-crystal display (LCD) in April 2020 [158], the mini-LED has been getting lots of tractions. For examples, Apple [159] is set to launch its first mini-LED backlit LCD iPad Pro in the first quarter of 2021 and mass produce mini-LED backlit LCD MacBook Pro in the second quarter of 2021. Samsung Electronics [160] plans to ship 2 million mini-LED backlit LCD televisions in 2021.

There are at least two different kinds of mini-LED display technology, namely, the mini-LED backlighting (backlit) LCD and the mini-LED RGB display. For LCD, each color filter defines a sub-pixel and we control the color filter to generate an image. For mini-LED RGB display, each mini-LED is a sub-pixel and we drive each mini-LED to generate an image. Mini-LED RGB display is the focus of this study.

Most of the current assembly methods of mini-LEDs RGB display are picking up the individual mini-LED from a diced LED-wafer and placing it on a PCB with solder paste and then SMT (surface mount technology) reflow [151]. Basically, this is the very old mini-LED (chip)-on-board technology [161]. One of the drawbacks of this method is the limitation (from PCB) of the pitch (or spacing) between the mini-LEDs and the other is the assembly yield (because of the flatness of the electroplated Cu-pad on PCB).

Another possible assembly method is to use PBGA (plastic ball grid array) packages which attach some of the mini-LEDs on an organic package substrate with solder balls on PCB. In this case, the pitch between the mini-LEDs can be slightly smaller and the pressure on PCB is eliminated. However, the assembly yield-loss due to the flatness of the electroplated Cu-pad on the organic package substrate remains. Also, there are additional costs on: (a) LED wafer bumping or stencil printing solder paste on the package substrate or LED wafer, and (b) the package substrate.

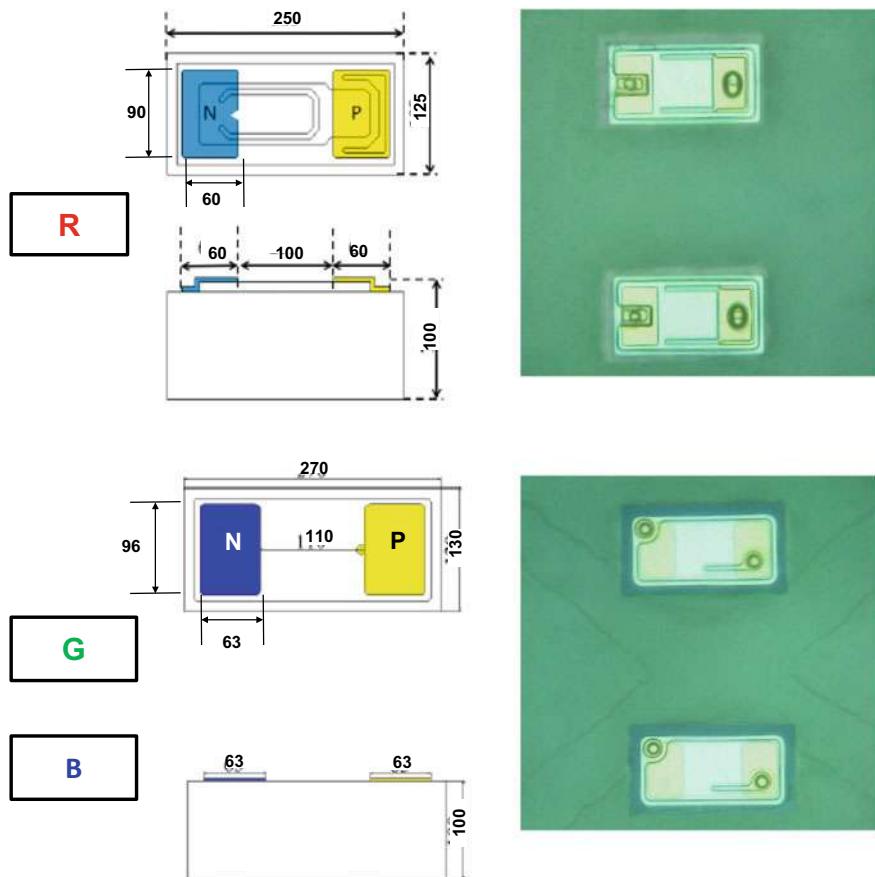
In order to have very high-density (e.g., ultra-fine pitch) and low-cost (e.g., minimum yield loss) mini-LED RGB display package, in this study, the fan-out (chip-first with die face-down) assembly process [1–10] is adopted. Because of the nature of fan-out technology [16, 104], the spacing between individual mini-LEDs can go down to  $< 50 \mu\text{m}$ . Also, because of the fan-out RDLs (redistribution-layers), the mini-LED is not in contacted to the electroplated Cu-pad on PCB. Comparing with the PBGA method, the costs and process steps of the package substrate and solder bumps between the LEDs and the package substrate are eliminated. Also, lower package profile can be obtained from fan-out technology. Alternatively, fan-out technology requires a temporary carrier and the fabrication of the RDLs.

There are at least two different kinds of temporary carrier for making the RDLs, namely, round (wafer) [12, 13] or rectangular (panel) [14, 15]. In order to have high throughputs, in this study, a rectangular panel is used as the temporary carrier.

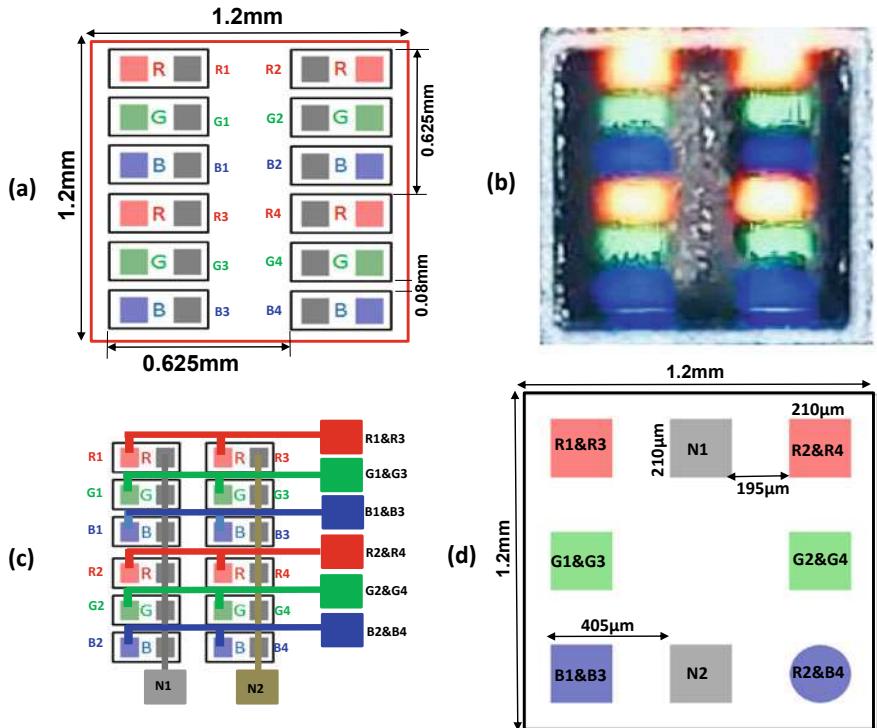
A PCB is designed and fabricated for the drop test of the mini-LED package. Thermal cycling of the mini-LED RGB display SMD PCB assembly is also performed by a 3-dimensional nonlinear temperature- and time-dependent finite-element simulation.

#### 4.8.1 Test Mini—LEDS

The mini-LEDs under consideration are shown in Fig. 4.77. Their dimensions are Red ( $125 \times 250 \times 100 \mu\text{m}$ ), Green ( $130 \times 270 \times 100 \mu\text{m}$ ), and Blue ( $130 \times 270 \times 100 \mu\text{m}$ ). The pad surface finishing of the P-electrode and N-electrode of these mini-LEDs is Cr/Au. The pad-size of the Green and Blue mini-LEDs is  $96 \mu\text{m} \times$



**Fig. 4.77** Test LEDs: Red ( $125 \times 250 \times 100 \mu\text{m}$ ), Green ( $130 \times 270 \times 100 \mu\text{m}$ ), and Blue ( $130 \times 270 \times 100 \mu\text{m}$ )



**Fig. 4.78** SMD. **a** 4(2 × 2 pixels) in one SMD, i.e., a total of 12 R, B, and G mini-LEDs. **b** The light-up SMD. **c** Daisy-chain layout of the SMD. **d** The bottom-side layout of the SMD

63  $\mu\text{m}$  and of the Red mini-LED is 90  $\mu\text{m} \times 60 \mu\text{m}$ . In order to improve SMT assembly yield, 12 individual mini-LEDs are grouped into a 4 in one SMD as shown in Fig. 4.78a. It can be seen that the spacing among the RGB mini-LEDs is 80  $\mu\text{m}$  and the pixel-to-pixel spacing is also  $\sim 80 \mu\text{m}$ . The pixel pitch is 625  $\mu\text{m}$ . The mini-LEDs are daisy-chained as shown in Fig. 4.78c. Figure 4.78d shows the layout of the bottom-side of the SMD [162].

#### 4.8.2 Test Mini-LED RGB Display SMD Package

The cross section of the test mini-LED RGB display SMD package is schematically shown in Fig. 4.79. It can be seen that the mini-LEDs are packaged by a fan-out chip-first with die face-down process. There are two RDLs with metal linewidth ( $L$ ) and spacing ( $S$ ) equal to 35/35  $\mu\text{m}$  for RDL1 and 35/50  $\mu\text{m}$  for RDL2 as shown in Fig. 4.80.

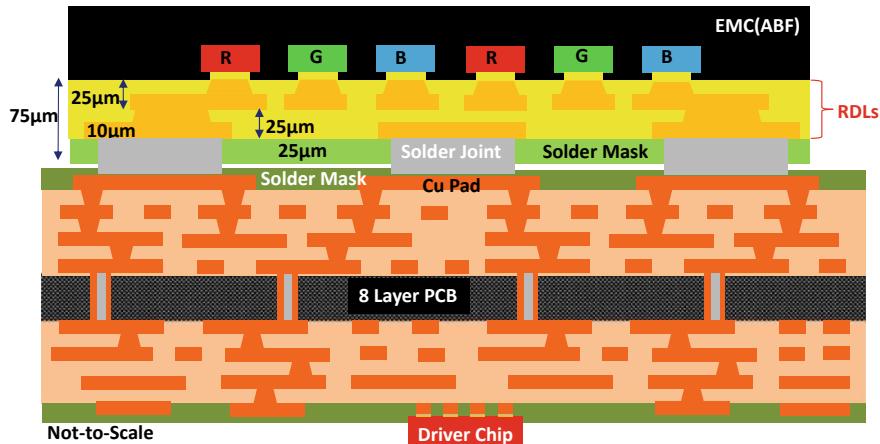


Fig. 4.79 Cross section schematic of the test mini-LED RGB SMD package PCB assembly

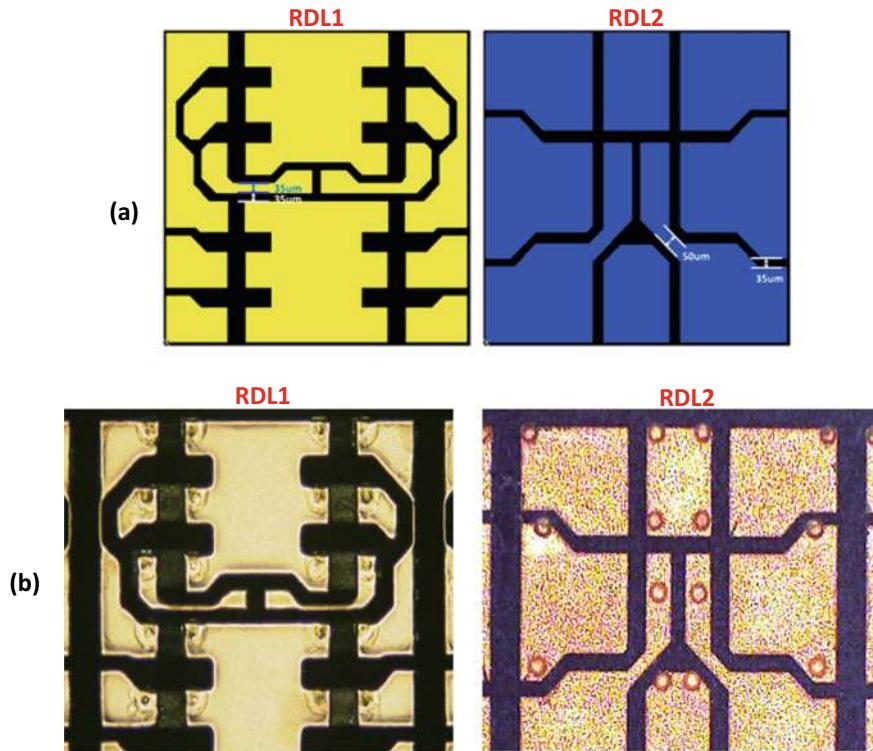


Fig. 4.80 RDLs. a Layout of RDL1 and RDL2. b Fabricated RDL1 and RDL2

### 4.8.3 RDL and Mini-LED RGB SMD Fabrication

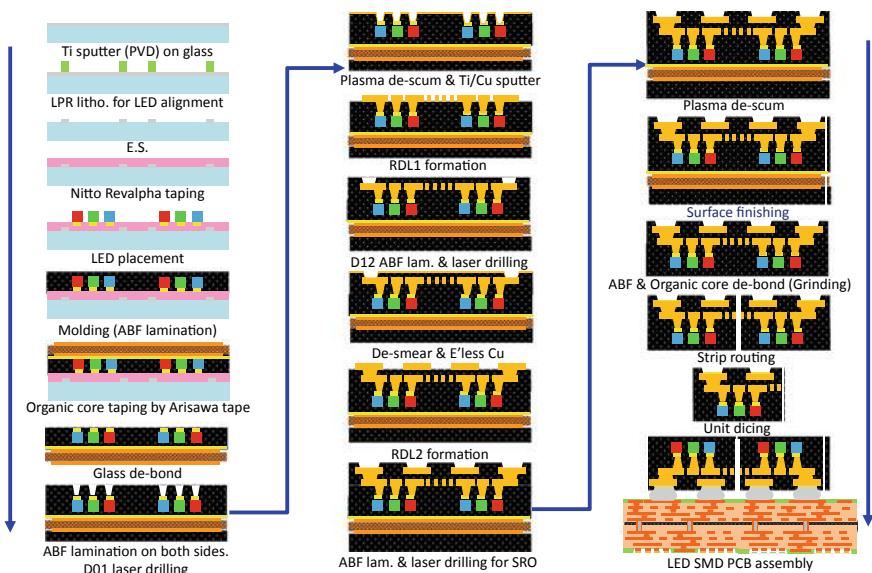
Figure 4.81 shows the key process steps in fabricating the RDLs of the mini-LED RGB display package by fan-out (chip-first and face-down) process [12, 13].

#### (A) Pick and Place of Mini-LEDs

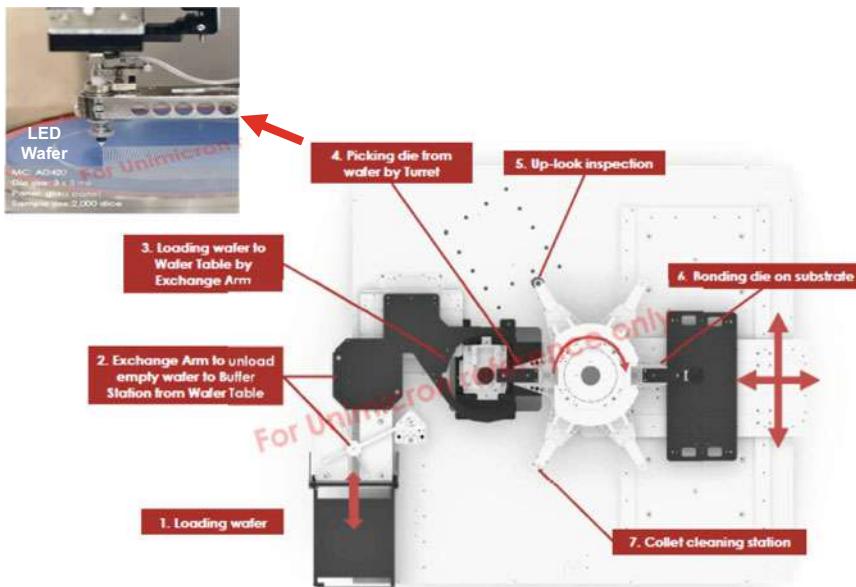
After the sputtering of Ti by physical vapor deposition (PVD) on a 515 mm × 510 mm × 1.1 mm glass temporary carrier, liquid photoresist (LPR) lithography for the LED alignments, etching and striping, and Nitto Revalpha taping, it is time to perform the pick and place (P&P) of the mini-LEDs as shown in Fig. 4.81. There will be 629,712 mini-LEDs per 515 mm × 510 mm panel. However, in order to save some of the mini-LEDs only 74,064 mini-LEDs are P&P on the temporary carrier. It is performed by the ASM AD420 high throughput chip shooter as shown in Fig. 4.82. Figure 4.83 shows the temporary panel with the P&P mini-LEDs.

#### (B) Molding with ABF

After P&P of the mini-LEDs, it is time for molding as shown in Fig. 4.81. In this study, the epoxy molding compound (EMC) is the ABF (Ajinomoto build-up film). The laminate condition of the ABF is operating in two stages: (1) at the first stage, the temperature is 120 °C for 30 s at vacuum condition and then press (0.68 MPa) for 30 s with the temperature and vacuum on, and (2) at the second stage, the temperature



**Fig. 4.81** Key process steps of fan-out panel-level packaging of mini-LEDs



**Fig. 4.82** Pick and place equipment for mini-LEDs by ASM

is 100 °C and press (0.58 MPa) for 60 s for flatness. Figure 4.84 shows the molded panel.

### (C) Second Carrier Attachment

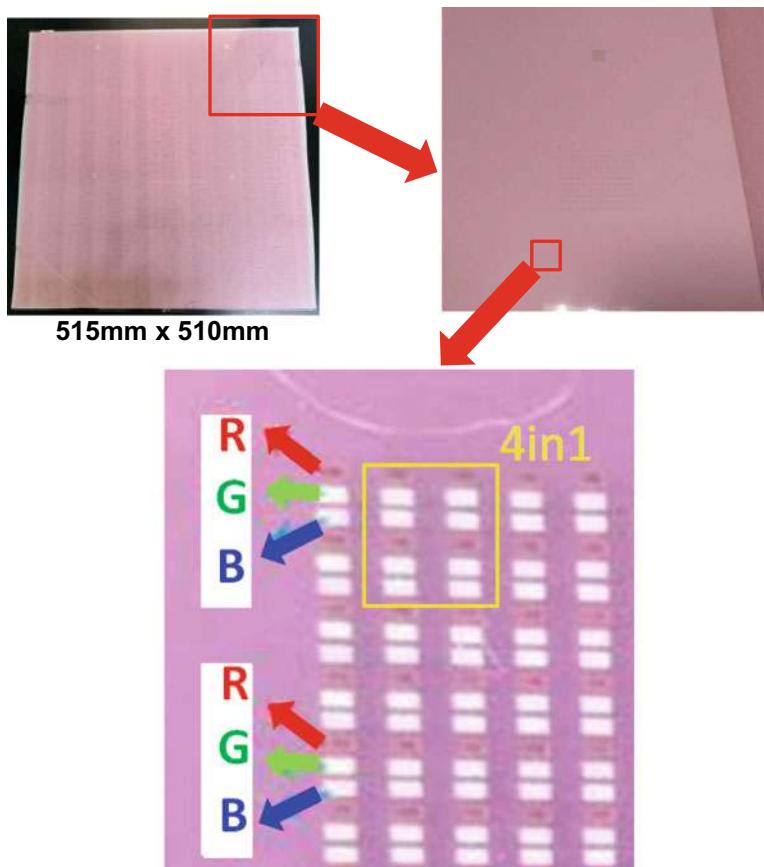
In order to save the ABF material and have a lower profile package, only 150  $\mu\text{m}$ -thick of ABF is used. Thus, before debonding the temporary glass carrier, an organic core is attached with an Arisawa tape to the backside of the ABF as shown in Fig. 4.81.

### (D) Debond the First Temporary Glass Carrier

The debonding temperature of the temporary glass carrier is 170 °C. Under this temperature, it is easy to remove the glass carrier and peel off the tape. Then, chemical clean the surface.

### (E) RDLs Fabrication

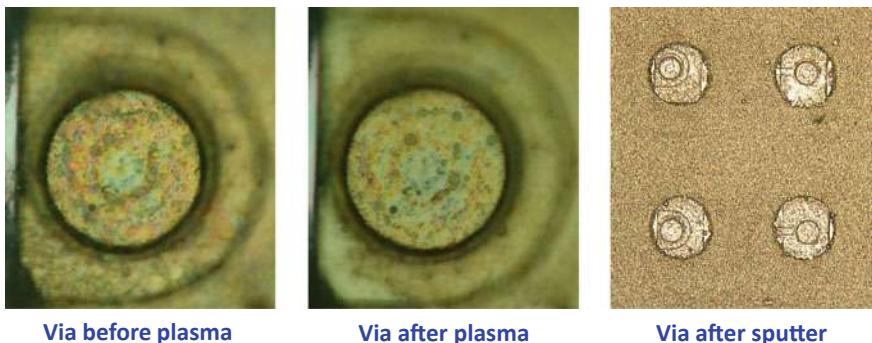
First, laminate the ABF on both sides of the reconstituted panel. It is followed by laser drilling, plasma de-scum and Ti/Cu sputtering (because of the Au surface finishing of the mini-LEDs), Fig. 4.85. Then, dry film lamination, LDI (laser direct imaging) and develop, electroplating Cu, dry film stripping, and Ti/Cu etching to obtain the first RDL (RDL1), as shown in Fig. 4.80b. The dielectric layer is ABF and the metal conductor layer is Cu.



**Fig. 4.83** Mini-LEDs on the temporary glass panel with the Revalpha tape

**Fig. 4.84** EMC (ABF) molding





**Fig. 4.85** Plasma de-scum and Ti/Cu sputtering of ABF vias

To fabricate RDL2, again laminate the ABF and laser drilling. Then, desmear and electroless Cu, dry film lamination, LDI and develop, electroplate Cu, dry-film stripping and seed layer etching to obtain the second RDL (RDL2) as shown in Fig. 4.80b.

#### (F) Solder Mask Opening and Surface Finishing

Laminating the ABF and laser drilling for solder mask opening (SMO) or solder resist opening (SRO) and plasma descum. Then, electroless palladium immersion gold (EPIG) as shown in Fig. 4.86.

#### (G) Backgrinding and Panel Routing

Finally, some of the ABF and the organic core are backgrinded away and the reconstituted panel is routed into individual mini-LED RGB display SMDs with 2 RDLs as shown in Fig. 4.87.

### 4.8.4 PCB Assembly

#### (A) PCB layout

The layout of the test PCB (132 mm × 77 mm) to support the mini-LED RGB display SMDs for drop test and thermal cycling test is shown in Fig. 4.88. It is an 8-layer PCB with a few different mini-LED RGB display SMDs such as 4-in-1, 16-in-1, etc.

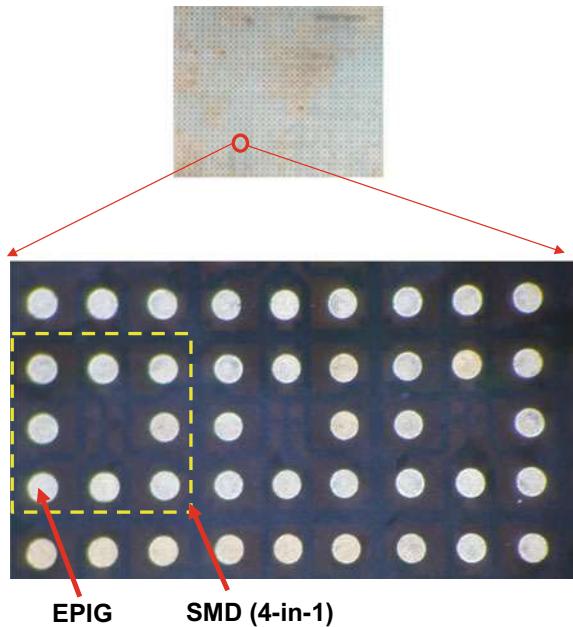


Fig. 4.86 SMO by laser drilling and EPIG surface finishing

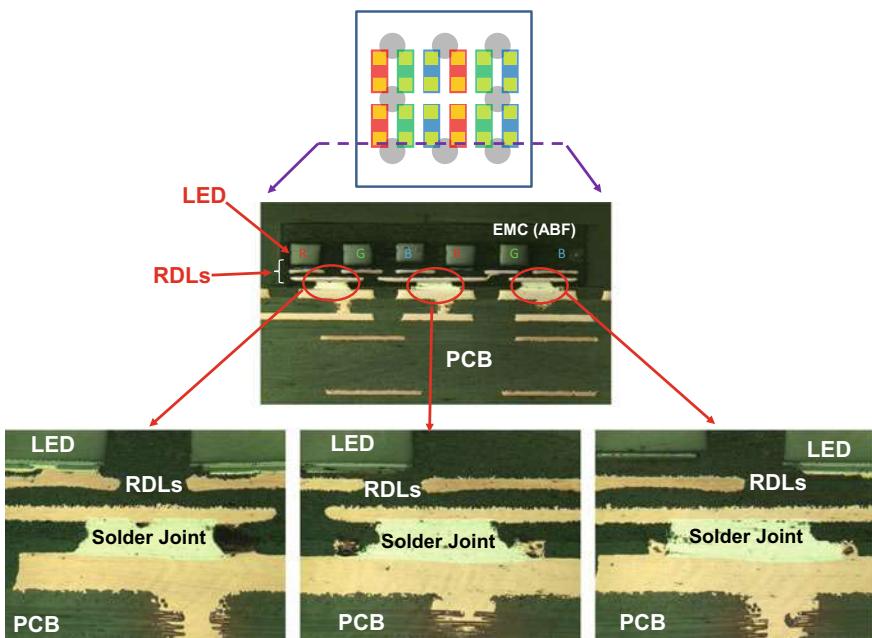
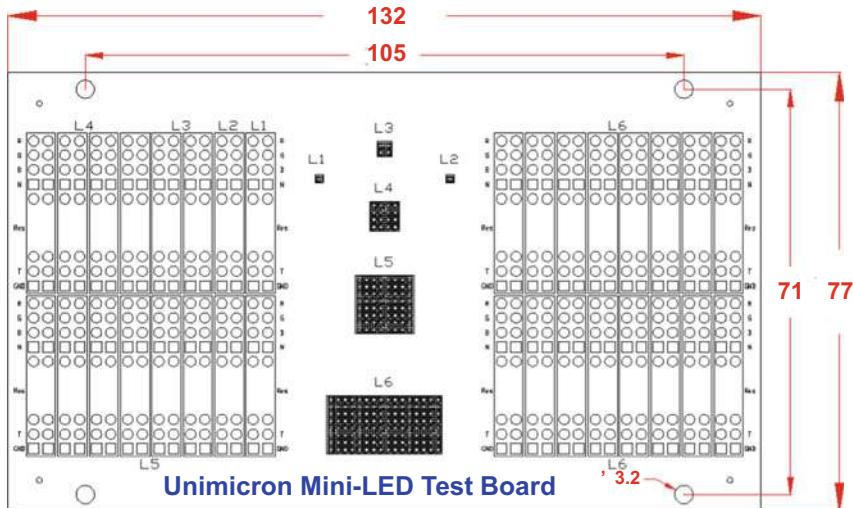


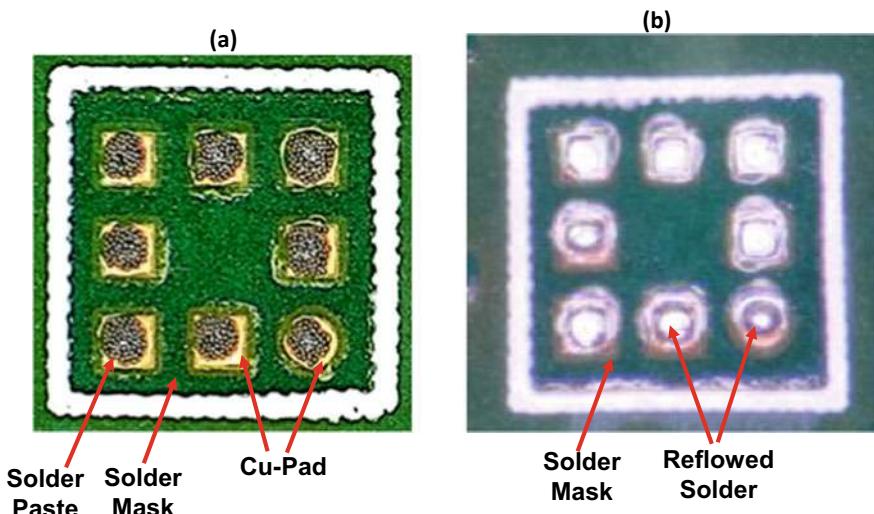
Fig. 4.87 Cross section image of the mini-LED SMD PCB assembly



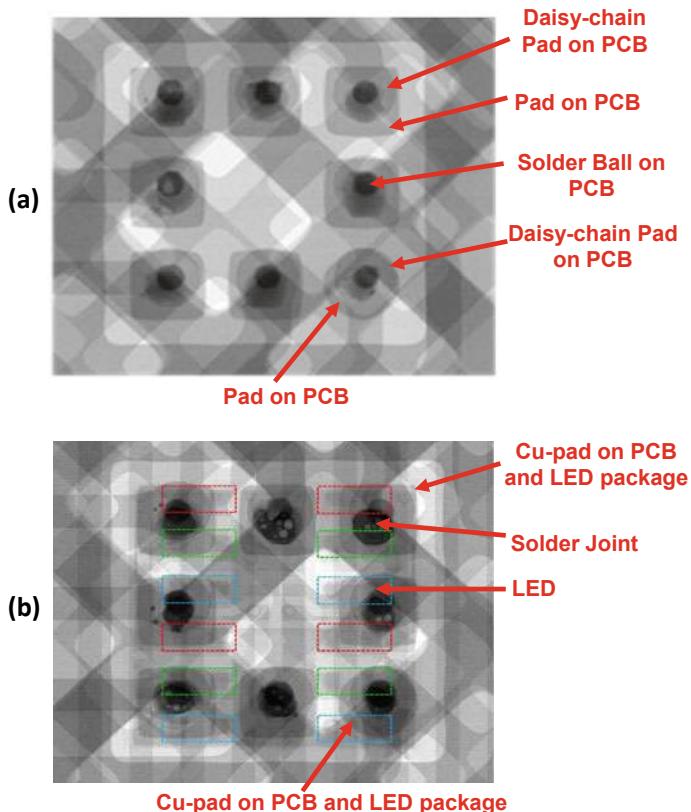
**Fig. 4.88** PCB layout for the drop test and thermal cycling test of mini-LEDs package

### (B) Stencil Printing Solder Paste on PCB

A stainless steel stencil with 170  $\mu\text{m}$ -diameter opening is used to print the Sn3Ag0.5Cu solder paste on the PCB as shown in Fig. 4.89a. After reflowed, the solder balls are shown in Figs. 4.89b and 4.90a.



**Fig. 4.89** **a** Solder paste printing on the PCB. **b** Reflow of the solder paste on PCB



**Fig. 4.90** **a** X-ray image of the PCB with reflowed solder. **b** X-ray image of the mini-LED SMD PCB assembly

### (C) Final SMT Assembly

The mini-LED RGB display SMD is picked and placed on the PCB with solder balls plus flux. Then, use the standard SMT reflow process. A typical cross section of the mini-LED RGB display SMD PCB assembly is shown in Fig. 4.87. In order to see the mini-LEDs, the solder joints are not cut along their center but near the edge. An x-ray image of the final assembly is shown in Fig. 4.90b.

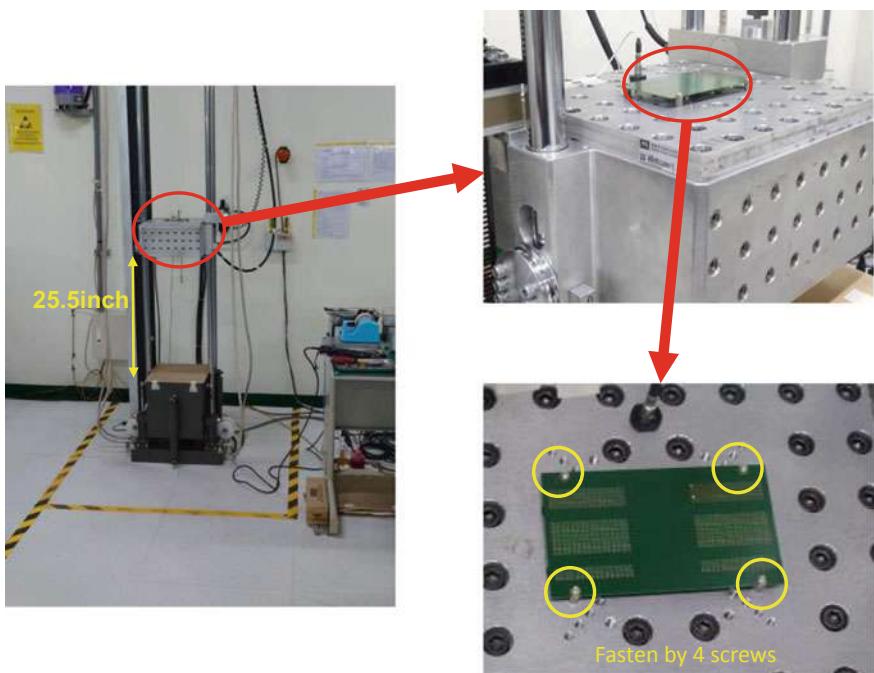
#### 4.8.5 Drop Test

##### (A) Test Setup

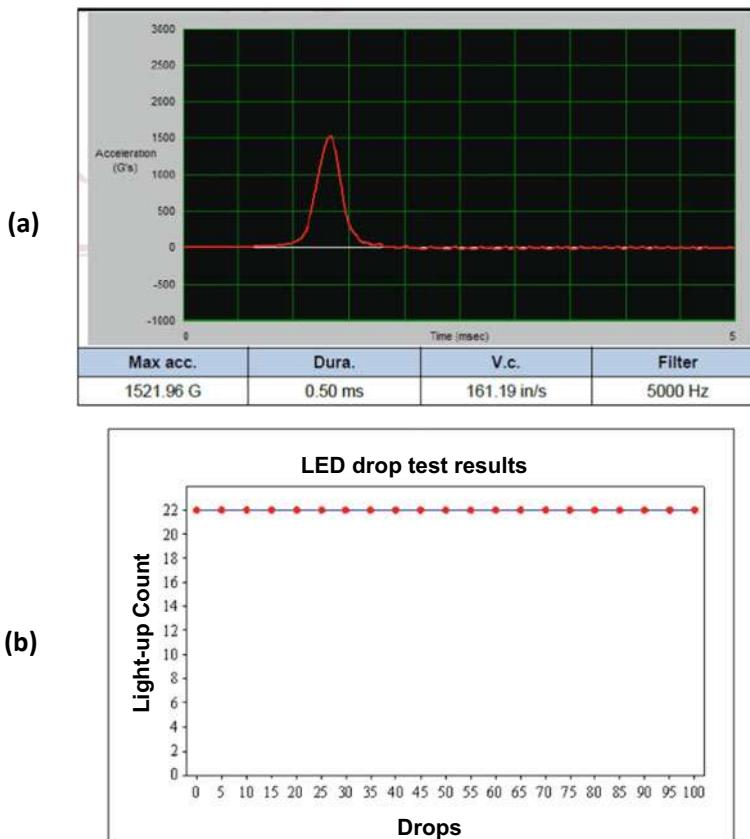
The mini-LED RGB display SMD PCB assembly is subjected to drop test. The test setup is according to JEDEC Standard JESD22-B111 as shown in Fig. 4.91. After more than 10 tries, the right height (648 mm) of the drop table is obtained, which yields the drop spectrum with 1522 G/ms (1522G and 0.5 ms half-sine pulse) as shown in Fig. 4.92a. The sample size is 22.

##### (B) Test Results

After 100 drops, the SMDs light-up very well such as that shown in Fig. 4.78b and there is no failure. However, a closer look at the cross sections of the tested samples, it is found that one of the Cu metal lines of the SMDs is almost broken (just barely contacted) as shown in Fig. 4.93.



**Fig. 4.91** Drop test setup of the mini-LED SMD PCB assembly

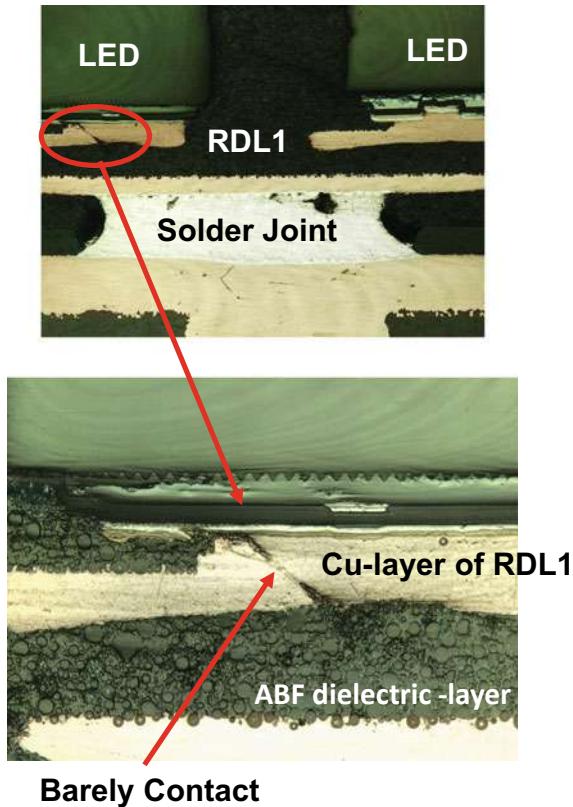


**Fig. 4.92** **a** Drop test spectrum. **b** Drop test results

#### 4.8.6 Thermal Cycling Simulation

##### (A) Structure and Kinematic Boundary Conditions

The PCB assembly of the mini-LED RGB display SMD is analyzed. Due to symmetry about the x- and y-axes as shown in Fig. 4.94, only quarter of the structure is modeled. Figure 4.95 shows the finite element model in various views for simulation. The kinematic boundary conditions are: (a) there is not displacement ( $u_x$ ) on the yz-plane and rotation about the y-axes, (b) there is not displacement ( $u_y$ ) on the xz-plane and rotation about the x-axes, and (c) the center of the bottom of PCB is fixed in the z-direction. The materials properties for simulation are shown in Table 4.4.



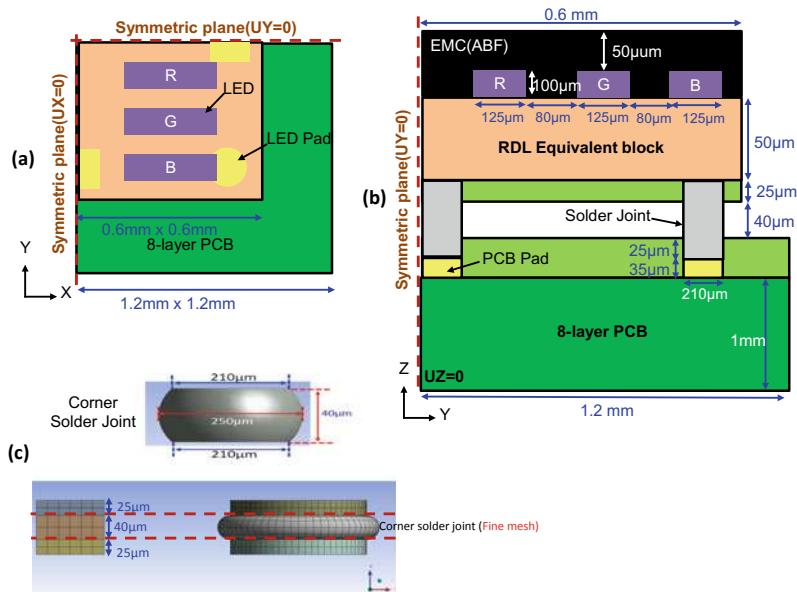
**Fig. 4.93** Sample after 100 drops. The Cu-layer of RDL1 is in barely contact

### (B) Kinetic Boundary Conditions

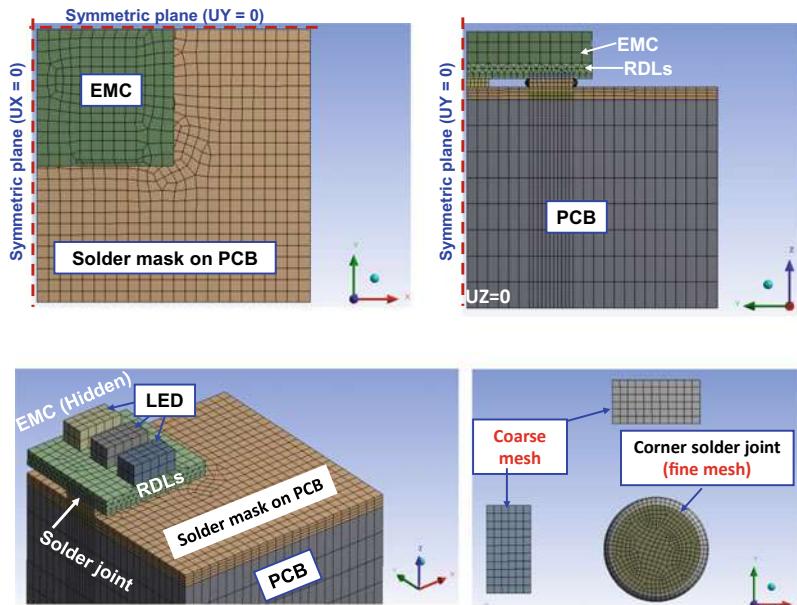
The kinetic temperature boundary condition for the simulation is shown in Fig. 4.96. It can be seen that the temperature is  $-40 \leq 85^{\circ}\text{C}$ . The cycle time is 60 min and the ramp-up, ramp-down, dwell-at-hot, and dwell-at-cold are each 15 min.

### (C) Simulation Results

The deformed shape (color contours) and the undeformed shape (dark lines) of the mini-LED RGB display SMD PCB assembly are shown in Fig. 4.97. It can be seen from Fig. 4.97b that at  $85^{\circ}\text{C}$ , the PCB expands more than the SMD and the structure is deformed in a concave shape (smiling face). It can also be seen from Fig. 4.97c that at  $-40^{\circ}\text{C}$ , the PCB shrinks more than the SMD and the structure is deformed into a convex shape (crying face). These results show that the displacement, rotation, and temperature boundary conditions are prescribed correctly.



**Fig. 4.94** **a** Quarter of structure. **b** Cross section of quarter assembly. **c** Fine meshes for corner solder joint

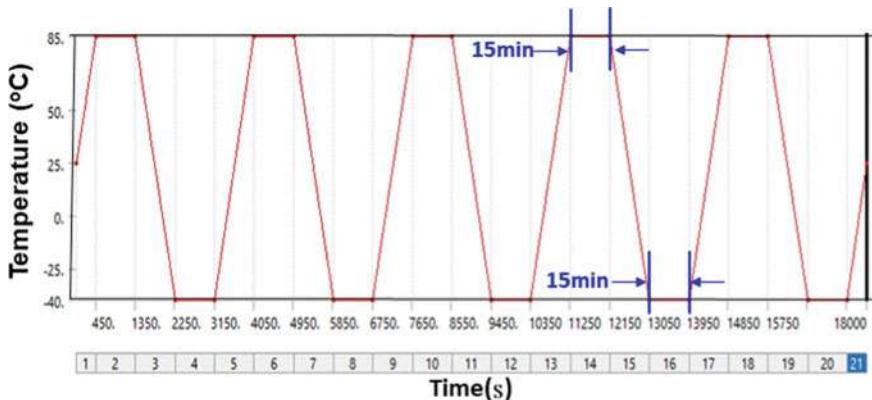


**Fig. 4.95** Finite element modeling

**Table 4.4** Materials properties for simulations

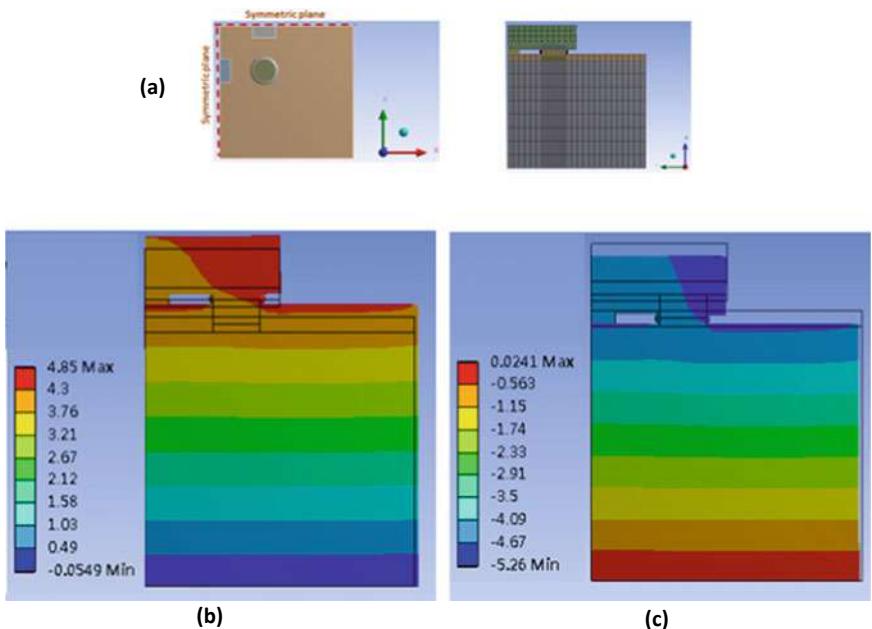
Materials	CTE ( $10^{-6}/^{\circ}\text{C}$ )	Young's modulus (GPa)	Poisson's ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Solder mask (LED)	7.0	7.0	0.3
Solder	$21 + 0.017T(^{\circ}\text{C})$	$49 - 0.07T(^{\circ}\text{C})$	0.3
EMC(ABF)	7.0	7.0	0.3
AlGaInP	5.0	103	0.31
Solder mask (PCB)	39	4.1	0.3
RDL (equiv. Block)	9.79	41.2	0.312

The constitutive eq. for solder is:  $\frac{d\varepsilon}{dt} = 500000[\sinh(0.01\sigma)]^5 \exp\left(-\frac{5800}{T}\right)$  where  $T$  is in Kelvin and  $\sigma$  is in MPa



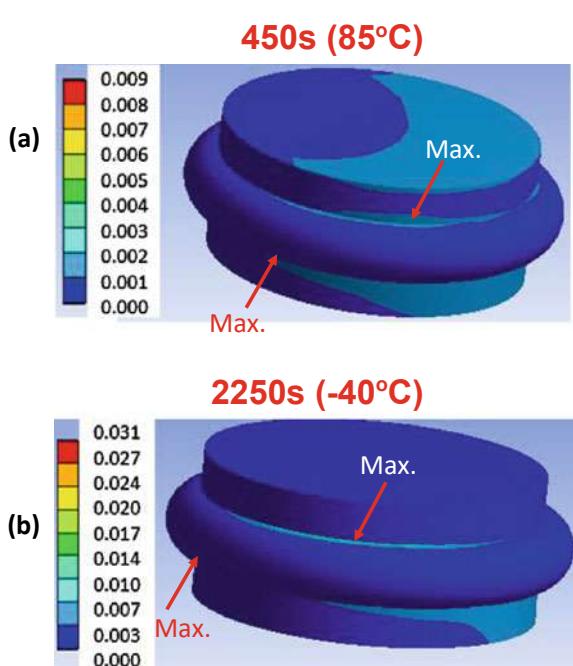
**Fig. 4.96** Temperature boundary condition

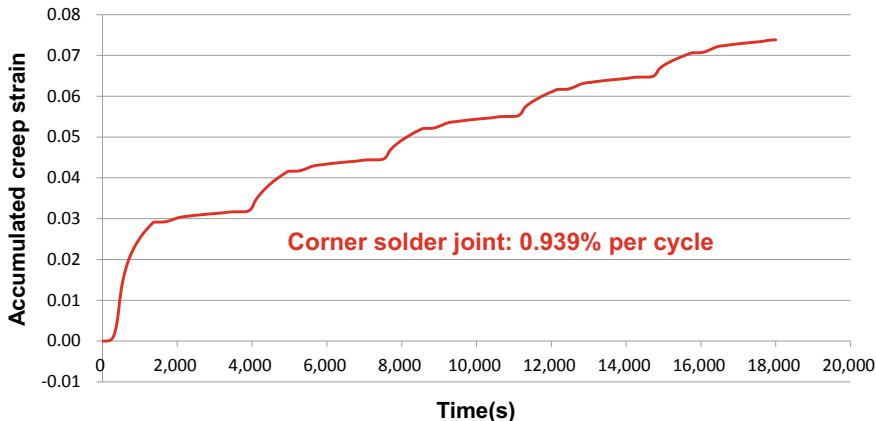
Figure 4.98 shows the maximum accumulated creep strain contours distribution, which occurs at the corner solder joint, at 450 s ( $85^{\circ}\text{C}$ ), Fig. 4.98a, and at 2250 s ( $-40^{\circ}\text{C}$ ), Fig. 4.98b. It can be seen that the maximum value occurs at a very small local area and the values of most of the other areas are very small. Figure 4.99 shows the maximum accumulated creep strain time-history at the corner solder joint. Again,



**Fig. 4.97** **a** Top-view and cross section view of the structure. **b** Deformed shape (color contours) at 450 s (85 °C). **c** Deformed shape (color contours) at 2250 s (-40 °C)

**Fig. 4.98** Accumulated creep strain at the corner solder joint. **a** At 450 s (85 °C). **b** At 2250 s (-40 °C)





**Fig. 4.99** Accumulated creep strain time-history at the corner solder joint

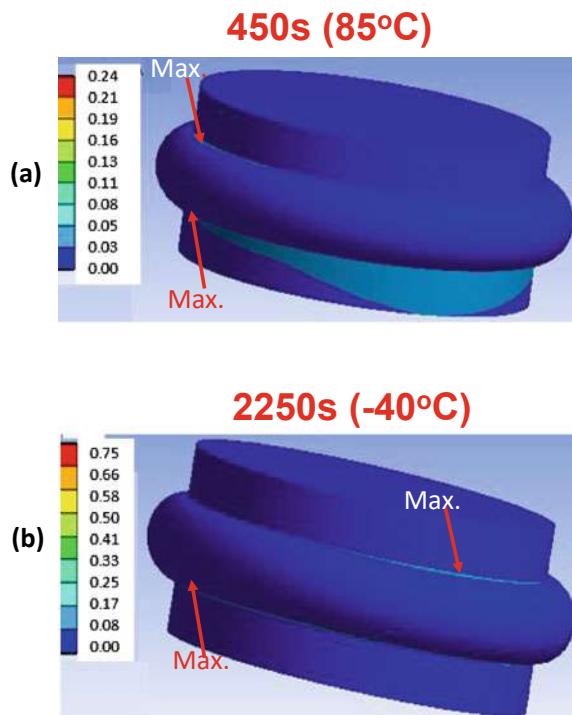
it can be seen that the maximum accumulated creep strain is very small (less than 1%).

Figure 4.100 shows the maximum creep strain energy density contour distribution, which occurs at the corner solder joint, at 450 s ( $85^{\circ}\text{C}$ ), Fig. 4.100a, and at 2250 s ( $-40^{\circ}\text{C}$ ), Fig. 4.100b. Again, it can be seen that the maximum value occurs at a very small local area and the values of most of the other areas are very small. Figure 4.101 shows the maximum creep strain energy density time-history at the corner solder joint. Again, it can be seen that the creep strain energy density per cycle is very small (less than 0.3 MPa).

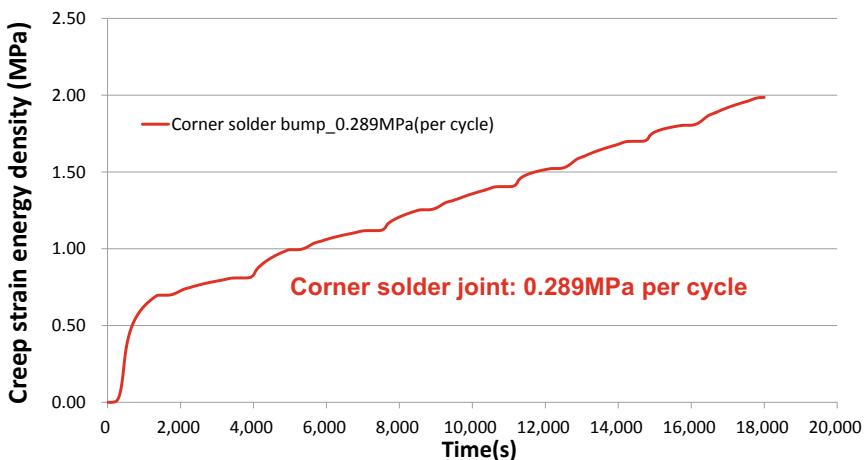
#### 4.8.7 Summary and Recommendation

Some important results and recommendation are summarized in the follows.

- The feasibility of the design, materials, process, fabrication, and reliability of a mini-LED RGB display SMD fabricated by a fan-out chip-first (face-down) panel-level packaging has been demonstrated.
- The present packaging method is not only very high throughput and high assembly yield, but potentially it is a very low-cost method.
- Low-profile SMD has been obtained with the lamination of the ABF, instead of the conventional compression of EMC.
- Reliability of the PCB assembly of the mini-LED RGB display SMD has been demonstrated by the drop test. After 100 drops and there is no failure.



**Fig. 4.100** Creep strain energy density at the corner solder joint. **a** At 450 s (85 °C). **b** At 2250 s (-40 °C)



**Fig. 4.101** Creep strain energy density time-history at the corner solder joint

- Reliability of the PCB assembly of the mini-LED RGB display SMD has been demonstrated by the thermal cycling simulation. It is found that the maximum accumulated creep strain per cycle and the creep strain energy density per cycle are too small to create reliability concerns.

## References

1. Hedler, H., T. Meyer, and B. Vasquez, "Transfer wafer level packaging," *US Patent 6,727,576*, filed on Oct. 31, 2001; patented on April 27, 2004.
2. Lau, J. H., "Patent Issues of Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 19, November/December 2015, pp. 42–46.
3. Brunnbauer, M., E. Furgut, G. Beer, T. Meyer, H. Hedler, J. Belonio, E. Nomura, K. Kiuchi, and K. Kobayashi, "An Embedded Device Technology Based on a Molded Reconfigured Wafer", *IEEE/ECTC Proceedings*, May 2006, pp. 547–551.
4. Brunnbauer, M., E. Furgut, G. Beer, and T. Meyer, "Embedded Wafer Level Ball Grid Array (eWLB)", *IEEE/EPTC Proceedings*, May 2006, pp. 1–5.
5. Keser, B., C. Amrine, T. Duong, O. Fay, S. Hayes, G. Leal, W. Lytle, D. Mitchell, and R. Wenzel, "The Redistribution Chip Package: A Breakthrough for Advanced Packaging", *Proceedings of IEEE/ECTC*, May 2007, pp. 286–291.
6. Kripesh, V., V. Rao, A. Kumar, G. Sharma, K. Houe, X. Zhang, K. Mong, N. Khan, and J. H. Lau, "Design and Development of a Multi-Die Embedded Micro Wafer Level Package", *IEEE/ECTC Proceedings*, May 2008, pp. 1544–1549.
7. Khong, C., A. Kumar, X. Zhang, S. Gaurav, S. Vempati, V. Kripesh, J. H. Lau, and D. Kwong, "A Novel Method to Predict Die Shift During Compression Molding in Embedded Wafer Level Package", *IEEE/ECTC Proceedings*, May 2009, pp. 535–541.
8. Sharma, G., S. Vempati, A. Kumar, N. Su, Y. Lim, K. Houe, S. Lim, V. Sekhar, R. Rajoo, V. Kripesh, and J. H. Lau, "Embedded Wafer Level Packages with Laterally Placed and Vertically Stacked Thin Dies", *IEEE/ECTC Proceedings*, 2009, pp. 1537–1543. Also, *IEEE Transactions on CPMT*, Vol. 1, No. 5, May 2011, pp. 52–59.
9. Kumar, A., D. Xia, V. Sekhar, S. Lim, C. Keng, S. Gaurav, S. Vempati, V. Kripesh, J. H. Lau, and D. Kwong, "Wafer Level Embedding Technology for 3D Wafer Level Embedded Package", *IEEE/ECTC Proceedings*, May 2009, pp. 1289–1296.
10. Lim, Y., S. Vempati, N. Su, X. Xiao, J. Zhou, A. Kumar, P. Thaw, S. Gaurav, T. Lim, S. Liu, V. Kripesh, and J. H. Lau, "Demonstration of High Quality and Low Loss Millimeter Wave Passives on Embedded Wafer Level Packaging Platform (EMWLP)", *IEEE/ECTC Proceedings*, 2009, pp. 508–515. Also, *IEEE Transactions on Advanced Packaging*, Vol. 33, 2010, pp. 1061–1071.
11. Lau, J. H., N. Fan, and M. Li, "Design, Material, Process, and Equipment of Embedded Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 20, May/June 2016, pp. 38–44.
12. Lau, J. H., M. Li, M. Li, T. Chen, I. Xu, X. Qing, Z. Cheng, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, P. Lo, K. Wu, J. Hao, S. Koh, R. Jiang, X. Cao, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, "Fan-Out Wafer-Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, 2018, September 2018, pp. 1544–1560.
13. Lau, J. H., M. Li, Y. Lei, M. Li, I. Xu, T. Chen, Q. Yong, Z. Cheng, K. Wu, P. Lo, Z. Li, K. Tan, Y. Cheung, N. Fan, E. Kuah, C. Xi, J. Ran, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, "Reliability of Fan-Out Wafer-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 148–162.

14. Ko, CT, H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. W. Lin, T. Chen, I. Xu, C. Chang, J. Pan, H. Wu, Q. Yong, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, K. Wu, J. Hao, R. Beica, M. Lin, Y. Chen, Z. Cheng, S. Koh, R. Jiang, X. Cao, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, "Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, September 2018, pp. 1561–1572.
15. Ko, C. T., H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. Lin, C. Chang, J. Pan, H. Wu, Y. Chen, T. Chen, I. Xu, P. Lo, N. Fan, E. Kuah, Z. Li, K. Tan, C. Lin, R. Beica, M. Lin, C. Xi, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, "Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 141–147.
16. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1–27.
17. Lau, J. H., "Recent Advances and Trends in Heterogeneous Integrations", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 16, April 2019, pp. 45–77.
18. Kurita, Y., T. Kimura, K. Shibuya, H. Kobayashi, F. Kawashiro, N. Motohashi, and M. Kawano, "Fan-out wafer-level packaging with highly flexible design capabilities," *IEEE/ECTC Proceedings*, May 2010, pp. 1–6.
19. Motohashi, N., T. Kimura, K. Mineo, Y. Yamada, T. Nishiyama, K. Shibuya, H. Kobayashi, Y. Kurita, and M. Kawano, "System in wafer-level package technology with RDL-first process," *IEEE/ECTC Proceedings*, May 2011, pp. 59–64.
20. Yoon, S., J. Caparas, Y. Lin, and P. Marimuthu, "Advanced Low Profile PoP Solution with Embedded Wafer Level PoP (eWLB-PoP) Technology", *IEEE/ECTC Proceedings*, May 2012, pp. 1250–1254.
21. Tseng, C., Liu, C., Wu, C., and D. Yu, "InFO (Wafer Level Integrated Fan-Out) Technology", *IEEE/ECTC Proceedings*, May 2016, pp. 1–6.
22. Hsieh, C., Wu, C., and D. Yu, "Analysis and Comparison of Thermal Performance of Advanced Packaging Technologies for State-of-the-Art Mobile Applications", *IEEE/ECTC Proceedings*, May 2016, pp. 1430–1438.
23. Yoon, S., P. Tang, R. Emigh, Y. Lin, P. Marimuthu, and R. Pendse, "Fanout Flipchip eWLB (Embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions", *IEEE/ECTC Proceedings*, May 2013, pp. 1855–1860.
24. Lin, Y., W. Lai, C. Kao, J. Lou, P. Yang, C. Wang, and C. Hsieh, "Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate", *IEEE/ECTC Proceedings*, May 2016, pp. 13–18.
25. Chen, N., T. Hsieh, J. Jinn, P. Chang, F. Huang, J. Xiao, A. Chou, and B. Lin, "A Novel System in Package with Fan-out WLP for high speed SERDES application", *IEEE/ECTC Proceedings*, May 2016, pp. 1495–1501.
26. Chang, H., D. Chang, K. Liu, H. Hsu, R. Tai, H. Hunag, Y. Lai, C. Lu, C. Lin, and S. Chu, "Development and Characterization of New Generation Panel Fan-Out (PFO) Packaging Technology", *IEEE/ECTC Proceedings*, May 2014, pp. 947–951.
27. Liu, H., Y. Liu, J. Ji, J. Liao, A. Chen, Y. Chen, N. Kao, and Y. Lai, "Warpage Characterization of Panel Fab-out (P-FO) Package", *IEEE/ECTC Proceedings*, May 2014, pp. 1750–1754.
28. Braun, T., S. Raatz, S. Voges, R. Kahle, V. Bader, J. Bauer, K. Becker, T. Thomas, R. Aschenbrenner, and K. Lang, "Large Area Compression Molding for Fan-out Panel Level Packing", *IEEE/ECTC Proceedings*, May 2015, pp. 1077–1083.
29. Che, F., D. Ho, M. Ding, X. Zhang, "Modeling and design solutions to overcome warpage challenge for fanout wafer level packaging (FO-WLP) technology," *IEEE/EPTC Proceedings*, May 2015, pp. 2–4.
30. Che, F., D. Ho, M. Ding, D. MinWoopp, "Study on Process Induced Wafer Level Warpage of Fan-Out Wafer Level Packaging", *IEEE/ECTC Proceedings*, May 2016, pp. 1879–1885.
31. Hsu, I., C. Chen, S. Lin, T. Yu, M. Hsieh, K. Kang, S. Yoon, "Fine-Pitch Interconnection and Highly Integrated Assembly Packaging with FOMIP (Fan-out Mediatek Innovation Package) Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 867–872.

32. Lai, W., P. Yang, I. Hu, T. Liao, K. Chen, D. Tarng, and C. Hung, "A Comparative Study of 2.5D and Fan-out Chip on Substrate : Chip First and Chip Last", *IEEE/ECTC Proceedings*, May 2020, pp. 354–360.
33. Julien, B., D. Fabrice, K. Tadashi, B. Pieter, K. Koen, P. Alain, M. Andy, P. Arnita, B. Gerald, and B. Eric, "Development of compression molding process for Fan-Out wafer level packaging", *IEEE/ECTC Proceedings*, May 2020, pp. 1965–1972.
34. Lee, K., Y. Lim, S. Chow, K. Chen, W. Choi, and S. Yoon, "Study of Board Level Reliability of eWLB (embedded wafer level BGA) for 0.35 mm Ball Pitch *IEEE/ECTC Proceedings*, May 2019, pp. 1165–1169.
35. Wu, D., R. Dahlbäck, E. Öjefors and M. Carlsson, F. Lim, Y. Lim, A. Oo, W. Choi, and S. Yoon, "Advanced Wafer Level PKG solutions for 60 GHz WiGig (802.11ad) Telecom Infrastructure", *IEEE/ECTC Proceedings*, May 2019, pp. 968–971.
36. Fowler, M., J. Massey, T. Braun, S. Voges, R. Gernhardt, and M. Wohrmann, "Investigation and Methods Using Various Release and Thermoplastic Bonding Materials to Reduce Die Shift and Wafer Warpage for eWLB Chip-First Processes", *IEEE/ECTC Proceedings*, May 2019, pp. 363–369.
37. Theuss, H., C. Geissler, F. Muehlbauer, C. Waechter, T. Kilger, J. Wagner, T. Fischer, U. Bartl, S. Helbig, A. Sigl, D. Maier, B. Goller, M. Vobl, M. Herrmann, J. Lodermeyer, and U. Krumbein, and A. Dehe, "A MEMS Microphone in a FOWLP", *IEEE/ECTC Proceedings*, May 2019, pp. 855–860.
38. Huang, C., T. Hsieh, P. Pan, M. Jhong, C. Wang, and S. Hsieh, "Comparative Study on Electrical Performance of eWLB, M-Series and Fan-Out Chip Last", *IEEE/ECTC Proceedings*, May 2018, pp. 1324–1329.
39. Ha, J., Y. Yu, and K. Cho, "Solder Joint Reliability of Double sided Assembled PLP Package", *IEEE/EPTC Proceedings*, December 2020, pp. 408–412.
40. Mei, S., T. Lim, X. Peng, C. Chong, and S. Bhattacharya, "FOWLP RF Passive Circuit Designs for 77 GHz MIMO radar applications", *IEEE/EPTC Proceedings*, December 2020, pp. 445–448.
41. Zhang, X., B. Lau, H. Chen, Y. Han, M. Jong, S. Lim, S. Lim, X. Wang, Y. Andriani, and S. Liu, "Board Level Solder Joint Reliability Design and Analysis of FOWLP", *IEEE/EPTC Proceedings*, December 2020, pp. 316–320.
42. Ho, S., S. Boon, L. Long, H. Yao, C. Choong, S. Lim, T. Lim, and C. Chong, "Double Mold Antenna in Package for 77 GHz Automotive Radar", *IEEE/EPTC Proceedings*, December 2020, pp. 257–261.
43. Jeon, Y., and R. Kumarasamy, "Impact of Package Inductance on Stability of mm-Wave Power Amplifiers", *IEEE/EPTC Proceedings*, December 2020, pp. 255–256.
44. Han, Y., T. Chai, and T. Lim, "Investigation of Thermal Performance of Antenna in Package for Automotive Radar System", *IEEE/EPTC Proceedings*, December 2020, pp. 246–250.
45. Bhardwaj, S., S. Sayeed, J. Camara, D. Vital, P. Raj, "Reconfigurable mmWave Flexible Packages with Ultra-thin Fan-Out Embedded Tunable Ceramic IPDs", *IMAPS Proceedings*, October 2019, pp. 1.1–1.4.
46. Hdizadeh, R., A. Laitinen, N. Kuusniemi, V. Blaschke, D. Molinero, E. O'Toole, and M. Pinheiro, "Low-Density Fan-Out Heterogeneous Integration of MEMS Tunable Capacitor and RF SOI Switch", *IMAPS Proceedings*, October 2019, pp. 5.1–5.5.
47. Ostholst, R., R. Santos, N. Ambrosius, D. Dunker, and J. Delrue, "Passive Die Alignment in Glass Embedded Fan-Out Packaging", *IMAPS Proceedings*, October 2019, pp. 7.1–7.5.
48. Ali, B., and M. Marshall, "Automated Optical Inspection (AOI) for FOPLP with Simultaneous Die Placement Metrology", *IMAPS Proceedings*, October 2019, pp. 8.1–8.8.
49. Ogura, N., S. Ravichandran, T. Shi, A. Watanabe, S. Yamada, M. Kathaperumal, and R. Tummala, "First Demonstration of Ultra-Thin Glass Panel Embedded (GPE) Package with Sheet Type Epoxy Molding Compound for 5G/mm-Wave Applications", *IMAPS Proceedings*, October 2019, pp. 9.1–9.7.
50. Yoon, S., Y. Lin, S. Gaurav, Y. Jin, V. Ganesh, T. Meyer, C. Marimuthu, X. Baraton, and A. Bahr, "Mechanical Characterization of Next Generation eWLB (embedded Wafer Level BGA) Packaging", *IEEE/ECTC Proceedings*, May 2011, pp. 441–446.

51. Jin, Y., J. Teyssye, X. Baraton, S. Yoon, Y. Lin, and P. Marimuthu, "Development and Characterization of Next Generation eWLB (embedded Wafer Level BGA) Packaging", *IEEE/ECTC Proceedings*, May 2012, pp. 1388–1393.
52. Osenbach, J., S. Emerich, L. Golick, S. Cate, M. Chan, S. Yoon, Y. Lin, and K. Wong, "Development of Exposed Die Large Body to Die Size Ratio Wafer Level Package Technology", *IEEE/ECTC Proceedings*, May 2014, pp. 952–955.
53. Lin, Y., E. Chong, M. Chan, K. Lim, and S. Yoon, "WLCSP + and eWLCSP in Flex-Line: Innovative Wafer Level Package Manufacturing", *IEEE/ECTC Proceedings*, May 2015, pp. 865–870.
54. Lin, Y., C. Kang, L. Chua, W. Choi, and S. Yoon, "Advanced 3D eWLB-PoP (embedded Wafer Level Ball Grid Array - Package on Package) Technology", *IEEE/ECTC Proceedings*, May 2016, pp. 1772–1777.
55. Chen, K., L. Chua, W. Choi, S. Chow, and S. Yoon, "28 nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages", *IEEE/ECTC Proceedings*, May 2017, pp. 581–586.
56. Yap, D., K. Wong, L. Petit, R. Antonicelli, and S. Yoon, "Reliability of eWLB (embedded wafer level BGA) for Automotive Radar Applications", *IEEE/ECTC Proceedings*, May 2017, pp. 1473–1479.
57. Braun, T., T. Nguyen, S. Voges, M. Wöhrmann, R. Gernhardt, K. Becker, I. Ndip D. Freimund, M. Ramelow, K. Lang, D. Schwantuschke, E. Ture, M. Pretl, S. Engels, "Fan-out Wafer Level Packaging of GaN Components for RF Applications", *IEEE/ECTC Proceedings*, May 2020, pp. 7–13.
58. Braun, T., K. Becker, O. Hoelck, S. Voges, R. Kahle, P. Graap, M. Wöhrmann, R. Aschenbrenner, M. Dreissigacker, M. Schneider-Ramelow, K. Lang, "Fan-out Wafer Level Packaging - A Platform for Advanced Sensor Packaging", *IEEE/ECTC Proceedings*, May 2019, pp. 861–867.
59. Woehrmann, M., H. Hichri, R. Gernhardt, K. Hauck, T. Braun, M. Toepper, M. Arendt, K. Lang, "Innovative Excimer Laser Dual Damascene Process for ultra-fine line multi-layer Routing with 10 µm Pitch Micro-Vias for Wafer Level and Panel Level Packaging", *IEEE/ECTC Proceedings*, May 2017, pp. 872–877.
60. Braun, T., S. Raatz, U. Maass, M. van Dijk, H. Walter, O. Holck, K.-F. Becker, M. Topper, R. Aschenbrenner, M. Wohrmann, S. Voges, M. Huhn, K.-D. Lang, M. Wietstruck, R. Scholz, A. Mai, and M. Kaynak, "Development of a Multi-Project Fan-Out Wafer Level Packaging Platform", *IEEE/ECTC Proceedings*, May 2017, pp. 1–7.
61. Braun, T., K.-F. Becker, S. Raatz, M. Minkus, V. Bader, J. Bauer, R. Aschenbrenner R. Kahle, L. Georgi, S. Voges, M. Wohrmann, K.-D. Lang, "Foldable Fan-out Wafer Level Packaging", *EEE/ECTC Proceedings*, May 2016, pp. 19–24.
62. Braun, T., K.-F. Becker, S. Voges, J. Bauer, R. Kahle, V. Bader, T. Thomas, R. Aschenbrenner, K.-D. Lang, "24" × 18" Fan-out Panel Level Packing", *EEE/ECTC Proceedings*, May 2014, pp. 940–946.
63. Braun, T., K.-F. Becker, S. Voges, T. Thomas, R. Kahle, J. Bauer, R. Aschenbrenner, K.-D. Lang, "From Wafer Level to Panel Level Mold Embedding", *EEE/ECTC Proceedings*, May 2013, pp. 1235–1242.
64. Braun, T., K.-F. Becker, S. Voges, T. Thomas, R. Kahle, V. Bader, J. Bauer, K. Piefke, R. Krüger, R. Aschenbrenner, K.-D. Lang, "Through Mold Vias for Stacking of Mold Embedded Packages", *EEE/ECTC Proceedings*, May 2011, pp. 48–54.
65. Braun, T., K.-F. Becker, L. Böttcher, J. Bauer, T. Thomas, M. Koch, R. Kahle, A. Ostmann, R. Aschenbrenner, H. Reichl, M. Bründel, J.F. Haag, and U. Scholz, "Large Area Embedding for Heterogeneous System Integration", *EEE/ECTC Proceedings*, May 2010, pp. 550–556.
66. Chiu, T., J. Wu, W. Liu, C. Liu, D. Chen, M. Shih, and D. Tarng, "A Mechanics Model for the Moisture Induced Delamination in Fan-Out Wafer-Level Package", *IEEE/ECTC Proceedings*, May 2020, pp. 1205–1211.
67. Poe, B., "An Innovative Application of Fan-Out Packaging for Test & Measurement-Grade Products", *IWLPC Proceedings*, October 2018, pp. 1.1–1.6.

68. Hadizadeh,R., A. Laitinen, D. Molinero, N. Pereira, and M. Pinheiro, “Wafer-Level Fan-Out for High-Performance, Low-cost Packaging of Monolithic RF MEMS/CMOS”, *IWLPC Proceedings*, October 2018, pp. 2.1–2.6.
69. Lianto, P., C. Tan, Q. Peng, A. Jumat, X. Dai, K. Fung, G. See, S. Chong, S. Ho, S. Soh, S. Lim, H. Chua, A. Haron, H. Lee, M. Zhang, Z. Ko, Y. San, and H. Leong, “Fine-Pitch RDL Integration for Fan-Out Wafer-Level Packaging”, *IEEE/ECTC Proceedings*, May 2020, pp. 1126–1131.
70. Ma, S, C. Wang, F. Zheng, D. Yu, H. Xie, X. Yang, L. Ma, P. Li , W. Liu , J. Yu , J. Goodelle, “Development of Wafer Level Process for the Fabrication of Advanced Capacitive Fingerprint Sensors Using Embedded Silicon Fan-Out (eSiFO®) Technology”, *IEEE/ECTC Proceedings*, May 2019, pp. 28–34.
71. Cho, J., J. Paul, S. Capecci, F. Kuechenmeister, T. Cheng, “Experiment of 22FDX® Chip Board Interaction (CBI) in Wafer Level Packaging Fan-Out (WLPFO)”, *IEEE/ECTC Proceedings*, May 2019, pp. 910–916.
72. Weichert, J., J. Weichert, A. Erhart, K. Viehweger, “Preconditioning Technologies for Sputtered Seed Layers in FOPLP”, *IEEE/ECTC Proceedings*, May 2019, pp. 1833–1841.
73. Liu, C., et al., “High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration,” *Proc. IEEE Int. Electron Devices Meeting*, December 2012, pp. 323–326.
74. Chen, S., D. Yu, et al., “High-performance inductors for integrated fan-out wafer level packaging (InFO-WLP),” *Symp. on VLSI Technol.*, June 2013, pp. T46–T47.
75. Tsai, C., et al., “Array antenna integrated fan-out wafer level packaging (InFO-WLP) for millimeter wave system applications,” *Proc. IEEE Int. Electron Devices Meeting*, June 2013, pp. 25.1.1–25.1.4.
76. Yu, D., “New system-in-package (SIP) integration technologies,” *Proc. Custom Integrated Circuits Conf.*, September 2014, pp. 1–6.
77. Yu, D., “A new integration technology platform: integrated fan-out wafer-level-packaging for mobile applications,” *Symp. on VLSI Technol.*, June 2015, pp. T46–T47.
78. Tsai, C., et al., “High performance passive devices for millimeter wave system integration on integrated fan-out (InFO) wafer level packaging technology,” in *Proc. International Electron Devices Meeting*, Dec. 2015, pp. 25.2.1–25.2.4.
79. Wang, C., et al., “Power saving and noise reduction of 28 nm CMOS RF system integration using integrated fan-out wafer level packaging (InFO-WLP) technology,” in *Proc. International 3D Systems Integration Conference*, Aug. 2015, pp. TS6.3.1–TS6.3.4.
80. Rogers, B. D. Sanchez, C. Bishop, C. Sandstrom, C. Scanlan and T. Olson, “Chips “Face-up” Panelization Approach for Fan-Out Packaging”, *Proceedings of IWLPC*, October 2015, pp. 1–8.
81. Wang, C., and D. Yu, “Signal and Power Integrity Analysis on Integrated Fan-out PoP (InFO\_PoP) Technology for Next Generation Mobile Applications”, *IEEE/ECTC Proceedings*, May 2016, pp. 380–385.
82. Hsu, C., C Tsai, J. Hsieh, K. Yee, C. Wang, and D. Yu, “High Performance Chip-Partitioned Millimeter Wave Passive Devices on Smooth and Fine Pitch InFO RDL”, *IEEE/ECTC Proceedings*, May 2017, pp. 254–259.
83. Lau, J. H., M. Li, D. Tian, N. Fan, E. Kuah, K. Wu, M. Li, J. Hao, Y. Cheung, Z. Li, K. Tan, R. Beica, T. Taylor, CT Lo, H. Yang, Y. Chen, S. Lim, NC Lee, J. Ran, X. Cao, S. Koh, and Q. Young, “Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT*, Vol. 7, Issue 10, October 2017, pp. 1729–1738.
84. Lau, J. H., M. Li, N. Fan, E. Kuah, Z. Li, K. Tan, T. Chen, I. Xu, M. Li, Y. Cheung, K. Wu, J. Hao, R. Beica, T. Taylor, C. Ko, H. Yang, Y. Chen, S. Lim, N. Lee, J. Ran, K. Wee, Q. Yong, C. Xi, M. Tao, J. Lo, and R. Lee, “Fan-Out Wafer-Level Packaging (FOWLP) of Large Chip with Multiple Redistribution Layers (RDLs)”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 14, Issue: 4, October 2017, pp. 123–131.

85. Lau, J. H., M. Li, Q. Li, I. Xu, T. Chen, Z. Li, K. Tan, X. Qing, C. Zhang, K. Wee, R. Beica, C. Ko, S. Lim, N. Fan, E. Kuah, K. Wu, Y. Cheung, E. Ng, X. Cao, J. Ran, H. Yang, Y. Chen, N. Lee, M. Tao, J. Lo, and R. Lee, "Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*, Vol. 8, Issue 6, June, 2018, pp. 991–1002.
86. Lau, J. H., M. Li, D. Tian, N. Fan, E. Kuah, K. Wu, M. Li, J. Hao, K. Cheung, Z. Li, K. Tan, R. Beica, C. Ko, Y. Chen, S. Lim, N. Lee, K. Wee, J. Ran, and C. Xi, "Warpage Measurements and Characterizations of FOWLP with Large Chips and Multiple RDLs", *IEEE Transactions on CPMT*, Vol. 8, Issue 10, October 2018, pp. 1729–1737.
87. Wang, C., T. Tang, C. Lin, C. Hsieh, C. Tsai, K. Wu, H. Pu, and D. Yu, "InFO\_AiP Technology for High Performance and Compact 5G Millimeter Wave System Integration", *IEEE/ECTC Proceedings*, May 2018, pp. 202–207.
88. Yu, C., L. Yen, C. Hsieh, J. Hsieh, V. Chang, C. Hsieh, C. Liu, C. Wang, K. Yee, and D. Yu, "High Performance, High Density RDL for Advanced Packaging", *IEEE/ECTC Proceedings*, May 2018, pp. 587–593.
89. Su, A., T. Ku, C. Tsai, K. Yee, and D. Yu, "3D-MiM (MUST-in-MUST) Technology for Advanced System Integration", *IEEE/ECTC Proceedings*, May 2019, pp. 1–6.
90. Wang, C., J. Hsieh, V. Chang, S. Huang, T. Ko, H. Pu, and D. Yu, "Signal Integrity of Submicron InFO Heterogeneous Integration for High Performance Computing Applications", *IEEE/ECTC Proceedings*, May 2019, pp. 688–694.
91. Chen, F., M. Chen, W. Chiou, D. Yu, "System on Integrated Chips (SoIC<sup>TM</sup>) for 3D Heterogeneous Integration" *IEEE/ECTC Proceedings*, May 2019, pp. 594–599.
92. Hou, S., K. Tsai, M. Wu, M. Ku, P. Tsao, and L. Chu, "Board level Reliability Investigation of FO-WLP Package", *IEEE/ECTC Proceedings*, May 2018, pp. 904–910.
93. Chun, S., T. Kuo, H. Tsai, C. Liu, C. Wang, J. Hsieh, T. Lin, T. Ku, D. Yu, "InFO\_SoW (System-on-Wafer) for High Performance Computing", *IEEE/ECTC Proceedings*, May 2020, pp. 1–6.
94. Ko, T., H. Pu, Y. Chiang, H. Kuo, C. Wang, C. Liu, and D. Yu, "Applications and Reliability Study of InFO\_UHD (Ultra-High-Density) Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 1120–1125.
95. Kurita, Y., K. Soejima, K. Kikuchi, M. Takahashi, M. Tago, M. Koike, "A Novel "SMAFTI" Package for Inter-Chip Wide-Band Data Transfer", *IEEE/ECTC Proceedings*, May 2006, pp. 289–297.
96. Kawano, M., S. Uchiyama, Y. Egawa, N. Takahashi, Y. Kurita, K. Soejima, "A 3D Packaging Technology for 4 Gbit Stacked DRAM with 3 Gbps Data Transfer", *IEEE/EMT Proceedings*, May 2006, pp. 581–584.
97. Kurita, Y., S. Matsui, N. Takahashi, K. Soejima, M. Komuro, M. Itou, "A 3D Stacked Memory Integrated on a Logic Device Using SMAFTI Technology", *IEEE/ECTC Proceedings*, May 2007, pp. 821–829.
98. Kawano, M., N. Takahashi, Y. Kurita, K. Soejima, M. Komuro, and S. Matsui, "A 3-D Packaging Technology for Stacked DRAM with 3 Gb/s Data Transfer", *IEEE Transactions on Electron Devices*, 55 (7), 2008, pp. 1614–1620.
99. Motohashi, N., Y. Kurita, K. Soejima, Y. Tsuchiya, and M. Kawano, "SMAFTI Package with Planarized Multilayer Interconnects", 2009, *IEEE/ECTC Proceedings*, May 2009, pp. 599–606.
100. Kurita, M., S. Matsui, N. Takahashi, K. Soejima, M. Komuro, M. Itou, "Vertical Integration of Stacked DRAM and High-Speed Logic Device Using SMAFTI Technology", *IEEE Transactions on Advanced Packaging*, May 2009, pp. 657–665.
101. Kurita, Y., N. Motohashi, S. Matsui, K. Soejima, S. Amakawa, K. Masu, "SMAFTI Packaging Technology for New Interconnect Hierarchy", *Proceedings of IITC*, June 2009, pp. 220–222.
102. Kurita, Y., T. Kimura, K. Shibuya, H. Kobayashi, F. Kawashiro, N. Motohashi, "Fan-Out Wafer Level Packaging with Highly Flexible Design Capabilities", *Proceedings of the Electronics System Integration Technology Conferences*, 2010, pp. 1–6.

103. Motohashi, N., T. Kimura, K. Mineo, Y. Yamada, T. Nishiyama, K. Shibuya, “System in a Wafer Level Package Technology with RDL-First Process”, *IEEE/ECTC Proceedings*, May 2011, pp. 59–64.
104. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
105. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.
106. Huemoeller, R., and C. Zwenger, “Silicon wafer integrated fan-out technology,” *Chip Scale Review*, Mar/Apr 2015, pp. 34–37.
107. Bu, L., F. Che, M. Ding, S. Chong, and X. Zhang, “Mechanism of Moldable Underfill (MUF) Process for Fan-Out Wafer Level Packaging”, *IEEE/EPTC Proceedings*, May 2015, pp. 1–7.
108. Che, F., D. Ho, M. Ding, and D. Woo, “Study on Process Induced Wafer Level Warpage of Fan-Out Wafer Level Packaging”, *IEEE/ECTC Proceedings*, May 2016, pp. 1879–1885.
109. Rao, V., C. Chong, D. Ho, D. Zhi, C. Choong, S. Lim, D. Ismael, and Y. Liang, “Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multi-layer Fine Pitch RDL for Mobile Applications”, *IEEE/ECTC Proceedings*, May 2016, pp. 1522–1529.
110. Chen, Z., F. Che, M. Ding, D. Ho, T. Chai, V. Rao, “Drop Impact Reliability Test and Failure Analysis for Large Size High Density FOWLP Package on Package”, May 2017, *IEEE/ECTC Proceedings*, 2017, pp. 1196–1203.
111. Lim, T., and D. Ho, “Electrical design for the development of FOWLP for HBM integration”, *IEEE/ECTC Proceedings*, May 2018, pp. 2136–2142.
112. Ho, S., H. Hsiao, S. Lim, C. Choong, S. Lim, and C. Chong, “High Density RDL build-up on FO-WLP using RDL-first Approach”, *IEEE/EPTC Proceedings*, December 2019, pp. 23–27.
113. Boon, S., D. Wee, R. Salahuddin, and R. Singh, “Magnetic Inductor Integration in FO-WLP using RDL-first Approach”, *IEEE/EPTC Proceedings*, December 2019, pp. 18–22.
114. Hsiao, H., S. Ho, S. S. Lim, W. Ching, C. Choong, S. Lim, H. Hong, and C. Chong, “Ultra-thin FO Package-on-Package for Mobile Application”, *IEEE/ECTC Proceedings*, May 2019, pp. 21–27.
115. Lin, B., F. Che, V. Rao, and X. Zhang, “Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging (FOPLP)”, *IEEE/ECTC Proceedings*, May 2019, pp. 1152–1158.
116. Sekhar, V., V. Rao, F. Che, C. Choong, and K. Yamamoto, “RDL-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging”, *IEEE/ECTC Proceedings*, May 2019, pp. 2126–2133.
117. Ma, M., S. Chen, P.I. Wu, A. Huang, C.H. Lu, A. Chen, C. Liu, and S. Peng, “The Development and the Integration of the 5  $\mu\text{m}$  to 1  $\mu\text{m}$  Half Pitches Wafer Level Cu Redistribution Layers”, *IEEE/ECTC Proceedings*, May 2016, pp. 1509–1614.
118. Kim, Y., J. Bae, M. Chang, A. Jo, J. Kim, S. Park, D. Hiner, M. Kelly, and W. Do, “SLIM™, High Density Wafer Level Fan-out Package Development with Submicron RDL”, *IEEE/ECTC Proceedings*, December 2017, pp. 18–13.
119. Hiner, D., M. Kolbehdari, M. Kelly, Y. Kim, W. Do, J. Bae, M. Chang, and A. Jo, “SLIM™ Advanced Fan-out Packaging for High Performance Multi-die Solutions”, *IEEE/ECTC Proceedings*, May 2017, pp. 575–580.
120. Lin, B., C. Ko, W. Ho, C. Kuo, K. Chen, Y. Chen, and T. Tseng, “A Comprehensive Study on Stress and Warpage by Design, Simulation and Fabrication of RDL-First Panel Level Fan-Out Technology for Advanced Package”, *IEEE/ECTC Proceedings*, May 2017, pp. 1413–1418.
121. Suk, K., S. Lee, J. Youn, K. Lee, H. Kim, S. Lee, P. Kim, D. Kim, D. Oh, and J. Byun, “Low Cost Si-less RDL Interposer Package for High Performance Computing Applications”, *IEEE/ECTC Proceedings*, May 2018, pp. 64–69.
122. Hwang, T., D. Oh, E. Song, K. Kim, J. Kim, and S. Lee, “Study of Advanced Fan-Out Packages for Mobile Applications”, *IEEE/ECTC Proceedings*, May 2018, pp. 343–348.
123. Lee, C., J. Su, X. Liu, Q. Wu, J. Lin, P. Lin, C. Ko, Y. Chen, W. Shen, T. Kou, S. Huang, A. Lin, Y. Lin, and K. Chen, “Optimization of laser release process for throughput enhancement of fan-out wafer level Packaging”, *IEEE/ECTC Proceedings*, May 2018, pp. 1818–1823.
124. Cheng, W., C. Yang, J. Lin, W. Chen, T. Wang, and Y. Lee, “Evaluation of Chip-last Fan-out Panel Level Packaging with G2.5 LCD Facility using FlexUPTM and Mechanical De-bonding Technologies”, *IEEE/ECTC Proceedings*, May 2018, pp. 386–391.

125. Cheng, S., C. Yang, W. Cheng, S. Cheng, W. Chen, H. Lai, T. Wang, and Y. Lee, "Application of Fan-Out Panel Level Packaging Techniques for Flexible Hybrid Electronics Systems", *IEEE/ECTC Proceedings*, May 2019, pp. 1877–1822.
126. Chang, K., C. Huang, H. Kuo, M. Jhong, T. Hsieh, M. Hung, and C. Wan, "Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity", *IEEE/ECTC Proceedings*, May 2019, pp. 41–46.
127. Lin, Y., M. Yew, M. Liu, S. Chen, T. Lai, P. Kayle, C. Lin, T. Fang, C. Chen, C. Yu, K. Lee, C. Hsu, P. Lin, F. Hsu, and S. Jeng, "Multilayer RDL Interposer for Heterogeneous Device and Module Integration", *EEE/ECTC Proceedings*, 2019, pp. 931–936.
128. Miki, S., H. Taneda, N. Kobayashi, K. Oi, K. Nagai, and T. Koyama, "Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder", *IEEE/ECTC Proceedings*, May 2019, pp. 1599–1604.
129. Murayama, K., S. Miki, H. Sugahara, K. Oi, "Electro-migration evaluation between organic interposer and build-up substrate on 2.3D organic package", *IEEE/ECTC Proceedings*, May 2020, pp. 716–722.
130. Lau, J. H., C. Ko, K. Yang, C. Peng, T. Xia, B. Lin, J. J. Chen, P. Huang, H. Liu, T. Tseng, E. Lin, and L. Chang, "Panel-Level Fan-Out RDL-First Packaging for Heterogeneous Integration" *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125–1137.
131. Lau, J. H., C. Ko, T. Peng, K. Yang, T. Xia, P. Lin, J. Chen, P. Huang, T. Tseng, E. Lin, L. Chang, C. Lin, and W. Lu, "Chip-Last (RDL-First) Fan-Out Panel-Level Packaging (FOPLP) for Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 17, No. 3, October 2020, pp. 89–98.
132. Takahashi, N., Y. Susumago, S. Lee, Y. Miwa, H. Kino, T. Tanaka, T. Fukushima, "RDL-first Flexible FOWLP Technology with Dielets Embedded in Hydrogel", *IEEE/ECTC Proceedings*, May 2020, pp. 811–816.
133. Scott, G., J. Bae, K. Yang, W. Ki, N. Whitchurch, M. Kelly, C. Zwenger, J. Jeon, "Heterogeneous Integration Using Organic Interposer Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 885–892.
134. Son, S., D. Khim, S. Yun, J. Park, E. Jeong, J. Yi, J. Yoo, K. Yang, M. Yi, S. Lee, W. Do, and J. Khim, "A New RDL-First PoP Fan-Out Wafer-Level Package Process with Chip-to-Wafer Bonding Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 1910–1915.
135. Mok, I., J. Bae, W. Ki, H. Yoo, S. Ryu, S. Kim, G. Jung, T. Hwang, and W. Do, "Wafer Level Void-Free Molded Underfill for High-Density Fan-out Packages", *IEEE/EPTC Proceedings*, December 2020, pp. 419–424.
136. Chong, S., V. Rao, K. Yamamoto, S. Lim, and S. Huang, "Development of RDL-1st Fan-Out Panel-Level Packaging (FO-PLP) on 550 mm × 650 mm size panels", *IEEE/EPTC Proceedings*, December 2020, pp. 425–429.
137. Rotaru, M., and K. Li, "Electrical characterization and design of hyper-dense interconnect on HD-FOWLP for die to die connectivity for AI and ML accelerator applications", *IEEE/EPTC Proceedings*, December 2020, pp. 430–434.
138. Lim, S., N. Jaafar, S. Chong, S. Lim, and T. Chai, "Development of wafer level solder ball placement process for RDL-first", *FOWLP IEEE/EPTC Proceedings*, December 2020, pp. 435–439.
139. Chai, T., D. Ho, S. Chong, H. Hsiao, S. Soh, S. Lim, S. Lim, E. Wai, B. Lau, W. Seit, G. Lau, T. Phua, K. Lim, S. Lim, Y. Ye, "Fan-Out Wafer Level Packaging Development Line", *IEEE/EPTC Proceedings*, December 2020, pp. 440–444.
140. Boon, S., W. Ho, S. Boon, S. Lim, R. Singh, and S. Raju, "Fan-Out Packaging with Thin-film Inductors", *IEEE/EPTC Proceedings*, December 2020, pp. 449–452.
141. Ji, L., T. Chai, G. See, and P. Suo, "Modelling and prediction on process dependent wafer warpage for FOWLP technology using finite element analysis and statistical approach", *IEEE/EPTC Proceedings*, December 2020, pp. 386–393.
142. Sayeed, S., D. Wilding, J. Camara, D. Vital, S. Bhardwaj, and P. Raj, "Deformable Interconnects with Embedded Devices in Flexible Fan-Out Packages", *IMAPS Proceedings*, October 2019, pp. 8.1–8.6.

143. Boulanger, R., J. Hander, and R. Moon, "Innovative Panel Plating for Heterogeneous Integration", *IMAPS Proceedings*, October 2019, pp. 8.7–8.11.
144. Fang, J., M. Huang, H. Tu, W. Lu, P. Yang, "A Production-worthy Fan-Out Solution – ASE FOCoS Chip Last", *IEEE/ECTC Proceedings*, May 2020, pp. 290–295.
145. Lin, J., C. Chung, C. Lin, A. Liao, Y. Lu, J. Chen, D. Ng, "Scalable Chiplet package using Fan-Out Embedded Bridge", *IEEE/ECTC Proceedings*, May 2020, pp. 14–18.
146. Wang, T., H. Lai, Y. Chung, C. Feng, L. Chang, J. Yang, T. Yu, S. Yan, Y. Lee, and S. Chiu, "Functional RDL of FOPLP by Using LTPS-TFT Technology for ESD protection Application", *IEEE/ECTC Proceedings*, May 2020, pp. 25–30.
147. Chong, S., E. Ching, S. Lim, S. Boon, T. Chai, "Demonstration of Vertically Integrated POP using FOWLP Approach", *IEEE/ECTC Proceedings*, May 2020, pp. 873–878.
148. Podpod, A., A. Phommahaxay, P. Bex, J. Slabbeekoor, J. Bertheau, A. Salahouelhadj, E. Sleckx, A. Miller, G. Beyer, E. Beyne, A. Guerrero, K. Yess, K. Arnold, "Advances in Temporary Carrier Technology for High-Density Fan-Out Device Build-up", *IEEE/ECTC Proceedings*, May 2019, pp. 340–345.
149. Elmogi, A., A. Desmet, J. Missinne, H. Ramon, J. Lambrecht, P. Heyn, M. Pantouvaki, J. Campenhout, J. Bauwelinck, and G. Steenberge, "Adaptive Patterning of Optical and Electrical Fan-out for photonic chip packaging", *IEEE/ECTC Proceedings*, May 2019, pp. 1757–1763.
150. Chen, D., I. Hu, K. Chen, M. Shih, D. Tarng, D. Huang, J. On, "Material and Structure Design Optimization for Panel-Level Fan-Out Packaging", *IEEE/ECTC Proceedings*, May 2019, pp. 1710–1715.
151. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joint*, Springer, New York, 2020.
152. Lau, J. H., State of the Art of Lead-Free Solder Joint Reliability, *ASME Transactions, Journal of Electronic Packaging*, June 2021, Vol. 143, pp. 1–21.
153. Pan, N., G. Henshall, F. Billaut, S. Dai, M. Strum, R. Lewis, E. Benedetto, and J. Rayner, "An Acceleration Model for Sn-Ag-Cu Solder Joint Reliability under Various Thermal Cycle Conditions", *SMTA International Conference Proceedings*, September 2005, pp. 876–883.
154. Lall, P., A. Shirgaokar, and D. Arunachalam, "Norris-Landzberg Acceleration Factor and Goldmann Constants for SAC305 Lead-Free Electronics", *ASME Transactions, Journal of Electronic Packaging*, Vol. 134, September 2012, pp. 1–8.
155. Osterman, M., "Modeling Temperature Cycle Fatigue Life of Select SAC Solders", *SMTA International Conference*, September 2018.
156. Lau, J. H., R. Lee, M. Yuen, and P. Chan, "3D LED and IC Wafer Level Packaging", *Journal of Microelectronics International*, Vol. 27, Issue 2, 2010, pp. 98–105.
157. Chen, Y., "Latest Mini LED and Micro LED Definition and Technology Analysis", *LED Inside*, July 2020.
158. Han, S., "MSI to Launch Gaming Notebook Backlit by Lextar-Made Mini-LED", *Digitimes*, April 2020.
159. Chen, M., "Taiwan Suppliers to Play Major Role in Apple Mini-LED Offerings in 2021", *Digitimes*, November 2020.
160. Yoon, G., "Samsung Electronics Preparing for Mass-Production of Mini-LED TVs", *Korea IT News*, November 2020.
161. Lau, J. H., *Chip On Board Technologies for Multichip Modules*, Van Nostrand Reinhold, New York, 1994.
162. Lau, J. H., C. T. Ko, C. Lin, T. Tseng, K. Yang, T. Xia, P. Lin, C. Peng, E. Lin, L. Chang, N. Liu, S. Chiu, and Z. N. Lee, "Design, Materials, Process, Fabrication, and Reliability of Mini-LED RGB Display by Fan-Out Panel-Level Packaging", *IEEE/ECTC Proceedings*, May 2021.

# Chapter 5

## 2D, 2.1D, and 2.3D IC Integration



### 5.1 Introduction

In this chapter, 2D, 2.1D, and 2.3D IC integrations will be discussed. In 2D IC integration, wire bonding, flip chip, a mix of wire bonding and flip chip, fan-out with chip-first, fan-out with chip-last, and fan-out with chip-last on hybrid RDLs (redistribution-layers) will be presented. In 2.1D IC integration, thin-film layers on build-up package substrate (also embed bridge in build-up substrate and embed bridge in fan-out epoxy molding compound (EMC)) will be discussed. In 2.3D IC integration, there are two groups, namely coreless organic interposer on build-up package substrate and fan-out (both chip-first and chip-last) RDL interposer on build-up package substrate, and they will be presented. There are not TSVs (through-silicon vias, which will be discussed in Chap. 6) for 2D, 2.1D, and 2.3D IC integrations.

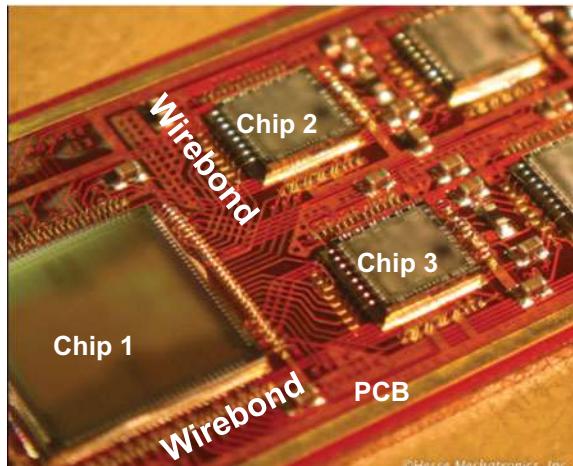
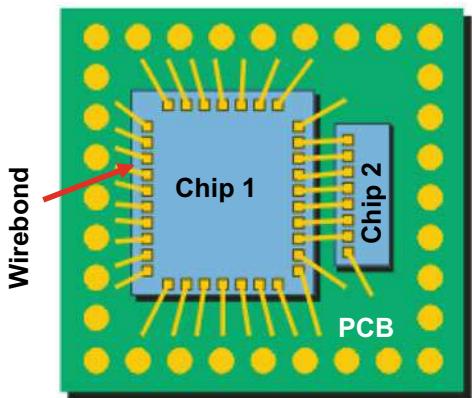
### 5.2 2D IC Integration—Wire Bonding

Figure 5.1 shows an example of multichip with wire bonding technology on a package substrate or PCB (printed circuit board). It can be seen that the chips are attached side-by-side on the same substrate.

### 5.3 2D IC Integration—Flip Chip

Figure 5.2 shows an example of multichip with flip chip technology on a package substrate and then on a PCB. It can be seen that the chips are flipped and attached side-by-side on the same package substrate.

**Fig. 5.1** Multichip with wire bonding



#### 5.4 2D IC Integration—Wire Bonding and Flip Chip

Figure 5.3 schematically shows an example of multichip with both wire bonding and flip chip technologies. It can be seen that the IC chip is solder bumped flip chip on the package substrate. Also there is the MEMS (micro-electro-mechanical system) chip, which is wired bonding on the same substrate.

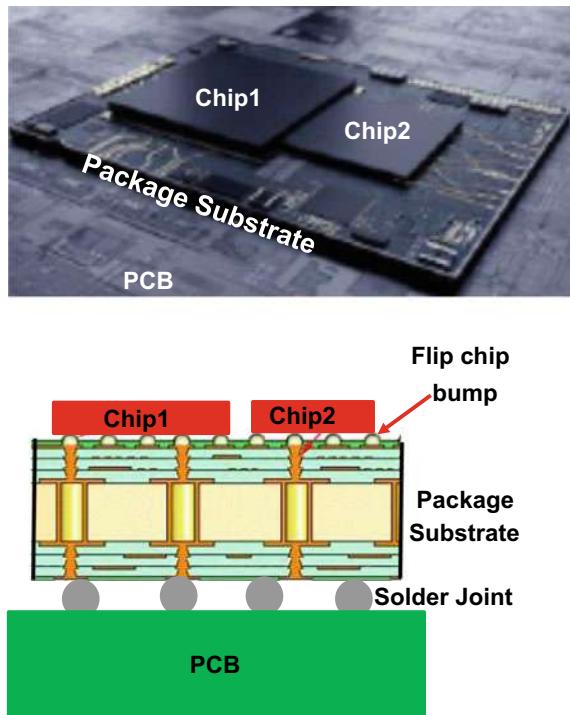


Fig. 5.2 Multichip with flip chip

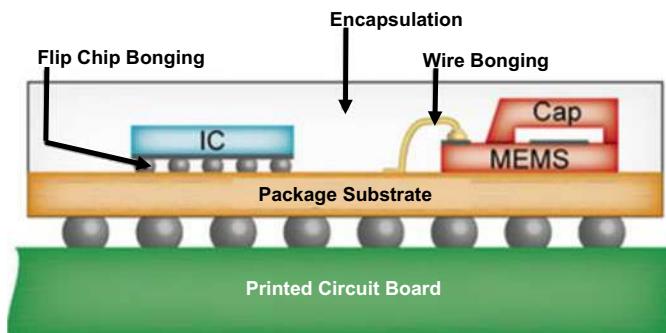


Fig. 5.3 Multichip with wire bonding and flip chip

## 5.5 RDLs

As shown in Chap. 4 that the heart of fan-out technology is RDLs. There are at least three different kinds of fan-out RDLs, namely organic RDLs, inorganic RDLs, and hybrid RDLs.

### 5.5.1 *Organic RDLs*

The RDLs fabricated by polymer (either photosensitive or not) for the dielectric layer and ECD (electrochemical deposition) Cu + etching for the metal conductor layer either for chip-first as shown in Sect. 4.2.7 or chip-last as shown in Sect. 4.7.4 are called organic RDLs [1–3]. The metal line width and spacing (L/S) of the organic RDLs are usually  $\geq 2 \mu\text{m}$  (for chip-last) and  $\geq 5 \mu\text{m}$  (for chip-first).

### 5.5.2 *Inorganic RDLs*

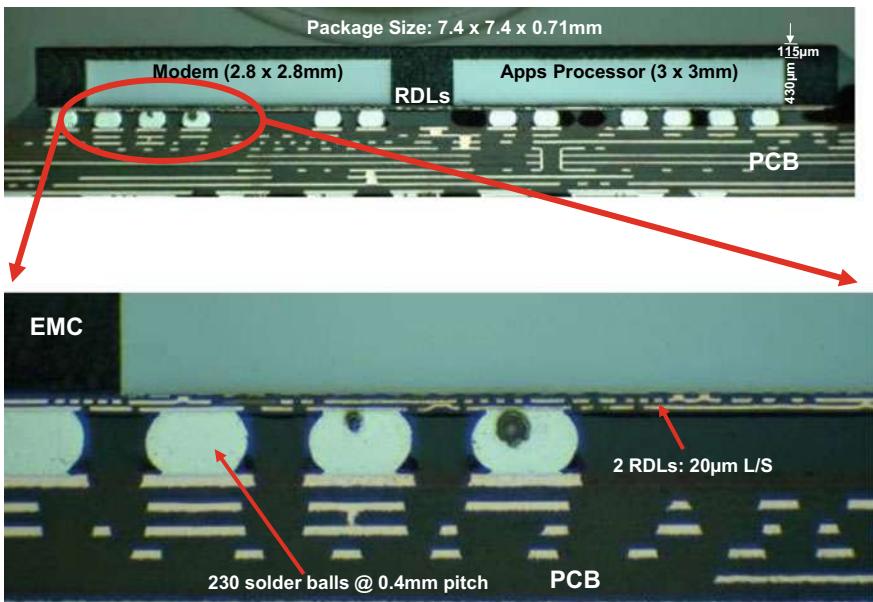
For L/S < 2  $\mu\text{m}$ , the dielectric layer of the RDL is fabricated by PECVD (plasma enhanced chemical vapor deposition) and the metal layer of the RDL is fabricated by Cu-Damascene + CMP (chemical-mechanical polishing). This is the oldest backend semiconductor process. This process uses SiO<sub>2</sub> or SiN for the dielectric layer and ECD to deposit the Cu on the whole wafer. That is followed by using CMP to remove the overburden Cu and seed layer to make the Cu conductor layer of the RDLs. The key process steps have been shown in [1–3]. The RDLs made by PECVD and Cu-damascene + CMP are called inorganic RDLs. The metal L/S of the inorganic RDLs can go down to submicron.

### 5.5.3 *Hybrid RDLs*

A combination of inorganic RDLs and organic RDLs is called hybrid RDLs. The key process steps are [1–3]: (a) first, a temporary glass carrier is coated with a sacrificial layer, (b) the first RDL is then fabricated by the PECVD for the SiO<sub>2</sub> dielectric layer and dual Cu-damascene + CMP for the conductor layer (inorganic RDL), and (c) the remaining RDLs are fabricated by the polymer (either photosensitive or not) and Cu-plating + etching method (organic RDL). The metal L/S of the hybrid RDLs can go down to submicron.

## 5.6 2D IC Integration—Fan-Out (Chip-First)

There are many examples on 2D IC integration with fan-out (chip-first) packaging technology [4–16]. In this section, two examples are given.



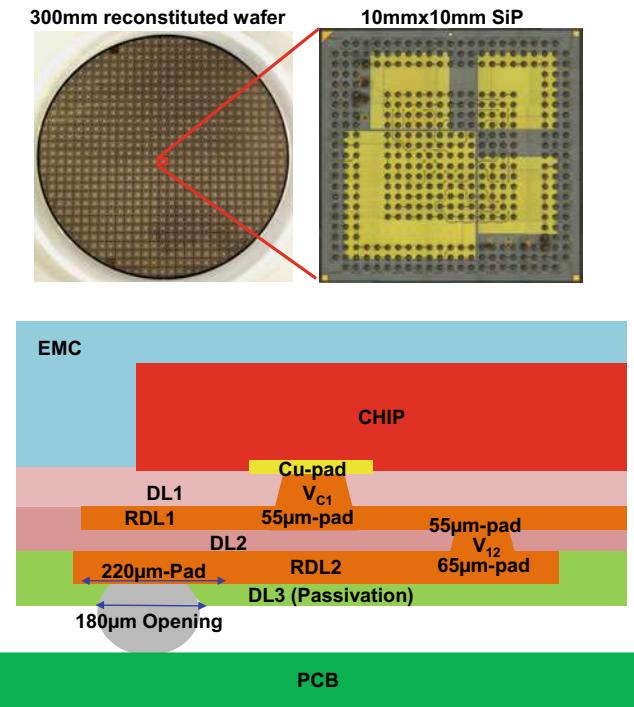
**Fig. 5.4** HTC's multichip with fan-out (chip-first) packaging

### 5.6.1 HTC's *Desire 606 W*

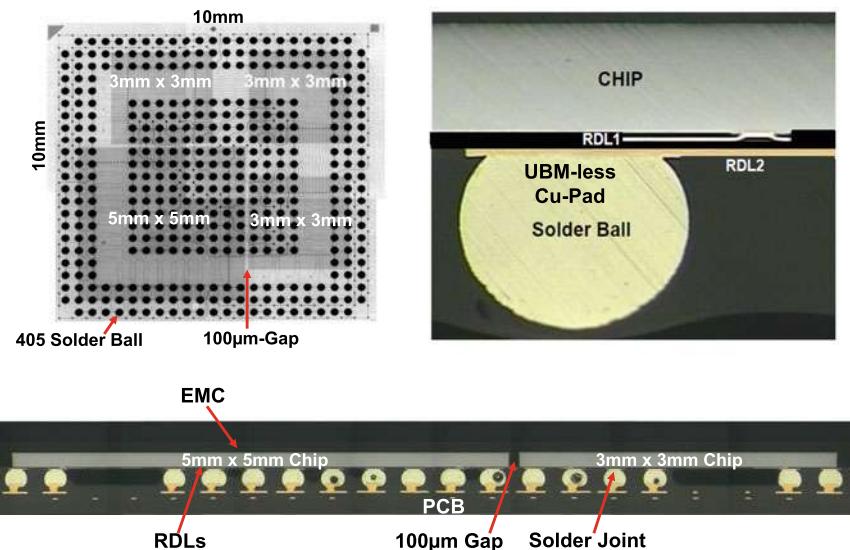
Figure 5.4 shows one of the early applications of fan-out packaging technology to mobile products. It is the baseband modem application processor chipset from HTC (Desire 606 W) shipped in 2013. It can be seen that the modem chip and the application processor chip are packaged side-by-side by the fan-out (chip first and face-down) technology. There are two RDLs fanning out from the chips and then solder ball attaching to the PCB. The key process steps in fabricating the RDLs are by organic RDL method. The assembly process of the chips on the reconstituted wafer is by SMT (surface mount technology) as discussed in Chap. 2.

### 5.6.2 Heterogeneous Integration of 4 Chips

Figures 5.5 and 5.6 show the heterogeneous integration of four chips by a fan-out packaging technology [11–16]. The large chip could be an application processor and the smaller chips could be memories. They are attached side-by-side with the fan-out chip-first and face-down packaging technology. There are two RDLs fabricated by the organic RDL method and the minimum metal L/S can go down to 5 µm.



**Fig. 5.5** Fan-out (chip-first) heterogeneous integration of 4 chips



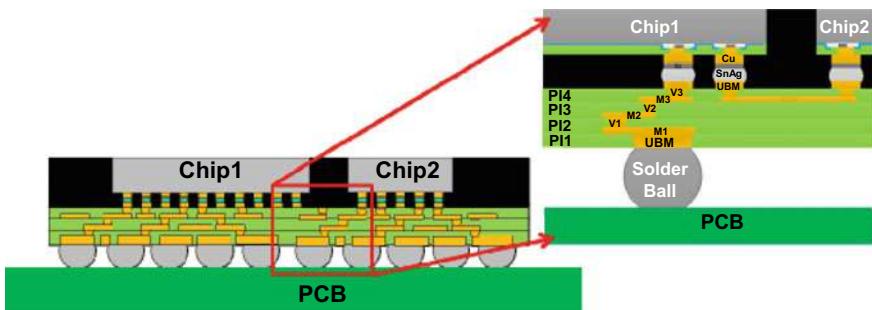
**Fig. 5.6** Fan-out (chip-first) heterogeneous integration of 4 chips on PCB

## 5.7 2D IC Integration—Fan-Out (Chip-Last)

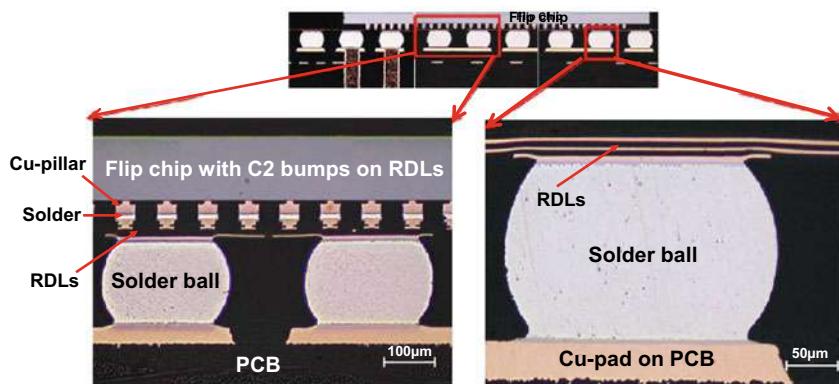
There are many examples on 2D IC integration with fan-out (chip-last) packaging technology. In this section, five examples are given. In fan-out with chip-last (or RDL-first) technology the RDLs usually will be fabricated first on a temporary glass carrier as shown in Sect. 4.7.4.

### 5.7.1 IME's Fan-Out with Chip-Last

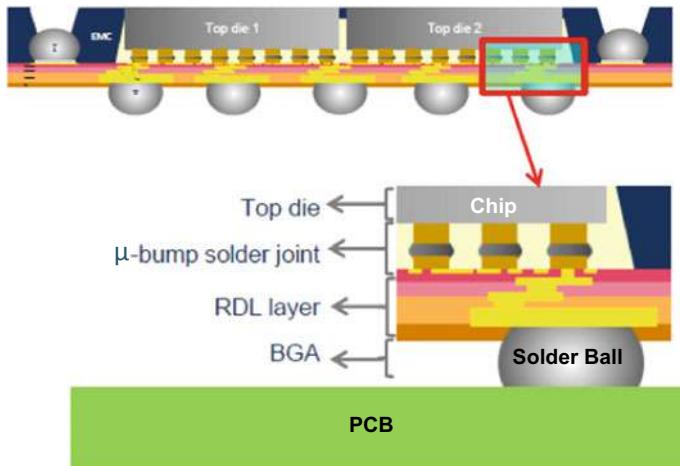
Figures 5.7 and 5.8 show the heterogeneous integration of two chips by fan-out chip-last (or RDL-first) packaging technology [17–26]. It can be seen that the RDL-substrate is fabricated first (as shown in Sect. 4.7.4). In parallel, perform the C2 (Cu-pillar + solder cap) wafer bumping, test for the KGD (known good die), and dice



**Fig. 5.7** Multichip with fan-out (chip-last) packaging [19]



**Fig. 5.8** Cross section images of fan-out (chip-last) packaging [19]



**Fig. 5.9** Amkor's SWIFT [31]

the wafer into individual KGDs. Then, perform the chip-to-wafer (RDL-substrate) bonding, underfilling and molding. Finally, debond the temporary carrier; mount the solder ball, and singulate the reconstituted wafer into individual packages.

### 5.7.2 *Amkor's SWIFT*

Figures 5.9 and 5.10 show Amkor's SWIFT (Silicon wafer integrated fan-out technology) [27–32]. The process flow (organic RDLs) is very similar to IME's. It can be seen that the Cu-pillar with solder cap is attached to the RDL-substrate and then the module is attached to the PCB with solder ball.

### 5.7.3 *Amkor's SLIM*

Figures 5.11 and 5.12 show Amkor's SLIM (silicon-less integrated module) [27–32]. The key difference between SWIFT and SLIM is that hybrid RDL is used for SLIM. In order to lower the metal L/S (go down to submicron), the hybrid RDL is fabricated with inorganic RDL first and organic RDL last. Figure 5.12 shows the 0.5  $\mu\text{m}$  metal L/S (RDL1) made by the semiconductor process and equipment (inorganic RDL method) and RDL2 and RDL3 made by the polymer and ECD (organic RDL method).

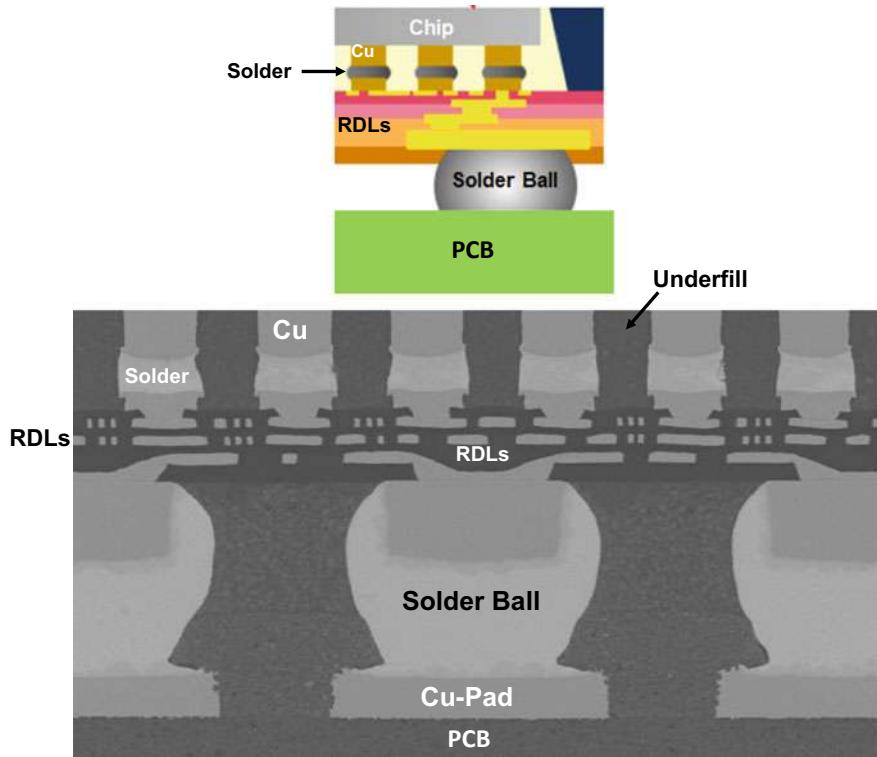


Fig. 5.10 SEM image of Amkor's SWIFT [31]

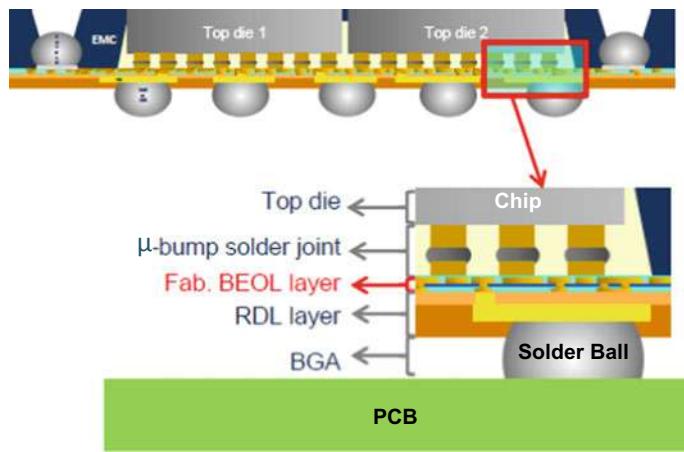
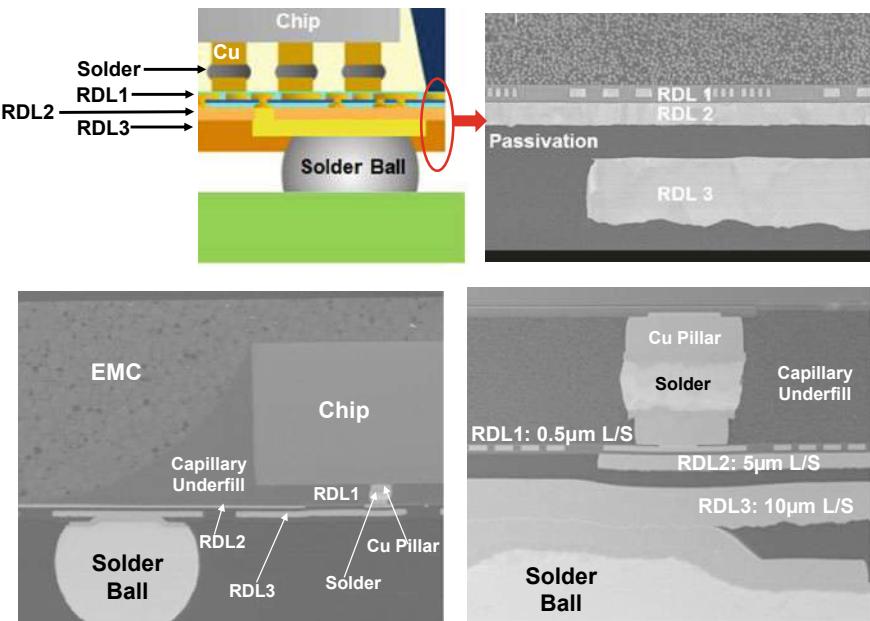


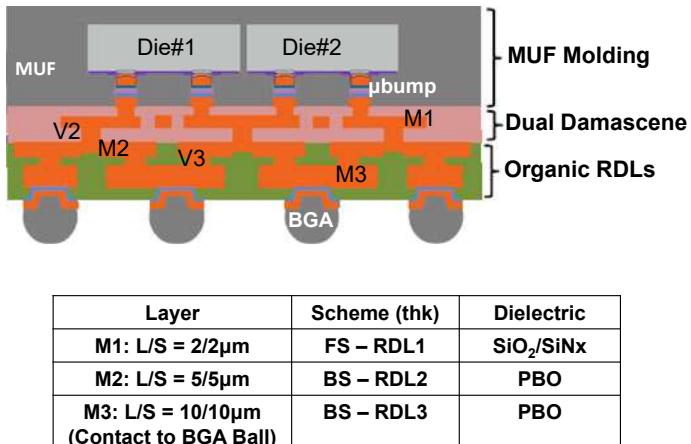
Fig. 5.11 Amkor's SLIM [30]



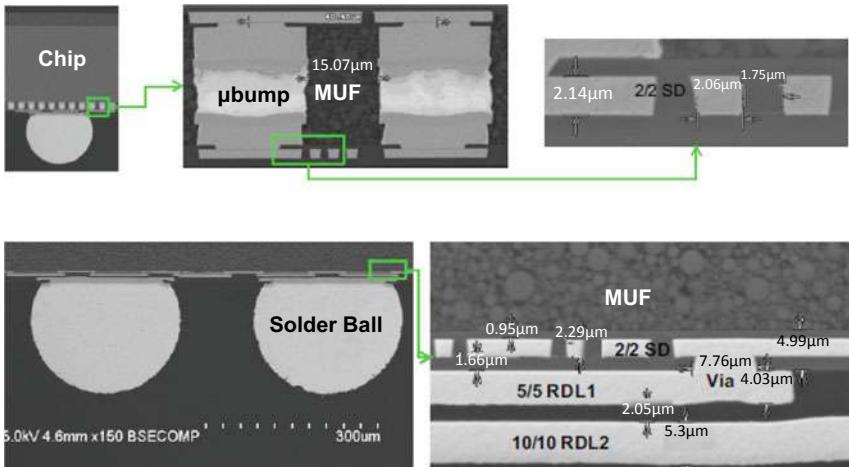
**Fig. 5.12** SEM image of Amkor's SLIM [30]

#### 5.7.4 SPIL's Fan-Out on Hybrid RDLs

In 2016, SPIL was the first one to demonstrate the feasibility of fan-out with chip-last on hybrid RDLs [33] as shown in Figs. 5.13 and 5.14. For the first (fine metal L/S)



**Fig. 5.13** SPIL's hybrid RDLs [33]



**Fig. 5.14** SEM image of SPIL's hybrid RDLs [33]

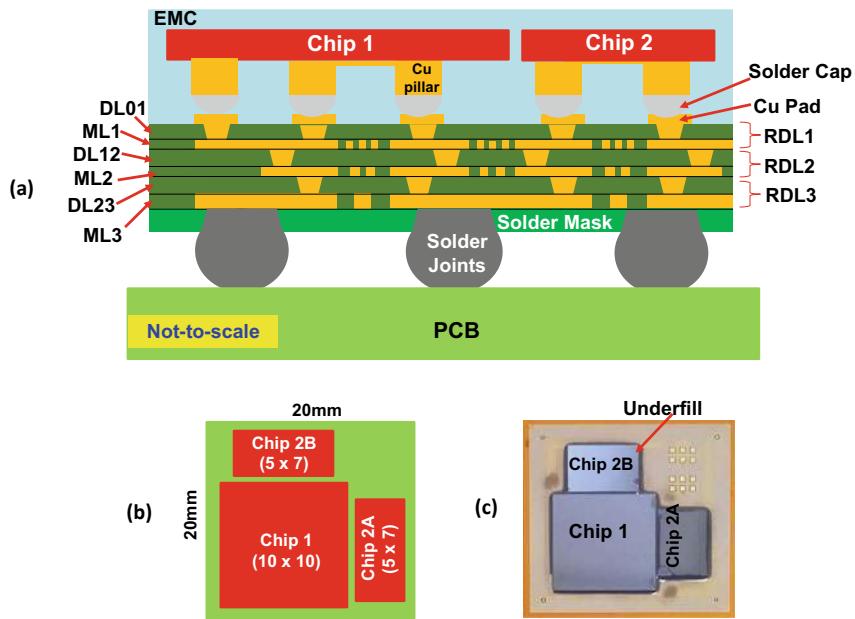
RDL, they used PECVD to make the  $\text{SiO}_2$  layer and dual-damascene + CMP to make the Cu metal layer with metal L/S = 2/2  $\mu\text{m}$  (inorganic RDL). Then they used polymer to make the dielectric layer and EDC + etching to make the Cu-layer for RDL2 and RDL3 (organic RDLs).

### 5.7.5 Unimicron's Fan-Out with Chip-Last

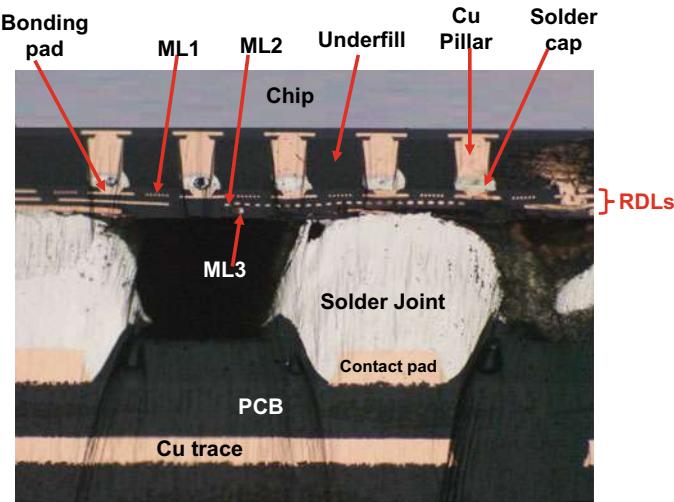
Figures 5.15 and 5.16 show the heterogeneous integration of one large chip (could be application processor) and two smaller chips (could be memories) on a RDL-first substrate with minimum metal L/S = 2/2  $\mu\text{m}$  [34, 35]. It can be seen from Fig. 5.16 that the large chip is Cu-pillar solder bumped on the fine metal L/S RDL substrate and then is solder balled on the PCB.

## 5.8 2.1D IC Integration

The 2.1D IC integration is defined as fabricating fine metal L/S thin-film layers on top of a build-up package substrate. In this section, eight examples will be briefly mentioned.



**Fig. 5.15** Unimicron's heterogeneous integration of three chips on fan-out RDL-first substrate

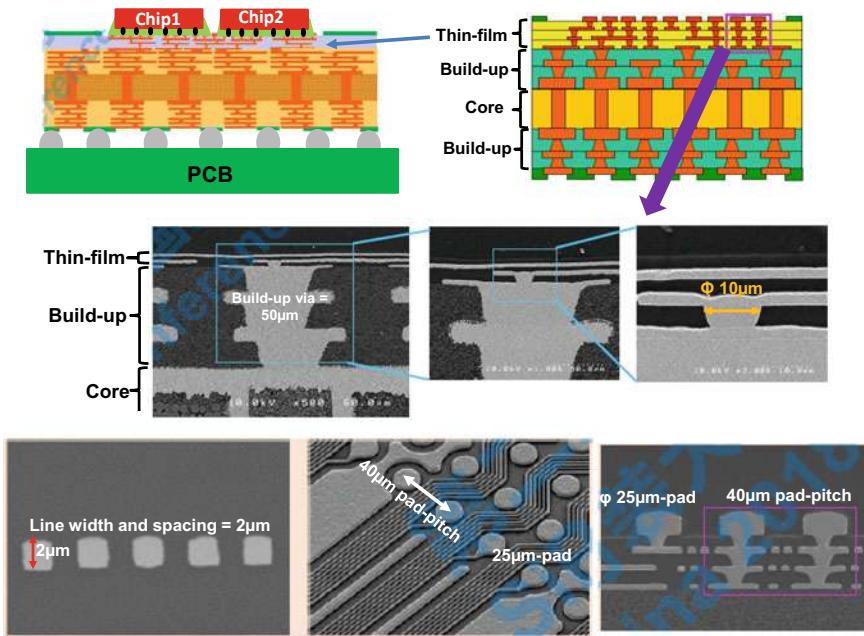


**Fig. 5.16** Cross section image of the PCB assembly of heterogeneous integration of three chips

### 5.8.1 Shinko's I-THOP

Shinko's i-THOP (integrated thin film high density organic package) is shown in Figs. 5.17, 5.18 and 5.19 [36, 37]. In 2013, Shinko proposed to make thin-film layers on top of the build-up layer of a package substrate. Figure 5.17 shows Shinko's i-THOP substrate [36] for high-performance applications. It is a 4 + (2-2-3) test vehicle, which means there is a two-layer metal core, three build-up metal layers at the bottom (PCB) side, two build-up metal layers on the top (chip) side, and the first number "4" represents that there are four thin-film Cu wiring layers (RDLs) on the surface of the top build-up layer. The thickness, line width, and spacing of the thin-film Cu RDLs can be as small as 2  $\mu\text{m}$ . The thin-film Cu RDLs are vertically connected through a 10  $\mu\text{m}$  via, as shown in Fig. 5.17. The surface Cu pad pitch is 40  $\mu\text{m}$ , and the Cu pad diameter is 25  $\mu\text{m}$  with a height of 10–12  $\mu\text{m}$ .

In 2014, Shinko demonstrated that [37] ultrafine pitch flip chips can be successfully assembled on the i-THOP substrate. Figure 5.18 schematically shows the two chips' lateral communications by the 2  $\mu\text{m}$  metal L/S RDLs of the two thin-film layers, which are built on top of the 1-2-2 build-up organic substrate, i.e., 2 + (1-2-2). Figure 5.19 shows the 40  $\mu\text{m}$  pitch microbumps (Cu pillar + Ni + SnAg) of the test chips and the 40  $\mu\text{m}$  pitch flip chip bonding pads (25  $\mu\text{m}$ -diameter). Typical images of the cross section of the flip chip assembly with optimized conditions are



**Fig. 5.17** Shinko's i-THOP [37]

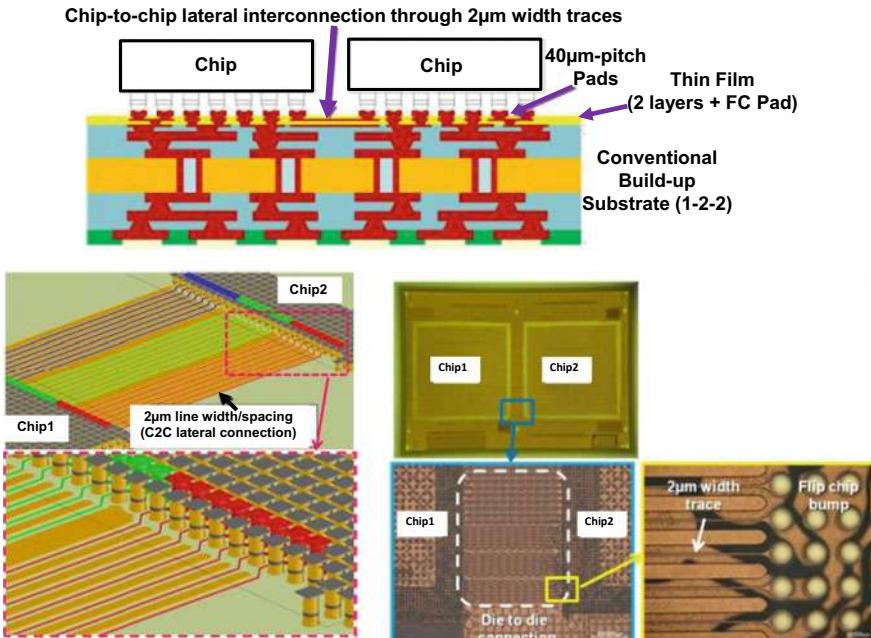


Fig. 5.18 Shinko's i-THOP with 2 thin-film layers [37]

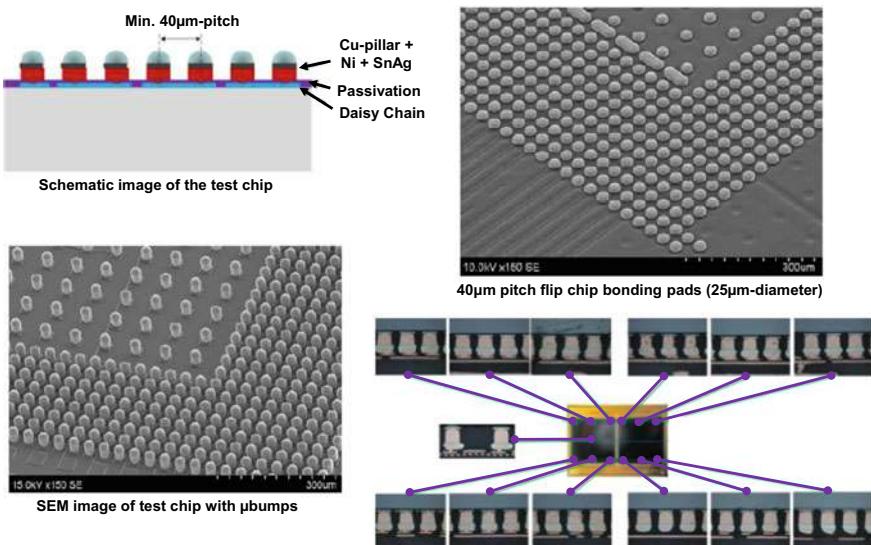
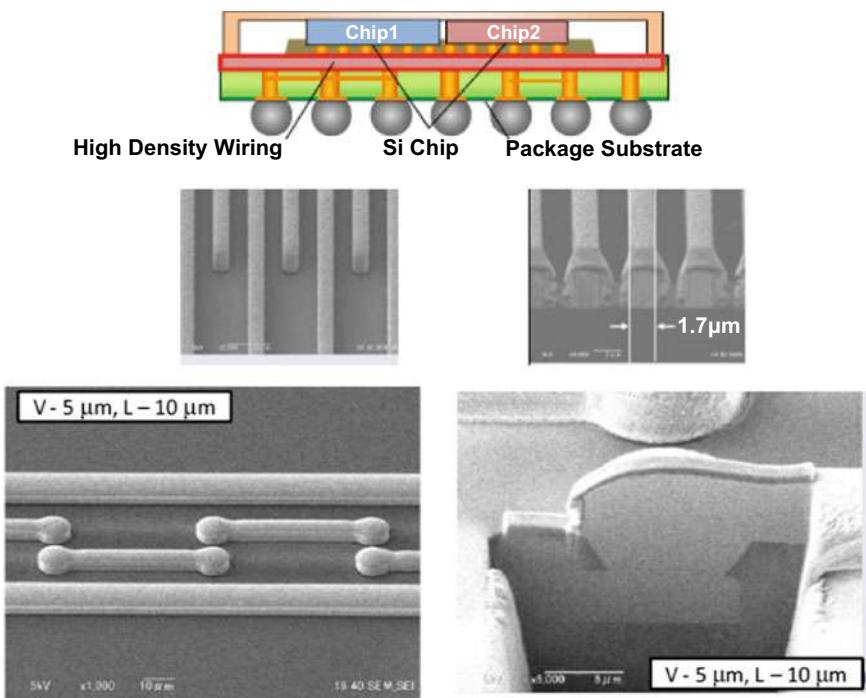


Fig. 5.19 Shinko's i-THOP test structure and assembly [37]

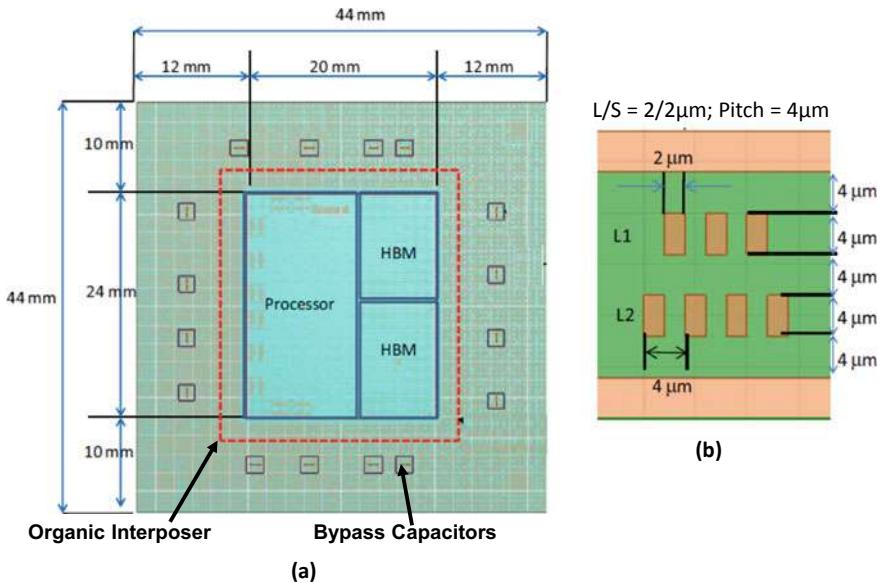
shown in Fig. 5.19. It can be seen that good solder joints are confirmed in all areas of the assembly [37].

### 5.8.2 Hitachi's 2.1D Organic Interposer

Figure 5.20 shows Hitachi's 2.1D organic interposer along with SEM images of the fine metal L/S RDLs and via patterns. It can be seen that  $2/2 \mu\text{m}$  L/S wiring are achieved. Also, a  $5 \mu\text{m}$ -diameter via and a  $10 \mu\text{m}$ -diameter via-land are obtained [38]. Figure 5.21a shows the schematic and physical dimensions of a 2.1D layout with high density wiring layers (organic interposer part) which are stacked at the top (Fig. 5.21b) of the conventional package substrate. For simulation results, please read [38].



**Fig. 5.20** Hitachi's 2.1D structure and images of line width and spacing [38]



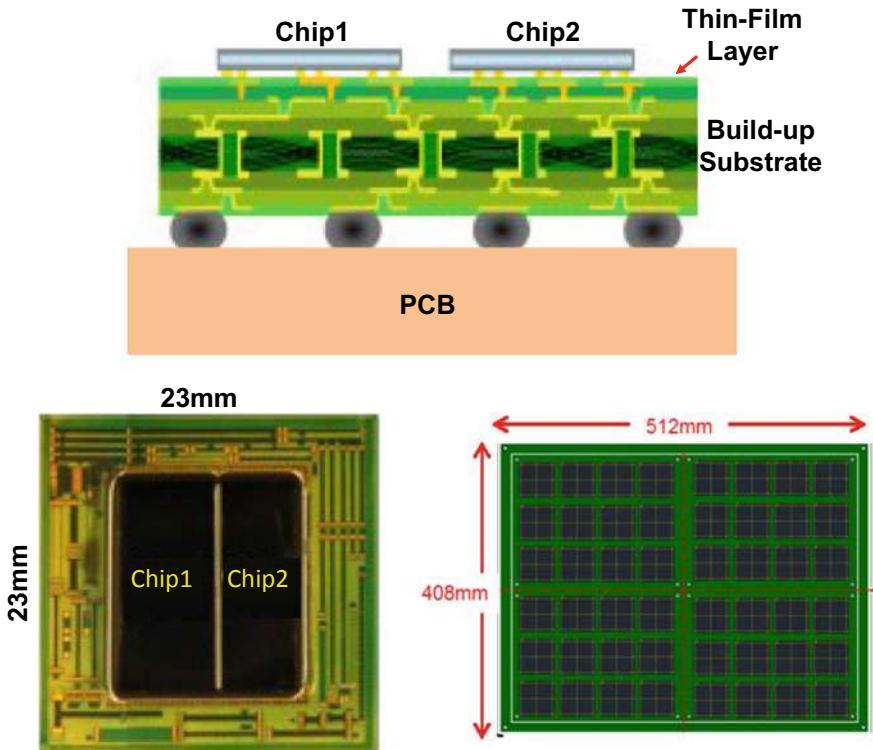
**Fig. 5.21** Structure for analysis of PDN impedance [38]

### 5.8.3 ASE's 2.1D Organic Interposer

Figure 5.22 shows ASE's 2.1D organic interposer [39]. It can be seen that the high density substrate is fabricated on a large panel ( $512\text{ mm} \times 408\text{ mm}$ ), which consists of 4 blocks with dimensions:  $256\text{ mm} \times 204\text{ mm}$ . There are three strips ( $240\text{ mm} \times 63.5\text{ mm}$ ) for each block and 16 units for each strip. Each unit ( $23\text{ mm} \times 23\text{ mm}$ ) supports two chips. Figure 5.23a shows the high-density thin-film patterns in various views and Fig. 5.23b shows the flip chip assembly on the 2.1D organic interposer.

### 5.8.4 SPIL's 2.1D Organic Interposer

Figure 5.24 shows SPIL's 2.1D organic interposer [40]. The package size is  $45\text{ mm} \times 45\text{ mm} \times 2.9\text{ mm}$  and the substrate thickness is  $1.2\text{ mm}$  (4-layer thin film + 2/2/3). The chip size is  $11.8\text{ mm} \times 20.8\text{ mm} \times 0.78\text{ mm}$ . The minimum metal  $L/S = 2/2\text{ } \mu\text{m}$  and the micro pad pitch is  $40\text{ } \mu\text{m}$  minimum. Figure 5.25 shows top and bottom views of the 2.1D organic interposer package. Also, the dimensions of the micro bump and the flip chip assembly on the thin-film layer are shown in Fig. 5.25. For simulation and reliability test results, please read [40].



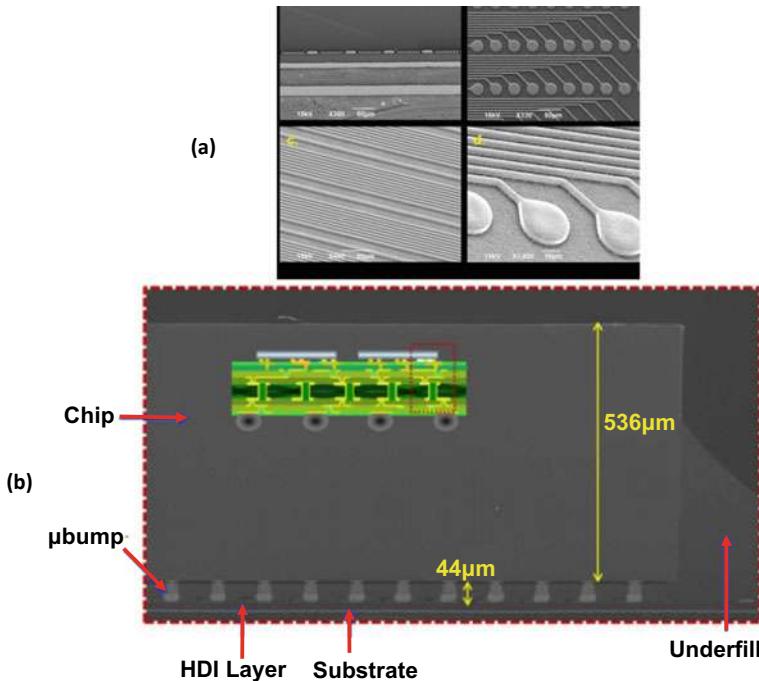
**Fig. 5.22** ASE's test vehicle [39]

### 5.8.5 JCET's UFOS

JCET's 2.1D organic interposer so called uFOS (ultra format organic substrate) [41] is shown in Fig. 5.26 and the key process steps and SEM image are shown in Fig. 5.27. It can be seen that the metal L/S = 2/2  $\mu\text{m}$  (uFOS) are built on top of the coreless package substrate. However, in order to mitigate of the warpage issue of the coreless package substrate, an embedded stiffness (e-STF) in the last layer of coreless package substrate is introduced during the substrate manufacturing process. Metallic pieces are impregnated with prepreg to enhance the substrate's overall stiffness [41] to resist bending as shown in Fig. 5.26.

### 5.8.6 Intel's EMIB

Figure 5.28 shows Intel's Agilex FPGA (field programmable grid array) module. It can be seen that the FPGA is with two different kinds of solder bumps (C4 bump

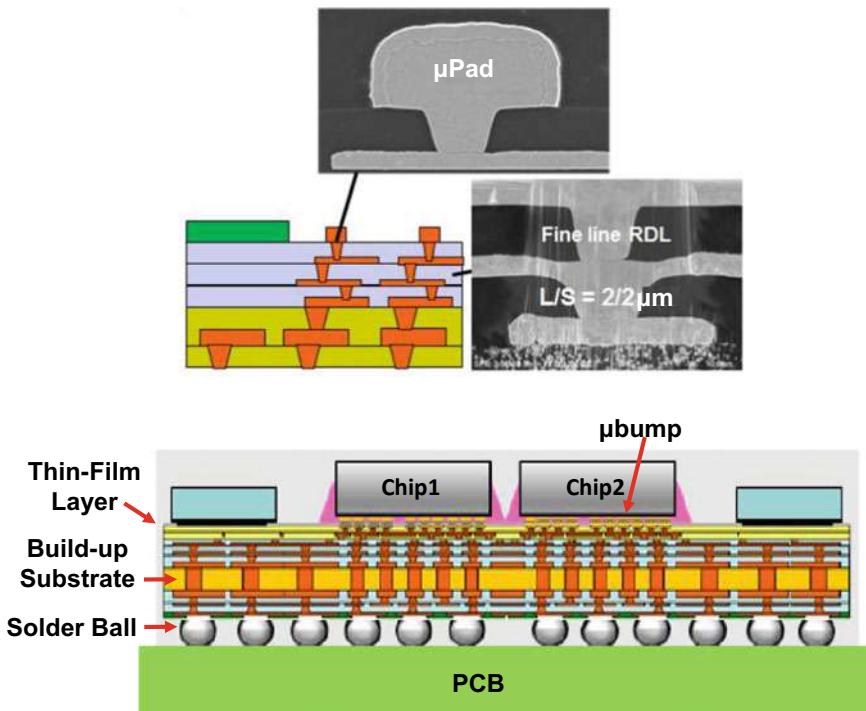


**Fig. 5.23** SEM of the thin-film layer and the cross section of the structural assembly [39]

and C2 microbump). The FPGA and other chips are attached on a build-up package substrate with embedded multi-die interconnect bridge (EMIB). EMIB is a piece of dummy silicon with fine metal L/S RDLs to allow horizontal interconnection of chips [42, 43].

### 5.8.7 Applied Materials' Bridge

On December 8, 2017, Applied Materials proposed to embed the bridge in an EMC with fan-out packaging method as shown in Fig. 5.29 [44]. It can be seen that the circuitries of the chips are fanned out with the fan-out RDLs and connected horizontally through the bridge. The vertical interconnects are through the TMV [44].



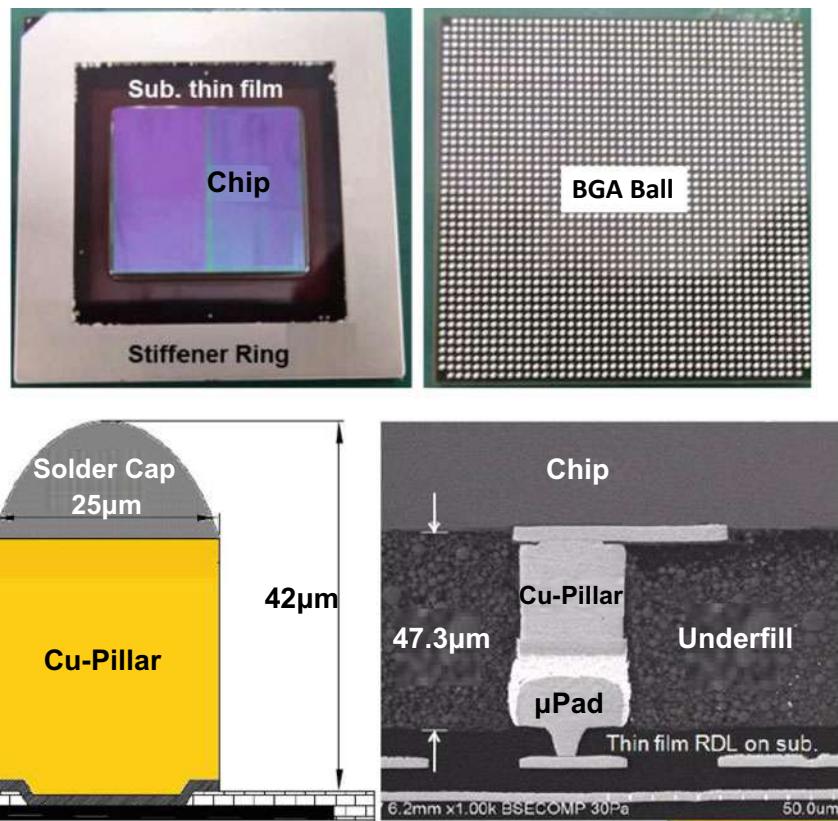
**Fig. 5.24** SEM images of the thin-film layers and the cross section of the structure (SPIL) [40]

### 5.8.8 TSMC'S LSI

During TSMC's Annual Technology Symposium (August 25, 2020), TSMC announced their LSI (local Si interconnect) technology as shown in Fig. 5.30. It can be seen that the LSI technology is very similar to Applied Materials'. There could be one big difference, which is, the LSI may not be a piece of TSV-less interposer with RDLs but may include TSVs or even CMOS devices.

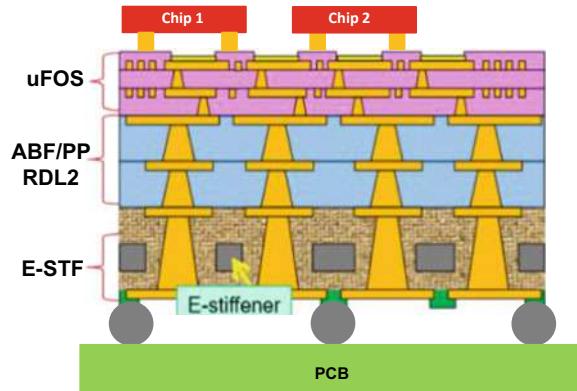
## 5.9 2.3D IC Integration

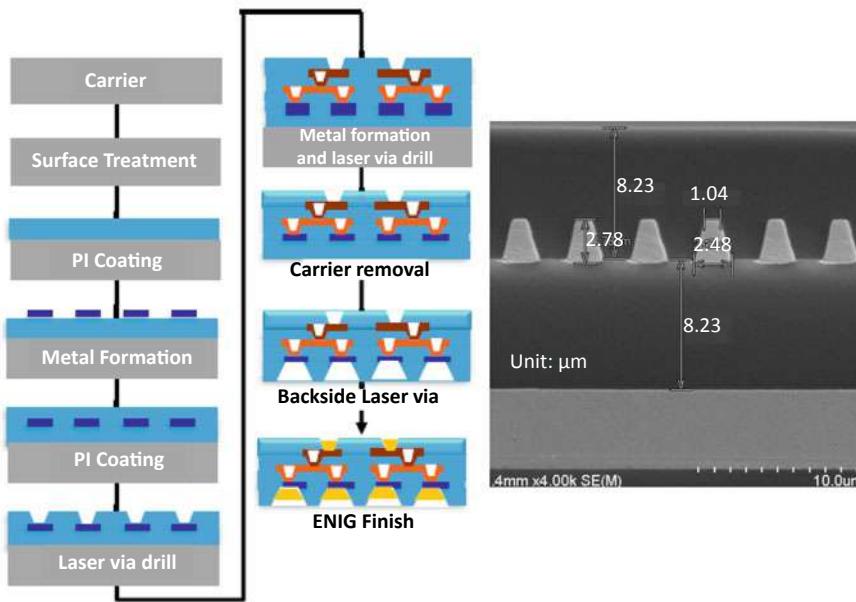
The 2.3D IC integration is defined as fabricating a coreless organic/inorganic interposer on top of a build-up package substrate. Coreless substrates (interposers) have been obtained tractions in the past 10 years. The biggest difference between the conventional build-up package substrate and the coreless substrate is all the layers of the coreless substrate are the build-up layers. The advantages of the coreless substrate are: (a) because of eliminating the core, the cost of coreless substrate is lower; (b) by eliminating the core, higher wiring ability can be achieved; (c) better electrical



**Fig. 5.25** SEM image of the chip on thin film layers with microbump and underfill [40]

**Fig. 5.26** Schematic of the structure with thin-film layer (uFOS) and the embedded stiffener (e-STF) layer [41]





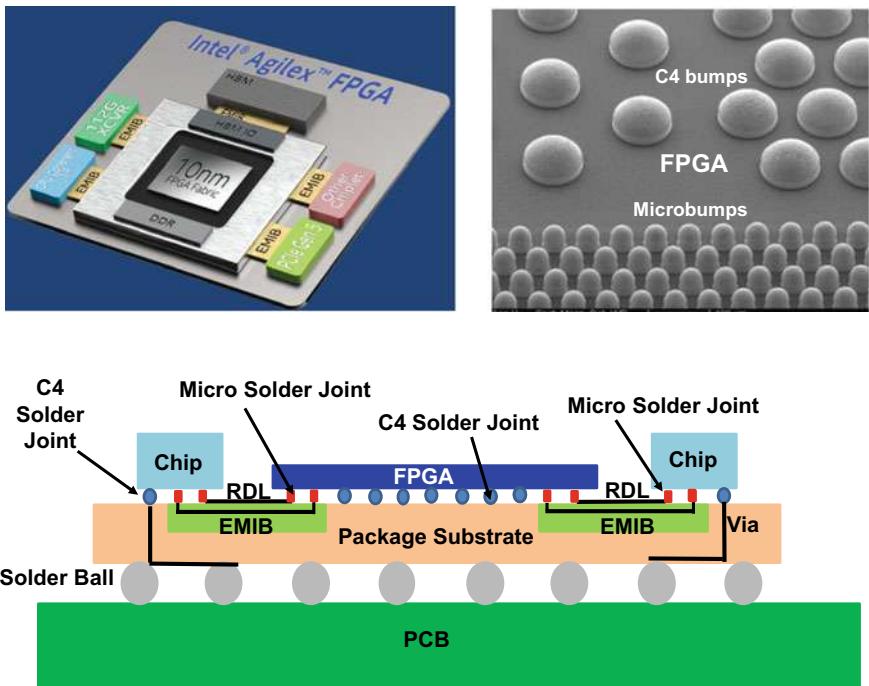
**Fig. 5.27** uFOS process flow and the SEM of the thin film layer (JCET) [41]

performance because of good high-speed transmission characteristic; and (d) definitely smaller form factor. On the other hand, the disadvantages are: (a) because of eliminating the core, the warpage of the coreless substrate is larger; (b) easier to have laminate chipping; (c) poor solder joint yield because of less substrate rigidity; and (d) new manufacturing infrastructure is necessary. In 2010, Sony manufactured the first coreless substrate for the Cell processor of their PlayStation3.

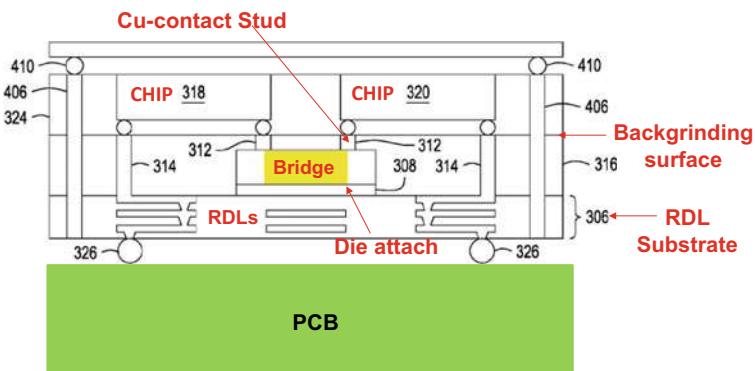
There are at least three methods to fabricate the coreless organic/inorganic interposer, namely, the conventional semi-additive process (SAP)/PCB method for organic interposer, fan-out with chip-first method for organic interposer, and fan-out with chip-last (or RDL-first) method for organic/inorganic interposer.

## 5.10 2.3D IC Integration with SAP/PCB Method

In this section, the organic interposer is made by the conventional SAP/PCB process. Two examples are briefly mentioned.



**Fig. 5.28** Intel’s EMIB embedded in the top-layer of build-up substrate for their Agilex FPGA module [43]

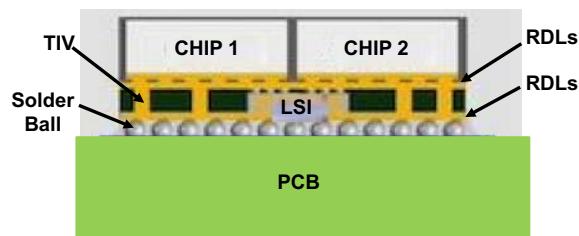


**Fig. 5.29** Applied Materials’ bridge embedded in EMC

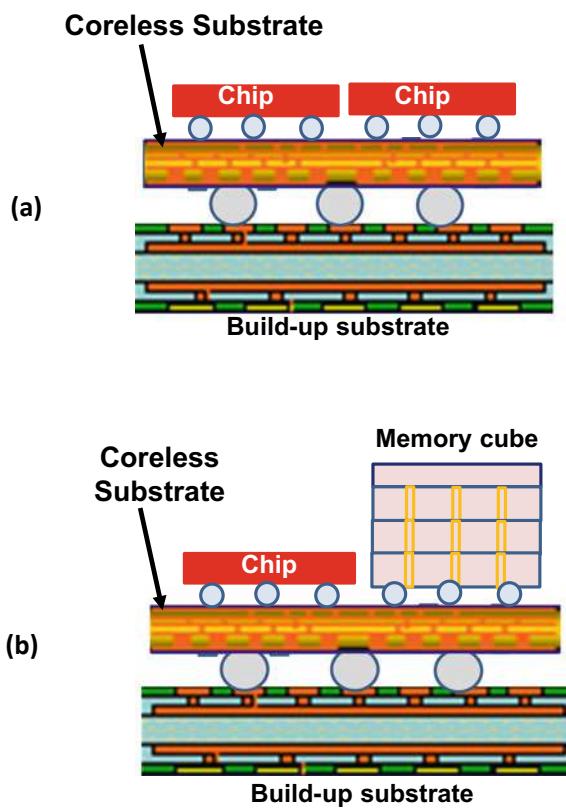
### 5.10.1 Shinko’s Coreless Organic Interposer

In 2012, Shinko proposed to use the coreless package substrate to replace the TSV-interposer as shown in Fig. 5.31. For sure, the cost in making the coreless substrate

**Fig. 5.30** TSMC's LSI (local silicon interconnect) bridge embed in EMC



**Fig. 5.31** Shinko's coreless organic interposer

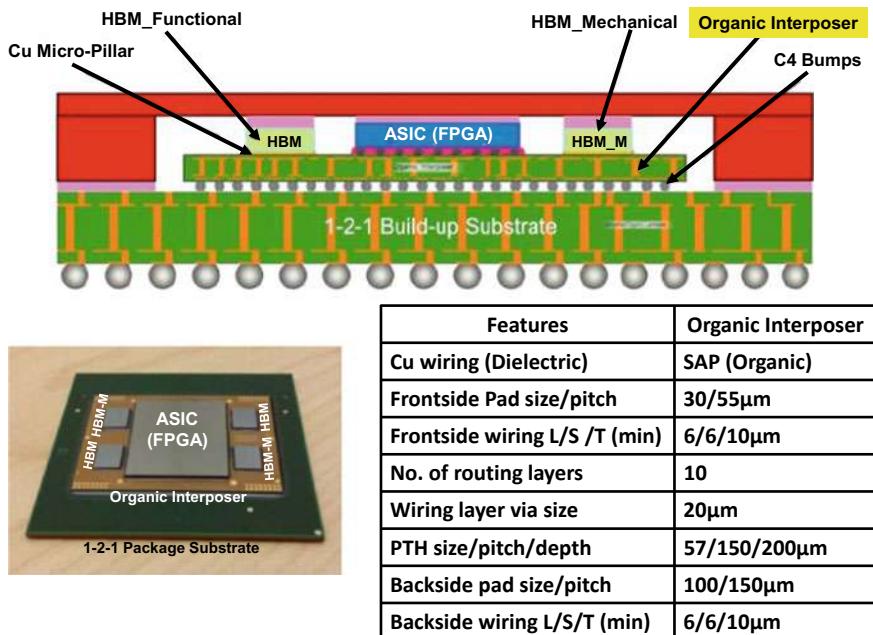


is much lower than that in making the through-silicon via and redistribution layers (TSV/RDL) interposer (which requires semiconductor equipment). Warpage could be an issue.

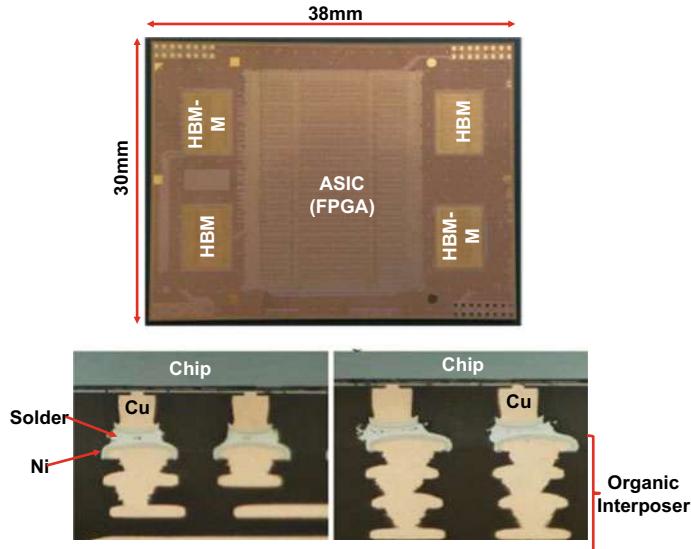
### 5.10.2 Cisco's Organic Interposer

Figure 5.32 shows a heterogeneous integration designed and manufactured with a large organic interposer (TSV-less interposer) with fine-pitch and fine-line interconnections by Cisco [45]. The organic interposer has a size of 38 mm × 30 mm × 0.4 mm. The minimum line width, spacing, and thickness of the front side and back side of the organic interposer are the same and are, respectively, 6, 6, and 10  $\mu\text{m}$ . It is a 10-layer high density organic interposer (substrate) and the via size is 20  $\mu\text{m}$ . The major manufacturing steps for making the organic interposer are the same as those for the organic build-up package substrate. These include: (a) plating through-hole (PTH) generation and filling for the core layer, (b) circuitization of the core layer, and (c) building Cu wiring layers on two sides of the core layer with SAP.

A high-performance application-specific IC (ASIC) die measured at 19.1 mm × 24 mm × 0.75 mm is attached on top of the organic interposer along with four high-bandwidth memory (HBM) dynamic random access memory (DRAM) die stacks. The 3D HBM die stack with a size of 5.5 mm × 7.7 mm × 0.48 mm includes one base buffer die and four DRAM core dice that are interconnected with TSVs and fine-pitch micro-pillars with solder cap bumps. The pad size and pitch of the front side of the organic interposer are 30  $\mu\text{m}$  and 55  $\mu\text{m}$ , respectively. Figure 5.33 shows a top view of the organic interposer manufactured and the cross sectional view of



**Fig. 5.32** Cisco's organic interposer [45]



**Fig. 5.33** Fabricated organic interposer and its cross section image [45]

the good solder joint made between the HBM die-stacks and the organic interposer [45].

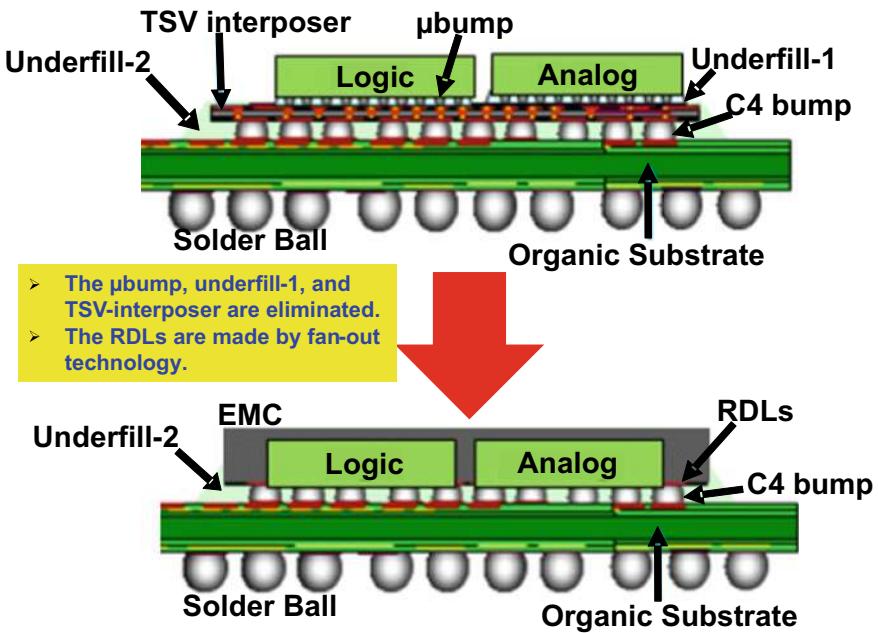
## 5.11 2.3D IC Integration with Fan-Out (Chip-First) Method

The 2.3D IC integration with coreless organic interposer fabricated by the fan-out and chip-first process is presented in this section. There are four examples.

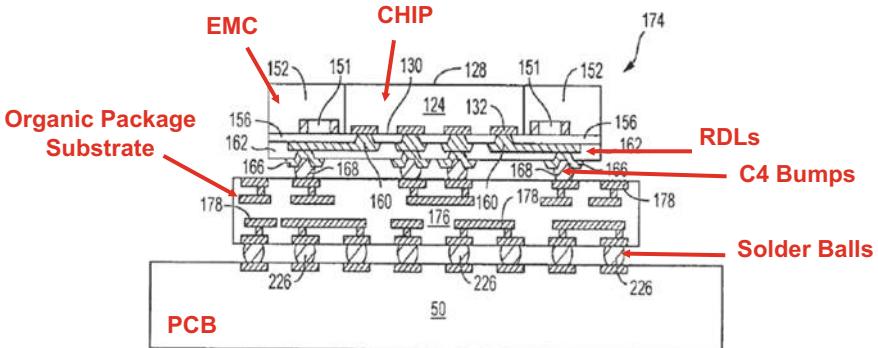
### 5.11.1 Statschippac's 2.3D eWLB

At ECTC2013, Statschippac proposed [46, 47] using the fan-out flip chip (FOFC)-eWLB (embedded wafer level ball grid array) to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 5.34. Their objective is to replace the TSV interposer, microbump, and underfill by the RDLs (coreless organic interposer) as indicated in their patent application (US 9,484,319 B2, filed on December 23, 2011) and granted on November 1, 2016 as shown in Fig. 5.35 [46].

Mediatek filed their patent (US 7,838,975 B2) on February 12, 2009 and was granted the patent on November 23, 2010 [48]. Mediatek's objective is not to replace

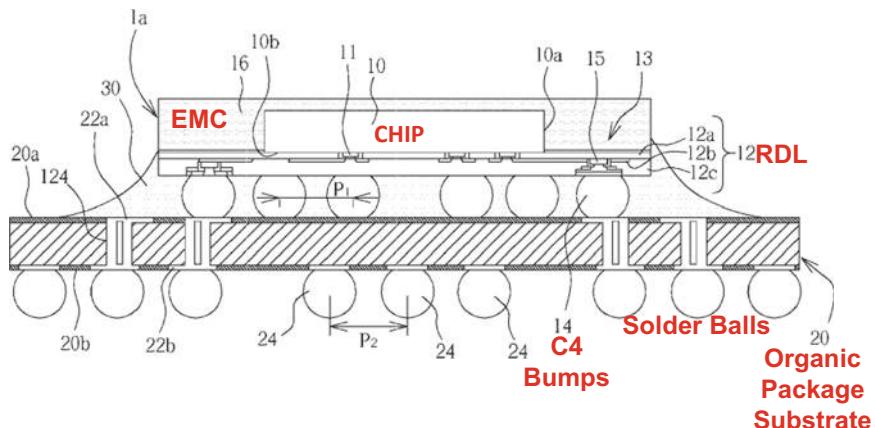


**Fig. 5.34** Statschippac's fan-out (chip-first) organic interposer [47]



**Fig. 5.35** Statschippac's patent on fan-out (chip-first) organic interposer

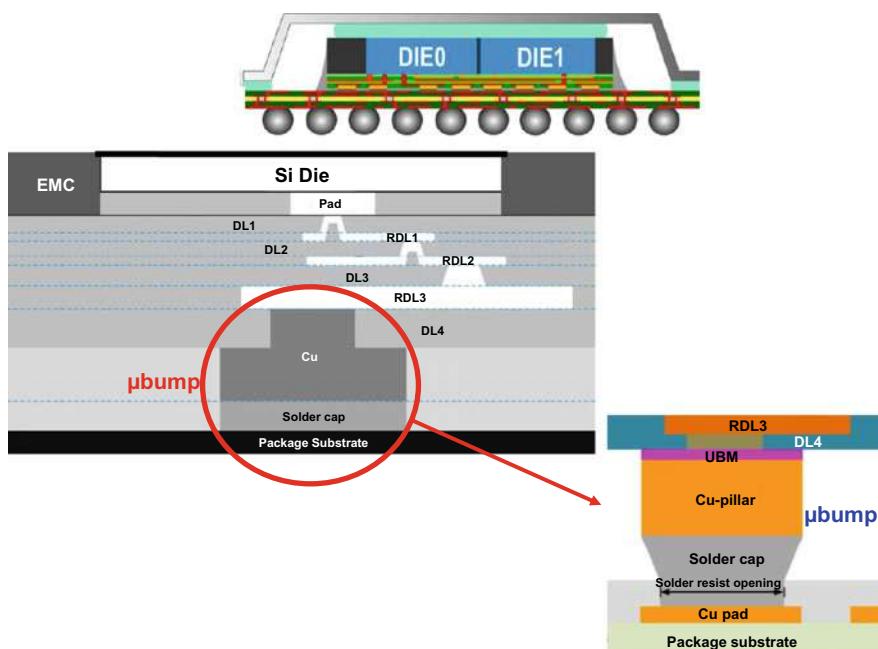
the TSV interposer, but to use the RDL interposer for very fine pitch flip chip pads so they can use the low-cost package substrate as shown in Fig. 5.36. The structures of US 9,484,319 B2 and US 7,838,975 B2 look similar.



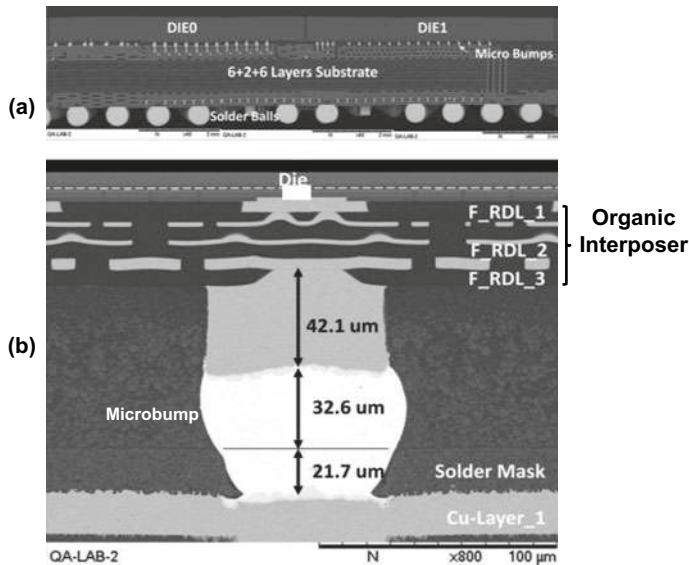
**Fig. 5.36** Mediatek's patent on fan-out (chip-first) organic interposer

### 5.11.2 Mediatek's Fan-Out (Chip-First)

During ECTC2016, Mediatek [49] proposed similar TSV-less interposer RDLs fabricated with FOWLP technology as shown in Figs. 5.37 and 5.38. Instead of the C4



**Fig. 5.37** Mediatek's fan-out (chip-first) organic interposer [49]



**Fig. 5.38** Mediatek's fan-out (chip-first) cross section SEM images of organic interposer [49]

bump, they used a microbump (Cu-pillar + solder cap) to connect the bottom RDL to the 6-2-6 package substrate.

### 5.11.3 ASE's *FOCoS (Chip-First)*

During ECTC2016, ASE [50] proposed using the fan-out wafer-level packaging (FOWLP) technology (chip-first and die face-down on a temporary wafer carrier and then over molded by the compression method) to make the RDLs for the chips to perform mostly lateral communications as shown in Figs. 5.39 and 5.40; the technology is called fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate using under bump metallurgy (UBM) and the C4 bump. Basically, ASE's is very similar to Statschippac's.

### 5.11.4 TSMC's *InFO\_OS and InFO\_MS*

Figure 5.41 schematically illustrates TSMC's fan-out RDL-substrates for heterogeneous integrations [51]. Figure 5.41a shows the integrated fan-out on substrate

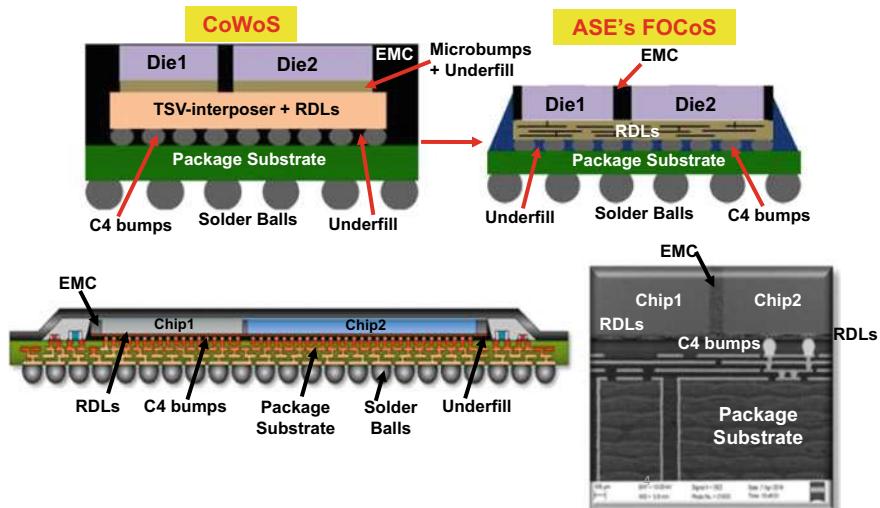


Fig. 5.39 ASE's fan-out (chip-first) organic interposer (FOCoS) [50]

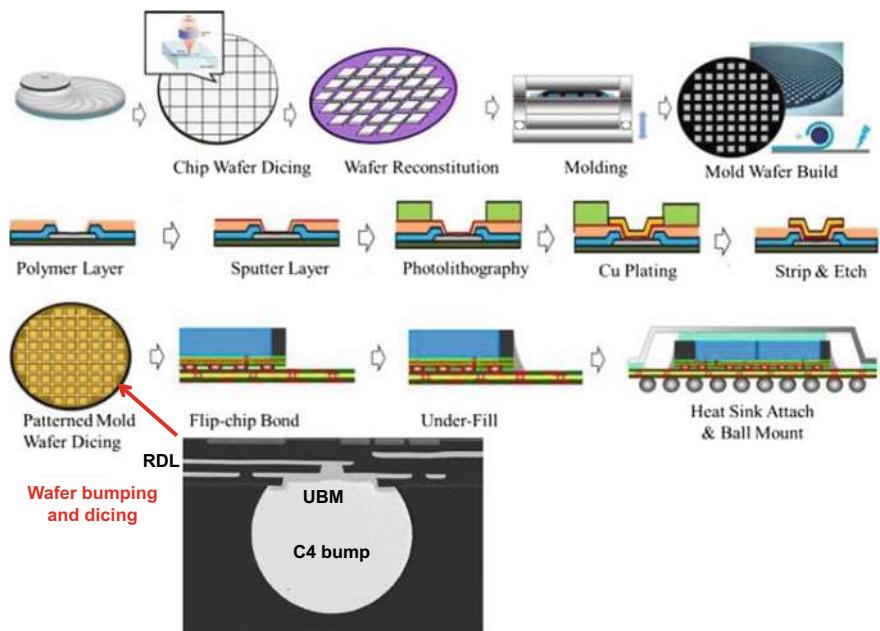
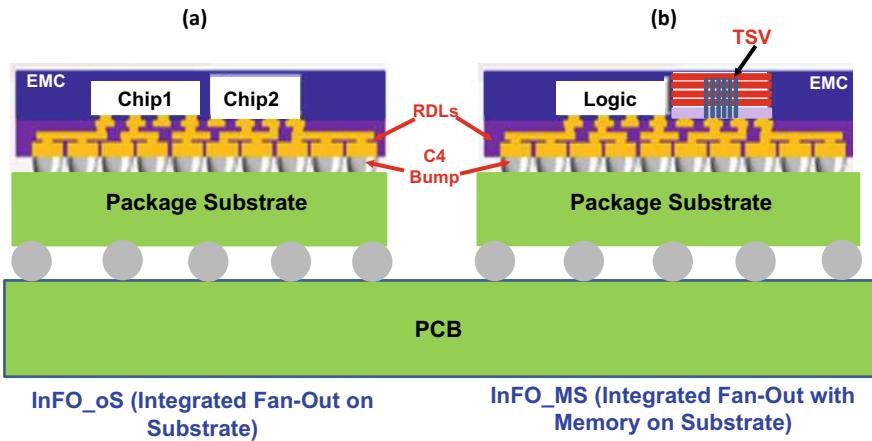


Fig. 5.40 Key process steps of ASE's chip-first FOCoS [50]



**Fig. 5.41** TSMC's **a** InFO\_oS. **b** InFO\_MS [51]

(InFO\_oS) for heterogeneous integration, which eliminates the micro bumps, underfill, and TSV interposer with the RDLs. Figure 5.41b shows the integrated fan-out with memory on substrate (InFO\_MS), which is meant for higher performance applications.

## 5.12 2.3D IC Integration with Fan-Out (Chip-Last) Method

The 2.3D IC integration with coreless organic/inorganic interposer fabricated by the fan-out and chip-last (or RDL-first) process is presented in this section. There are six examples.

### 5.12.1 SPIL'S NTI

During ECTC2016, SPIL proposed the NTI (non-TSV interposer) for 2.3D IC integration with coreless inorganic interposer [52, 53]. First, they used the 65 nm process technology to make the RDLs with a 0.4  $\mu\text{m}$ -pitch minimum on a wafer. Then, they performed the chip-to-wafer bonding on the RDLs, underfilled the gap between the chips and the RDL interposer, and molded the chips with EMC. The rest of the key process steps are shown in Fig. 5.42. Figure 5.43 shows the cross section of the assembly. It can be seen that the chips are attached to the inorganic interposer (RDLs) with microbump (Cu-pillar + solder cap). Then, the RDLs interposer is attached to the build-up package substrate with C4 bump.

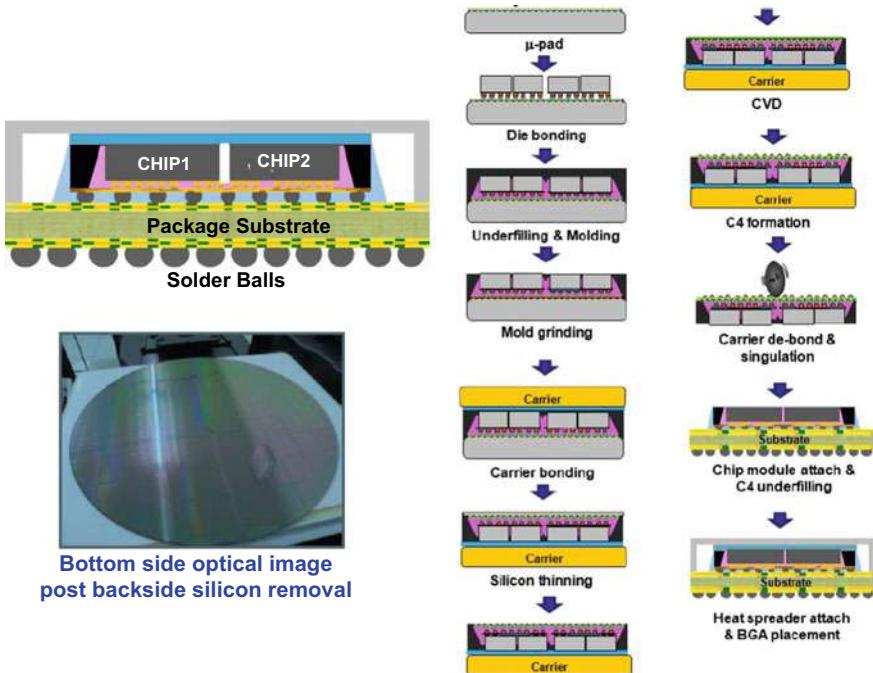
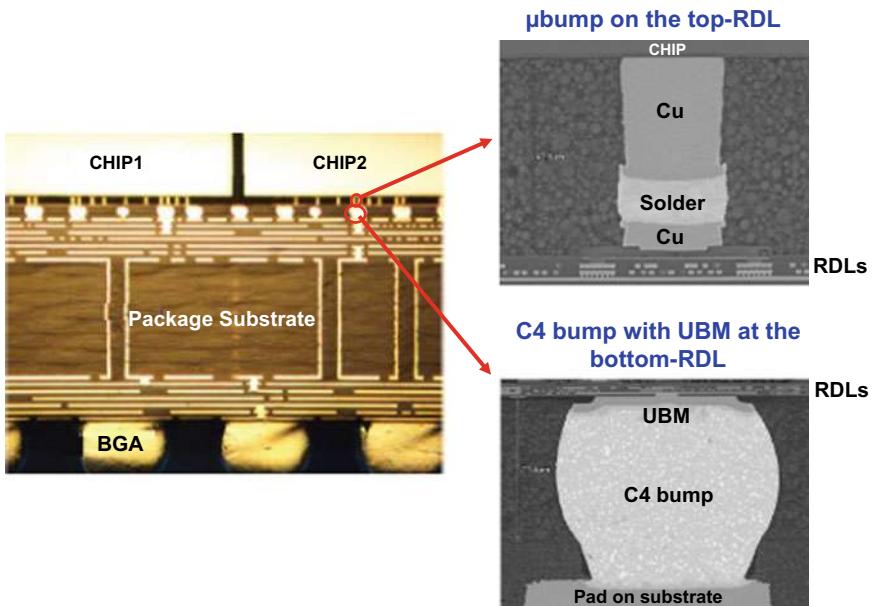


Fig. 5.42 SPIL's fan-out (chip-last) inorganic interposer [53]

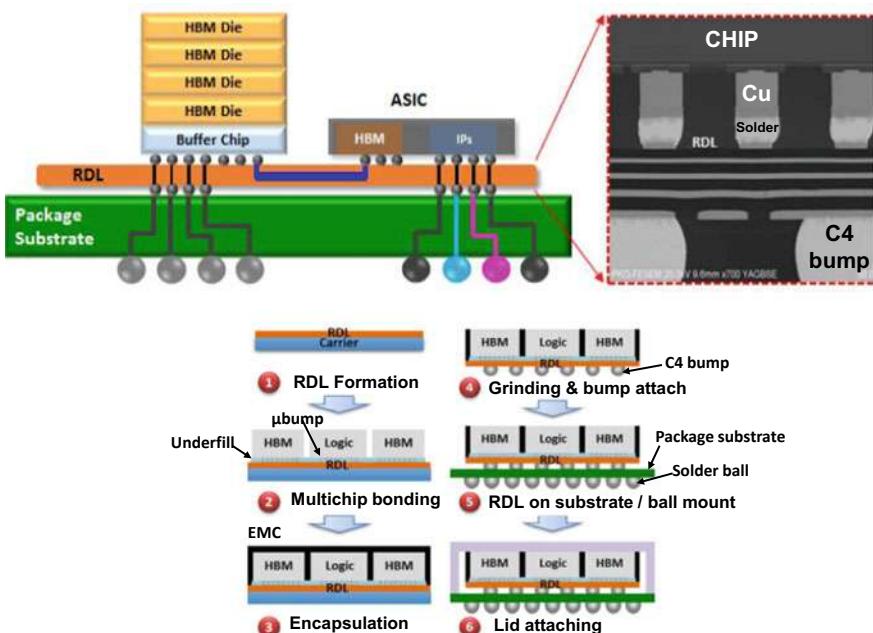
### 5.12.2 Samsung's Si-Less RDL Interposer

During ECTC2018, Samsung [54, 55] proposed the use of chip-last or RDL-first FOWLP to eliminate the TSV-interposer for high performance computing heterogeneous integration applications. First of all, the RDLs are built on a bare glass—either in a wafer or a panel format. In parallel, wafer bumping of the logic and HBM chips will be done. Then, the following processes are done: fluxing, chip-to-wafer or chip-to-panel bonding, cleaning, underfill dispensing and curing. Those steps are followed by epoxy molding compound (EMC) compression molding. Then, backgrinding the EMC, chips, and HBM cube and C4 wafer bumping are done (Fig. 5.44). After those steps, one can attach the whole module on the build-up package substrate. Finally, solder ball mounting and lid attachment are done. Samsung called the resulting structure a Si-less RDL interposer [54].

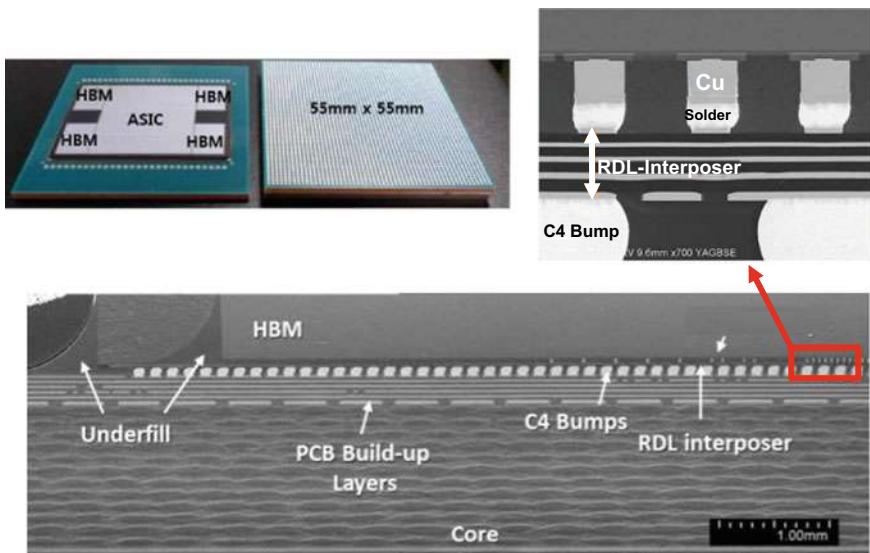
Samsung's test vehicle is shown in Fig. 5.45. The RDL interposer is 55 mm x 55 mm and consists of 5-RDLs including bonding layer, signal and ground layers. Samsung showed that the thermal cycling performance of the C4 solder joint in the organic-interposer module (Fig. 5.46) is better than that of the TSV-interposer module (Fig. 5.47) [54]. This is because of the thermal expansion mismatch between the silicon-interposer and build-up package substrate is larger than that between the organic-interposer.



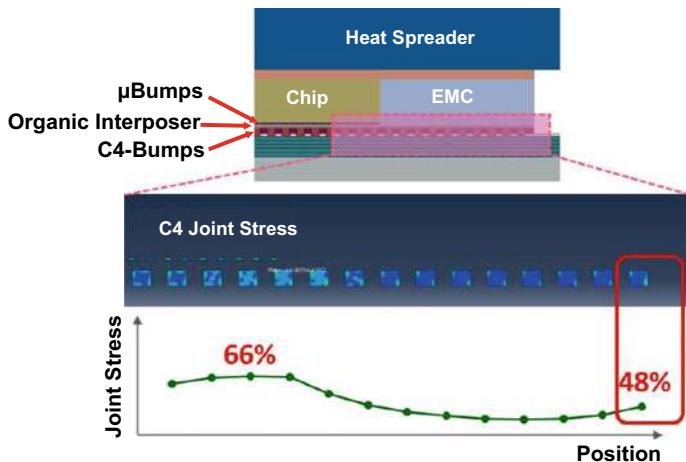
**Fig. 5.43** Cross section of the assembly with SEM images of the RDLs, microbump and C4 bump [53]



**Fig. 5.44** Samsung's fan-out (chip-last) organic interposer including key process steps [54]



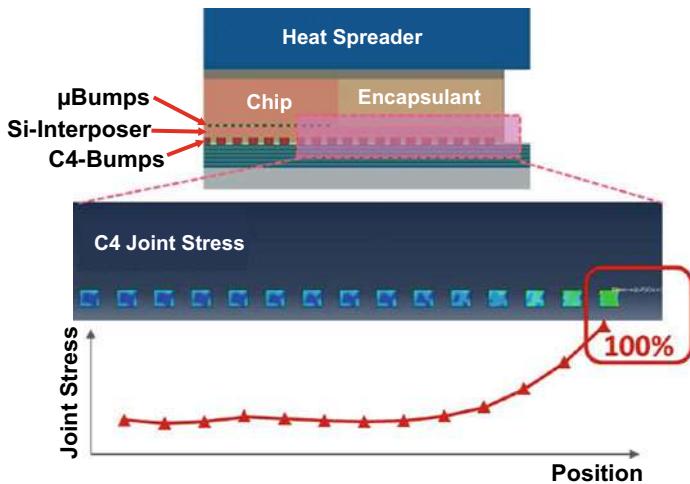
**Fig. 5.45** Samsung's test vehicle and cross section SEM images [54]



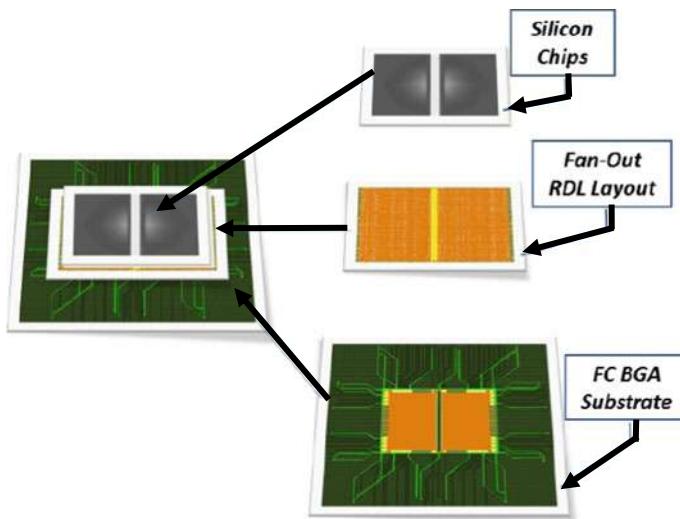
**Fig. 5.46** Stress in solder joints with organic interposer [54]

### 5.12.3 ASE's FOCoS (Chip-Last)

Figures 5.48 and 5.49 show ASE's FOCoS with fan-out chip-last process [56–58]. First, they fabricate a RDL-interposer on a temporary glass carrier. It can be seen from Fig. 5.49 that there are at least 4 RDLs with stacked vias and non-stacked vias. In parallel, they perform the wafer bumping for the microbump. Then, they

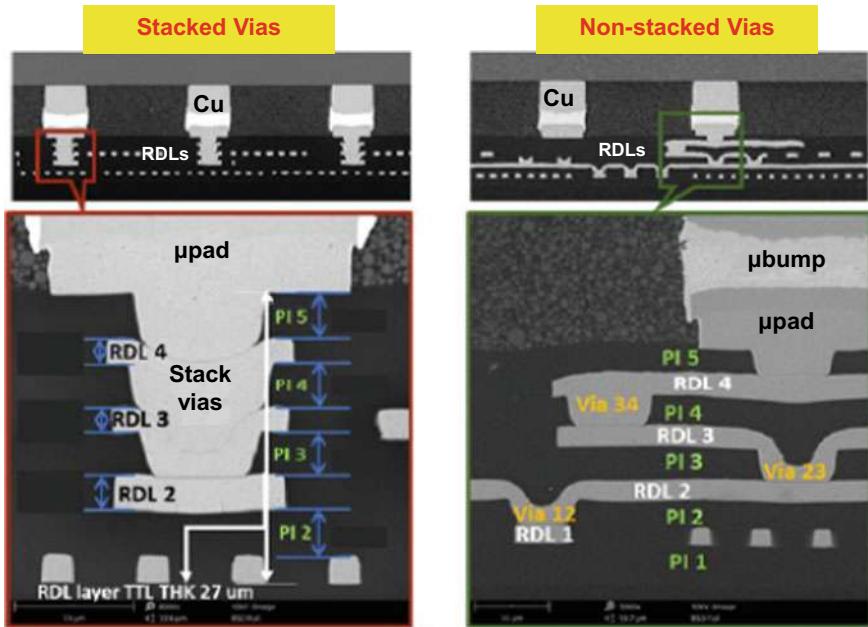


**Fig. 5.47** Stress in solder joints with Si-interposer [54]



**Fig. 5.48** ASE's fan-out (chip-last) organic interposer [56]

perform the chip-to-RDL-wafer bonding, underfilling, and molding. It is followed by debonding the temporary carrier, C4 bump mounting, and dicing into individual modules. Finally, the module is attached on a build-up package substrate.



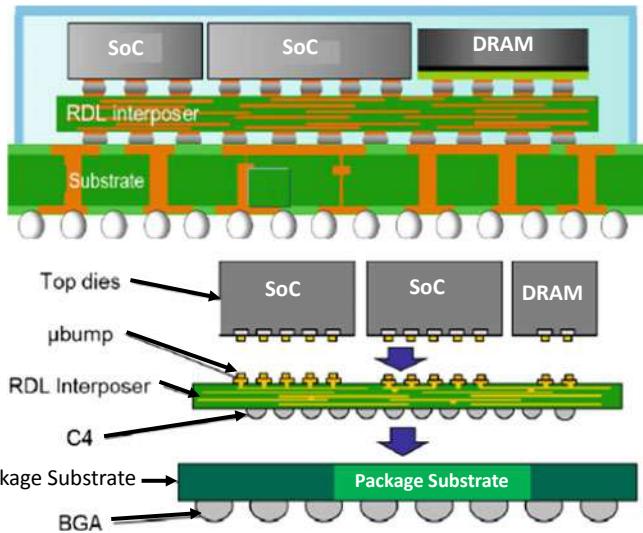
**Fig. 5.49** SEM images of ASE's organic interposer (chip-last) with stacked vias and non-stacked vias [56]

#### 5.12.4 TSMC's Multilayer RDL Interposer

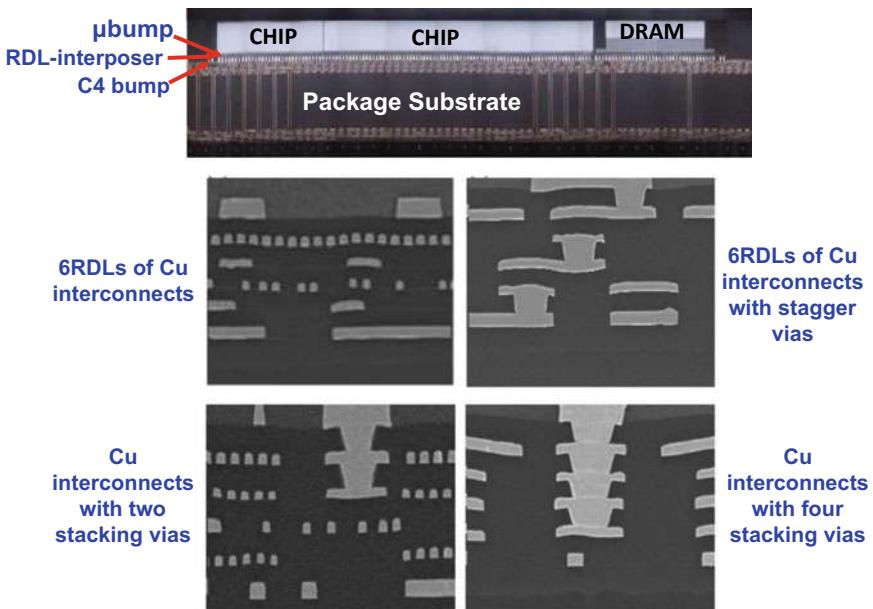
Figures 5.50 and 5.51 show TSMC's multilayer RDL-interposer for heterogeneous device and module integration [59]. The structure is basically the same as all the others [52–58]: (a) first fabricate the RDL-substrate (interposer), (b) wafer bumping and dicing into individual chips, (c) the chips are attached on the organic or inorganic RDL interposer with microbumps and underfill, (d) the RDL interposer is attached to a build-up package substrate with C4 bump with underfill, and (e) the package substrate is attached to a PCB with BGA (ball grid array) solder ball. Figure 5.51 shows some images of the assembly. It can be seen that the chips and DRAM are attached to a multilayer RDL-interposer with  $\mu$ bumps and then attached to a package substrate with C4 bumps. There are 6 RDLs with various via structures such as stager vias, two stacking vias, and four stacking vias.

#### 5.12.5 Shinko's 2.3D Organic Interposer

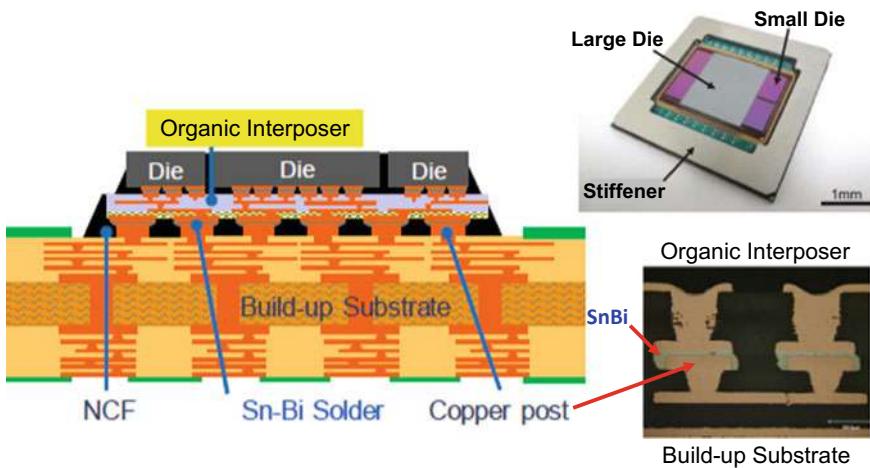
Figures 5.52, 5.53 and 5.54 show Shinko's 2.3D coreless organic interposer for high performance computing applications [60, 61]. It can be seen from Fig. 5.52 that Shinko use NCF (non-conductive film) as the underfill between the organic



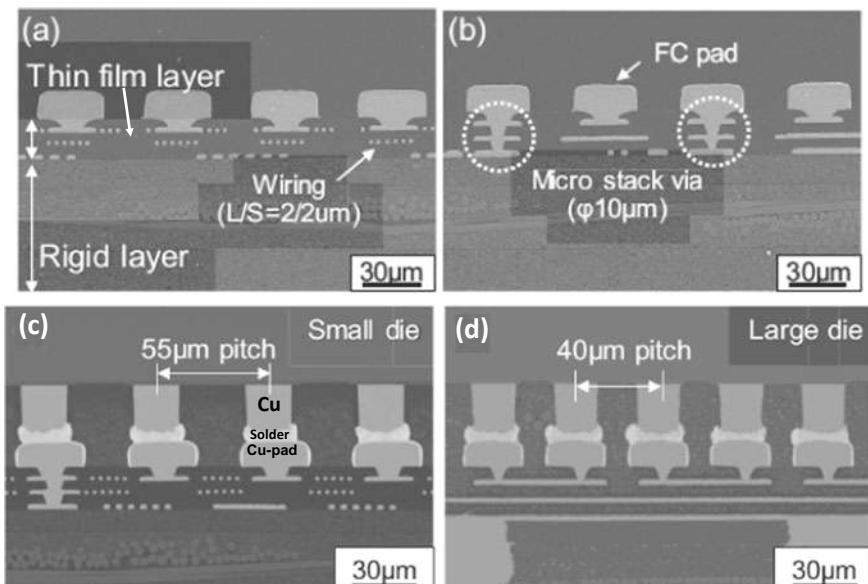
**Fig. 5.50** TSMC's fan-out (chip-last) organic RDL interposer [59]



**Fig. 5.51** SEM images of TSMC's chip-last organic RDL-interposer with stagger vias and stacking vias [59]

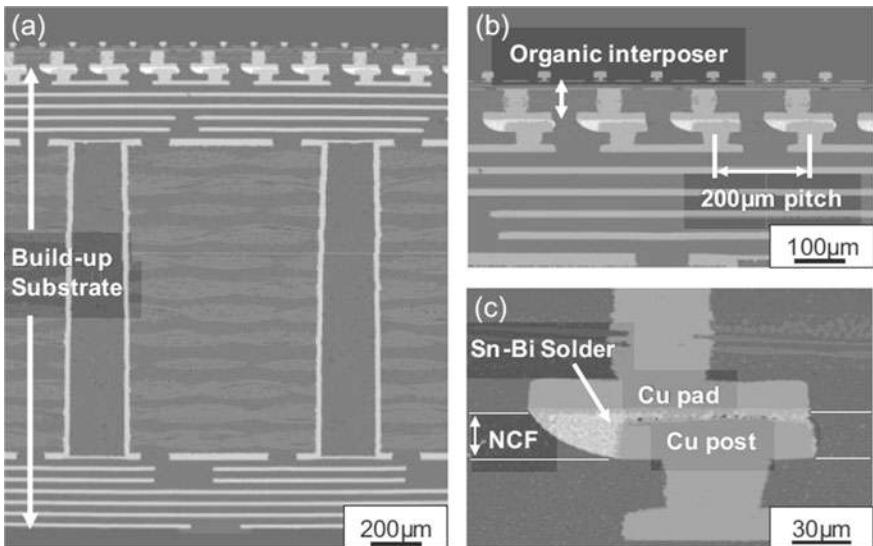


**Fig. 5.52** Shinko's fan-out (chip-last) organic interposer [60]



**Fig. 5.53** SEM images of chips-to-organic interposer bonding with SnAgCu solder alloy [60]

interposer and build-up package substrate. Also, between the organic interposer and the build-up package substrate, they use Sn-Bi solder alloy instead of the SnAgCu. In fabricating the organic RDL interposer they use a temporary carrier and a rigid layer so they don't have to switch to another temporary carrier before chip-to-panel bonding. Figure 5.53 shows the SEM images of the organic interposer (thin-film

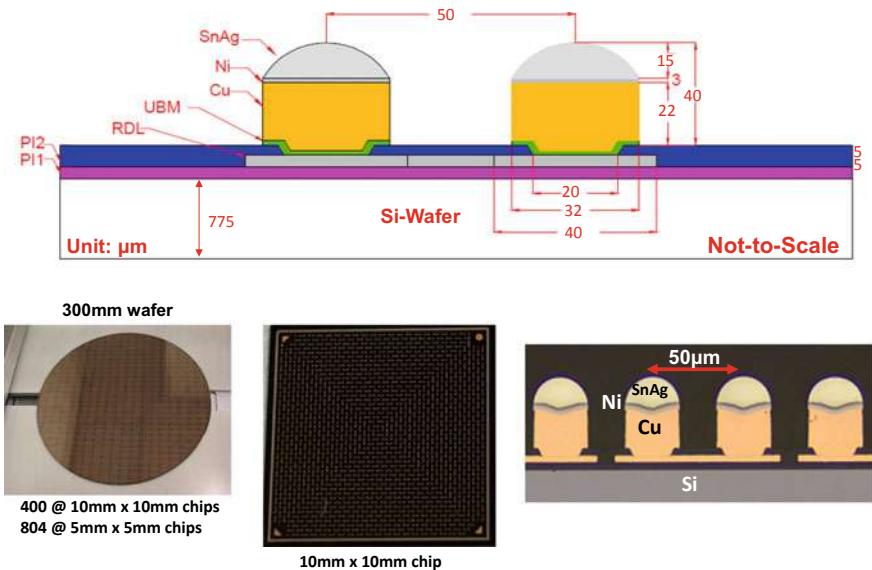


**Fig. 5.54** SEM images of organic interposer bonded on the build-up package substrate with SnBi solder alloy and NCF [60]

layer). It can be seen that the metal L/S are 2/2  $\mu\text{m}$  with stacking vias. In parallel, they perform the wafer (Cu-pillar + solder cap) bumping and dicing. The pitch is 40  $\mu\text{m}$  for the large chip and 55  $\mu\text{m}$  for the small chip. The chip-to-panel bonding is by TCB (thermocompression bonding) as shown in Fig. 5.53. Figure 5.54 shows the images of the assembly between the organic interposer and the build-up package substrate. It can be seen that the interconnect material is SnBi.

### 5.12.6 Unimicron's 2.3D RDL-Interposer

In this section, the fan-out panel-level chip-last packaging for heterogeneous integration is investigated. Emphasis is placed on the design, materials, process, and fabrication of: (a) the heterogeneous integration of one large chip (10 mm  $\times$  10 mm) and one small chip (5 mm  $\times$  5 mm) with 50  $\mu\text{m}$ -pitch (minimum), (b) a fine metal linewidth (L) and spacing (S) redistribution-layer (RDL)-first substrate on a 515 mm  $\times$  510 mm temporary glass carrier, (c) an ordinary build-up package substrate on a 510 mm  $\times$  510 mm panel, (d) the hybrid substrate which is by soldering the RDL-substrate on top of the build-up substrate, and (e) the chips to hybrid substrate bonding and underfilling. Reliability assessment by thermomechanical simulation includes thermal cycling of the heterogeneous integration of the two-chip package on the hybrid substrate that is performed by a nonlinear temperature- and time-dependent finite-element analysis [62].



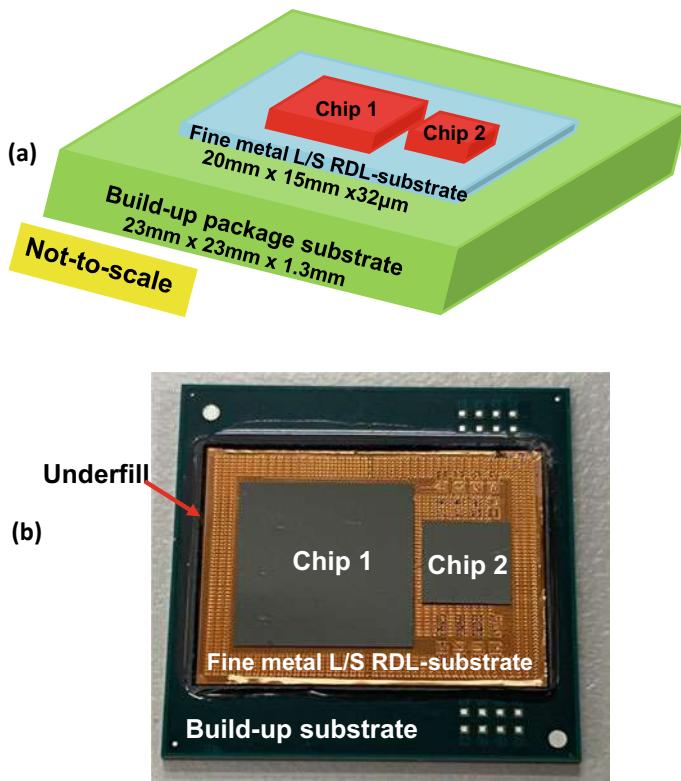
**Fig. 5.55** Test chips: 10 mm × 10 mm and 5 mm × 5 mm with 50  $\mu\text{m}$ -pitch

#### (A) TEST CHIPS

Figure 5.55 shows the test chips under consideration. It can be seen that the size of the large chip is 10 mm × 10 mm × 150  $\mu\text{m}$ . There are 3,592 area array pads which are daisy chained. The small chip is 5 mm × 5 mm × 150  $\mu\text{m}$  and with 1,072 area array daisy chained pads. For both chips, the pitch of the outer peripheral pads is 50  $\mu\text{m}$  and of all the inner pads is 200  $\mu\text{m}$ .

The wafer bumping of the large and small chips is with the standard PVD (physical vapor deposition) for seed layer and ECD (electrochemical deposition) for Cu and solder process. Then, dice the wafers into individual bumped chips.

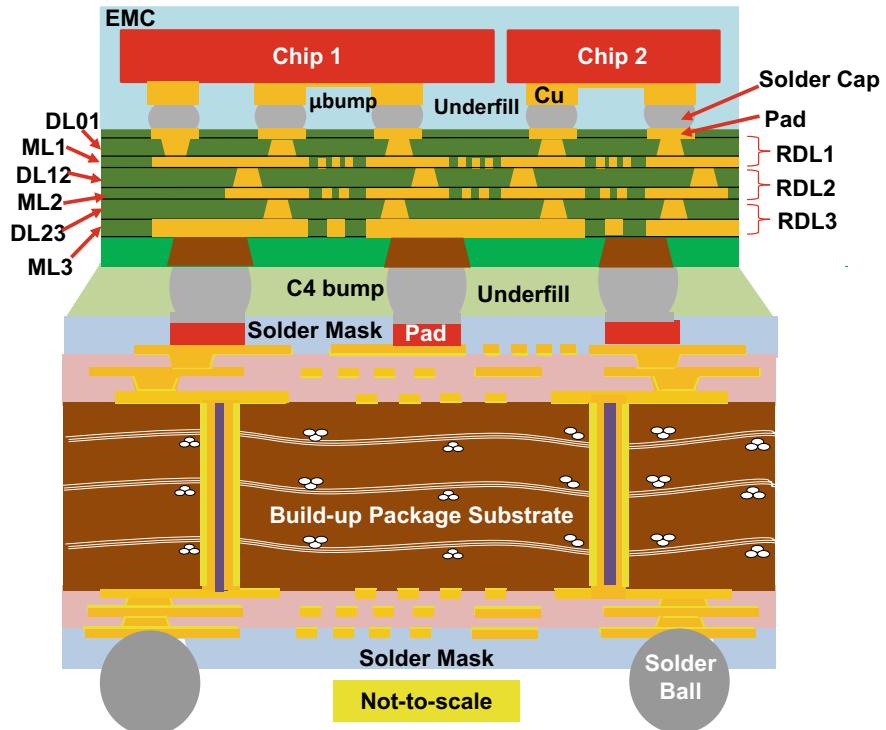
The cross section of both chips is also shown in Fig. 5.1. It can be seen that the Cu pad size is 40  $\mu\text{m}$  × 40  $\mu\text{m}$ , the Ti/Cu (0.1/0.2  $\mu\text{m}$ ) UBM (under bump metallurgy) pad size is 32  $\mu\text{m}$ -diameter, and the passivation (PI2) opening is 20  $\mu\text{m}$ -diameter. The diameter of the Cu-pillar is 32  $\mu\text{m}$  and its height is 22  $\mu\text{m}$ , and the height of the SnAg solder cap is 15  $\mu\text{m}$  plus a 3  $\mu\text{m}$  Ni-barrier.



**Fig. 5.56** **a** Schematic of the test package. **b** Assembled test package. Chips are bonded on the hybrid substrate which consists of the (20 mm × 15 mm) fine metal L/S RDL- substrate and (23 mm × 23 mm) build-up substrate

### (B) HETEROGENEOUS INTEGRATION TEST PACKAGE

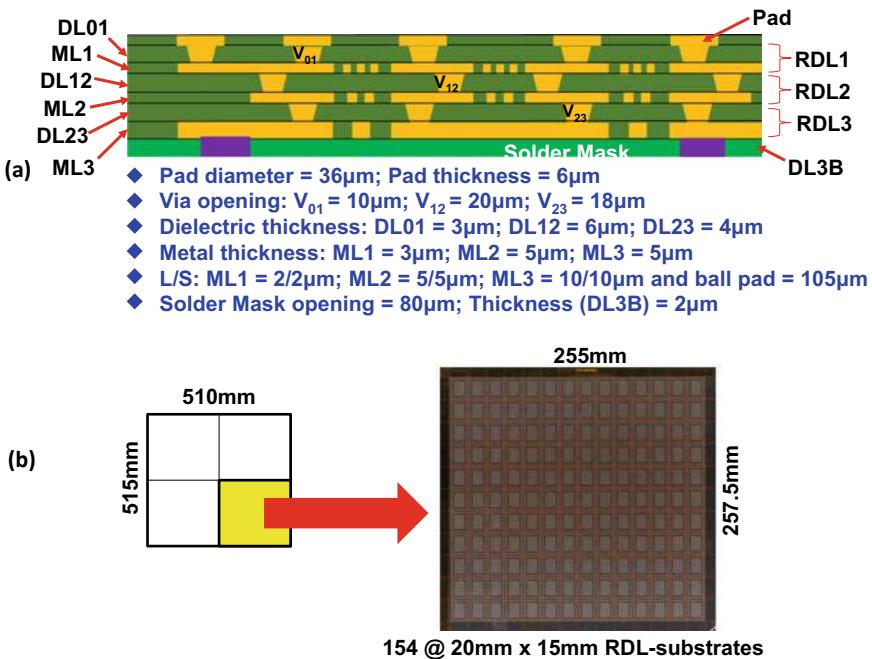
Figure 5.56a schematically shows the test package. It can be seen there are 2 chips of the heterogeneous integration, namely the large chip (Chip 1, 10 mm × 10 mm) and the small chip (Chip 2, 5 mm × 5 mm). The spacing (gap) between the large chip and small chips is 100 μm. The chips are bonded on top of the hybrid substrate which consists of the fine metal L/S RDL-substrate (20 mm × 15 mm × 32 μm) and build-up substrate (23 mm × 23 mm × 1.3 mm) as shown in Fig. 5.57.



**Fig. 5.57** Schematic of the cross section of the (chip-last) heterogeneous integration test package

The RDL-substrate has three RDLs and each RDL consists of one dielectric layer (DL) and one metal layer (ML). The line width and spacing of ML1, ML2, and ML3 of RDL1, RDL2, and RDL3, respectively are  $2/2 \mu\text{m}$ ,  $5/5 \mu\text{m}$ , and  $10/10 \mu\text{m}$  as shown in Fig. 5.58a. The thickness of ML1, ML2, and ML3 are, respectively  $3 \mu\text{m}$ ,  $5 \mu\text{m}$ , and  $5 \mu\text{m}$ . The thickness of DL01 (dielectric layer between the Cu pad and ML1), DL12 (dielectric layer between ML1 and ML2), and DL23 (dielectric layer between ML2 and ML3) are, respectively  $3 \mu\text{m}$ ,  $6 \mu\text{m}$ , and  $4 \mu\text{m}$ . The pad diameter and thickness are  $35 \mu\text{m}$  and  $6 \mu\text{m}$ , respectively. The  $V_{01}$  (via connecting between the pad and ML1) is  $10 \mu\text{m}$ ,  $V_{12}$  (via connecting between ML1 and ML2) is  $20 \mu\text{m}$ , and  $V_{23}$  (via connecting between ML2 and ML3) is  $18 \mu\text{m}$ . The solder mask (resist) opening and thickness are, respectively  $80 \mu\text{m}$  and  $2 \mu\text{m}$ .

The temporary panel for fabricating the RDL-substrate for the heterogeneous integration of 2-chip package is shown in Fig. 5.58b. It can be seen that the panel size is  $515 \text{ mm} \times 510 \text{ mm}$  and is made of glass. The panel is divided into four strips and each strip ( $257.5 \text{ mm} \times 255 \text{ mm}$ ) has 154 ( $20 \text{ mm} \times 15 \text{ mm}$ ) RDL-substrates. Thus, in one shot, it can make RDL-substrates for 1,232 chips in 616 heterogeneous integration packages.



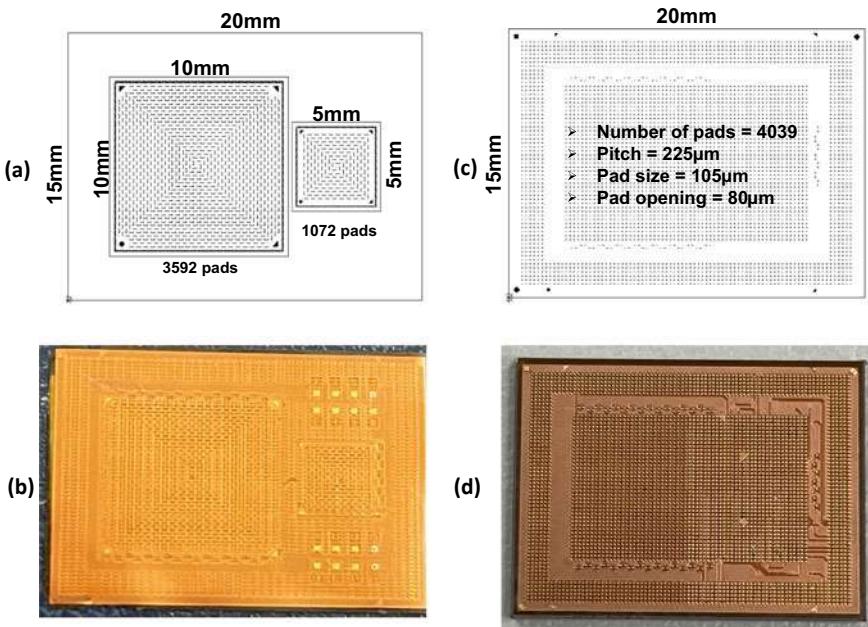
**Fig. 5.58** **a** Fine metal L/S RDL-substrate. **b** Panel for fabricating the RDL-substrate and the assembled one

The top-view and bottom-view of the 20 mm  $\times$  15 mm RDL-substrate of the heterogeneous integration of the 2-chip test package are shown in Fig. 5.59. It can be seen that:

- There are  $3,592 + 1,072 = 4,664$  pads on the top of the RDL-substrate, Figs. 5.59a. These pads are for the chips-to-substrate bonding,
- There are 4,039 solder ball pads (105  $\mu\text{m}$ -diameter) on a 0.225 mm-pitch at the bottom of the RDL-substrate, Fig. 5.59c. The pads are SMD (solder mask defined) and the solder mask opening is 80  $\mu\text{m}$ . These pads are for Sn3Ag0.5Cu lead-free C4 solder bump mounting and the solder ball-diameter is 80  $\mu\text{m}$ .

### (C) HYBRID SUBSTRATE FABRICATION

The key process steps for fabricating the RDL-first substrate, build-up package substrate, and hybrid substrate are shown in Fig. 5.60.



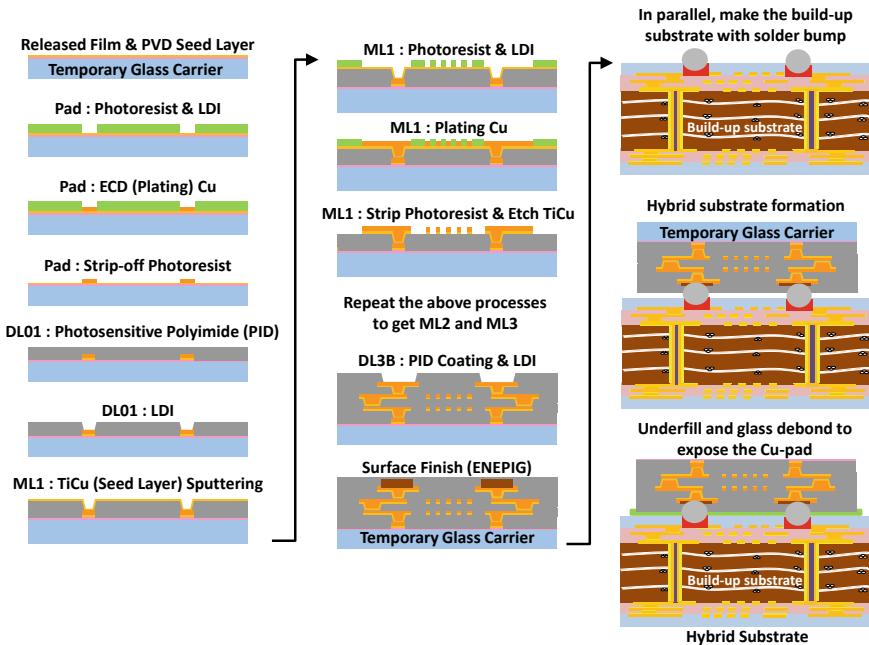
**Fig. 5.59** **a** Schematic of the top-view of RDL-substrate. **b** Top-view of the fabricated RDL-substrate. **c** Schematic of the bottom-view of RDL-substrate. **d** Bottom-view of the fabricated RDL-substrate

### (a) RDL-First Substrate Fabrication

In order to increase the throughput, the fabrication of the RDL-first substrate is on a 515 mm × 510 mm panel. First, slit coat a sacrificial layer (released film) on a temporary glass carrier and then PVD a Ti/Cu seed layer. It is followed by photoresist and laser direct imaging (LDI) development. Then, ECD Cu and strip off the photoresist to get the contact pad.

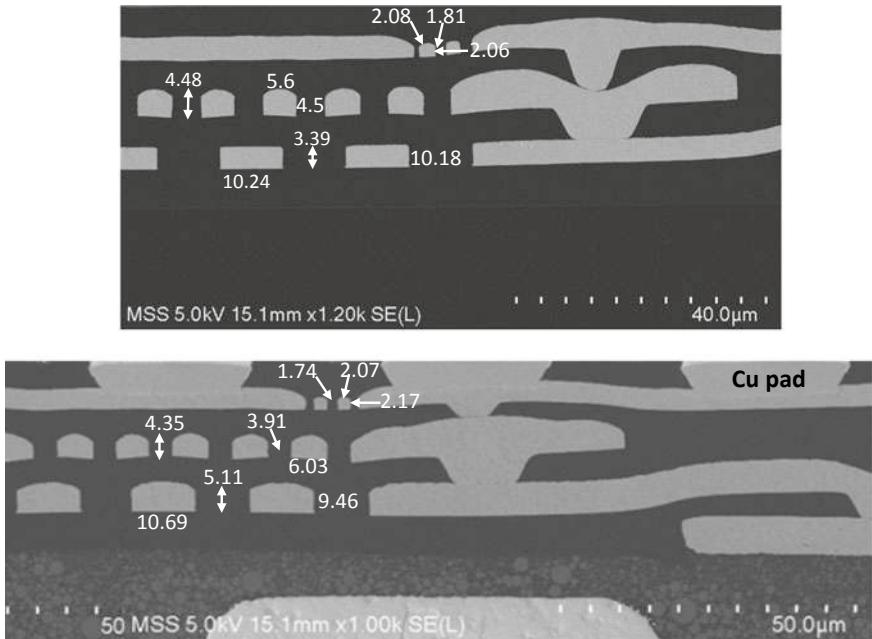
It is followed by slit coating a PID (photoimageable dielectric) and LDI to get the first dielectric layer (DL01) of RDL1. Then, sputter the Ti/Cu seed layer, photoresist, LDI and develop, and ECD the Cu. It is followed by stripping off the photoresist and etching off the TiCu seed layer to get the first metal layer (ML1) of RDL1. Repeat the same process steps to get DL12 and ML2 of RDL2, and DL23 and ML3 of RDL3. Figure 5.59b shows the photo image of the fabricated top-side of the RDL-substrate.

After making the ML3, it is followed by slit coating a PID and LDI to get the passivation (or solder mask). Then, surface finishing with ENEPIG (electroless nickel electroless palladium immersion gold). The fabrication of the fine metal L/S RDL-substrate is completed. Figure 5.59d shows the photo image of the bottom-side of the RDL-substrate.



**Fig. 5.60** Key process steps to fabricate the RDL-first hybrid substrate (fine metal L/S RDL-substrate + build-up substrate)

Figure 5.61 shows the scanning electron microscope (SEM) images of a typical cross section of the RDL-substrate. This cross section is showing (including) all three ML1, ML2, and ML3, and the contact pad. A closer look at the SEM images, it can be seen that for RDL1, the line width is not exactly equals to  $2 \mu\text{m}$ , but  $2.07, 2.08 \mu\text{m}, \dots$  the spacing is not exactly equals to  $2 \mu\text{m}$ , but  $1.74, 1.81 \mu\text{m} \dots$  the thickness is not exactly equals to  $3 \mu\text{m}$ , but  $2.06, 2.17 \mu\text{m}, \dots$  For RDL2, the line width is not exactly equals to  $5 \mu\text{m}$ , but  $5.6, 6.03 \mu\text{m}, \dots$  the spacing is not exactly equals to  $5 \mu\text{m}$ , but  $3.91, 4.5 \mu\text{m} \dots$  the thickness is not exactly equals to  $5 \mu\text{m}$ , but  $4.35, 4.48 \mu\text{m}, \dots$  For RDL3, the line width is not exactly equals to  $10 \mu\text{m}$ , but  $10.24, 10.69 \mu\text{m}, \dots$  the spacing is not exactly equals to  $10 \mu\text{m}$ , but  $9.46, 10.18 \mu\text{m} \dots$  the thickness is not exactly equals to  $5 \mu\text{m}$ , but  $3.39, 5.11 \mu\text{m}, \dots$  Thus, there are rooms for improvements such as use better PID, higher resolution LDI or a stepper.

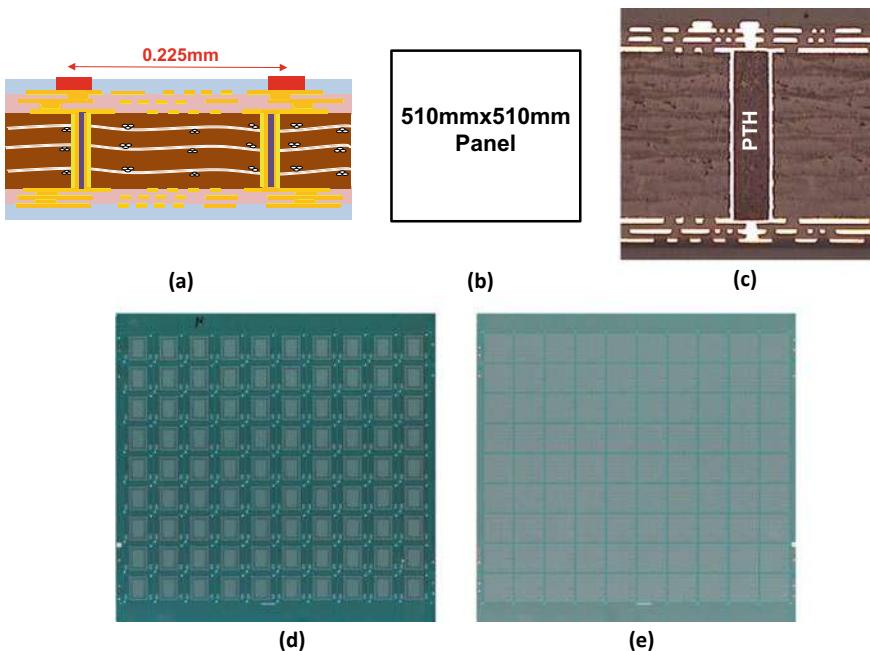


**Fig. 5.61** Cross sections of SEM image of RDL-substrate

### (b) Build-up Package Substrate Fabrication

The build-up package substrate ( $23\text{ mm} \times 23\text{ mm} \times 1.3\text{ mm}$ ) is a 2-2-2 structure as schematically shown in Fig. 5.62a. There are 4,039 pads on a  $0.225\text{ mm}$ -pitch on each substrate. It is fabricated on a  $510\text{ mm} \times 510\text{ mm}$  panel, Fig. 5.62b, by a conventional method. Figure 5.62c shows a typical cross section image of the 2-2-2 build-up substrate. Figures 5.62d, e show, respectively the top-view and bottom-view of the fabricated build-up package substrate panel.

Figure 5.63 shows the individual build-up package substrate. Figures 5.63a, b show, respectively the schematic and fabricated top-side of the package. While Figs. 5.63c, d show, respectively the schematic and fabricated bottom-side of the package. It can be seen that the top-side of the package substrate matches with the bottom-side of the RDL-substrate, Figs. 5.59c, d. There are 475 pads with  $1\text{ mm}$ -pitch on the bottom side of the substrate. The pad size is  $500\text{ }\mu\text{m}$  and is solder mask defined with the solder mask opening =  $300\text{ }\mu\text{m}$ .



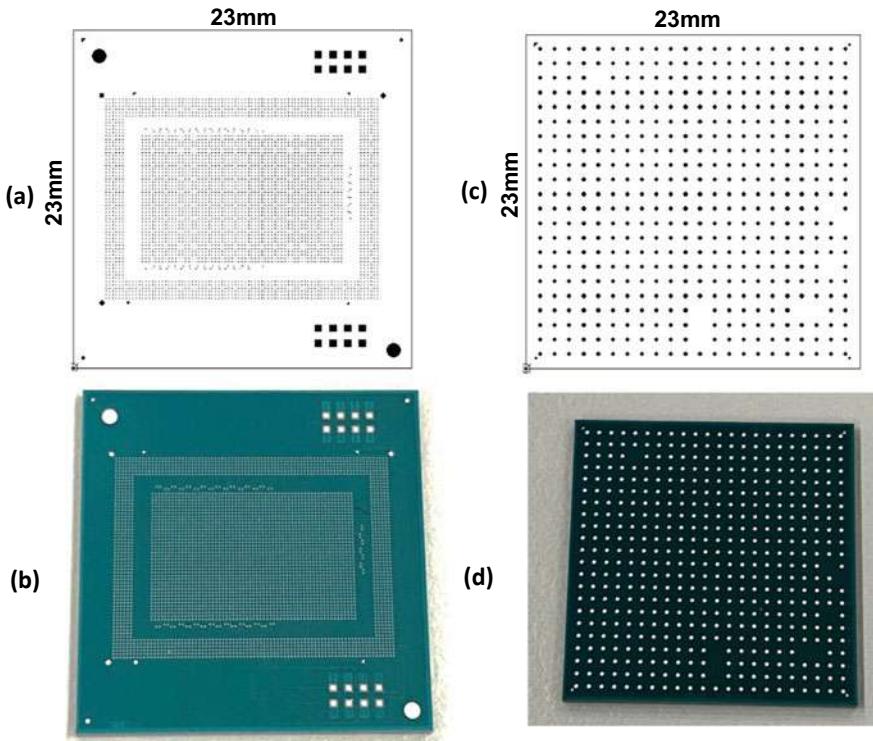
**Fig. 5.62** 2-2-2 build-up package substrate panel. **a** Schematic. **b** Panel size. **c** Cross section image. **d** Tow-view of the fabricated build-up substrate. **e** Bottom-view of the fabricated build-up substrate

### (c) C4 Bump Formation

The C4 bumps are fabricated by stencil printing a Sn<sub>3</sub>Ag0.5Cu solder paste with a 29  $\mu\text{m}$ -thickness stainless steel stencil on top of the build-up package substrate. During solder reflow process, because of the surface tension of the molten solder, which creates smooth truncated spherical 30  $\mu\text{m}$ -diameter solder bumps as shown in Fig. 5.64.

### (d) Warpage Measurements

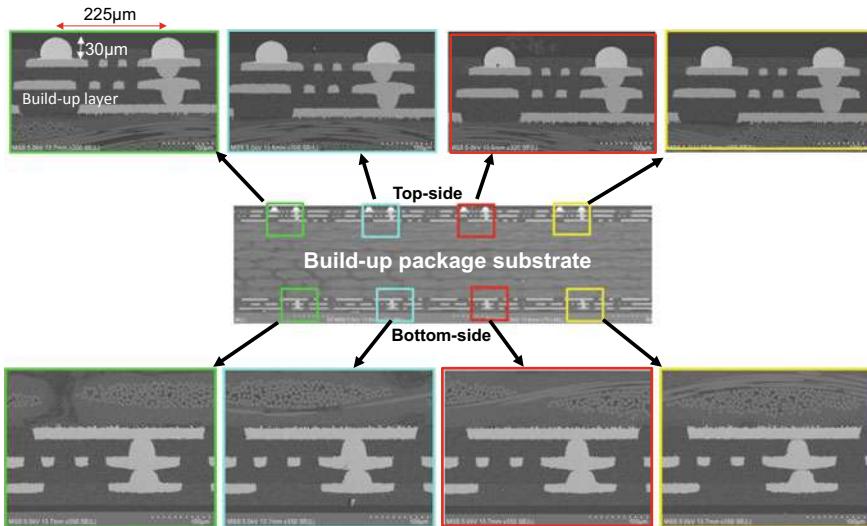
The warpage of the build-up package substrate (BU), fine metal L/S RDL-substrate with glass carrier RDL(G), and fine metal L/S RDL-substrate with organic carrier RDL(O) at various temperatures has been measured by the shadow Moire method via the TherMoire Platform. The results are shown in Fig. 5.65. It can be seen that the warpage of BU and RDL (G) is very small. However, the warpage of RDL (O) is very large compared with the others. (This is because of the thermal expansion mismatch between the glass carrier and the RDL-substrate is smaller than that between the organic carrier and the RDL-substrate). Thus, in this study, the hybrid substrate will be formed by the combination of the build-up package substrate and the fine metal L/S RDL-substrate with glass carrier.



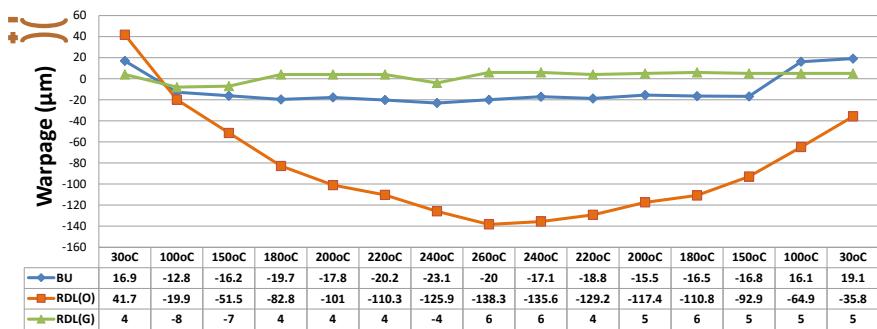
**Fig. 5.63** Individual build-up package substrate. **a** Schematic of the top-view of the build-up substrate. **b** Top-view of the fabricated build-up substrate. **c** Schematic of the bottom-view of the build-up substrate. **d** Bottom-view of the fabricated build-up substrate

#### (e) Hybrid Substrate Formation

Now that we have the fine metal L/S RDL-substrate with glass carrier and the build-up package substrate with solder bumps ready, it is time to fabricate the hybrid substrate as shown in Fig. 5.60. First, use a lookup and look-down camera to identify the location of the bumps on the package substrate and the pads on the RDL-substrate with glass carrier; second apply flux on both the bumps and pads; and third, pick and place the RDL-substrate with glass carrier on the package substrate then reflow. Figure 5.66 shows the top view of an assembled hybrid substrate. A typical cross section SEM image of the hybrid substrate is shown in Fig. 5.67 and close-up images are shown in Fig. 5.68. It can be seen that the fine metal L/S RDL-substrate, solder joints, underfill, and the build-up package substrate are properly assembled.



**Fig. 5.64** SEM images of the fabricated 2-2-2 build-up package substrate with C4 bumps

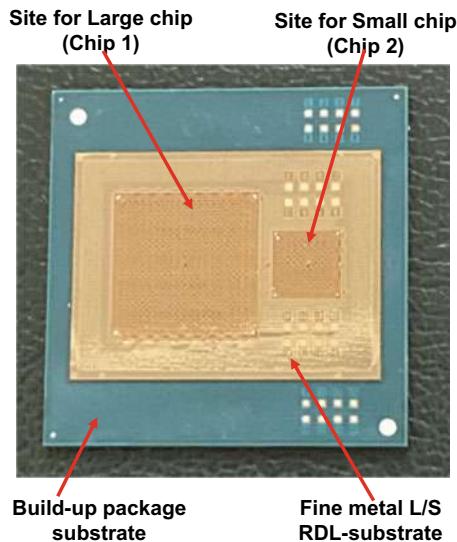


**Fig. 5.65** Shadow Moire warpage measurement of build-up substrate (BU), fine metal L/S RDL-substrate on glass carrier RDL(G), and fine metal L/S RDL-substrate on organic carrier RDL(O)

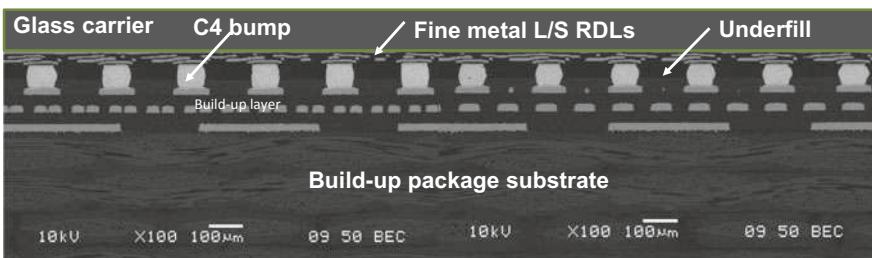
#### (D) FINAL PACKAGE ASSEMBLY

##### (a) Debond The Temporary Glass Carrier

Before the final package assembly, we have to remove the glass carrier to expose the bonding pads on the fine metal L/S RDL-substrate as shown in Fig. 5.60. By scanning a laser on the glass, the sacrificial layer will become a powder and it is very easy to remove the glass carrier. Then, chemical clean the surface.



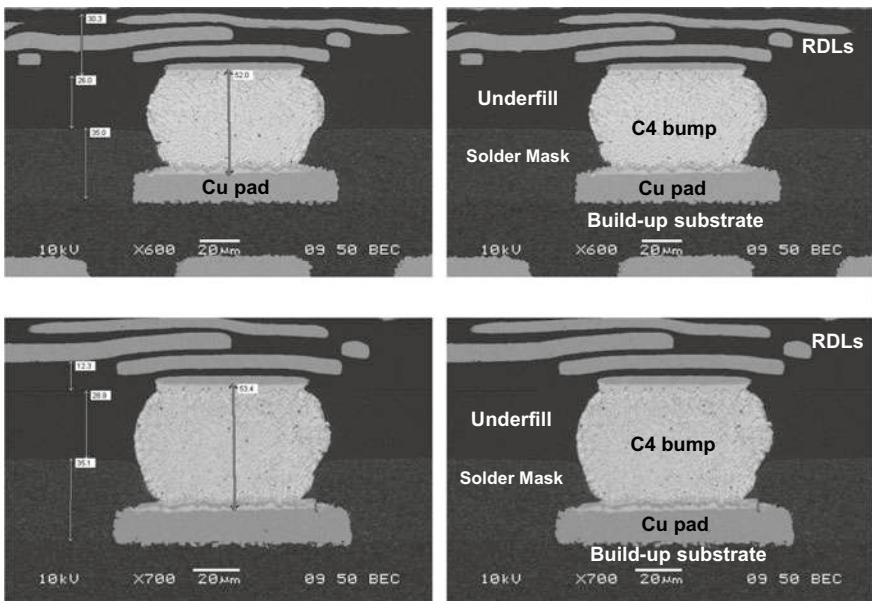
**Fig. 5.66** Hybrid substrate = fine metal L/S RDL-substrate with glass carrier soldered on top of the build-up package substrate



**Fig. 5.67** Cross section image of the hybrid substrate

### (b) Chips-to-Hybrid Substrate Bonding

Now that we have the microbumped chips (Fig. 5.55) and the hybrid substrate (Figs. 5.66, 5.67 and 5.68) ready, it is time to do the final assembly. First, use a lookup and look-down camera to identify the location of the microbumps on the chips and the bonding pads on the hybrid-substrate; second apply flux on both the bumps and pads; and third, pick and place the chips on the hybrid substrate, then reflow. Figure 5.56b shows the assembled heterogeneous integration of the 2-chip package.



**Fig. 5.68** Close-up look at the cross section SEM images of the hybrid substrate

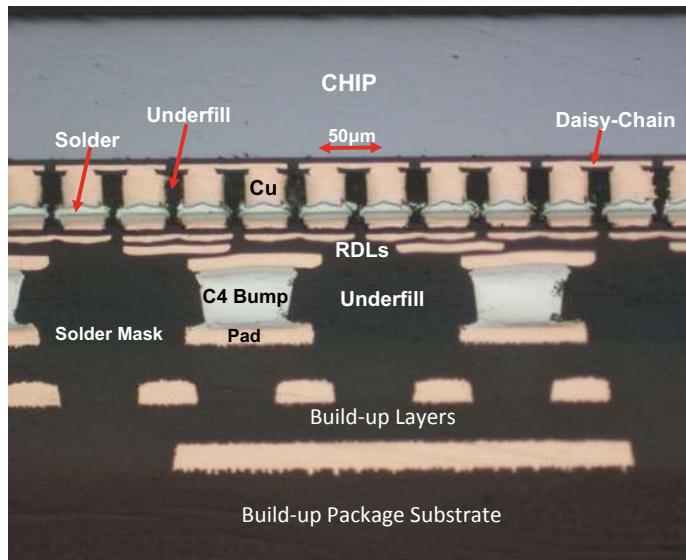
### (c) Underfill

After underfilling of those 2 chips, a typical cross section image of the final assembly is shown in Fig. 5.69. It can be seen that the chip, microbumps, underfill, RDL-substrate, C4-bumps, and build-up package substrate are properly done.

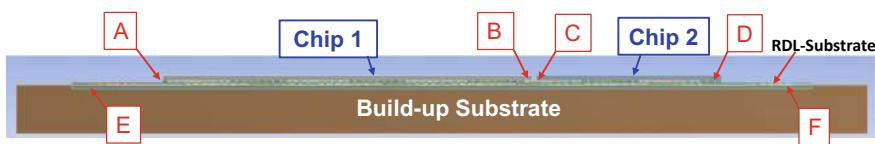
## (E) THERMAL CYCLING SIMULATION

### (a) The Structure and Finite Element Modeling

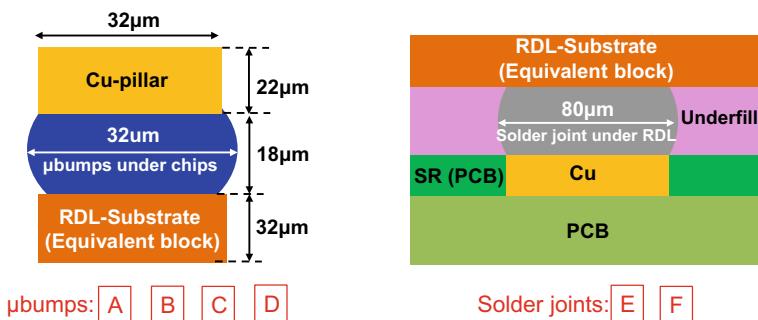
The focus of the present thermal cycling simulation of the final assembly of the heterogeneous integration of the 2-chip on hybrid substrate package is on the microbump solder joints and C4-bump solder joints reliability as shown in Fig. 5.70. A 2-D generalized plane-strain finite element modeling as shown in Fig. 5.71 is performed. Fine meshes are used for critical locations such as microbump solder joints A, B, C, and D connecting the chips and the RDL-substrate and the C4-bump solder joints E and F connecting the RDL-substrate and the build-up package substrate. The 3-layer RDL-substrate consists of the Cu conductor layers and the ABF dielectric layers, which is represented as an equivalent block.



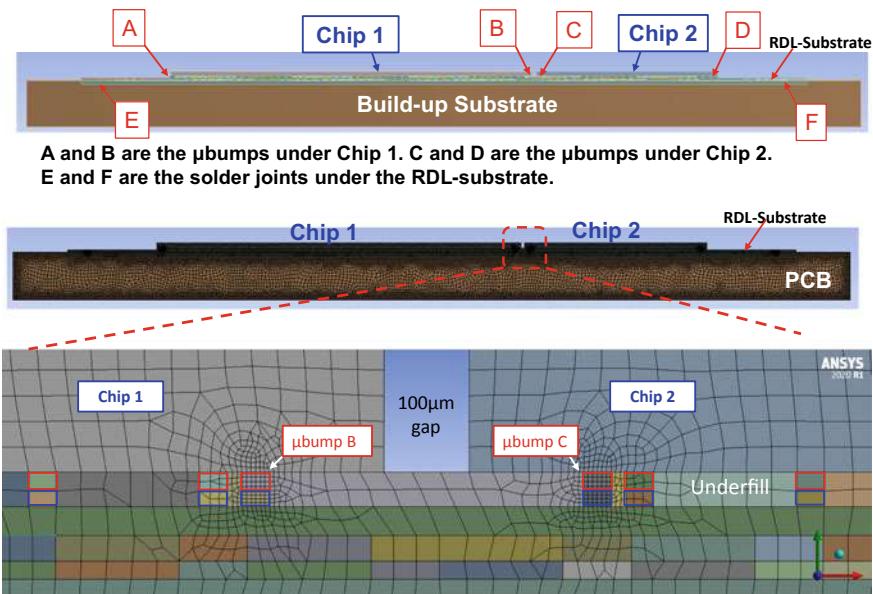
**Fig. 5.69** Heterogeneous integration of 2-chip package on the hybrid substrate = fine metal L/S RDL-substrate + build-up substrate



A and B are the  $\mu$ bumps under Chip 1. C and D are the  $\mu$ bumps under Chip 2.  
E and F are the solder joints under the RDL-substrate.



**Fig. 5.70** The structure and  $\mu$ bump joints and solder joints



**Fig. 5.71** Finite element modeling of the PCB assembly of heterogeneous integration of 2 chips on hybrid substrate

### (b) Material Properties for Simulation

The material properties for modeling are shown in Table 5.1. All the materials are assumed to be constant except the Sn<sub>3</sub>Ag0.5Cu which is time and temperature dependent and its constitutive equation is also shown in Table 5.1.

### (c) Kinetic Boundary Condition

The temperature boundary condition for simulation is shown in Fig. 5.72. It can be seen that the temperature is  $-40 \leq 85^{\circ}\text{C}$ . The cycle time is 60 min and the ramp-up, ramp-down, dwell-at-hot, and dwell-at-cold are each 15 min.

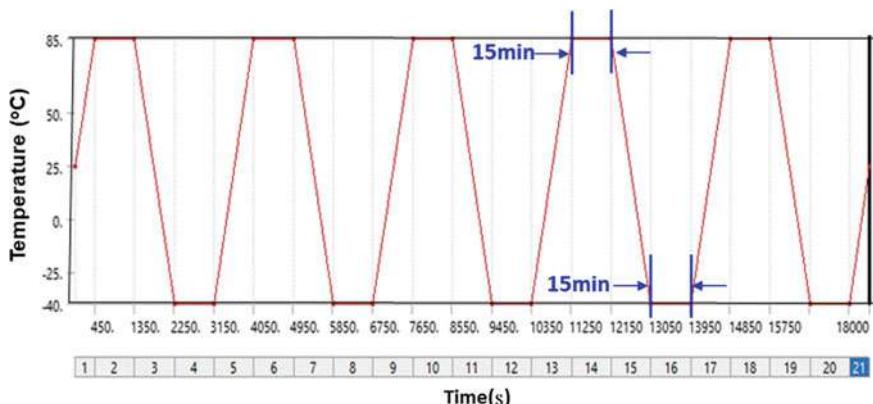
### (d) Simulation Results—Deformation

The deformed shape (color contours) and the undeformed shape (dark lines) of the heterogeneous integration of 2 chips on the hybrid substrate assembly are shown in Fig. 5.73. It can be seen from Fig. 5.73a that at 450 s ( $85^{\circ}\text{C}$ ), the hybrid substrate expands more than the chips and the structure is deformed in a concave shape (smiling face). It can also be seen from Fig. 5.73b that at 2250 s ( $-40^{\circ}\text{C}$ ), the hybrid substrate shrinks more than the chips and the structure is deformed into a convex shape (crying face). These results are expected.

**Table 5.1** Material properties for simulations

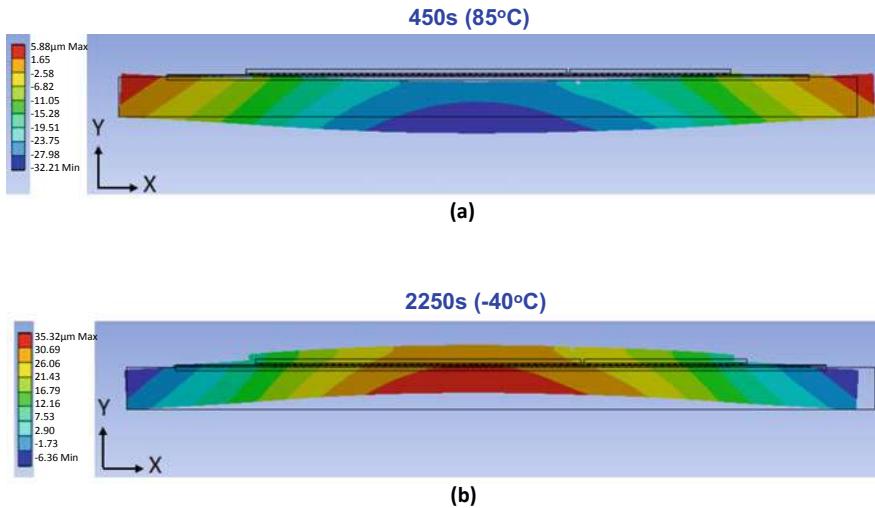
Materials	CTE ( $10^{-6}/^{\circ}\text{C}$ )	Young's modulus (GPa)	Poisson's ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ ; $\alpha_z = 70$	$E_x = E_y = 22$ ; $E_z = 10$	0.28
Solder mask (RDL)	7.0	7.0	0.3
Solder	$21 + 0.017T$ ( $^{\circ}\text{C}$ )	$49 - 0.07T$ ( $^{\circ}\text{C}$ )	0.3
EMC(ABF)	7.0	7.0	0.3
Silicon	2.8	131	0.278
Solder mask (PCB)	39	4.1	0.3
RDL Equiv. block	14.08	70.53	0.32
Underfill	50	4.5	0.35

The constitutive equation of solder:  $\frac{d\varepsilon}{dt} = 500000[\sinh(0.01\sigma)]^5 \exp\left(-\frac{5800}{T}\right)$  where  $T$  is in Kelvin and  $\sigma$  is in MPa

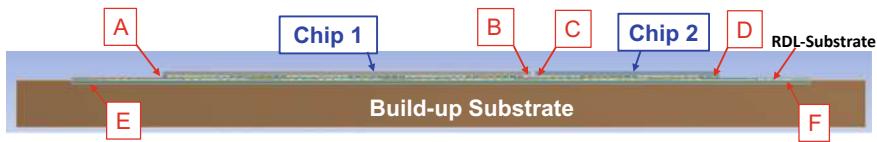
**Fig. 5.72** Temperature boundary condition

### (e) Simulation Results—Accumulated Creep Strain

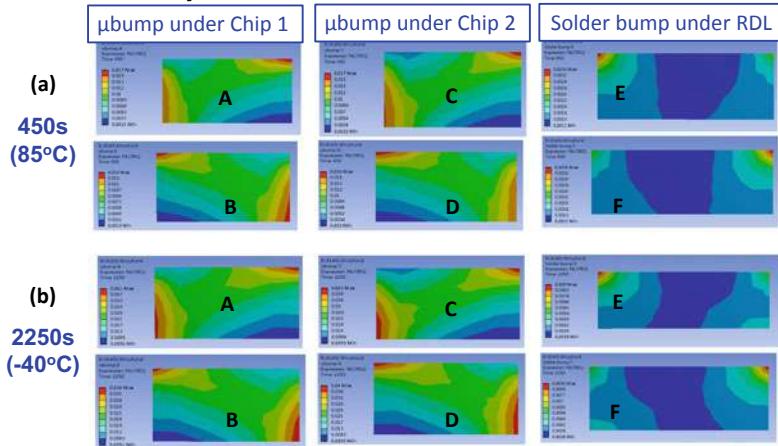
The accumulated creep strain contour distributions at the critical microbump solder joints A, B, C, and D and the critical C4-bump solder joints E and F are shown in Fig. 5.74 and the maximum accumulate creep strain time-history at these locations



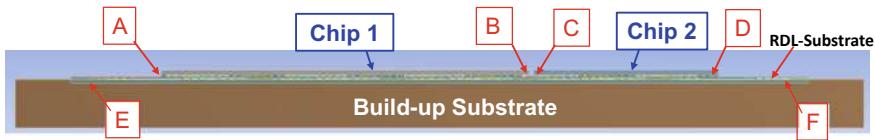
**Fig. 5.73** Deformed shape (color contours) and un-deformed shape (dark lines). **a** At 450 s (85 °C). **b** At 2250 s (-40 °C)



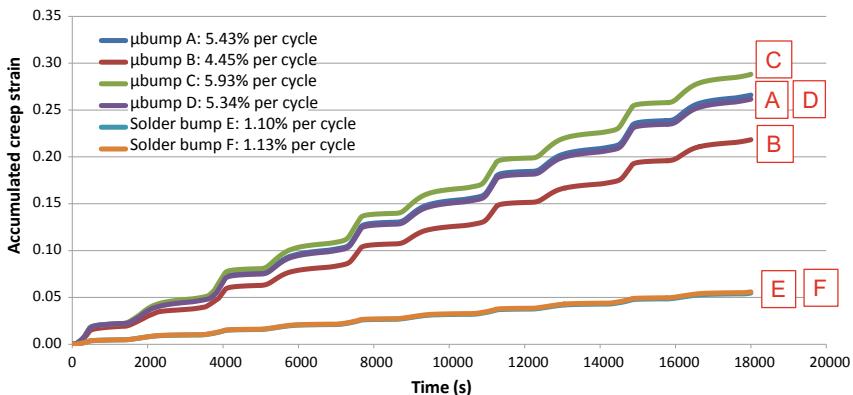
A and B are the **µbumps under Chip 1**. C and D are the **µbumps under Chip 2**.  
E and F are the **solder joints under the RDL-substrate**.



**Fig. 5.74** Accumulated creep strain contour distributions in µbump joints A, B, C, and D, and solder joints E and F



A and B are the  $\mu$ bumps under Chip 1. C and D are the  $\mu$ bumps under Chip 2.  
E and F are the solder joints under the RDL-substrate.

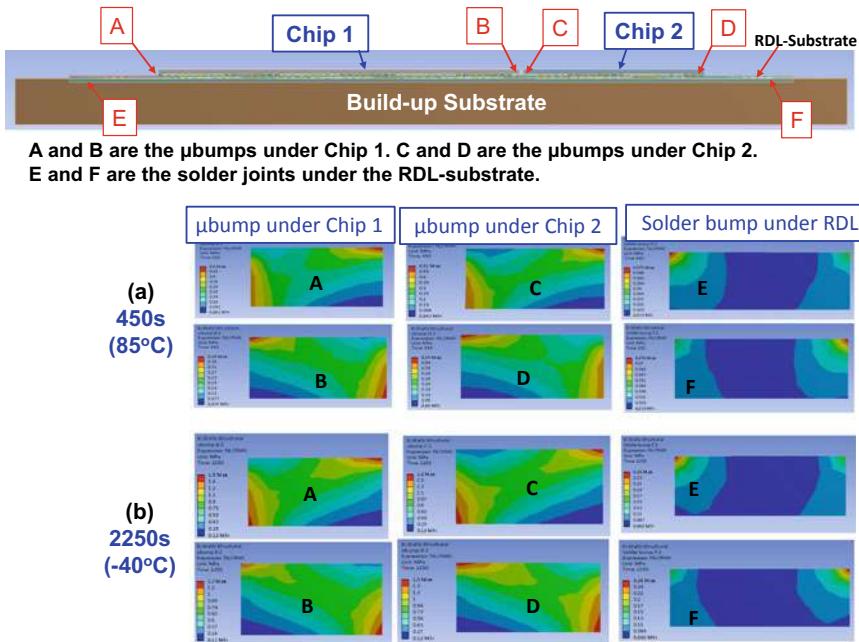


**Fig. 5.75** Accumulated creep strain time-history in  $\mu$ bump joints A, B, C, and D, and solder joints E and F

are shown in Fig. 5.75. It can be seen that the maximum accumulated creep strain occurs near the corner of the solder joints A, B, C, D, E, and F. Also, the maximum accumulated creep strain per cycle in the microbump solder joints A, B, C, and D is at least 4 times larger than that in the C4-bump solder joints E and F. This is because the thermal expansion mismatch between the chips and the RDL-substrate is larger than that between the RDL-substrate and the build-up package substrate. The maximum accumulated creep strain per cycle in the microbump solder joints is 5.93% and it occurs at a very small area. Thus, this structure should be reliable for most operating conditions.

#### (f) Simulation Results—Creep Strain Energy Density

The creep strain energy density contour distributions at the microbump solder joints A, B, C, and D and the C4-bump solder joints E and F are shown in Fig. 5.76 and the maximum creep strain energy density time-history at these solder joints are shown in Fig. 5.77. It can be seen that the maximum creep strain energy density occurs near the corner of the solder joints A, B, C, D, E, and F. Also, the maximum creep strain energy density per cycle in the microbump solder joints A, B, C, and D is at least 5 times larger than that in the C4-bump solder joints E and F. Again, this is because the thermal expansion mismatch between the chips and the RDL-substrate is larger than that between the RDL-substrate and the build-up package substrate. The maximum



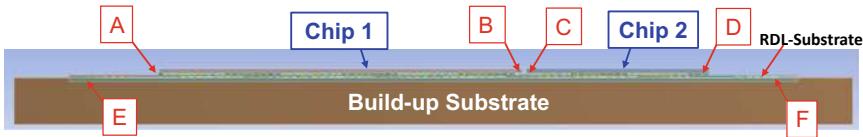
**Fig. 5.76** Creep strain energy density contour distributions in μbump joints A, B, C, and D, and solder joints E and F

creep strain energy density per cycle in the microbump solder joints is only 2.63 MPa and it occurs at a very small area. Again, this structure should be reliable for most operating conditions.

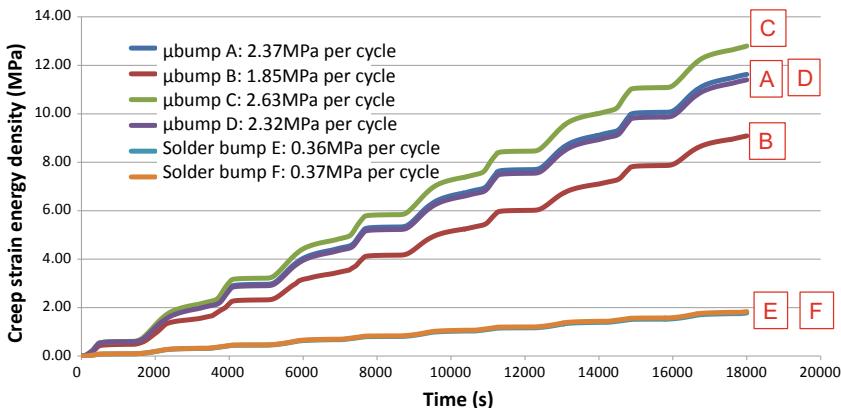
### 5.13 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- 2D IC integration on organic substrate is in HVM such as the SiP and homogeneous integration and will be used the most.
- 2.1D IC integration with thin-film layers on top of the build-up package substrate is not in HVM yet due to yield loss. 2.1D IC integration with EMIB (by Intel) is in small volume manufacturing. TSMC's LSI is during qualification and is scheduled to be in production in the second half of 2021 or early 2022.
- 2.3D IC integration with coreless organic interposer by PCB technology is in small volume manufacturing. 2.3D IC integration with coreless inorganic/organic RDL interposers by fan-out (either chip-first or chip-last) technology is scheduled to be in HVM by ASE in 2021.



A and B are the  $\mu$ bumps under Chip 1. C and D are the  $\mu$ bumps under Chip 2. E and F are the solder joints under the RDL-substrate.



**Fig. 5.77** Creep strain energy density time-history in  $\mu$ bump joints A, B, C, and D, and solder joints E and F

## References

1. Lau, J. H., P. Tzeng, C. Lee, C. Zhan, M. Li, J. Cline, K. Saito, Y. Hsin, P. Chang, Y. Chang, J. Chen, S. Chen, C. Wu, H. Chang, C. Chien, C. Lin, T. Ku, R. Lo, and M. Kao, “Redistribution Layers (RDLs) for 2.5D/3D IC Integration”, *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 11, No. 1, First Quarter 2014, pp. 16–24.
2. Lau, J. H., “8 Ways to Make RDLs for FOW/PLP”, *Chip Scale Review*, Vol. 22, May/June 2018, pp. 11–19.
3. Lau, J. H., “Redistribution-Layers for Heterogeneous Integrations”, *Chip Scale Review*, Vol. 23, January/February 2019, pp. 20–25.
4. Kripesh, V., V. Rao, A. Kumar, G. Sharma, K. Houe, X. Zhang, K. Mong, N. Khan, and J. H. Lau, “Design and Development of a Multi-Die Embedded Micro Wafer Level Package”, *IEEE/ECTC Proceedings*, 2008, pp. 1544–1549.
5. Khong, C., A. Kumar, X. Zhang, S. Gaurav, S. Vempati, V. Kripesh, J. H. Lau, and D. Kwong, “A Novel Method to Predict Die Shift During Compression Molding in Embedded Wafer Level Package”, *IEEE/ECTC Proceedings*, 2009, pp. 535–541.
6. Sharma, G., S. Vempati, A. Kumar, N. Su, Y. Lim, K. Houe, S. Lim, V. Sekhar, R. Rajoo, V. Kripesh, and J. H. Lau, “Embedded Wafer Level Packages with Laterally Placed and Vertically Stacked Thin Dies”, *IEEE/ECTC Proceedings*, 2009, pp. 1537–1543. Also, *IEEE Transactions on CPMT*, Vol. 1, No. 5, May 2011, pp. 52–59.
7. Kumar, A., D. Xia, V. Sekhar, S. Lim, C. Keng, S. Gaurav, S. Vempati, V. Kripesh, J. H. Lau, and D. Kwong, “Wafer Level Embedding Technology for 3D Wafer Level Embedded Package”, *IEEE/ECTC Proceedings*, 2009, pp. 1289–1296.
8. Lim, Y., S. Vempati, N. Su, X. Xiao, J. Zhou, A. Kumar, P. Thaw, S. Gaurav, T. Lim, S. Liu, V. Kripesh, and J. H. Lau, “Demonstration of High Quality and Low Loss Millimeter Wave

- Passives on Embedded Wafer Level Packaging Platform (EMWLP)", *IEEE/ECTC Proceedings*, 2009, pp. 508–515. Also, *IEEE Transactions on Advanced Packaging*, Vol. 33, 2010, pp. 1061–1071.
9. Lau, J. H., "Patent Issues of Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 19, November/December 2015, pp. 42–46.
  10. Lau, J. H., N. Fan, and M. Li, "Design, Material, Process, and Equipment of Embedded Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 20, May/June 2016, pp. 38–44.
  11. Lau, J. H., M. Li, M. Li, T. Chen, I. Xu, X. Qing, Z. Cheng, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, P. Lo, K. Wu, J. Hao, S. Koh, R. Jiang, X. Cao, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, "Fan-Out Wafer-Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, 2018, September 2018, pp. 1544–1560.
  12. [12]Lau, J. H., M. Li, Y. Lei, M. Li, I. Xu, T. Chen, Q. Yong, Z. Cheng, K. Wu, P. Lo, Z. Li, K. Tan, Y. Cheung, N. Fan, E. Kuah, C. Xi, J. Ran, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, "Reliability of Fan-Out Wafer-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 148–162.
  13. Ko, C.T., H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. W. Lin, T. Chen, I. Xu, C. Chang, J. Pan, H. Wu, Q. Yong, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, K. Wu, J. Hao, R. Beica, M. Lin, Y. Chen, Z. Cheng, S. Koh, R. Jiang, X. Cao, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, "Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, September 2018, pp. 1561–1572.
  14. Ko, C. T., H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. Lin, C. Chang, J. Pan, H. Wu, Y. Chen, T. Chen, I. Xu, P. Lo, N. Fan, E. Kuah, Z. Li, K. Tan, C. Lin, R. Beica, M. Lin, C. Xi, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, "Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 141–147.
  15. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1–27.
  16. Lau, J. H., "Recent Advances and Trends in Heterogeneous Integrations", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 16, April 2019, pp. 45–77.
  17. Bu, L., F. Che, M. Ding, S. Chong, and X. Zhang, "Mechanism of Moldable Underfill (MUF) Process for Fan-Out Wafer Level Packaging", *IEEE/EPTC Proceedings*, 2015, pp. 1–7.
  18. Che, F. D. Ho, M. Ding, and D. Woo, "Study on Process Induced Wafer Level Warpage of Fan-Out Wafer Level Packaging", *IEEE/ECTC Proceedings*, 2016, pp. 1879–1885.
  19. Rao, V., C. Chong, D. Ho, D. Zhi, C. Choong, S. Lim, D. Ismael, and Y. Liang, "Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multilayer Fine Pitch RDL for Mobile Applications", *IEEE/ECTC Proceedings*, 2016, pp. 1522–1529.
  20. Chen, Z., F. Che, M. Ding, D. Ho, T. Chai, V. Rao, "Drop Impact Reliability Test and Failure Analysis for Large Size High Density FOWLP Package on Package", *IEEE/ECTC Proceedings*, 2017, pp. 1196–1203.
  21. Lim, T., and D. Ho, "Electrical design for the development of FOWLP for HBM integration", *IEEE/ECTC Proceedings*, 2018, pp. 2136–2142.
  22. Ho, S., H. Hsiao, S. Lim, C. Choong, S. Lim, and C. Chong, "High Density RDL build-up on FO-WLP using RDL-first Approach", *IEEE/EPTC Proceedings*, 2019, pp. 23–27.
  23. Boon, S., D. Wee, R. Salahuddin, and R. Singh, "Magnetic Inductor Integration in FO-WLP using RDLfirst Approach", *IEEE/EPTC Proceedings*, 2019, pp. 18–22.
  24. Hsiao, H., S. Ho, S. S. Lim, W. Ching, C. Choong, S. Lim, H. Hong, and C. Chong, "Ultra-thin FO Packageon-Package for Mobile Application", *IEEE/ECTC Proceedings*, 2019, pp. 21–27.
  25. Lin, B., F. Che, V. Rao, and X. Zhang, "Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging (FOPLP)", *IEEE/ECTC Proceedings*, 2019, pp. 1152–1158.
  26. Sekhar, V., V. Rao, F. Che, C. Choong, and K. Yamamoto, "RDL-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging", *IEEE/ECTC Proceedings*, 2019, pp. 2126–2133.

27. Huemoeller, R. and C. Zwenger, "Silicon wafer integrated fan-out technology," *Chip Scale Review*, March/April 2015, pp. 34–37.
28. Hiner, D., M. Kelly, R. Huemoeller, and R. Reed, "Silicon interposer-less integrated module - SLIM," *IMAPS/Device Packaging*, March 2015.
29. Hiner, D., M. Kolbehdari, M. Kelly, Y. Kim, W. Do, J. Bae, "SLIM™ advanced fan-out packaging for high performance multi-die solutions," *IEEE/ECTC Proceedings*, May 2017, pp. 575–580.
30. Kim, Y., J. Bae, M. Chang, A. Jo, J. Kim, S. Park, et al., "SLIM™, high density wafer-level fan-out package development with sub-micron RDL," *IEEE/ECTC Proceedings*, May 2017, pp. 18–13.
31. Zwenger, C., G. Scott, B. Baloglu, M. Kelly, W. Do, W. Lee, and J. Yi, "Electrical and Thermal Simulation of SWIFT™ High-density Fan-out PoP Technology", *IEEE/ECTC Proceedings*, May 2017, pp. 1962–1967.
32. Scott, G., J. Bae, K. Yang, W. Ki, N. Whitchurch, M. Kelly, C. Zwenger, J. Jeon, and T. Hwang, "Heterogeneous Integration Using Organic Interposer Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 885–892.
33. Ma, M., S. Chen, P. I. Wu, A. Huang, C. H. Lu, A. Chen, C. Liu, and S. Peng, "The development and the integration of the 5  $\mu\text{m}$  to 1  $\mu\text{m}$  half pitches wafer level Cu redistribution layers", *IEEE/ECTC Proceedings*, May 2016, pp. 1509–1514.
34. Lau, J. H., C. Ko, T. Peng, K. Yang, T. Xia, P. Lin, J. Chen, P. Huang, T. Tseng, E. Lin, L. Chang, C. Lin, and W. Lu, "Chip-Last (RDL-First) Fan-Out Panel-Level Packaging (FOPLP) for Heterogeneous Integration", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 17, No. 3, October 2020, pp. 89–98.
35. Lau, J. H., C. Ko, K. Yang, C. Peng, T. Xia, P. Lin, J. Chen, P. Huang, H. Liu, T. Tseng, E. Lin, and L. Chang, "Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125–1137.
36. Shimizu, N., W. Kaneda, H. Arisaka, N. Koizumi, S. Sunohara, A. Rokugawa, and T. Koyama, "Development of Organic Multi Chip Package for High Performance Application", *IMAPS Proceedings of International Symposium on Microelectronics*, October 2013, pp. 414–419.
37. Oi, K., S. Otake, N. Shimizu, S. Watanabe, Y. Kunimoto, T. Kurihara, T. Koyama, M. Tanaka, L. Aryasomayajula, and Z. Kutlu, "Development of New 2.5D Package with Novel Integrated Organic Interposer Substrate with Ultra-fine Wiring and High Density Bumps", *IEEE/ECTC Proceedings*, May 2014, pp. 348–353.
38. Uematsu, Y., N. Ushifusa, and H. Onozeki, "Electrical Transmission Properties of HBM Interface on 2.1-D System in Package using Organic Interposer", *IEEE/ECTC Proceedings*, May 2017, pp. 1943–1949.
39. Chen, W., C. Lee, M. Chung, C. Wang, S. Huang, Y. Liao, H. Kuo, C. Wang, and D. Tarng, "Development of novel fine line 2.1 D package with organic interposer using advanced substrate-based process", *IEEE/ECTC Proceedings*, May 2018, pp. 601–606.
40. Huang, C., Y. Xu, Y. Lu, K. Yu, W. Tsai, C. Lin, C. Chung, "Analysis of Warpage and Stress Behavior in a Fine Pitch Multi-Chip Interconnection with Ultrafine-Line Organic Substrate (2.1D)", *IEEE/ECTC Proceedings*, May 2018, pp. 631–637.
41. Islam, N., S. Yoon, K. Tan, and T. Chen, "High Density Ultra-Thin Organic Substrate for Advanced Flip Chip Packages", *IEEE/ECTC Proceedings*, May 2019, pp. 325–329.
42. Chiu, C., Z. Qian, and M. Manusharow, "Bridge interconnect with air gap in package assembly," *US Patent No. 8,872,349*, 2014.
43. Mahajan, R., R. Sankman, N. Patel, D. Kim, K. Aygun, Z. Qian, et al., "Embedded multi-die interconnect bridge (EMIB) – a high-density, high-bandwidth packaging interconnect," *IEEE/ECTC Proceedings*, May 2016, pp. 557–565.
44. Hsiung, C., and a. Sundarrajan, "Methods and Apparatus for Wafer-Level Die Bridge", US 10,651,126 B2, Filed on December 8, 2017, Granted on May 12, 2020.
45. Li, L., P. Chia, P. Ton, M. Nagar, S. Patil, J. Xue, J. DeLaCruz, M. Voicu, J. Hellings, B. Isaacson, M. Coor, and R. Havens, "3D SiP with Organic Interposer for ASIC and Memory Integration", *IEEE/ECTC Proceedings*, May 2016, pp. 1445–1450.

46. Pendse, R., "Semiconductor Device and Method of Forming Extended Semiconductor Device with Fan-Out Interconnect Structure to Reduce Complexity of Substrate", *US 9,484,319 B2*, Filed: December 23, 2011, Granted: November 1, 2016.
47. Yoon, S., P. Tang, R. Emigh, Y. Lin, P. Marimuthu, and R. Pendse, "Fanout Flipchip eWLB (Embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions", *IEEE/ECTC Proceedings*, 2013, pp. 1855–1860.
48. Chen, N., "Flip-Chip Package with Fan-Out WLCSP", *US 7,838,975 B2*, Filed: February 12, 2009, Granted: November 23, 2010.
49. Chen, N. C., T. Hsieh, J. Jinn, P. Chang, F. Huang, J. Xiao, A. Chou, B. Lin, "A Novel System in Package with Fan-out WLP for high speed SERDES application", *IEEE/ECTC Proceedings*, May 2016, pp. 1496–1501.
50. Lin, Y., W. Lai, C. Kao, J. Lou, P. Yang, C. Wang, and C. Hsieh, "Wafer warpage experiments and simulation for fan-out chip on substrate," *IEEE/ECTC Proceedings*, May 2016, pp. 13–18.
51. Yu, D., "Advanced system integration technology trends," *SiP Global Summit*, SEMICON Taiwan, Sept. 6, 2018.
52. Kwon, W., S. Ramalingam, X. Wu, L. Madden, C. Huang, H. Chang, et al., "Cost-effective and high-performance 28 nm FPGA with new disruptive silicon-less interconnect technology (SLIT)," *Proc. of Inter. Symp. on Micro.*, October 2014, pp. 599–605.
53. Liang, F., H. Chang, W. Tseng, J. Lai, S. Cheng, M. Ma, et al., "Development of non-TSV interposer (NTI) for high electrical performance package," *IEEE/ECTC Proceedings*, May 2016, pp. 31–36.
54. Suk, K., S. Lee, J. Kim, S. Lee, H. Kim, S. Lee, P. Kim, D. Kim, D. Oh, and J. Byun, "Low Cost Si-less RDL Interposer Package for High Performance Computing Applications", *IEEE/ECTC Proceedings*, May 2018, pp. 64–69.
55. You, S., S. Jeon, D. Oh, K. Kim, J. Kim, S. Cha, G. Kim, "Advanced Fan-Out Package SI/PI/Thermal Performance Analysis of Novel RDL Packages", *IEEE/ECTC Proceedings*, May 2018, pp. 1295–1301.
56. Chang, K., C. Huang, H. Kuo, M. Jhong, T. Hsieh, M. Hung, C. Wang, "Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity", *IEEE/ECTC Proceedings*, May 2019, pp. 41–46.
57. Lai, W., P. Yang, I. Hu, T. Liao, K. Chen, D. Tarn, and C. Hung, "A Comparative Study of 2.5D and Fan-out Chip on Substrate: Chip First and Chip Last", *IEEE/ECTC Proceedings*, May 2020, pp. 354–360.
58. Fang, J., M. Huang, H. Tu, W. Lu, P. Yang, "A Production-worthy Fan-Out Solution – ASE FOCoS Chip Last", *IEEE/ECTC Proceedings*, May 2020, pp. 290–295.
59. Lin, Y., M. Yew, M. Liu, S. Chen, T. Lai, P. Kavle, C. Lin, T. Fang, C. Chen, C. Yu, K. Lee, C. Hsu, P. Lin, F. Hsu, and S. Jeng, "Multilayer RDL Interposer for Heterogeneous Device and Module Integration", *IEEE/ECTC Proceedings*, May 2019, pp. 931–936.
60. Miki, S., H. Taneda, N. Kobayashi, K. Oi, K. Nagai, T. Koyama, "Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder", *IEEE/ECTC Proceedings*, May 2019, pp. 1599–1604.
61. Murayama, K., S. Miki, H. Sugahara, and K. Oi, "Electro-migration evaluation between organic interposer and build-up substrate on 2.3D organic package", *IEEE/ECTC Proceedings*, May 2020, pp. 716–722.
62. Lau, J. H., G. Chen, R. Chou, C. Yang, and T. Tseng, "Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2021.

# Chapter 6

## 2.5D IC Integration



### 6.1 Introduction

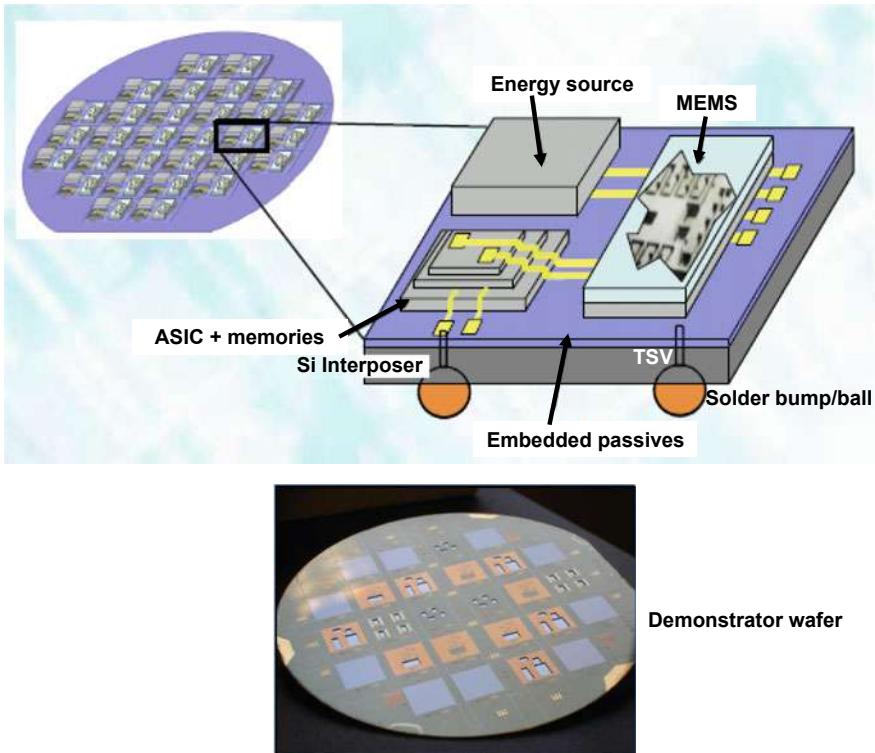
The 2.5D IC integration defined by the electronic semiconductor industry as chips are supported by a passive TSV (through-silicon via) interposer, which is then attached to a package substrate [1–111]. Unlike the active TSV-interposer (will be discussed in Chap. 7) which is with CMOS (complementary metal oxide semiconductor) device, the passive TSV-interposer is just a piece of dummy silicon with TSVs and RDLs (redistribution-layers). Today, 2.5D IC integration is in HVM (high volume manufacturing) by foundries such as TSMC (e.g., for Xilinx and NVidia) and UMC (e.g., for AMD) and will be discussed in this chapter. The recent developments of 2.5D IC integration will also be briefly presented. The origin of 2.5D IC integration will be briefly mentioned first.

### 6.2 Leti's SoW (the Origin of 2.5D IC Integration)

One of the early applications of 2.5D IC integration is system-on-wafer (SoW) given by Leti [1, 2] as shown in Fig. 6.1. It can be seen that a system of chips such as application specific IC (ASIC) and memories, PMIC (power management IC) and MEMS (micro-electro-mechanical system) are on a silicon wafer with TSVs (through-silicon vias) and RDLs. After dicing, the individual unit becomes a system or subsystem and can be attached on an organic package substrate or stand alone.

### 6.3 IME's 2.5D IC Integration

During IEEE/ECTC2008, IME presented three papers on 2.5D IC integration [3–5]. They will be briefly mentioned in the following sections.

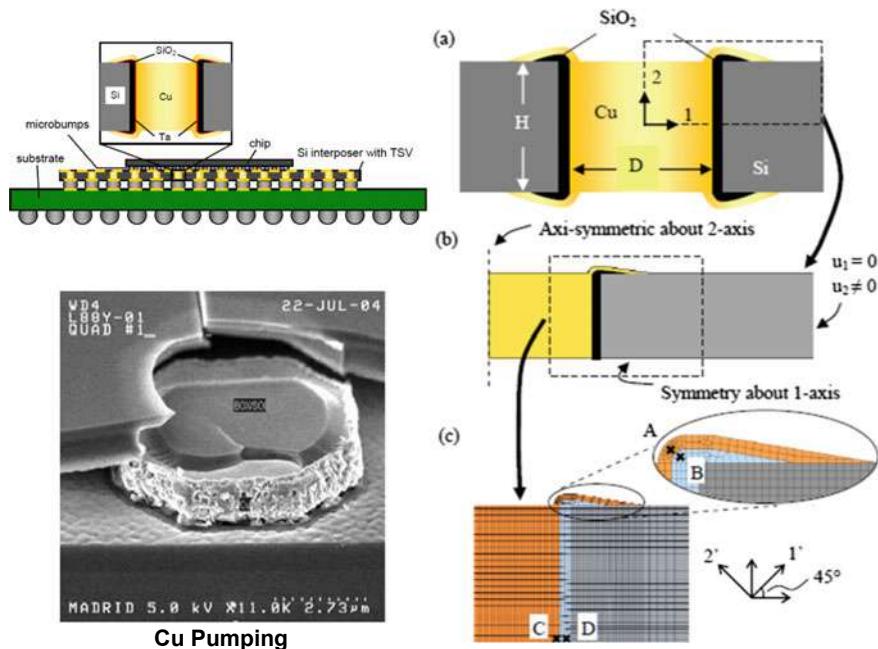


**Fig. 6.1** Leti's SoW (the origin of 2.5D IC integration) [1]

### 6.3.1 3D Nonlinear Local and Global Analysis of 2.5D IC Integration

Nonlinear simulation of the local and global thermal-mechanical responds of a 2.5D IC integration has been given in [3, 6]. Figure 6.2 shows the largest passive TSV-interposer developed in 2007 [3, 6] to support a very large chip ( $21\text{ mm} \times 21\text{ mm}$ ) with 11,000 I/Os. For local effects, simulation results show [3, 6] that due to the very large local thermal expansion coefficient (TEC) mismatch between the Si ( $2.5 \times 10^{-6}/^\circ\text{C}$ ) and the Cu ( $17.5 \times 10^{-6}/^\circ\text{C}$ ) in the vertical-direction, during heating, the TSV Cu tends to pump out from the surrounding Si as shown in Fig. 6.2. If the TSV Cu is partially covered by the  $\text{SiO}_2$ , during heating, the local thermal expansion mismatch Cu may (push out to) crack the  $\text{SiO}_2$  as shown in Fig. 6.2, which is called Cu pumping. In [3, 6], it shows that in general, above an aspect ratio (thickness/diameter) of 5, there is little dependence of stress and strain on the aspect ratio of the TSV.

The diagonal strain at Point A and B (Figure 6.2) are plotted in Figs. 6.3a, b for the filled via and Figs. 6.3c, d for the unfilled via. As shown in the figures for the filled via, there is a linear relationship between the diagonal strain and the diameter

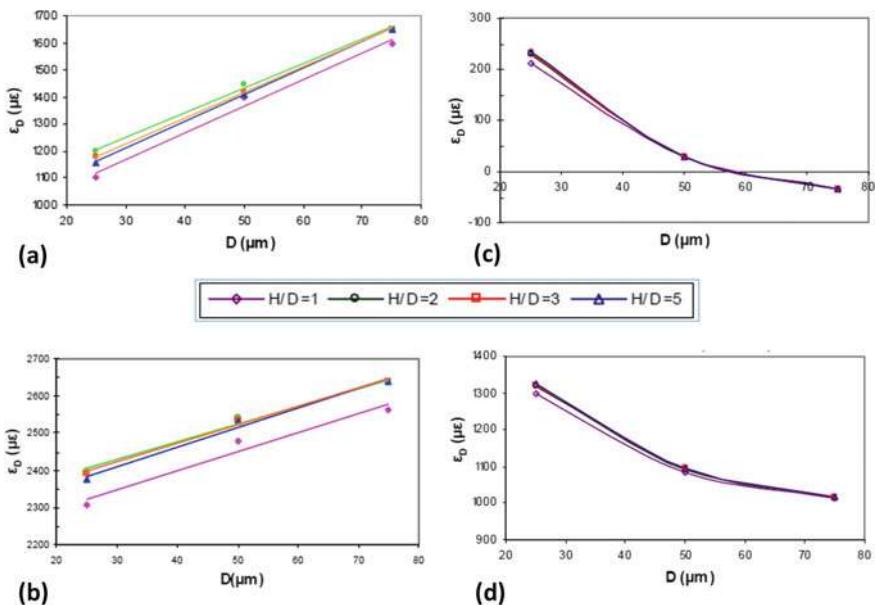


**Fig. 6.2** Package incorporating TSV interposer. **a** Diagram of simplified TSV. **b** Quarter model of TSV with applied boundary Conditions. **c** Mesh of critical region

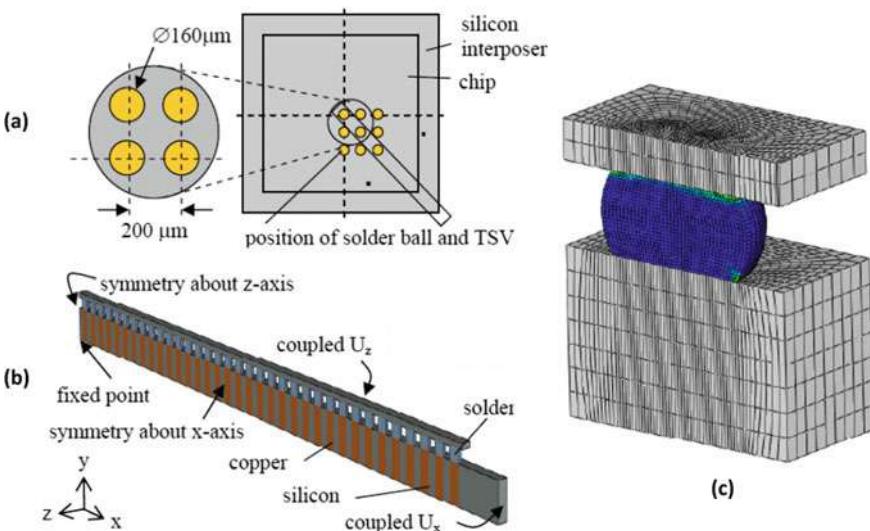
of the via. As expected, the strain in the copper is lower than that in the silicon oxide. In the unfilled via with the RDL, diagonal strains decrease with diameter. This is because the ratio of  $t$  (silicon oxide)/ $D$  is smaller resulting in relatively less expansion in copper.

The effective TEC of the silicon interposer is higher when it contains copper in the form of filled TSVs. As a result, on temperature cycling, the interposer will expand and contract more than the chip, resulting in a fatigue loading on the solder joint. The effect of this global mismatch on the reliability of the solder bump is investigated in the following simulations. The global model consisting of a chip assembled onto a silicon interposer containing TSVs is made to undergo three cycles of temperature cycling between -40 and 125 °C. A diagonal slice of this model is considered for computational efficiency. A schematic diagram of the model, the applied boundary conditions and the mesh of the critical region are shown in Fig. 6.4. Results of the analysis indicate that as the height of the interposer ( $H$ ) increases, the creep strain energy density in the solder increase as shown in Fig. 6.5a. For interposer heights of 50–200, the maximum strain energy density occurs at the top of the solder joint.

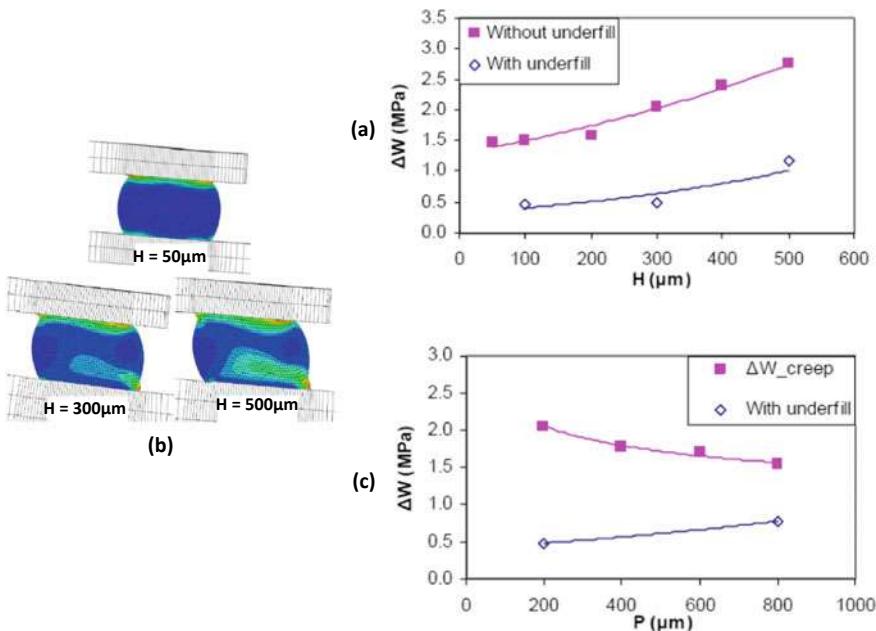
On the other hand, for interposer heights of 300–500, the maximum strain energy occurs at the bottom surface of the solder joint. Maximum strain energy position is transferred to the bottom when the expansion of the interposer begins to exert a shearing load on the solder. This effect can be seen in Fig. 6.5b where the solder



**Fig. 6.3** Diagonal strain ( $\epsilon_D$ ) at critical location for **a** copper (Point A) and **b** silicon oxide (Point B) in filled vias with RDL. Diagonal strain ( $\epsilon_D$ ) at critical location for **c** copper (Point A) and **d** silicon oxide (Point B) in unfilled vias with RDL



**Fig. 6.4** **a** Diagram of global model. **b** Diagonal slice model with applied boundary conditions. **c** Mesh of critical region

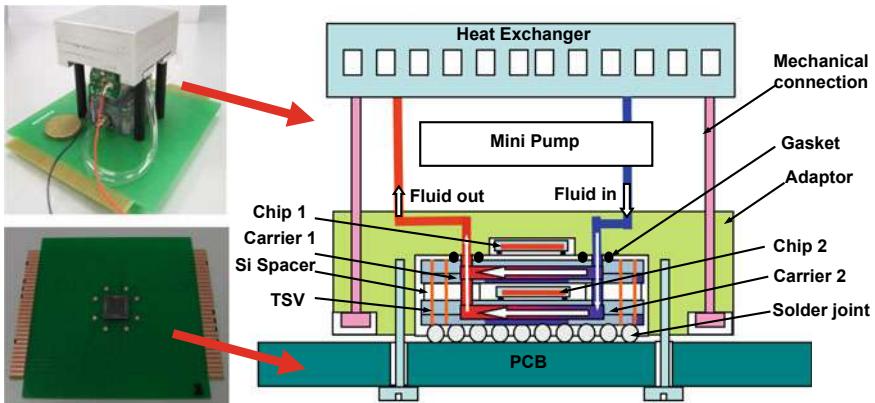


**Fig. 6.5** **a** Creep Strain energy density per cycle variation with interposer height ( $H$ ). **b** Creep strain energy densities for three interposer heights. **c** Creep Strain energy density per cycle variation with via pitch ( $P$ )

joint on the shortest interposer has much reduced strain energy density at its bottom surface. The use of underfill reduces the inelastic strain energy density by 4 times. Increasing the pitch ( $P$ ) results in a decreasing of the creep strain energy density as shown in Fig. 6.5c. This is a result of the decreased copper content and hence decreased mismatch between the silicon chip and the silicon interposer with TSVs.

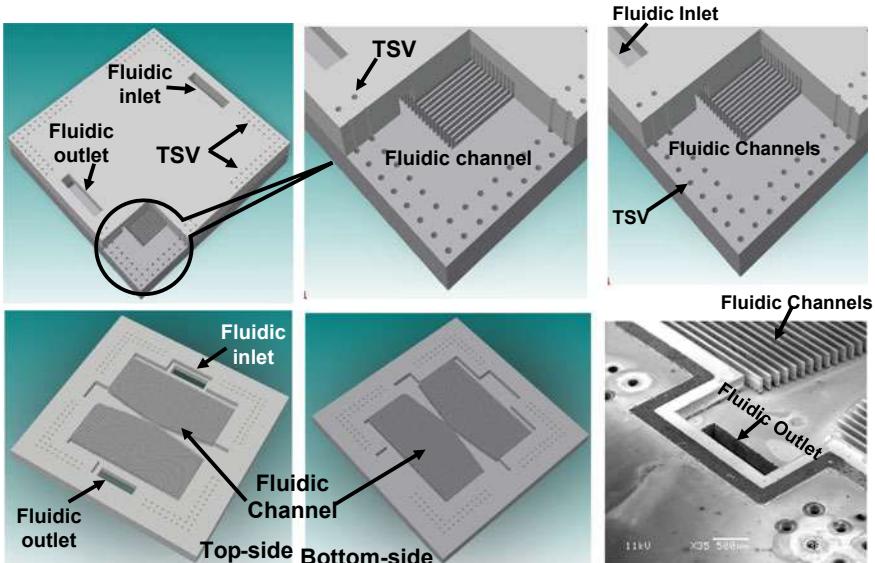
### 6.3.2 2.5D IC Integration for Electrical and Fluidic Interconnects

Figure 6.6 shows two identical TSV-interposers (carriers) with microchannels for thermal management and TSVs for electrical feed-through [4, 7–10]. The size of the whole system is about 1/4 of a fist. Each TSV-interposer is supporting a chip ( $10\text{ mm} \times 10\text{ mm}$ ) with  $100\text{ W}$  of (heat) power dissipation. This TSV-interposer is fabricated by wafer-on-wafer (WoW) bonding two silicon wafers together, and an optimized liquid cooling channel structure, fabricated by DRIE (deep reactive ion etching), is embedded in between the interposer. A mini pump is used to pump the cold water from the heat exchanger to the inlet of the interposer, through the microchannels, come out from the outlet of the interposer, and then back to the heat exchanger as



**Fig. 6.6** Integrated liquid cooling system by stacked TSV-interposers

shown in Figs. 6.6 and 6.7. Silicon is chosen as interposer material because it is a suitable material for the integration of both electrical (TSV) and fluidic structure (microchannel) in the same substrate with DRIE. The difference between these two interposers is that the bottom Si interposer does not have any outlets. TSVs can be designed along the periphery of the interposer. After WoW bonding, electrical interconnection through the carrier is made by the TSV with on-wall metallization (in this case, the copper filling may not be necessary).



**Fig. 6.7** Top-view and cross-sectional view of the TSV-interposer with fluidic channels

**Fig. 6.8** Pressure-drop measurements versus flow rate

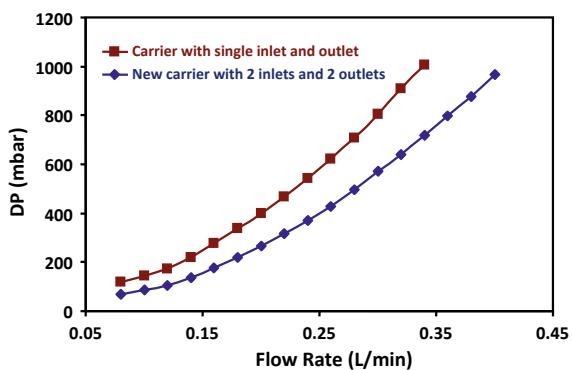
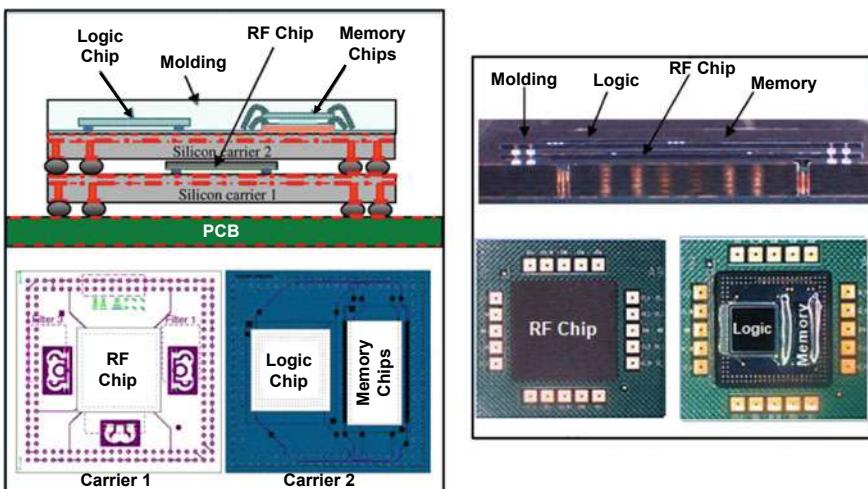


Figure 6.8 shows the pressure-drop measurements. It can be seen that the carrier with two inlets and two outlets performs better thermally than the carrier with one inlet and one outlet. More technical details can be found in [4, 7–10].

### 6.3.3 Double Stacked Passive TSV-Interposers

Figure 6.9 shows a module consists of two stacks assembled one over the other with 3 different kinds of chips [5, 11]. The module size is 12 mm × 12 mm and 1.3 mm-thick. The top TSV-interposer (carrier 2) is 12 mm × 12 mm × 0.2 mm with 168 peripherally populated vias. The bottom carrier (Carrier 1) is assembled

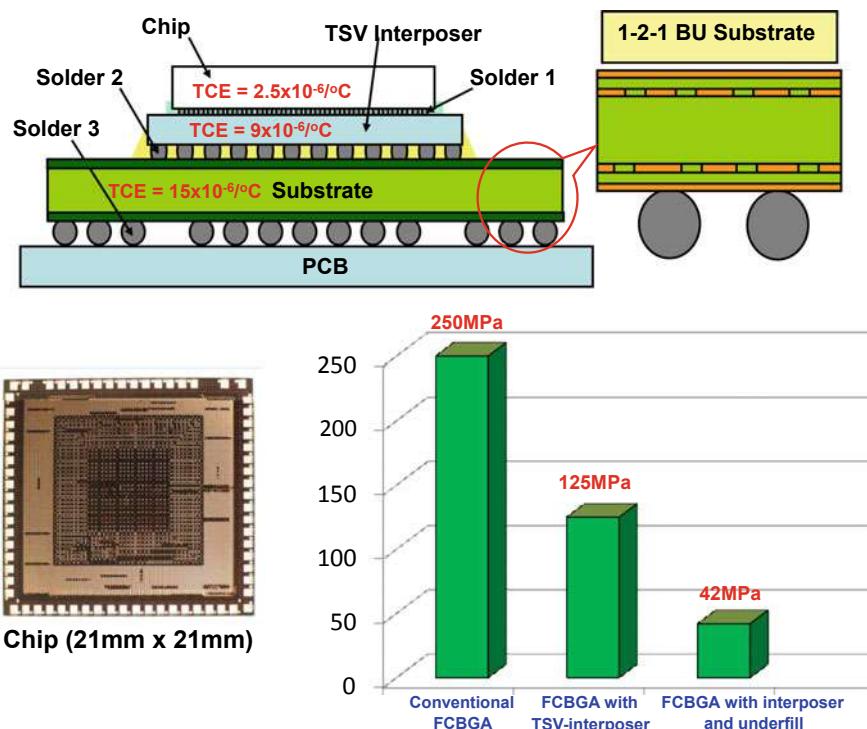


**Fig. 6.9** Two stacked TSV-interposers with 3 different kinds of chips

with a  $5\text{ mm} \times 5\text{ mm}$  RF flip chip. The top carrier (Carrier 2) is assembled with a  $5\text{ mm} \times 5\text{ mm}$  logic chip and two stacked  $3\text{ mm} \times 6\text{ mm}$  wire bonded chips. Carrier 2 is over molded (using the transfer molding process) to protect the wire-bond chips. The TSV-interposers have been fabricated with two metal layers with  $\text{SiO}_2$  as dielectric/passivation layer. Electrical connections through the carriers are formed by TSVs. Carrier 1 is mounted on a FR4 PCB using SAC305 solder ball of  $250\text{ }\mu\text{m}$  diameter. Carrier 1 assembly is underfilled (cured at  $165\text{ }^{\circ}\text{C}$  for 3 h). More technical information is given in [5, 11].

### 6.3.4 TSV-Interposer Used as Stress (Reliability) Buffer

During ECTC2009, IME presented a paper on using TSV-interposer as a stress buffer [12, 13]. Figure 6.10 shows a large chip ( $21\text{ mm} \times 21\text{ mm}$ ) which is attached on top of a Cu-filled TSV interposer and then the interposer is attached on an organic package substrate. It has been shown in [12, 13] that the Cu-filled TSV interposer acts like a stress relief (reliability) buffer and reduces the stress (from 250 to 125 MPa) acting

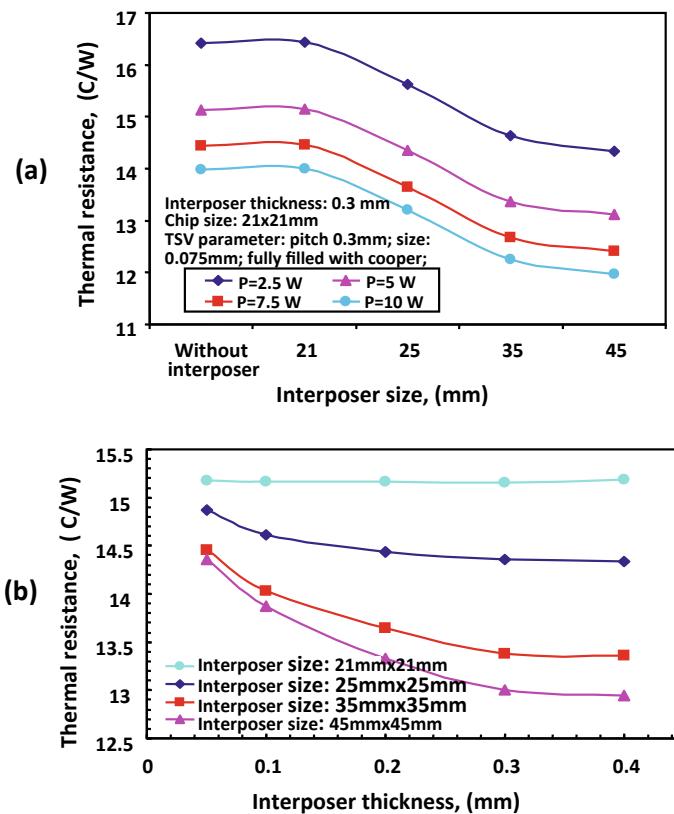


**Fig. 6.10** TSV-interposer used as stress relief buffer

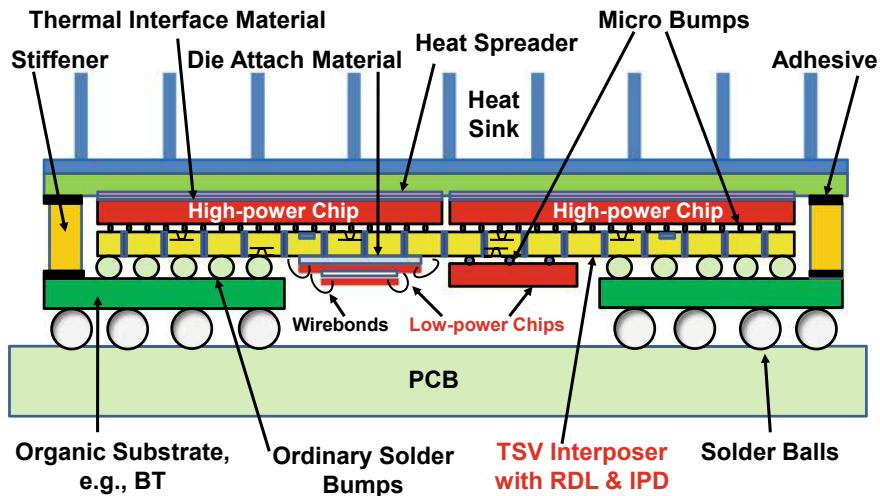
at the Cu-low-k pads of the large chip. This is more important for smaller feature size devices because the allowable stress on their Cu-low-k pads is smaller. If a special (with a very small filler size) underfill is added between the chip and the interposer, the stress acting at the Cu-low-k pads of the chip is further reduced to 42 MPa as shown in Fig. 6.10.

Figure 6.11a shows the effect of the TSV-interposer size on the package thermal performance. It can be seen that the thermal resistance ( $R_{ja}$ ) decreases about 14% when the TSV interposer size increases from  $21 \times 21$  mm to  $45 \times 45$  mm. This indicates that package thermal performance can be improved by increasing the TSV-interposer size.

Figure 6.11b shows the effect of the TSV-interposer thickness on the package thermal performance. It can be seen that the thicker the TSV-interposer the lower the thermal resistance. This is because of the increasing spreading effect with thicker interposer. However, for small size interposers, this effect is negligible.



**Fig. 6.11** Effects of interposer size **a** and interposer thickness **b** on thermal performance



**Special underfill between the TSV interposer and the high- and low-power flip chips.**  
**Ordinary underfill between the TSV interposer and the organic substrate.**  
**Encapsulant for wirebonding memory stack.**

**Fig. 6.12** TSV-interposer with chips on both sides

## 6.4 HKUST's TSV-Interposer with Chips on Both Sides

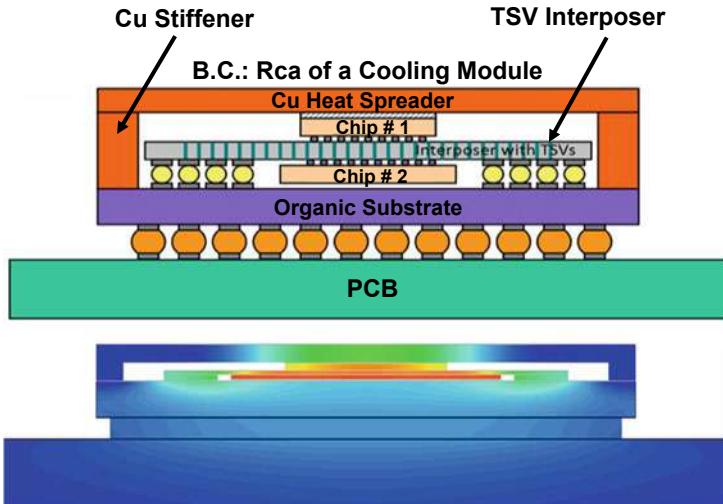
Figure 6.12 shows a new design, which allows chips on both sides of a passive TSV-interposer [14–16]. The high-power flip chips are attached on the topside of the TSV-interposer and the chips' backside is directly attached to a heat spreader or even a heat sink. The low-power chips are attached on the bottom side of the TSV-interposer. The cavity of the package substrate is optional.

## 6.5 ITRI's 2.5D IC Integration

Since 2011 ITRI has been published papers on 2.5D IC integration [17–41] and some will be briefly mention in this section.

### 6.5.1 *Thermal Management of TSV-Interposer with Chips on Both Sides*

Figure 6.13 shows a TSV-interposer with chips on its both sides. This is one of the degenerations of the new generic design shown in Fig. 6.12. The dimension of the



**Average Temperature. Chip #1: 109°C; Chip #2: 121°C**

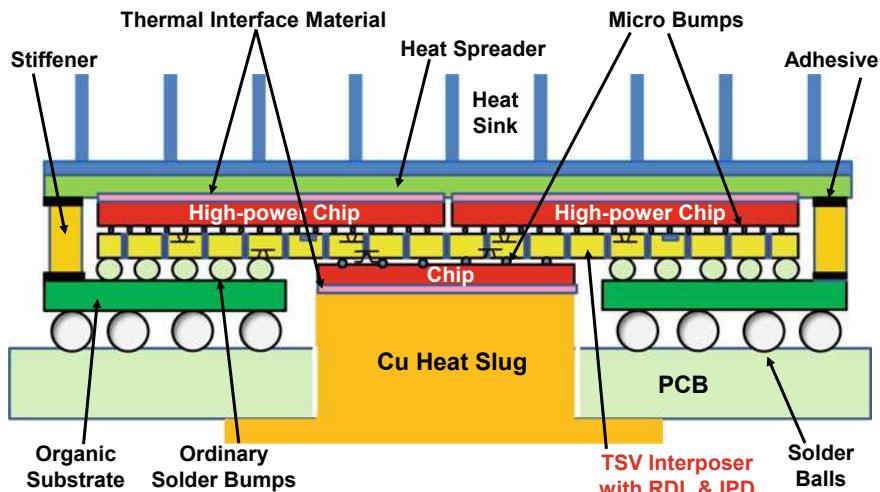
**Fig. 6.13** Thermal analysis of TSV-interposer with chips on both sides

structure, material properties, and thermal boundary condition are shown in [17–21]. The dimensions of the chips are 20 mm × 20 mm for Chip #2 and 12 mm × 12 mm for Chip #1. The dimensions of the TSV-interposer are 30 mm × 30 mm × 100  $\mu\text{m}$ . There is a heat spreader at the backside of Chip #1.

The ambient temperature is assumed to be 20 °C. The boundary condition on the top-side and bottom-side of the PCB is  $h$  (heat-transfer coefficient) = 10 W/m<sup>2</sup> K, which is to imitate a natural convection condition. For the heat spreader, we use the thermal resistance,  $R_{ca}$ , in place of cooling module for simplifying the simulations. The  $R_{ca}$  is assumed to be 0.3 °C/W to imitate the heat spreader cooled by a pretty good heat sink with fan or a liquid cooling module. The power generation of chip #1 is 75 W and that of chip #2 is 15 W. The total power consumption of the SiP is 90 W. Icepak is the simulation tool to solve the heat conduction problems using finite volume method.

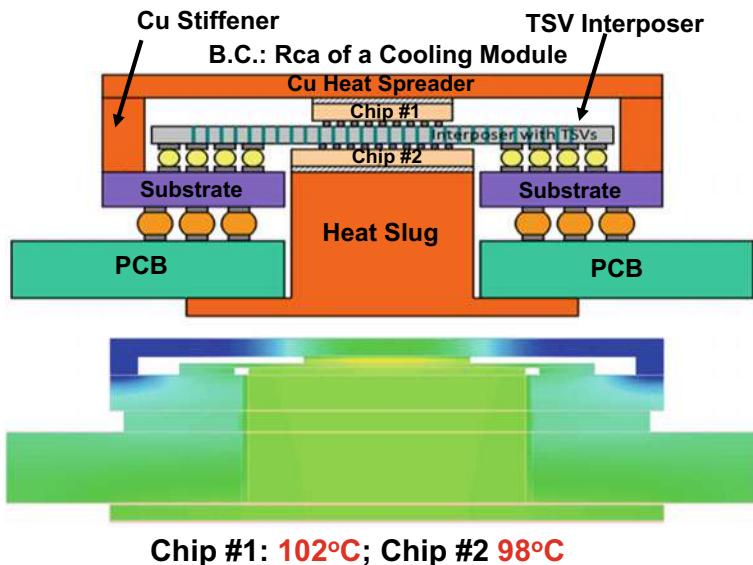
The SiP is under the boundary conditions of  $R_{ca} = 0.3$  °C/W for heat spreader topside and  $h = 10$  W/m K for PCB both sides. Figure 6.13 shows the cross section temperature distribution of the analyzed SiP. The average temperatures of Chip #1 and Chip #2 are 109 °C and 121 °C respectively under ambient temperature 20 °C as shown in Fig. 6.13. It is noted that even the chip #2 has a lower heat generation; however its temperature is still higher than that of the chip #1. This is because Chip #1 has a heat spreader at its back to conduct the heat out. Thus, a way to lower the temperature in Chip #2 is necessary.

Figure 6.14 shows the bottom chip of Fig. 6.12 which is attached to a Cu heat slug with TIM and Fig. 6.15 shows the boundary condition for analysis. All the



**Special underfill between the TSV interposer and the high- and low-power flip chips.  
Ordinary underfill between the TSV interposer and the organic substrate.**

**Fig. 6.14** TSV-interposer with chips on both sides and a Cu heat slug attached to the backside of the bottom chip



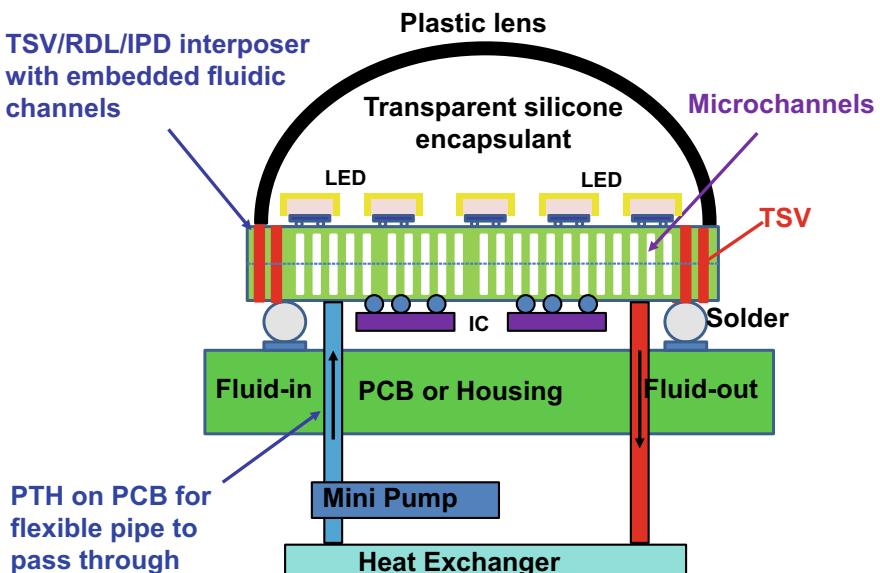
**Fig. 6.15** Thermal analysis of TSV-interposer with chips on both sides and a Cu heat slug attached to the backside of the bottom chip

dimensions of the chips and interposer, and the boundary conditions are the same with Fig. 6.13 except there is a cavity of the PCB [17–21].

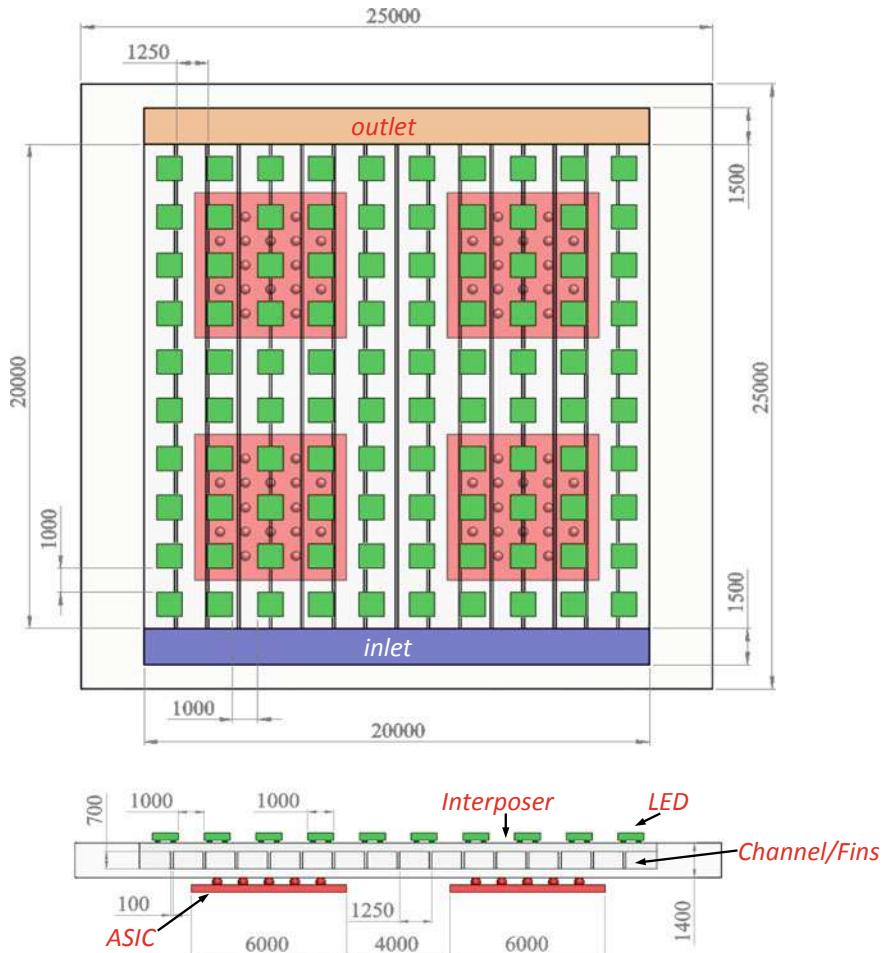
Figure 6.15 shows the simulation results. It can be seen that Chip #2 temperature is reduced from original 121 to 98.0 °C. Also, the temperature of Chip #1 reduces from original 109 to 102 °C. This result shows that the chip at the bottom of an interposer can be cooled down effectively by using such a simple heat slug structure as shown in Figs. 6.14 and 6.15.

### 6.5.2 TSV-Interposer with Embedded Fluidic Microchannels for LEDs

Figure 6.16 shows an application of a TSV-interposer with embedded microchannels (as shown in Fig. 6.7) for LED thermal management [22]. It consists (Fig. 6.17) of 100 identical LEDs uniformly distributed on the top-side of the TSV-interposer and 4 identical logics (e.g., ASIC) uniformly distributed at its bottom-side. The dimensions of the LEDs are 1 mm × 1 mm × 300 μm, the IC chips are 6 mm × 6 mm × 300 μm, and of the TSV-interposer are 25 mm × 25 mm × 1.4 mm. The microchannel height is 700 μm, the fin width is 0.1 mm and on a 1.25 mm pitch. The fluidic inlet/outlet openings are 20 mm × 1.5 mm. The material properties and boundary conditions are shown in [22].

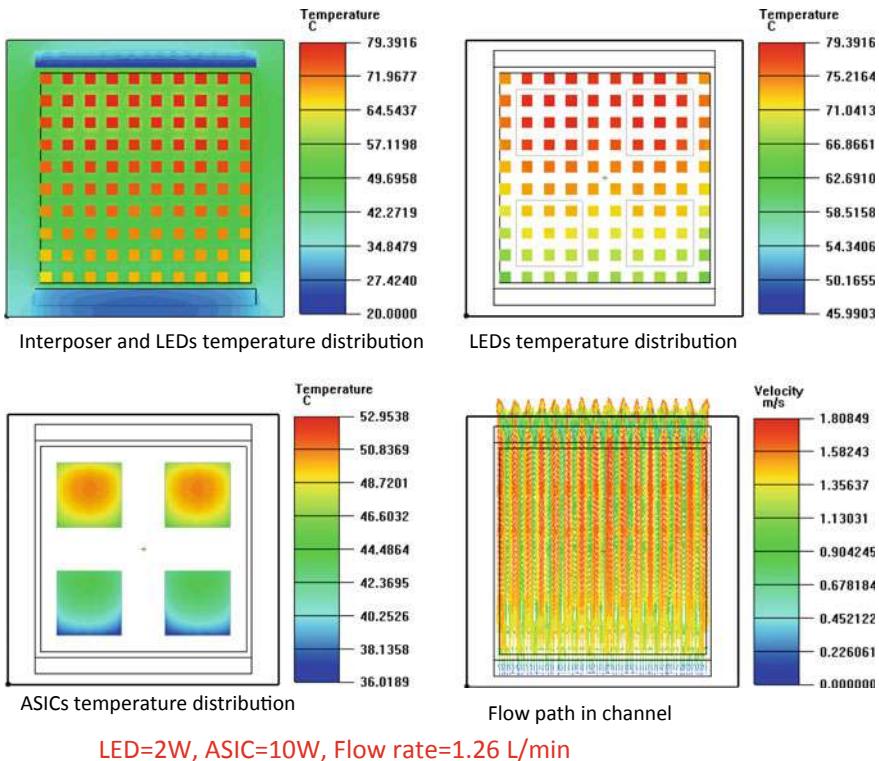


**Fig. 6.16** TSV-interposer with microchannels for LED thermal management



**Fig. 6.17** Structural dimensions of the LEDs and ASICs for analysis

Figure 6.18 shows the simulation results: (1) the temperature of the LEDs and chips near the inlet is the smallest and near the outlet is the largest (the water carriers the heat out); (2) the temperature of the LEDs and chips near the interposer center is larger than that near both sides (parallel to the fluid direction) of the interposer; and (3) the temperature in the LEDs is in general larger than that in the ASIC. It can be shown that [22] that: (1) the larger the LED power the higher the LED temperature; (2) the larger the ASIC power the higher the ASIC temperature; (3) the larger the SiP chips power the higher the LED, ASIC, and water outlet temperature; and (4) the rate of change of average temperature of LEDs is larger than that of ASIC and water outlet.

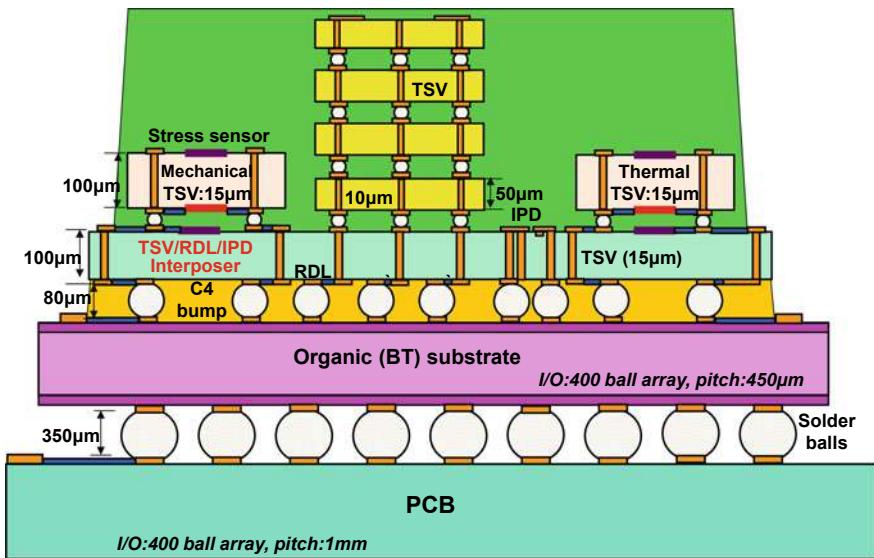


**Fig. 6.18** Simulation results for LED = 2 W, ASIC = 10 W, and flow rate = 1.26L/min

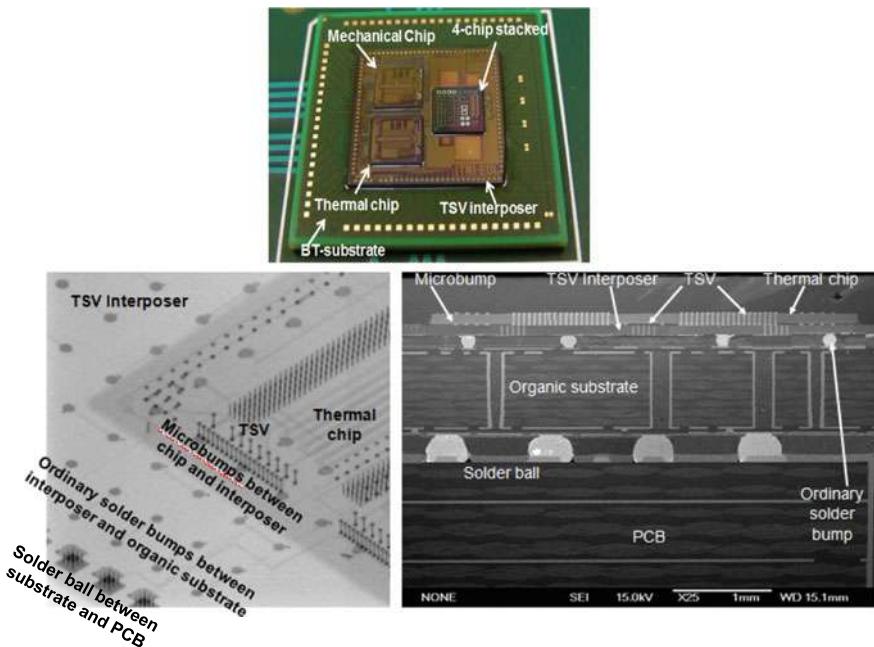
### 6.5.3 TSV-Interposer with SoCs and Memory Cube

Figure 6.19 shows a cross section of ITRI's 3D 2.5D IC integration test vehicle [23–26], which consists of an interposer supporting four memory chips, one thermal chip, and one mechanical chip. It is over molded for pick-and-place purpose as well as protecting the chips from harsh environments. There are RDLs on both top and bottom sides of the interposer. Also, stress sensors are implanted on the top side and IPDs (integrated passive devices) are fabricated through the thickness (100  $\mu\text{m}$ ) of the interposer (12.3 mm  $\times$  12.2 mm). Figure 6.20 shows the sample and the SEM image of a cross section and the x-ray image of the test vehicle [23–26].

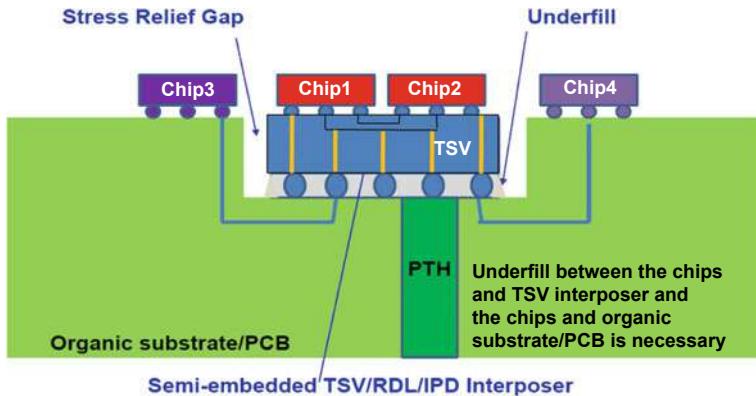
This test vehicle can be degenerated to the case of: (a) wide I/O memory if there is neither the memory-chip stacking nor the TSVs in the mechanical/thermal chips and the interposer is either an logic, microprocessor, or SoC; (b) wide I/O DRAM if there are not mechanical and thermal chips and the interposer is a logic chip; and (c) wide I/O interface if there is not the memory-chip stacking and there is not any TSV in the thermal/mechanical chips.



**Fig. 6.19** TSV-interposer supporting a memory cube and two SoCs



**Fig. 6.20** The assembled test vehicle. SEM image of a typical cross section and x-ray image of the structure



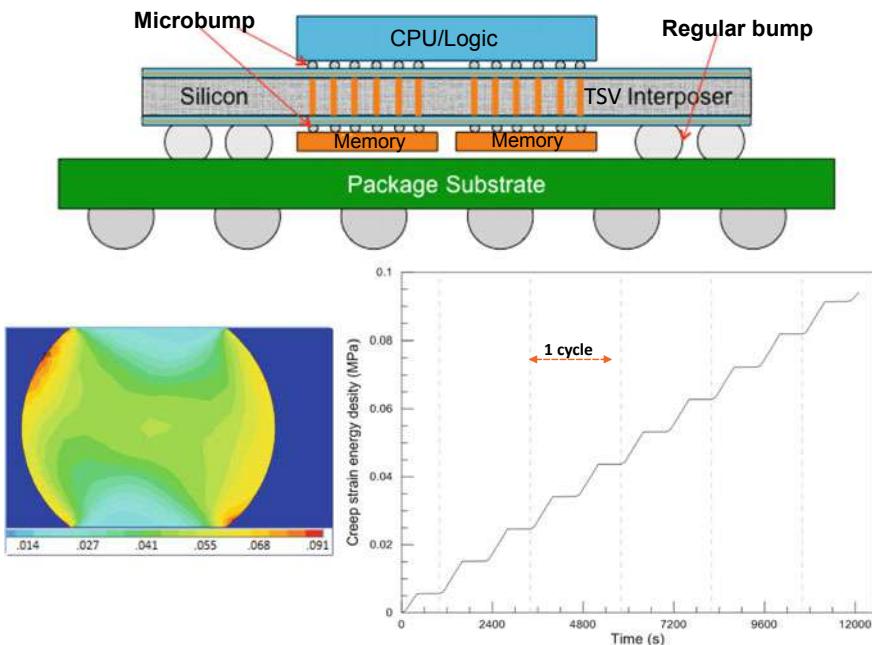
**Fig. 6.21** A TSV-interposer semi-embedded in an organic substrate with stress relief gap

#### 6.5.4 *Semi-embedded TSV-Interposer*

Figure 6.21 shows a semi-embedded TSV-interposer (with a stress relief gap) supporting multiple chips on its top surface. The advantages of this design are: (1) low profile; (2) free to use of any chips without TSVs; (3) short design cycle; (4) low manufacturing cost; (5) RDLs allow chips to talk to each other at short distance; (6) lots TSVs can be used for powers, grounds, and some signals; (7) reworkable (test the chip-interposer module on substrate/PCB before underfilling); (8) the heat can get out from chips' backside through a heat spreader/sink and/or a heat slug with a spreader (not shown) conducting the heat from the solder bumps to the bottom-side of the substrate/PCB; (9) reliable (because the stress relief gap reduces the global thermal expansion mismatch between the embedded interposer ( $6 - 8 \times 10^{-6}/^{\circ}\text{C}$ ) and the organic substrate/PCB ( $15 - 18.5 \times 10^{-6}/^{\circ}\text{C}$ )); and (10) potentially low system cost. For more details, please read [30].

#### 6.5.5 *TSV-Interposer with Double-Sided Chip Attachments*

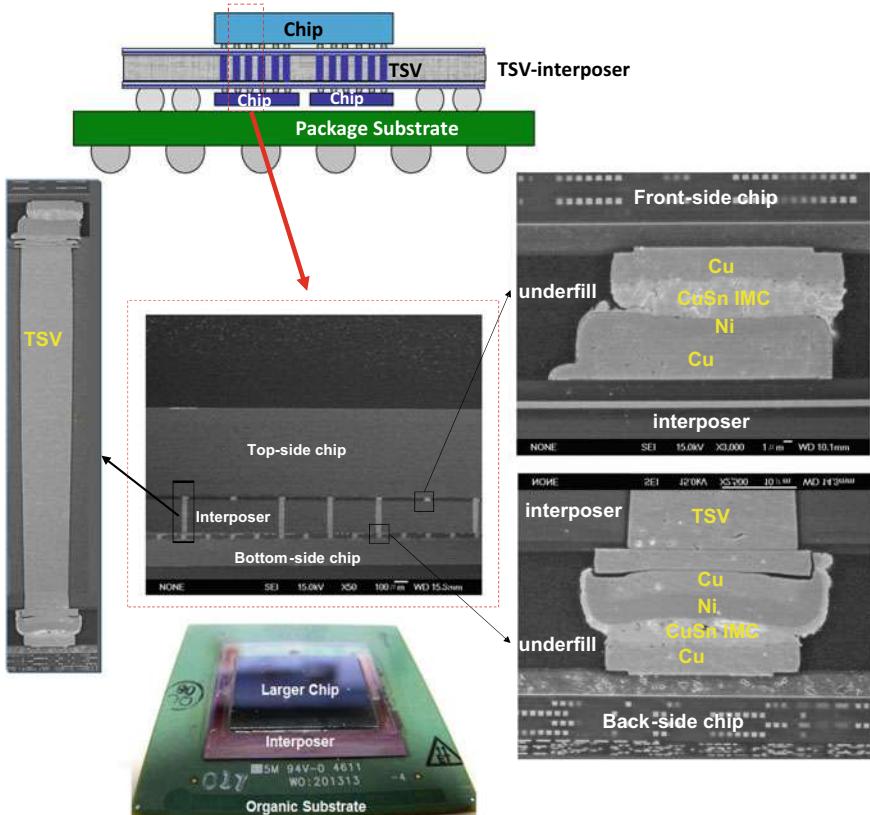
Figure 6.22 shows a TSV-interposer with chips on both sides [32, 33]. It can be seen that the interposer that supported one CPU chip on its top-side and two memory chips on its bottom-side. The interposer is  $28\text{ mm} \times 28\text{ mm} \times 150\text{ }\mu\text{m}$ , the CPU/ASIC is  $22\text{ mm} \times 18\text{ mm} \times 400\text{ }\mu\text{m}$ , and the DRAM is  $10\text{ mm} \times 10\text{ mm} \times 100\text{ }\mu\text{m}$ . The package substrate is  $40\text{ mm} \times 40\text{ mm} \times 950\text{ }\mu\text{m}$  and the PCB is  $114.3\text{ mm} \times 101.6\text{ mm} \times 1600\text{ }\mu\text{m}$ . The diameter of micro solder bumps between all the chips and the interposer is  $25\text{ }\mu\text{m}$  and on  $250\text{ }\mu\text{m}$  pitch. The diameter of the ordinary solder bumps is  $150\text{ }\mu\text{m}$  and on  $250\text{ }\mu\text{m}$  pitch. The diameter of the solder balls is  $600\text{ }\mu\text{m}$  and on  $1000\text{ }\mu\text{m}$  pitch.



**Fig. 6.22** TSV-interposer with chips on its both sides. Creep strain energy density time-history of the corner solder joint

The maximum creep strain energy density time-history acting at the corner ordinary solder joint between the interposer and the organic (BT) substrate subjected to temperature cycling ( $-40$  to  $125$  °C) is shown in Fig. 6.22, where the von Mises stress contours are also provided. It can be seen that that the creep strain energy density per cycle is  $0.018$  MPa which is much less than  $0.1$  MPa and thus it should be reliable for most of the environmental condition. Underfill helps!

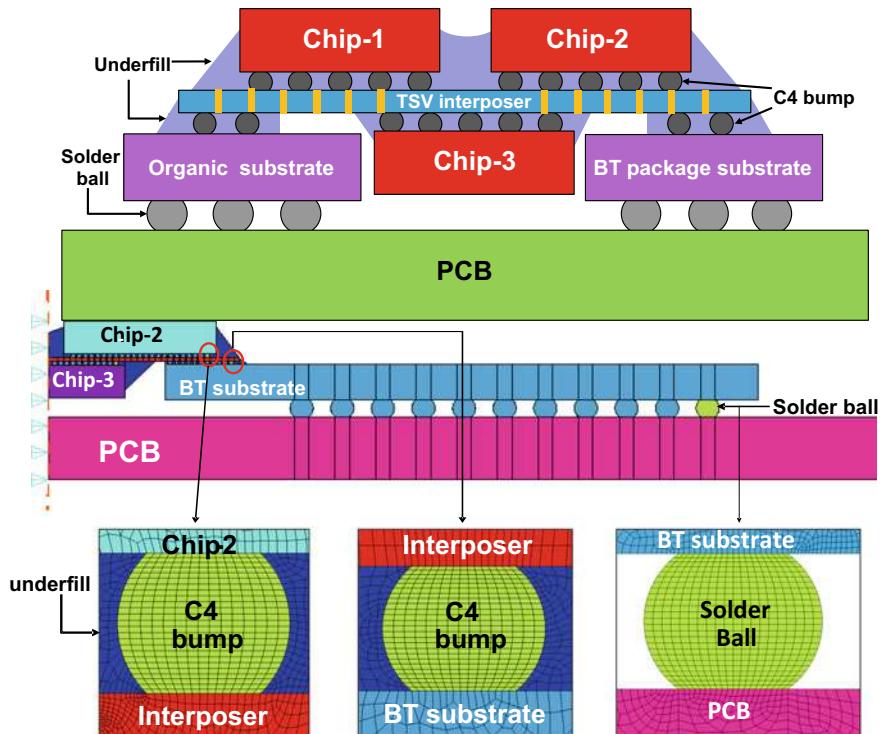
The SEM image of a cross section of the assembly is shown in Fig. 6.23. It can be seen that there is a larger and thicker chip on the top-side of the passive interposer and a smaller and thinner chip on its bottom-side. The micro solder joint between the top chip and the interposer is also enlarged and shown in Fig. 6.23. It can be seen that: (a) the UBM on the interposer is Cu and Ni; (b) the solder becomes the IMC (intermetallic compound),  $\text{Cu}_6\text{Sn}_5$ ; and (c) the Cu UBM from the larger chip. Similarly, the micro solder joint between the interposer with a TSV and the smaller chip is enlarged and shown in Fig. 6.23.



**Fig. 6.23** SEM images of the structure elements, e.g., TSV, microbumps, chips, and sample

### 6.5.6 TSV-Interposer with Chips on Both Sides

Figure 6.24 shows the schematics of a TSV-interposer with chips on its both sides [34–37]. It can be seen that: (a) on the top-side, there are two chips and (b) on the bottom-side, there is one chip. The size of the package substrate is 35 mm × 35 mm × 970  $\mu\text{m}$ . Underfills are used between the chips and interposer and the interposer and package substrate. The TSVs' diameter is 10  $\mu\text{m}$  and on 150  $\mu\text{m}$  pitch. The diameter of the solder bumps between the chips and interposer and between the interposer and package substrate is 90  $\mu\text{m}$  and on 125  $\mu\text{m}$  pitch. The diameter of the solder balls between the package substrate and the PCB is 600  $\mu\text{m}$  and on 1000  $\mu\text{m}$  pitch. Figure 6.24 also shows the finite element model for nonlinear analysis. Figure 6.25 shows the creep strain energy density history for the corner solder bumps between Chip-2 and the interposer. It can be seen that the creep strain energy density per cycle of the corner solder bumps between Chip-2 and the interposer is 0.0107 MPa. This magnitude is too small to create solder joint thermal-fatigue reliability problem under



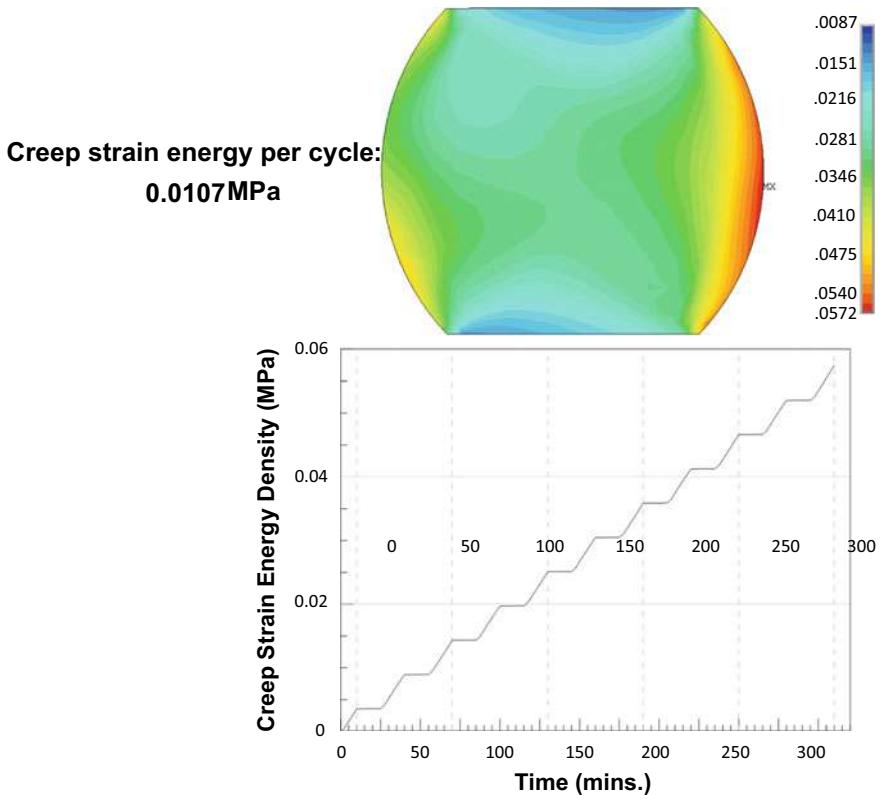
**Fig. 6.24** TSV-interposer with chips on its both sides. Finite element models for simulations

the environmental condition:  $-25 \rightarrow 125^{\circ}\text{C}$  on a 60-min cycle. Underfill helps! For the creep responses at other solder joint locations, please see [34–37].

Figure 6.26 shows the cross-sections of the fully assembly module. It can be seen that the interposer is properly supporting the 3 chips with underfill. This interposer is soldered (with underfill) to a 4-2-4 package substrate.

### 6.5.7 Through-Silicon Hole-Interposer (TSH-Interposer)

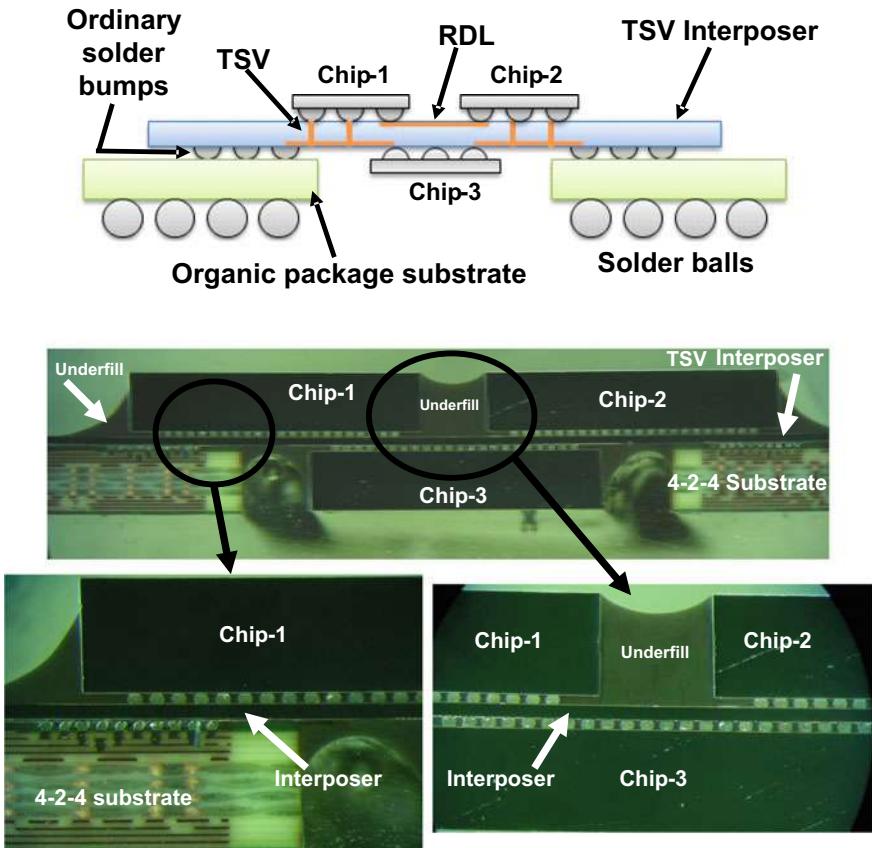
Figure 6.27 schematically shows a TSH-interposer supporting a few chips on its top- and bottom-side [38, 39]. The key feature of the TSH-interposer is there is not metallization and copper filling in the holes. Thus, dielectric layer, barrier and seed layers, via filling, CMP for removing overburden copper, and Cu revealing are not necessary. Comparing to the TSV-interposer, TSH-interposer only needs to make holes (by either laser or DRIE) on a piece of silicon wafer. Just like the TSV interposers, RDLs are needed by the TSH-interposer.



**Fig. 6.25** Creep strain energy density contours and time-history

The TSH interposers can be used to support the chips on its top side as well as bottom side. The holes can let the signals of the chips on the bottom-side transmit to the chip on the top-side (or vice versa) through the Cu pillars and solders. The chips on the same side can communicate to each other with the RDLs of the TSH-interposer. Physically, the top chips and bottom chips are connected through Cu pillars and micro solder joints. Also, the peripherals of all the chips are soldered to the TSH-interposer for structural integrity to resist shock and thermal conditions. In addition, the peripherals of the bottom-side of the TSH-interposer have ordinary solder bumps which are attached to a package substrate.

The test vehicle is shown in Fig. 6.28. It can be seen that it consists a TSH-interposer, which is supporting a top-chip with Cu pillars and a bottom-chip with UBM and solder. The interposer module is connected to a package substrate and then attached to a PCB. The final assembled test vehicle is shown in Fig. 6.29. It can be seen that the PCB is supporting the package substrate, which is supporting the TSH-interposer, which is supporting the top-chip. The bottom-chip is blocked by the TSH-interposer and cannot be seen.

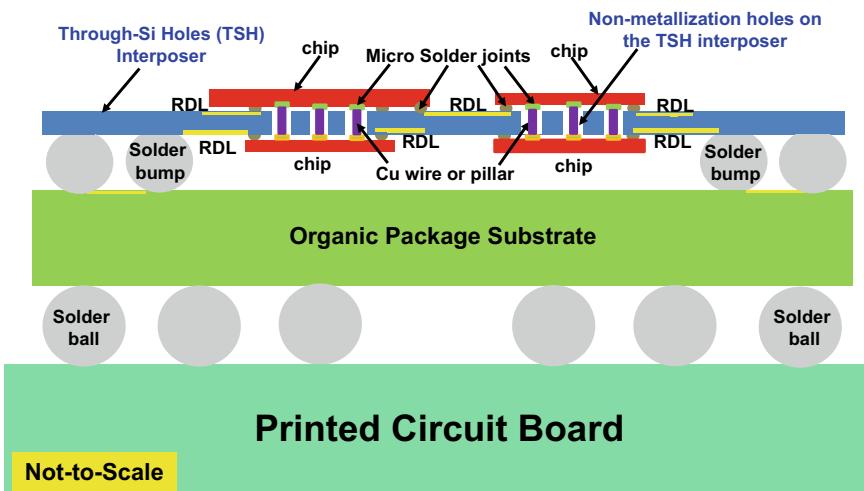


**Fig. 6.26** Cross section images of the assembled structure

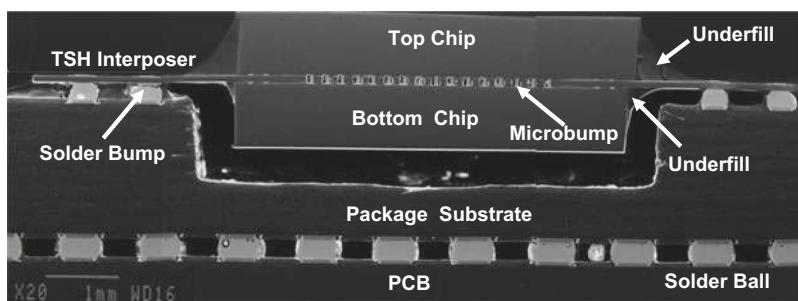
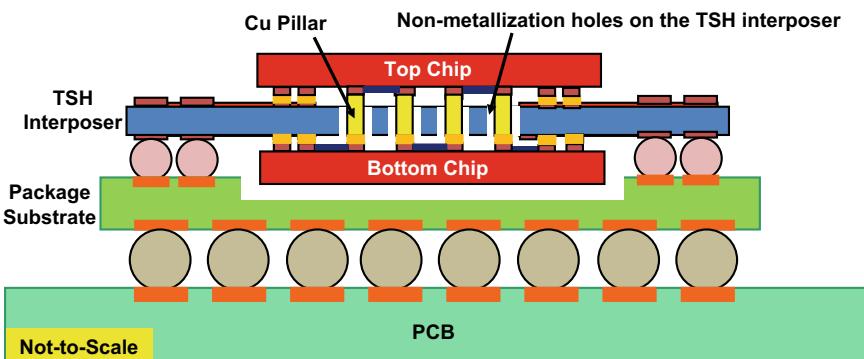
Figure 6.29 also shows the x-ray images of the final assembly. It can be seen that: (a) the Cu pillars are not contacting the side-wall of the TSH, and (b) the Cu pillars are almost at the center of the TSH. Figure 6.28 also shows the SEM image of a cross-section of the assembly, which includes all the key elements such as the top-chip, TSH-interposer, bottom-chip, package substrate, PCB, micro bumps, solder bumps, solder ball, TSH, and Cu pillars. It can be seen through the x-ray and SEM images that the key elements of the structure are properly fabricated.

## 6.6 TSMC's CoWoS

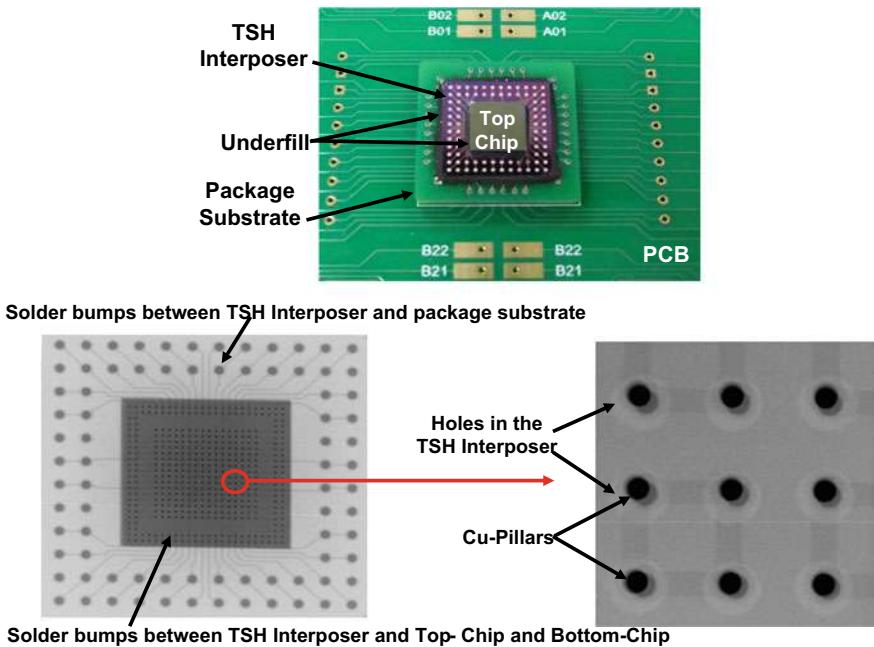
During the TSMC's investor conference for the third quarter of 2011 when Dr. Morris Chang (founder of TSMC), without any advance warning, shocked everybody by announcing his company would move into the packaging and testing field.



**Fig. 6.27** Through-silicon hole (TSH) packaging



**Fig. 6.28** TSH test vehicle. Cross section image of the TSH test vehicle



**Fig. 6.29** The assembled structure. X-ray image of the Cu-pillars and silicon holes

The first product would be CoWoS (chip-on-wafer-on-substrate), which integrates logic computing and memory chips by mounting them on a silicon interposer and then placing them directly on a package substrate. Today, the industry calls CoWoS as 2.5D IC integration.

## 6.7 Xilinx/TSMC's 2.5D IC Integration

Since 2011 Xilinx have been published papers on 2.5D IC integration [46–60]. As shown in Fig. 6.30, in order for better device manufacturing yield (to save cost), a very large SoC (system-on-chip) has been sliced into 4 smaller FPGA (field-programmable gate array) chips made by TSMC's 28 nm process technology. The 10,000 + of lateral interconnections between FPGA chips are connected mainly by the 0.4  $\mu\text{m}$ -pitch (minimum) RDLs of the TSV-interposer. The minimum thickness of the metal layer and dielectric layer of the RDLs is  $\sim 1 \mu\text{m}$ . Each FPGA has more than 50,000 micro bumps (200,000 + micro bumps on the TSV-interposer) at 45  $\mu\text{m}$  pitch as shown in Figs. 6.31 and 6.32. Thus, passive TSV/RDL interposers are for extremely fine-pitch, high-I/O, high performance, and high-density semiconductor IC applications. On October 20, 2013 Xilinx and TSMC [61] have jointly announced production release of the Virtex-7 HT family with 28 nm process technology, what

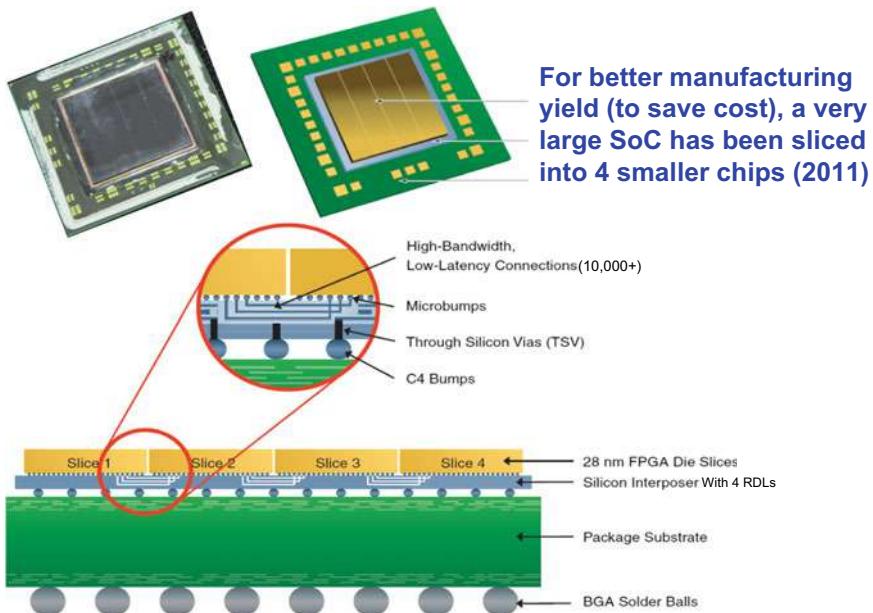
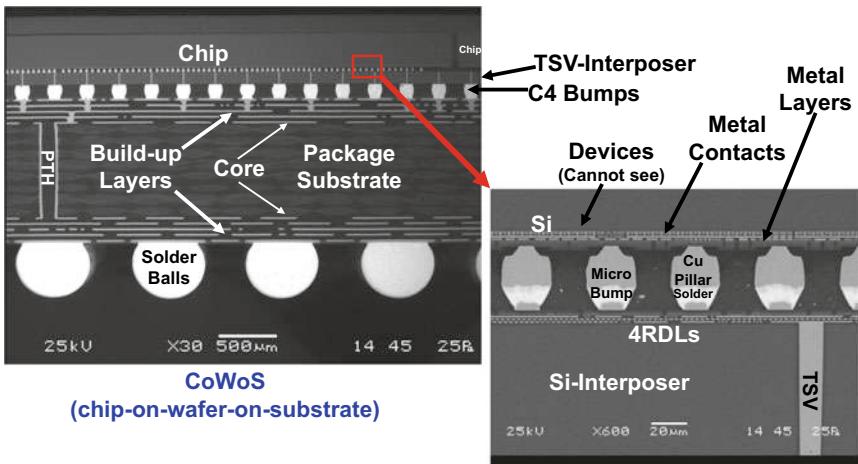


Fig. 6.30 Xilinx's sliced FPGA [46]



- RDLS: 0.4μm-pitch line width and spacing
- Each FPGA has >50,000 pbumps on 45μm pitch
- Interposer is supporting >200,000 pbumps

Fig. 6.31 Xilinx/TSMC's CoWoS for FPGA [52]

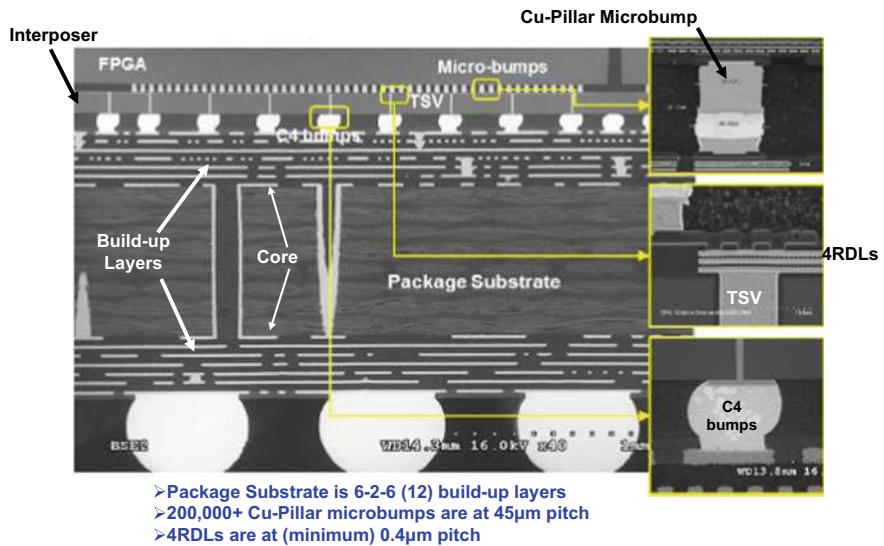
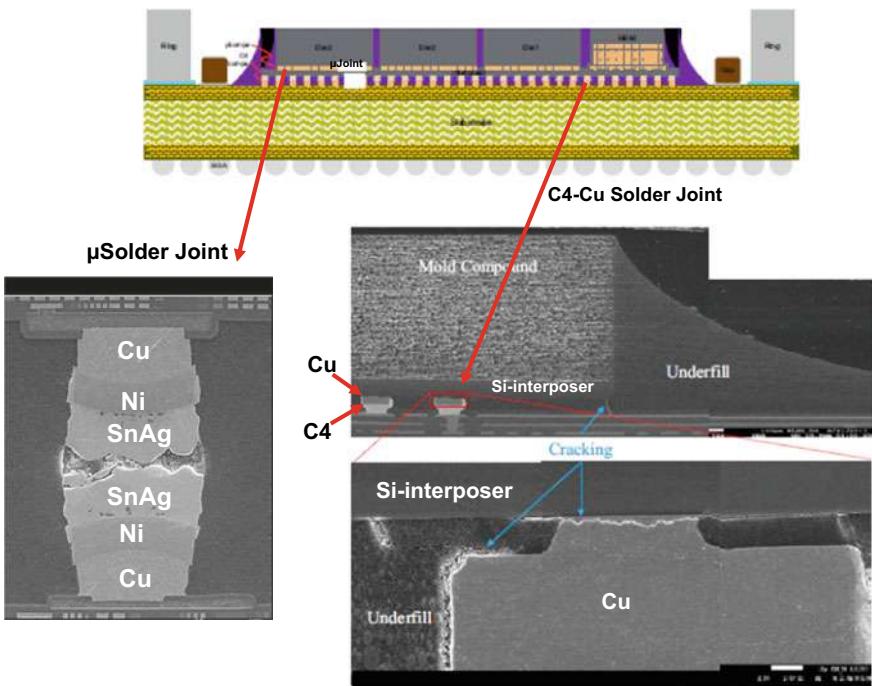


Fig. 6.32 Xilinx/TSMC's CoWoS (6-2-6 build-up package substrate) [52]

the pair claims is the industry's first 2.5D IC integration in production. The Xilinx Virtex-7 HT FPGAs feature up to sixteen 28.05Gbps and seventy-two 13.1Gbps transceivers.



Fig. 6.33 Xilinx/TSMC's VIRTEX [60]



**Fig. 6.34** SEM images of the Xilinx/TSMC's VIRTEX [60]

Today, Xilinx and TSMC are working far beyond the above. Figure 6.33 shows a test vehicle, which consists of a  $31.5\text{ mm} \times 41.7\text{ mm} \times 100\text{ }\mu\text{m}$  TSV-interposer and is fabricated using TSMC's CoWoS XLT<sup>TM</sup> 65 nm BEOL technology. There are three FPGAs and two HBMs (high bandwidth memories). The package substrate size is  $55\text{ mm} \times 55\text{ mm} \times 1.9\text{ mm}$ . For the first batch of thermal cycling test results there are some failures before the required 1200 cycles. Figure 6.34 shows cross-section scanning electron microscopy (SEM) failure analysis. The SEM shows a crack in the C4 underfill running from the edge of the interposer to the C4 bump region. The crack is primarily located along the interposer edge, along it occasionally appears along the copper pillar in the C4. The stress which causes failure is primarily due to CTE mismatch between the substrate and die-interposer assembly. The shrinking of the underfill due to curing and thermal aging is a secondary concern. By increasing the substrate thickness, the thermal cycling test passed the 1200 cycles. For more information, please read [59].

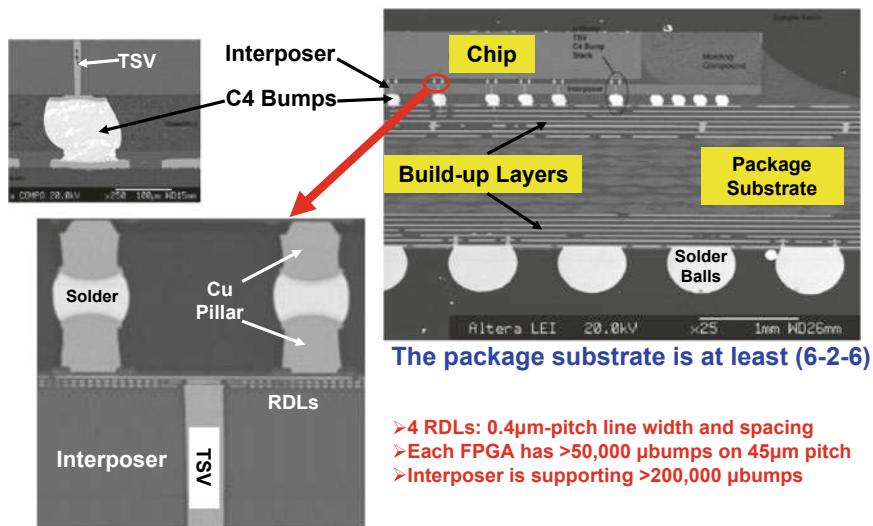


Fig. 6.35 Altera/TSMC's CoWoS [63]

## 6.8 Altera/TSMC's 2.5D IC Integration

Figure 6.35 shows one of the cross sections of Altera's 2.5D IC integration [62, 63]. It can be seen that the chips are supported by the TSV-interposer with Cu-pillar + solder cap microbumps. Then the TSV-interposer is C4 bumped on a 6-2-6 package substrate. The TSV-interposer is fabricated by TSMC's CoWoS technology. Unfortunately, this never went into HVM.

## 6.9 AMD/UMC's 2.5D IC Integration

Figure 6.36 shows AMD's Radeon R9 Fury X graphic processor unit (GPU) shipped in the second-half of 2015. The GPU is built on TSMC's 28 nm process technology and is supported by four HBM (high bandwidth memory) which will be discussed in Chap. 7 cubes manufactured by Hynix. Each HBM consists of four DRAMs with Cu-pillar + solder cap bumps and a logic base with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM cubes are on top of a TSV interposer (28 mm  $\times$  35 mm), which is fabricated by UMC with a 64 nm process technology. The final assembly of the TSV interposer with C4 (controlled collapse chip connection) bumps on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

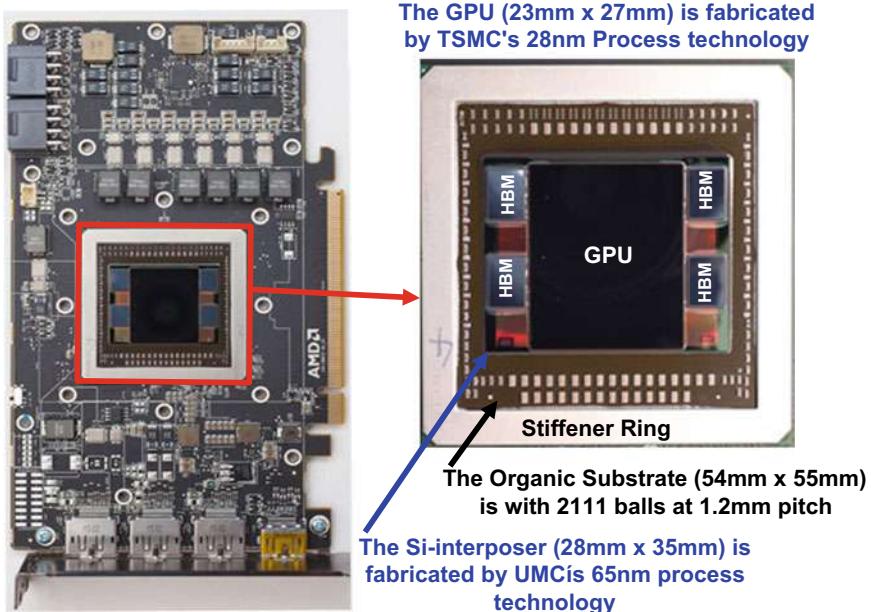


Fig. 6.36 AMD/UMC's GPU (Fiji)

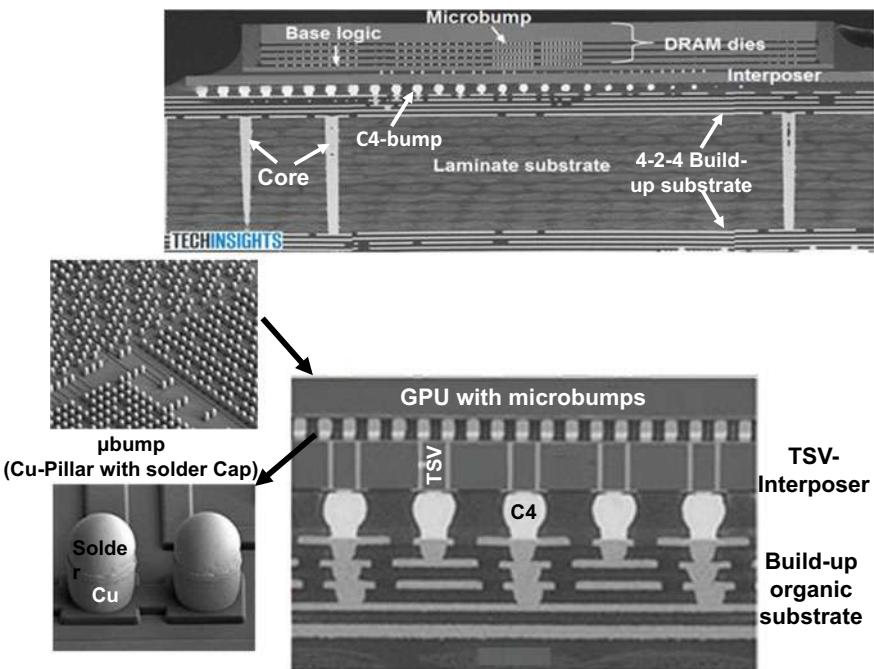
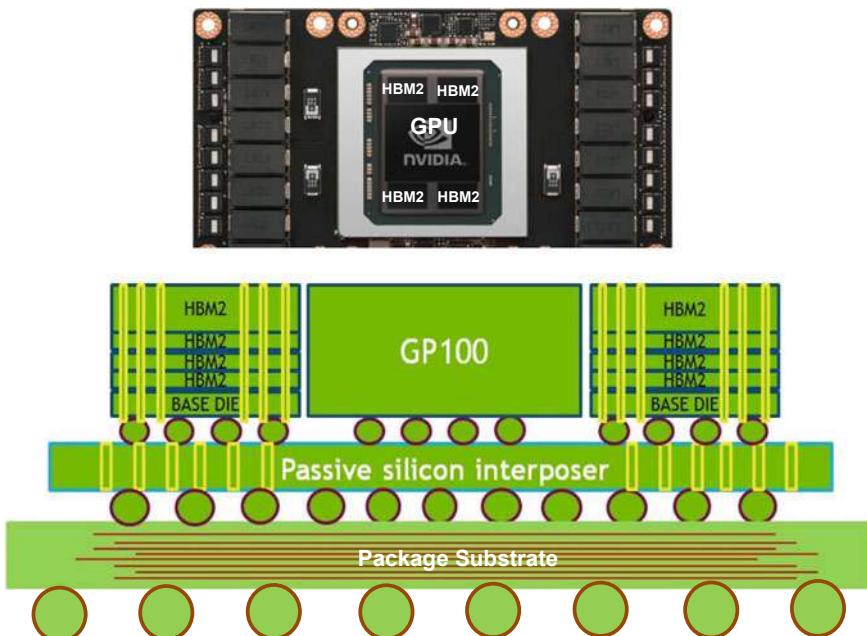


Fig. 6.37 SEM images of the AMD/UMC's GPU module

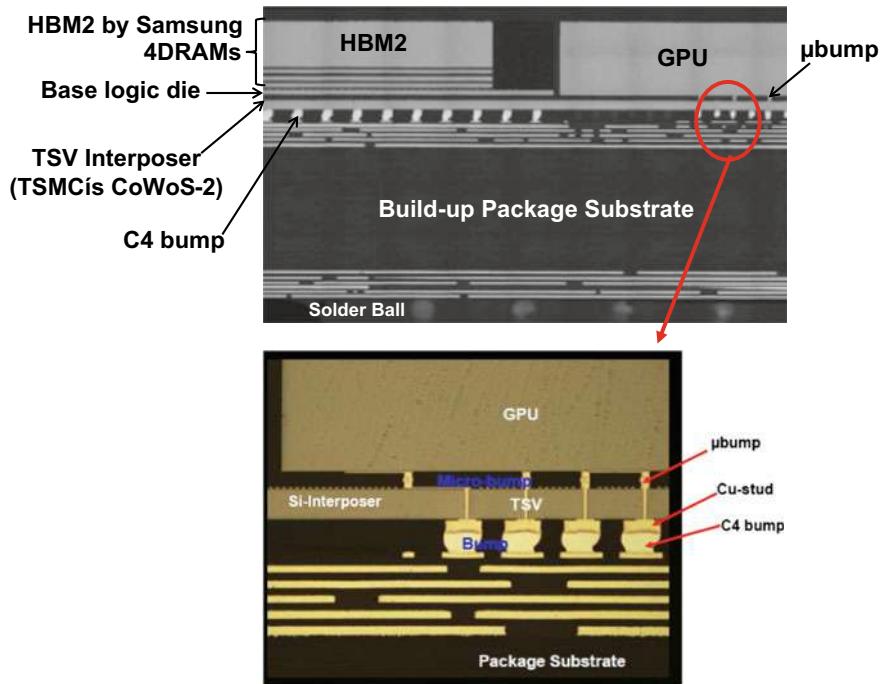
Some cross section SEM images are shown in Fig. 6.37. It can be seen that the GPU and the HBM are supported by the TSV-interposer with microbumps (Cu-pillar + solder cap). The TSV-interposer is supported by the 4-2-4 build-up package substrate with C4 bumps.

## 6.10 NVidia/TSMC's 2.5D IC Integration

Figures 6.38 and 6.39 show NVidia's Pascal 100 GPU, which was shipped in the second-half of 2016. The GPU is built on TSMC's 16 nm process technology and is supported by four HBM2 (16 GB) fabricated by Samsung [43]. Each HBM2 consists of four DRAMs with Cu-pillar + solder cap bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2s are attached with microbumps on top of a TSV interposer ( $1200 \text{ mm}^2$ ), which is fabricated by TSMC with a 64 nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with Cu-C4 bumps.



**Fig. 6.38** NVidia/TSMC's P100 [43]



**Fig. 6.39** SEM images of the NVidia/TSMC's P100 [43]

## 6.11 TSMC's CoWoS Roadmap

TSMC's roadmap on CoWoS is shown in Fig. 6.40 [64]. It can be seen that the first version (1.0X maximum reticle size  $\sim 33 \text{ mm} \times 26 \text{ mm} = 858 \text{ mm}^2$ ) in 2011 is for the product of Xilinx in 2013. Over the years, CoWoS technology development has focused on supporting increasing silicon interposer dimensions. TSMC will be expanding the interposer size to 3X maximum reticle (2021) and 4X maximum reticle (2023), to support processors and HBM stacks in the overall package.

## 6.12 Recent Advances in 2.5D IC Integration

Some recent developments on 2.5D IC integration are briefly mentioned in this section.

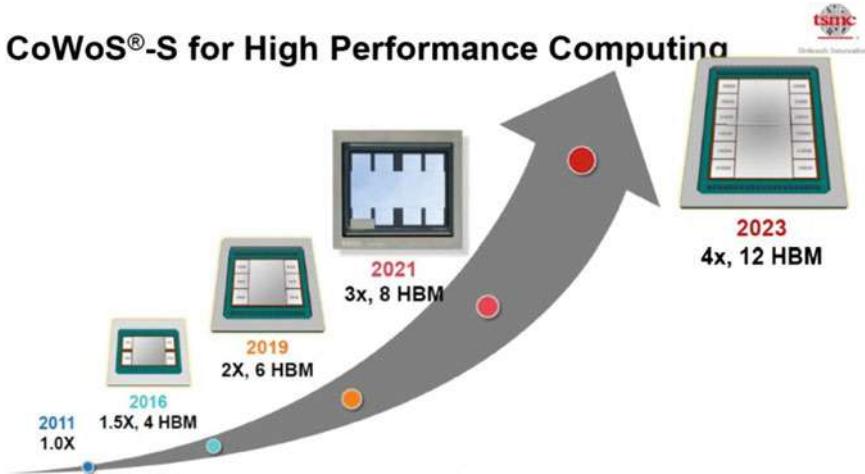


Fig. 6.40 TSMC CoWoS roadmap

### 6.12.1 TSMC's CoWoS with Deep Trench Capacitor (DTC)

Figure 6.41 shows a conceptual structure of high performance computing on a new CoWoS platform [65]. It consists of a logic die, HBM2Es, a silicon interposer, and a substrate. The logic and HBM2Es are first bonded side-by-side on the silicon interposer to form chip-on-wafer (CoW) with the fine pitch and high density interconnect routing among the devices. In the silicon interposer, the DTC is developed with the high aspect ratio silicon etch at dimensions. The high-k dielectric layer of the DTC is sandwiched between a top and a bottom electrode layer in the silicon trenches of aspect ratio over 10 to form the capacitor [65]. Two distinct process sequences are available to realize the DTC in the silicon interposer.

Figure 6.42a shows normalized capacitance density versus voltage of the DTC that is defined over the equivalent plenary surface area over the DTC structure. The capacitance density at 100 kHz measured by a LCR meter is  $\sim 300 \text{ nF/mm}^2$  at zero applied voltage for the high-k dielectric film. It provides the capacitance density of an order higher than metal-insulator-metal capacitor. Figure 6.42b shows two normalized I-V curves for this high-k dielectric film measured at 25 °C and 100 °C, respectively. It can be seen that the measured leakage current at  $\pm 1.35 \text{ V}$  bias is still below  $1 \text{ fA}/\mu\text{m}^2$  even at the testing temperature of 10 °C. This excellent characteristic prevents the additional power wasted in the DTC [65].

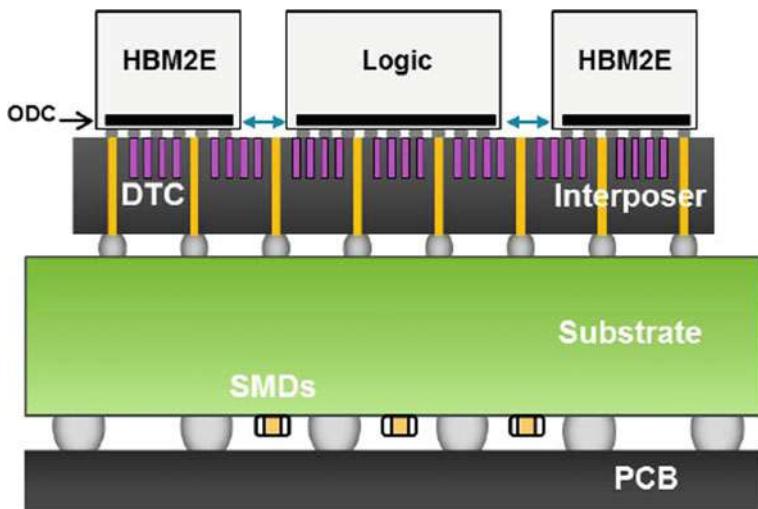


Fig. 6.41 TSMC' CoWoS with deep trench capacitor [65]

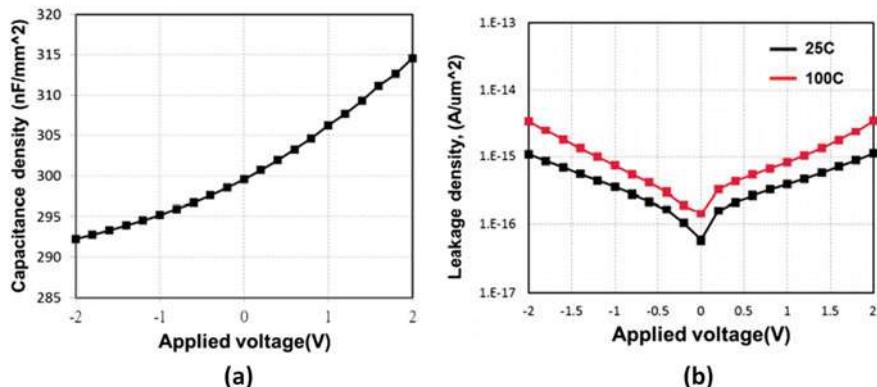
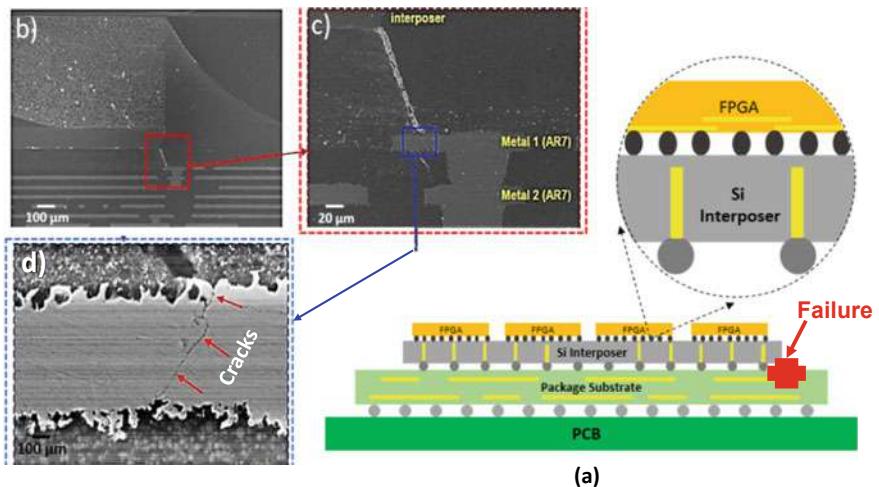


Fig. 6.42 **a** Capacitance density versus applied voltage. **b** Leakage density versus applied voltage [65]

### 6.12.2 IME's Non-destructive Fault Isolation in 2.5D IC Integration

In [66], IME developed an approach, physical failure analysis (PFA), to accurately localize the failures in 2.5D IC integrations. Figure 6.43 shows the location of the open defect in a 2.5D IC structure. The PFA confirms the defect and reveals that the open failure is because of a crack in the metal layer right after the via near to the interface of the substrate and the interposer. The possible reason for such defect is

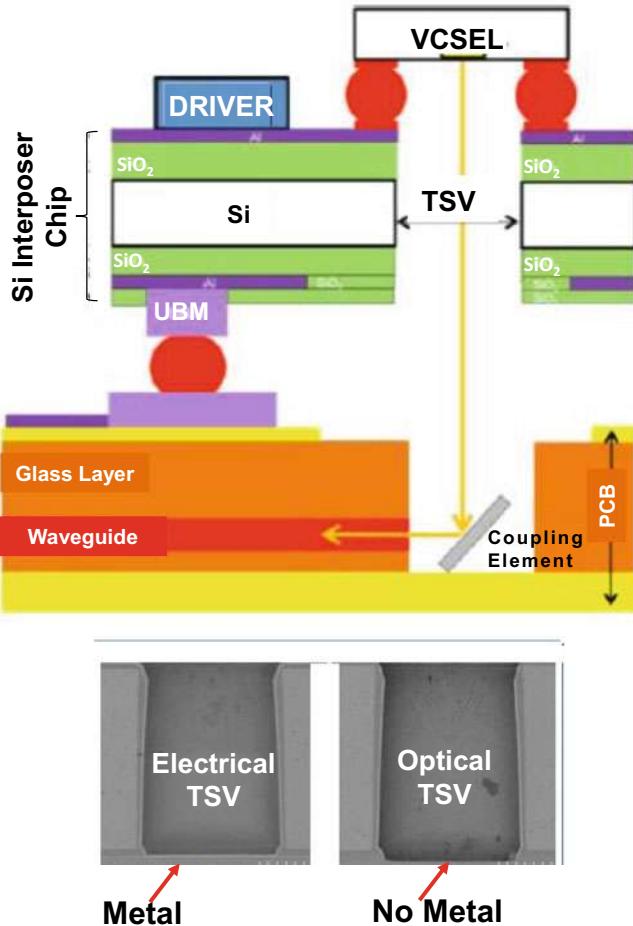


**Fig. 6.43** IME's non-destructive fault isolation in TSV-interposer [66]

due to the stress propagation from the edge of the silicon interposer to the substrate [66].

### 6.12.3 Fraunhofer's Photonics Interposer

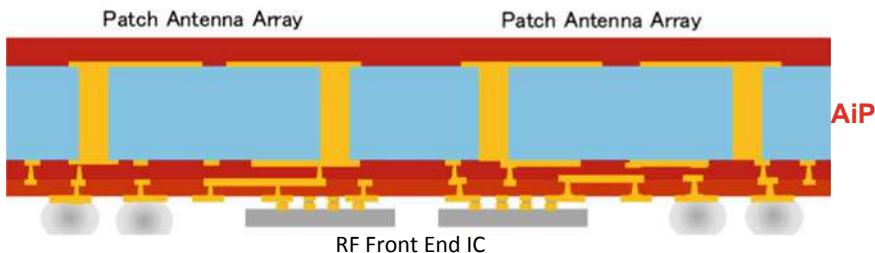
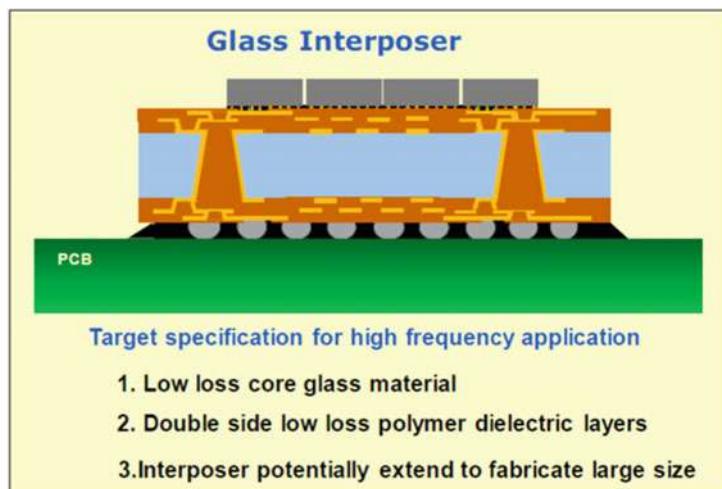
Figure 6.44 shows the conceptual layout of the single mode router. The interposer is intended to be assembled on an glass based OPCB (optical printed circuit board), where the interconnectivity between the optical layer of the OPCB and the Si-interposer is done vertically by means of one mirror coupling element, as shown in Fig. 6.44 [67]. For the routing operation, each one of the 12 optical channels streamed from the OPCB is fed to a separate PD (photodiode) and its respective electronic TIA (transimpedance amplifier). The TIA can then perform opto-electronic conversion of the incoming signals, while the received electrical signal is then transmitted to an electronic driver amplifier prior to driving the modulation operation of a VCSEL (vertical-cavity surface-emitting laser). Each VCSEL is then tuned to a different wavelength through current injection to match the channel spacing of the AWG (arrays waveguide grating) multiplexer on the silicon layer. TSVs used for electrical connection of frond-and backsides of the wafer using underlying metals stack (left) and so-called optical TSV without metal layers at the TSV bottom (right).



**Fig. 6.44** Fraunhofer's photonics TSV-interposer [67]

#### 6.12.4 Dai Nippon/AGC's Glass Interposer

Figure 6.45 shows Dai Nippon/AGC's glass interposer for high frequency and high speed applications, especially for antenna-in-package (AiP) [68]. Their basic structure consists of coplanar waveguide (CPW) on top of a quartz substrate with through quartz via (TQV) connecting top to bottom circuits. The process flow is shown in Fig. 6.46 and the typical TGV (through-glass via) and Cu wiring are also shown. The interposer thickness is 400  $\mu\text{m}$ , and the top-diameter of the TGV is approximately 80  $\mu\text{m}$  while the bottom-diameter is 50  $\mu\text{m}$ . The linewidth and spacing of the Cu wire are 2  $\mu\text{m}$ .



**Fig. 6.45** Dai Nippon/AGC's glass interposer for AiP [68]

### 6.12.5 Fujitsu's Multilayer Glass Interposer

Figure 6.47 shows Fujitsu's multilayer glass interposer. The TGVs are fabricated by the laser induced deep etching (LIDE). The TGVs are filled by screen printing of a conductive paste. The microbumps (Cu-pillar + solder cap) at 40  $\mu\text{m}$ -pitch are the interconnects between the chip and the glass interposer. For more information of this package, please read [69].

## 6.13 Summary and Recommendation

Some important results and recommendations are summarized as follows.

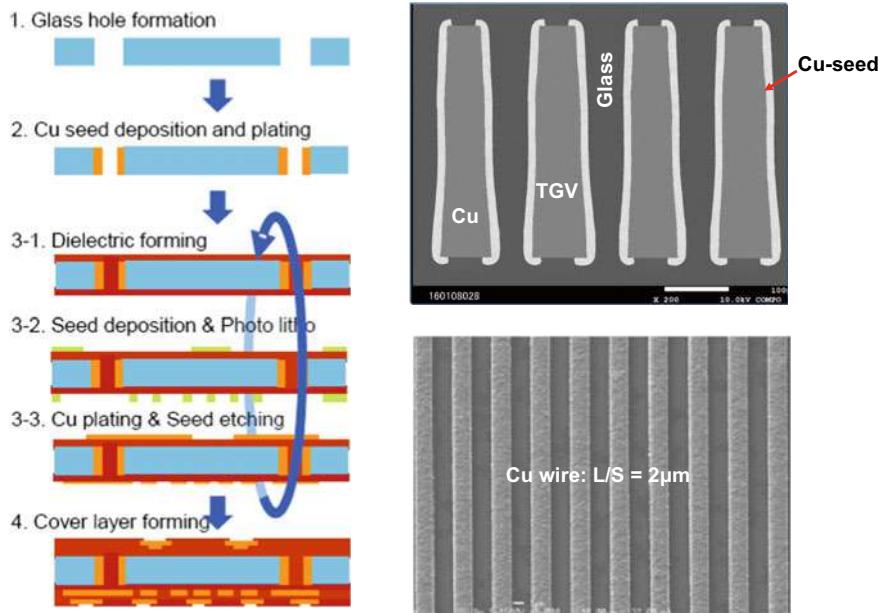


Fig. 6.46 Process flow. TGV and wiring RDL on the glass interposer [68]

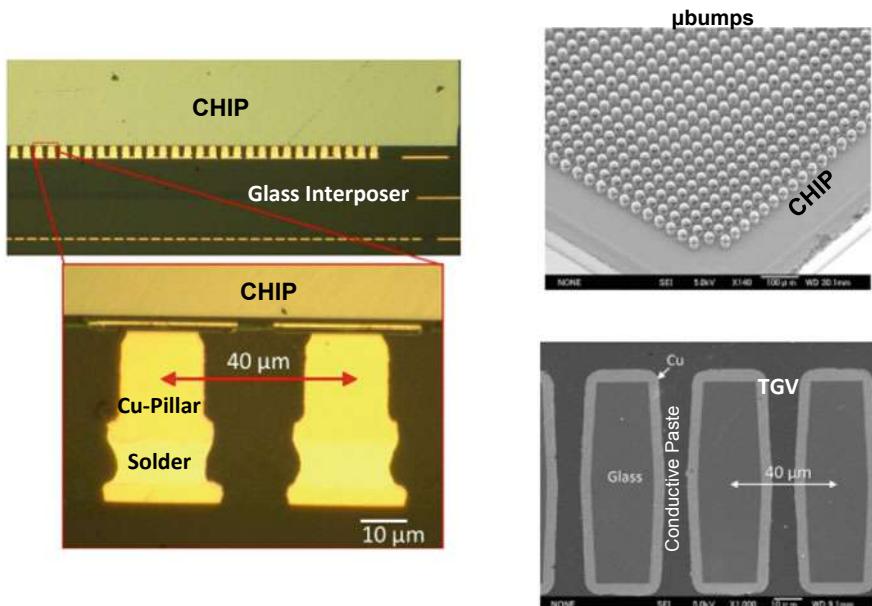


Fig. 6.47 Fujitsu's glass interposer with TGV filled with conductive paste [69]

- 2.5D IC integration is meant for very high-performance and high-density applications such as HPC. Usually, the passive TSV-interposer is supporting the very large SoC such as CPU or GPU and a few HBM, HBM2, or HBM2E.
- According to TSMC CoWoS roadmap, the size of the passive TSV-interposer is getting bigger. During SEMICON Taiwan (September 2020), TSMC announced that they are working on a TSV-interposer and the size is approximately 2400 mm<sup>2</sup>. One of their potential customers is trying to use a build-up package substrate (70 mm × 78 mm) to support the TSV-interposer.
- When the size of the TSV-interposer is very large, the assembly of chips on the TSV-interposer and of the TSV-interposer on the build-up package substrate poses a great challenge (due to warpage issue of the large interposer and substrate). Also, SMT assembly of the module on PCB posts another big challenge (due to the warpage issue of the module).
- When the size of the TSV-interposer is very large, reliability is a big issue. The reliability of the microbumps between the chips and the interposer and of the C4 bumps between the interposer and package substrate can be secured with underfill. However, because of the size of the package substrate, the solder joint reliability between the package substrate and PCB could be an issue. May be underfill is needed on the PCB.
- For more information on 2.5D IC integration, please read [92–96].

## References

1. Souriau, J., O. Lignier, M. Charrier, and G. Poupon, “Wafer Level Processing Of 3D System in Package for RF and Data Applications”, *IEEE/ECTC Proceedings*, 2005, pp. 356–361.
2. Henry, D., D. Belhachemi, J-C. Souriau, C. Brunet-Manquat, C. Puget, G. Ponthenier, J. Vallejo, C. Lecouvey, and N. Sillon, “Low Electrical Resistance Silicon Through Vias: Technology and Characterization”, *IEEE/ECTC Proceedings*, 2006, pp. 1360–1366.
3. Selvanayagam, C., J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, “Nonlinear Thermal Stress/Strain Analysis of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps”, *IEEE/ECTC Proceedings*, May 2008, pp. 1073–1081.
4. Yu, A., N. Khan, G. Archit, D. Pinjala, K. Toh, V. Kripesh, S. Yoon, and J. H. Lau, “Fabrication of Silicon Carriers with TSV Electrical Interconnection and Embedded Thermal Solutions for High Power 3-D Package”, *IEEE/ECTC Proceedings*, May 2008, pp. 24–28.
5. Khan, N., V. Rao, S. Lim, H. We, V. Lee, X. Zhang, E. Liao, R. Nagarajan, T. C. Chai, V. Kripesh, and J. H. Lau, “Development of 3-D Silicon Module With TSV for System in Packaging”, *IEEE/ECTC Proceedings*, May 2008, pp. 550–555.
6. Selvanayagam, C., J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, “Nonlinear Thermal Stress/Strain Analyses of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps”, *IEEE Transactions on Advanced Packaging*, Vol. 32, No. 4, November 2009, pp. 720–728.
7. Khan, N., L. Yu, P. Tan, S. Ho, N. Su, H. Wai, K. Vaidyanathan, D. Pinjala, J. H. Lau, T. Chuan, “3D Packaging with Through Silicon Via (TSV) for Electrical and Fluidic Interconnections”, *IEEE/ECTC Proceedings*, May, 2009, pp. 1153–1158.
8. Yu, A., N. Khan, G. Archit, D. Pinjala, K. Toh, V. Kripesh, S. Yoon, and J. H. Lau, “Fabrication of Silicon Carriers With TSV Electrical Interconnections and Embedded Thermal Solutions

- for High Power 3-D Packages”, *IEEE Transactions on CPMT*, Vol. 32, No. 3, September 2009, pp. 566–571.
- 9. Tang, G. Y., S. Tan, N. Khan, D. Pinjala, J. H. Lau, A. Yu, V. Kripesh, and K. Toh, “Integrated Liquid Cooling Systems for 3-D Stacked TSV Modules”, *IEEE Transactions on CPMT*, Vol. 33, No. 1, March 2010, pp. 184–195.
  - 10. Khan, N., H. Li, S. Tan, S. Ho, V. Kripesh, D. Pinjala, J. H. Lau, and T. Chuan, “3-D Packaging With Through-Silicon Via (TSV) for Electrical and Fluidic Interconnections”, *IEEE Transactions on CPMT*, Vol. 3, No. 2, February 2013, pp. 221–228.
  - 11. Khan, N., V. Rao, S. Lim, H. We, V. Lee, X. Zhang, E. Liao, R. Nagarajan, T. C. Chai, V. Kripesh, and J. H. Lau, “Development of 3-D Silicon Module With TSV for System in Packaging”, *IEEE Transactions on CPMT*, Vol. 33, No. 1, March 2010, pp. 3–9.
  - 12. Zhang, X., T. Chai, J. H. Lau, C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, et al., “Development of Through Silicon Via (TSV) Interposer Technology for Large Die (21x21mm) Fine-pitch Cu/low-k FCBGA Package”, *IEEE/ECTC Proceedings*, May 2009, pp. 305–312.
  - 13. Chai, T. C., X. Zhang, J. H. Lau, C. S. Selvanayagam, D. Pinjala, et al., “Development of Large Die Fine-Pitch Cu/low-k FCBGA Package with through Silicon via (TSV) Interposer”, *IEEE Transactions on CPMT*, Vol. 1, No. 5, May 2011, pp. 660–672.
  - 14. Lau, J. H., S. Lee, M. Yuen, J. Wu, C. Lo, H. Fan, and H. Chen, “Apparatus having thermal-enhanced and cost-effective 3D IC integration structure with through silicon via interposer”. US Patent No: 8,604,603, Filed Date: February 19, 2010, Date of Patent: December 10, 2013.
  - 15. Lau, J. H., Y. S. Chan, and R. S. W. Lee, “3D IC Integration with TSV Interposers for High-Performance Applications”, *Chip Scale Review*, Vol. 14, No. 5, September/October, 2010, pp. 26–29.
  - 16. Lau, J. H., M. S. Zhang, and S. W. R. Lee, “Embedded 3D Hybrid IC Integration System-in-Package (SiP) for Opto-Electronic Interconnects in Organic Substrates”, *ASME Transactions, Journal of Electronic Packaging*, Vol. 133, September 2011, pp. 1–7.
  - 17. Chien, J., Y. Chao, J. H. Lau, M. Dai, R. Tain, M. Dai, P. Tzeng, C. Lin, Y. Hsin, S. Chen, J. Chen, C. Chen, C. Ho, R. Lo, T. Ku, and M. Kao, “A Thermal Performance Measurement Method for Blind Through Silicon Vias (TSVs) in a 300 mm Wafer”, *IEEE/ECTC Proceedings*, June 2011, pp. 1204–1210.
  - 18. Chien, H. C., J. H. Lau, Y. Chao, R. Tain, M. Dai, S. T. Wu, W. Lo, and M. J. Kao, “Thermal Performance of 3D IC Integration with Through-Silicon Via (TSV)”, *Proceedings of IMAPS International Conference*, Long Beach, CA, October 2011, pp. 25–32.
  - 19. Chien, H. C., J. H. Lau, Y. Chao, R. Tain, M. Dai, S. T. Wu, W. Lo, and M. J. Kao, “Thermal Performance of 3D IC Integration with Through-Silicon Via (TSV)”, *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 9, 2012, pp. 97–103.
  - 20. Chien, J., J. H. Lau, Chao, Y. M. Dai, R. Tain, L. Li, P. Su, J. Xue, M. Brillhart, “Thermal Evaluation and Analyses of 3D IC Integration SiP with TSVs for Network System Applications”, *IEEE/ECTC Proceedings*, May 2012, pp. 1866–1873.
  - 21. Chien, H., J. H. Lau, T. Chao, M. Dai, and R. Tain, “Thermal Management of Moore’s Law Chips on Both sides of an Interposer for 3D IC integration SiP”, *IEEE/ICEP Proceedings*, Japan, April 2012, pp. 38–44.
  - 22. Lau, J. H., H. C. Chien, and R. Tain, “TSV Interposers with Embedded Microchannels for 3D IC and LED Integration”, *ASME Paper no. InterPACK2011-52204*, Portland, OR, July 2011.
  - 23. Lau, J. H., C-J Zhan, P-J Tzeng, C-K Lee, M-J Dai, H-C Chien, Y-L Chao, et al., “Feasibility Study of a 3D IC Integration System-in-Packaging (SiP) from a 300 mm Multi-Project Wafer (MPW)”, *IMAPS International Symposium on Microelectronics*, October 2011, pp. 446–454.
  - 24. Lau, J. H., C-J Zhan, P-J Tzeng, C-K Lee, M-J Dai, H-C Chien, Y-L Chao, et al., “Feasibility Study of a 3D IC Integration System-in-Packaging (SiP) from a 300 mm Multi-Project Wafer (MPW)”, *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 8, No. 4, Fourth Quarter 2011, pp. 171–178.
  - 25. Zhan, C., P. Tzeng, J. H. Lau, M. Dai, H. Chien1, C. Lee, S. Wu, et al., “Assembly Process and Reliability Assessment of TSV/RDL/IPD Interposer with Multi-Chip-Stacking for 3D IC Integration SiP”, *IEEE/ECTC Proceedings*, May 2012, pp. 548–554.

26. Tzeng, P., J. H. Lau, M. Dai, S. Wu, H. Chien, Y. Chao, C. Chen, S. Chen, C. Wu, C. Lee, C. Zhan, J. Chen, Y. Hsu, T. Ku, and M. Kao, "Design, Fabrication, and Calibration of Stress Sensors Embedded in a TSV Interposer in a 300 mm Wafer", *IEEE/ECTC Proceedings*, San Diego, CA, May 2012, pp. 1731–1737.
27. Sheu, S., Z. Lin, J. Hung, J. H. Lau, P. Chen, S. Wu, K. Su, C. Lin, S. Lai, T. Ku, W. Lo, M. Kao, "An Electrical Testing Method for Blind Through Silicon Vias (TSVs) for 3D IC Integration", *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 8, No. 4, Fourth Quarter 2011, pp. 140–145.
28. Chen, J. C., J. H. Lau, P. J. Tzeng, S. Chen, C. Wu, C. Chen, H. Yu, Y. Hsu, S. Shen, S. Liao, C. Ho, C. Lin, T. K. Ku, and M. J. Kao, "Effects of Slurry in Cu Chemical Mechanical Polishing (CMP) of TSVs for 3-D IC Integration", *IEEE Transactions on CPMT*, Vol. 2, No. 6, June 2012, pp. 956–963.
29. Lau, J. H., and G. Y. Tang, "Effects of TSVs (through-silicon vias) on thermal performances of 3D IC integration system-in-package (SiP)", *Journal of Microelectronics Reliability*, Vo. 52, Issue 11, November 2012, pp. 2660–2669.
30. Lau, J. H., S. T. Wu, and H. C. Chien, "Nonlinear Analyses of Semi-Embedded Through-Silicon Via (TSV) Interposer with Stress Relief Gap Under Thermal Operating and Environmental Conditions", *IEEE EuroSime Proceedings, Chapter 11: Thermo-Mechanical Issues in Microelectronics*, Lisbon, Portugal, April 2012, pp. 1/6–6/6.
31. Wu, C., S. Chen, P. Tzeng, J. H. Lau, Y. Hsu, J. Chen, Y. Hsin, C. Chen, S. Shen, C. Lin, T. Ku, and M. Kao, "Oxide Liner, Barrier and Seed Layers, and Cu-Plating of Blind Through Silicon Vias (TSVs) on 300 mm Wafers for 3D IC Integration", *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 9, No. 1, First Quarter 2012, pp. 31–36.
32. Li, L., P. Su, J. Xue, M. Brillhart, J. H. Lau, P. Tzeng, C. Lee, C. Zhan, M. Dai, H. Chien, and S. Wu, "Addressing Bandwidth Challenges in Next Generation High Performance Network Systems with 3D IC Integration," *IEEE ECTC Proceedings*, San Diego, CA, May 2012, pp. 1040–1046.
33. Lau, J. H., P. Tzeng, C. Zhan, C. Lee, M. Dai, J. Chen, Y. Hsin, S. Chen, C. Wu, L. Li, P. Su, J. Xue, and M. Brillhart, "Large Size Silicon Interposer and 3D IC Integration for System-in-Packaging (SiP)", *Proceedings of the 45th IMAPS International Symposium on Microelectronics*, September 2012, pp. 1209–1214.
34. Lau, J. H., P. Tzeng, C. Lee, C. Zhan, M. Li, J. Cline, K. Saito, Y. Hsin, P. Chang, Y. Chang, J. Chen, S. Chen, C. Wu, H. Chang, C. Chien, C. Lin, T. Ku, R. Lo, and M. Kao, (Redistribution Layers (RDLs) for 2.5D/3D IC Integration", *Proceedings of the 46th IMAPS International Symposium on Microelectronics*, October 2013, pp. 434–441.
35. Wu, S. T., H. Chien, J. H. Lau, M. Li, J. Cline, and M. Ji, "Thermal and Mechanical Design and Analysis of 3D IC Interposer with Double-Sided Active Chips", *IEEE/ECTC Proceedings*, May 2013, pp. 1471–1479.
36. P. J., Tzeng, J. H. Lau, C. Zhan, Y. Hsin, P. Chang, Y. Chang, J. Chen, S. Chen, C. Wu, C. Lee, H. Chang, C. Chien, C. Lin, T. Ku, M. Kao, M. Li, J. Cline, K. Saito, and M. Ji, "Process Integration of 3D Si Interposer with Double-Sided Active Chip Attachments", *IEEE/ECTC Proceedings*, May 2013, pp. 86–93.
37. Lau, J. H., P. Tzeng, C. Lee, C. Zhan, M. Li, J. Cline, K. Saito, Y. Hsin, P. Chang, Y. Chang, J. Chen, S. Chen, C. Wu, H. Chang, C. Chien, C. Lin, T. Ku, R. Lo, and M. Kao, "Redistribution Layers (RDLs) for 2.5D/3D IC Integration", *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 11, No. 1, First Quarter 2014, pp. 16–24.
38. Lau, J. H., C. Lee, C. Zhan, S. Wu, Y. Chao, M. Dai, R. Tain, H. Chien, C. Chien, R. Cheng, Y. Huang, Y. Lee, Z. Hsiao, W. Tsai, P. Chang, H. Fu, Y. Cheng, L. Liao, W. Lo, and M. Kao, "Low-Cost TSH (Through-Silicon Hole) Interposers for 3D IC Integration", *Proceedings of IEEE/ECTC*, May 2014, pp. 290–296.
39. Lau, J. H., C. Lee, C. Zhan, S. Wu, Y. Chao, M. Dai, R. Tain, H. Chien, J. Hung, C. Chien, R. Cheng, Y. Huang, Y. Lee, Z. Hsiao, W. Tsai, P. Chang, H. Fu, Y. Cheng, L. Liao, W. Lo, and M. Kao, "Low-Cost Through-Silicon Hole Interposers for 3D IC Integration", *IEEE Transactions on CPMT*, Vol. 4, No. 9, September 2014, pp. 1407–1419.

40. Hsieh, M. C., S. T. Wu, C. J. Wu, and J. H. Lau, "Energy Release Rate Estimation for Through Silicon Vias in 3-D Integration", *IEEE Transactions on CPMT*, Vol. 4, No. 1, January 2014, pp. 57–65.
41. Lee, C. C., C. S. Wu,, K. S. Kao, C. W. Fang, C. J. Zhan, J. H. Lau, and T. H. Chen, "Impact of high density TSVs on the assembly of 3D-ICs packaging", *Microelectronic Engineering*, Vol. 107, July 2013, pp. 101–106.
42. Che, F., M. Kawano, M. Ding, Y. Han, and S. Bhattacharya, "Co-design for Low Warpage and High Reliability in Advanced Package with TSV-Free Interposer (TFI)", *Proceedings of IEEE/ECTC*, May 2017, pp. 853–861.
43. Hou, S., W. Chen, C. Hu, C. Chiu, K. Ting, T. Lin, W. Wei, W. Chiou, V. Lin, V. Chang, C. Wang, C. Wu, and D. Yu, "Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology", *IEEE Transactions on Electron Devices*, October 2017, pp. 4071–4077.
44. Lau, J. H., and G. Tang, "Thermal Management of 3D IC Integration with TSV (Through Silicon Via)", *IEEE/ECTC Proceedings*, May 2009, pp. 635–640.
45. Lau, J. H., "TSV Manufacturing Yield and Hidden Costs for 3D IC Integration", *IEEE/ECTC Proceedings*, May 2010, pp. 1031–1041.
46. Banijamali, B., S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced Reliability Study of TSV Interposers and Interconnects for the 28 nm Technology FPGA", *Proceedings of IEEE/ECTC*, May 2011, pp. 285–290.
47. Kim, N., D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer Design Optimization for High Frequency Signal Transmission in Passive and Active Interposer using Through Silicon Via (TSV)", *IEEE/ECTC Proceedings*, May 2011, pp. 1160–1167.
48. Banijamali, B., S. Ramalingam, N. Kim, C. Wyland, N. Kim, D. Wu, J. Carrel, J. Kim, and Paul Wu, "Ceramics versus low-CTE Organic packaging of TSV Silicon Interposers", *IEEE/ECTC Proceedings*, May 2011, pp. 573–576.
49. Chaware, R., K. Nagarajan, and S. Ramalingam, "Assembly and Reliability Challenges in 3D Integration of 28 nm FPGA Die on a Large High Density 65 nm Passive Interposer", *Proceedings of IEEE/ECTC*, May 2012, San Diego, CA, pp. 279–283.
50. Banijamali, B., S. Ramalingam, H. Liu and M. Kim, "Outstanding and Innovative Reliability Study of 3D TSV Interposer and Fine Pitch Solder Micro-bumps", *Proceedings of IEEE/ECTC*, San Diego, CA, May 2012, pp. 309–314.
51. Kim, N., D. Wu, J. Carrel, J. Kim, and P. Wu, "Channel Design Methodology for 28 Gb/s SerDes FPGA Applications with Stacked Silicon Interconnect Technology", *IEEE/ECTC Proceedings*, May 2012, pp. 1786–1793.
52. Banijamali, B., C. Chiu, C. Hsieh, T. Lin, C. Hu, S. Hou, et al., "Reliability evaluation of a CoWoS-enabled 3D IC package," *IEEE/ECTC Proceedings*, May 2013, pp. 35–40.
53. Hariharan, G., R. Chaware, L. Yip, I. Singh, K. Ng, S. Pai, M. Kim, H. Liu, and S. Ramalingam, "Assembly Process Qualification and Reliability Evaluations for Heterogeneous 2.5D FPGA with HiCTE Ceramic", *IEEE/ECTC Proceedings*, May 2013, pp. 904–908.
54. Kwon, W., M. Kim, J. Chang, S. Ramalingam, L. Madden, G. Tsai, S. Tseng, J. Lai, T. Lu, and S. Chin, "Enabling a Manufacturable 3D Technologies and Ecosystem using 28 nm FPGA with Stack Silicon Interconnect Technology", *IMAPS Proceedings of International Symposium on Microelectronics*, Orlando, FL, October 2013, pp. 217–222.
55. Banijamali, B., T. Lee, H. Liu, S. Ramalingam, I. Barber, J. Chang and M. Kim, and L. Yip, "Reliability Evaluation of an Extreme TSV Interposer and Interconnects for the 20 nm Technology CoWoS IC Package", *IEEE/ECTC Proceedings*, May 2015, pp. 276–280.
56. Hariharan, G., R. Chaware, I. Singh, J. Lin, L. Yip, K. Ng, and S. Pai, "A Comprehensive Reliability Study on a CoWoS 3D IC Package", *IEEE/ECTC Proceedings*, May 2015, pp. 573–577.
57. Chaware, R., G. Hariharan, J. Lin, I. Singh, G. O'Rourke, K. Ng, S. Pai, C. Li, Z. Huang, and S. Cheng, "Assembly Challenges in Developing 3D IC Package with Ultra High Yield and High Reliability", *IEEE/ECTC Proceedings*, May 2015, pp. 1447–1451.

58. Xu, J., Y. Niu, S. Cain, S. McCann, H. Lee, G. Ahmed, and S. Park, “The Experimental and Numerical Study of Electromigration in 2.5D Packaging”, *IEEE/ECTC Proceedings*, May 2018, pp. 483–489.
59. McCann, S., H. Lee, G. Ahmed, T. Lee, S. Ramalingam, “Warpage and Reliability Challenges for Stacked Silicon Interconnect Technology in Large Packages”, *IEEE/ECTC Proceedings*, May 2018, pp. 2339–2344.
60. Wang, H., J. Wang, J. Xu, V. Pham, K. Pan, S. Park, H. Lee, and G. Ahmed, “Product Level Design Optimization for 2.5D Package Pad Cratering Reliability during Drop Impact”, *IEEE/ECTC Proceedings*, May 2019, pp. 2343–2348.
61. <http://press.xilinx.com/2013-10-20-Xilinx-and-TSMCReach-Volume-Production-on-all-28nm-CoWoS-based-All-Programmable-3D-IC-Families>.
62. Xie, J., H. Shi, Y. Li, Z. Li, A. Rahman, K. Chandrasekar, D. Ratakonda, M. Deo, K. Chanda, V. Hool, M. Lee, N. Vodrahalli, D. Ibbotson, and T. Verma, “Enabling the 2.5D Integration”, *Proceedings of IMAPS International Symposium on Microelectronics*, September 2012, San Diego, CA, pp. 254–267.
63. Li, Z., H. Shi, J. Xie, and A. Rahman, “Development of an Optimized Power Delivery System for 3D IC Integration with TSV Silicon Interposer”, *Proceedings of IEEE/ECTC*, May 2012, pp. 678–682.
64. <https://sem/wiki.com/semiconductor-manufacturers/tsmc/290560-highlights-of-the-tsmc-technology-symposium-part-2>.
65. Chen, W., C. Lin, C. Tsai, H. Hsia, K. Ting, S. Hou, C. Wang, and D. Yu, “Design and Analysis of Logic-HBM2E Power Delivery System on CoWoS® Platform with Deep Trench Capacitor”, *IEEE/ECTC Proceedings*, May 2020, pp. 380–385.
66. Bhuvanendran, S., N. Gourikutty, K. Chua, J. Alton, J. Chinq, R. Umralkar, V. Chidambaram1, and S. Bhattacharya, “Non-destructive fault isolation in through-silicon interposer based system in package”, *IEEE/EPTC Proceedings*, December 2020, pp. 281–285.
67. Sirbu, B., Y. Eichhammer, H. Oppermann, T. Tekin, J. Kraft, V. Sidorov, X. Yin, J. Bauwelinck, C. Neumeyer, and F. Soares, “3D Silicon Photonics Interposer for Tb/s Optical Interconnects in Data Centers with double-side assembled active components and integrated optical and electrical Through Silicon Via on SOI”, *IEEE/ECTC Proceedings*, May 2020, pp. 1052–1059.
68. Tanaka, M., S. Kuramochi, T. Dai, Y. Sato, and N. Kidera, “High Frequency Characteristics of Glass Interposer”, *IEEE/ECTC Proceedings*, May 2020, pp. 601–610.
69. Iwai, T., T. Sakai, D. Mizutani, S. Sakuyama, K. Iida, T. Inaba, H. Fujisaki, A. Tamura, and Y. Miyazawa, “Multilayer Glass Substrate with High Density Via Structure for All Inorganic Multi-chip Module”, *IEEE/ECTC Proceedings*, May 2020, pp. 1952–1957.
70. Ding, Q., H. Liu, Y. Huan, and J. Jiang, “High Bandwidth Low Power 2.5D Interconnect Modeling and Design”, *IEEE/ECTC Proceedings*, May 2020, pp. 1832–1837.
71. Kim, M., H. Liu, D. Klokov, A. Wong, T. To, and J. Chang, “Performance Improvement for FPGA due to Interposer Metal Insulator Metal Decoupling Capacitors (MIMCAP)”, *IEEE/ECTC Proceedings*, May 2020, pp. 386–392.
72. Bhuvanendran, S., N. Gourikutty, Y. Chow, J. Alton, R. Umralkar, H. Bai, K. Chua, and S. Bhattacharya, “Defect Localization in Through-Si-Interposer Based 2.5DICs”, *IEEE/ECTC Proceedings*, May 2020, pp. 1180–1185.
73. Hsiao, Y., C. Hsu, Y. Lin, and C. Chien, “Reliability and Benchmark of 2.5D Non-molding and Molding Technologies”, *IEEE/ECTC Proceedings*, May 2019, pp. 461–466.
74. Pares, G., J. Michel, E. Deschaseaux, P. Ferris, A. Serhan, and A. Giry, “Highly Compact RF Transceiver Module using High Resistive Silicon Interposer with Embedded Inductors and Heterogeneous Dies Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 1279–1286.
75. Okamoto, D., Y. Shibasaki, D. Shibata, and T. Hanada, F. Liu, M. Kathaperumal, and R. Tummala, “Fabrication and Reliability Demonstration of 3  $\mu\text{m}$  Diameter Photo Vias at 15  $\mu\text{m}$  Pitch in Thin Photosensitive Dielectric Dry Film for 2.5 D Glass Interposer Applications”, *IEEE/ECTC Proceedings*, May 2019, pp. 2112–2116.
76. Ravichandran, S., S. Yamada, G. Park, H. Chen, T. Shi, C. Buch, F. Liu, V. Smet, V. Sundaram, and R. Tummala, “2.5D Glass Panel Embedded (GPE) Packages with Better I/O Density,

- Performance, Cost and Reliability than Current Silicon Interposers and High-Density Fan-Out Packages”, *IEEE/ECTC Proceedings*, May 2018, pp. 625–630.
- 77. Wang, J., Y. Niu, S. Park, A. Yatskov, “Modeling and design of 2.5D package with mitigated warpage and enhanced thermo-mechanical reliability”, *IEEE/ECTC Proceedings*, May 2018, pp. 2471–2477.
  - 78. Okamoto, D., Y. Shibasaki, D. Shibata, T. Hanada, F. Liu, V. Sundaram, R. Tummala, “An Advanced Photosensitive Dielectric Material for High-Density RDL with Ultra-Small Photo-Vias and Ultra-Fine Line/Space in 2.5D Interposers and Fan-Out Packages.
  - 79. Cai1, H., S. Ma, J. Zhang, W. Xiang, W. Wang, Y. Jin, J. Chen, L. Hu, and S. He, “Thermal and Electrical characterization of TSV interposer embedded with Microchannel for 2.5D integration of GaN RF devices”, *IEEE/ECTC Proceedings*, May 2018, pp. 2150–2156.
  - 80. Hong, J., K. Choi, D. Oh, S. Shao, H. Wang, Y. Niu, and V. Pham, “Design Guideline of 2.5D Package with Emphasis on Warpage Control and Thermal Management”, *IEEE/ECTC Proceedings*, May 2018, pp. 682–692.
  - 81. Nair, C., B. DeProspo, H. Hichri, M. Arendt, F. Liu, V. Sundaram, and R. Tummala, “Reliability Studies of Excimer Laser-Ablated Microvias Below 5 Micron Diameter in Dry Film Polymer Dielectrics for Next Generation, Panel-Scale 2.5D Interposer RDL”, *IEEE/ECTC Proceedings*, May 2018, pp. 1005–1009.
  - 82. Lai, C., H. Li, S. Peng, T. Lu, and S. Chen, “Warpage Study of Large 2.5D IC Chip Module”, *IEEE/ECTC Proceedings*, May 2017, pp. 1263–1268.
  - 83. Shih, M., C. Hsu, Y. Chang, K. Chen, I. Hu, T. Lee, D. Tarng, and C. Hung, “Warpage Characterization of Glass Interposer Package Development”, *IEEE/ECTC Proceedings*, May 2017, pp. 1392–1397.
  - 84. Agrawal, A., S. Huang, G. Gao, L. Wang, J. DeLaCruz, and L. Mirkarimi, “Thermal and Electrical Performance of Direct Bond Interconnect Technology for 2.5D and 3D integrated Circuits”, *IEEE/ECTC Proceedings*, May 2017, pp. 989–998.
  - 85. Choi, S., J. Park, D. Jung, J. Kim, H. Kim, K. Kim, “Signal Integrity Analysis of Silicon/Glass/Organic Interposers for 2.5D/3D Interconnects”, *IEEE/ECTC Proceedings*, May 2017, pp. 2139–2144.
  - 86. Wang, X., Q. Ren, and M. Kawano, “Yield Improvement of Silicon Trench Isolation for One-Step TSV”, *IEEE/EPTC Proceedings*, December 2020, pp. 22–26.
  - 87. Ren, Q., W. Loh, S. Neo, and K. Chui, “Temporary Bonding and De-bonding Process for 2.5D/3D Applications”, *IEEE/EPTC Proceedings*, December 2020, pp. 27–31.
  - 88. Chuan, P. and S. Tan, “Glass Substrate Interposer for TSV-integrated Surface Electrode Ion Trap”, pp. 262–265. *IEEE/EPTC Proceedings*, December 2020, pp. 262–265.
  - 89. Loh, W. and K. Chui, “Wafer Warpage Evaluation of Through Si Interposer (TSI) with Different Temporary Bonding Materials”, *IEEE/EPTC Proceedings*, December 2020, pp. 268–272.
  - 90. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.
  - 91. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
  - 92. Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill, New York, 2016.
  - 93. Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, McGraw-Hill, New York, 2013.
  - 94. Lau, J. H., *Reliability of RoHS compliant 2D & 3D IC Interconnects*, McGraw-Hill, New York, 2011.
  - 95. Lau, J. H., “Overview and Outlook of 3D IC Packaging, 3D IC Integration, and 3D Si Integration”, *ASME Transactions, Journal of Electronic Packaging*, December 2014, Vol. 136, Issue 4, pp. 1–15.
  - 96. Lau, J. H., “Overview and Outlook of TSV and 3D Integrations”, *Journal of Microelectronics International*, Vol. 28, No. 2, 2011, pp. 8–22.
  - 97. Lau, J. H., “Critical Issues of 3D IC Integrations”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging, First Quarter Issue*, 2010, pp. 35–43.
  - 98. Lau, J. H., “Design and Process of 3D MEMS Packaging”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging, First Quarter Issue*, 2010, pp. 10–15.

99. Lau, J. H., Lee, R., Yuen, M., and Chan, P., “3D LED and IC Wafer Level Packaging”, *Journal of Microelectronics International*, Vol. 27, Issue 2, 2010, pp. 98–105.
100. Lau, J. H., “3D IC Integration with a Passive Interposer”, *Proceedings of SMTA International Conference*, Chicago, IL, September 2014, pp. 11–19.
101. Lau, J. H., “The Role and Future of 2.5D IC Integration”, *IPC APEX EXPO Proceedings*, Las Vegas, NE, March 2014, pp. 1–14.
102. Chen, J., J. H. Lau, T. Hsu, C. Chen, P. Tzeng, P. Chang, C. Chien, Y. Chang, S. Chen, Y. Hsin, S. Liao, C. Lin, T. Ku, and M. Kao, “Challenges of Cu CMP of TSVs and RDLS Fabricated from the Backside of a Thin Wafer”, *IEEE International 3D Systems Integration Conference*, San Francisco, CA, October 2013, pp. 1–5.
103. Lau, J. H., H. C. Chien, S. T. Wu, Y. L. Chao, W. C. Lo, and M. J. Kao, “Thin-Wafer Handling with a Heat-Spreader Wafer for 2.5D/3D IC Integration”, *Proceedings of the 46<sup>th</sup> IMAPS International Symposium on Microelectronics*, Orlando, FL, October 2013, pp. 389–396.
104. Hung, J. F., J. H. Lau, P. Chen, S. Wu, S. Hung, S. Lai, M. Li, S. Sheu, Z. Lin, C. Lin, W. Lo, and M. Kao, “Electrical Performance of Through-Silicon Vias (TSVs) for High-Frequency 3D IC Integration Applications”, *Proceedings of the 45<sup>th</sup> IMAPS International Symposium on Microelectronics*, September 2012, pp. 1221–1228.
105. Lau, J. H., “Supply Chains for 3D IC Integration Manufacturing”, *Proceedings of IEEE Electronic Materials and Packaging Conference*, December 2012, pp. 72–78.
106. Lau, J. H., S. T. Wu, and H. C. Chien, “Thermal-Mechanical Responses of 3D IC Integration with a Passive TSV Interposer”, *IEEE EuroSime Proceedings, Chapter 5: Reliability Modeling*, Lisbon, Portugal, April 2012, pp. 1/8 – 8/8.
107. Lau, J. H., “The Most Cost-Effective Integrator (TSV Interposer) for 3D IC Integration System-in-Package (SiP)”, *ASME Paper no. InterPACK2011-52189*, Portland, OR, July 2011.
108. Lau, J. H., and X. Zhang, “Effects of TSV Interposer on the Reliability of 3D IC Integration SiP”, *ASME Paper no. InterPACK2011-52205*, Portland, OR, July 2011.
109. Lau, J. H., “State-of-the-art and Trends in Through-Silicon Via (TSV) and 3D Integrations”, *ASME Paper no. IMECE2010-37783*.
110. Lau, J. H., Y. S. Chan, S. W. R. Lee, “Thermal-Enhanced and Cost-Effective 3D IC Integration with TSV Interposers for High-Performance Applications”, *ASME Paper no. IMECE2010-40975*.
111. Lau, J. H., “Evolution and Outlook of TSV and 3D IC/Si Integration” *IEEE/EPTC Proceedings*, Singapore, December 2010, pp. 560–570.

# Chapter 7

## 3D IC Integration and 3D IC Packaging

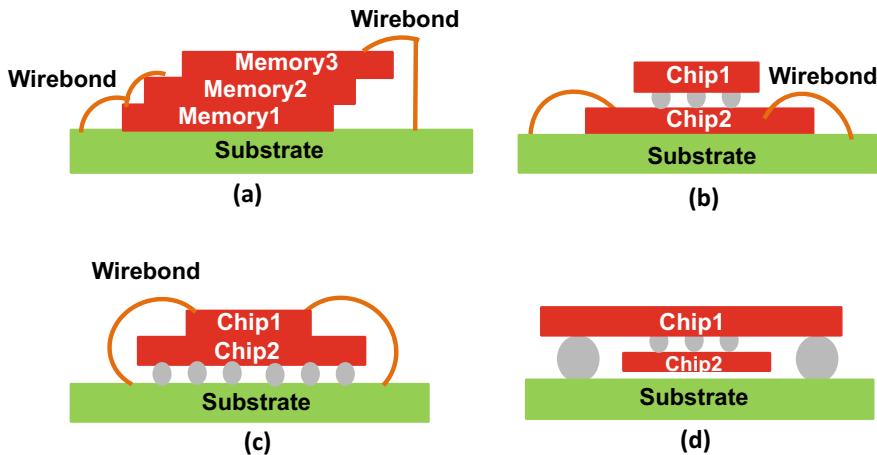


### 7.1 Introduction

3D integration [1–70] consists of at least 3D IC integration and 3D IC packaging. First of all, by definition, both 3D IC integration and 3D IC packaging are for stacking the chips in the vertical direction. The key difference between 3D IC integration and 3D IC packaging, in this book, is 3D IC integration uses through-silicon vias (TSVs) [36–38] but 3D IC packaging does not.

### 7.2 3D IC Packaging

There are many different kinds of 3D IC packaging. Figures 7.1 and 7.2 schematically show just a few. Figure 7.1a shows the memory chips stacking with wirebonds. Figure 7.1b shows the two chips are face-to-face solder bumped flip chip and then with wire bonds to the next level of interconnect. Figure 7.1c shows the two chips are back-to-back bonding; the bottom chip is solder bumped flip chip to the substrate and the top chip is with wire bonds to the substrate. Figure 7.1d shows the two chips are face-to-face solder bumped bonding and the top chip is with solder ball to the substrate. Figure 7.2a shows a PoP (package-on-package) for the application chipsets (application processor + memory). It can be seen that in the bottom package the application processor is solder bumped flip chip on a build-up package substrate with underfill. The top package is used to house the memory, which is usually cross stacked and wire bonded on a coreless organic substrate. Figure 7.2b shows another kind of PoP formation for the application chipset. In the bottom package, the application processor is fanned out with RDLs (redistribution-layers) and then solder balled on a printed circuit board (PCB). The wafer bumping for flip chip, build-up package substrate, and underfill are eliminated. The upper package remains the same which is to house the memory chips.



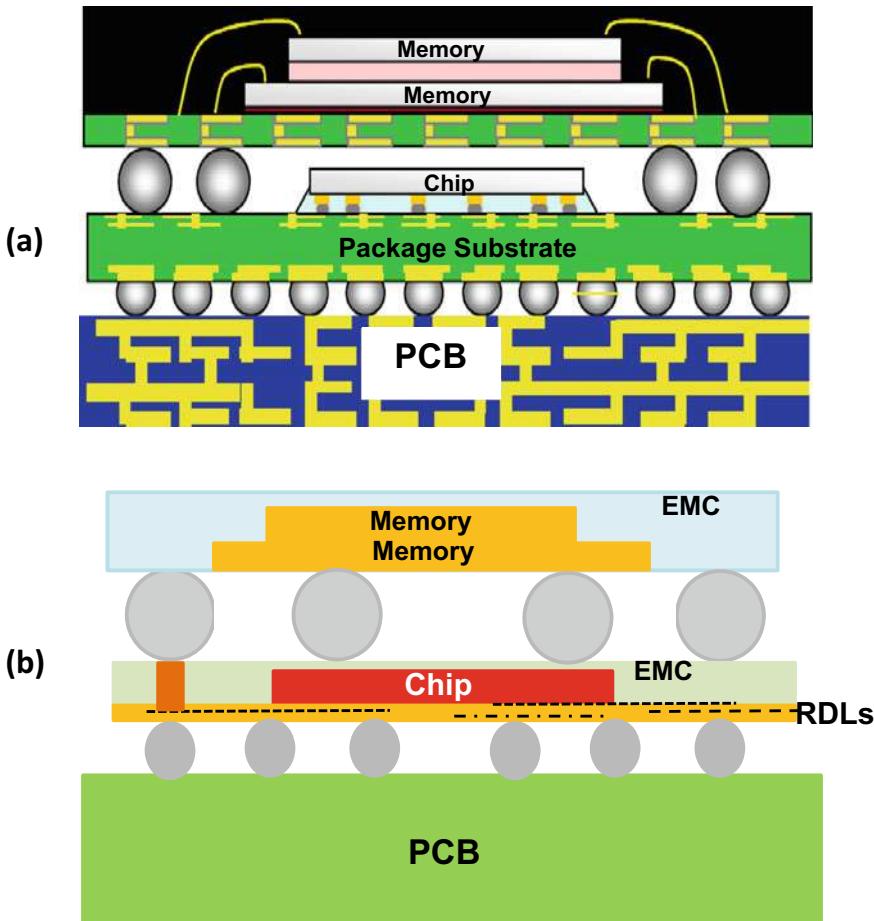
**Fig. 7.1** 3D IC packaging. **a** Memory chips stacked with wirebonds. **b** Face-to-face bonding with wirebonds to the substrate. **c** Back-to-back bonding with wirebonds to the substrate. **d** Face-to-face bonding with solder bump/ball to substrate

### 7.2.1 3D IC Packaging—Memory Stack with Wire Bonding

Figures 7.3, 7.4 and 7.5 show different kinds 3D memory stacks with wire bonding technology. Today, more than 50% of the wires have been shifted from Au to Cu or even some Ag materials. In wire bonding technology all the wires are bonded along the peripherals (one to two rows) of the chip as shown in Figs. 7.3, 7.4 and 7.5. Figure 7.6 shows the cross section of an eight-stack flash manufactured by Samsung for Apple's iPhone. The package, including substrate is 0.93 mm-thick and the chip-stack is 670  $\mu\text{m}$ -high. The chip thicknesses vary from 55 to 70  $\mu\text{m}$ , with the thickest chip at the bottom. Figures 7.7 and 7.8 show Samsung's solid state drives (SSD). It can be seen that 16, 48-layer V-NAND 3D flash memory chips are stacked by wire bonding technology. The thickness of each chip is only 40  $\mu\text{m}$ . The stack of chips is on a coreless organic package substrate with area array solder balls to be attached on a PCB.

### 7.2.2 3D IC Packaging—Face-to-Face Bonding with Wire Bonding to Substrate

Figure 7.9 shows Sony's PlayStation CXD53135GG. It can be seen that it is a 5-chip stack with both wire bonds and solder bumps flip chip. The double data rate type-2 (DDR2) SDRAM, spacer die, and DDR2 SDRAM are stacked with wire bonds. However, the 1 GB wide input/output (I/O) synchronous dynamic random access



**Fig. 7.2** 3D IC packaging. **a** PoP with flip chip technology. **b** PoP with fan-out packaging technology

memory (SDRAM) and the processor are face-to-face solder bumped flip chip and then wire bonding from the processor to the next level interconnect.

Figure 7.10 shows Sony's backside illuminated CMOS image sensor (BI-CIS) [1, 2]. The BI-CIS chip is face-to-face hybrid bonding (see Sect. 8.5.3) to the processor chip and then it is wire bonded from the processor chip to the next level interconnect.

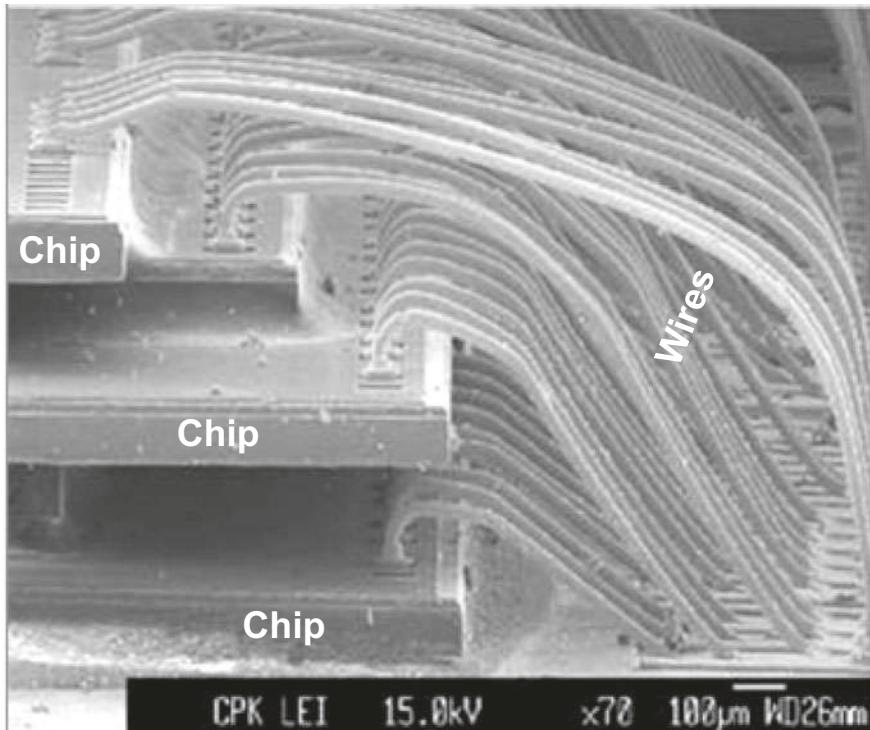


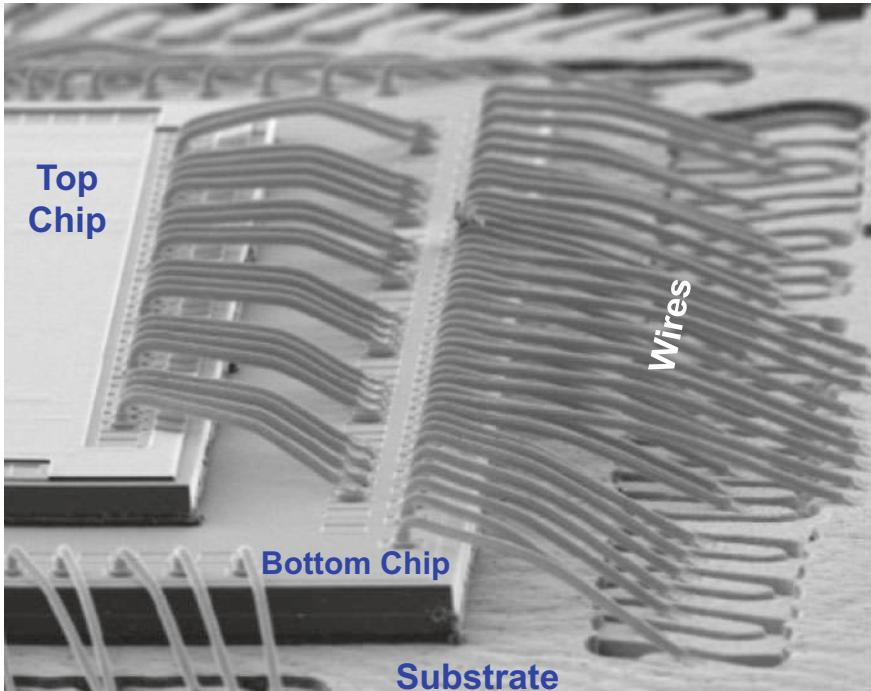
Fig. 7.3 Three-chip stacked with wire bonding

### 7.2.3 3D IC Packaging—Back-to-Back Bonding with Wire Bonding to Substrate

Figure 7.11 shows the modem chipset by Intel for the second most important chipset of the iPhone XR. It can be seen that the baseband application processor (AP) is solder bumped flip chip on a 3-layer embedded trace substrate (ETS). The DRAM is die attached on the backside of the AP and is wire bonded to the ETS. This is an example of back-to-back bonding with wire bonding to substrate.

### 7.2.4 3D IC Packaging—Face-to-Face Bonding with Solder Bump/Ball to Substrate

Figure 7.12 shows a face-to-face bonding with solder ball to the next level interconnect. It can be seen that the memory is bonded with C2 bump (Cu-pillar with AuSn solder cap) on the logic chip. Then, the logic chip is with SnAgCu solder ball attached to the substrate [3].



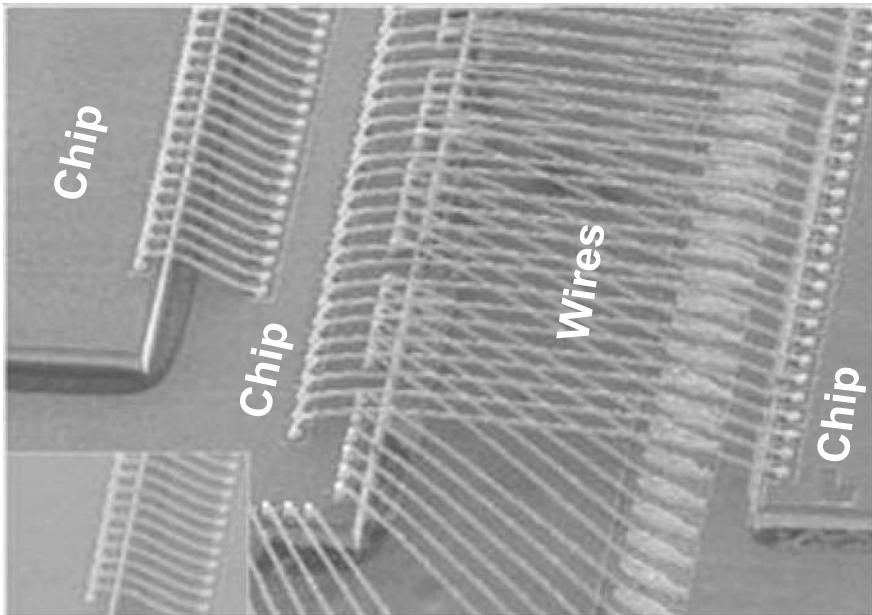
**Fig. 7.4** Two-chip stacked with wire bonding

Figure 7.13 shows a 3D IC packaging from Georgia Institute of Technology [4]. It can be seen that the chips are face-to-face bonded to the router chip with solder bumps from the chips and fan-out RDLs from the router chip. The signals are then connected to the solder bump/ball through the through-glass vias (TGVs).

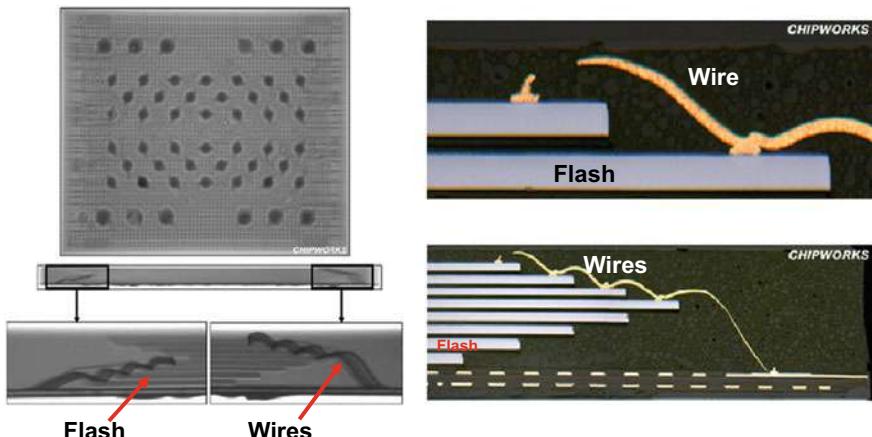
Figure 7.14 shows the chip-to-chip and face-to-face bonding from Fraunhofer [5]. It can be seen that the micro-electro-mechanical systems (MEMS) chip is face-to-face bonded to an ASIC chip. The signals can escape from the ASIC either by solder balls or wire bonds.

Figure 7.15 shows a face-to-face bonding with C4 bump to a substrate. It can be seen that [6] the application specific IC (ASIC) chip is face-to-face (with micro bump + solder cap) bonded to the field programmable gate array (FPGA). Then, the FPGA is C4 (controlled collapse chip connection) solder bumped to the package substrate.

Figure 7.16 shows Amkor's Double-POSSUM package [7]. It can be seen that the package is actually defined by two levels of nesting die. The three daughter dies are flip-chip attached to the larger mother die which is then attached to the largest grandma die. The grandma die is then flip-chip attached to the package substrate. The bumps between the daughter dies and the mother die are C2 bumps. C4 bumps



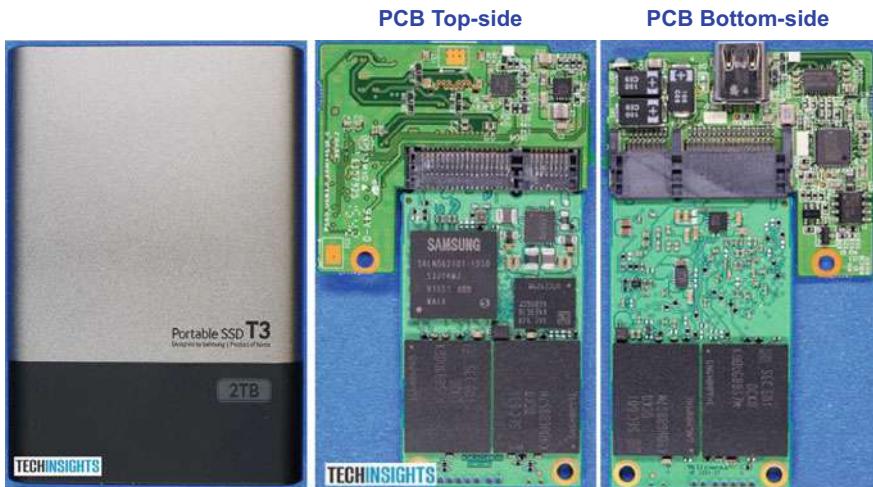
**Fig. 7.5** Chip stacked with two-row wire bonding



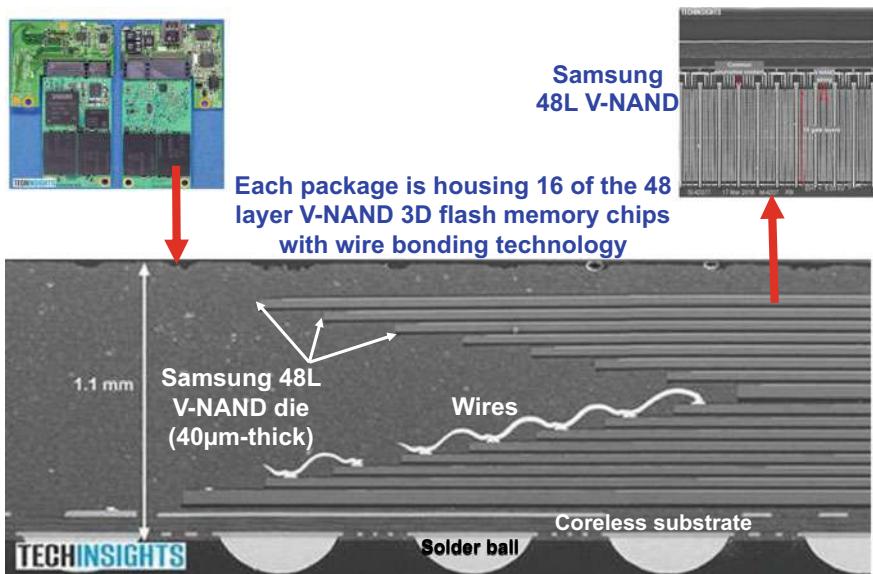
**Fig. 7.6** Eight flash memory chips stacked with wire bonding

are used between the mother die and grandma die, and between the grandma die and package substrate.

Figure 7.17 shows the top and cross-sectional views of a 3D embedded MEMS device and its paired controller die [8]. The portion of the functional MEMS and

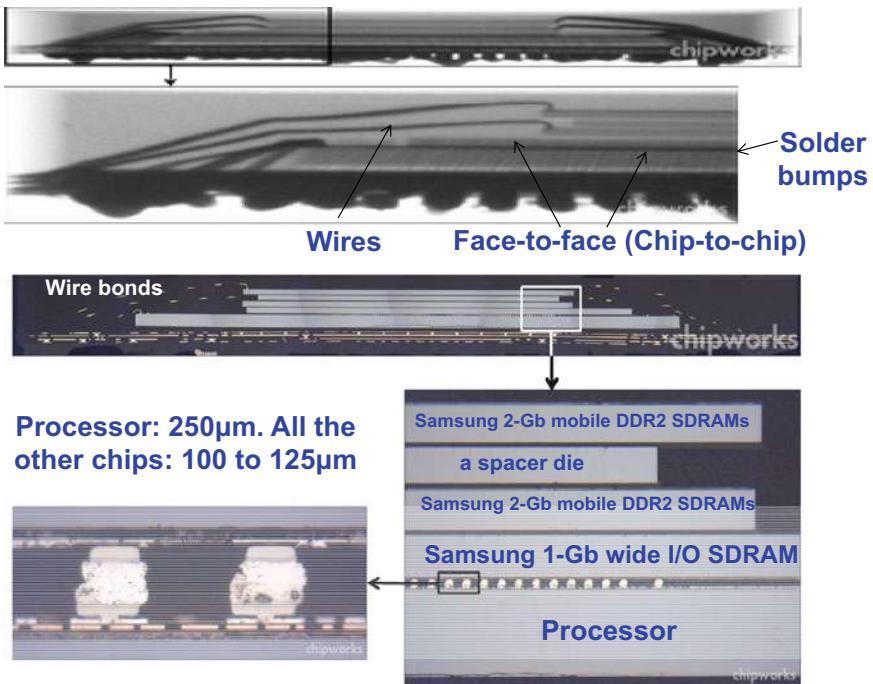


**Fig. 7.7** Samsung's SSD: top-side and bottom-side of the PCB

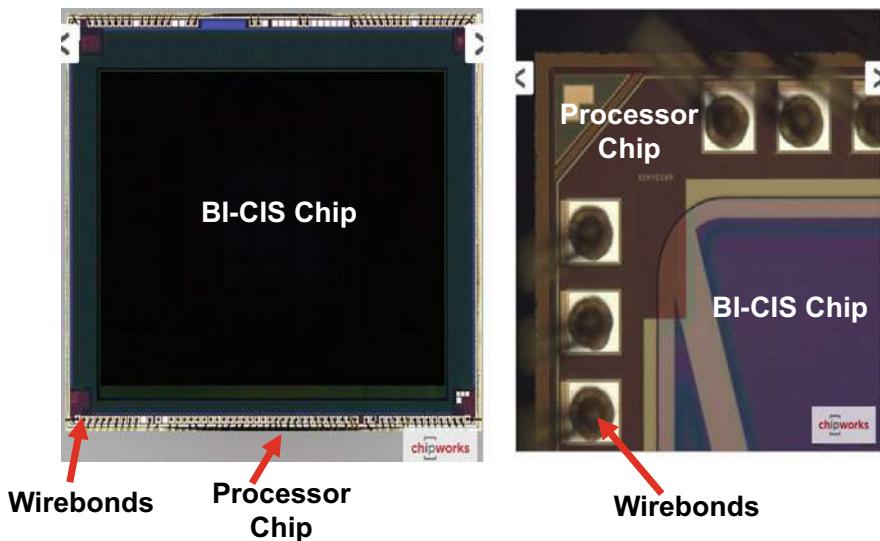


**Fig. 7.8** SEM image of the cross section of Samsung's SSD

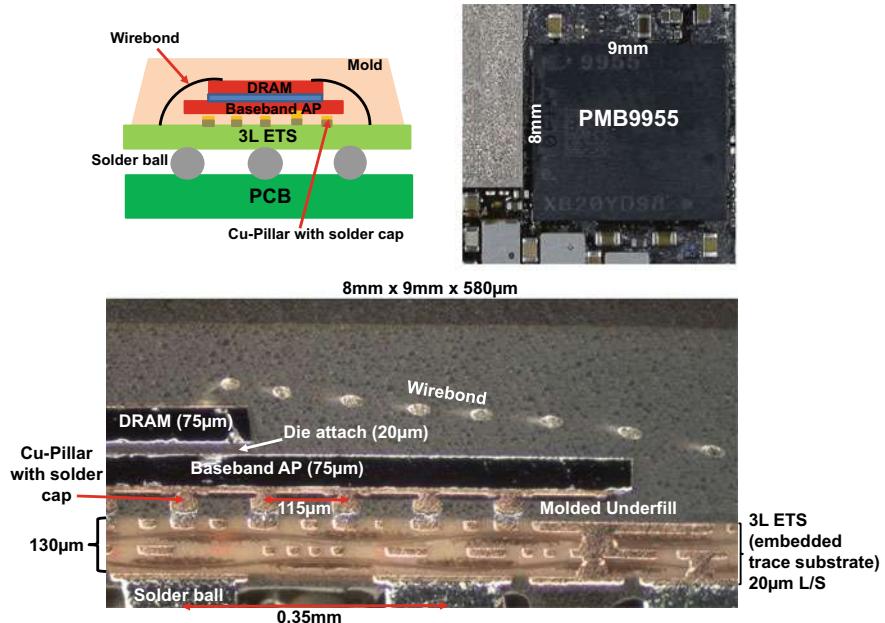
ASIC devices is approximately 600  $\mu$ m in thickness. Also, included is a near face-to-face chip-to-chip assembly with faces separated by only the solder bumps (from flip chip B) and a single layer RDL (fan-out from chip A). The interconnection is from the PCB, solder balls, through package via (TPV), RDLs, and to the solder bumps and chips.



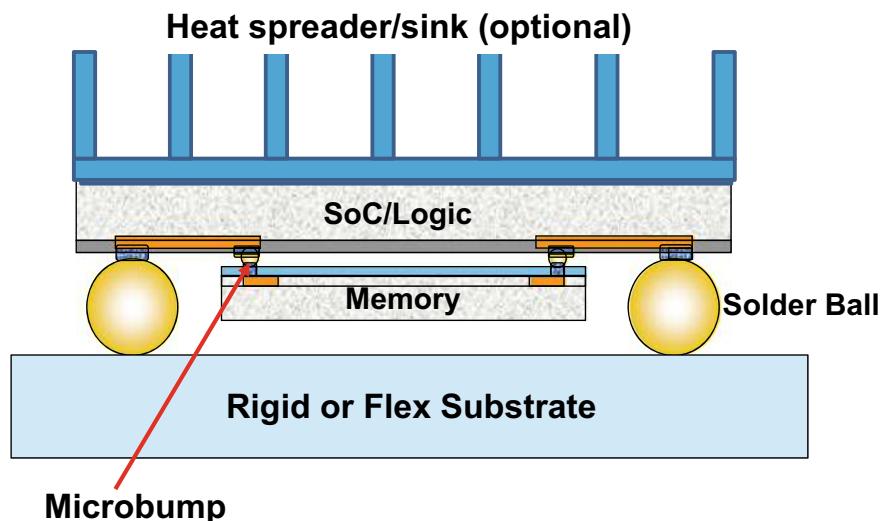
**Fig. 7.9** Sony's 5-chip stacked (face-to-face with wirebonds to the next level interconnect)



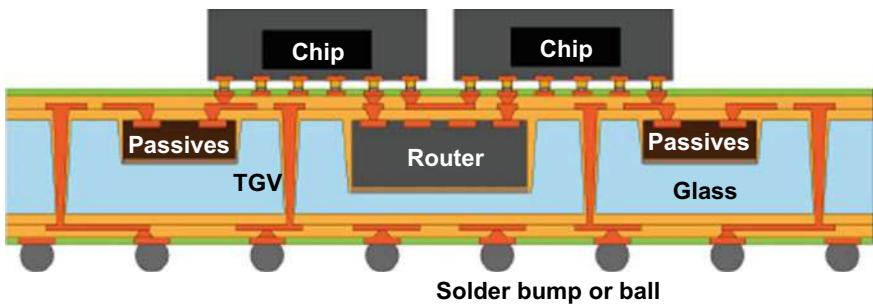
**Fig. 7.10** Sony's face-to-face bonding with wirebonds to the next level interconnect [1]



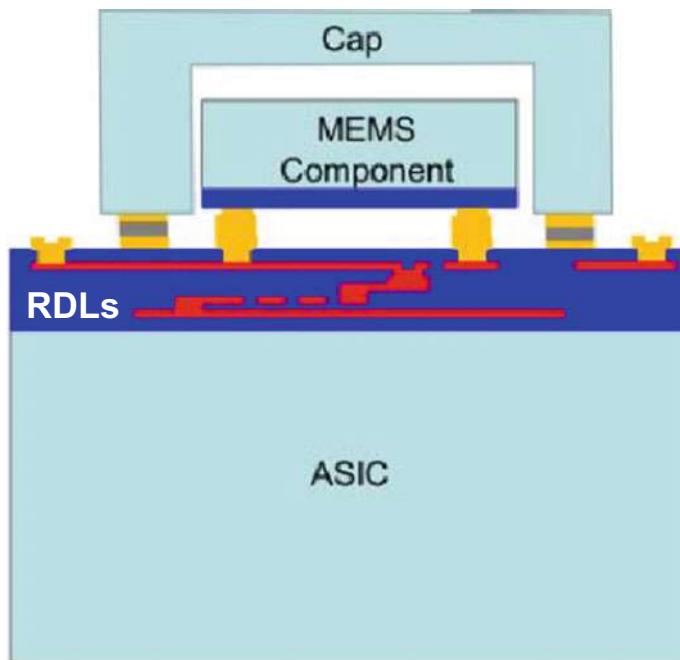
**Fig. 7.11** Intel's back-to-back bonding with wirebonds to the ETS substrate



**Fig. 7.12** IME's face-to-face bonding with solder ball to substrate



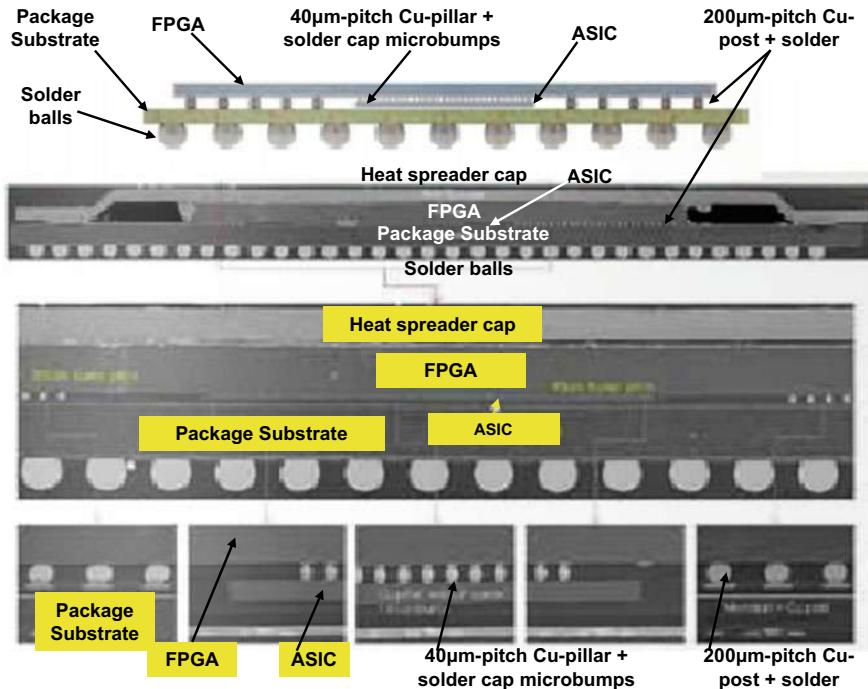
**Fig. 7.13** GIT's face-to-face bonding with TMV and solder ball to the next level of interconnect [4]



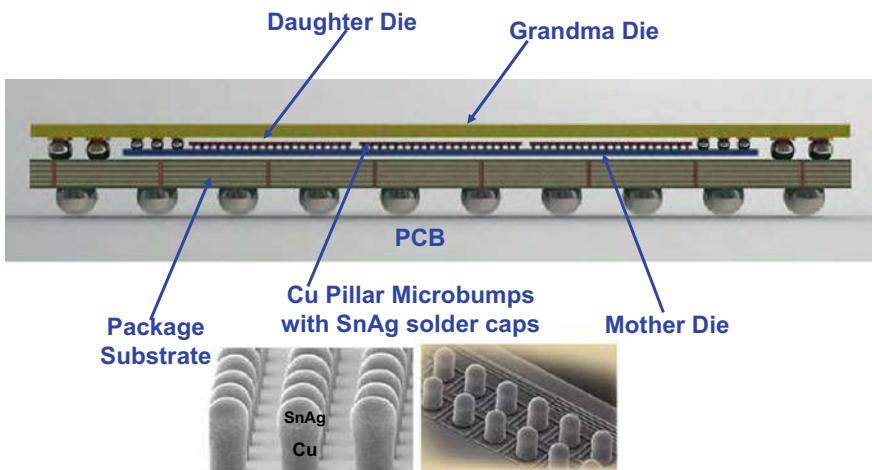
**Fig. 7.14** IZM's face-to-face bonding with either wirebond or solder ball from the ASIC to the next level of interconnect [5]

### 7.2.5 3D IC Packaging—Face-to-Back

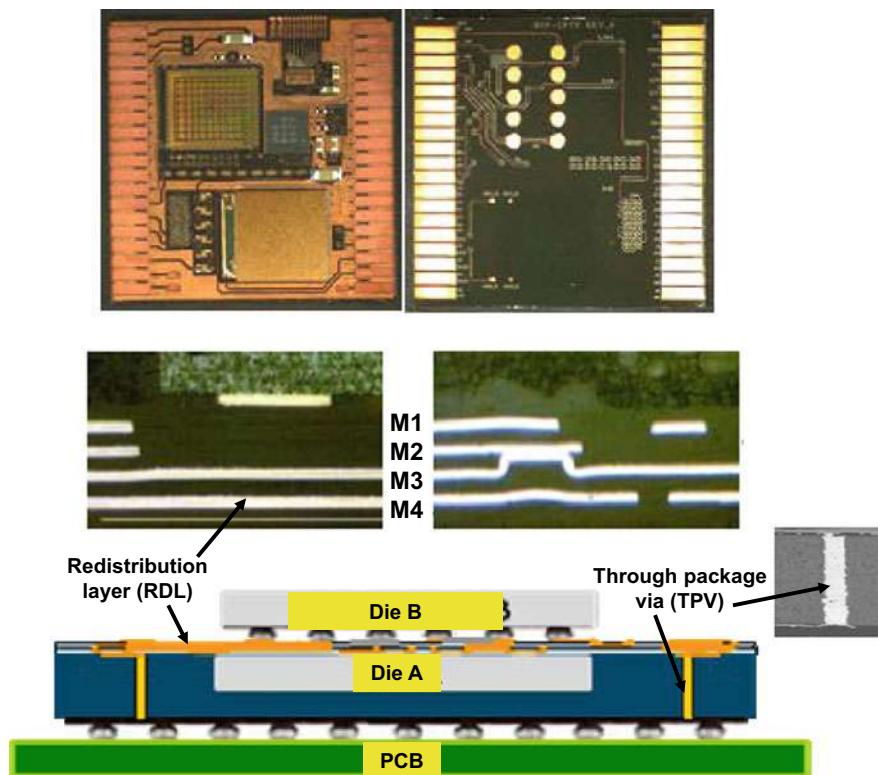
Figure 7.18 shows a 3D fan-out wafer level packaging [9, 10], which is housing Chip 1 and Chip 2 with over molded and RDLs. A solder bumped flip chip (Chip 3) which is face-down attached to the back-side of the fan-out package of Chip 1 and Chip 2.



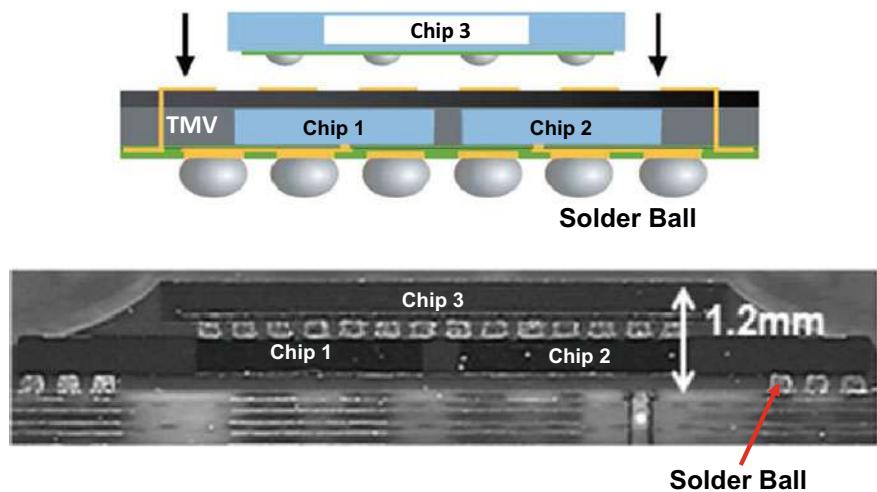
**Fig. 7.15** Face (ASIC)-to-face (FPGA) bonding with C2 bump to the package substrate



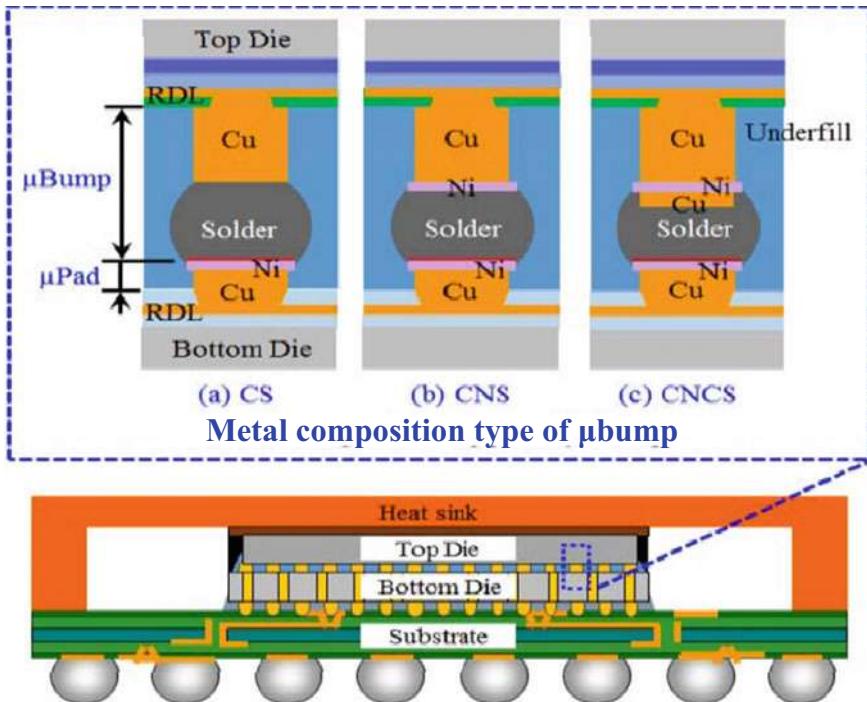
**Fig. 7.16** Amkor's Double-POSSUM package [7]



**Fig. 7.17** Face-to-face with TPV to solder ball to PCB



**Fig. 7.18** Face-to-back with TMV to solder ball on PCB [9]



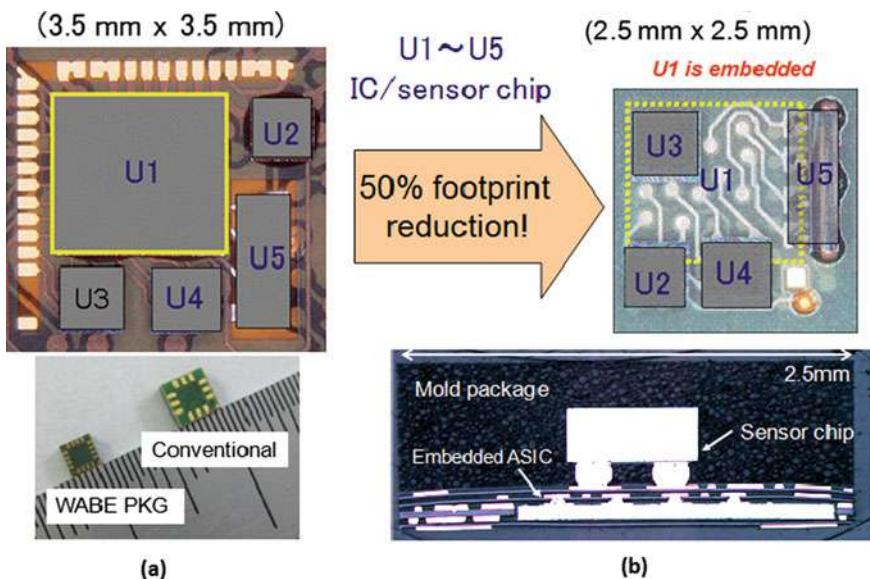
**Fig. 7.19** Face-to-back with fan-out RDLs, micro bump, and TMV to the next level interconnect [11]

The interconnection is from the PCB, solder balls, to the lower RDLs, Chip 1 and Chip 2, TMV, and upper RDLs and Chip 3.

Figure 7.19 shows a 3D IC package by SPIL [11]. It can be seen that the top chip is bonded to the backside of the bottom chip. The interconnect between the top chip and bottom chip is by fan-out RDLs, micro bumps (Cu-pillar + solder cap), and TMV. The interconnect between the chips and the package substrate is by C4 solder bumps.

### 7.2.6 3D IC Packaging—Embedded Chip (Face-to-Face) in SiP

Figure 7.20 shows the 3D SiP with embedded chip. It can be seen from Fig. 7.20a that for the conventional SiP there are 5 (IC and sensor) chips (U1 through U5) side-by-side on the substrate ( $3.5\text{ mm} \times 3.5\text{ mm}$ ). In Fig. 7.20b, it shows that the U1 chip is embedded into the flexible substrate ( $2.5\text{ mm} \times 2.5\text{ mm}$ ) by Fujikura's WABE (wafer and board level embedded package) technology [12]. The other 4 chips are on top of the substrate surface. (The sensor chip and the embedded IC are face-to-face). The package size has been reduced by 50%.



**Fig. 7.20** Embedded chip (face-to-face) in SiP

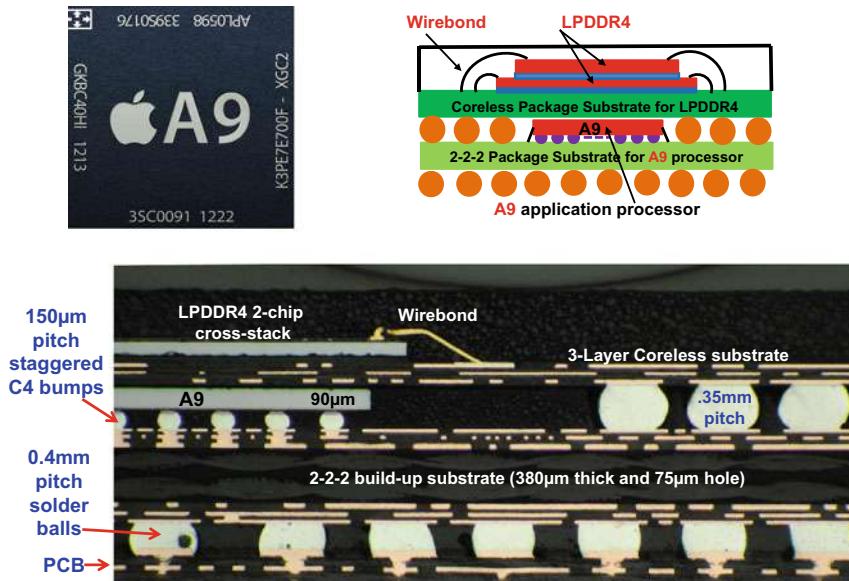
### 7.2.7 3D IC Packaging—PoP with Flip-Chip Technology

Figure 7.21 shows the cross section of an iPhone 6 Plus. It can be seen that the A9 application processor (AP) is housed in the bottom package of a package-on-package (PoP) format and the C4 solder bumped flip chip is mass reflowed on a 2-2-2 organic build-up package substrate with underfill.

High-bonding force thermocompression bonding (TCB) of the chips with C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate (Fig. 7.22) was first studied by Amkor [13] and has been used to assemble Qualcomm's SNAP-DRAGON application processor for Samsung's Galaxy smartphone as shown in Fig. 7.22. The substrate, MCeP (molded core embedded package) is provided by Shinko. The NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

Figure 7.23 shows NXP's 3D IC packaging [14]. It can be seen that the bottom package is housing the processor on a 4-layer ETS and the top package is housing the memory chips. The interconnects between the top and bottom packages are by double stacked solder balls and an TSV-less interposer.

Figure 7.24 shows Shinko's 3D IC packaging [15]. It can be seen that the bottom package is housing the memory chip while the top package is housing the ASIC chip. The interconnects between the top and bottom packages are by Shinko's Cu core solder balls.



**Fig. 7.21** PoP with flip chip technology (Apple)

### 7.2.8 3D IC Packaging—PoP with Fan-Out Technology

In order to get a lower profile package than the PoP shown in Figs. 7.21, 7.22, 7.23 and 7.24. Figure 7.25 shows the cross section scanning electron microscope (SEM) images of a 3D fan-out PoP [16] suggested by Statschippad. It consists of a bottom package which is a fan-out package (i.e., to replace the solder bumped flip chip package of Figs. 7.21, 7.22, 7.23, 7.24) and a top package which is a memory package. It can be seen that (a) the fan-out package is only 450  $\mu\text{m}$  thick, (b) the fan-out package is housing an application processor, (c) the top package is 520  $\mu\text{m}$  thick and it is housing the memory chips with wire bonding, and (d) the interconnection is from the PCB, solder balls, RDLs, to processor, and solder balls, RDL, to the memory chips.

Figure 7.26 shows the schematic and images of the PoP for the AP chipset in the iPhone. The PoP of the AP (A12) and the mobile DRAMs is fabricated using TSMC's InFO-WLP technology [17, 18]. Basically, the PoP platform used for all the APs (A10, A11, A12, A13, and A14) is very similar. However, because TSMC used 7 nm process technology to fabricate the A12, the chip dimensions are slightly smaller than that of A11 even though more functions, such as artificial intelligence, are included. In order to have a better electrical performance, there are a few integrated passive devices (IPDs), which are solder bumped flip chips at the bottom of the fan-out package as shown in Fig. 7.26. There are three RDLs and the minimum metal line width and spacing are 8  $\mu\text{m}$ . The pitch of the solder balls of the package is 0.35 mm. Recently, TSMC's 5 nm process technology has been used for A14. Figure 7.27

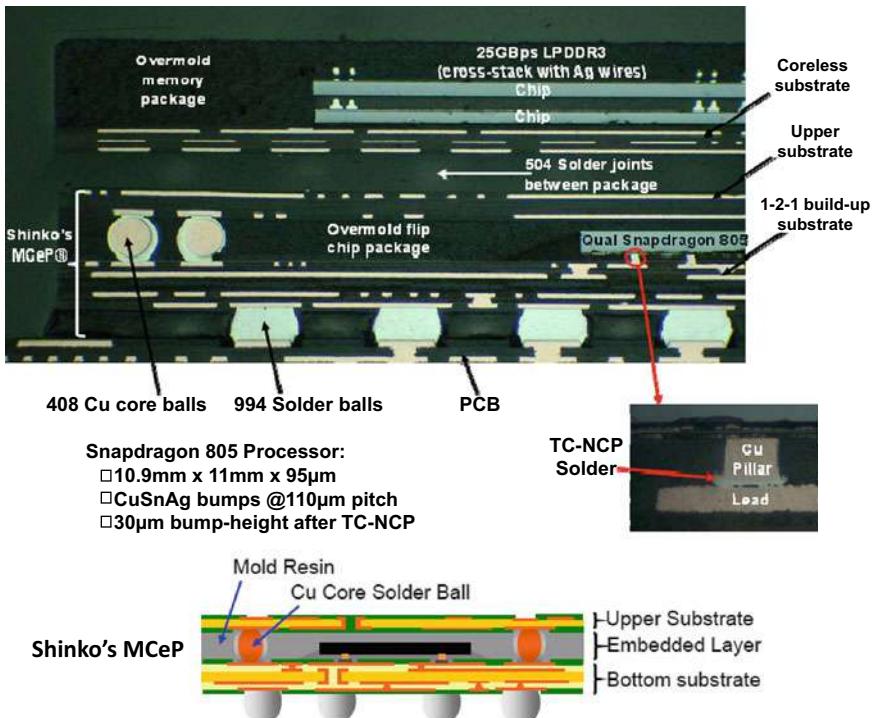


Fig. 7.22 PoP with flip chip technology (Qualcomm) [13]

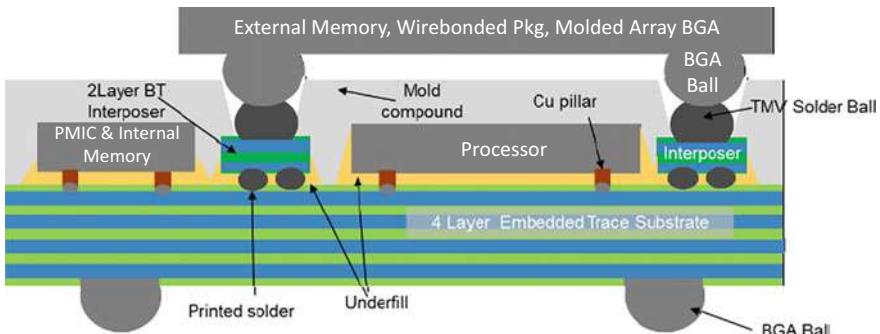
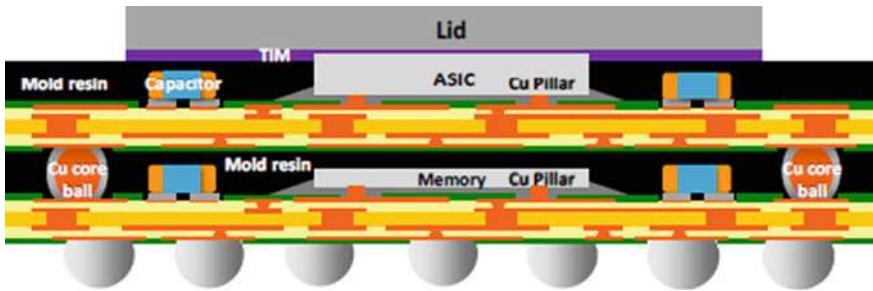


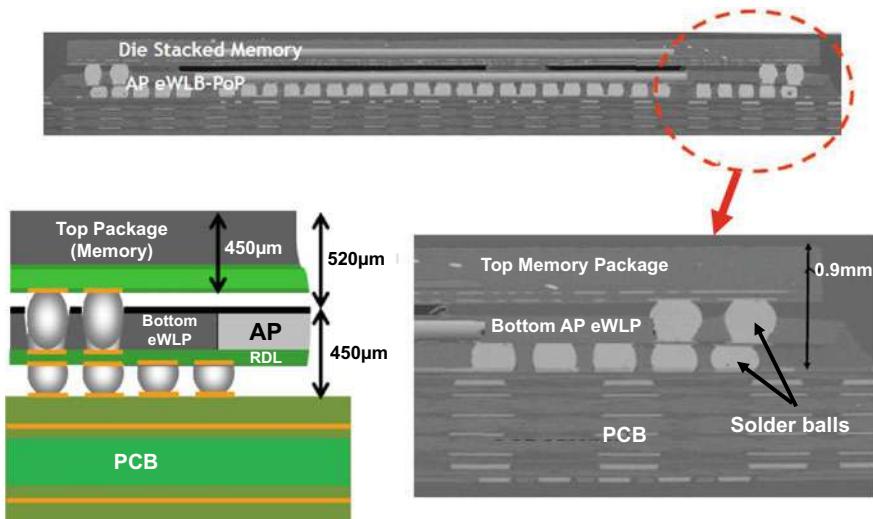
Fig. 7.23 PoP with flip chip technology (NXP)

shows another TSMC's PoP [19]. It can be seen that the bottom package is housing the chiplets with fan-out packaging technology. Between the bottom package and the top package (for the memory chips), there is a laminated TSV-less interposer.

Figure 7.28 shows Samsung's smartwatch in a PoP format. The upper package is housing the memory ePoP (embedded package-on-package) which consists of



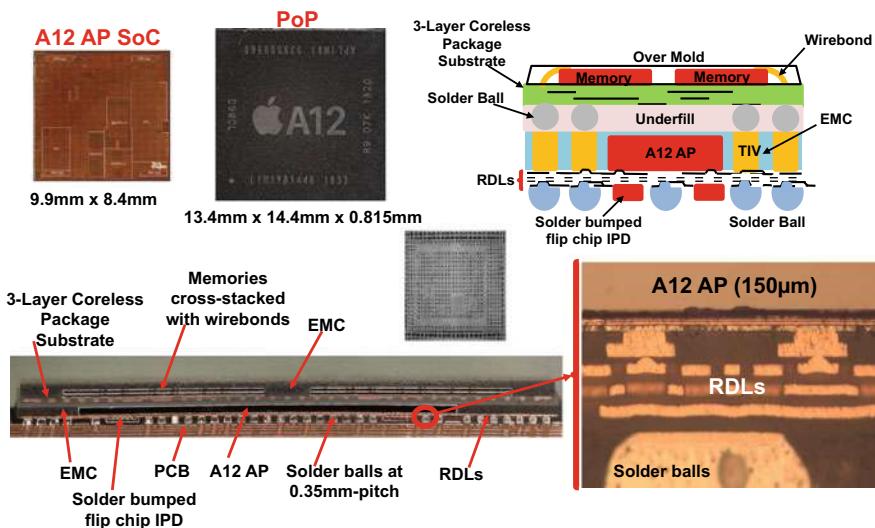
**Fig. 7.24** PoP with flip chip technology (Shinko) [15]



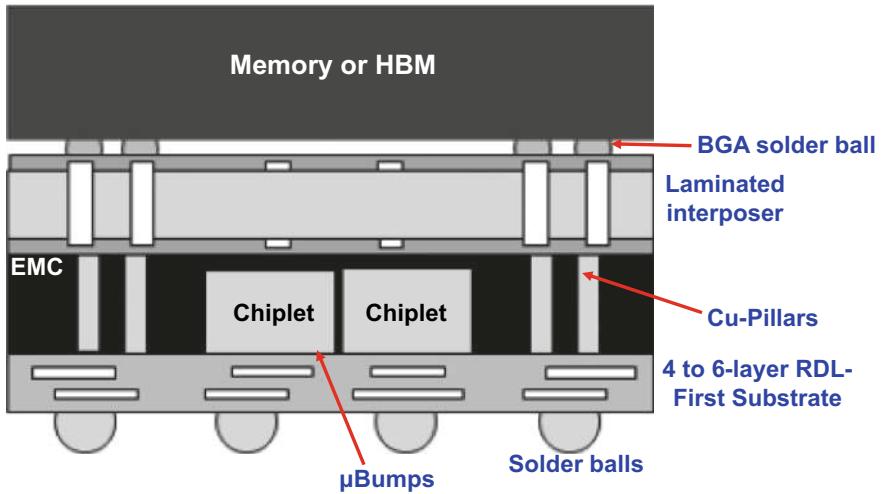
**Fig. 7.25** PoP with fan-out technology (Statschippac) [16]

2DRAM, 2NAND flash, and 1NAND-controller. These memories are wirebonding on a 3-layer coreless package substrate, as shown in Fig. 7.28. The dimensions of the upper package are  $8\text{ mm} \times 9.5\text{ mm} \times 1\text{ mm}$ . The bottom package is housing the AP and PMIC (power management IC) side-by-side by their fan-out panel level packaging technology. The chip size of the AP is  $5\text{ mm} \times 3\text{ mm}$  and that of the PMIC is  $3\text{ mm} \times 3\text{ mm}$ . The key process steps [20] are first make a cavity on a PCB, then place the chips on the cavity and laminate an EMC (epoxy molding compound). It is followed by attaching to a carrier, making the RDLs, and mounting the solder balls.

Unlike Figs. 7.25, 7.26, 7.27 and 7.28, which use fan-out with chip-first for the bottom package, IME use chip-last (or RDL-first) for the bottom package as shown in Fig. 7.29 [21]. It can be seen that there are microbumps between the processor and the RDL-first substrate. Also, unlike Figs. 7.27 and 7.28, there is not solder balls between the bottom package and the top package (for the memory chips).



**Fig. 7.26** PoP with fan-out technology (Apple/TSMC) [17]



**Fig. 7.27** PoP with fan-out technology (TSMC) [19]

### 7.2.9 Summary and Recommendation

Some important results and recommendation are summarized as follows.

- 3D IC packaging (without TSVs) is the playing ground of fabless design house and mainly manufactured by outsourced semiconductor assembly and test (OSAT).

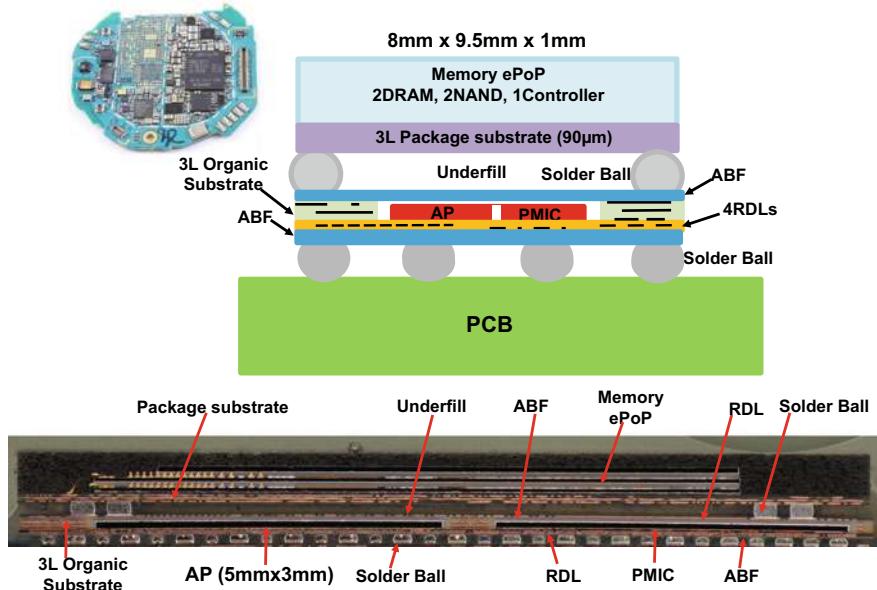


Fig. 7.28 PoP with fan-out technology (Samsung) [20]

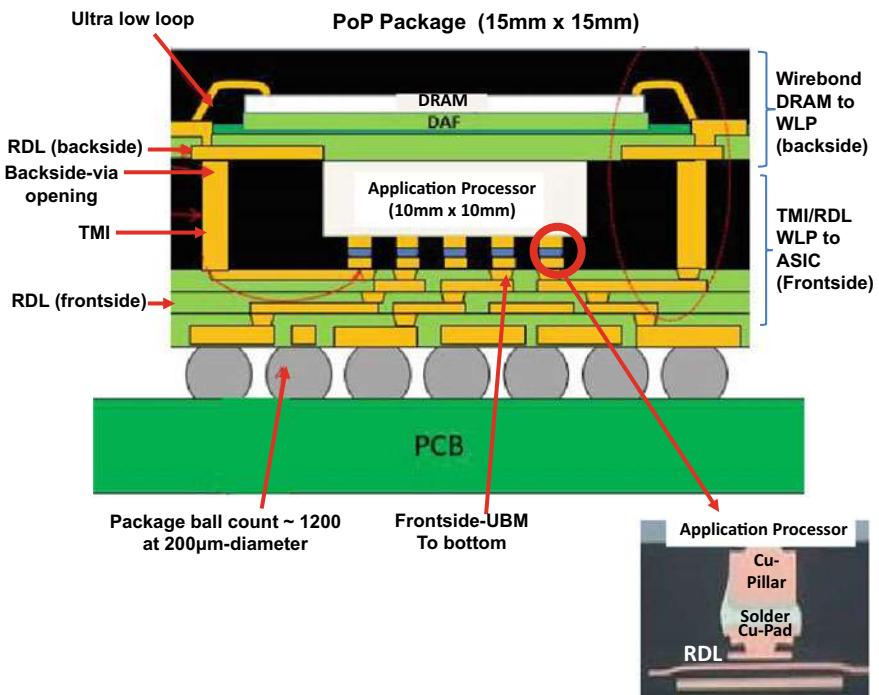


Fig. 7.29 PoP with fan-out (RDL-first) technology (IME) [21]

Some companies such as Intel, IBM, Samsung, Hynix, Micron, NXP, Infineon, etc. also manufacture their 3D IC packages. Recently, even Foundry such as TSMC and Samsung is making 3D IC package of their advanced nodes IC semiconductor.

- There are many kinds of 3D IC packaging (just use your imagination) and the sky is the limit.

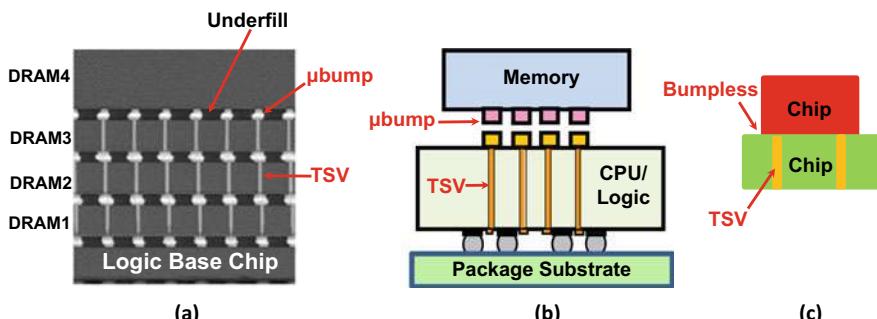
## 7.3 3D IC Integration

As mentioned earlier, 3D IC integration is for stacking chips in three dimensions with TSVs as schematically shown in Fig. 7.30. It can be seen from Fig. 7.30a that the DRAMs and base logic are stacked with TSVs, micro bumps, and underfill. Figure 7.30b shows that a high bandwidth memory is attached (with micro bumps) on a logic with TSVs. Figure 7.30c shows a bumpless chip is hybrid bonding on another bumpless chip with TSVs.

### 7.3.1 3D IC Integration—HBM Specifications

Figure 7.31 shows the high bandwidth memory (HBM), HBM2, and HBM2E. They work with SoC (system-on-chip) and are a must [22] for high-performance computing (HPC) applications driven by 5G (5th generation technology standard for broadband cellular networks) and AI (artificial intelligence) as shown in Fig. 7.32. In the whole world only Samsung and Hynix make the HBM chips/modules in HVM. Recently, Micron also wants to make it.

HBM uses less power but posts higher bandwidth than on double data rate 4 (DDR4) or graphics double data rate 5 (GDDR5) memory with smaller chips, making it appealing to graphics card vendors. HBM technology works by vertically stacking memory chips on top of one another. The memory chips are connected through TSVs



**Fig. 7.30** 3D IC integration. **a** Memory stacking with microbumps and TSVs. **b** Memory on logic with TSVs. **c** Bumpless hybrid bonding of chip-to-chip with TSVs

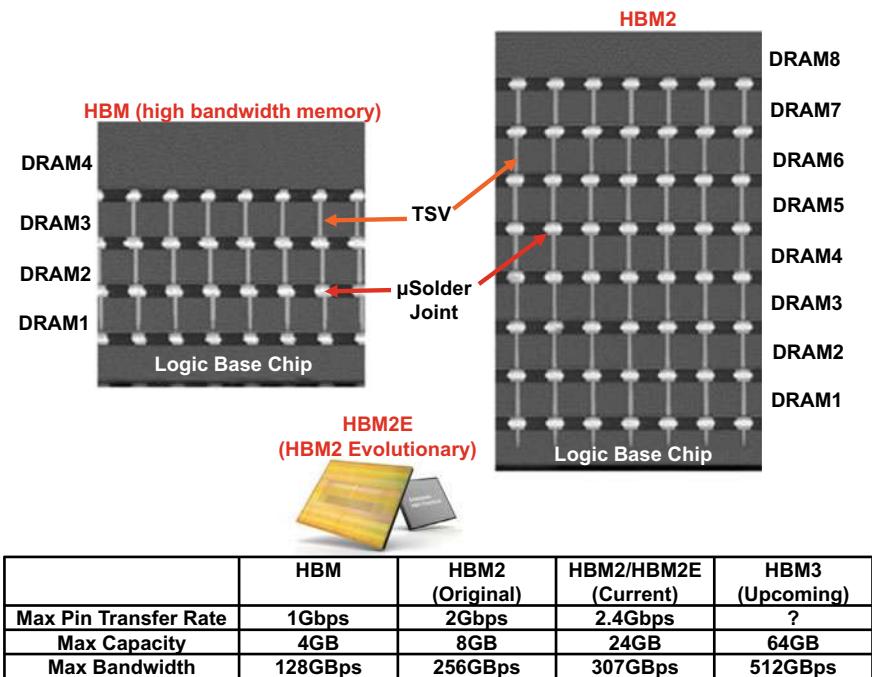


Fig. 7.31 HBM, HBM2, HBM2E, HBM3

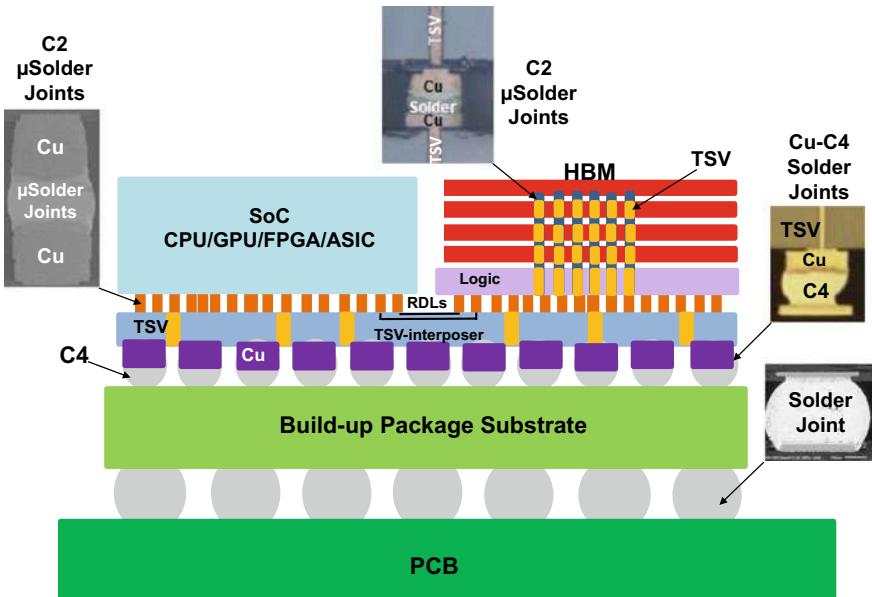


Fig. 7.32 The use of HBM in HPC

and microbumps. Additionally, with two 128-bit channels per die, HBM's memory bus is wider than that of other types of DRAM memory. The first HBM memory cube was produced by Hynix in 2013.

HBM2 debuted in 2016, and in December 2018 the JEDEC updated the HBM2 standard. The updated standard is commonly referred to as both HBM2 and HBM2E (to denote the deviation from the original HBM2 standard). The HBM2 standard allows up to 12 dies per stack for a maximum capacity of 24 GB. The standard also pegs memory bandwidth at 307 GBps, delivered across a 1,024-bit memory interface separated by 8 unique channels on each stack. Originally, the HBM2 standard called for up to eight dies in a stack (as with HBM) with an overall bandwidth of 256 GBps.

While not yet available, the HBM3 standard is currently in discussion. According to an Ars Technica report, HBM3 is expected to support up to 64 GB capacities and speeds up to 512 GBps. HBM3 will deliver more dies per stack and more than 2x the density per die with a similar power budget.

### 7.3.2 3D IC Integration—HBM Assembly

Both Samsung and Hynix use the high-bonding force TCB of the C2 (Cu-pillar + solder cap) bumped DRAMs with nonconductive film (NCF) (after singulation from the NCF laminated C2 bumped wafer), as shown in Fig. 7.33 to fabricate the 3D IC integration stack as shown in Fig. 7.34. This 3D memory cube is stacked one chip at

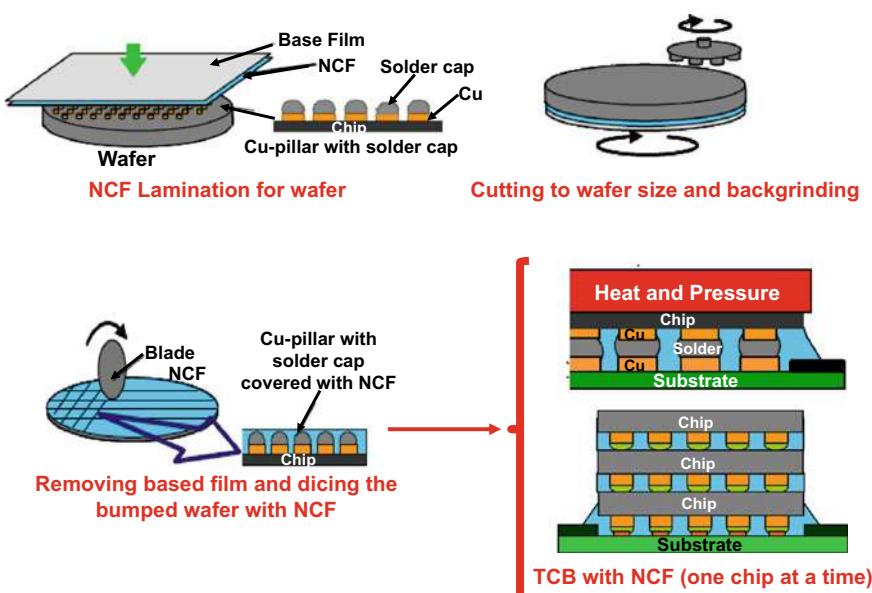
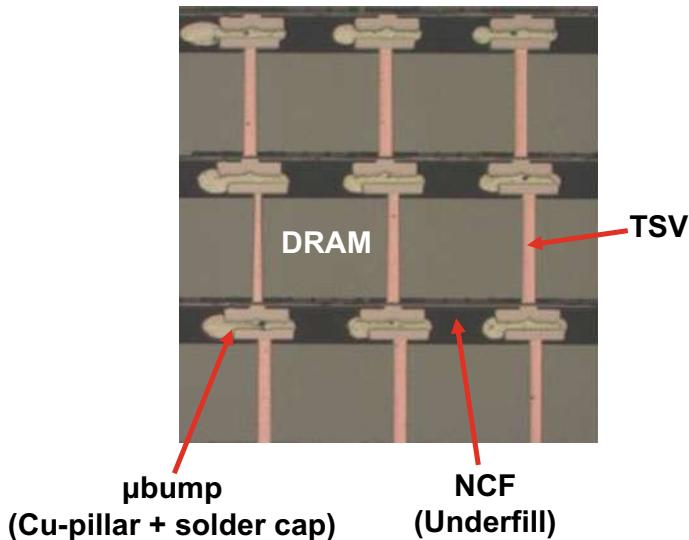


Fig. 7.33 HBM stacked with TCB-NCF



**Fig. 7.34** Image of HBM stacked with TCB-NCF

a time and each chip takes  $\sim 10$  s for the underfill film to gel, the solder to melt and solidify, and the film to cure. Throughput is a problem, however.

In order to resolve this problem, Toray [23, 24] proposed a collective bonding method, which is shown in Fig. 7.35. It can be seen that the C2 chip with NCF is pre-bond (bond force = 30 N, temperature = 150 °C, and time < 1 s) on a stage with temperature = 80 °C. For post-bond [first step (3 s): bond-force = 50 N and temperature = 220–260 °C, second step (7 s): bond-force = 70 N and temperature = 280 °C] on a stage temperature = 80 °C. Therefore, instead of using 40 s in stacking up four chips by the conventional method, it only takes less than 14 s by the collective TCB method. Some images of the cross section of the proposed collective bonding method are shown in 7.35. Reasonable good joints are achieved with optimized conditions.

### 7.3.3 3D IC Integration—Chip-on-Chip with TSVs

Figure 7.36 shows Sony's ISX014 stacked camera sensor [25]. It can be seen that the backside illuminated CMOS image sensor (BI-CIS) chip is on top of the processor chip and the interconnects between these chip are through the TSVs along the edges of the BI-CIS chip. The signals are wire bonded from the edges of the processor chip as shown in Fig. 7.36.

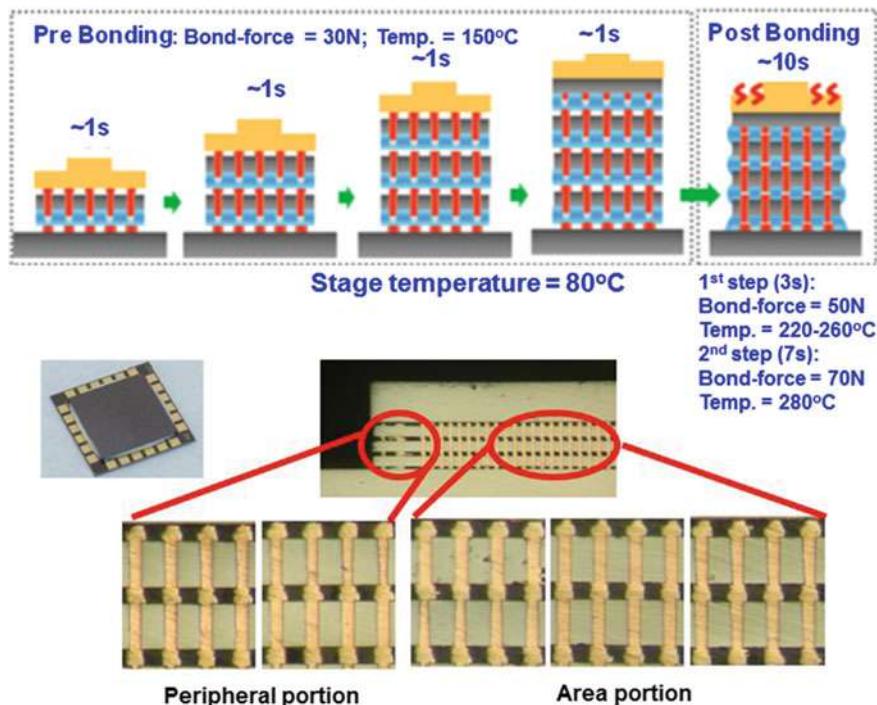
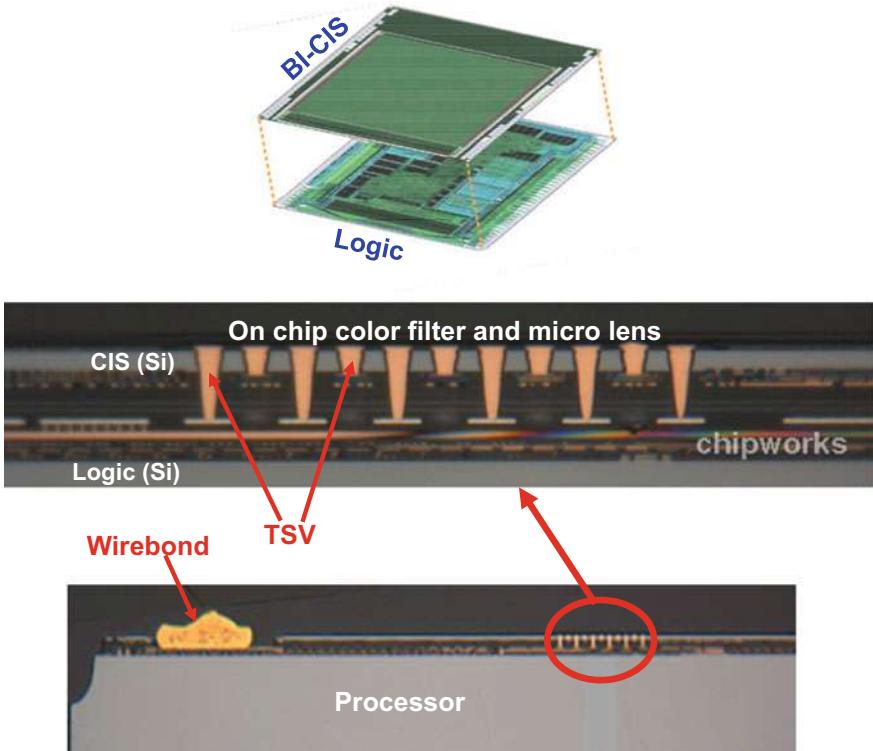


Fig. 7.35 Toray's collective bonding method for HBM [23]

Excited by the Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS), UCSB and AMD [26] proposed a future very high-performance system shown in Fig. 7.37. This system comprises a central processing unit (CPU) chiplet and several graphic processing unit (GPU) chiplets, as well as HBMs on an active TSV-interposer (i.e., a TSV-interposer with CMOS devices).

During 2020 IEEE Hot Chips 32 Symposium (HCS), Samsung announced their 3D IC integration technology, eXtended-Cube (X-Cube), as shown in Fig. 7.38 for high-performance applications. Leveraging Samsung's through-silicon via (TSV) technology, X-Cube enables significant leaps in speed and power efficiency to help address the rigorous performance demands of next-generation applications including HPC driven by 5G and AI, as well as mobile and wearable. It can be seen from Fig. 7.38 that the top chip (usually is a high bandwidth memory) is on top of a logic with TSV (or called an active TSV-interposer). The interconnects between these two chips are C2 microbumps.

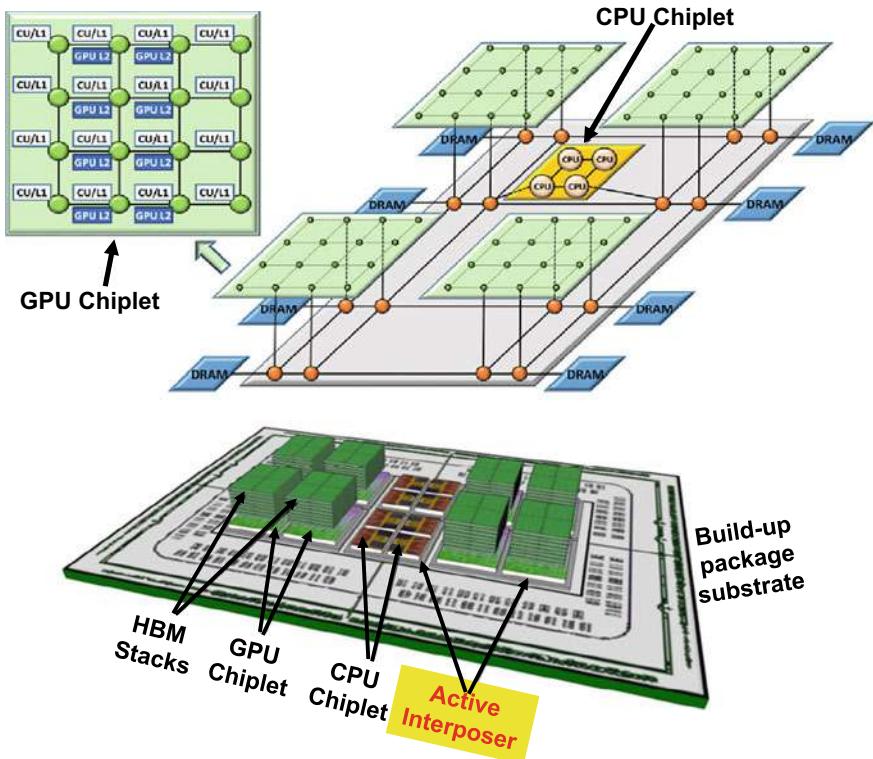
Figure 7.39 shows some active TSV-interposers, such as those proposed by Intel. Figure 7.39a shows the FOVEROS technology (announced in December 2018). It can be seen that the TSV interposer is with CMOS devices (an active interposer), just like a chip, and is face-to-face thermal compression bonded with the chiplets or



**Fig. 7.36** Chip-to-chip with TSV assembly (Sony's CIS) [25]

system-on-chip (SoC). Figures 7.39b, c show another new technology, announced in July 2019, by Intel called omni-directional interconnect (ODI). For ODI Type 1, Fig. 7.39b, the active TSV interposers (chips) are underneath the big chip such as an SoC, and are face-to-face thermal compression bonded with the SoC. For ODI Type 2, Fig. 7.39c, the active TSV interposer (bridge, i.e., chip) is underneath and connecting the chiplets/SoCs. ODI Type 3 is a special case of Type 2, in which the active interposer (or the base logic chip) is connecting the SoCs/chiplets. Intel also announced the management data input/output (MDIO) for die-to-die interface, which is used to replace the current advanced interface bus (AIB). All these heterogeneous integrations on TSV interposers are for extreme high performance, and the active TSV interposers are for even higher performance. In July 2020, Intel shipped the “Lakefield” processor with the FOVEROS technology as shown in Fig. 7.40 [27–29].

Figures 7.41 and 7.42 show IME’s memory chip and logic chip with TSVs bonded with microbumps. The design, material, process, and fabrication of the test structure have been reported in [30]. The SEM image of the structure, especially the TSVs portion, is shown in Fig. 7.41. The microbump (Cu-pillar + Sn cap) and under bump metallization (UBM) (electroless Ni immersion Au) of the interconnect are shown in Fig. 7.42.



**Fig. 7.37** Chip-to-active TSV-interposer (AMD/UCSB) [26]

### 7.3.4 3D IC Integration—Bumpless Hybrid Bonding of Chip-on-Chip with TSVs

During Intel Architecture Day (August 13, 2020), Intel announced a Cu–Cu hybrid bonding for their FOVEROS technology, Fig. 7.43. More details will be elaborated in Sect. 9.8.

Figure 7.44 shows some of TSMC’s 3DFabric technology [31–34], which consists of the frontend SoIC (system on integrated chips) technology and the backend SoIC + InFO technology. For frontend SoIC, Fig. 7.44a, TSMC use bumpless hybrid bonding to bond the chip on top of another chip with TSVs. For backend SoIC + InFO, Fig. 7.44b, TSMC use integrated chip first and face-up fan-out (InFO) to package the SoIC. More details will be elaborated in Sect. 9.9. TSMC also use their bumpless hybrid bonding for HBM for various number of DRAMs as shown in Fig. 7.45 [34]. It can be seen that because it is bumpless the package profile is lower than that from the conventional microbump flip chip technology.

Figure 7.46 shows the schematics of ARM’s bumpless hybrid bonding of chips with TSVs. Figure 7.46a is for bumpless face-to-face bonding, while Fig. 7.46b is

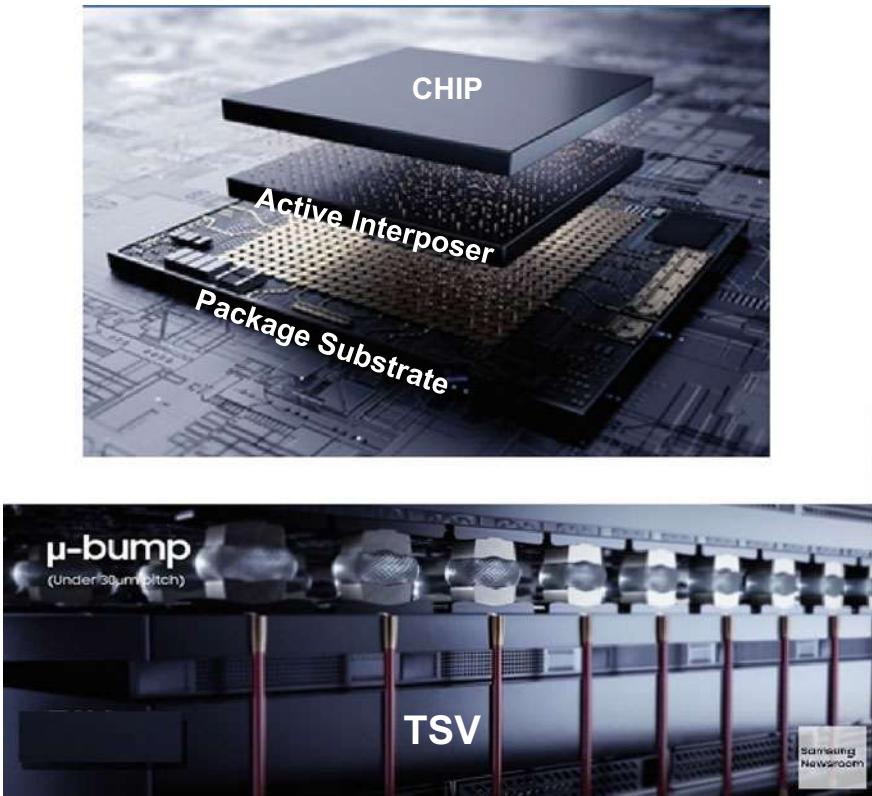


Fig. 7.38 Chip-to-active TSV-interposer (Samsung X-Cube)

bumpless face-to-back bonding [35]. Figure 7.46 also plots the maximum steady-state temperature (relative to the 2D baseline) for all the 3D configurations. It can be seen that for the 3D logic and memory partitioned CPU, the logic tier is always hotter due to higher power density. For the CPU-on-CPU case, the CPU on the bottom die shows a higher temperature profile since it is not in proximity to the heat sink. Among the different 3D configurations, the logic-on-memory 3D design has a temperature rise of around 5 °C while the memory-on-logic 3D design has a temperature rise of 9 °C compared to the 2D baseline.

### 7.3.5 3D IC Integration—Bumpless Hybrid Bonding of Chip-on-Chip Without TSVs

Figure 7.47 shows Sony's IMX260 BI-CIS [1, 2]. It can be seen that the BI-CIS chip (without TSVs) is bumpless hybrid bonding on the processor chip. Since 2016 Sony

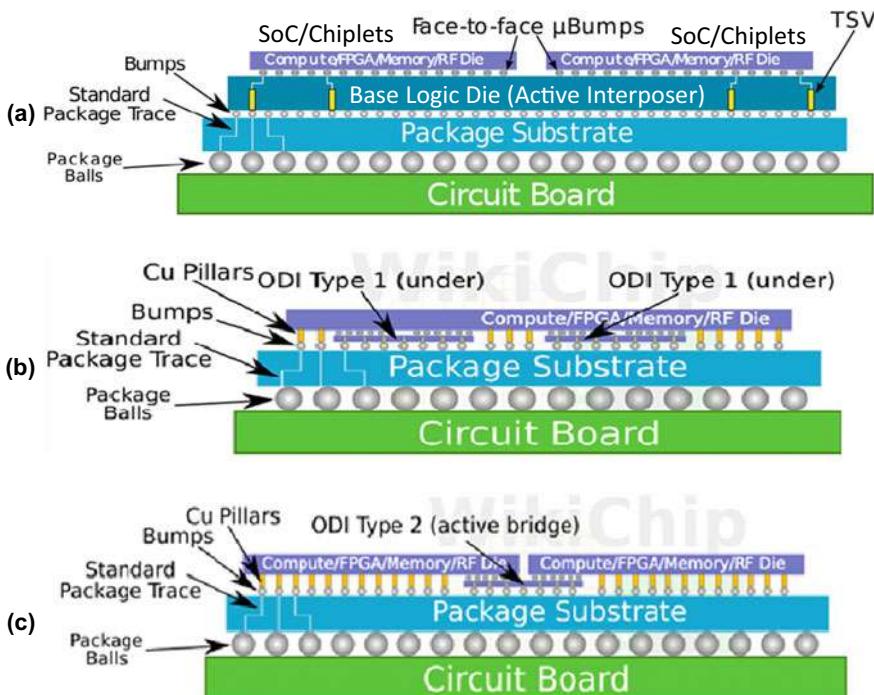


Fig. 7.39 Chip-to-active TSV-interposer (Intel) [27]

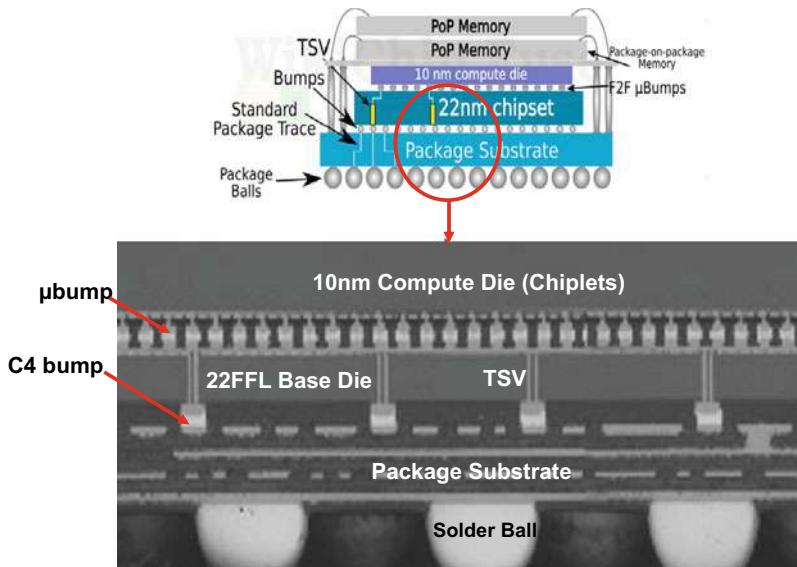
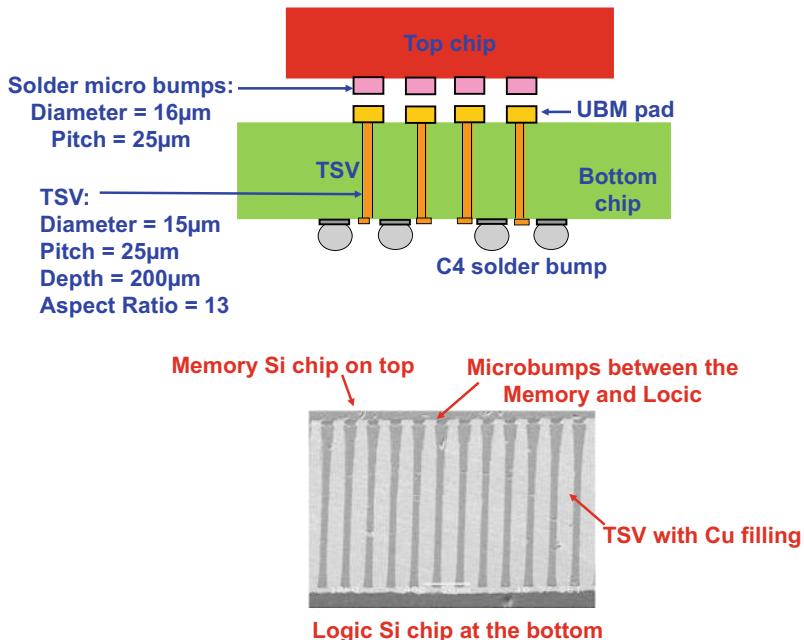


Fig. 7.40 Chip-to-active TSV-interposer (Intel FOVEROS) [27]



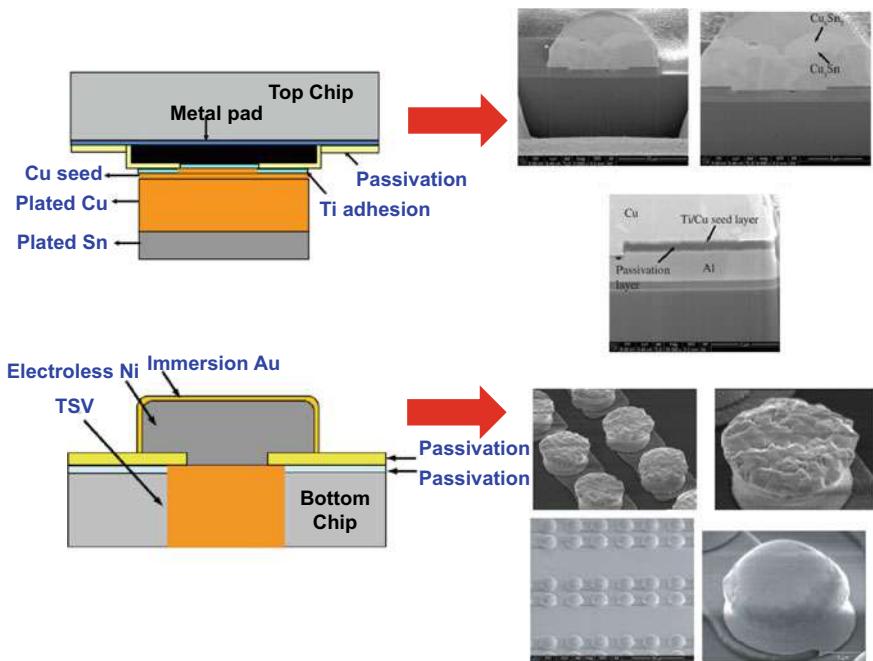
**Fig. 7.41** Chip-to-chip with TSVs (IME)

has been shipping this product at high volume. More details will be elaborated in Sect. 8.5.3.

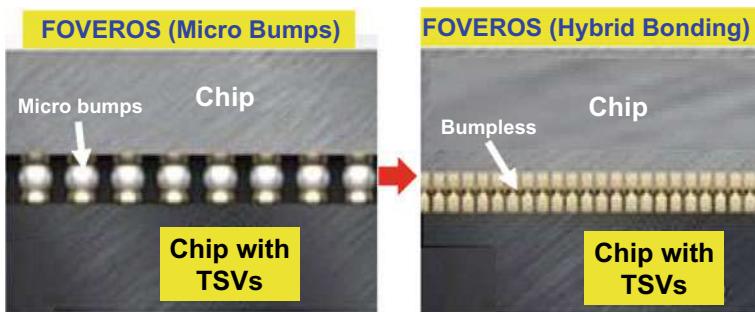
### 7.3.6 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- 3D IC packaging is the playground of fabless design houses and OSAT. Recently, however some system houses and foundries are doing 3D IC packaging such as PoP with their own advanced nodes semiconductor devices.
- 3D IC integration (with TSVs), straightly speaking, is fabricated by the foundry such as TSMC and IDM such as Intel.
- There are only a few ways to make the TSVs on device wafer, e.g., either via-middle or via-last [36–38]. Also, there are only a few ways (e.g., CoC, CoW, and WoW) to stack up the chips with TSVs, and a few interconnect structures/materials, e.g., either microbumps or bumpless. Right now, most TSVs in device wafer are fabricated by via-middle method and the assembly process is by CoW bonding with microbumps. However, bumpless CoW hybrid bonding is getting traction.

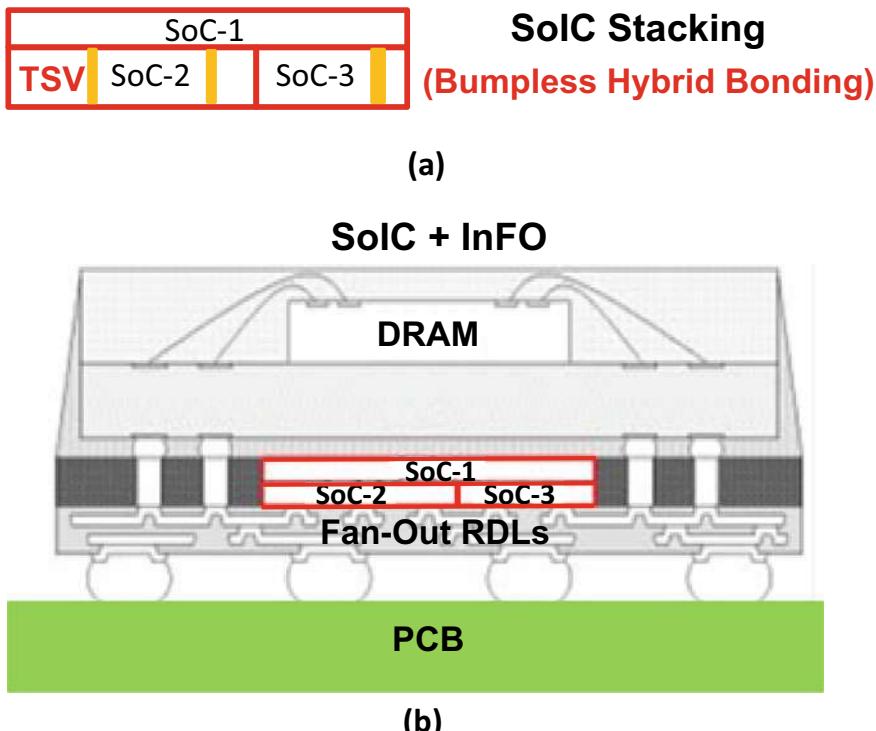


**Fig. 7.42** Chip-to-chip with TSVs interconnects (IME)

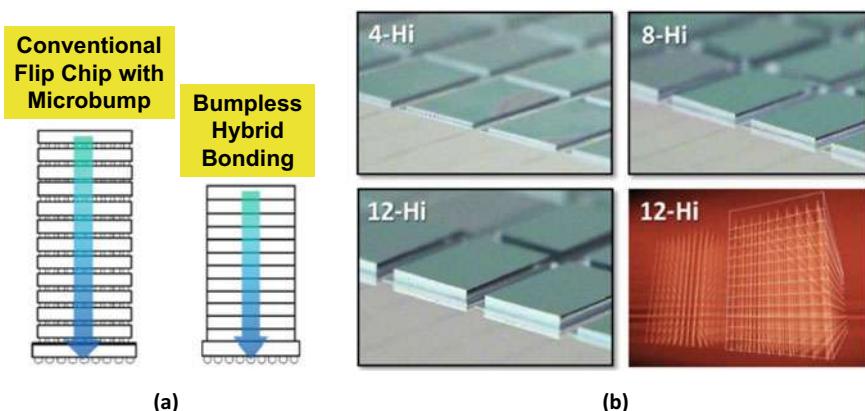


**Fig. 7.43** Bumpless hybrid bonding (Intel)

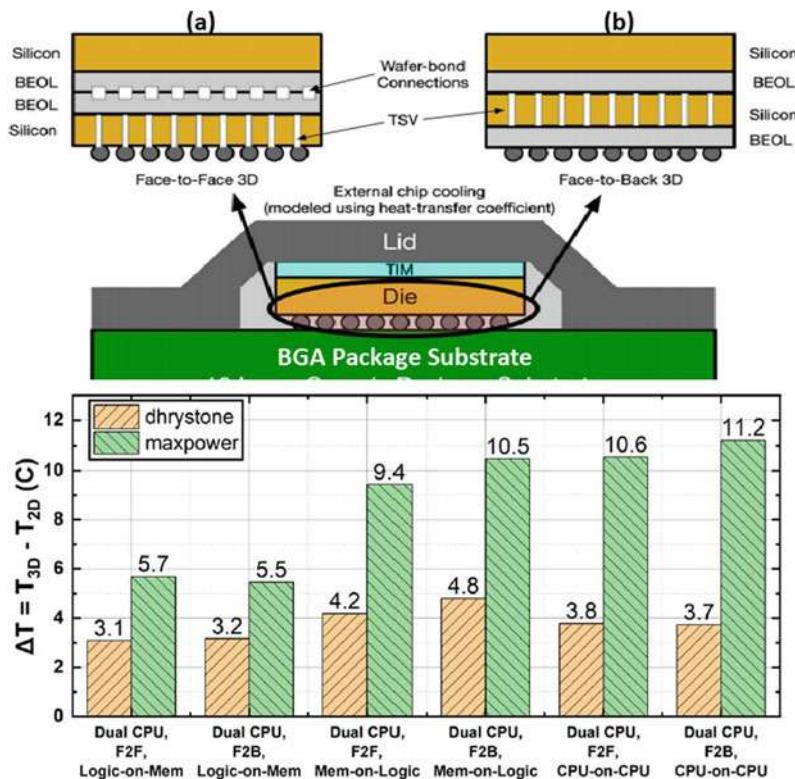
- For more information on the design, materials, process, manufacturing, and reliability of TSVs, 3D IC integration, and 3D IC packaging, please read [36–38].



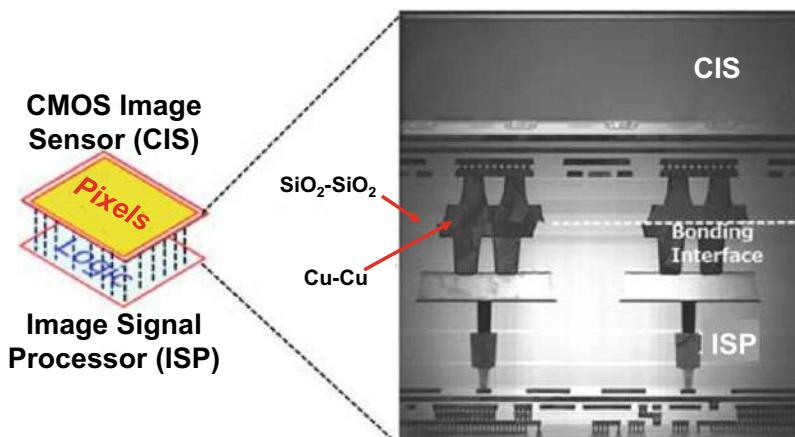
**Fig. 7.44** Bumpless hybrid bonding (TSMC). **a** Frontend SoIC. **b** Backend SoIC + InFO [33]



**Fig. 7.45** Bumpless hybrid bonding (TSMC). **a** Profile height comparison: conventional flip chip with microbump versus bumpless hybrid bonding. **b** Various stacks with bumpless hybrid bonding [34]



**Fig. 7.46** ARM's bumpless hybrid bonding of chips with TSVs. **a** Face-to-face hybrid bonding. **b** Face-to-back hybrid bonding [35]



**Fig. 7.47** Sony's bumpless hybrid bonding of chips without TSVs [1]

## References

1. Kagawa, Y., N. Fujii, K. Aoyagi, Y. Kobayashi, S. Nishi, N. Todaka, et al., “Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding,” *Proceedings of IEEE/IEDM*, Dec. 2016, pp. 8.4.1–8.4.4.
2. Kagawa, Y., N. Fujii, K. Aoyagi, Y. Kobayashi, S. Nishi, N. Todaka, S. Takeshita, J. Taura, H. Takahashi, Y. Nishimura, et al., “An Advanced CuCu Hybrid Bonding for Novel Stack CMOS Image Sensor”, *IEEE/EDTM Proceedings*, March 2018, pp. 1–3.
3. Lim, S., V. Rao, W. Hnin, W. Ching, V. Kripesh, C. Lee, J. H. Lau, J. Milla, and A. Fenner, “Process Development and Reliability of Microbumps”, *IEEE Transactions on CPMT*, Vol. 33, No. 4, December 2010, pp. 747–753.
4. Ravichandran, S., M. Kathaperumal, M. Swaminathan, and R. Tummala, “Large-body-sized Glass-based Active Interposer for High-Performance Computing”, *IEEE/ECTC Proceedings*, May 2020, pp. 879–884.
5. Zoschke, K., P. Mackowiak, K. Kröhnert, H. Oppermann, N. Jürgensen, M. Wietstruck, A. Göritz, S. Wipf, M. Kaynak, and K. Lang, “Cap Fabrication and Transfer Bonding Technology for Hermetic and Quasi Hermetic Wafer Level MEMS Packaging”, *IEEE/ECTC Proceedings*, May 2020, pp. 432–438.
6. Xie, J., and D. Patterson, “Realizing 3D IC Integration with Face-to-Face Stacking”, *Chip Scale Review*, May-June Issue, 2013, pp. 16–19.
7. Sutanto, J., 2012, “POSSUMTM Die Design as a Low Cost 3D Packaging Alternative,” *3D Package*, 25, pp. 16–18.
8. Hayes, S., N. Chhabra, T. Duong, Z. Gong, D. Mitchell, and J. Wright, “System-in-Package Opportunities with the Redistributed Chip Package (RCP)”, *Proceedings of IWLPC*, November 2011, pp. 10.1–10.7.
9. Yoon, S., J. Caparas, Y. Lin, and P. Marimuthu, “Advanced Low Profile PoP Solution with Embedded Wafer Level PoP (eWLB-PoP) Technology”, *Proceedings of IEEE/ECTC*, May 2012, pp. 1250–1254.
10. Jin, Y., J. Teyssyrex, X. Baraton, S. Yoon, Y. Lin, P. Marimuthu, “Development of Next General eWLB (Embedded Wafer Level BGA) Technology”, *Proceedings of IWLPC*, November 2011, pp. 7.1–7.7.
11. Chang, N., C. Chung, Y. Wang, C. Lin, P. Su, T. Shih, N. Kao, J. Hung, “3D Micro Bump Interface Enabling Top Die Interconnect to True Circuit Through Silicon Via Wafer”, *IEEE/ECTC Proceedings*, May 2020, pp. 1888–1893.
12. Itoi, K., M. Okamoto, Y. Sano, N. Ueta, S. Okude and O. Nakao, T. Tessier, S. Sivaswamy, and G. Stout, “Laminate Based Fan-Out Embedded Die Packaging Using Polyimide Multilayer Wiring Boards”, *Proceedings of IWLPC*, November 2011, pp. 7.8–7.14.
13. Lee, M., Yoo, M., Cho, J., Lee, S., Kim, J., Lee, C., Kang, D., Zwenger, C., and Lanzone, R., “Study of Interconnection Process for Fine Pitch Flip Chip,” *IEEE/ECTC Proceedings*, May 2009, pp. 720–723.
14. Singh, A., K. Sullivan, G. Leal, and T. Gong, “Assembly challenges with Flip Chip multi-die and interposer-based SiP Modules”, *IMAPS Proceedings*, October 2019, pp. T1–T18.
15. Furukawa, T., T. Kasuga, M. Umehara, and Y. Tamadate, “Prospects for automotive SiP modules applying IC assembly and packaging technology”, *IMAPS Proceedings*, October 2019, pp. M5–M10.
16. Yoon, S., P. Tang, R. Emigh, Y. Lin, P. C. Marimuthu, and R. Pendse, “Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions”, *Proceedings of IEEE/ECTC*, May 2013, pp. 1855–1860.
17. C.-F. Tseng, C.-S. Liu, C.-H. Wu, and D. Yu, “InFO (wafer level integrated fan-out) technology,” *Proceedings of IEEE/ECTC*, May 2016, pp. 1–6.
18. C.-C. Hsieh, C.-H. Wu, and D. Yu, “Analysis and comparison of thermal performance of advanced packaging technologies for state-of-the-art mobile applications,” *Proceedings of IEEE/ECTC*, May 2016, pp. 1430–1438.

19. Chuang, P., M. Lin, S. Hung, Y. Wu, D. Wong, M. Yew, C. Hsu, L. Liao, P. Lai, P. Tsai, S. Chen, S. Cheng, and S. Jeng, "Hybrid Fan-out Package for Vertical Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 333–338.
20. Kim, J., I. Choi, J. Park, J. Lee, T. Jeong, J. Byun, Y. Ko, K. Hur, D. Kim, and K. Oh, "Fan-out Panel Level Package with Fine Pitch Pattern", *IEEE/ECTC Proceedings*, May 2018, pp. 52–57.
21. Chong, S., E. Ching, S. Siang, S. Boon, T. Chai, "Demonstration of Vertically Integrated POP using FOWLP Approach", *IEEE/ECTC Proceedings*, May 2020, pp. 873–878.
22. Hou, S., W. Chen, C. Hu, C. Chiu, K. Ting, T. Lin, W. Wei, W. Chiou, V. Lin, V. Chang, C. Wang, C. Wu, and D. Yu, "Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology", *IEEE Transactions on Electron Devices*, Vol. 64, No. 10, October 2017, pp. 4071–4077.
23. Matsumura, K., Tomikawa, M., Sakabe, Y., and Shiba, Y., "New Non Conductive Film for high productivity process", *IEEE Proceedings of CPMT Symposium Japan*, 2015, pp. 19–20.
24. Asahi, N., Miyamoto, Y., Nimura, M., Mizutani, Y., and Arai, Y., "High Productivity Thermal Compression Bonding for 3D-IC", *Proceedings of IEEE International 3D Systems Integration Conference*, 2015, pp. TS7.3.1–TS7.3.5.
25. Sukegawa, S., T. Umebayashi, T. Nakajima, H. Kawanobe, K. Koseki, I. Hirota, T. Haruta, et al., "A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor," *Proceedings of IEEE/ISSCC*, San Francisco, CA, February 2013, pp. 484–486.
26. Stow, D., Y. Xie, T. Siddiqua, and G. H. Loh, "Cost-effective design of scalable high-performance systems using active and passive interposers," *Proc. of IEEE/ACM International Conf. on Computer-Aided Design*, Nov. 2017, pp. 728–735.
27. Ingerly, D., S. Amin, L. Aryasomayajula, A. Balankutty, D. Borst, A. Chandra, K. Cheemalapati, C. Cook, R. Criss, K. Enamul1, W. Gomes, D. Jones, K. Kolluru, A. Kandas, G.. Kim, H. Ma, D. Pantuso, C. Petersburg, M. Phen-givoni, A. Pillai, A. Sairam, P. Shekhar, P. Sinha, P. Stover, A. Telang, and Z. Zell, "Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices", *IEEE/IEDM Proceedings*, December 2019, pp. 19.6.1–19.6.4.
28. Gomes, W., S. Khushu, D. Ingerly, P. Stover, N. Chowdhury, F. O'Mahony, etc., "Lakefield and Mobility Computer: A 3D Stacked 10 nm and 2FFL Hybrid Processor System in  $12 \times 12 \text{ mm}^2$ , 1 mm Package-on-Package", *IEEE/ISSCC Proceedings*, February 2020, pp. 40–41.
29. WikiChip, "A Look at Intel Lakefield: A 3D-Stacked Single-ISA Heterogeneous Penta-Core SoC", <https://en.wikichip.org/wiki/chiplet>, May 27, 2020.
30. Yu, A. B., J. H. Lau, S. Ho, A. Kumar, W. Hnin, W. Lee, M. Jong, et al., "Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects", *IEEE Transactions on CPMT*, Vol. 1, No. 9, September 2011, pp. 1336–1344.
31. Chen, M. F. C. S. Lin, E. B. Liao, W. C. Chiou, C. C. Kuo, C. C. Hu, C. H. Tsai, C. T. Wang and D. Yu, "SoIC for Low-Temperature, Multi-Layer 3D Memory Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.
32. Chen, Y. H., C. A. Yang, C. C. Kuo, M. F. Chen, C. H. Tung, W. C. Chiou, and D. Yu, "Ultra High Density SoIC with Sub-micron Bond Pitch", *IEEE/ECTC Proceedings*, May 2020, pp. 576–581.
33. Chen, F., M. Chen, W. Chiou, D. Yu, "System on Integrated Chips (SoIC<sup>TM</sup>) for 3D Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2019, pp. 594–599.
34. Chen, M., C. Lin, E. Liao, W. Chiou, C. Kuo, C. Hu, C. Tsai, C. Wang and D. Yu, "SoIC for Low-Temperature, Multi-Layer 3D Memory Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.
35. Mathur, R., C. Chao, R. Liu, N. Tadepalli, P. Chandupatla, S. Hung, X. Xu, S. Sinha, and J. Kulkarni, "Thermal Analysis of a 3D Stacked High-Performance Commercial Microprocessor using Face-to-Face Wafer Bonding Technology", *IEEE/ECTC Proceedings*, May 2020, pp. 541–547.
36. Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill, New York, 2016.
37. Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, McGraw-Hill, New York, 2013.

38. Lau, J. H., *Reliability of RoHS compliant 2D & 3D IC Interconnects*, McGraw-Hill, New York, 2011.
39. Kumahara, K., R. Liang, S. Lee, Y. Miwa, M. Murugesan, H. Kino, T. Fukushima, and T. Tanaka, “Low-temperature multichip-to-wafer 3D integration based on via-last TSV with OER-TEOS-CVD and microbump bonding without solder extrusion”, *IEEE/ECTC Proceedings*, May 2020, pp. 1199–1204.
40. Ma, S., Y. Liu, F. Zheng, F. Li, D. Yu, A. Xiao, and X. Yang, “Development and Reliability study of 3D WLCSP for automotive CMOS image sensor using TSV technology”, *IEEE/ECTC Proceedings*, May 2020, pp. 461–466.
41. Camara, J., S. Soroushiani, D. Wilding, S. Sayeed, M. Monshi, J. Volakis, S. Bhardwaj, and P. Raj, “Remateable and Deformable Area-Array Interconnects in 3D Smart Wireless Sensor Packages”, *IEEE/ECTC Proceedings*, May 2020, pp. 671–676.
42. Kawano, M., X. Wang, and Q. Ren, “Trench Isolation Technology for Cost-effective Wafer-level 3D Integration with One-step TSV”, *IEEE/ECTC Proceedings*, May 2020, pp. 1161–1166.
43. Miwa, Y., K. Kumahara, S. Lee, R. Liang, H. Kino, T. Fukushima, and T. Tanaka, “7- $\mu\text{m}$ -thick NCF technology with low-height solder microbump bonding for 3D integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 1453–1458.
44. Kaul, A., S. Rajan, M. Hossen, G. May, and M. Bakir, “BEOL-Embedded 3D Polylithic Integration: Thermal and Interconnection Considerations”, *IEEE/ECTC Proceedings*, May 2020, pp. 1459–1467.
45. Seo, H., S. Kim, H. Park, G. Kim, and Y. Park, “Effects of two-step plasma treatment on Cu and SiO<sub>2</sub> surfaces for 3D bonding applications”, *IEEE/ECTC Proceedings*, May 2020, pp. 1677–1683.
46. Jourdain, A., J. Vos, E. Chery, G. Beyer, G. Plas, E. Walsby, K. Roberts, H. Ashraf, D. Thomas, and E. Beyne, “Extreme Wafer Thinning and nano-TSV processing for 3D Heterogeneous Integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 42–48.
47. Chen, Y., C. A. Yang, C. C. Kuo, M. F. Chen, C. H. Tung, W. C. Chiou, and D. Yu, “Ultra High Density SoIC with Sub-micron Bond Pitch”, *IEEE/ECTC Proceedings*, May 2020, pp. 576–581.
48. Liu, D., P. Chen, and K. Chen\*, “A Novel Low-Temperature Cu-Cu Direct Bonding with Cr Wetting Layer and Au Passivation Layer”, *IEEE/ECTC Proceedings*, May 2020, pp. 1322–1327.
49. Rahimi, A., P. Somarajan, and Q. Yu, “Modeling and Characterization of Through-SiliconVias (TSVs) in Radio Frequency Regime in an Active Interposer Technology”, *IEEE/ECTC Proceedings*, May 2020, pp. 1383–1389.
50. Lim, T., D. Ho, C. Chong, and S. Bhattacharya, “3D FOWLP Integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 1728–1735.
51. Kim, J., K. Yoon, H. Oh, E. Ahn, Y. Shin, and Y. Kim, “Study on Advanced Substrate for Double-side Package to Reduce Module Size”, *IEEE/ECTC Proceedings*, May 2020, pp. 1904–1909.
52. Singh, S., and T. Kukal, “LTCC PoP Technology-Based Novel Approach for mm-Wave 5G System for Next Generation Communication System”, *IEEE/ECTC Proceedings*, May 2020, pp. 1973–1978.
53. Tsai, M., R. Chiu, D. Huang, F. Kao, E. He, J. Chen, S. Chen, J. Tsai, and Y. Wang, “Innovative Packaging Solutions of 3D Double Side Molding with System in Package for IoT and 5G Application”, *IEEE/ECTC Proceedings*, May 2019, pp. 700–706.
54. Mori, K., S. Yamashita, T. Fukuda, M. Sekiguchi, H. Ezawa, and S. Akejima, “3D Fan-Out Package Technology with Photosensitive Through Mold Interconnects”, *IEEE/ECTC Proceedings*, May 2019, pp. 1140–1145.
55. Ravichandran, S., S. Yamada, F. Liu, V. Smet, M. Kathaperumal, and R. Tummala, “Low-Cost Non-TSV based 3D Packaging using Glass Panel Embedding (GPE) for Power-efficient, High-Bandwidth Heterogeneous Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 1796–1802.
56. England, L., D. Fisher, K. Rivera, B. Guthrie, P. Kuo, C. Lee, C. Hsu, F. Min, K. Kang, and C. Weng, “Die-to-Wafer (D2W) Processing and Reliability for 3D Packaging of Advanced Node Logic”, *IEEE/ECTC Proceedings*, May 2019, pp. 600–606.

57. Yu, D., Y. Zou, X. Xu, A. Shi, X. Yang, and Z. Xiao, “Development of 3D WLCSP with Black Shielding for Optical Finger Print Sensor for the Application of Full Screen Smart Phone”, *IEEE/ECTC Proceedings*, May 2019, pp. 884–889.
58. Kawano, M., X. Wang, and Q. Ren, “New Cost-effective Via-last Approach by “One-step TSV” after Wafer Stacking for 3D Memory Applications”, *IEEE/ECTC Proceedings*, May 2019, pp. 1996–2002.
59. Panigrahy, A., S. Bonam, T. Ghosh, S. Rama, K. Vanjari, and S. Singh, “Diffusion enhanced drive sub 100 °C wafer level fine-pitch Cu-Cu thermocompression bonding for 3D IC integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 2156–2161.
60. Lee, J., S. Park, Y. Kim, J. Lee, S. Lee, C. Lee, Y. Kwon, C. Lee, J. Kim, N. Kim, Y. Sung, “Three-Dimensional Integrated Circuit (3D-IC) Package Using Fan-out Technology”, *IEEE/ECTC Proceedings*, May 2019, pp. 35–40.
61. Jung, J., H. Lee, J. Kim, Y. Park, J. Yu, Y. Park, J. Lim, H. Choi, S. Cho, D. Kim, and S. An, “A Study of 3D Packaging Interconnection Performance affected by Thermal Diffusivity and Pressure Transmission”, *IEEE/ECTC Proceedings*, May 2019, pp. 204–209.
62. Coudrain, P., J. Charbonnier, A. Garnier, P. Vivet, R. Vélard, A. Vinci, F. Ponthenier, A. Farcy, R. Segaud, P. Chausse, L. Arnaud, D. Lattard, E. Guthmuller, G. Romano, A. Gueugnot, F. Berger, J. Beltritti, T. Mourier, M. Gottardi, S. Minoret, C. Ribiére, G. Romero, P. Philip, Y. Exbrayat, D. Scevola, D. Campos, M. Argoud, N. Allouti, R. Eleouet, C. Tortolero, C. Aumont, D. Dutoit, C. Legalland, J. Michailos, S. Chéramy, and G. Simon, “Active interposer technology for chiplet-based advanced 3D system architectures”, *IEEE/ECTC Proceedings*, May 2019, pp. 569–578.
63. Su, A., T. Ku, C. Tsai, K. Yee, and D. Yu, “3D-MiM (MUST-in-MUST) Technology for Advanced System Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 1–6.
64. Watanabe, A., Y. Wang, N. Ogura, P. Raj, V. Smet, M. Tentzeris, and R. Tummala, “Low-Loss Additively-Deposited Ultra-Short Copper-Paste Interconnections in 3D Antenna-Integrated Packages for 5G and IoT Applications”, *IEEE/ECTC Proceedings*, May 2019, pp. 972–976.
65. Ahmed, O., G. Jalilvand, H. Fernandez, P. Su, T. Lee, and T. Jiang, “Long-Term Reliability of Solder Joints in 3D ICs under Near-Application Conditions”, *IEEE/ECTC Proceedings*, May 2019, pp. 1106–1112.
66. Jouve, A., L. Sanchez, C. Castan, M. Laugier, E. Rolland, B. Montmayeul, R. Franiatte, F. Fournel, and S. Cheramy, “Self-Assembly process for 3D Die-to-Wafer using direct bonding: A step forward toward process automatisation”, *IEEE/ECTC Proceedings*, May 2019, pp. 225–234.
67. Hwang, T., D. Oh, J. Kim, E. Song, T. Kim, K. Kim, J. Lee, and T. Kim, “The Thermal Dissipation Characteristics of The Novel System-In-Package Technology (ICE-SiP) for Mobile and 3D High-end Packages”, *IEEE/ECTC Proceedings*, May 2019, pp. 614–619.
68. Sirbu, B., Y. Eichhammer, H. Oppermann, T. Tekin, J. Kraft, V. Sidorov, X. Yin, J. Bauwelinck, C. Neumeyr, and F. Soares, “3D Silicon Photonics Interposer for Tb/s Optical Interconnects in Data Centers with double-side assembled active components and integrated optical and electrical Through Silicon Via on SOI”, *IEEE/ECTC Proceedings*, May 2019, pp. 1052–1059.
69. Sun, X., N. Pantano, S. Kim, G. Van der Plas and E. Beyne, “Inductive links for 3D stacked chip-to-chip communication”, *IEEE/ECTC Proceedings*, May 2019, pp. 1215–1220.
70. Jani, I., D. Lattard, P. Vivet, L. Arnaud, S. Cheramy, E. Beigné, A. Farcy, J. Jourdon, Y. Henrion, E. Deloffre, and H. Bilgen, “Characterization of fine pitch Hybrid Bonding pads using electrical misalignment test vehicle”, *IEEE/ECTC Proceedings*, May 2019, pp. 1926–1932.

# Chapter 8

## Hybrid Bonding



### 8.1 Introduction

First of all, the focus of this chapter is on silicon-to-silicon flip chip bonding and is not for silicon-to-organic substrate flip chip bonding as shown in Chaps. 2, 3, and 5. There are at least two different Cu–Cu bondings, namely Cu–Cu thermal compression bonding (TCB) [1–11] and low-temperature direct bond interconnect (hybrid bonding) [12–37]. Most Cu–Cu TCBs operate at high temperature (normally 350–400 °C) and high pressure to drive the diffusion of Cu atoms across the interface to form monolithic copper. Hybrid bonding (that combines a dielectric bond with a metal bond to form an interconnection) is very different from Cu–Cu TCB. Hybrid bonding is also known industry-wide as low-temperature DBI (direct bond interconnect), which operates at room temperature and then anneal at 150–300 °C.

DBI was invented by Research Triangle Institute (RTI) and patented it as ZiBond (a direct oxide to oxide bonding that involves wafer-to-wafer processing at low temperatures to initiate high bond strengths). Between 2000 and 2001, Fountain, Engquist, Tong, and several other colleagues founded Ziptronix as a spin-out of RTI. Between 2004 and 2005, based on their ZiBond technology, Ziptronix combined the dielectric bond with embedded metal to simultaneously bond wafers and form the interconnects at low temperature (so called DBI) [36, 37]. Ziptronix was acquired by Tessera on August 28, 2015. Tessera has changed its name to Xperi on February 23, 2017.

The breakthrough for Ziptronix DBI technology came in the spring of 2015 when Sony, already using its “Zibond” oxide to oxide bonding technology extended its license to include DBI. DBI is now being used for much of the CMOS image sensor market in the world’s smartphones and other image-based devices.

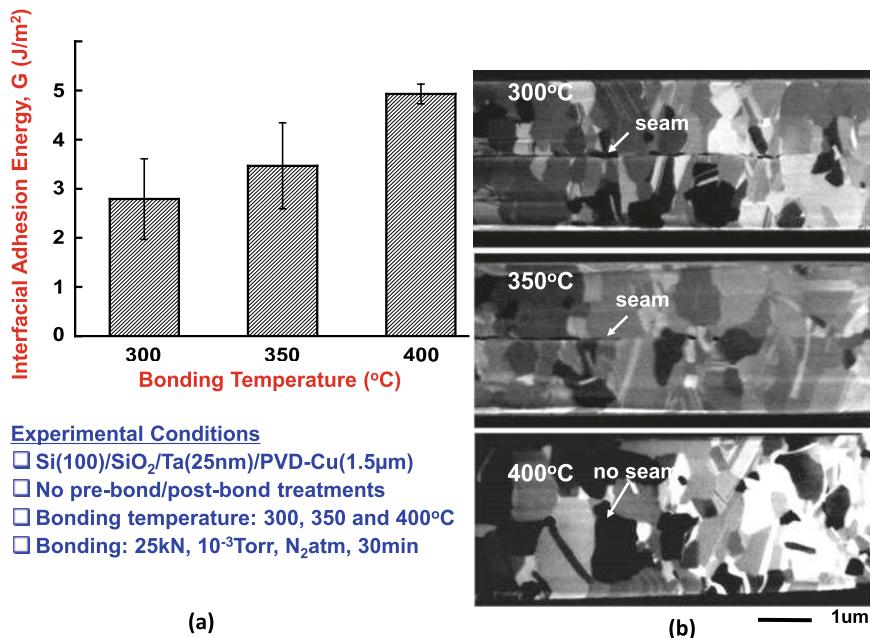
In this chapter, Cu–Cu TCB, SiO<sub>2</sub>–SiO<sub>2</sub> TCB, and room-temperature (RT) Cu–Cu TCB will be briefly mentioned first. Then, the DBI will be discussed. Finally, some new developments in hybrid bonding will be briefly mentioned.

## 8.2 Cu–Cu TCB

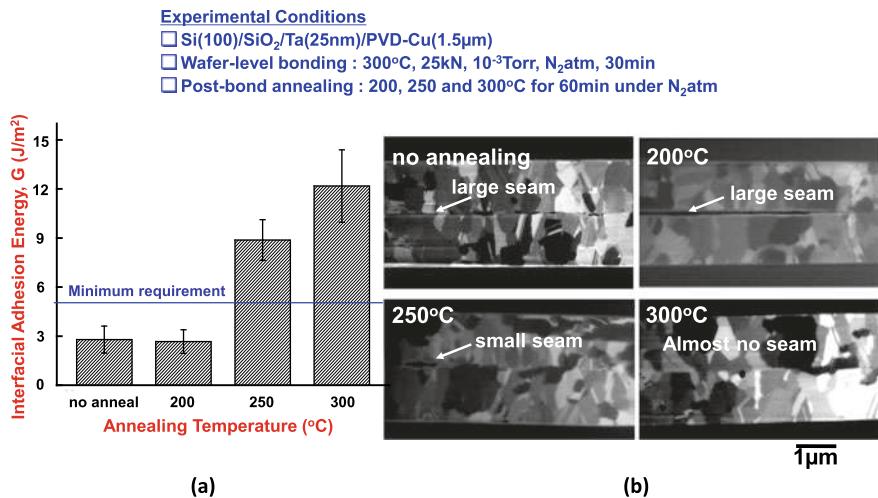
### 8.2.1 Some Fundamental on Cu–Cu TCB

The advantages of Cu–Cu bonding interconnects are to provide much lower electrical resistivity, very high density, and lower electromigration than any other joints. On the other hand, in order to reduce the tendency to form native oxides which strongly affect the bonding reliability, Cu–Cu bonding usually operates at high temperature ( $\sim 400^\circ\text{C}$ ) and pressure and long process time (60–120 min), which are not desirable for throughput (not to mention the cool-down time) and the device reliability.

Figure 8.1 shows the effect of bonding temperature on the critical interfacial adhesion energy. (The critical interfacial adhesion energy is also called critical energy release rate at the interface. If the maximum interfacial adhesion energy is larger than the critical interfacial adhesion energy, then the interfacial delamination will take place.) It can be seen that the higher the bonding temperature the higher the critical interfacial adhesion energy ( $G_c$ ), i.e., the stronger the bond (joint). Also, it is shown from Fig. 8.1 that the higher the temperatures, the less the seams between the interface and the original bond interface tends to disappear due to an activated



**Fig. 8.1** Effect of bonding temperature on bond interface properties: **a** Interfacial adhesion energies, and **b** SEM images of microstructures



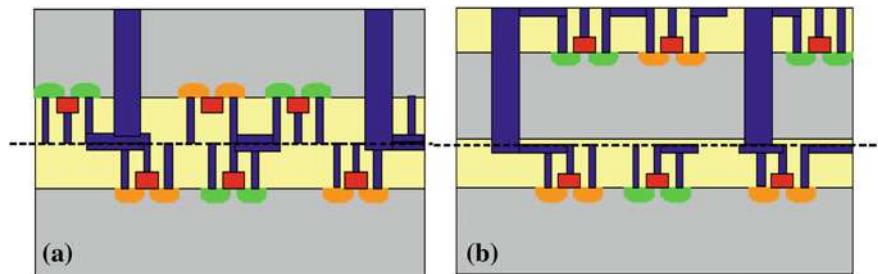
**Fig. 8.2** Effect of (Cu–Cu) post-bond annealing temperature on the bond interface properties: **a** Interfacial adhesion energies, and **b** SEM images of microstructures

interdiffusion through the two interfacial layers. That's the major reason why high temperature is needed for Cu–Cu bonding [1].

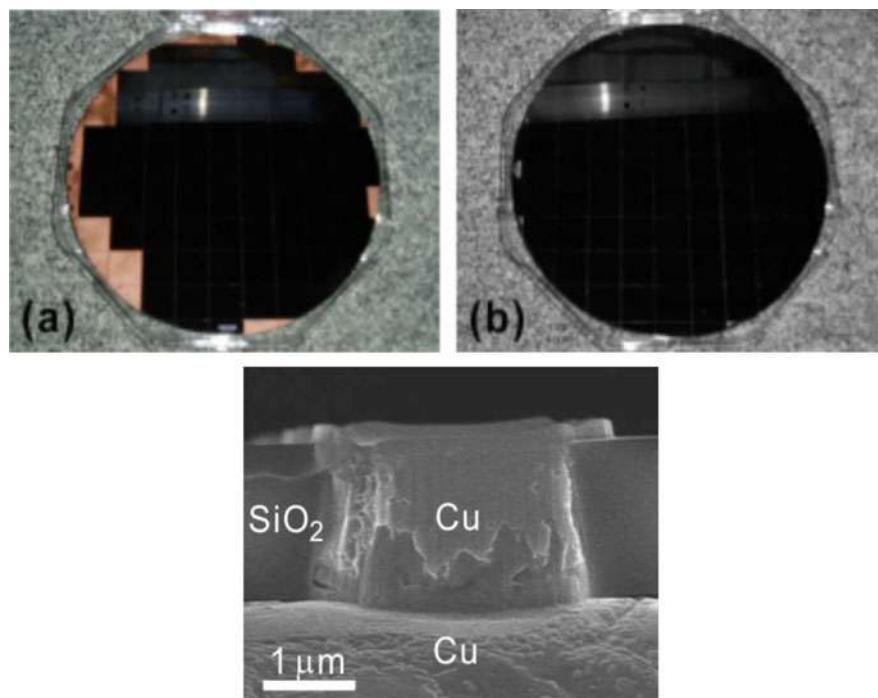
One way to reduce the bonding temperature and obtain high quality bonds (interconnects) is by annealing. Figure 8.2 shows the effects of various annealing temperatures on the critical interfacial adhesion energy,  $G_c$ . It can be seen that for bonding temperature at 300 °C for 30 min under 25kN force on a 8" wafer, after annealing temperature at 300 °C for 60 min under N<sub>2</sub> atm, the  $G_c$  is increased from 2.8 J/m<sup>2</sup> (without annealing) to 12.2 J/m<sup>2</sup>. Even for 60 min of annealing temperature at 250 °C, the  $G_c$  is increased to 8.9 J/m<sup>2</sup>. However, too low an annealing temperature won't help, e.g., 200 °C as shown in Fig. 8.2.

### 8.2.2 IBM/RPI's Cu–Cu TCB

Figure 8.3a schematically shows the IBM/RPI bonding structure of two device layers bonded in a face-to-face approach, and Fig. 8.3b shows one with the face-to-back approach [2–4]. A typical Cu–Cu interconnect is shown in Fig. 8.4, which shows a high-quality bonding interface. Before bonding, the Cu interconnects (pads) are fabricated with the standard BEOL (back end of line) damascene process, followed by the oxide CMP (chemical-mechanical polishing) process (oxide touch-up) to recess the oxide level to 40 nm lower than the Cu surface. The bonding temperature is ramped up to 400 °C.



**Fig. 8.3** **a** Face-to-face WoW bonding. **b** Face-to-back WoW bonding [2]



**Fig. 8.4** IBM/RPI's Cu–Cu WoW bonding [2]

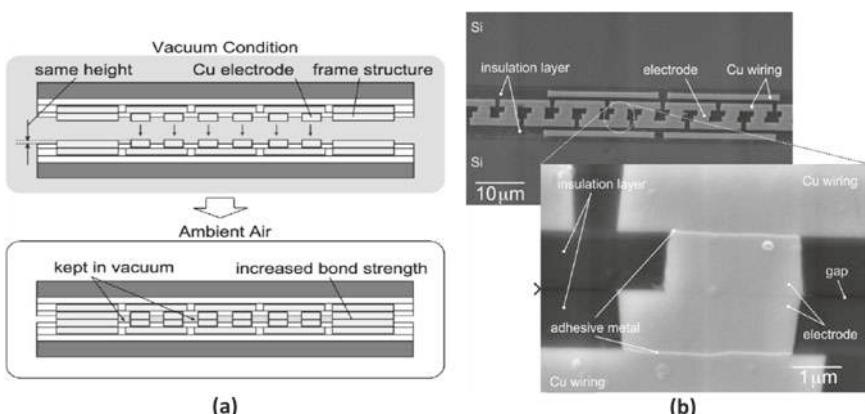
## 8.3 Cu–Cu TCB at Room Temperature

### 8.3.1 Some Fundamental on Cu–Cu TCB at Room Temperature

Cu–Cu bonding at room temperature leads to the highest throughput and least device reliability concerns as well as very low costs. However, the drawbacks of room temperature bonding are the stringent requirements on: (1) pad/trace/wafer planarization and (2) surface treatment to ensure smooth hydrophilic surfaces for high quality bonding.

### 8.3.2 NIMS/AIST/Toshiba/University of Tokyo's Cu–Cu TCB at Room Temperature

Figure 8.5a schematically shows the NIMS/AIST/Toshiba/University of Tokyo bonding structure of two device layers bonded at room temperature [5–11]. A typical cross-sectional scanning electron microscope (SEM) image of the interface between the bumpless electrodes (pads) after a high-temperature storage test is shown in Fig. 8.5b. It can be seen that a tight adhesion between surfaces is maintained even after exposed to 150 °C for 1000 h [5–11].



**Fig. 8.5** NIMS/AIST/Toshiba/University of Tokyo's room temperature Cu–Cu bonding [8]

## 8.4 SiO<sub>2</sub>–SiO<sub>2</sub> TCB

### 8.4.1 Some Fundamental on SiO<sub>2</sub>–SiO<sub>2</sub> TCB

SiO<sub>2</sub>–SiO<sub>2</sub> bonding usually takes three steps, pre-bonding, bonding, and post-bonding. The pre-bonding is operated at room temperature, which eliminates run-out errors in wafer alignment, and thus leads to higher post-bond alignment accuracy. In order to achieve covalent bonds (interconnects), the bonding temperature is very high (~400 °C). In order to achieve strong chemical bonds (interconnects) with lower annealing (post-bond) temperature (200–400 °C), the surface chemistry must be modified by plasma activation. Figure 8.6 shows the effects of annealing temperature on the critical bonding energy. As expected, the higher the annealing temperatures the stronger the critical bonding energy. Unfortunately, due to the maximum allowable temperature of most devices, 400 °C is the most used. Figure 8.7 shows the effect of temperature annealing time on the critical surface energy at 300 °C annealing temperature. It can be seen that: (1) the longer the annealing time the larger the critical surface energy; (2) one hour annealing time is more than enough;

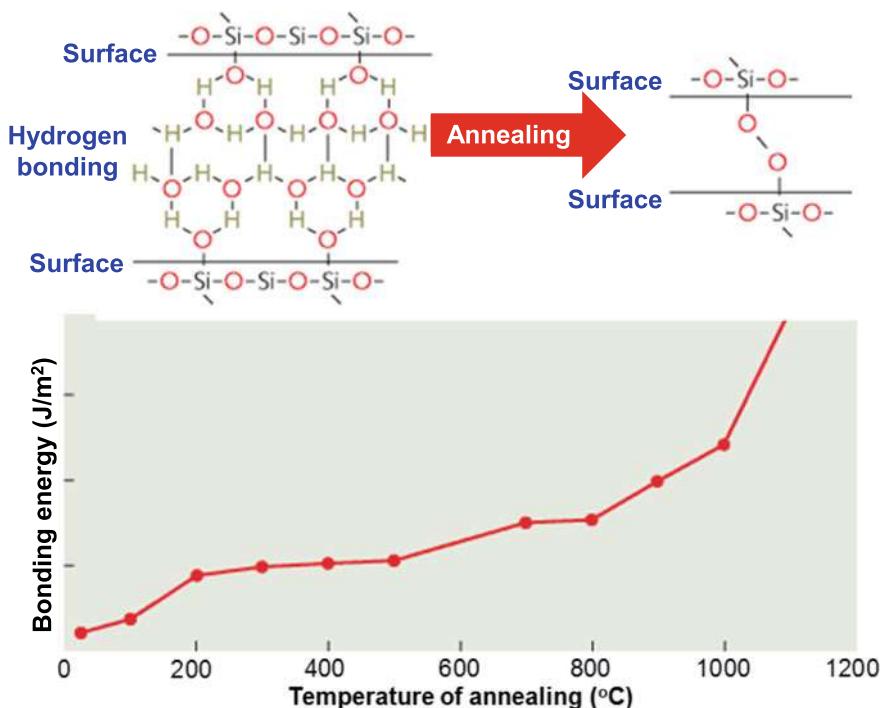
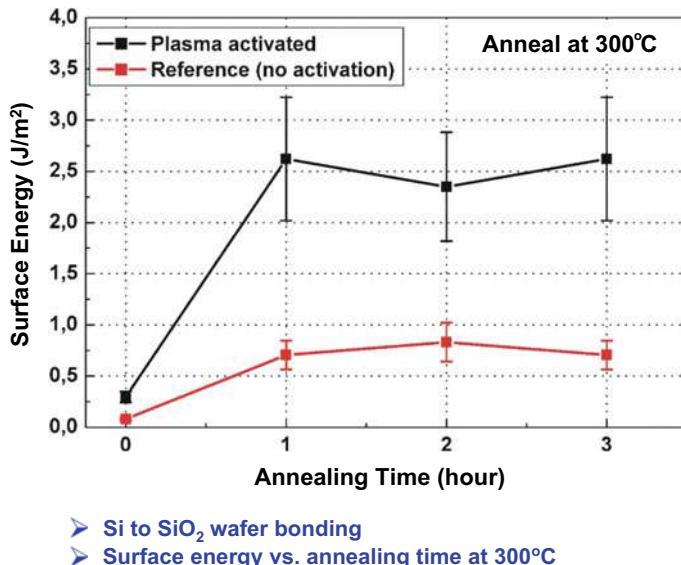


Fig. 8.6 Bonding energy (SiO<sub>2</sub>–SiO<sub>2</sub>) as a function of temperature of annealing



**Fig. 8.7** Surface energy as a function of thermal annealing time at 300 °C (SiO<sub>2</sub>–SiO<sub>2</sub>)

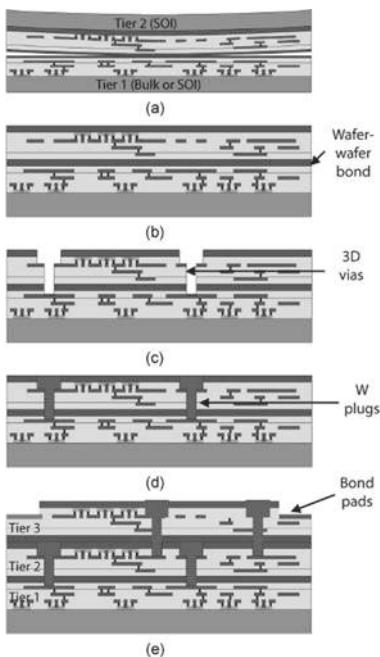
and (3) the plasma activation on the surface chemistry before bonding has a great impact on the critical surface energy.

#### 8.4.2 MIT's SiO<sub>2</sub>–SiO<sub>2</sub> TCB

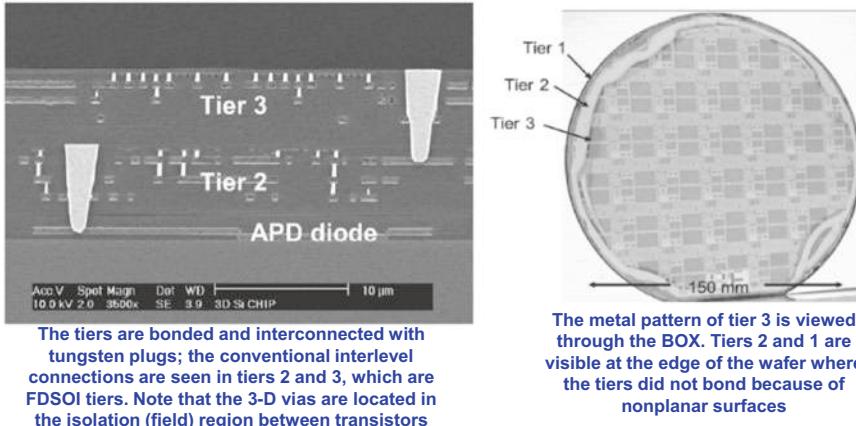
Figure 8.8 schematically shows MIT's oxide-to-oxide bonding structure of three device layers bonded at 275 °C [38–44]. It can be seen that: (a) two completed circuit wafers (Tier 1 and Tier 2) are planarized, aligned, and bonded face-to-face together; (b) a wet etch of the handle silicon exposes the buried oxide (BOX) of the upper wafer; (c) 3D vias are patterned and etched through the BOX and deposited oxides expose metal contacts in both layers; (d) a Ti/TiN liner and 1  $\mu\text{m}$  of tungsten (W) are deposited to fill the 3D vias (with the larger diameter equal to 1.5  $\mu\text{m}$ ) and electrically connect the two layers; and (e) a third layer can then be bonded with its face to the BOX (back) of Tier (layer) 2 and 3D vias are formed. Figure 8.9 shows a typical cross section of the three-layer 3D (ring oscillator) structure. It can be seen that: (1) the layers are bonded and interconnected with W-plugs, (2) the conventional interlevel connections are in the bottom two layers, and (3) the 3D vias are located in the isolation (field) region between transistors. A few functional 3D structures/circuits have been created and demonstrated [38–44].

**MIT's Assembly Process for a 3D Si integration:**

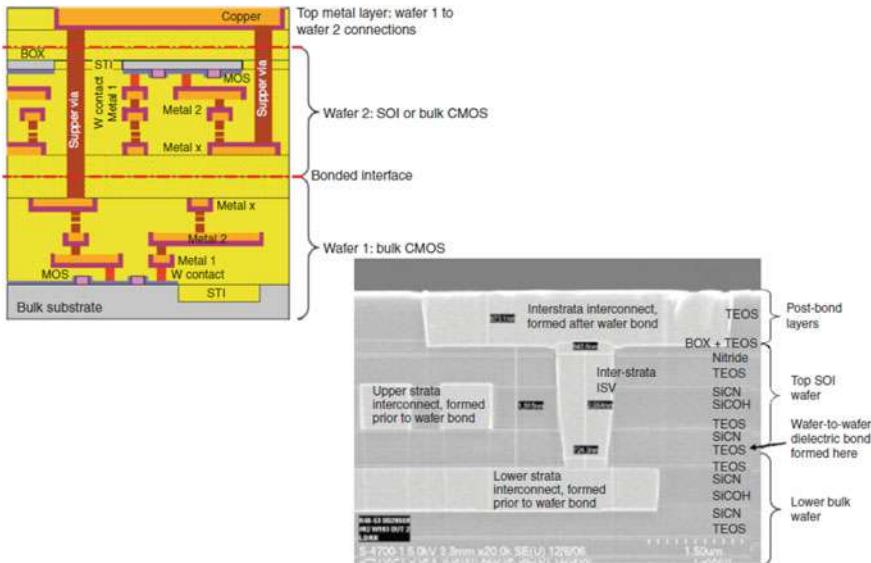
1. Two completed circuit wafers are planarized, aligned, and bonded face to face.
2. The handle silicon is removed.
3. 3-D vias are etched through the deposited buried oxide (BOX) and the field oxides.
4. Tungsten plugs are formed to connect circuits in both tiers.
5. After tier 3 is transferred, bond pads are etched through the BOX for testing and packaging.



**Fig. 8.8** MIT's WoW assembly process for  $\text{SiO}_2\text{-SiO}_2$  [38]



**Fig. 8.9** MIT's  $\text{SiO}_2\text{-SiO}_2$  WoW bonding results [38]



**Fig. 8.10** Leti/Freescale/STMicroelectronics' SiO<sub>2</sub>–SiO<sub>2</sub> WoW bonding [45]

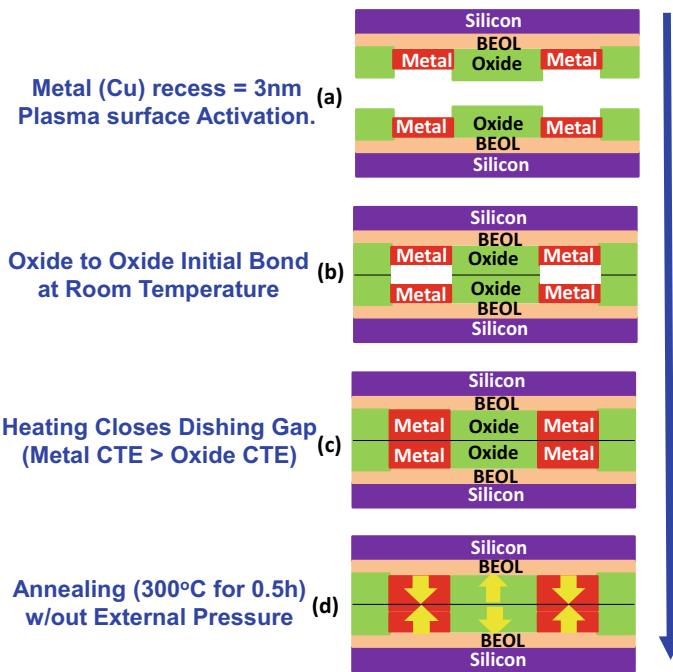
### 8.4.3 Leti/Freescale/STMicroelectronics' SiO<sub>2</sub>–SiO<sub>2</sub> TCB

Figure 8.10 schematically shows Leti/Freescale/STMicroelectronics' dielectric-to-dielectric bonding structure of two device layers bonded at <400 °C [45–47]. It can be seen that: (a) first, a metal level is formed on a 200 mm bulk wafer and SOI wafer; next, these wafers are bonded face to face, and then the bulk silicon of the SOI wafer is removed down to the BOX layer; (b) the interstrata vias (ISVs) are formed, which make contact from upper strata to lower strata; and (c) a metal layer is formed at the top of the back side of the SOI wafer. The typical cross-section of an ISV is shown in Fig. 8.10 [45–47], and it can be seen that this ISV (~1.5 μm) makes good contact.

## 8.5 Low Temperature DBI

### 8.5.1 Some Fundamental on Low Temperature DBI

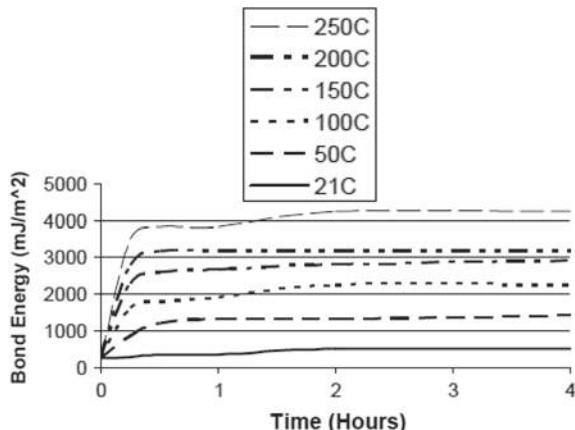
Figure 8.11 shows the key process steps for the low temperature DBI [12–37]. First of all, controlling nano-scale topography is very important for the DBI technology. The dielectric surface should be extremely flat and smooth before activation and bonding. Chemical-mechanical polishing (CMP) should achieve a very low dielectric roughness (<0.5 nm RMS) and a certain recess of metal areas below the dielectric surface as shown in Fig. 8.11a. Upon contact, the dry plasma-activated dielectric surfaces



**Fig. 8.11** Key process steps of low temperature DBI

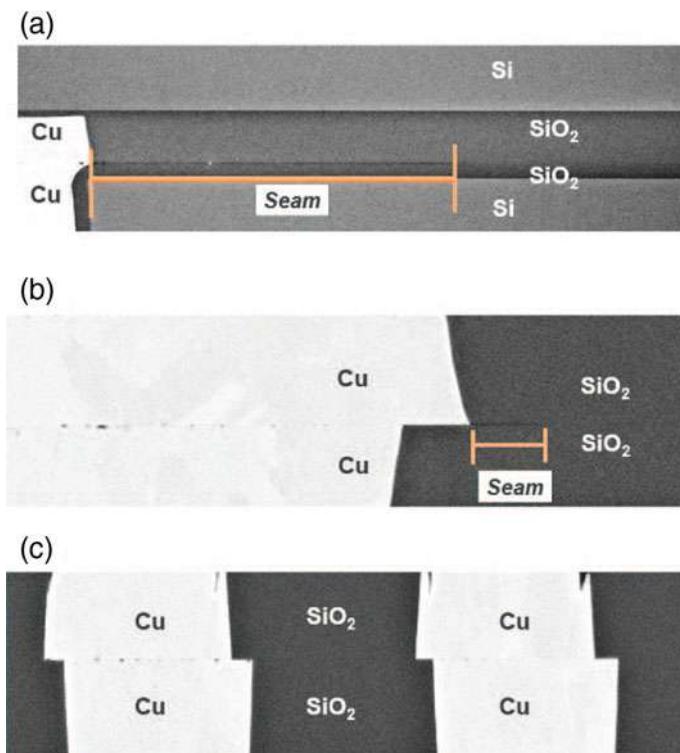
bond together instantaneously as shown in Fig. 8.11b at room temperature. (Very high bond energies can be obtained at very low temperatures as shown in Fig. 8.12 [18]). The dishing gap can be closed by heating as shown in Fig. 8.11c. (This step is optional because the dishing gap can also be closed by the following annealing step). Metal-to-metal bond occurs during a subsequent batch annealing. The coefficient

**Fig. 8.12** ZiBond<sup>TM</sup> bond energy versus time

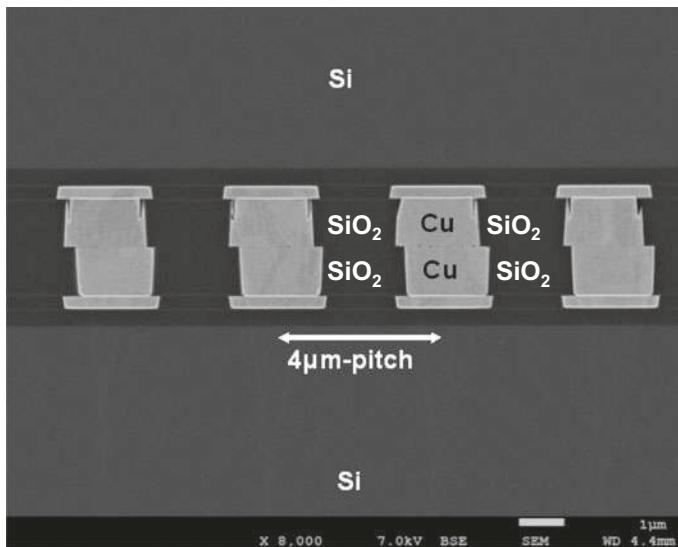


of thermal expansion of metals are typically far larger than dielectrics. The metal expands to fill the gap and then build up the internal pressure as shown in Fig. 8.11d. It is under this internal pressure and annealing temperature that metal atoms diffuse across the interface, making good metal-to-metal bond and hence electrical connection [18]. External pressure is optional for this type of bonding. In this case, the copper oxidation during bonding is minimized. Because the bonded oxide layer surrounding the copper interconnect protects the interconnect from oxidation in the annealing oven, thus minimizing Cu oxidation during the anneal. The bonded oxide surface also hermetically seals the Cu interconnect during operation.

The impact of CMP on DBI can be seen from Fig. 8.13 [18]. Figure 8.13a shows the bonding without optimized CMP. It can be seen that there is large seams (non-bonded SiO<sub>2</sub>–SiO<sub>2</sub> areas) and they are near the Cu bonding areas. Figure 8.13b shows the bonding with much flatter oxide by CMP and DBI design, which lead to minimize the occurrence of seams. Figure 8.13c shows the bond interface of optimal CMP and DBI design, which yield no visible seams. Optimizing the CMP condition is the key to produce the right amount of surface characteristics such as metal recess, dielectric



**Fig. 8.13** Cross-sectional SEM images of DBI. **a** Significant non-bonded SiO<sub>2</sub> area (seam) near the Cu pads. **b** Minimal seam during bond. **c** Optimized CMP DBI without visible seams [18]



**Fig. 8.14** SEM image of optimized CMP DBI

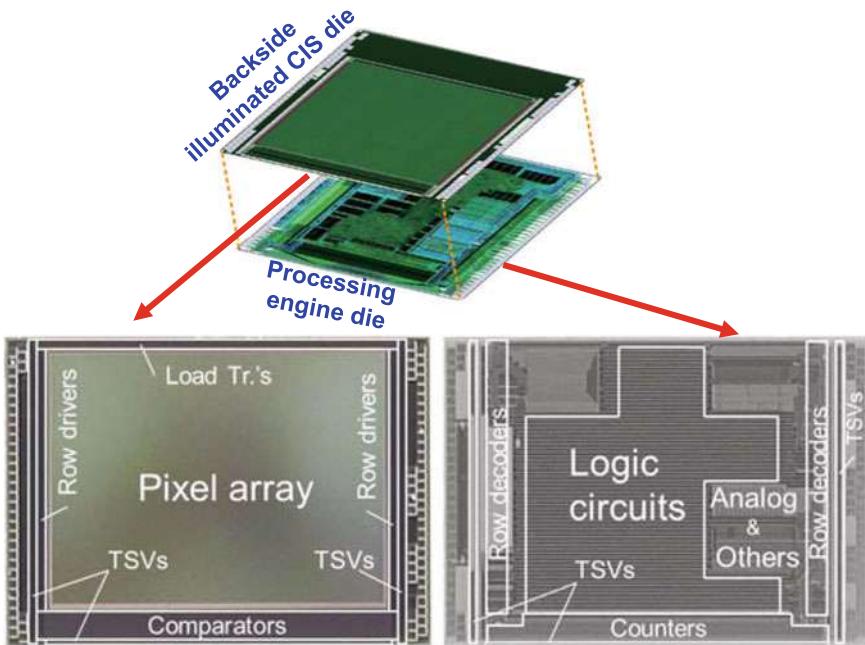
roughness, and dielectric curvature for DBI [18]. Figure 8.14 shows an optimal DBI with 4  $\mu\text{m}$ -pitch and 2  $\mu\text{m}$ -diameter pads.

### 8.5.2 Sony's CMOS Image Sensors (CIS) with TSVs

Sony's 3D (three-dimension) CMOS image sensors (CIS) at least have two versions, one is with TSV (through silicon via) and the other is without but with hybrid bonding.

Sony's CIS with TSV is shown in Fig. 8.15. It can be seen that the CIS consists of two chips, the CIS pixel chip and the logic circuit chip and they are vertically connected through TSVs (through-silicon vias) around their edges as shown in Fig. 8.15. The advantages of this design are that (a) more pixels can be placed on the same CIS pixel chip size (or smaller chip size can be used for the same amount of pixels) and (b) the CIS pixel chip and logic chip can be fabricated separately with different process technologies. As a result, the CIS chip size is reduced by 30% and the scaling of the logic circuit chip is increased from 500 to 2400 k gates [48].

The number of TSVs is in the order of thousands, including signals, power supplies, and grounds. There is no TSV in the pixel array area. The column TSVs are placed in between the comparators on the pixel CIS chip and the counters of the logic circuits chip. The row TSVs are placed in between the row drivers of the CIS chip and the row decoders of the logic chip (Fig. 8.15). These arrangements of the TSVs can reduce the influence of noise and make it easy to manufacture the CIS chip. For example, to reduce the influence of noise, comparators are arranged on the pixel



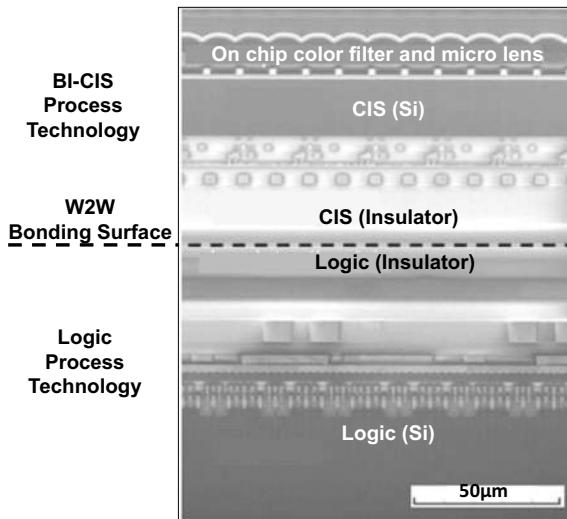
**Fig. 8.15** Sony 3D CIS pixel chip and logic IC integration with TSVs [48]

CIS chip, which can be manufactured by using Sony's matured process technology, rather than on the logic circuit chip.

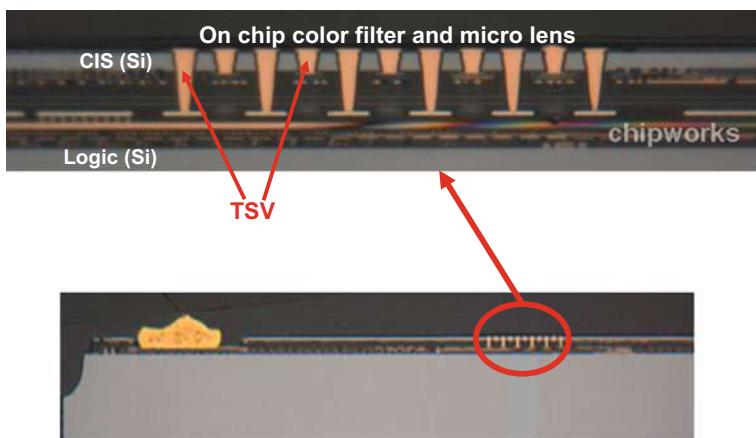
The CIS pixel chip is fabricated by the Sony conventional 1P4M BI-CIS (90 nm) process technology. The logic chip is fabricated by the matured 65 nm 1P7M logic process technology. The size of the pixel chip and the logic chip is about the same. The CIS Si-insulator of the CIS wafer is bonded to the logic Si-insulator of the logic wafer ( $\text{SiO}_2\text{-SiO}_2$  wafer-to-wafer Zibond). The TSVs are then formed and Cu filled after the bonding of the wafers. Figures 8.16 and 8.17 show the cross-section SEM (scanning electron microscopy) images of the 3D CIS pixel chip and logic IC chip integration. It can be seen that (a) the top part is the CIS chip, (b) the bottom part is the logic chip, (c) the CIS wafer and the logic wafer are insulator-to-insulator (wafer-to-wafer) bonding (Fig. 8.16), and (d) the CIS chip is connected to the logic chip through TSVs (Fig. 8.17).

### 8.5.3 Sony's CIS Without TSV (Hybrid Bonding)

Sony's CIS without TSV but with Hybrid bonding is shown in Figs. 8.18, 8.19 and 8.20. Sony is the first to use low temperature Cu–Cu DBI in high volume manufacturing [12, 13]. Sony produced the IMX260 backside illuminated CMOS image

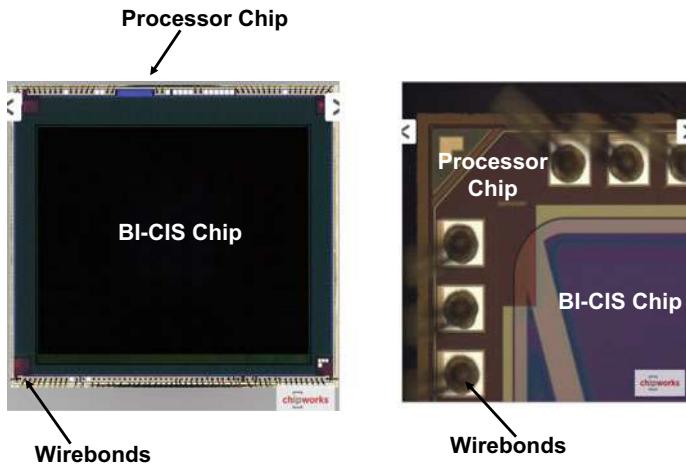


**Fig. 8.16** Sony CIS (insulator) wafer to logic (insulator) wafer bonding [48]

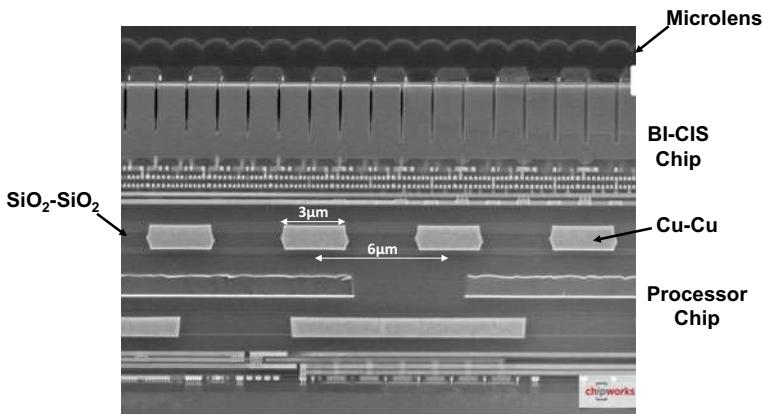


**Fig. 8.17** TSVs connecting the CIS pixel chip and the logic circuit chip [48]

sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results showed that their robust Cu–Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also super. A top view and cross section views of the IMX260 BI-CIS are shown in Figs. 8.18, 8.19 and 8.20, respectively. It can be seen that, unlike in [48] for Sony's ISX014 stacked camera sensor, the TSVs are eliminated and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu–Cu DBI. The signals are coming from the package substrate with wire bonds to the edges of the processor chip.



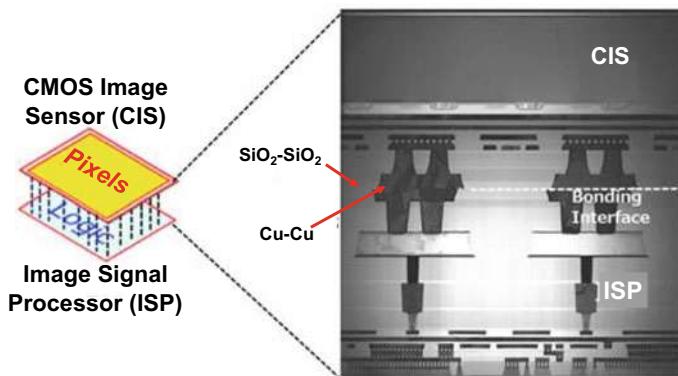
**Fig. 8.18** Sony 3D CIS and processor IC integration without TSVs [12]



**Fig. 8.19** SEM image of Sony 3D CIS and processor IC hybrid bonding [12]

Usually, wafer-to-wafer bonding is for the same chip size from both wafers. In Sony's case, the processor chip is slightly larger than the pixel chip. In order to perform wafer-to-wafer bonding, some of the area for the pixel wafer must be wasted. Also, since there are not TSVs in both chips, wire bonding on the processor chip is used to let the signals go to the next level of interconnects.

The assembly process of Cu–Cu DBI starts off with surface cleaning, metal oxide removal, and activation of  $\text{SiO}_2$  or  $\text{SiN}$  (by wet cleaning and dry plasma activation) of wafers for the development of high bonding strength. Then, use optical alignment to place the wafers in contact at room temperature and in a typical cleanroom atmosphere. The first thermal annealing ( $100\text{--}150^\circ\text{C}$ ) is designed to strengthen the bond



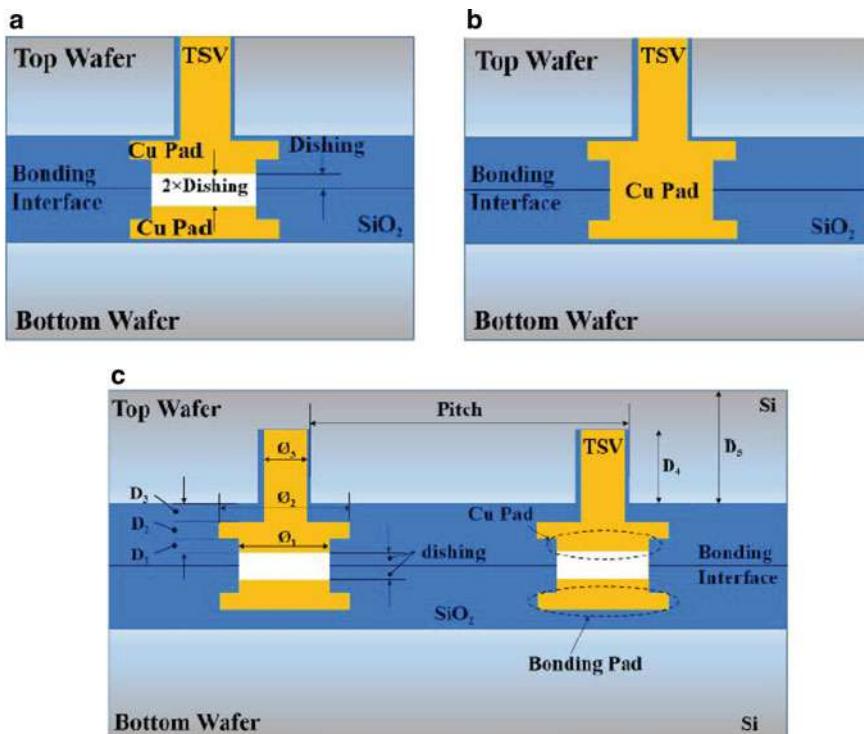
**Fig. 8.20** Cross-sectional schematic and view showing gap between Cu pads closed after annealing process [12]

between the SiO<sub>2</sub> or SiN surfaces of the wafers while minimizing the stress in the interface due to the thermal expansion mismatch among the Si, Cu, and SiO<sub>2</sub> or SiN. Then, apply higher temperature and pressure (300 °C, 25 kN, 10–3 Torr, N<sub>2</sub> atm) for 30 min to introduce the Cu diffusion at the interface and grain growth across the bond interface. The post-bond annealing is 300 °C under N<sub>2</sub> atm for 60 min. This process leads to the seam-less bonds (Figs. 8.19 and 8.20) formed for both Cu and SiO<sub>2</sub> or SiN at the same time.

## 8.6 Recent Developments of Low Temperature Hybrid Bonding

### 8.6.1 IME's Thermo-Mechanical Performance of Hybrid Bonding

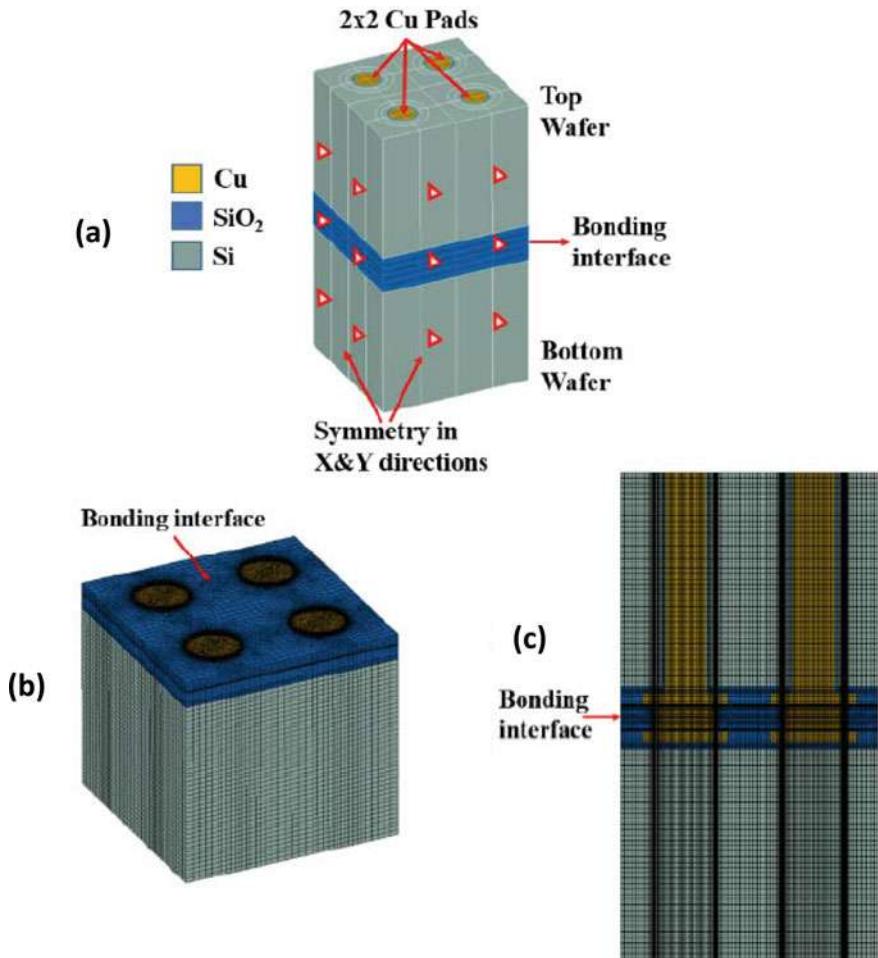
The common design and process parameters such as dishing value, annealing temperature and dwell duration, TSV pitch, and depth with regard to thermo-mechanical bonding performance have been studied in [19, 20]. The structure under thermo-mechanical simulation is shown in Fig. 8.21 and the important dimensions are shown in Table 8.1. The finite element model is shown in Fig. 8.22. It can be seen that a localized quarterly-symmetric finite element model including only 2 × 2 sets of Cu pads is proposed as shown in Fig. 8.22a. The mesh details are shown in Figs. 8.22b, c. The annealing temperature profile is shown in Fig. 8.23. All the parameters used in defining annealing temperature profile and dishing values used in surface treatment before annealing process are listed in Table 8.2. The material properties used in the



**Fig. 8.21** Cross-sectional view showing gap between Cu-pads: **a** before annealing and **b** after annealing. **c** Dimensions

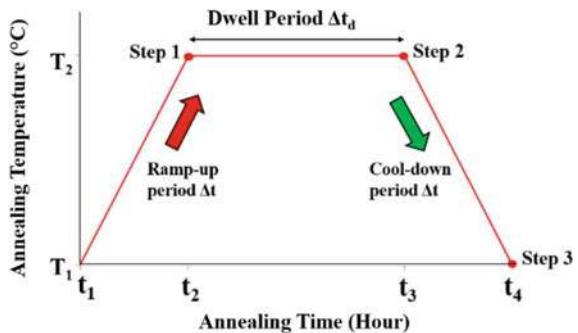
**Table 8.1** Design parameters used in WoW hybrid bonding simulations [20]

Design parameters	Values ( $\mu\text{m}$ )
Cu pad/bonding pad/TSV pitch	6, 9, 12
Cu pad diameter $\varphi_1$	3
Bonding pad diameter $\varphi_2$	4
TSV diameter $\varphi_3$	2
Cu pad thickness $D_1$	0.6
Bonding pad thickness $D_2$	0.6
SiO <sub>2</sub> layer thickness $D_3$	0.2
TSV depth $D_4$	5, 10, 15
Si thickness $D_5$	30



**Fig. 8.22** Finite element models. **a** FEA model. **b** Mesh (bottom half model). **c** Mesh (front view cross-section)

**Fig. 8.23** Hybrid bonding annealing temperature profile [20]



**Table 8.2** Process parameters used in WoW hybrid bonding simulations [20]

Process parameters	Values
Dishing	5, 10, 15 nm
Initial/End temperature $T_1$	25 °C
Annealing temperature $T_2$	300, 350, 400 °C
Ramp-up/Cool-down duration $\Delta t$	0.5 h
Annealing dwell duration $\Delta t_d$	1, 2, 3 h

**Table 8.3** Material properties used in WoW hybrid bonding simulations [20]

Materials	Young's modulus (GPa)	Poisson's ratio	CTE ( $10^{-6}/^\circ\text{C}$ )
Silicon	131	0.28	2.6
Copper	91.8	0.34	17.6
Dielectric (SiO <sub>2</sub> )	73	0.17	0.5

**Table 8.4** Copper plastic and creep material properties used in WoW hybrid bonding simulations [20]

Material properties	Value
Yield strength (MPa)	321
Tangent modulus (MPa)	2000
Creep constant 1	$1.43 \times 10^{10}$
Creep constant 2	2.5
Creep constant 3	-0.9
Creep constant 4	23695

simulations are presented in Table 8.3. Elastic-plastic-creep material properties for copper material are listed in Table 8.4 [20].

**Fig. 8.24** Effects of annealing temperature and dishing value on Cu–Cu bonding area [20]

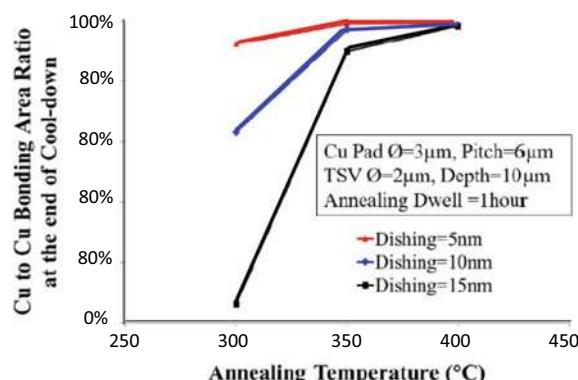
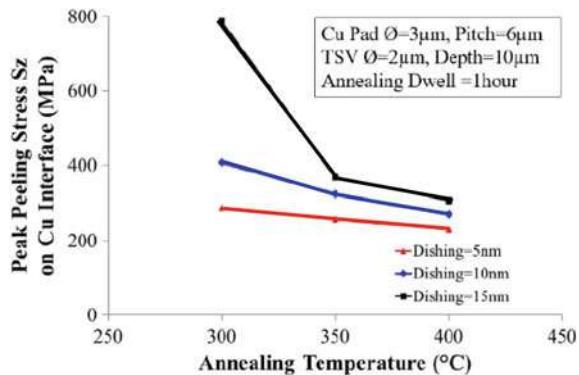


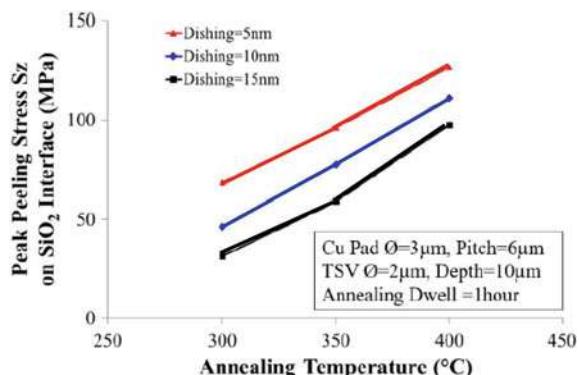
Figure 8.24 shows the effect of annealing temperature on Cu–Cu bonding area after annealing process with different dishing values. It can be seen that both annealing temperature and dishing value play a very important role in forming Cu–Cu bonding. The higher the annealing temperature ( $400\text{ }^{\circ}\text{C}$ ) and the smaller the dishing (5 nm) lead to a good Cu–Cu bonding ( $\geq 97\%$  copper pad area). It also can be seen from Fig. 8.24 that at a low annealing temperature ( $300\text{ }^{\circ}\text{C}$ ) the dishing effect is more critical than that at high annealing temperature such as  $\geq 350\text{ }^{\circ}\text{C}$  [20].

Similar findings are observed for peak peeling stresses on copper interfaces as shown in Fig. 8.25 [20]. The peak stress on Cu–Cu bonding interface decreases with higher annealing temperature and less dishing. This is in line with the trend for forming Cu–Cu bonding area. However, the trend is on the opposite side for the peeling stress on dielectric bonding interface as shown in Fig. 8.26. It can be seen that the higher annealing temperature and less dishing the higher the peak peeling stress on dielectric interface, which leads to higher chance of delamination or even crack in the dielectric layers.

**Fig. 8.25** Effects of annealing temperature and dishing value on peak peeling stress on Cu interfaces [20]



**Fig. 8.26** Effects of annealing temperature and dishing value on peak peeling stress on dielectric material ( $\text{SiO}_2$ ) bonding interfaces [20]

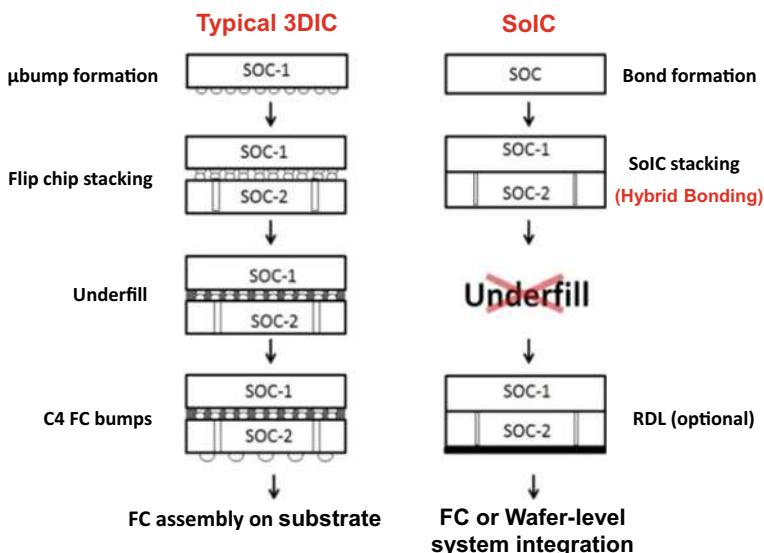


### 8.6.2 TSMC's Hybrid Bonding

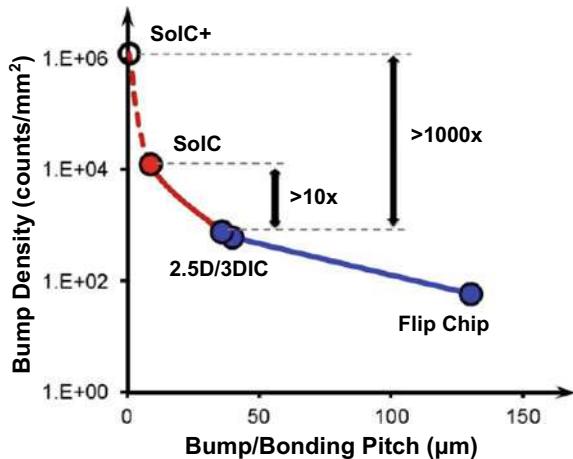
Figure 8.27 shows the TSMC's frontend SoIC (system on integrated chips) along with the conventional 3D IC integration with flip chip technology [21, 22]. It can be seen that the key difference between SoIC and 3D IC integration is that SoIC is bumpless and the interconnects between the chiplets is Cu–Cu hybrid bonding. The assembly process of SoIC can be either wafer-on-wafer (WoW), chip-on-wafer (CoW), or chip-on-chip (CoC) hybrid bonding. Figure 8.28 shows the bump density from various bonding assembly technologies such as flip chip, 2.5D/3D, SoIC, and SoIC+. It can be seen that SoIC can go down to ultra-fine pitch with extremely high density. Another advantage of SoIC is free of the CPI (chip-package-interaction) reliability issue from fine-pitch flip chip assembly.

The SoIC technology has a better electrical performance than the flip chip technology as shown in Fig. 8.29. (The SoIC chiplets are vertically hybrid bonded and the flip chips are 2D side-by-side assembled.) It can be seen that the insertion loss of SoIC technology is almost zero and is far smaller than that of the flip chip technology [21, 22] (Fig. 8.29).

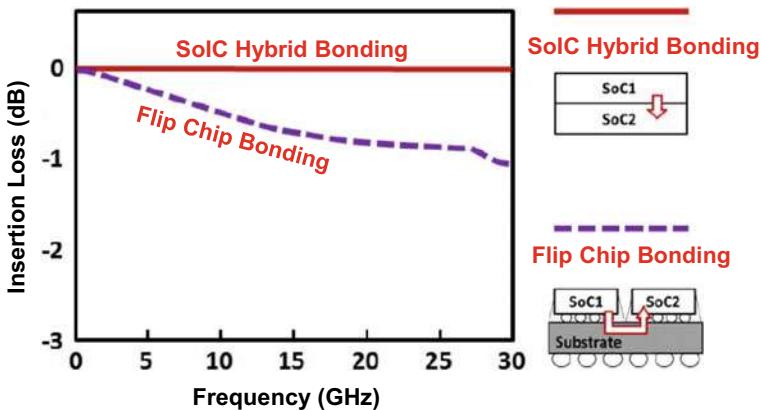
Figure 8.30a shows the backend TSMC's SoIC with CoWoS (chip-on-wafer-on-substrate) for very high density and performance such as high-performance computing (HPC) applications. Figure 8.30(b) shows the backend TSMC's SoIC with InFO\_PoP (integrated fan-out package-on-package) for mobile applications. In both applications, the SoIC is just like the conventional SoC (system-on-chip).



**Fig. 8.27** Comparison of integration flow between conventional 3D IC integration and SoIC integration [21]



**Fig. 8.28** Bump density versus bump/bonding pitch for flip chip, 2.5D/3D IC, and SoIC [21]

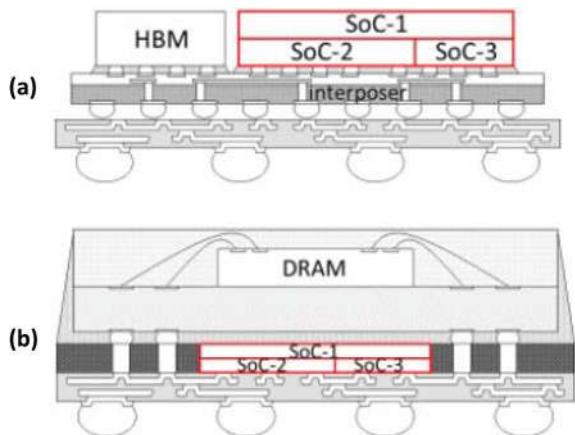


**Fig. 8.29** Insertion loss of SoIC and flip chip at various frequencies [21]

### 8.6.3 IMEC's Hybrid Bonding

Figure 8.31 shows IMEC's test vehicle with TSV (through silicon via) which is integrated in a unit cell of  $240 \times 240 \mu\text{m}^2$  for hybrid bonding [23–26]. The unit cells are arranged in an array of  $16 \times 16$  within the square die of  $4.32 \times 4.32 \text{ mm}$ . The variable size test chips can finally be diced from a wafer with the step of  $4.32 \text{ mm}$ . To enable face-to-face hybrid bonding, the wafer pairs received an additional surface finish, i.e.  $500 \text{ nm SiO}_2$  and  $120 \text{ nm SiCN}$ . The hybrid interface consists of  $0.54 \mu\text{m}$  square pads embedded into the dielectric of the top wafer and  $1.17 \mu\text{m}$  square pads plated on the bottom wafer as shown in the TEM (transmission electron microscopy)

**Fig. 8.30** **a** CoWoS with SoIC integration for high performance applications. **b** InFO\_PoP with SoIC integrating for mobile applications [21]



**Fig. 8.31** Schematic on the unit cell of the test chip [23]

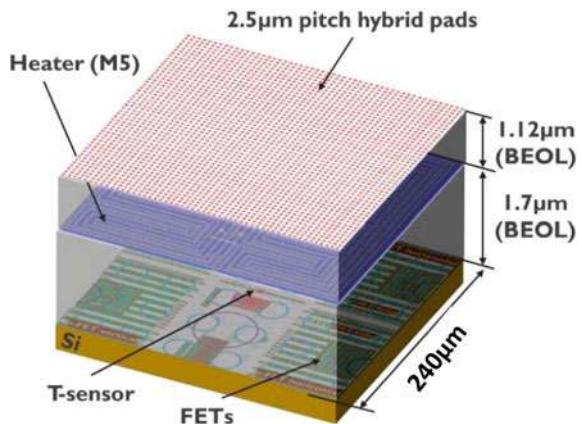
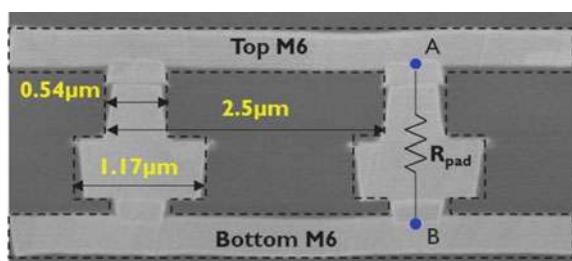
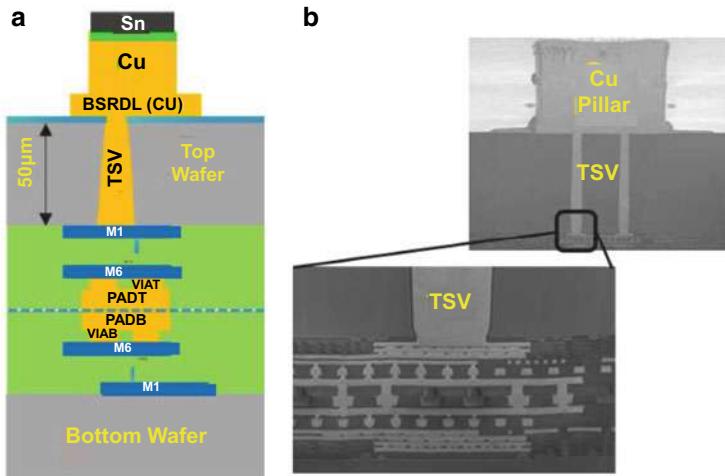


image in Fig. 8.32. The alignment and bonding are done at room temperature and with the following post-bond anneal at 250 °C for 2 h [23–26]. The cross section of the hybrid stack is shown in Fig. 8.33. The top wafer is thinned down to 50 μm to reveal the integrated (via-middle) through TSVs from the backside. The redistribution

**Fig. 8.32** TEM image of the hybrid bonding interface [23]



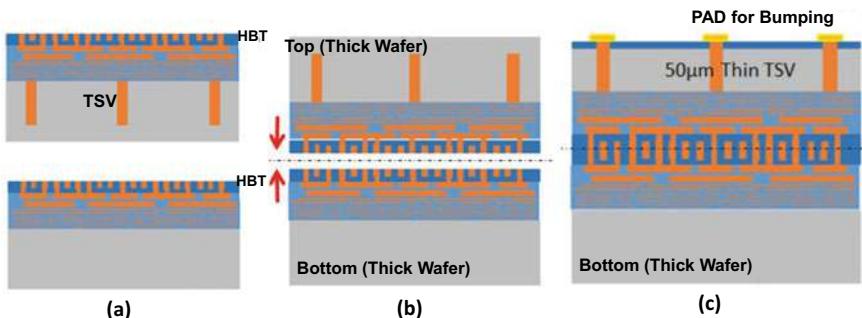


**Fig. 8.33** Hybrid bonding stack. **a** Schematic cross section view. **b** SEM images [23]

layer and the flip-chip pillars are processed on the back side of the top wafer to allow electrical measurements and to enable flip-chip assembly. For more information on thermal and mechanical reliability of the hybrid bonding, please read [23–26].

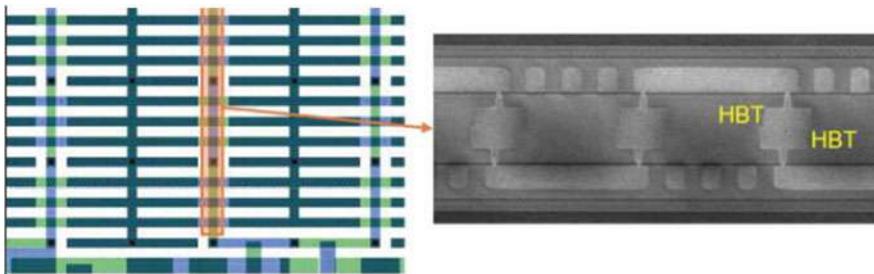
#### 8.6.4 Globalfoundries' Hybrid Bonding

Figure 8.34 shows Globalfoundries' hybrid bonding with TSVs [27]. Figure 8.34a shows the top wafer prepared in fab with TSV integration and separate wafer built without TSV integration. Both hybrid bond terminal (HBT) metals have matching

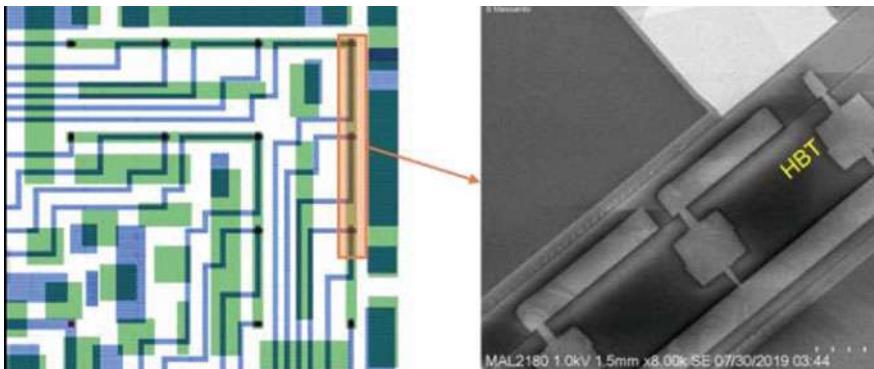


**Fig. 8.34** **a** Top wafer with TSV and bottom wafer without TSV. **b** Top and bottom wafers undergoing F2F bonding. **c** Revealed TSV (thinned) side is the bump/pad terminal side [27]

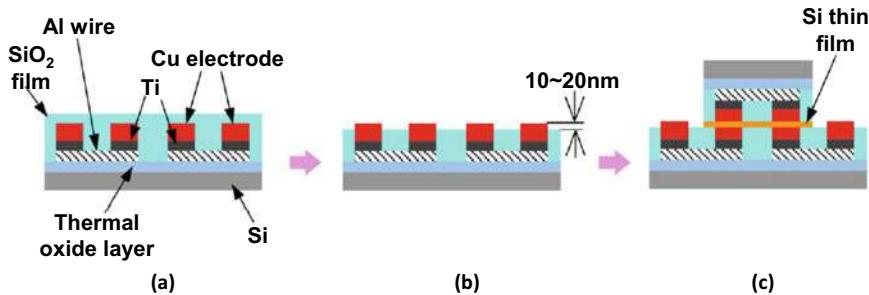
bonding surfaces. Figure 8.34b shows the top and bottom wafers undergoing face-to-face bonding. Incoming surface preparation is of great importance for the hybrid wafer bonding (HWB) step. Surface flatness is the key to avoiding bonding voids, which could result in poor bond strength and terminal conductivity. The shape correction plays a vital role in alignment of the copper terminal pads [27]. Both wafers are full thickness at this point in the process flow. Figure 8.34c shows the final wafer stack cross-sectional drawing after backside pad metal step. Revealed TSV (thinned) side is the bump/pad side. Figures 8.35 and 8.36 show the design and cross sections of the test vehicle near the hybrid bonding interfaces. Figure 8.35 shows the via chain macro and cross section of via chain at hybrid wafer bonding interface, while Fig. 8.36 show the single contact macro design and cross section of the single contact at hybrid wafer bonding interface. For some reliability test results, please read [27].



**Fig. 8.35** Via chain macro design and cross section of via chain at hybrid wafer bonding interface [27]



**Fig. 8.36** Single contact macro design and cross section of the single contact at hybrid wafer bonding interface [27]



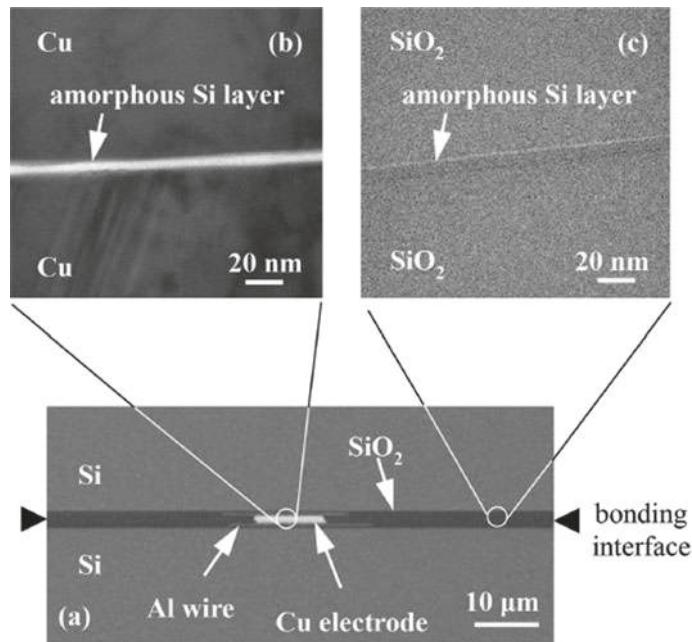
**Fig. 8.37** Key process steps for Cu/SiO<sub>2</sub> hybrid bonding: **a** Before, **b** after CMP process and the deference in level between Cu electrode and SiO<sub>2</sub> is 10–20 nm, and **c** the bonded wafers using the Si thin film [28]

### 8.6.5 Mitsubishi's Hybrid Bonding

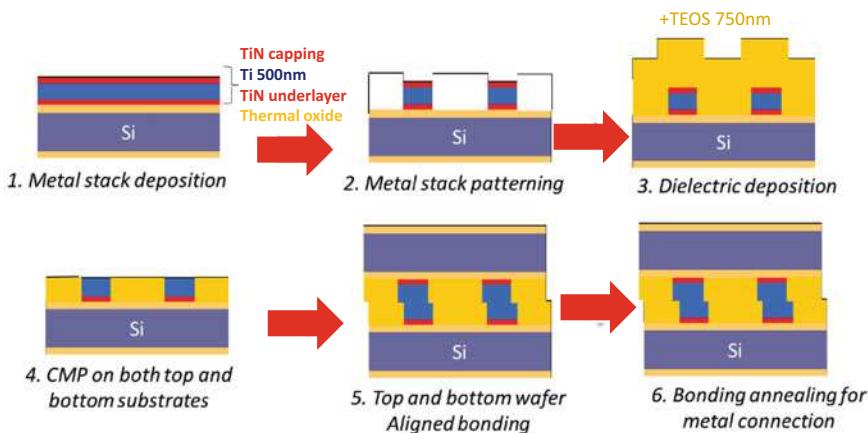
The key process steps of Mitsubishi's hybrid bonding is shown in Fig. 8.37 [28]. It can be seen that the Cu electrode, SiO<sub>2</sub>, Ti, and Al-wire of the wafer before CMP is shown in Fig. 8.37a. Figure 8.37b shows the structure after CMP. The deference in level between Cu electrode and SiO<sub>2</sub> is 10 to 20 nm. Figure 8.37c shows the bonded wafers using a Si thin film. The bonding is between a 6" test-element-group (TEG) wafer and an 8" TEG wafer. The surface of the wafers is activating through an Ar fast atom beam (FAB). A Si thin film is deposited on the lower 6" TEG wafer surface at a rate of approximately 0.4 nm/min. The total thickness of the Si thin film is estimated to be approximately 4 nm after the bonding. The 8-in and 6-in TEG wafers are then brought into contact with a bonding compression force of 10,000 kgf after alignment with very high accuracy. All of the Ar-FAB irradiation processes are performed at a background vacuum pressure smaller than approximately  $5 \times 10^{-6}$  Pa [28]. Figure 8.38 shows the hybrid bonding results. Figure 8.38a shows a SEM cross-sectional image of the bonded Cu/SiO<sub>2</sub> hybrid interface. There are no seams or gaps can be observed in the cross-section, and the alignment error is estimated to be approximately 1  $\mu$ m. Figure 8.38b shows a TEM cross-sectional image of the interface of the bonded Cu/Cu electrodes, and Fig. 8.38c shows a TEM cross-sectional image of the bonded SiO<sub>2</sub>/SiO<sub>2</sub> interface. At both bonding interfaces, there are no micro voids are observed. However, there is an intermediate layer with a thickness of approximately 5 nm. The layer is assumed to be amorphous Si layers.

### 8.6.6 Leti's Hybrid Bonding

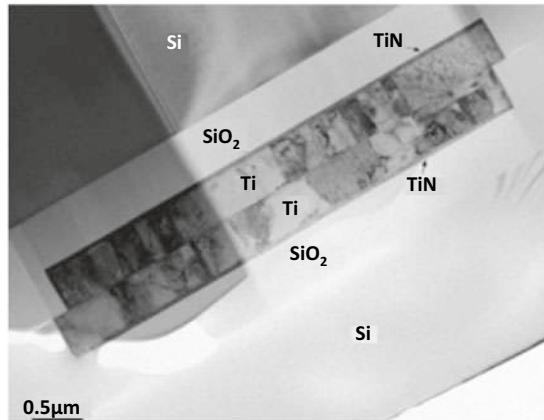
Figure 8.39 shows the key process steps of Leti's hybrid bonding [29]. Their Ti/SiO<sub>2</sub> hybrid bonding is developed on a 200 mm non-functional short loop wafers. Figure 8.39 (1) shows the metal pattern preparation. First a TiN is deposited as a



**Fig. 8.38** **a** SEM cross-sectional image of the bonded Cu/SiO<sub>2</sub> hybrid interface. **b** TEM cross-sectional image of the interface of the bonded Cu/Cu electrodes. **c** TEM cross-sectional image of the bonded SiO<sub>2</sub>/SiO<sub>2</sub> interface [28]



**Fig. 8.39** Ti/TEOS hybrid 3D interconnection process flow [29]

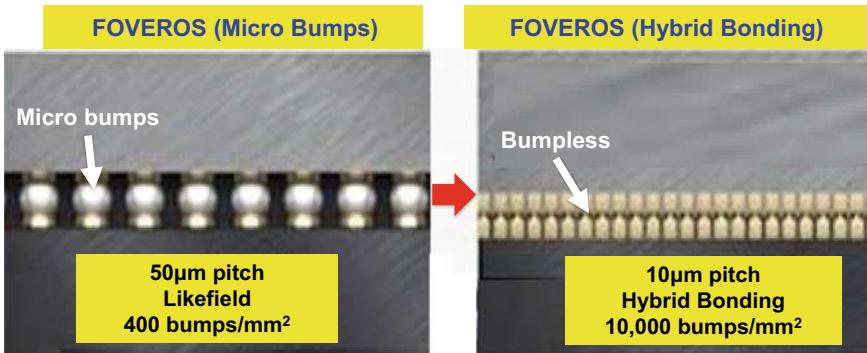


**Fig. 8.40** TEM cross section of Ti/SiO<sub>2</sub> hybrid bonding interface [29]

barrier layer. Then, a Ti layer (500 nm) is deposited by sputtering. Finally, the Ti is capped by a thin TiN layer. Figure 8.39 (2) shows the metal stack patterning. Figure 8.39 (3) shows the dielectric deposition. After patterning, the pads are encapsulated by a tetraethylorthosilicate (TEOS) oxide. After the TEOS oxide deposition, an annealing step is applied for two reasons: (i) for densification of the dielectric and (ii) to eliminate the water molecules absorbed in the dielectric layer in order to prevent future bonding void formation by outgassing. Figure 8.39 (4) shows the CMP for the planarization and surface preparation of the wafers. For Ti/SiO<sub>2</sub> planarization the CMP process starts with the SiO<sub>2</sub> removal and stops in the final Ti/SiO<sub>2</sub> hybrid surface. The topography measurement are carried out by white-light interferometry (WLI) and oxide surface roughness by atomic force microscopy (AFM) indicating excellent surface planarity and roughness [29]. Figure 8.39 (5) shows the top and bottom wafers bonding. Figure 8.39 (6) shows the annealing for metal connection. Finally, the bonded wafers were annealed at 400 °C for two hours in order to ensure a proper metal/metal connection. The bonding interface quality is locally assessed with focused ion beam scanning electron microscopy (FIB-SEM) and transmission electron microscopy (TEM). Figure 8.40 shows the TEM image which demonstrates an excellent Ti/Ti connection and there is not seams in the metal and dielectric interfaces [29].

### 8.6.7 Intel's Hybrid Bonding

During Intel Architecture Day (August 13, 2020), Intel presented a hybrid bonding technology with their FOVEROS along with the conventional microbump flip chip technology as shown in Fig. 8.41. It can be seen that with the hybrid bonding tech-



**Fig. 8.41** Intel's FOVEROS hybrid bonding

nology the pad pitch can go down to  $10\text{ }\mu\text{m}$  and with  $10,000$  bumpless interconnects per  $\text{mm}^2$ . This is many times more than the one with  $50\text{ }\mu\text{m}$ -pitch microbump flip chip technology.

## 8.7 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- Some fundamentals of low temperature DBI (hybrid bonding) have been provided.
- Some new developments on hybrid bonding have also been briefly mentioned.
- Due to different chip size and wafer yield, chip-to-wafer (CoW) hybrid bonding is another way to go and improves assembly yield.
- So far, Sony's BI-CSI is the only HVM product using WoW bumpless hybrid bonding.
- In order to have more HVM products using the bumpless hybrid bonding technology, more research and development efforts should be placed on areas such as:
  - Cost reduction
  - Nanoscale topography (CMP)
  - Thin-wafer handling
  - Design parameter optimization
  - Process parameter optimization
  - Bonding environment
  - CoW and WoW bonding alignment
  - Wafer distortion and warpage
  - Inspection and testing
  - Contact integrity
  - Contact quality and reliability

- Manufacturing yield
- Manufacturing throughput
- Thermal management.

## References

1. Kim, B., T. Matthias, M. Wimplinger, P. Kettner, and P. Lindner, “Comparison of Enabling Wafer Bonding Techniques for TSV Integration”, *ASME Paper No. IMECE2010-400002*.
2. Chen, K., S. Lee, P. Andry, C. Tsang, A. Topop, Y. Lin, Y., J. Lu, A. Young, M., Jeong, and W. Haensch, W., “Structure, Design and Process Control for Cu Bonded Interconnects in 3D Integrated Circuits”, *IEEE Proceedings of International Electron Devices Meeting*, (IEDM 2006), San Francisco, CA, December 11–13, 2006, pp. 367-370.
3. Liu, F., Yu, R., Young, A., Doyle, J., Wang, X., Shi, L., Chen, K., Li, X., Dipaola, D., Brown, D., Ryan, C., Hagan, J., Wong, K., Lu, M., Gu, X., Klymko, N., Perfecto, E., Merryman, A., Kelly K., Purushothaman, S., Koester, S., Wisniewff, R., and Haensch, W., “A 300- Wafer-Level Three-Dimensional Integration Scheme Using Tungsten Through-Silicon Via and Hyprid Cu-Adhesive Bonding”, *IEEE Proceedings of IEDM*, December 2008, pp. 1–4.
4. Yu, R., Liu, F., Polastre, R., Chen, K., Liu, X., Shi, L., Perfecto, E., Klymko, N., Chace, M., Shaw, T., Dimilia, D., Kinser, E., Young, A., Purushothaman, S., Koester, S., and Haensch W., “Reliability of a 300-mm-compatible 3DI Technology Base on Hybrid Cu-adhesive Wafer Bonding”, *Proceedings of Symposium on VLSI Technology Digest of Technical Papers*, 2009, pp. 170–171.
5. Shigetou, A. Itoh, T., Sawada, K., and Suga, T., “Bumpless Interconnect of 6-um pitch Cu Electrodes at Room Temperature”, In *IEEE Proceedings of ECTC*, Lake Buena Vista, FL, May 27–30, 2008, pp. 1405-1409.
6. Tsukamoto, K., E. Higurashi, and T. Suga, “Evaluation of Surface Microroughness for Surface Activated Bonding”, *Proceedings of IEEE CPMT Symposium Japan*, August 2010,, pp. 147–150.
7. Kondou, R., C. Wang, and T. Suga, “Room-temperature Si-Si and Si-SiN wafer bonding”, *Proceedings of IEEE CPMT Symposium Japan*, August 2010,, pp. 161–164.
8. Shigetou, A. Itoh, T., Matsuo, M., Hayasaka, N., Okumura, K., and Suga, T., “Bumpless Interconnect Through Ultrafine Cu Electrodes by Mans of Surface-Activated Bonding (SAB) Method”, *IEEE Transaction on Advanced Packaging*, Vol. 29, No. 2, May 2006, pp. 226.
9. Wang, C., and Suga, T., “A Novel Moire Fringe Assisted Method for Nanoprecision Alignment in Wafer Bonding”, In *IEEE Proceedings of ECTC*, San Diego, CA, May 25–29, 2009, pp. 872–878.
10. Wang, C., and Suga, T., “Moire Method for Nanoprecision Wafer-to-Wafer Alignment: Theory, Simulation and Application”, *IEEE Proceedings of Int. Conference on Electronic Packaging Technology & High Density Packaging*, August 2009, pp. 219–224.
11. Higurashi, E., Chino, D., Suga, T., and Sawada, R., “Au-Au Surface-Activated Bonding and Its Application to Optical Microsensors with 3-D Structure”, *IEEE Journal of Selected Topic in Quantum Electronics*, Vol. 15, No. 5 September/October 2009, pp. 1500–1505.
12. Kagawa, Y., N. Fujii, K. Aoyagi, Y. Kobayashi, S. Nishi, N. Todaka, et al., “Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding,” *Proceedings of IEEE/IEDM*, Dec. 2016, pp. 8.4.1–4.

13. Kagawa, Y., N. Fujii, K. Aoyagi, Y. Kobayashi, S. Nishi, N. Todaka, S. Takeshita, J. Taura, H. Takahashi, Y. Nishimura, et al., “An Advanced CuCu Hybrid Bonding for Novel Stack CMOS Image Sensor”, *IEEE/EDTM Proceedings*, March 2018, pp. 1–3.
14. Gao, G., L. Mirkarimi, G. Fountain, T. Workman, J. Theil, and G. Guevara, C. Uzoh, D. Suwito, B. Lee, K. Bang, and R. Katkar, “Die to Wafer Stacking with Low Temperature Hybrid Bonding”, *IEEE/ECTC Proceedings*, May 2020, pp. 589–594.
15. Gao, G., L. Mirkarimi, T. Workman, G. Fountain, J. Theil, G. Guevara, P. Liu, B. Lee, P. Mrozek, M. Huynh, C. Rudolph, T. Werner, and A. Hanisch, “Low Temperature Cu Interconnect with Chip to Wafer Hybrid Bonding”, *IEEE/ECTC Proceedings*, May 2019, pp. 628–635.
16. Gao, G., T. Workman, L. Mirkarimi, G. Fountain, J. Theil, G. Guevara, C. Uzoh, B. Lee, P. Liu, and P. Mrozek, “Chip to Wafer Hybrid Bonding with Cu Interconnect: High Volume Manufacturing Process Compatibility Study”, *IWLPC Proceedings*, October 2019, pp. 1–9.
17. Gao, G., L. Mirkarimi, T. Workman, G. Guevara, J. Theil, C. Uzoh, G. Fountain, B. Lee, P. Mrozek, M. Huynh, and R. Katkar, “Development of Low Temperature Direct Bond Interconnect Technology for Die-to-Wafer and Die-to-Die Applications – Stacking, Yield Improvement, Reliability Assessment”, *IWLPC Proceedings*, October 2018, pp. 1–7.
18. Lee, B., P. Mrozek, G. Fountain, J. Posthill, J. Theil, G. Gao, R. Katkar, and L. Mirkarimi, “Nanoscale Topography Characterization for Direct Bond Interconnect”, *IEEE/ECTC Proceedings*, May 2019, pp. 1041–1046.
19. Ji, L., F. Che, H. Ji, H. Li, and M. Kawano, “Modelling and characterization on wafer to wafer hybrid bonding technology for 3D IC packaging”, *IEEE/EPTC Proceedings*, December 2019, pp. 87–94.
20. Ji, L., F. Che, H. Ji, H. Li, and M. Kawano, “Bonding integrity enhancement in wafer to wafer fine pitch hybrid bonding by advanced numerical modeling”, *IEEE/ECTC Proceedings*, May 2020, pp. 568–575.
21. Chen, M. F., C. S. Lin, E. B. Liao, W. C. Chiou, C. C. Kuo, C. C. Hu, C. H. Tsai, C. T. Wang and D. Yu, “SoIC for Low-Temperature, Multi-Layer 3D Memory Integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.
22. Chen, F., M. Chen, W. Chiou, D. Yu, “System on Integrated Chips (SoIC<sup>TM</sup>) for 3D Heterogeneous Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 594–599.
23. Cherman, V., S. Van Huylenbroeck, M. Lofrano, X. Chang, H. Oprins, M. Gonzalez, G. Van der Plas, G. Beyer, K. Rebibis, and E. Beyne, “Thermal, Mechanical and Reliability assessment of Hybrid bonded wafers, bonded at 2.5  $\mu\text{m}$  pitch”, *IEEE/ECTC Proceedings*, May 2020, pp. 548–553.
24. Kennes, K., A. Phommahaxay, A. Guerrero, O. Bauder, S. Suhard, P. Bex, S. Iacovo, X. Liu, T. Schmidt, G. Beyer, and E. Beyne, “Introduction of a New Carrier System for Collective Die-to-Wafer Hybrid Bonding and Laser-Assisted Die Transfer”, *IEEE/ECTC Proceedings*, May 2020, pp. 296–302.
25. Huylenbroeck, S., J. De Vos, Z. El-Mekki, G. Jamieson, N. Tutunjyan, K. Muga, M. Stucchi, A. Miller, G. Beyer, and E. Beyne, “A Highly Reliable 1.4  $\mu\text{m}$  pitch Via-last TSV Module for Wafer-to-Wafer Hybrid Bonded 3D-SOC Systems”, *IEEE/ECTC Proceedings*, May 2019, pp. 1035–1040.
26. Suhard, S., A. Phommahaxay, K. Kennes, P. Bex, F. Fodor, M. Liebens, J. Slabbekoorn, A. A. Miller, G. Beyer, and E. Beyne, “Demonstration of a collective hybrid die-to-wafer integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 1315–1321.
27. Fisher, D., S. Knickerbocker, D. Smith, R. Katz, J. Garant, J. Lubguban, V. Soler, and N. Robson, “Face to Face Hybrid Wafer Bonding for Fine Pitch Applications”, *IEEE/ECTC Proceedings*, May 2019, pp. 595–600.
28. Utsumi, J., K. Ide, and Y. Ichiyanagi, “Cu/SiO<sub>2</sub> hybrid bonding obtained by surface-activated bonding method at room temperature using Si ultrathin films”, *Micro and Nano Engineering*, February 2019, pp. 1–6.
29. Jouve, A., E. Lagoutte1, R. Crochemore1, G. Mauguen1, T. Flahaut1, C. Dubarry1, V. Balan, F. Fournel, E. Bourjot, F. Servant1, M. Scannell1, K. Rohracher, T. Bodner, A. Faes, and J. Hofrichter, “A reliable copper-free wafer level hybrid bonding technology for high-performance medical imaging sensors”, *IEEE/ECTC Proceedings*, May 2020, pp. 201–209.

30. Jani, I., D. Lattard, P. Vivet, L. Arnaud, S. Cheramy, E. Beigné, Alexis Farcy, Joris Jourdon, Y. Henrion, E. Deloffre, and H. Bilgen, "Characterization of fine pitch Hybrid Bonding pads using electrical misalignment test vehicle", *IEEE/ECTC Proceedings*, May 2019, pp. 1926–1932.
31. Chong, S., X. Ling, H. Li, and S. Lim, "Development of Multi-Die Stacking with Cu–Cu interconnects using Gang Bonding Approach", *IEEE/ECTC Proceedings*, May 2020, pp. 188–193.
32. Chong, S., and S. Lim, "Comprehensive Study of Copper Nano-paste for Cu–Cu Bonding", *IEEE/ECTC Proceedings*, May 2019, pp. 191–196.
33. Araki, N., S. Maetani, Y. Kim, S. Kodama, and T. Ohba, "Development of Resins for Bumpless Interconnects and Wafer-On-Wafer (WOW) Integration", *IEEE/ECTC Proceedings*, May 2019, pp. 1002–1008.
34. Fujino, M., K.Takahashi, Y. Araga, and K. Kikuchi, "300 mm wafer-level hybrid bonding for Cu/interlayer dielectric bonding in vacuum", *Japanese J. Appl. Phys.* Vol. 59, February 2020, pp. 1–8.
35. Kim, S., P. Kang, T. Kim, K. Lee, J. Jang, K. Moon, H. Na, S. Hyun, and K. Hwang, "Cu Microstructure of High Density Cu Hybrid Bonding Interconnection", *IEEE/ECTC Proceedings*, May 2019, pp. 636–641.
36. Tong, Q., G. Fountain, and P. Enquist, "Method for Low Temperature Bonding and Bonded Structure", *US 6,902,987 B1*, filed on February 16, 2000, granted on June 7, 2005.
37. Tong, Q., G. Fountain, and P. Enquist, "Method for Low Temperature Bonding and Bonded Structure", *US 7,387,944 B2*, filed on August 14, 2005, granted on June 17, 2008.
38. Burns, J., Aull, B., Keast, C., Chen, C., Chen, C., Keast, C., Knecht, J., Suntharalingam, V., Warner, K., Wyatt, P., and Yost, D., "A Wafer-Scale 3-D Circuit Integration Technology", *IEEE Transactions on Electron Devices*, Vol. 53, No. 10, October 2006, pp. 2507–2516.
39. Chen, C., Warner, K., Yost, D., Knecht, J., Suntharalingam, V., Chen, C., Burns, J., and Keast, C., "Sealing Three-Dimensional SOI Integrated-Circuit Technology", *IEEE Proceedings of Int. SOI Conference*, 2007, pp. 87–88.
40. Chen, C., Chen, C., Yost, D., Knecht, J., Wyatt, P., Burns, J., Warner, K., Gouker, P., Healey, P., Wheeler, B., and Keast, C., "Three-dimensional integration of silicon-on-insulator RF amplifier", *Electronics Letters*, Vol. 44, No. 12, June 2008, pp. 1–2.
41. Chen, C., Chen, C., Yost, D., Knecht, J., Wyatt, P., Burns, J., Warner, K., Gouker, P., Healey, P., Wheeler, B., and Keast, C., "Wafer-Scale 3D Integration of Silicon-on-Insulator RF Amplifiers", *IEEE Proceedings of Silicon Monolithic IC in RF Systems*, 2009, pp. 1–4.
42. Chen, C., Chen, C., Wyatt, P., Gouker, P., Burns, J., Knecht, J., Yost, D., Healey, P., and Keast, C., "Effects of Through-BOX Vias on SOI MOSFETs", *IEEE Proceedings of VLSI Technology, Systems and Applications*, 2008, pp. 1–2.
43. Chen, C., Chen, C., Burns, J., Yost, D., Warner, K., Knecht, J., Shibles, D., and Keast, C., "Thermal Effects of Three Dimensional Integrated Circuit Stacks", *IEEE Proceedings of Int. SOI Conference*, 2007, pp. 91–92.
44. Aull, B., Burns, J., Chen, C., Felton, B., Hanson, H., Keast, C., Knecht, J., Loomis, A., Renzi, M., Soares, A., Suntharalingam, V., Warner, K., Wolfson, D., Yost, D., and Young, D., "Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers", *IEEE Proceedings of Int. Solid-State Circuits Conference*, 2006, pp. 16.9.
45. Chatterjee, R., Fayolle, M., Leduc, P., Pozder, S., Jones, B., Acosta, E., Charlet, B., Enot, T., Heitzmann, M., Zussy, M., Roman, A., Louveau, O., Maitrequean, S., Louis, D., Kernevez, N., Sillon, N., Passemard, G., Pol, V., Mathew, V., Garcia, S., Sparks, T., and Huang, Z., "Three dimensional chip stacking using a wafer-to-wafer integration", *IEEE Proceedings of IITC*, 2007, pp. 81–83.
46. Ledus, P., Crecy, F., Fayolle, M., Fayolle, M., Charlet, B., Enot, T., Zussy, M., Jones, B., Barbe, J., Kernevez, N., Sillon, N., Maitrequean, S., Louis, D., and Passemard, G., "Challenges for 3D IC integration: bonding quality and thermal management", *IEEE Proceedings of IITC*, 2007, pp. 210–212.

47. Poupon, G., Sillon, N., Henry, D., Gillot, C., Mathewson, A., Cioccio, L., Charlet, B., Leduc, P., Vinet, M., and Batude, P., "System on Wafer: A New Silicon Concept in SiP", *Proceedings of the IEEE*, Vol. 97, No. 1, January 2009, pp. 60–69.
48. Sukegawa, S., T. Umebayashi, T. Nakajima, H. Kawanobe, K. Koseki, I. Hirota, T. Haruta, et al., "A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor," *Proceedings of IEEE/ISSCC*, San Francisco, CA, February 2013, pp. 484–486.

# Chapter 9

## Chiplet Heterogeneous Integration



### 9.1 Introduction

Recently, heterogeneous integration of chiplets (chiplet heterogeneous integration or heterogeneous chiplet integration) is getting lots of tractions [1–18]. Microprocessors such as AMD’s EPYZ and Intel’s Lakefield are in high volume manufacturing with chiplet designs and heterogeneous integration packaging technology. They will be discussed in this chapter. The definition and advantages/disadvantages of chiplet heterogeneous integration will also be briefly presented. Defense advanced research projects agency (DARPA)’s efforts in chipet heterogeneous integration and System-on-chip (SoC) versus chiplet heterogeneous integration will be briefly mentioned first.

### 9.2 DARPA’s Efforts in Chipet Heterogeneous Integration

DARPA has been making very good progress on heterogeneous integration in more than 15 years with more than 30 first-tire companies such as Intel, Micron, Cadence, Synopsys, Lockheed Martin, Northrop Grumman, Michigan University, and Georgia Institute of Technology, and their key programs in heterogeneous integration are briefly mentioned.

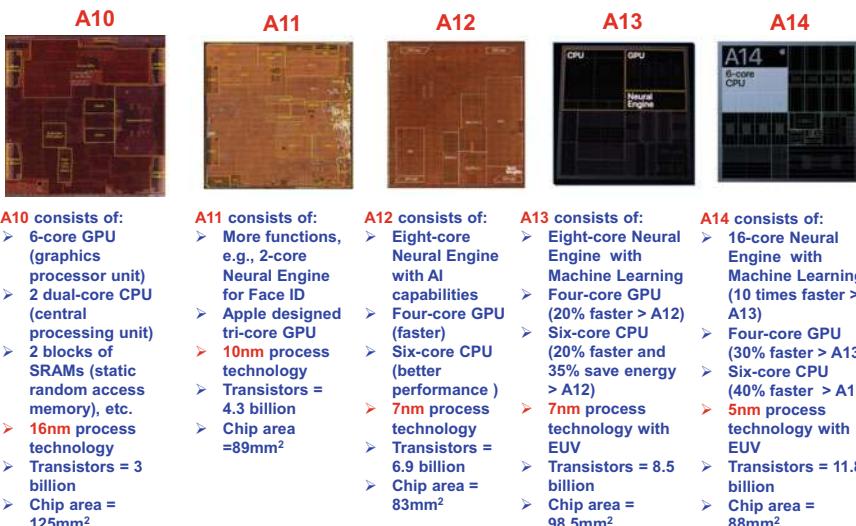
DARPA’s first effort on heterogeneous integration is the COSMOS (compound semiconductor materials on silicon) program [19] which started in May 2007. COSMOS developed three unique approaches to the heterogeneous integration of (indium phosphide) (heterojunction bipolar transistors) with deep submicron Si (complementary metal-oxide semiconductor). COSMOS is now a diverse accessible heterogeneous integration (DAHI) program [20] thrust. The DAHI program is developing the following key technical challenges: (1) heterogeneous integration process development, (2) high-yield manufacturing and foundry establishment, and (3) circuit design and architecture innovation.

DARPA started the CHIPS (common heterogeneous integration and IP (Intellectual Property) reuse strategies) program [21] in 2017. The aim of the CHIPS program is to make modular computers out of chiplets. The CHIPS program is addressing integration standards, IP blocks, and design tools. Intel is providing a royalty-free license for their advanced interface bus technology to CHIPS program participants.

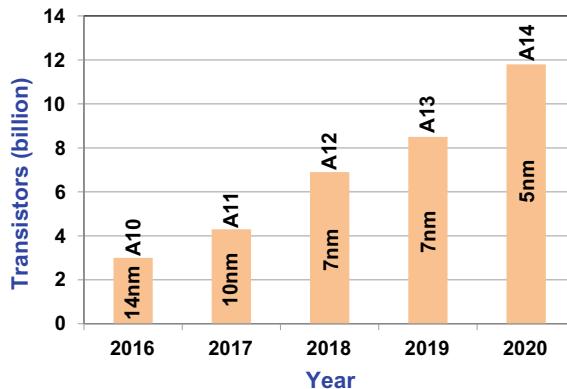
Navy proposed a state-of-the-art heterogeneous integrated packaging (SHIP) program [22] in the mid-2019. The primary objective of the SHIP project will be to demonstrate a novel approach to a secure, assessable, and cost-effective state-of-the-art integrated, design, assembly, and test leveraging the expertise of commercial industry. Designs must also adhere to the interface standards developed under the DARPA CHIPS program to ensure proper insertion and testability of the final product.

### 9.3 SoC (System-on-Chip)

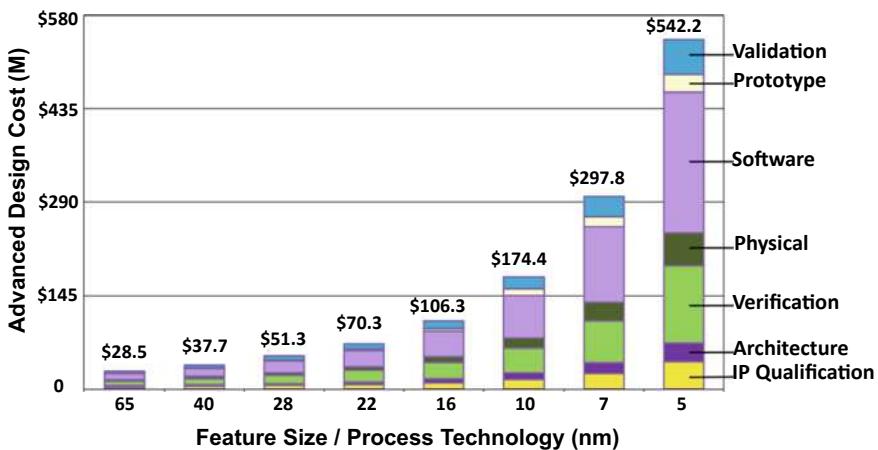
As mentioned in Chap. 2, SoC integrates ICs with different functions such as CPU (central processing unit), GPU (graphic processing unit), memory, etc. into a single chip for the system or subsystem. The most famous SoC is Apple's application processors (AP), which are simply shown in Fig. 9.1 for A10 through A14. The number of transistor versus year with various feature size (process technology) is shown in Fig. 9.2. It can be seen the power of Moore's law, which increases the number of transistors and functionalities with a reduction of feature size. Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to



**Fig. 9.1** Apple's application processors (SoC)



**Fig. 9.2** Transistors versus years with various feature sizes for Apple's APs



**Fig. 9.3** Advanced design cost versus feature size

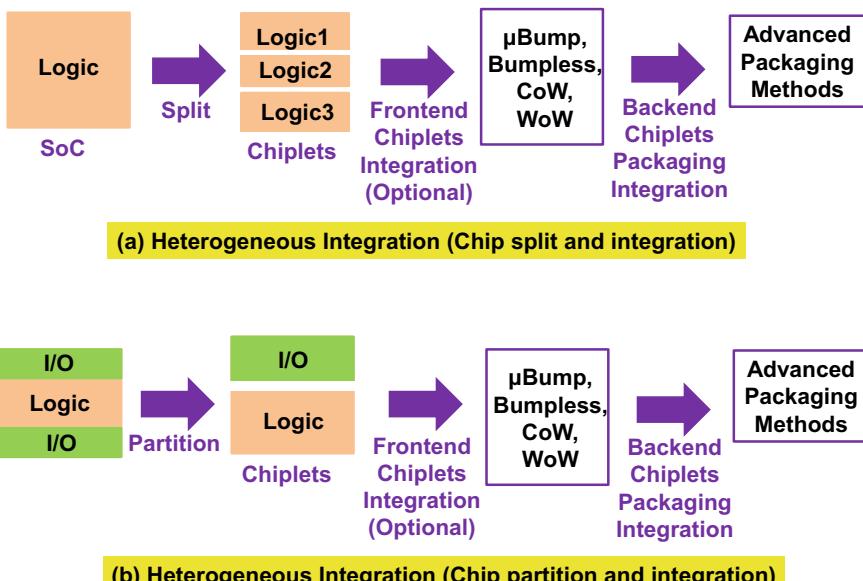
reduce the feature size (to do the scaling) to make the SoC. According to International Business Strategies, Fig. 9.3 shows the advanced design cost versus feature size through 5 nm. It can be seen that it will take more than \$500 million to just design the 5 nm feature size. For the 5 nm process technology development it will take another \$1 billion.

## 9.4 Chiplet Heterogeneous Integration

Heterogeneous chiplet integration contrasts with SoC. Chiplet heterogeneous integration redesigns the SoC into smaller chiplets and then uses packaging technology to integrate dissimilar chiplets with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem [23, 24]. A chiplet is a functional integrated circuit (IC) block that is often made of reusable IP (intellectual property) blocks.

There are at least two different chiplet heterogeneous integrations as shown in Fig. 9.4, namely chip split and integration (driven by cost and yield) and chip partition and integration (driven by cost and technology optimization). In chip split and integration, the SoC such as logic is split into smaller chiplets such as logic1, logic2, and logic3. These chiplets can be stacked (integrated) by the frontend CoW (chip-on-wafer) or WoW (wafer-on-wafer) methods [7–9] and then assembled (integrated) on the same substrate of a single package by using advanced packaging techniques. It should be emphasized that the frontend chiplets integration can yield a smaller package area and better electrical performance but is optional.

In chip partition and integration, the SoC such as the logic and I/Os are partitioned into functions: logic and I/O, and then integrated (stacked) by frontend CoW or WoW methods. It is followed by using advanced packaging methods to assemble the logic and I/O chiplets on the same substrate of a single package. Again, the frontend integration of chiplets is optional.

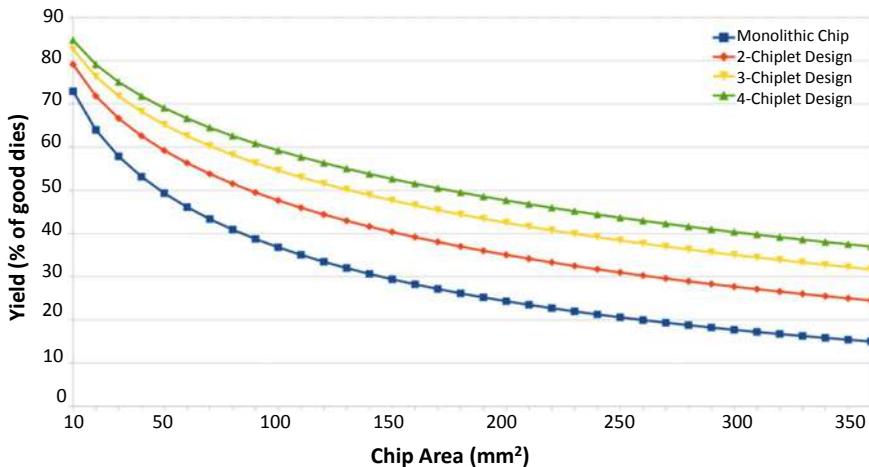


**Fig. 9.4** Chiplets: **a** Chip split and integration. **b** Chip partition and integration

## 9.5 Advantages and Disadvantages of Chiplet Heterogeneous Integration

The key advantages of chiplet heterogeneous integrations comparing with SoCs are yield improvement (lower cost) during manufacturing, time-to-market, and cost reduction during design. Figure 9.5 shows the plots of yield (percent of good dies) per wafer versus chip size for monolithic design and 2-, 3-, and 4-chiplet design [25]. It can be seen that a  $360 \text{ mm}^2$  monolithic die will have a yield of 15% while a 4-chiplet design (each  $99 \text{ mm}^2$ ) more than doubles the yield to 37%. The total die area of the 4-chiplet design incurs a ~10% area penalty ( $36 \text{ mm}^2$  for a combined silicon area of  $396 \text{ mm}^2$ ) but the significant improvement in yield which directly translates to lower cost. Also, chip partitioning will enhance the time-to-market. Furthermore, AMD, with its highly successful EPYC CPUs, has demonstrated the use of chiplets with CPU cores can reduce silicon design and manufacturing costs of a 32-core CPU by up to 40% [26]. Finally, there is also thermal benefit to using chiplets as the chips are spread out across the package.

The disadvantages of chiplet heterogeneous integration are: (1) additional area for interfaces and replicated logic, (2) higher packaging costs, (3) more complexity and design effort, and (4) past methodologies are less suitable for chiplets.

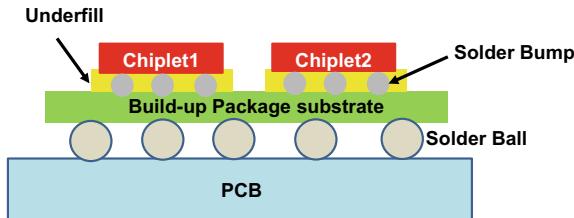


**Fig. 9.5** Yield versus chip size for SoC and various chiplet designs

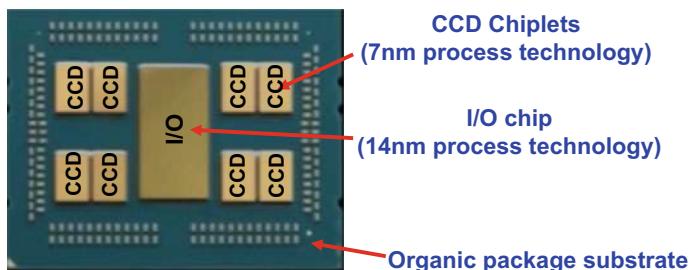
## 9.6 Advanced Packaging for Chiplet Heterogeneous Integration

### 9.6.1 2D Chiplet Heterogeneous Integration on Organic Substrate

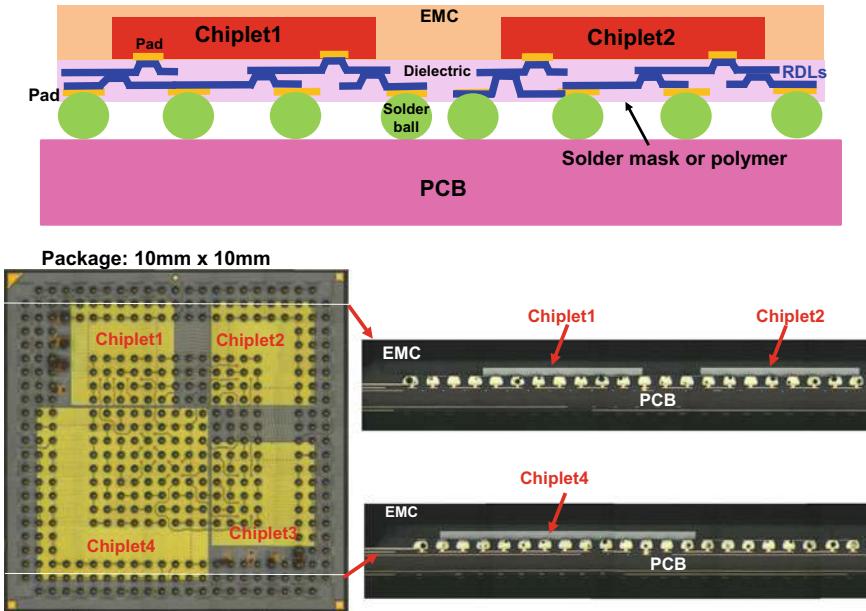
Figure 9.6 shows the schematic of a 2D chiplets heterogeneous integration on organic substrates which have been and will be used the most. It can be seen that the chiplets are solder bumped flip chip with underfill on a build-up package substrate and then solder balled on a PCB (printed circuit board). The assembly methods are mainly SMT (surface mount technology) and flip chip technology. The most famous 2D chiplets heterogeneous integration on organic substrate is the AMD EPYC processors [1–3], Fig. 9.7, which will be elaborated in Sect. 9.7. It can be seen that there are 4 pairs of chiplets (fabricated with 7 nm process technology) on each side of a larger I/O chip (fabricated by a 14 nm process technology) tightly coupled on an organic build-up substrate with underfill. If fan-out packaging technology [27–30] is used as shown in Fig. 9.8, then the chiplets are attached on the PCB through the fan-out redistribution-layers (RDLs) and solder balls. Wafer bumping for flip chip, build-up package substrate, and underfill are eliminated.



**Fig. 9.6** 2D chiplet heterogeneous integration on organic substrate



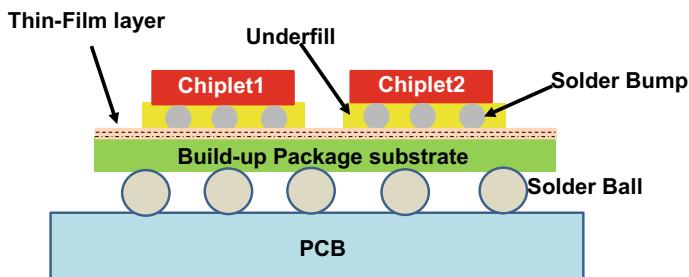
**Fig. 9.7** AMD's 2nd generation EPYC 2D chiplet heterogeneous integration on organic substrate [1]



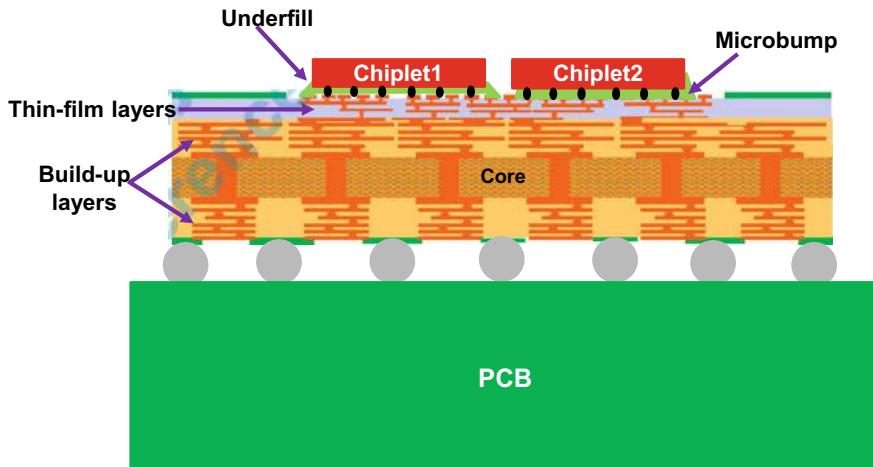
**Fig. 9.8** 2D chiplet fan-out heterogeneous integration on organic substrate

### 9.6.2 2.1D Chiplet Heterogeneous Integration on Organic Substrate

Figure 9.9 shows the schematic of a 2.1D chiplet heterogeneous integration on organic substrates. It can be seen that the chiplets are solder bumped flip chip on a build-up package substrate with thin-film layers. The most famous 2.1D substrate is the Shinko i-THOP (integrated thin-film high density organic package) [31, 32] and shown in Fig. 9.10. The metal line width and spacing of the thin-film layer are 2  $\mu\text{m}$ .



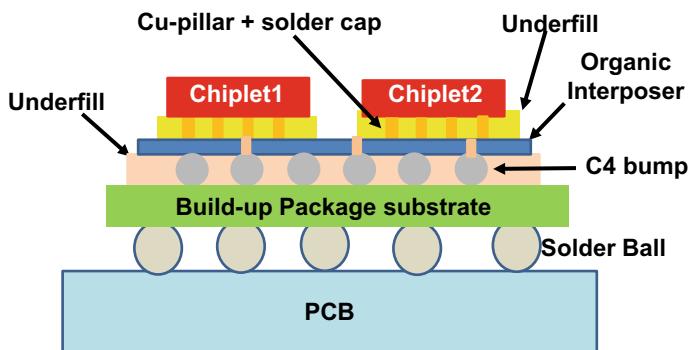
**Fig. 9.9** 2.1D chiplet heterogeneous integration on organic substrate



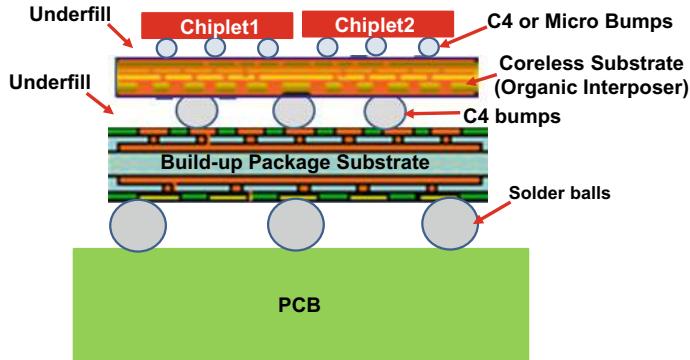
**Fig. 9.10** Shinko's 2.1D chiplet heterogeneous integration on organic substrate [32]

### 9.6.3 2.3D Chiplet Heterogeneous Integration on Organic Substrate

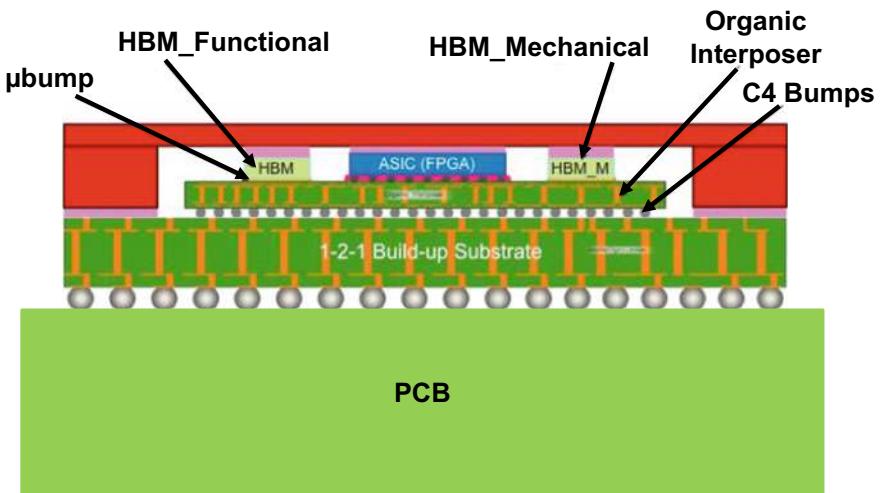
Figure 9.11 schematic shows a 2.3D chiplet heterogeneous integration on organic substrate. It can be seen that the chiplets are solder bumped flip chip on a coreless organic interposer. The most famous one is proposed by Shinko in 2012 (Fig. 9.12). They proposed to use the coreless package substrate to support the flip chip with underfill. For sure, the cost in making the coreless substrate is much lower than that in making the through-silicon via (TSV)-interposer. In 2016, Cisco used the similar technology [33] to support the FPGA (field programmable gate array) and high bandwidth memories (HBM)s as shown in Fig. 9.13.



**Fig. 9.11** 2.3D chiplet heterogeneous integration on organic substrate



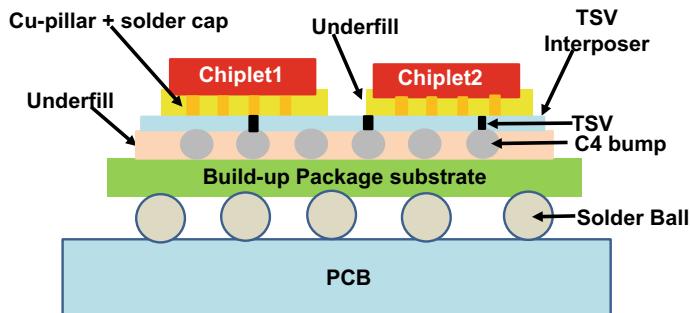
**Fig. 9.12** Shinko's 2.3D chiplet heterogeneous integration on coreless substrate



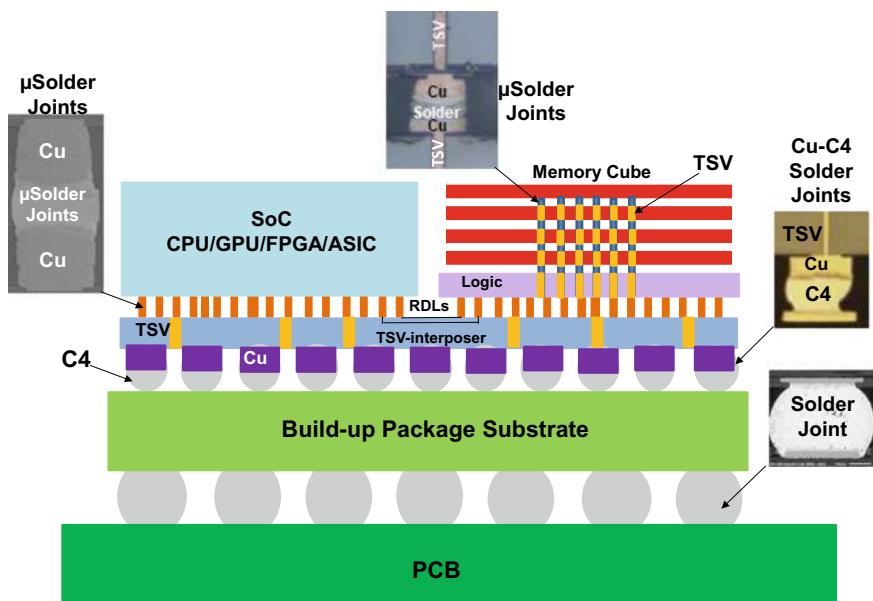
**Fig. 9.13** Cisco's 2.3D chiplet heterogeneous integration on organic interposer [33]

#### 9.6.4 2.5D Chiplet Heterogeneous Integration on Silicon Substrate (Passive TSV-Interposer)

Figure 9.14 schematic shows a 2.5D chiplet heterogeneous integration on silicon substrate. It can be seen that the chiplets are solder bumped flip chip with micro bumps (Cu-pillar + solder cap) on a passive TSV-interposer [34–41], which does not have CMOS (complementary metal oxide semiconductor) devices. The most famous one is the CoWoS (chip on wafer on substrate) as shown in Fig. 9.15 by TSMC for their customers such as Xilinx [42–45] and NVidia [46]. The TSV-interposer is usually with 4 RDLs (redistribution-layers) with minimum pitch equals to 0.4  $\mu\text{m}$  and

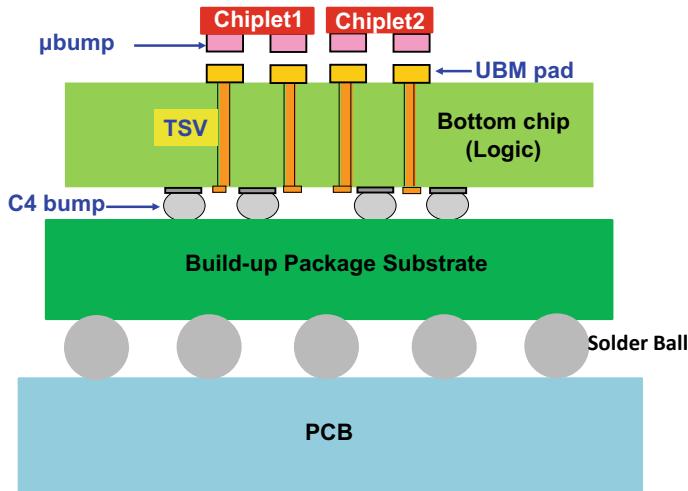


**Fig. 9.14** 2.5D chiplet heterogeneous integration on passive TSV-interposer



**Fig. 9.15** 2.5D (CoWoS-2) chiplet heterogeneous integration on passive TSV-interposer [41]

used to support SoC and HBMs. It is meant for high-density and high-performance applications.



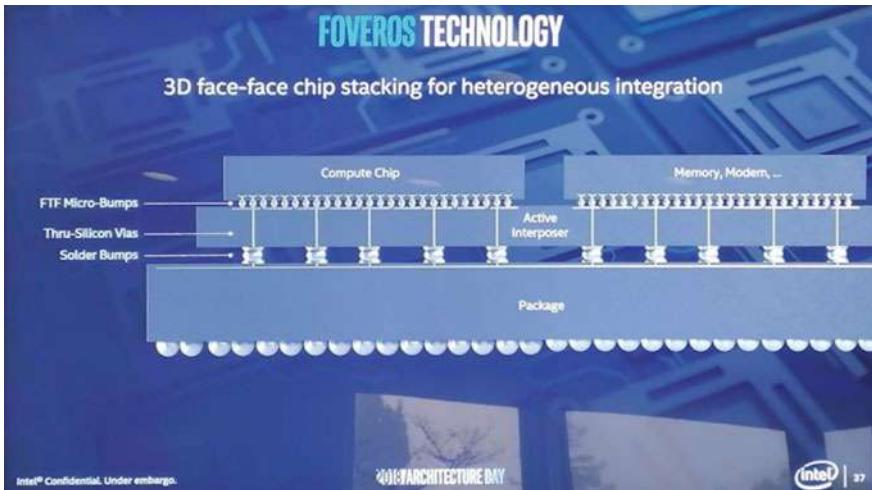
**Fig. 9.16** 3D chiplet heterogeneous integration

### 9.6.5 3D Chiplet Heterogeneous Integration on Silicon Substrate (Active TSV-Interposer)

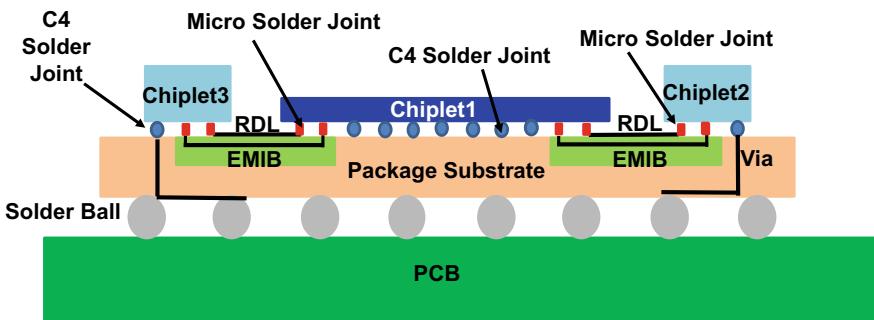
Figure 9.16 schematic shows a 3D chiplet heterogeneous integration on silicon substrate. It can be seen that the chiplets are solder bumped flip chip with micro bumps (Cu-pillar + solder cap) on an active TSV-interposer with CMOS devices. The most famous one and the only one in HVM today is Intel's FOVEROS as shown in Fig. 9.17 [4–6]. It can be seen that the chiplets (computer chip and memory chip, etc.) are face-to-face bonded to an active TSV-interposer and then the module is bonded to an organic package substrate. Please read Sect. 7.3.3 for more details.

### 9.6.6 Chiplet Heterogeneous Integration on Organic Substrate with Silicon Bridges

Figure 9.18 schematic shows a chiplet heterogeneous integration on organic substrate with a silicon bridge. It can be seen that the chiplets are flip-chip bonded with both C4 bumps and C2 bumps on an organic build-up package substrate with embedded silicon bridge with RDLs [47, 48]. The most famous bridge is Intel's EMIB (embedded multi-die interconnect bridge) as shown in Fig. 9.19 for Intel's FPGA (Agilex).



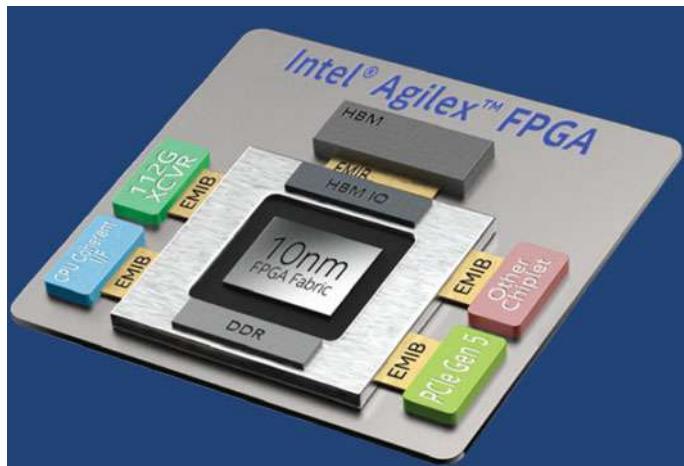
**Fig. 9.17** Intel's 3D chiplet heterogeneous integration (FOVEROS)



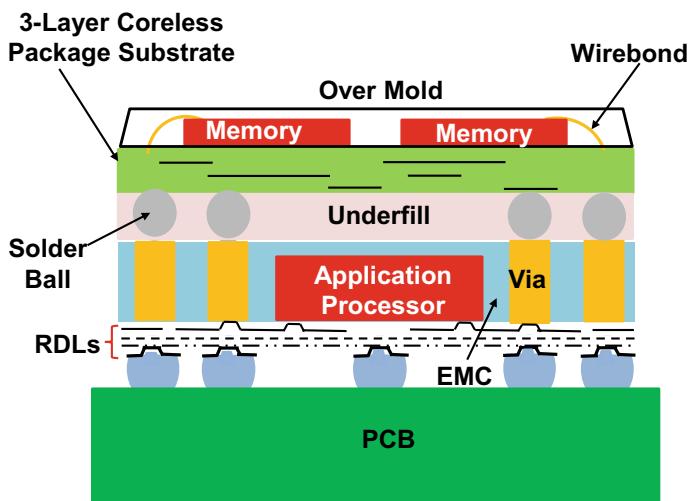
**Fig. 9.18** Chiplet heterogeneous integration on organic substrate with silicon bridge

### 9.6.7 PoP Chiplet Heterogeneous Integration

Figure 9.20 schematic shows a PoP (package-on-package) chiplet heterogeneous integration. It can be seen that the application processor chiplet is packaged by TSMC's InFO (integrated fan-out) WLSI (wafer level system integration) technology (the bottom package) and the memory chiplets are packaged by wire bonding on a coreless organic substrate technology (the top package). The cross section of the application processor chipset in the iPhone XS is shown in Fig. 9.21.



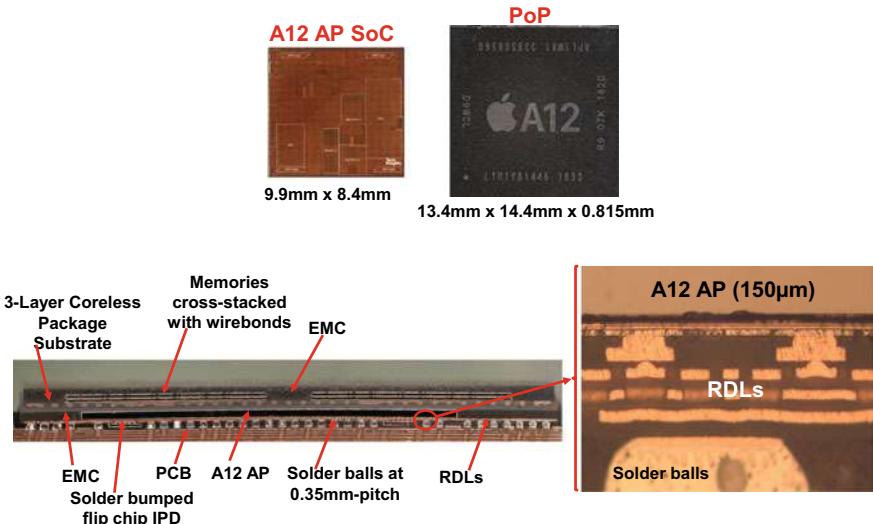
**Fig. 9.19** Intel’s Chiplet heterogeneous integration on organic substrate with silicon bridge (Agilex FPGA) [47]



**Fig. 9.20** PoP chiplet heterogeneous integration

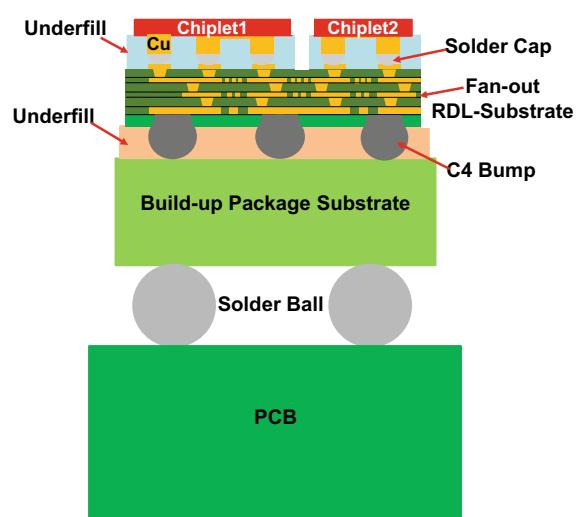
### 9.6.8 Chiplet Heterogeneous Integration on Fan-Out RDL-Substrate

Figure 9.22 schematic shows a chiplet heterogeneous integration on RDL-substrate. It can be seen that the chiplets are flip-chip bonded with C2 (Cu-pillar + solder cap) bumps on a fan-out chip-last (or RDL-first) substrate and then C4 bump bonded on a build-up organic package substrate. (A 2.5D IC integration). Finally, the whole



**Fig. 9.21** Apple iPhone’s PoP InFO Chiplet heterogeneous integration

**Fig. 9.22** Chiplet heterogeneous integration with fan-out (RDL-first) substrate



module is assembled on a PCB with solder balls [15, 49–55]. This packaging technology is meant for high-density, high-performance, and large chiplets applications just next to CoWoS as shown in Sect. 9.6.4. For smaller chiplets such as  $5\text{ mm} \times 5\text{ mm}$ , then fan-out with chip-first substrate (with lower cost) [56–60] is adequate.

## 9.7 AMD's Chiplet Heterogeneous Integration

In mid-2019, AMD introduced the 2nd-generation EPYC, 7002-series, codename Rome which doubled the number of cores to sixty-four. The 2nd Gen EPYC is a new breed of server processors which sets a higher standard for data centers. In [1–3], it shows that Rome server product makes use of a 9-2-9 package for signal connectivity with 4 layers above the package core for signal routing. One of the signaling layers (others are similar) is shown in Fig. 9.23 along with the physical position of the CCD (CPU compute die), IOD (IO die), as well as main external DRAM (dynamic random-access memory) and SerDes interfaces.

The AMD chiplets evolution (development) of the hybrid multi-die architecture is shown in Fig. 9.24 [1–3]. For high-performance servers and desktop processors the I/Os are very heavy. Analog devices and bump pitches for I/Os benefit very little from leading edge technology and is very costly. One of the solutions is to partition the SoC into chiplets, reserving the expensive leading-edge silicon for CPU core while leaving the I/Os and memory interfaces in n-1 generation silicon [1–3]. Because AMD committed to keep the EPYC package size and pin-out unchanged, there need to be a close silicon/package co-design as the number of die increases from four in the first EPYC to nine in the 2nd Gen EPYC.

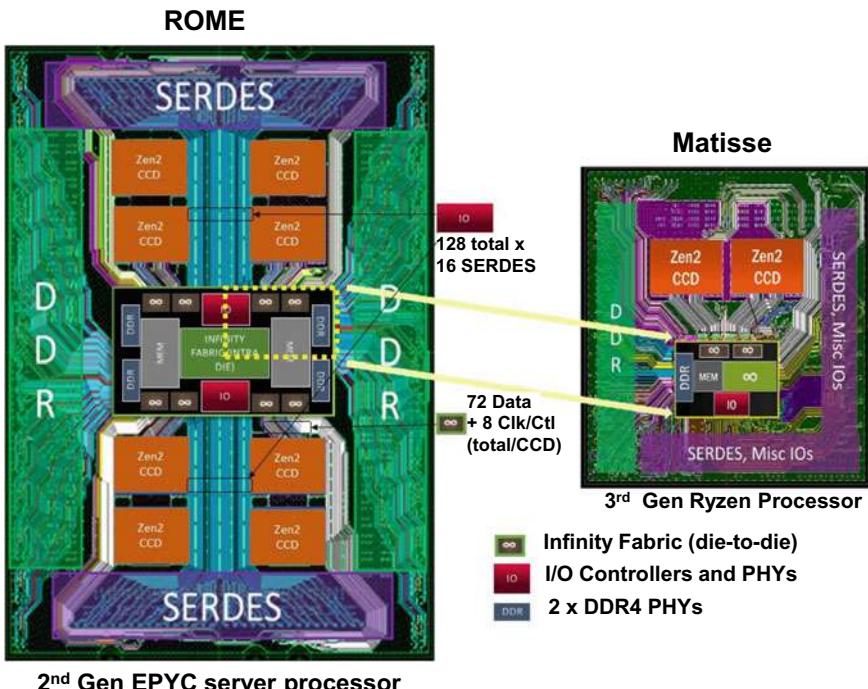


Fig. 9.23 AMD's 2nd generation EPYC server and desktop processor with chiplets [1]

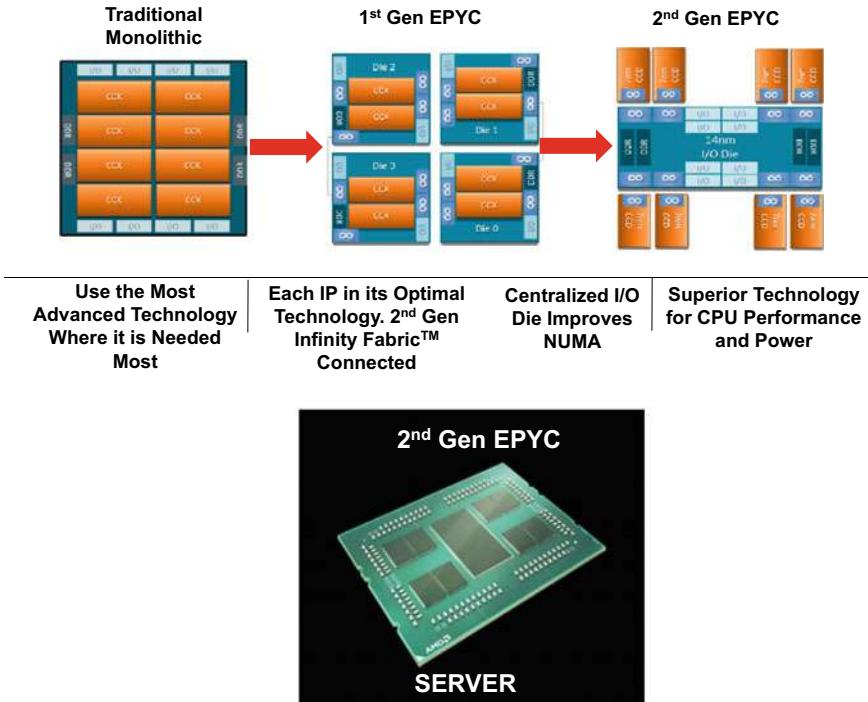
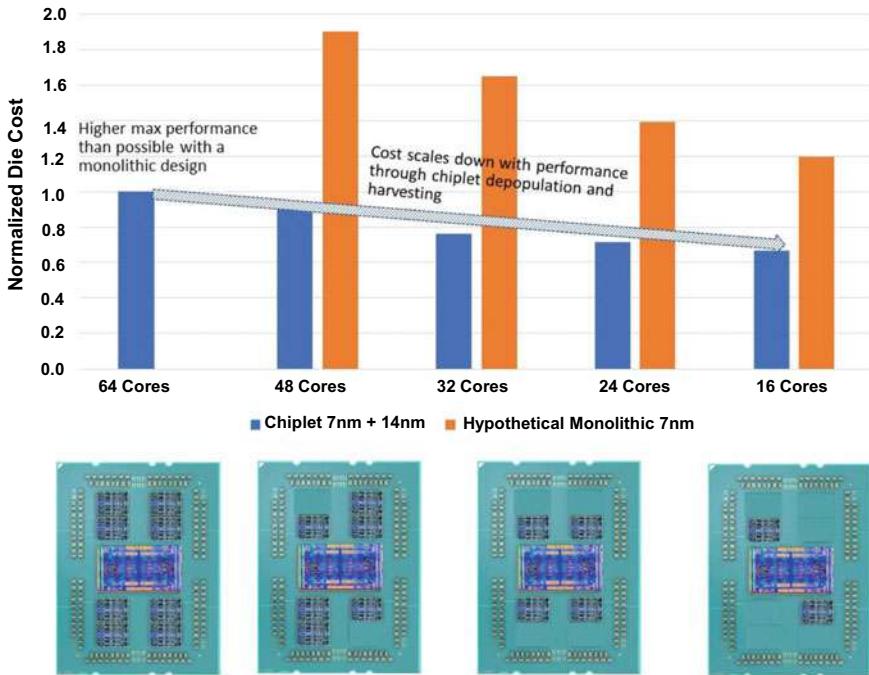


Fig. 9.24 AMD's chiplets evolution [1]

The 2nd Gen EPYC chiplet performance versus cost is shown in Fig. 9.25 [1–3]. AMD reveal that on TSMC's 7 nm process technology the cost to manufacture a 16-core monolithic die is more than double that of a multi-chiplets CPU. It can be seen from Fig. 9.25 that: (a) the lower the core counts, the lower the saving, (b) higher core counts and performance than possible with a monolithic design, (c) lower costs at all core count/performance points in the product line, (d) cost scales down with performance by depopulating chiplets, and (e) 14 nm process technology for IOD reduces the fixed cost.

AMD also optimize the cost structure and improve die yields by using much smaller chiplets. AMD used the expensive 7 nm process technology by TSMC for the core cache dies and moved the DRAM and Pie logic to a 14 nm I/O die fabricated by Global Foundries.

The 2nd-generation EPYC is a 2D chiplets integration technology, i.e., all the chiplets are side-by-side on the same substrate of a single package. AMD's future chiplet heterogeneous integration [3] will be 3D chiplets integration as shown in Fig. 9.26, i.e., the chiplets are (stacked) on top of the other chiplet such as logic, so called the active TSV-interposer.

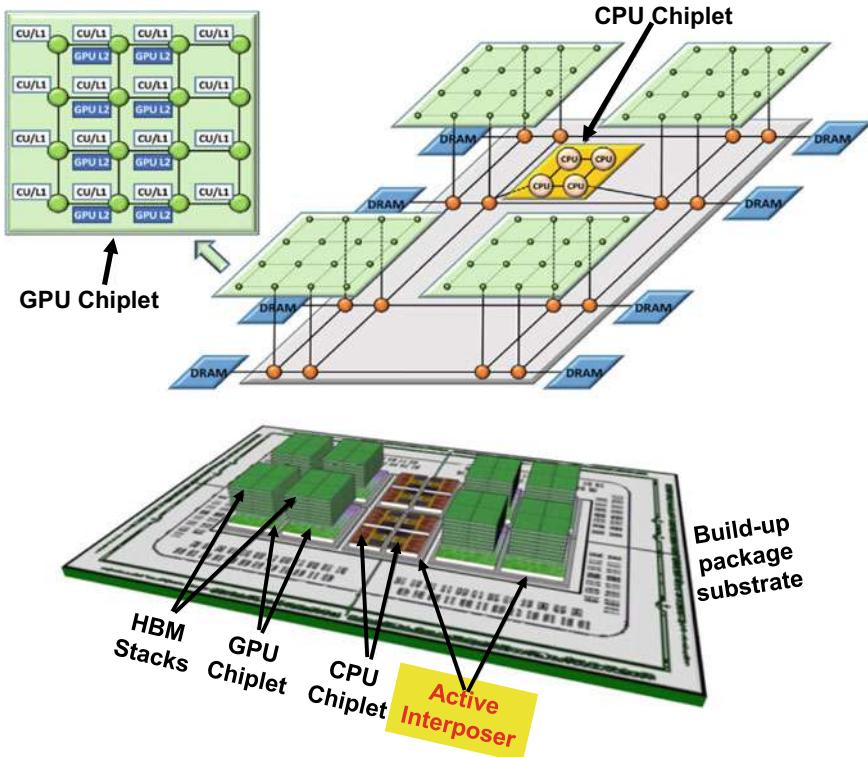


**Fig. 9.25** AMD's die cost comparison: chiplet (7 nm + 12 nm) versus monolithic (7 nm) [1]

## 9.8 Intel's Chiplet Heterogeneous Integration

In July 2020, Intel shipped their mobile (notebook) processor “Lakefield”, which is based on their FOVEROS technology (TYPE-3 of the Omni-directional interconnect announced in July 2019). The SoC is partitioned (e.g., CPU, GPU, LPDDR4, etc.) and split (e.g., the CPU is split into one big CPU and 4 smaller CPU) into chiplets as shown in Fig. 9.27. These chiplets are then face-to-face bonded (stacked) on an active TSV-interposer (a large 22FFL base chip) with a CoW process as shown in Figs. 9.28 and 9.29 [4–6]. The interconnect between the chiplets and the logic base chip is micro bump (Cu pillar + SnAg solder cap) as shown in Figs. 9.28 and 9.29. The interconnect between the base chip and the package substrate is C4 bump and between the package substrate and PCB is solder ball. The final package formant is a PoP (12 mm × 12 mm × 1 mm) as shown in Fig. 9.27. The chiplet heterogeneous integration is in the bottom package and the upper package is housing the memories with wire bonding technology.

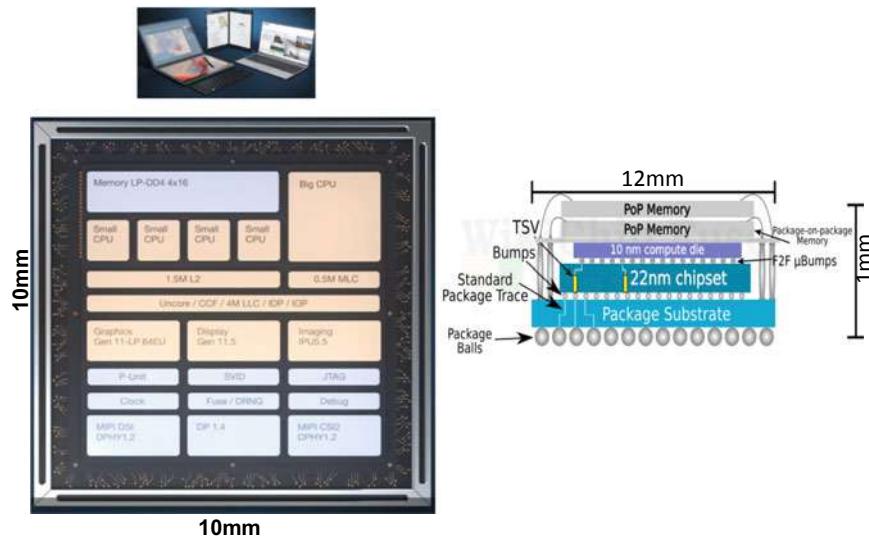
The fabrication of the chiplets is with Intel's 10 nm process technology and of the base chip is 22 nm. Since chiplets' size is smaller and not all the chips are using the 10 nm process technology, the overall yield must be higher and thus it translates to lower cost.



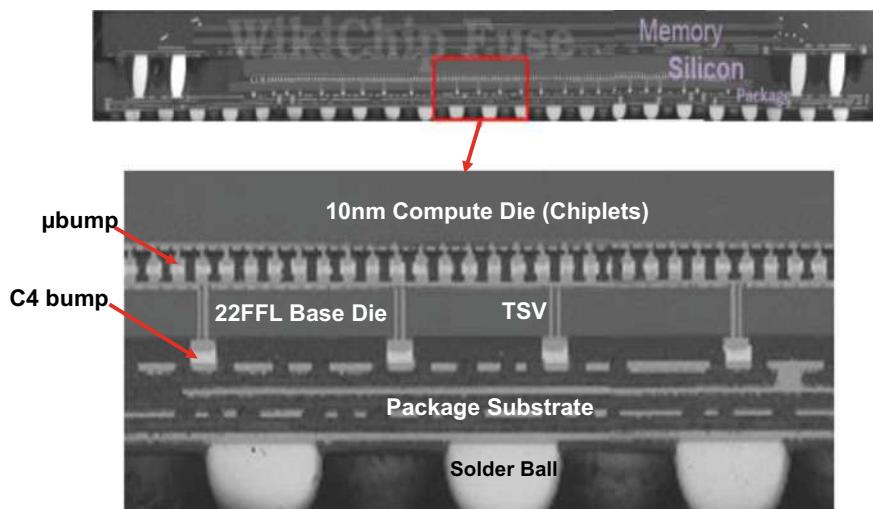
**Fig. 9.26** AMD's future chiplet technology—3D chiplet integration (active TSV-interposer) [3]

It should be noted that this is the very first HVM of 3D chiplets integration. Also, this is the very first HVM of processors for mobile products such as the notebook by 3D IC integration.

During Intel Architecture Day (August 13, 2020), they announced a Cu–Cu hybrid bonding for their FOVEROS technology. They demonstrated that with bumpless hybrid bonding the pitch can go down to  $10\text{ }\mu\text{m}$  instead of  $50\text{ }\mu\text{m}$  like the Lakefield as shown in Fig. 9.30.



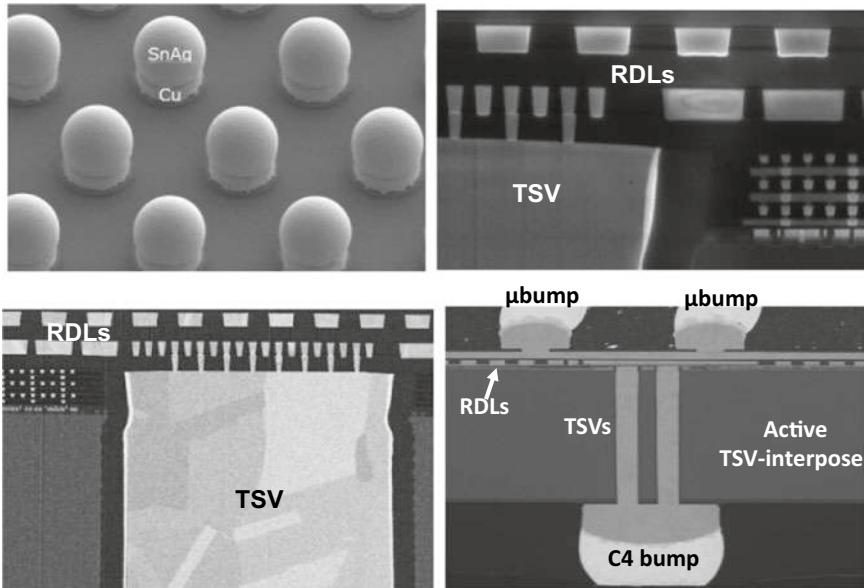
**Fig. 9.27** Intel's Lakefield mobile (notebook) processor by FOVEROS technology [5]



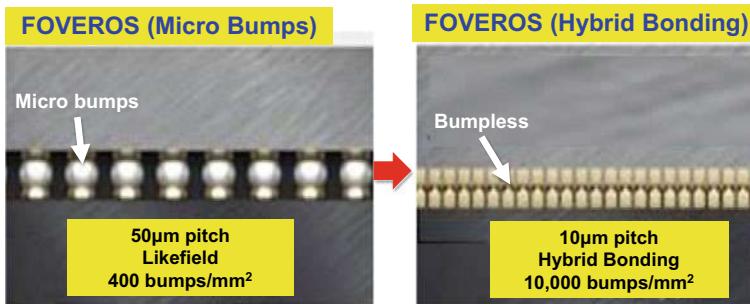
**Fig. 9.28** SEM image of the cross section of the Lakefield processor [5]

## 9.9 TSMC's Chiplet Heterogeneous Integration

On TSMC Annual Technology Symposium (August 25, 2020) TSMC announced their 3DFabric (3D fabrication) technology for mobile, high-performance computing, automotive, and IoT (internet of things) applications [7–9]. 3DFabric provides chiplet



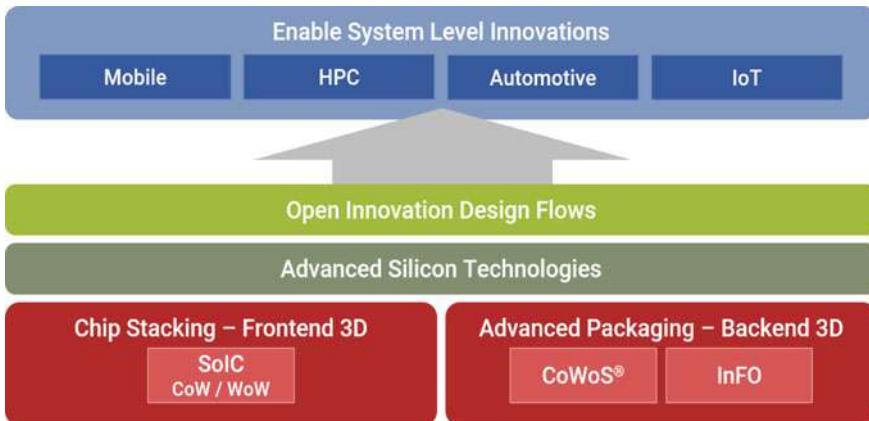
**Fig. 9.29** SEM images of the details of the cross section of the Lakefield processor [5]



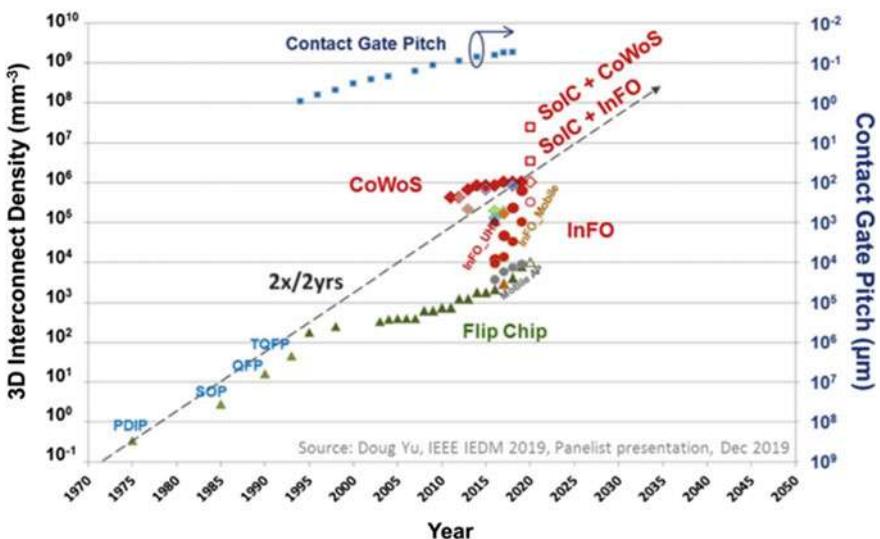
**Fig. 9.30** Intel's FOVEROS with microbump (50 µm-pitch) and bumpless (10 µm-pitch) [5]

heterogeneous integrations that are fully integrated from frontend to backend as shown in Fig. 9.31. The application-specific platform leverages TSMC's advanced wafer technology, open innovation platform design ecosystem, and 3DFabric for fast improvements and time-to-market.

TSMC's chiplet heterogeneous integration roadmap is shown in Fig. 9.32 [8]. Frontend 3D hybrid bonding (stacking) technology (SoIC) with CoW and WoW, provides flexible chip-level chiplets design and integration (Fig. 9.33). Comparing with the conventional chiplets microbump flip chip technology, hybrid bonding SoIC (system on integrated chips) has many advantages, e.g., better thermal performance and less energy spent per bit data as shown in Fig. 9.34 [9].

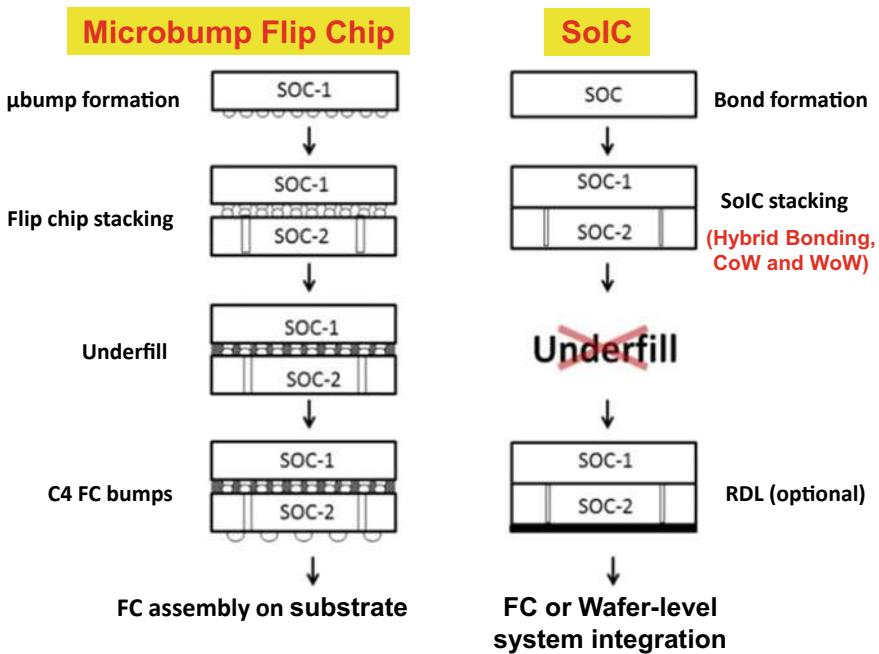


**Fig. 9.31** TSMC's 3DFabric integration



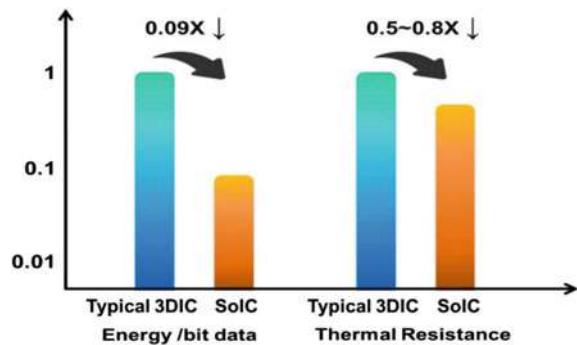
**Fig. 9.32** TSMC's 3DFabric roadmap [9]

In 3D backend package integration, CoWoS' increased envelope and enriched technology content offers exceptionally high computing performance and high memory bandwidth to meet HPC needs on clouds, data center, and high-end servers as shown in Fig. 9.35a. In another 3D backend package integration, InFO derivative technology offers memory-to-logic, logic-to-logic, PoP, etc. applications as shown in Fig. 9.35b. The HVM of SoIC, SoIC + CoWoS, and SoIC + InFO is expected in 2021.



**Fig. 9.33** TSMC's hybrid bonding SoIC versus the conventional microbump flip chip technology [9]

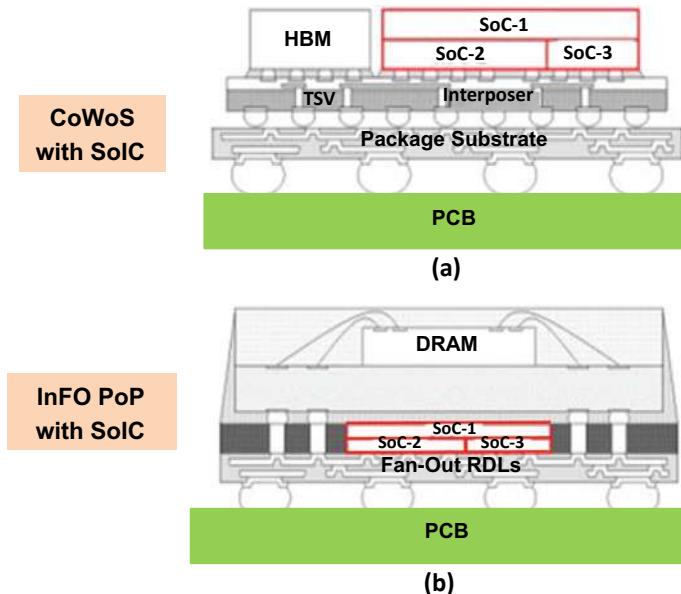
**Fig. 9.34** Thermal and energy performance: SoIC versus conventional 3D IC [9]



## 9.10 Summary and Recommendation

Some important results and recommendation are summarized as follows.

- SoCs with chip scaling are here to stay. However only a handful of companies such as Apple, Samsung, Huawei, Google can afford them at finer feature size (advanced nodes). Usually, there are some reasons for them to do so. Take Apple for example, there are at least three reasons: (a) on April 23, 2008, Apple acquired



**Fig. 9.35** TSMC’s backend integration. **a** SoIC + CoWoSSoIC + CoWoS. **b** SoIC + InFO PoP SoIC + InFO [9]

Palo Alto Semiconductor and has been building their chips with lots of IPs and coupled (integrated) with their software development, (b) breaking their SoC design up into chiplets would not be an attractive prospect because the additional chip-to-chip interconnection and communication overhead would create more headaches than it’s worth, and (c) the world’s number one foundry (TSMC) is Apple’s loyal partner and they committed to Apple’s schedule, e.g., the application processor (A16) is planned to be manufactured with TSMC’s 3 nm process technology in the second half of 2022.

- Chiplets provide alternatives (options) to SoCs, especially for advanced nodes, which most companies cannot afford.
- In order to promote/popular the chiplets heterogeneous integrations, standards are necessary! The DARPA CHIPS is heading into the right direction.
- EDA (electronic design automation) tools for automating system splitting and partitioning and design are desperately needed for complex chiplets heterogeneous integrations.
- For more information on chiplets heterogeneous integration, please read [23].

## References

1. Naffziger, S., K. Lepak, M. Paraschour, and M. Subramony, “AMD Chiplet Architecture for High-Performance Server and Desktop Products”, *IEEE/ISSCC Proceedings*, February 2020, pp. 44–45.
2. Naffziger, S., “Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs”, *Symposia on VLSI Technology and Circuits*, June 2020, pp. 1–39.
3. Stow, D., Y. Xie, T. Siddiqua, and G. Loh, “Cost-Effective Design of Scalable High-Performance Systems Using Active and Passive Interposers”, *IEEE/ICCAD Proceedings*, November 2017, pp. 1–8.
4. Ingerly, D., S. Amin, L. Aryasomayajula, A. Balankutty, D. Borst, A. Chandra, K. Cheemalapati, C. Cook, R. Criss, K. Enamul1, W. Gomes, D. Jones, K. Kolluru, A. Kandas, G.. Kim, H. Ma, D. Pantuso, C. Petersburg, M. Phen-givoni, A. Pillai, A. Sairam, P. Shekhar, P. Sinha, P. Stover, A. Telang, and Z. Zell, “Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices”, *IEEE/IEDM Proceedings*, December 2019, pp. 19.6.1–19.6.4.
5. Gomes, W., S. Khushu, D. Ingerly, P. Stover, N. Chowdhury, F. O’Mahony, etc., “Lakefield and Mobility Computer: A 3D Stacked 10 nm and 2FFL Hybrid Processor System in  $12 \times 12 \text{ mm}^2$ , 1 mm Package-on-Package”, *IEEE/ISSCC Proceedings*, February 2020, pp. 40–41.
6. WikiChip, “A Look at Intel Lakefield: A 3D-Stacked Single-ISA Heterogeneous Penta-Core SoC”, <https://en.wikichip.org/wiki/chiplet>, May 27, 2020.
7. Chen, M. F., C. S. Lin, E. B. Liao, W. C. Chiou, C. C. Kuo, C. C. Hu, C. H. Tsai, C. T. Wang and D. Yu, “SoIC for Low-Temperature, Multi-Layer 3D Memory Integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.
8. Chen, Y. H., C. A. Yang, C. C. Kuo, M. F. Chen, C. H. Tung, W. C. Chiou, and D. Yu, “Ultra High Density SoIC with Sub-micron Bond Pitch”, *IEEE/ECTC Proceedings*, May 2020, pp. 576–581.
9. Chen, F., M. Chen, W. Chiou, D. Yu, “System on Integrated Chips (SoIC™) for 3D Heterogeneous Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 594–599.
10. Lin, J., C. Chung, C. Lin, A. Liao, Y. Lu, J.g Chen, and D. Ng, ”Scalable Chiplet package using Fan-Out Embedded Bridge”, *IEEE/ECTC Proceedings*, May 2020, pp. 14–18.
11. Coudrain, P., J. Charbonnier, A. Garnier, P. Vivet, R. Vélard, A. Vinci, F. Ponthenier, A. Farcy, R. Segaud, P. Chausse, L. Arnaud, D. Lattard, E. Guthmuller, G. Romano, A. Gueugnot, F. Berger, J. Beltritti, T. Mourier, M. Gottardi, S. Minoret, C. Ribière, G. Romero, P.-E. Philip, Y. Exbrayat, D. Scevola, D. Campos, M. Argoud, N. Allouti, R. Eleouet, C. Fuguet Tortolero, C. Aumont, D. Dutoit, C. Legalland, J. Michailos, S. Chéramy, and G. Simon, “Active interposer technology for chiplet-based advanced 3D system architectures”, *EEE/ECTC Proceedings*, May 2019, pp. 569–578.
12. Jo, P., T. Zheng, and M. Bakir, “Polyolithic Integration of 2.5D and 3D Chiplets using Interconnect Stitching”, *IEEE/ECTC Proceedings*, May 2019, pp. 1803–1808.
13. Ko, T., H. P. Pu, Y. Chiang, H. J. Kuo, C. T. Wang, C. S. Liu, and D. C. Yu, “Applications and Reliability Study of InFO\_UHD (Ultra-High-Density) Technology”, *IEEE/ECTC Proceedings*, May 2020, pp. 1120–1125.
14. Huang, Y., C. Chung, C. Lin, G. Lu, C. Tseng, H. Chang, C. Hsu, and B. Xu, “Challenges of large Fan out multi-chip module and fine Cu line space”, *IEEE/ECTC Proceedings*, May 2020, pp. 1140–1145.
15. Chuang, P., M. Lin, S. Hung, Y. Wu, D. Wong, M. Yew, C. Hsu, L. Liao, P. Lai, P. Tsai, S. Chen, S. Cheng, and S. Jeng, “Hybrid Fan-out Package for Vertical Heterogeneous Integration”, *IEEE/ECTC Proceedings*, May 2020, pp. 333–338.
16. Rupp, B., A. Plochowitzt, L. Crawford, M. Shreve, S. Raychaudhuri, S. Butylkov, Y. Wang, P. Mei, Q. Wang, J. Kalb, Y. Wang, E. Chow, and J. Lu, “Chiplet Micro-Assembly Printer”, *IEEE/ECTC Proceedings*, May 2019, pp. 1312–1315.
17. Fish, M., P. McCluskey, and A. Bar-Cohen, “Thermal Isolation Within High-Power 2.5D Heterogeneously Integrated Electronic Packages”, *IEEE/ECTC Proceedings*, May 2016, pp. 1847–1855.

18. Gomez, D., K. Ghosal, M. Meitl, S. Bonafede, C. Prevatte, T. Moore, B. Raymond, D. Kneeburg, A. Fecioru, A. Trindade, and C. Bower1, “Process Capability and Elastomer Stamp Lifetime in Micro Transfer Printing”, *IEEE/ECTC Proceedings*, May 2016, pp. 680–687.
19. <https://www.darpa.mil/program/compound-semiconductor-materials-on-silicon>
20. <https://www.darpa.mil/program/dahi-compound-semiconductor-materials-on-silicon>.
21. <https://www.darpa.mil/program/common-heterogeneous-integration-and-ip-reuse-strategies>.
22. <https://nxtl.org/opportunity/state-of-the-art-heterogeneous-integrated-packaging-ship-prototype-project/>.
23. Lau, J. H., *Heterogeneous Integration*, Springer, New York, 2019.
24. Lau, J. H., “Recent Advances and Trends in Heterogeneous Integrations”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 16, April 2019, pp. 45–77.
25. <https://en.wikichip.org/wiki/chiplet>, March 27, 2020.
26. <https://www.netronome.com/blog/its-time-disaggregated-silicon/>, March 12, 2020.
27. Lau, J. H., M. Li, M. Li, T. Chen, I. Xu, X. Qing, Z. Cheng, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, P. Lo, K. Wu, J. Hao, S. Koh, R. Jiang, X. Cao, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, “Fan-Out Wafer-Level Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, 2018, September 2018, pp. 1544–1560.
28. Lau, J. H., M. Li, Y. Lei, M. Li, I. Xu, T. Chen, Q. Yong, Z. Cheng, K. Wu, P. Lo, Z. Li, K. Tan, Y. Cheung, N. Fan, E. Kuah, C. Xi, J. Ran, R. Beica, S. Lim, N. Lee, C. Ko, H. Yang, Y. Chen, M. Tao, J. Lo, and R. Lee, “Reliability of Fan-Out Wafer-Level Heterogeneous Integration”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 148–162.
29. Ko, CT, H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. W. Lin, T. Chen, I. Xu, C. Chang, J. Pan, H. Wu, Q. Yong, N. Fan, E. Kuah, Z. Li, K. Tan, Y. Cheung, E. Ng, K. Wu, J. Hao, R. Beica, M. Lin, Y. Chen, Z. Cheng, S. Koh, R. Jiang, X. Cao, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, “Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, September 2018, pp. 1561–1572.
30. Ko, C. T., H. Yang, J. H. Lau, M. Li, M. Li, C. Lin, J. Lin, C. Chang, J. Pan, H. Wu, Y. Chen, T. Chen, I. Xu, P. Lo, N. Fan, E. Kuah, Z. Li, K. Tan, C. Lin, R. Beica, M. Lin, C. Xi, S. Lim, N. Lee, M. Tao, J. Lo, and R. Lee, “Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 15, Issue: 4, October 2018, pp. 141–147.
31. Shimizu, N., Kaneda, W., Arisaka, H., Koizumi, N., Sunohara, S., Rokugawa, A., and Koyama, T., “Development of Organic Multi Chip Package for High Performance Application,” *IMAPS International Symposium on Microelectronics*, Orlando, FL, Sep. 30–Oct. 3, 2013, pp. 414–419.
32. Oi, K., Otake, S., Shimizu, N., Watanabe, S., Kunimoto, Y., Kurihara, T., Koyama, T., Tanaka, M., Aryasomayajula, L., and Kutlu, Z., “Development of New 2.5D Package With Novel Integrated Organic Interposer Substrate With Ultra-Fine Wiring and High Density Bumps,” *IEEE/ECTC Proceedings*, May 2014, pp. 348–353.
33. Li, L., P. Chia, P. Ton, M. Nagar, S. Patil, J. Xue, J. DeLaCruz, M. Voicu, J. Hellings, B. Isaacson, M. Coor, and R. Havens, “3D SiP with organic interposer of ASIC and memory integration,” *IEEE/ECTC Proceedings*, May 2016, pp. 1445–1450.
34. Souriau, J., O. Lignier, M. Charrier, and G. Poupon, “Wafer Level Processing Of 3D System in Package for RF and Data Applications”, *IEEE/ECTC Proceedings*, 2005, pp. 356–361.
35. Henry, D., D. Belhachemi, J-C. Souriau, C. Brunet-Manquat, C. Puget, G. Ponthenier, J. Vallejo, C. Lecouvey, and N. Sillon, “Low Electrical Resistance Silicon Through Vias: Technology and Characterization”, *IEEE/ECTC Proceedings*, 2006, pp. 1360–1366.
36. Shao, S., Y. Niu, J. Wang, R. Liu, S. Park, H. Lee, G. Refai-Ahmed, and L. Yip, “Comprehensive Study on 2.5D Package Design for Board-Level Reliability in Thermal Cycling and Power Cycling”, *Proceedings of IEEE/ECTC*, May 2018, pp. 1662–1669.
37. McCann, S., H. Lee, G. Refai-Ahmed, T. Lee, and S. Ramalingam, “Warpage and Reliability Challenges for Stacked Silicon Interconnect Technology in Large Packages”, *Proceedings of IEEE/ECTC*, May 2018, pp. 2339–2344.

38. Lai, C., H. Li, S. Peng, T. Lu, and S. Chen, “Warpage Study of Large 2.5D IC Chip Module”, *Proceedings of IEEE/ECTC*, May 2017, pp. 1263–1268.
39. Hong, J., K. Choi, D. Oh, S. Park, S. Shao, H. Wang, Y. Niu, and V. Pham, “Design Guideline of 2.5D Package with Emphasis on Warpage Control and Thermal Management”, *Proceedings of IEEE/ECTC*, May 2018, pp. 682–692.
40. Lee, J., C. Lee, C. Kim, and S. Kalchuri, “Micro Bump System for 2nd Generation Silicon Interposer with GPU and High Bandwidth Memory (HBM) Concurrent Integration”, *Proceedings of IEEE/ECTC*, May 2018, pp. 607–612.
41. Hou, S., W. Chen, C. Hu, C. Chiu, K. Ting, T. Lin, W. Wei, W. Chiou, V. Lin, V. Chang, C. Wang, C. Wu, and D. Yu, “Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology”, *IEEE Transactions on Electron Devices*, October 2017, pp. 4071–4077.
42. Chaware, R., K. Nagarajan, and S. Ramalingam, “Assembly and reliability challenges in 3D integration of 28 nm FPGA die on a large high-density 65 nm passive interposer,” *IEEE/ECTC Proceedings*, May 2012, pp. 279–283.
43. Banijamali, B., S. Ramalingam, K. Nagarajan, and R. Chaware, “Advanced reliability study of TSV interposers and interconnects for the 28 nm technology FPGA,” *IEEE/ECTC Proceedings*, May 2011, pp. 285–290.
44. Banijamali, B., S. Ramalingam, H. Liu, and M. Kim, “Outstanding and innovative reliability study of 3D TSV interposer and fine-pitch solder micro-bumps,” *IEEE/ECTC Proceedings*, May 2012, pp. 309–314.
45. Banijamali, B., C. Chiu, C. Hsieh, T. Lin, C. Hu, S. Hou, et al., “Reliability evaluation of a CoWoS-enabled 3D IC package,” *IEEE/ECTC Proceedings*, May 2013, pp. 35–40.
46. Lee, J., C. Lee, C. Kim, and S. Kalchuri, “Micro Bump System for 2nd Generation Silicon Interposer with GPU and High Bandwidth Memory (HBM) Concurrent Integration”, *IEEE/ECTC Proceedings*, May 2018, pp. 607–612.
47. Mahajan, R., R. Sankman, N. Patel, D. Kim, K. Aygun, Z. Qian, et al., “Embedded multi-die interconnect bridge (EMIB) – a high-density, high-bandwidth packaging interconnect,” *IEEE/ECTC Proceedings*, May 2016, pp. 557–565.
48. Podpod, A., J. Slabbeekoor, A. Phommahaxay, F. Duval, A. Salahouedlhadj, M. Gonzalez, K. Rebibis, R.A. Miller, G. Beyer, and E. Beyne, “A Novel Fan-Out Concept for Ultra-High Chip-to-Chip Interconnect Density with 20- $\mu\text{m}$  Pitch”, *IEEE/ECTC Proceedings*, May 2018, pp. 370–378.
49. Suk, K., S. Lee, J. Kim, S. Lee, H. Kim, S. Lee, H. Kim, S. Lee, P. Kim, D. Kim, D. Oh, and J. Byun, “Low-cost Si-less RDL interposer package for high-performance computing applications,” *IEEE/ECTC Proceedings*, May 2018, pp. 64–69.
50. Miki, S., H. Taneda, N. Kobayashi, K. Oi, K. Nagai, T. Koyama, “Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder”, *IEEE/ECTC Proceedings*, May 2019, pp. 1599–1604.
51. Murayama, K., S. Miki, H. Sugahara, and K. Oi, “Electro-migration evaluation between organic interposer and build-up substrate on 2.3D organic package”, *IEEE/ECTC Proceedings*, May 2020, pp. 716–722.
52. Chang, K., C. Huang, H. Kuo, M. Jhong, T. Hsieh, M. Hung, and C. Wang, “Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity”, *IEEE/ECTC Proceedings*, May 2019, pp. 41–46.
53. Lin, Y., M. Yew, M. Liu, S. Chen, T. Lai, P. Kavle, C. Lin, T. Fang, C. Chen, C. Yu, K. Lee, C. Hsu, P. Lin, F. Hsu and S. Jeng, “Multilayer RDL Interposer for Heterogeneous Device and Module Integration”, *IEEE/ECTC Proceedings*, May 2019, pp. 931–936.
54. Lau, J. H., C. Ko, T. Peng, K. Yang, T. Xia, P. Lin, J. Chen, P. Huang, T. Tseng, E. Lin, L. Chang, C. Lin, and W. Lu, “Chip-Last (RDL-First) Fan-Out Panel-Level Packaging (FOPLP) for Heterogeneous Integration”, *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 17, No. 3, October 2020, pp. 89–98.
55. Lau, J. H., C. Ko, K. Yang, C. Peng, T. Xia, P. Lin, J. Chen, P. Huang, H. Liu, T. Tseng, E. Lin, and L. Chang, “Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125–1137.

56. Pendse, R., "Semiconductor device and method of forming extended semiconductor device with fan-out interconnect structure to reduce complexity of substrate," filed on Dec. 23, 2011, *US 2013/0161833 A1*, pub. date: June 27, 2013.
57. Yoon, S. W., P. Tang, R. Emigh, Y. Lin, P. C. Marimuthu, and R. Pendse, "Fan-out flip-chip eWLB (embedded wafer-level ball grid array) technology as 2.5D packaging solutions," *IEEE/ECTC Proceedings*, May 2013, pp. 1855–1860.
58. Lin, Y., W. Lai, C. Kao, J. Lou, P. Yang, C. Wang, et al., "Wafer warpage experiments and simulation for fan-out chip-on-substrate," *IEEE/ECTC Proceedings*, May 2016, pp. 13–18.
59. Chen, N. C., T. Hsieh, J. Jinn, P. Chang, F. Huang, J. Xiao, A. Chou, and B. Lin, "A Novel System in Package with Fan-out WLP for high speed SERDES application", *IEEE/ECTC Proceedings*, May 2016, pp. 1496–1501.
60. Lee, Y., W. Lai, I. Hu, M. Shih, C. Kao, D. Tarng, and C. Hung, "Fan-Out Chip on Substrate Device Interconnection Reliability Analysis", *IEEE/ECTC Proceedings*, May 2017, pp. 22–27.

# Chapter 10

## Low Loss Dielectric Materials



### 10.1 Introduction

Semiconductor industry has identified five major growth engines (applications) [1, 2]: (1) mobile such as smartphones, smartwatches, notebooks, wearables, tablets, etc., (2) high-performance computing (HPC), also known as supercomputing, which is able to process data and perform complex calculations at high speeds on a supercomputer, (3) autonomous vehicle (or self-driving cars), (4) IoTs (internet of things) such as smart factory and smart health, and (5) big data (for cloud computing) and instant data (for edge computing).

The system-technology drivers such as 5G (5th generation technology standard for broadband cellular networks) are boosting the growths of these 5 semiconductor applications. According to the US Federal Communications Commission: (a) the mid-band spectrum (also called Sub-6 GHz 5G) is defined as  $900 \text{ MHz} < \text{Frequency} < 6 \text{ GHz}$  and data speeds  $\leq 1 \text{ Gbps}$ , and (b) the high-band spectrum (also called 5G millimeter wave or 5G mmWave) is defined as  $24 \text{ GHz} \leq \text{Frequency} \leq 100 \text{ GHz}$  and  $1 \text{ Gbps} < \text{data speeds} \leq 10 \text{ Gbps}$ . The applications of Sub-6 GHz 5G and LTE (4G) coexist with large distance between antenna and multi-mode RF transceiver. The applications of 28/39 GHz are for, e.g., the antenna of 5G mobile generation, of 60 GHz are for, e.g., high-speed wireless data link, of 77 GHz are for, e.g., automotive radar, and of 94 GHz are for, e.g., radar imaging.

In order to meet the requirements for boosting signal transmission speed/rate and managing a huge data flood, advanced development of semiconductor, packaging, and materials, etc. are necessary. With respect to the electrical performance of insulation materials, low loss Df (dissipation factor or loss tangent) and Dk (dielectric constant or permittivity) materials are highly preferred for 5G applications [3–18]. In this chapter, the material properties of Df and Dk for high speed and frequency applications in the literature [3–18] of last three years are systematically presented. Why need low Df and Dk, and low coefficient of thermal expansion dielectric materials for 5G applications are briefly mentioned first.

$$\boxed{\text{Transmission Loss}} = \boxed{\text{Conductor Loss}} + \boxed{\text{Dielectric Loss}}$$

$$\boxed{\text{Conductor Loss}} \sim \text{Conductor Skin Resistance} \cdot \sqrt{D_k}$$

$$\boxed{\text{Dielectric Loss}} \sim f \cdot D_f \cdot \sqrt{D_k}$$

where

$f$  = Frequency

$D_f$  = Dissipation Factor (Loss Tangent)

$D_k$  = Dielectric Constant (Permittivity)

**Fig. 10.1** Transmission loss in a circuit

## 10.2 Why Need Low Dk and Df Dielectric Materials?

Figure 10.1 shows the transmission loss, which is equal to the sum of the conductor loss and dielectric loss. The dielectric loss is proportion to the frequency,  $D_f$ , and the square root of  $D_k$ . Thus, in order to have lower transmission loss lower values of  $D_f$  and  $D_k$  are needed.

Conductor loss is proportion to the conductor skin resistance and the square root of  $D_k$ . Usually, the higher the frequency the closer to the conductor surface the current signal flows (skin effect). For a rough surface conductor, the current signal is presumed to travel a longer distance on the surface, which leads to greater transmission loss. Thus, utilizing copper with lower surface roughness can reduce the conductor skin resistance. Conductor loss is out of the scope of this book.

## 10.3 Why Need Low CTE Dielectric Materials?

For multilayer substrate or RDLs (redistribution-layers), the insulating film (dielectric material) is used as an interlayer adhesive between the conductor layers. Since most conductor layers are made of electroplated Cu with a coefficient of thermal expansion (CTE)  $\sim 17.5 \times 10^{-6}/^\circ\text{C}$ , thus the low CTE ( $\leq 20-30 \times 10^{-6}/^\circ\text{C}$ ) dielectric materials are preferred. The advantages of small thermal expansion mismatch between the Cu conductor layers and the dielectric layer are; (a) less substrate warpage, (b) less interlayer delamination, and (c) better reliability.

Besides low  $D_f$ ,  $D_k$ , and CTE, the next generation dielectric materials require low moisture absorption, good mechanical and thermal properties to resist the inherent stresses in the substrate and RDLs. Also, the emerging dielectric materials must be low temperature curable, ease of manufacturability, and overcome the complexity of assembly.

## 10.4 NAMICS's Dk and Df

By proper filler selection and resin combination, NAMICS developed a stable dielectric material with low Df and Dk and good adhesion [3]. Figure 10.2 shows the appearance of the Film, which maintains sufficient flexibility while having low CTE resulting from added spherical silica particle ( $\text{SiO}_2$ ) filler. Their test vehicle is prepared by vacuum heat molding (under 200 °C, 1 MPa for 1 h) using an optimized resin composition. The test results are also shown in the table of Fig. 10.2. It can be seen that: (a) at 2 GHz, the  $D_k = 3$  and  $D_f = 0.0025$ , (b) the  $\text{CTE} = 25 \times 10^{-6}/\text{°C}$ , (c) the tensile strength = 630 MPa, and (d) the tensile strength on the Cu rough side ( $R_a = 1.8 \mu\text{m}$ ) is 7 N/cm and on the Cu shiny side ( $R_a = 0.25 \mu\text{m}$ ) is 5.5 N/cm. All these values are better than expected.

Figures 10.3 and 10.4 show the test results of the dielectric film's Df and Dk in different frequencies, respectively. It can be seen that the material properties of



Items	Film
$D_k$ (2GHz)	3
$D_f$ (2GHz)	0.0025
Tensile strength (MPa)	630
Cu peeling strength (N/cm) Cu rough side	7
Cu peeling strength (N/cm) Cu shiny side	5.5
CTE ( $10^{-6}/\text{°C}$ )	25
Tg (°C) (DMA)	150

Fig. 10.2 Appearance and material properties of film [3]

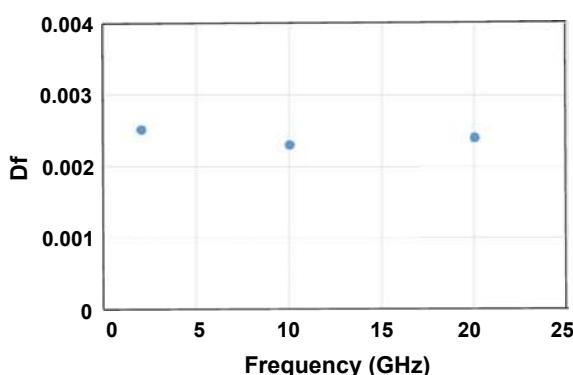


Fig. 10.3 Df versus frequency [3]

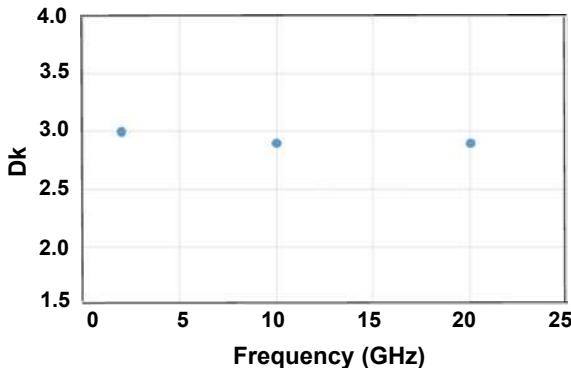


Fig. 10.4  $D_k$  versus frequency [3]

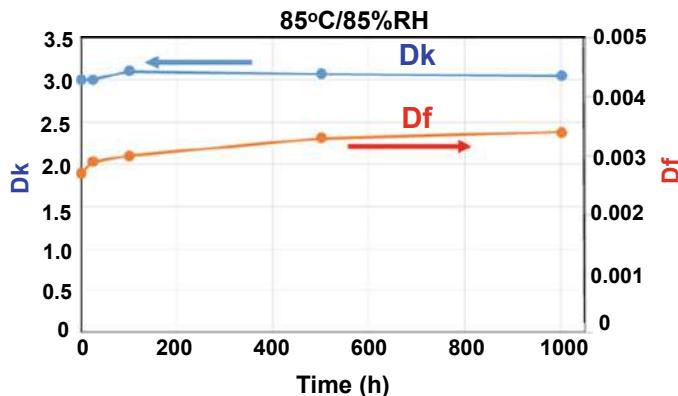
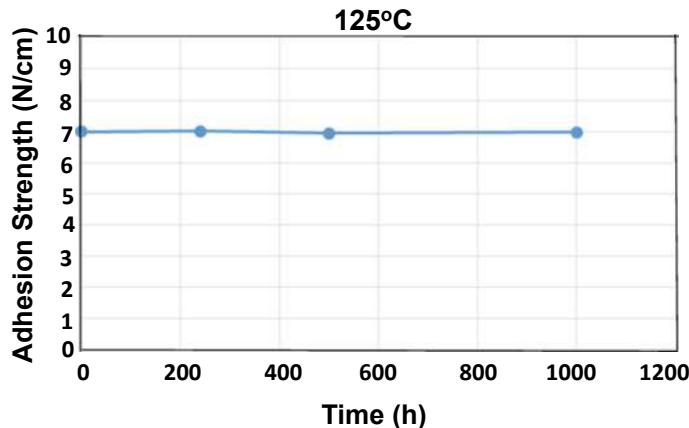
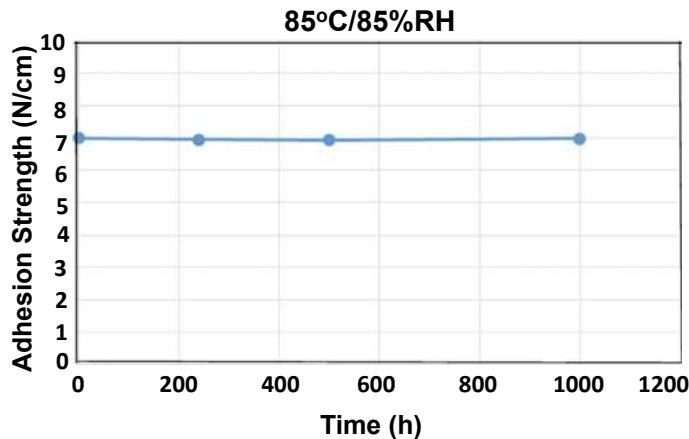


Fig. 10.5  $D_f$  and  $D_k$  versus time at 85 °C/85%RH [3]

the dielectric Film maintain at low  $D_k$  and low  $D_f$  with frequency-independent. Figure 10.5 shows the test results of the dielectric film's  $D_f$  and  $D_k$  at 85 °C/85%RH for up to 1000 h. It can be seen that (a) the  $D_k$  maintains the same at all times, and (b) the  $D_f$  increases slightly (from 0.0030 to 0.0034). The effect of temperature (125 °C) and 85 °C/85%RH on the adhesion strength of the dielectric film is shown in, respectively Figs. 10.6 and 10.7. It can be seen that the adhesion strength of the dielectric film maintains the same for up to 1000 h.



**Fig. 10.6** Adhesion strength versus time at 125 °C [3]

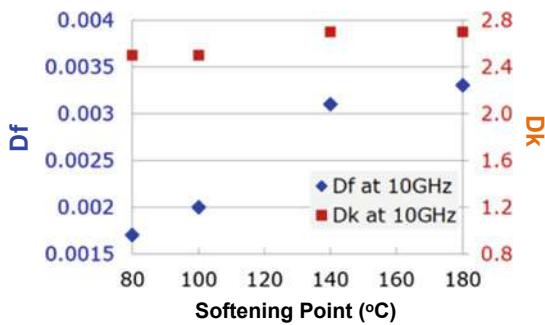


**Fig. 10.7** Adhesion strength versus time at 85 °C/85%RH [3]

## 10.5 Arakawa's Dk and Df

Arakawa [4] developed solvent-soluble polyimides with good heat resistance and low dielectric constant (Dk) and dissipation factor (Df) characteristics by optimizing the composition ratio of the aliphatic, cycloaliphatic, and aromatic groups presented in the polyimide back bone. Figure 10.8 shows the extent to which the properties (Dk and Df vs. softening point) of the polyimides could be controlled. It can be seen that the left vertical axis shows Df, while the right vertical axis shows Dk. The horizontal axis shows the Tg (softening point) of the polyimides. Red square points show Dk and blue rhombic points show Df. They are able to control the Df to less than 0.0035 and the Dk to less than 2.8 and the Tg from 80 to 180 °C of their polyimides.

**Fig. 10.8** Df and Dk versus softening point ( $T_g$ ) ( $^{\circ}\text{C}$ )



Items	Units	Values
Peeling Strength	N/mm	0.8
Fracture Elongation	%	100
Dk (10GHz) $T_g = 80^{\circ}\text{C}$	-	2.5
Df (10GHz) $T_g = 80^{\circ}\text{C}$	-	0.0017
Elastic modulus	GPa	0.136

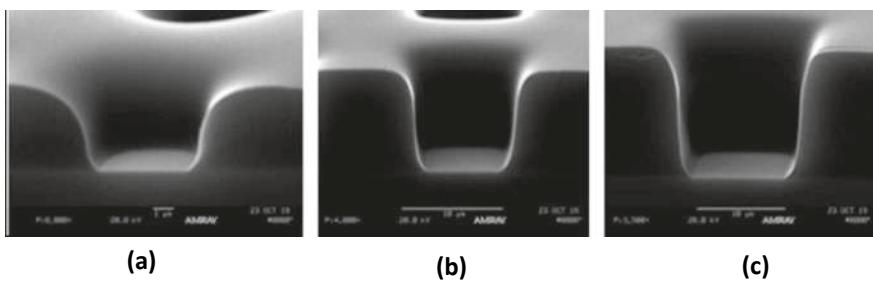
A flexible copper clad laminate (FCCL) is constructed with their polyimide (25  $\mu\text{m}$ ), sandwiched by adhesive layers (12–13  $\mu\text{m}$ ), and then sandwiched by rolled copper layers (12  $\mu\text{m}$ ). The 5-layer structure is subjected to peeling test. The results are shown in the table of Fig. 10.8. It can be seen that good adhesive strength (0.8 N/mm) between the polyimide film and low-profile copper foil is achieved. Also, at 10 GHz and  $T_g = 80^{\circ}\text{C}$  the  $Dk = 2.5$  and  $Df = 0.0017$ .

## 10.6 DuPont's Dk and Df

Based on the novel arylalkyl thermoset polymer chemistry that allows a lowered curing temperature, DuPont developed XP-Formulation A and XP-Formulation B for 5G photo-dielectric applications. The overall summary of properties of XP-Formulation A and XP-Formulation B is listed in Table 10.1 [5, 6]. Basically, XP-Formulation A uses an acrylic network to achieve negative tone contrast as its lithographic mechanism. The acrylic approach produces some desirable properties such as good glass transition temperature ( $T_g = 220^{\circ}\text{C}$ ), good chemical resistance and particularly good lithography. XP-Formulation B uses a new photosystem that is non-acrylate based in order to achieve high contrast (>1:1 aspect ratio) photo-patterning while achieving  $Df = 0.0022$  (28 GHz) and  $Df = 0.0029$  (77 GHz), and  $Dk = 2.5$  (10–40 GHz). The cross section of vias SEM (scanning electron microscope) images fabricated by XP-Formulation B are shown in Fig. 10.9a for 4.44  $\mu\text{m}$  CD in a 5  $\mu\text{m}$  film, Fig. 10.9b for 7.74  $\mu\text{m}$  CD in a 10  $\mu\text{m}$  film, and Fig. 10.9c for 10.14  $\mu\text{m}$  CD in a 15  $\mu\text{m}$  film.

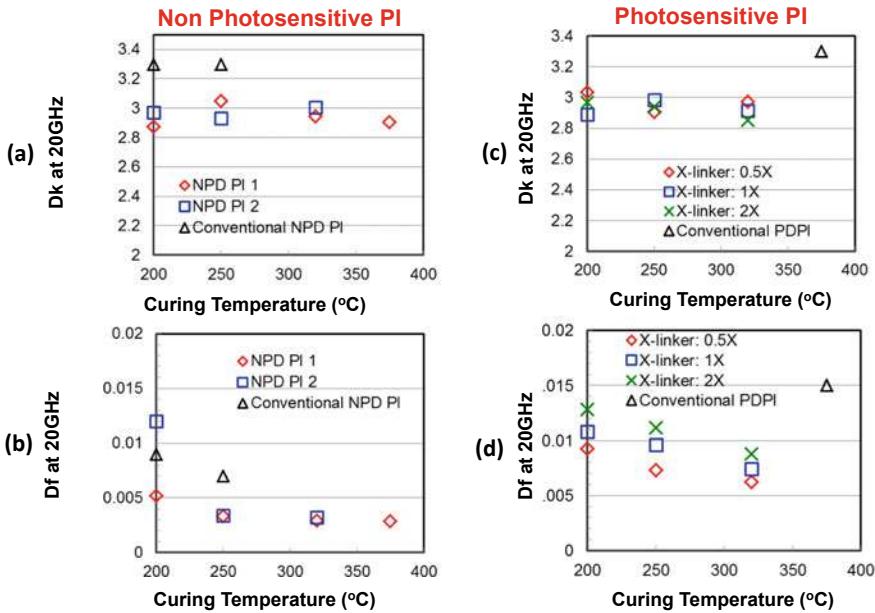
**Table 10.1** Material properties of formulation A and formulation B [6]

	XP-formulation A	XP-formulation B
Film thickness	5–25 $\mu\text{m}$	5–15 $\mu\text{m}$
Tensile strength (MPa)	91	85
Elongation at break (%)	12	18 (30% max)
Tensile modulus (GPa)	2.1	1.6
Dielectric constant (10–40 GHz)	2.6	2.5
Dissipation factor (28, 39, 60, 77 GHz)	0.0041, 0.0044, ND, ND	0.0022, 0.0024, 0.0028, 0.0029
Dissipation factor, post-HAST	No change	No change
Decomposition temperature ( $^{\circ}\text{C}$ )	300	320
Tg ( $^{\circ}\text{C}$ ), DMA	220	170
Water absorbance (23 $^{\circ}\text{C}$ /45%RH)	0.16%	0.13%
Aspect ratio	2.5 to 1	1 to 1
Resolution	5 $\mu\text{m}$ via	5 $\mu\text{m}$ via
Developer/Rinse	PGMEA/PGMEA	PGMEA/PGMEA
Single layer cure condition	170 $^{\circ}\text{C}$ @ 1 h	170 $^{\circ}\text{C}$ @ 1 h
Hard cure condition	200 $^{\circ}\text{C}$ @ 1 h	200 $^{\circ}\text{C}$ @ 1 h
Shelf life @ 20 $^{\circ}\text{C}$	>3 weeks	>3 weeks

**Fig. 10.9** SEM images of vias fabricated by XP-Formulation B. **a** For 4.44  $\mu\text{m}$  CD in a 5  $\mu\text{m}$  film. **b** For 7.74  $\mu\text{m}$  CD in a 10  $\mu\text{m}$  film. **c** For 10.14  $\mu\text{m}$  CD in a 15  $\mu\text{m}$  film [6]

## 10.7 Hitachi/DuPont MicroSystems' Dk and Df

Hitachi/DuPont MicroSystems developed a non-photosensitive and a photosensitive polyimide with excellent electrical and mechanical properties [7]. At first they redesigned the polymer backbone in order to obtain low Dk and Df performance. As a result, their new non-photosensitive PI achieved 2.9 of Dk at 20 GHz and 0.003 of Df

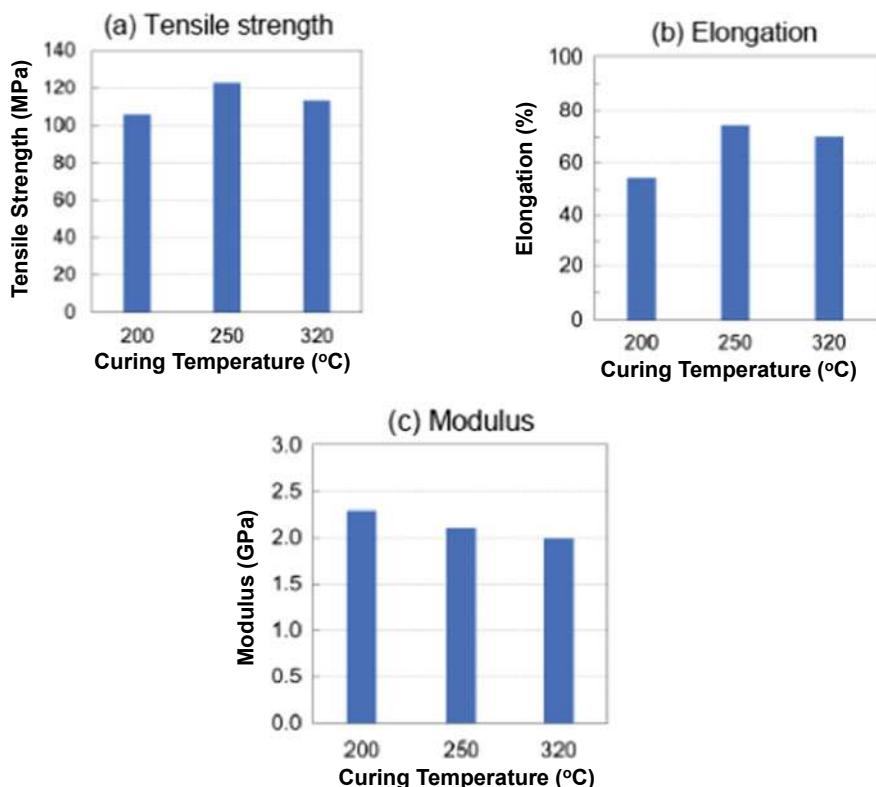


**Fig. 10.10** For non-photosensitive PI versus curing temperature (°C): **a** Dk and **b** Df. For photosensitive PI versus curing temperature (°C): **c** Dk and **d** Df

at 20 GHz, respectively as shown in Figs. 10.10a, b. In the next step, they selected the photo package of new PI carefully to maintain both low Dk/Df and high resolution. After that, they modified the photo initiator content, crosslinker content, and so on to have both high lithographic performance and high electrical performance. As a result, new photosensitive PI cured at 320 °C showed 3.0 of Dk at 20 GHz and 0.006 of Df at 20 GHz, respectively as shown in Figs. 10.10c, d. In addition, this material cured at 200 °C also showed 3.0 of Dk at 20 GHz and 0.009 of Df at 20 GHz. They also confirmed high mechanical properties of new PI (Fig. 10.11): (a) the elongation of this PI cured at >250 °C is approximately 70%, (b) the tensile strength is larger than 100 MPa, and (c) the modulus is larger than 2GPa. From lithographic aspects, the new PI achieved 15 μm L/S with 10 μm thickness.

## 10.8 JSR's Dk and Df

Figure 10.12 shows the Dk and the Df of various polymers [8, 9]. It can be seen that general materials having both low Dk and low Df include hydrocarbon-based materials are already on the market in addition to PTFE. Hydrocarbon-based polyolefin, hydrogenated rubber, COC and polystyrene exhibit Dk less than 2.5 and Df less than 0.001. These materials also have low water absorption property. However, many of



**Fig. 10.11** New photosensitive PI versus curing temperature (°C). **a** Tensile strength. **b** Elongation. **c** Young's modulus

the materials in Fig. 10.12 have weak adhesion property. In addition, depending on the material type, there is a practical problem in terms of heat resistance. Not only low Df but also properties such as adhesion to substrates and conductors, heat resistance and low CTE have to be taken into material design consideration. On the other hand, polyimides, which have excellent heat resistance and mechanical strength, have achieved low Df for high frequency FPC (flexible printed circuit board) application.

Figure 10.13 shows JSR's HC polymer based on aromatic polyether using their unique polymer synthesis technology. Table 10.2 (column three) shows the material properties of the JSR HC polymer. It can be seen that the  $Dk = 2.46$  and  $Df = 0.0027$  at 10 GHz. The modulus = 3 GPa, the tensile strength = 62 MPa, the elongation = 34%, and the  $T_g = 206$  °C. The HC polymer can be modified for easy control of the Df and Dk properties simply by selecting the monomer structure. For example, by using various monomers, the Df can be reduced to 0.002 at  $T_g$  around 150 °C as shown in Fig. 10.13.

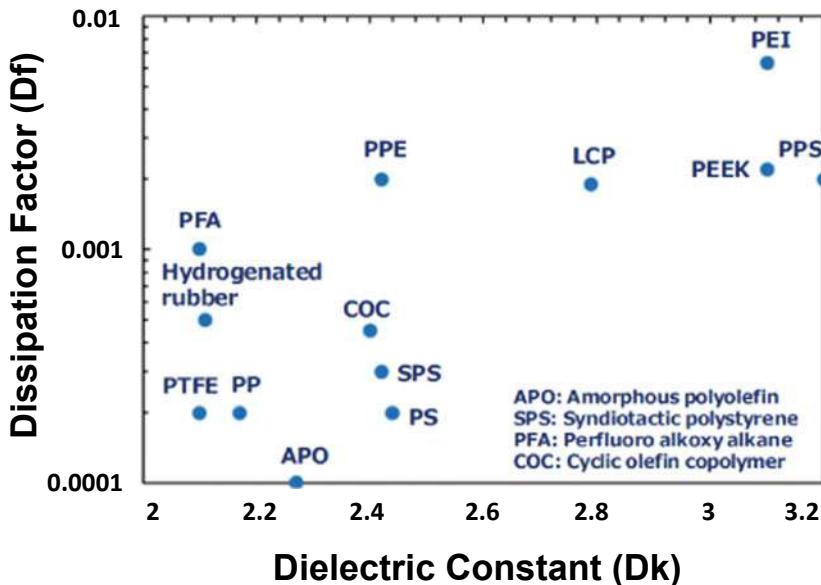


Fig. 10.12 Df and Dk of various polymers at 10 GHz [9]

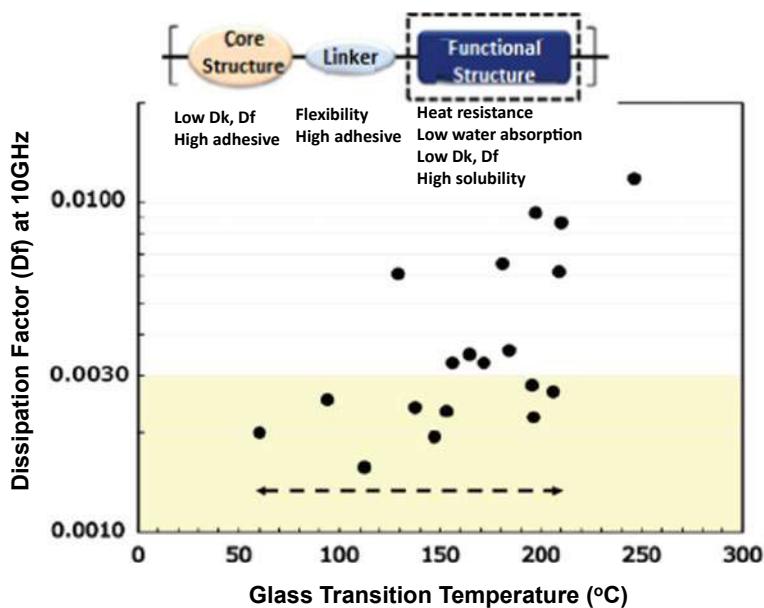
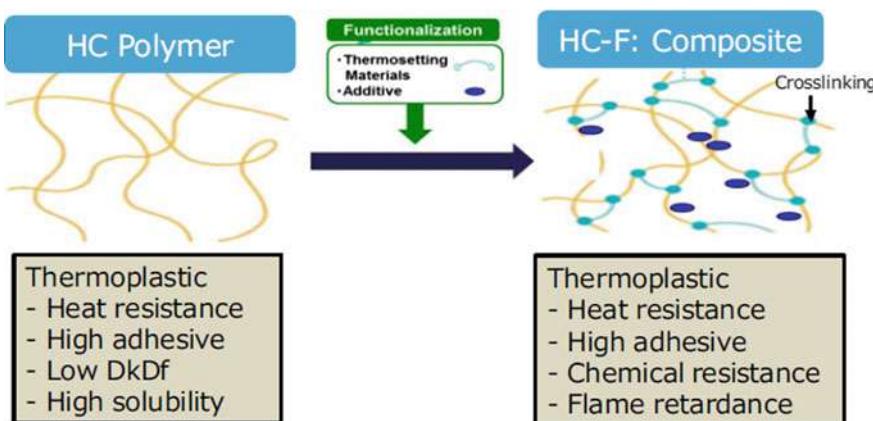


Fig. 10.13 Df versus Tg at 10 GHz of HC polymer [9]

**Table 10.2** Material properties of HC polymers [9]

Grade name		HC	HC-F composite (TPE)	
			HC-F	New HC-F
Basic information	Type		Thermoset	Thermoset
	Cure condition (°C/h)		185/1	185/1
Thermal property	Tg (°C)	206	168	138
	Solder resistance		Good	Good
Mechanical property	Modulus (GPa)	3.0	3.2	1.1
	Tensile strength (MPa)	62	86	48
	Elongation (%)	34	6	60
Electrical property	Dk @ 10 GHz	2.46	2.67	2.49
	Df @ 10 GHz	0.0027	0.0059	0.0016

**Fig. 10.14** HC-F composite of HC polymer [9]

Based on these HC polymers, thermosetting HC-F is developed targeting FPC applications [8, 9]. From a wide selection of crosslinkers, additives and other chemical components, tuning of the resultant thermosetting HC-F base polymer's characteristics such as thermal properties, mechanical property, and low Dk can be accomplished (Fig. 10.14). Table 10.2 (columns 4 and 5) shows the material properties of two types of thermosetting polyether HC-F composites. Their curing condition is 185 °C for 1 h. The Tg for the HC polymer is the highest (206 °C) and for the New HC-F polymer is the lowest (138 °C). The New HC-F polymer, test at 10 GHz, has the lowest Df (0.0016), the HC polymer is second (0.0027), and the HC-F polymer is the highest (0.0059). On the other hand, test at 10 GHz, the HC polymer has the lowest Dk (2.46), the New HC-F polymer is the second (2.49), and the HC-F polymer is the third (2.67). Thus, from low loss dielectric materials point of view, the New HC-F and the HC polymers can be used for high speed and frequency applications, especially the New HC-F polymer.

**Table 10.3** Material properties of polyimides [11]

	PI-A	PI-B	PI-C
Patterning method	Wet Etch laser	Laser	Photo-Litho. Laser
Dk (20 GHz)	3.0	2.7	2.7
Df (20 GHz)	0.003	0.002 (0.001*)	0.007
Tg (°C)	145	175	120
CTE ( $10^{-6}/^{\circ}\text{C}$ )	70	65	70
Young's modulus (GPa)	2	1.9	1.7
Tensile strength (MPa)	100	95	65
Elongation (%)	150	40	15
Moisture uptake (%)	0.6	0.6	0.6
Cure temperature (°C)	220	220	200

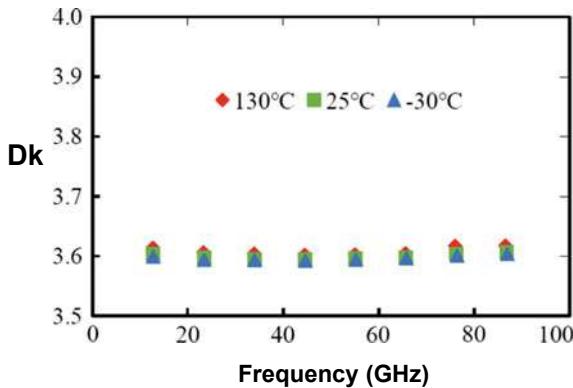
\*Result of 1 GHz

## 10.9 Toray's Dk and Df

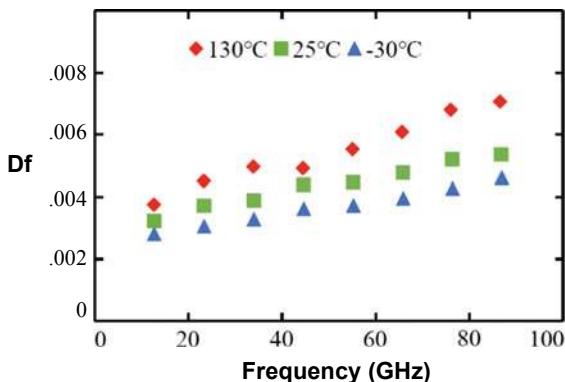
By investigate polyimides having various molecular mobility and polarity in polymer backbone, Toray understand how to design low Dk and Df polyimide [10–13]. They found that molecular mobility at  $-150$  to  $-50$  °C is corresponding to Df from 10 to 100 GHz. To reduce Df at GHz order, it is important to reduce molecular mobility at low temperature around  $-50$  °C. In addition, to reduce polarity and flexibility in the polyimide backbone is also important to obtain low Df and Dk polyimide. With these observations, Toray make two molecular designs, one is control of molecular mobility in polyimide chain and another is less polarity. Then, they develop three types of low Dk and Df polyimides (PI-A, PI-B, and PI-C) as shown in Table 10.3. It can be seen that the Dk = 2.7 and Df = 0.002 (at 20 GHz) of the PI-B polyimide are the lowest. The cure temperature of the PI-C polyimide is the lowest (200 °C). The tensile strength (100 MPa) and Young's modulus (2GPa) of the PI-A polyimide are the highest.

## 10.10 Fujitsu's Dk and Df

Based on the measurement of Cyclo Olefin Polymer (Zeon Corporation) with a thickness of 0.356 mm low-loss glass cloth substrate at various temperatures ( $-30$ ,  $25$ , and  $130$  °C) from 10 GHz to 95 GHz, Fujitsu obtained the Dk and Df as shown in Figs. 10.15 and 10.16, respectively [14]. It can be seen that: (a) Dk is approximately constant with respect to frequency, (b) there is very little change of Dk with respect to temperature, (c) Df is a function of frequency; the higher the frequency the higher the Df, and (d) Df is temperature dependent; the higher the temperature the higher the Df.



**Fig. 10.15** Dk versus frequency tested at  $-30$ ,  $25$ , and  $130$   $^{\circ}\text{C}$  [14]



**Fig. 10.16** Df versus frequency tested at  $-30$ ,  $25$ , and  $130$   $^{\circ}\text{C}$  [14]

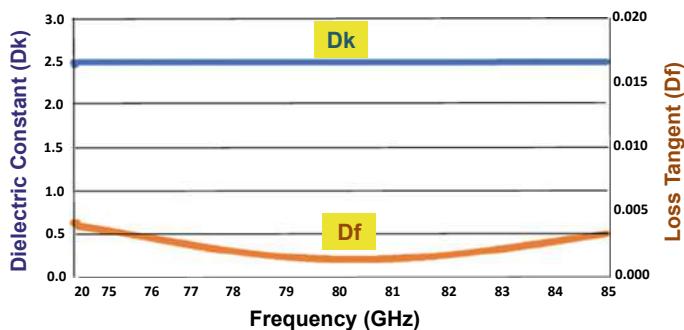
## 10.11 Kayaku's Dk and Df

Kayaku Advanced Materials and Nippon Kayaku have jointly synthesized a novel block co-polymer and formulation sensitive to photo curing. This unique material is referred to as PRL-29 [15]. PRL-29 is a negative tone resist that can be applied as a photo-patternable layer with post cure thickness of up to  $15\ \mu\text{m}$  with low temperature curing capability below  $225\ ^{\circ}\text{C}$ . The material properties of PRL-29 are shown in Table 10.4. It can be seen that the  $\text{Dk} = 2.5$  and  $\text{Df} = 0.004$  (average) for  $20$ – $85\ \text{GHz}$  (Fig. 10.17).

The glass transition temperature ( $T_g$ ) is  $220\ ^{\circ}\text{C}$  as shown in Fig. 10.18. The elongation and Young's modulus of the PRL-29 are, respectively  $35\%$  and  $1.8\ \text{GPa}$  (the slope of the liner stress vs. strain curve) as shown in Fig. 10.19. The Young's modulus versus temperature of the PRL-29 (Fig. 10.20) is just like other materials such as Epoxy and KMRD, the higher the temperature the lower the Young's modulus.

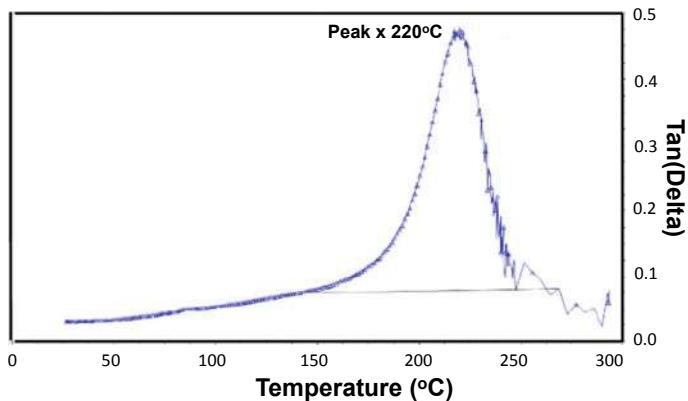
**Table 10.4** Material properties of PRL-29 [15]

Item	PRL-29
Cure temperature (°C)	200
Aspect ratio	1:1
Tg (°C)	220
Young's modulus (GPa)	1.8
Tensile strength (MPa)	60
Elongation at break (max) (%)	35
CTE ( $<\text{Tg}$ ) ( $10^{-6}/^\circ\text{C}$ )	62
Shear adhesion (MPa)	35
Dielectric constant (1–85 GHz)	2.5
Dissipation factor (1–85 GHz)	0.004
Water absorbance (%)	0.3
Thermal conductivity (W/m/K)	0.23
PCT (121 °C/100%RH, 48 h)	Pass
Bias HAST (85/85RH, 3.3 V, 168 h)	Pass
Chemical resistance	Excellent

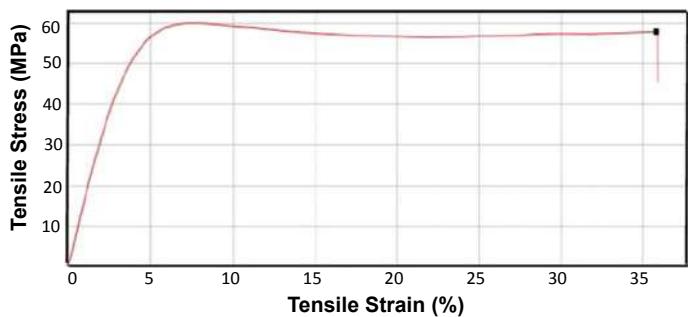


**Fig. 10.17** Df and Dk versus frequency [15]

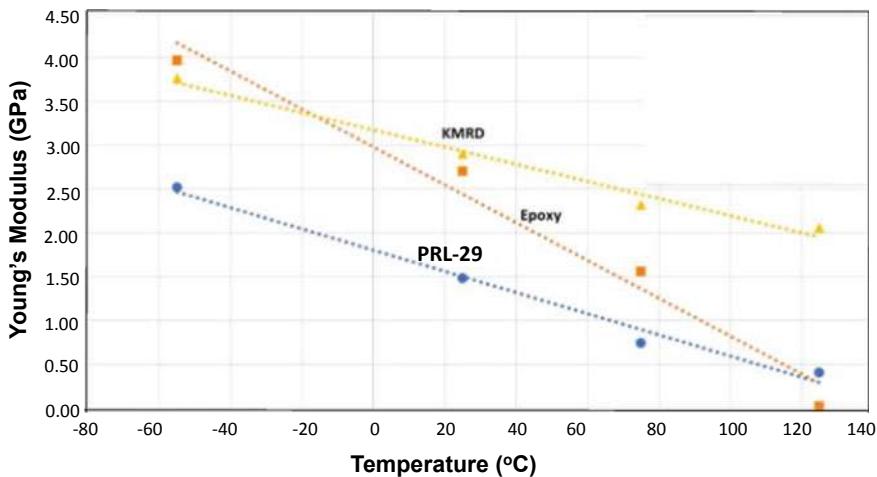
It is noted that the Young's modulus of the PRL-29 is smaller than that of the Epoxy and KMRD. This means PRL-29 is softer, which leads to less stress with increased strain. Also, the curing temperature of the PRL-29 is about 200 °C. Figures 10.21a, b show, respectively the 20 μm via on a 15 μm-thick film and the 15 μm metal linewidth and spacing on a 15 μm-thick film. All these properties are essential for electrical performance and mechanical/thermal integrity of 5G applications.



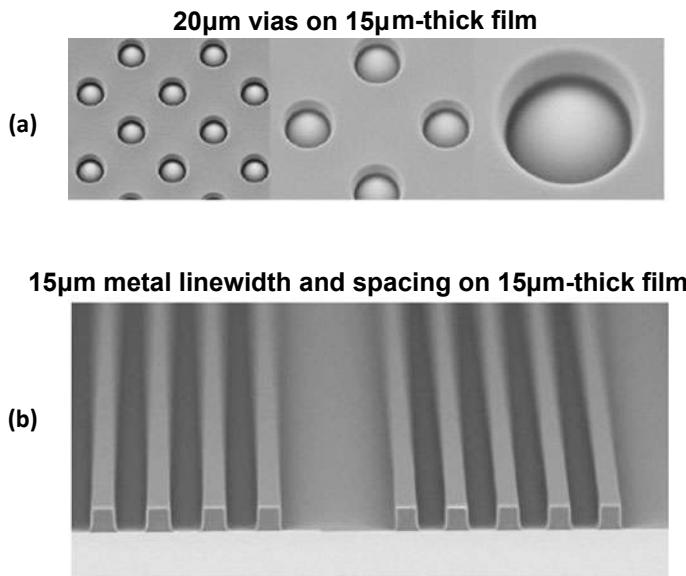
**Fig. 10.18** Glass transition temperature ( $T_g = 220\text{ }^{\circ}\text{C}$ ) of PRL-29 [15]



**Fig. 10.19** Stress-stain curve of PRL-29 (elongation = 35%) [15]



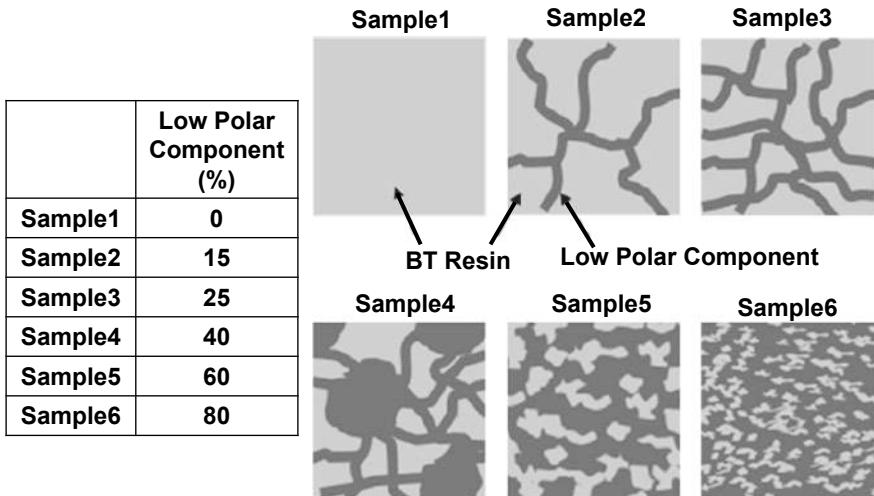
**Fig. 10.20** Young's modulus versus temperature of PRL, KMRD, and epoxy materials [15]



**Fig. 10.21** With PRL-29 material: **a** 20  $\mu\text{m}$  vias on 15  $\mu\text{m}$ -thick film and **b** 15  $\mu\text{m}$  metal linewidth and spacing on 15  $\mu\text{m}$ -thick film [15]

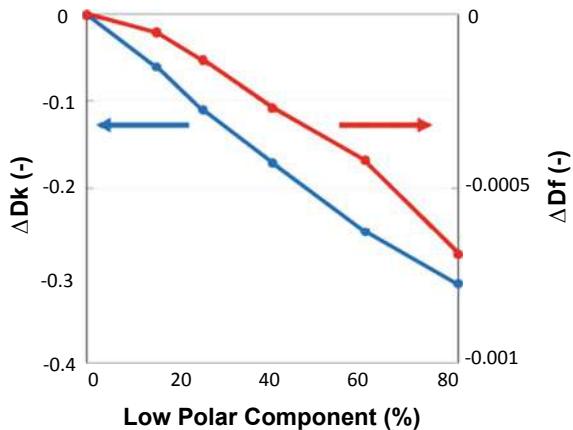
## 10.12 Mitsubishi's Dk and Df

In [16] Mitsubishi developed a new additional low polar component for BT (bismaleimide triazine) resins and combined with the main component by the newly developed polymer blending technology. To search for the optimal ratio of the low polar component in the material formulation, a feasibility study with several BT composites are conducted prior to fabrication of laminates. The table in Fig. 10.22 shows the contents of the low polar component in the BT composites. For example, Sample1 did not contain any polar component, while 80% of the composite is the low polar component in Sample6. The cross sections of the samples are also shown in Fig. 10.22 (the light gray area is for the main components and the dark gray area is for the low polar component.) It is found that [16], 25% (Sample3) is optimal for BT composite in the use of networking. Figure 10.23 shows the electrical material properties of the BT composites. It can be seen that both Dk and Df reduce as the low polar component increases. The effects of 85 °C/85%RH and temperature (130 °C) on the Df are shown, respectively in Figs. 10.24 and 10.25. It can be seen that (a) the Df (at 10 GHz) increase as with time at 85 °C/85%RH, and (b) the Df (at 10 GHz) remains the same as with time at 130 °C. Also, from Figs. 10.24 to 10.25, the Df = 0.0025 at 10 GHz.



**Fig. 10.22** Cross-section images of BT composites with low polar component. Dark gray area means low polar component and light gray area means main components [16]

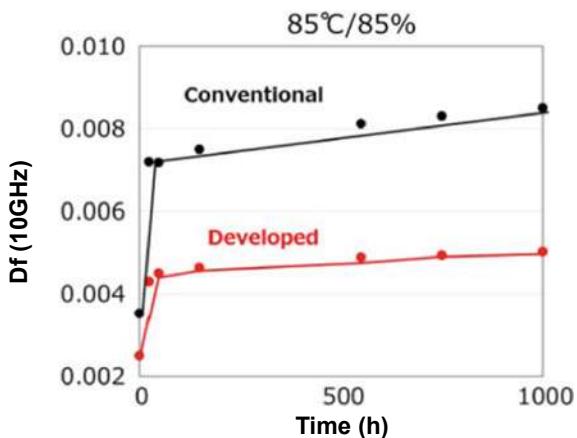
**Fig. 10.23** Df and Dk versus low polar component [16]



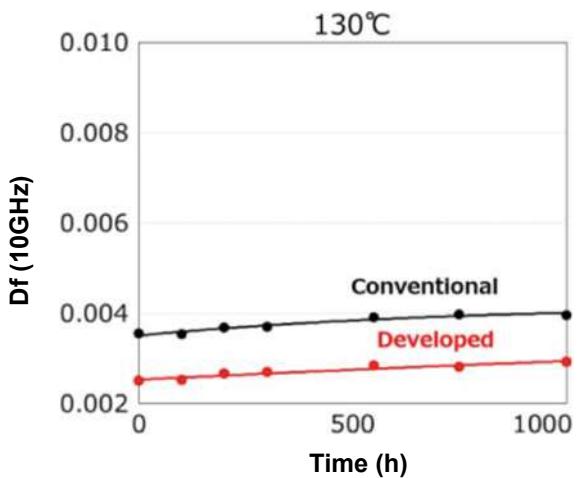
## 10.13 TAITO INK's Dk and Df

By optimized the epoxy and silica blend, a novel dry film build-up material has been developed to achieve low transmission loss for the next-generation substrates by TAITO INK [17]. The left-side of Fig. 10.26 shows a molecular structure with cross-linking points in the traditional material design. The new design (Material A) utilizes a new curing system with a lower polarity structure and lower number of crosslinking points with large portion of silica fillers (the right-side of Fig. 10.26). Figure 10.27 shows the dry-film Material A manufactured in the form of commercially-useful rolls.

**Fig. 10.24** Df versus time at 85 °C/85%RH [16]



**Fig. 10.25** Df versus time at 130 °C [16]



The material properties of Material A are shown in Table 10.5. It can be seen that  $D_f = 0.0025$  and  $D_k = 3.2$  at 10 GHz under SPDR (split post dielectric resonator) and can be used for frequencies from 10 to 80 GHz as shown in Fig. 10.28. Figure 10.29 shows the metal line images formed by Material A and the conventional materials. It can be seen that, with the Material A, the surface of metal lines are smoother, which is due to the use of reduced nano-silica size and the improvement in the dispersibility of the resin and the silica.

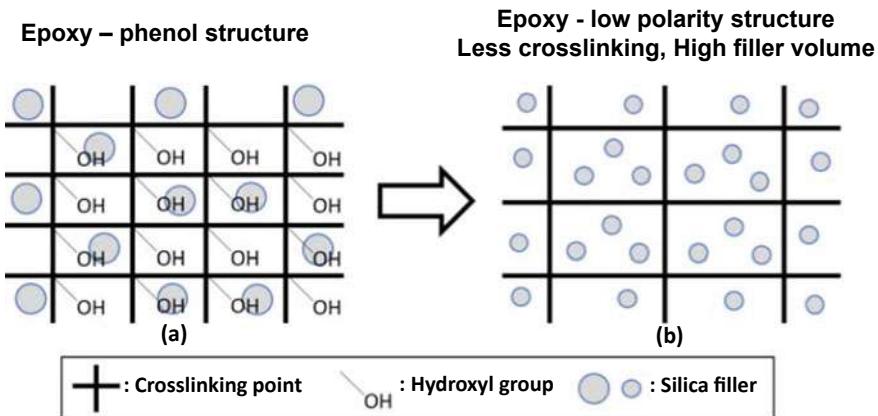


Fig. 10.26 a Traditional epoxy-based material. b Newly-designed low-polarity material [17]

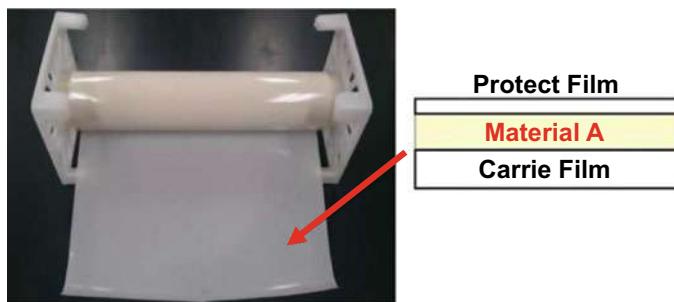
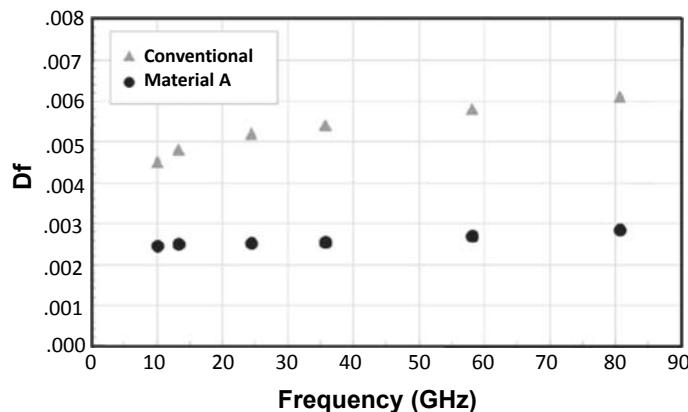


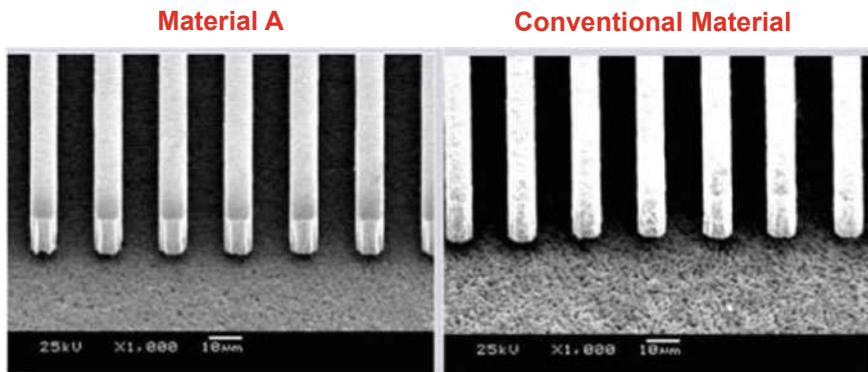
Fig. 10.27 Low Df dry film build-up material (Material A) [17]

Table 10.5 Material properties of Material A [17]

Cured material properties	Material A	Conventional material
Dk (10 GHz, SPDR)	3.2	3.4
Df (10 GHz, SPDR)	0.0025	0.0045
Frequency	10–80 GHz	10 GHz
CTE (30–100 °C)	$18 \times 10^{-6}/^{\circ}\text{K}$	$17 \times 10^{-6}/^{\circ}\text{K}$
Tg (TMA)	160 °C	170 °C
Young's modulus	10 GPa	12 GPa



**Fig. 10.28** Df versus frequency. Comparison between the conventional material and Material A [17]

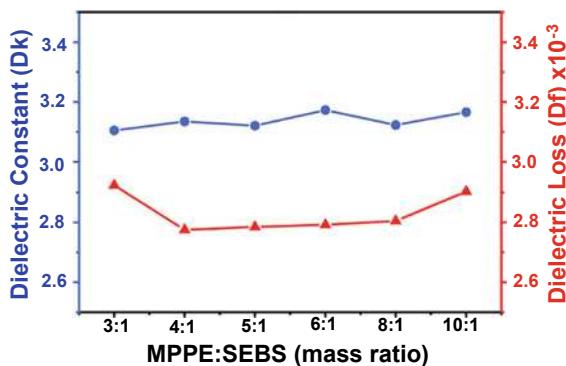


**Fig. 10.29** SEM images of surface state after flash etching: Material A versus conventional material [17]

## 10.14 Zhejiang University's Dk and Df

In [18], Zhejiang University provided the electrical material properties (Dk and Df) of P-CCL (PCB-copper clad laminate) and LT-CCL ( $\text{Li}_2\text{TiO}_3$ -copper clad laminate). The composite laminates obtained with resins and E-glass fabrics are abbreviated as P-CCLs. Similarly, the composite laminates (MPPE:SEBS = 5:1) filled with LT ceramic powders are abbreviated as LT-CCLs. Figure 10.30 shows the Dk and Df of P-CCLs with different weight ratio between MPPE (modified poly phenylene ether) and SEBS (styrene-ethylene/butylene-styrene). It can be seen that the Dk of P-CCLs maintains at 3.1. The dielectric loss of P-CCLs shown in Fig. 10.30 is within 0.0027–0.0029 at 10 GHz, which is a quite competitive value in the manufacturing and application of CCLs.

**Fig. 10.30** Df and Dk versus MPPE: SEBS (mass ratio) of P-CCL material



**Fig. 10.31** Df and Dk versus LT/resin (mass ratio) of LT-CCL

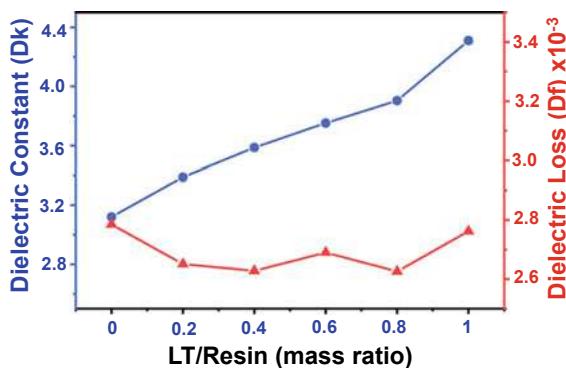


Figure 10.31 shows the effect of LT ceramic powders content on the Dk and Df of LT-CCLs when the weight ratio of MPPE to SEBS is 5:1. It can be seen that the Dk is a function of the LT ceramic powders content; the higher the LT content the higher the Dk. On the other hand, the Df gets lower and remains between 0.0026 and 0.0028 at 10 GHz for the addition of LT ceramic powders. Besides, the Df of LT-CCLs exhibits a slight rise with the weight ratio increased to 1 as shown in Fig. 10.31.

## 10.15 Summary and Recommendation

Some important results and recommendations are summarized as follows.

- The most important task in high speed and frequency circuits is to reduce transmission loss, which is equal to the sum of conductor loss and dielectric loss. The solution to conductor loss is to use high adhesion technology for very low surface roughness Cu foil, and the solution to dielectric loss is to use excellent dielectric properties and stable low loss Dk and Df for a wide range of frequency, temperature, humidity, etc.

- For high speed and frequency applications such as 5G, the dielectric materials are not only should be low loss (value) and stable D<sub>k</sub> and D<sub>f</sub> through varied humidity conditions, but also should have low CTE, low curing temperature, low Young's modulus (< 2GPa), low moisture absorption (< 0.3%), low shrinkage during curing (< 5%), high elongation, high tensile strength, long shelf life, easy of manufacturability, suitable for assembly, etc.
- The low loss D<sub>k</sub> and D<sub>f</sub> of various dielectric materials from different companies have been systematically presented.
- Based on the reported D<sub>f</sub> and D<sub>k</sub> from literatures, the roadmaps of D<sub>f</sub> and D<sub>k</sub> for the next five years are shown in Figs. 10.32 and 10.33, respectively.

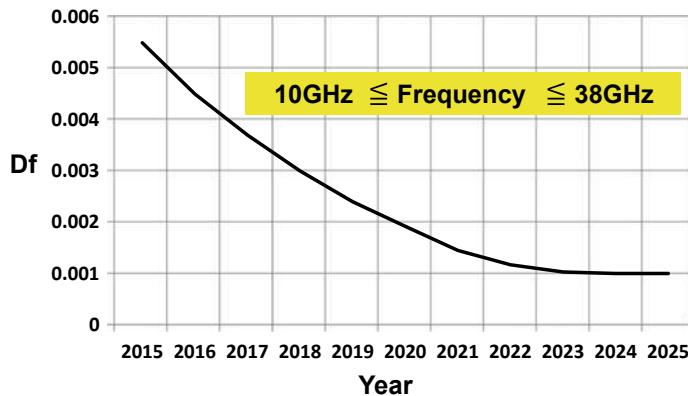


Fig. 10.32 Roadmap of D<sub>f</sub> in the next 5 years

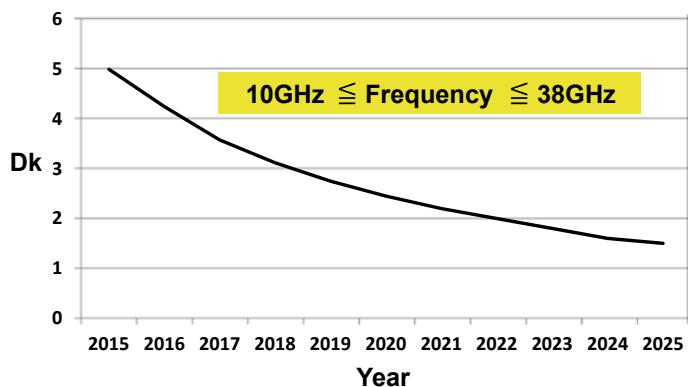


Fig. 10.33 Roadmap of D<sub>k</sub> in the next 5 years

## References

1. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
2. Lau, J. H., *Heterogeneous Integration*, Springer, New York, 2019.
3. Sato, J., S. Teraki, M. Yoshida, and H. Kondo, “High Performance Insulating Adhesive Film for High-Frequency Applications”, *Proceedings of IEEE/ECTC*, May 2017, pp. 1322–1327.
4. Tasaki, T., “Low Transmission Loss Flexible Substrates using Low Dk/Df Polyimide Adhesives”, *TechConnect Briefs*, V4, May 2018, pp. 75–78.
5. Hayes, C., K. Wang, R. Bell, C. Calabrese, J. Kong, J. Paik, L. Wei, K. Thompson, M. Gallagher, and R. Barr, “Low Loss Photodielectric Materials for 5G HS/HF Applications”, *Proceeding of International Symposium on Microelectronics*, October 2019, pp. 1–5.
6. Hayes, C., K. Wang, R. Bell, C. Calabrese, M. Gallagher, K. Thompson, and R. Barr, “High Aspect Ratio, High Resolution, and Broad Process Window Description of a Low Loss Photodielectric for 5G HS/HF Applications Using High and Low Numerical Aperture Photolithography Tools”, *Proceedings of IEEE/ECTC*, May 2020, pp. 623–628.
7. Matsukawa, D., N. Nagami, K. Mizuno, N. Saito, T. Enomoto, and T. Motobe, “Development of Low Dk and Df Polyimides for 5G Application”, *Proceeding of International Symposium on Microelectronics*, October 2019, pp. 1–4.
8. Ito, H., K. Kanno, A. Watanabe, R. Tsuyuki, R. Tatara, M. Raj, and R. Tummala, “Advanced Low-Loss and High-Density Photosensitive Dielectric Material for RF/Millimeter-Wave Applications” *Proceedings of International Wafer Level Packaging Conference*, October 2019, pp. 1–6.
9. Nishimura, I., S. Fujitomi, Y. Yamashita, N. Kawashima, and N. Miyaki, “Development of new dielectric material to reduce transmission loss”, *Proceedings of IEEE/ECTC*, May 2020, pp. 641–646.
10. Araki, H., Y. Kiuchi, A. Shimada, H. Ogasawara, M. Jukei, and M. Tomikawa, “Low Df Polyimide with Photosensitivity for High Frequency Applications”, *Journal of Photopolymer Science and Technology*, V33, 2020, pp. 165–170.
11. Araki, H., Y. Kiuchi, A. Shimada, H. Ogasawara, M. Jukei, and M. Tomikawa, “Low Permittivity and Dielectric Loss Polyimide with Patternability for High Frequency Applications”, *Proceedings of IEEE/ECTC*, May 2020, pp. 635–640.
12. Tomikawa, M., H. Araki, M. Jukei, H. Ogasawara, and A. Shimada, “Low Temperature Curable Low Df Photosensitive Polyimide”, *Proceeding of International Symposium on Microelectronics*, October 2019, pp. 1–5.
13. Tomikawa, M., H. Araki, M. Jukei, H. Ogasawara, and A. Shimada, “Hsigh Frequency Dielectric Properties of Low Dk, Df Polyimides”, *Proceeding of International Symposium on Microelectronics*, October 2020, pp. 1–5.
14. Takahashi, K., S. Kikuchi, A. Matsui, M. Abe and K. Chouraku, “Complex Permittivity Measurements in a Wide Temperature Range for Printed Circuit Board Material Used in Millimeter Wave Band”, *Proceedings of IEEE/ECTC*, May 2020, pp. 938–945.
15. Han, K., Y. Akatsuka, J. Cordero, S. Inagaki, and D. Nawrocki, “Novel Low Temperature Curable Photo-Patternable Low Dk/Df for Wafer Level Packaging (WLP)”, *Proceedings of IEEE/ECTC*, May 2020, pp. 83–88.
16. Yamamoto, K., S. Koga, S. Seino, K. Higashita, K. Hasebe, E. Shiga, T. Kida, and S. Yoshida, “Low Loss BT resin for substrates in 5G communication module”, *Proceedings of IEEE/ECTC*, May 2020, pp. 1795–1800.
17. Kakutani, T., D. Okamoto, Z. Guan, Y. Suzuki, M. Ali, A. Watanabe, M. Kathaperumal, and M. Swaminathan, “Advanced Low Loss Dielectric Material Reliability and Filter Characteristics at High Frequency for mmWave Applications”, *Proceedings of IEEE/ECTC*, May 2020, pp. 1795–1800.
18. Guo, J., H. Wang, C. Zhang, Q. Zhang, and H. Yang, “MPPE/SEBS Composites with Low Dielectric Loss for High-Frequency Copper Clad Laminates Applications”, *Polymers*, V12, August 2020, pp. 1875–1887.

# Chapter 11

## Advanced Packaging Trends

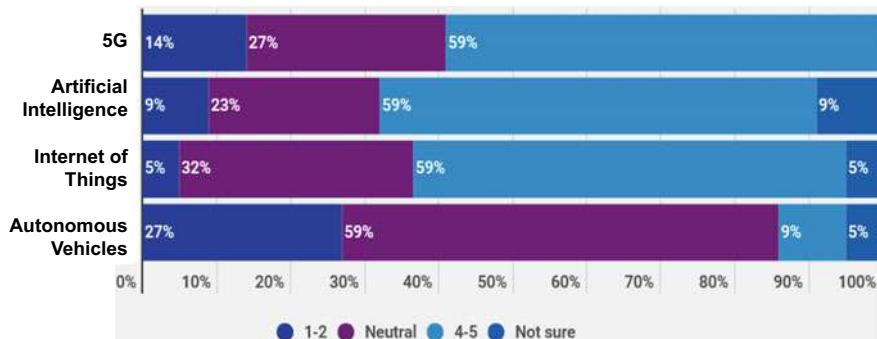


### 11.1 Introduction

The trends in advanced packaging will be presented in this chapter. The trends in assembly processes such as SMT (surface mount technology), wire bonding technology, flip chip technology, and CoC (chip-on-chip), CoW (chip-on-wafer), and WoW (wafer-on-wafer) TCB (thermocompression bonding) and hybrid bonding will also be briefly discussed. The trends in SoC (system-on-chip) and chiplets will be provided. The impact of COVID-19 on semiconductor industry will be briefly mentioned first.

### 11.2 The Impact of COVID-19 on Semiconductor Industry

KPMG collaborate with the GSA (Global Semiconductor Alliance) to conduct a pulse survey on the impact of COVID-19 on the semiconductor industry [1]. Their key findings on the impact of COVID-19 on the investment, growth, and adoption of the 5G (5th Generation Technology Standard for Broadband Cellular Networks), artificial intelligence (AI), internet of things (IoTs), and autonomous vehicles end markets are shown in Fig. 11.1 (rating scale: 1 = significantly negative impact and 5 = significantly positive impact). It can be seen that most of the participants consider the impact of COVID-19 on the investment, growth, and adoption of 5G, AI, IoTs, and self-driving cars are positive.



**Fig. 11.1** Impact of COVID-19 on the investment, growth, and adoption of the 5G, AI, IoTs, and autonomous vehicles (rating scale: 1 = significantly negative impact and 5 = significantly positive impact)

### 11.3 The Impact of COVID-19 on Foundry Industry

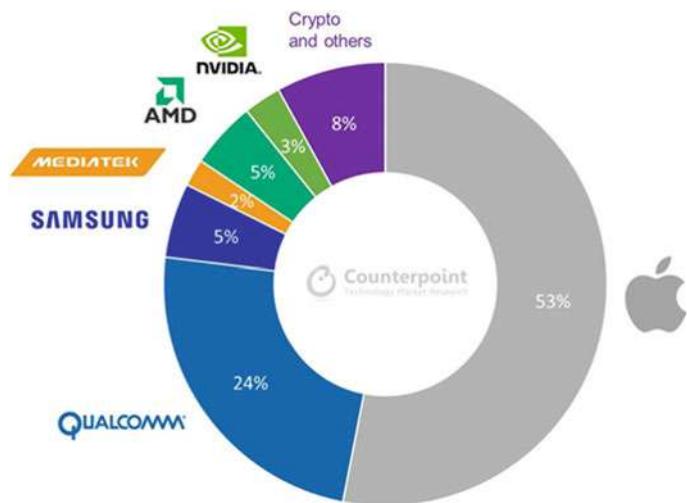
The impact of COVID-19 on foundry industry is leading to logistical challenges and trade tensions prompting increase in wafer bookings. COVID-19 is a favorable macro environment. This is compounded with the process technology migrations in advanced nodes such as 7 and 5 nm + EUV (extreme ultraviolet) lithography appear to be accelerating to meet the demand from 5G smartphones, AI HPC (high performance computing), and AI/GPU (graphics processing unit)/FPGA (field-programmable gate array) in big data (for cloud computing) and instant data (for edge computing).

In 2020, the foundry industry revenue reached about \$82 billion, representing a 23% YoY (year-over-year) growth. Despite this high base of 2020, the double-digit growth will persist in 2021. Counterpoint forecast a 12% YoY growth with total revenue of \$92 billion in 2021 and \$100 billion during 2022–2023 [2]. The world largest foundry (TSMC) is expected to keep outperforming the industry by posting 13–16% YoY sales growth in 2021.

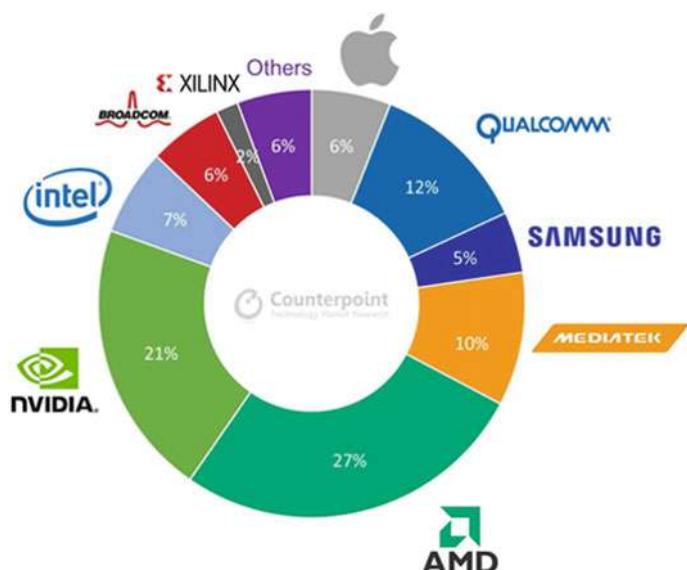
### 11.4 The Impact of COVID-19 on the Semiconductor Customers

In 2021, there are only two companies (TSMC and Samsung) in the world who can do 5 and 7 nm process technology. According to Counterpoint [3], the potential customers for 5 nm in 2021 are shown in Fig. 11.2 and 7 nm are shown in Fig. 11.3. The COVID-19 will not slow down the growth of semiconductor customers.

For the 5 nm process technology, Apple is the top customer (with all orders to TSMC) in 5 nm in 2021 (Fig. 11.2), including both for iPhones (A14/A15) and the newly released Apple Silicon. Qualcomm will be the second-largest 5 nm customer



**Fig. 11.2** Potential customers for 5 nm process technology in 2021



**Fig. 11.3** Potential customers for 7 nm process technology in 2021

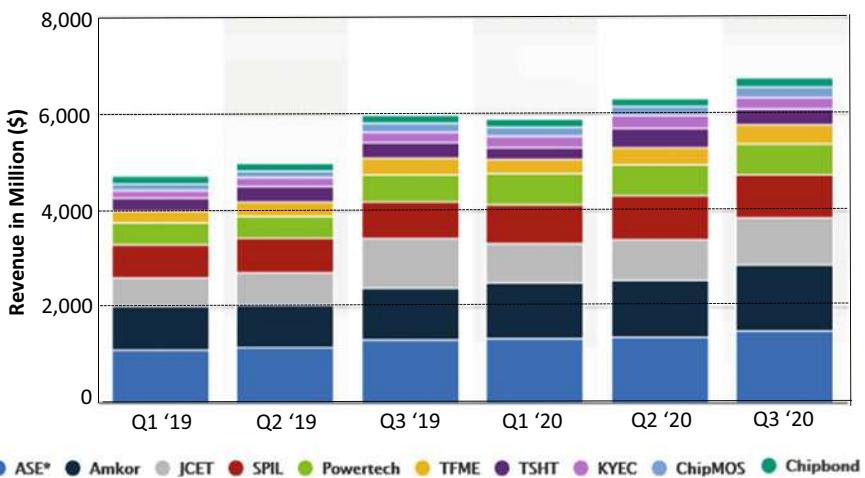
as the iPhone 13 may adopt its X60 modem. TSMC is expected to book \$10-billion revenue from 5 nm in 2021. Samsung Foundry will also gain good traction from 5 nm order wins, including its in-house (Exynos) SoC (system-on-chip) and Qualcomm.

For the 7 nm process technology, it is different from 5 nm, with over 80% wafers used in smartphones, the 7 nm applications are more diversified into AI/GPUs, CPUs

(central processing unit), networking and automotive processors. TSMC has a variety of 7 nm (DUV (deep ultraviolet) only), 7 nm plus (with EUV) and 6 nm (with EUV) in its 7 nm family, while Samsung has introduced 7 nm/6 nm with both adopting EUV production. In this geometry, smartphones will only consume 35% of wafers (Fig. 11.3) and the majority will ship to AMD (27% of 7 nm shipment volume) and NVidia (21%). In the light of stronger demand for game consoles, cloud server/AI processors and mainstream 5G smartphones, the capacity for 7 nm looks extremely tight through the whole of 2021. Therefore, for emerging demand such as crypto-mining ASIC and ARM-based processors (in server and automotive), the chipset vendors and OEMs will find it difficult to get allocation for extra capacities in the near term.

## 11.5 The Impact of COVID-19 on Packaging Industry

OSAT (outsourced semiconductor assembly and test) market was valued at \$31.64 billion in 2020 and is expected to reach \$49.71 billion at a CAGR (compound annual growth rate) of 7.3% over the forecast period (2021–2026) [4]. The increased demand from automotive subsystems and connected devices are said to be the main driving force in the forecasted period. The smartphone segment was the biggest customer of OSAT providers, with more than 1 billion shipments last year. The introduction of 5G is further going to bring a new lease of life to the market. Connectivity is the core of Industry 4.0 due to which there demand edge computing and IoT device is said to grow exponentially in the future. The impact of COVID-19 on the OSAT market in 2020 can be seen from Fig. 11.4 [4]. The demand for end-devices such as



**Fig. 11.4** OSAT revenues in 2019 and 2020

notebooks and tablets sees a continued growth due to the rise of the stay-at-home or safer-at-home order/economy brought about by the COVID-19 pandemic.

## 11.6 Drivers, Semiconductor, and Advanced Packaging

The Semiconductor industry has identified five major growth engines (applications):

- Mobile
- HPC
- Autonomous vehicle
- IoTs
- Big data (for cloud computing) and instant data (for edge computing).

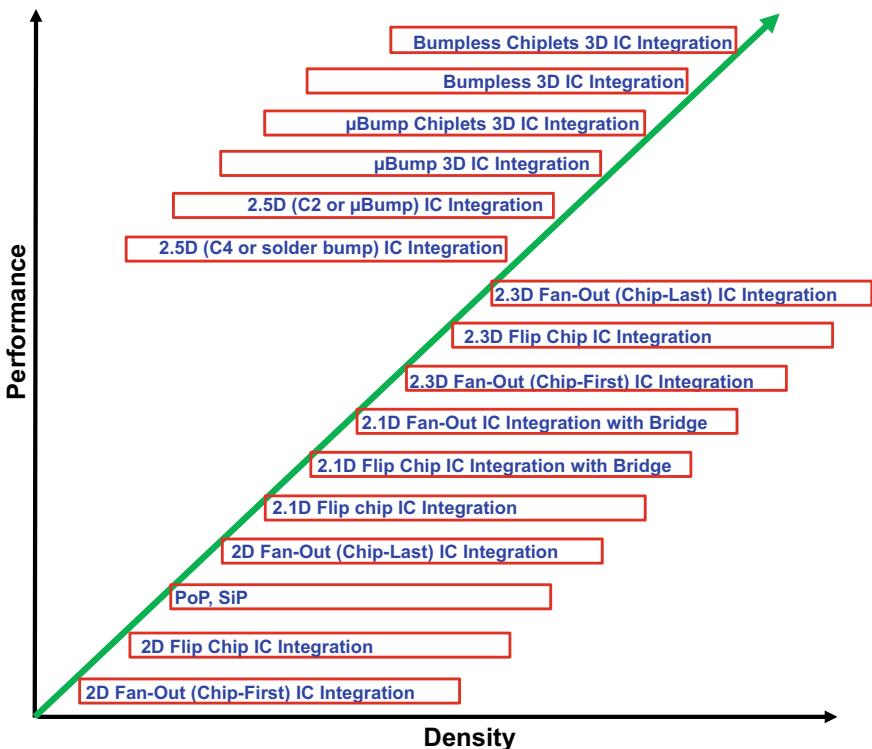
The following system-technology drivers are boosting the growths of the 5 semiconductor applications:

- AI
- 5G.

The advanced packaging technologies housing the semiconductors are:

- 2D fan-out (chip-first) IC integration,
- 2D flip chip IC integration,
- PoP (package-on-package),
- SiP (system-in-package) or heterogeneous integration,
- 2D fan-out (chip-last) IC integration,
- 2.1D flip chip IC integration,
- 2.1D flip chip IC integration with bridges,
- 2.1D fan-out IC integration with bridges,
- 2.3D fan-out (chip-first) IC integration,
- 2.3D flip chip IC integration,
- 2.3D fan-out (chip-last) IC integration,
- 2.5D (solder bump) IC integration,
- 2.5D ( $\mu$ bump) IC integration,
- $\mu$ bump 3D IC integration,
- $\mu$ bump chiplets 3D IC integration,
- Bumpless 3D IC integration,
- Bumpless chiplets 3D IC integration.

The density and performance range of the above advanced packaging are shown in Fig. 11.5 and they are grouped in Fig. 11.6. Their substrates size and pin-count on substrate, in the next 5 years, are shown in Fig. 11.7. It can be seen that, for build-up package substrate the size can be  $5000 \text{ mm}^2$ , the pin-count can be 6000, and the metal L/S  $\geq 6 \mu\text{m}$  (for 2.1D with thin-film layer on top of the build-up layer, the metal L/S  $\geq 2 \mu\text{m}$ ); for TSV-interposer the substrate size can be  $3000 \text{ mm}^2$ , the pin-count can be  $> 100,000$ , and the metal L/S  $\leq 1 \mu\text{m}$ ; for fan-out (chip-first) RDL-substrate (or



**Fig. 11.5** Performance and density of advanced packaging

interposer) the substrate size can be  $600 \text{ mm}^2$ , the pin-count can be 2500, and the metal L/S  $\geq 5 \mu\text{m}$ ; for fan-out (chip-last) RDL-interposer the substrate size can be as large as  $2500 \text{ mm}^2$ , the pin-count can be 5000, and the metal L/S  $\geq 2 \mu\text{m}$ ; and for the bridges, the size is very small ( $< 200 \text{ mm}^2$ ), the pin-count is little ( $< 2000$ ), and the metal L/S  $\geq 2 \mu\text{m}$ .

## 11.7 Assembly Process for Advanced Packaging

There are many assembly processes for advanced packaging. In this section the followings will be briefly mentioned.

- Wire bonding
- SMT
- Wafer Bumping
- Flip Chip on Organic Substrate
- CoC, CoW, and WoW TCB and hybrid bonding.

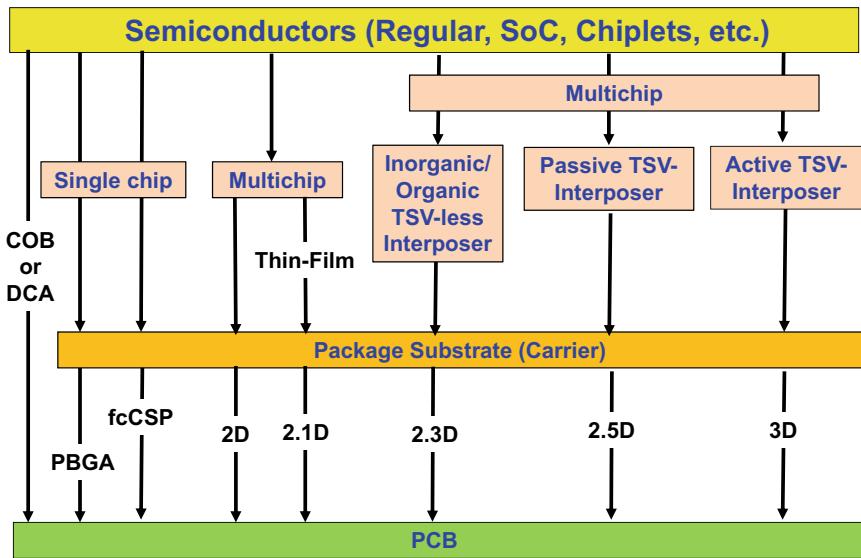


Fig. 11.6 Groups of advanced packaging

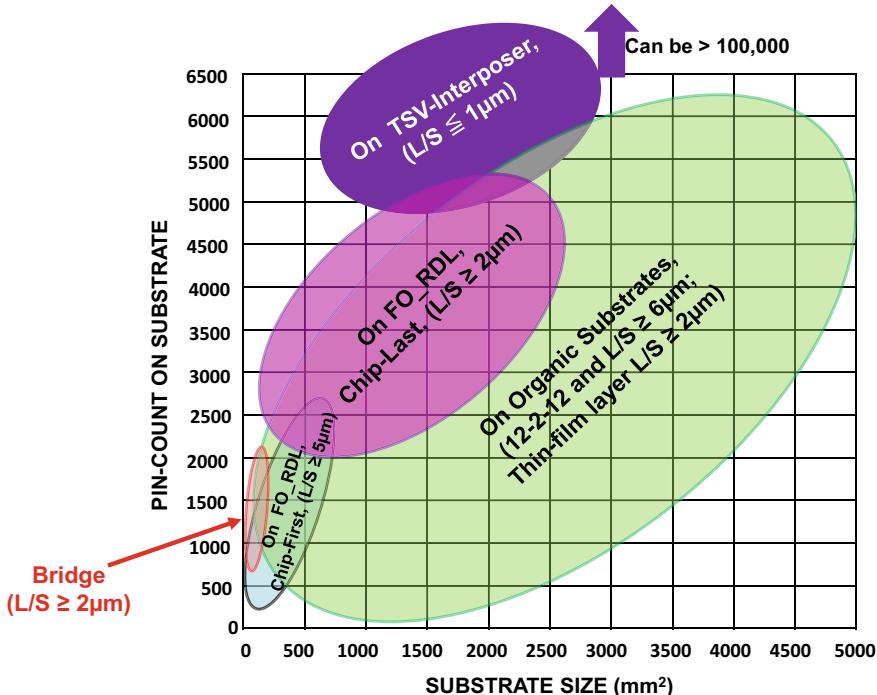
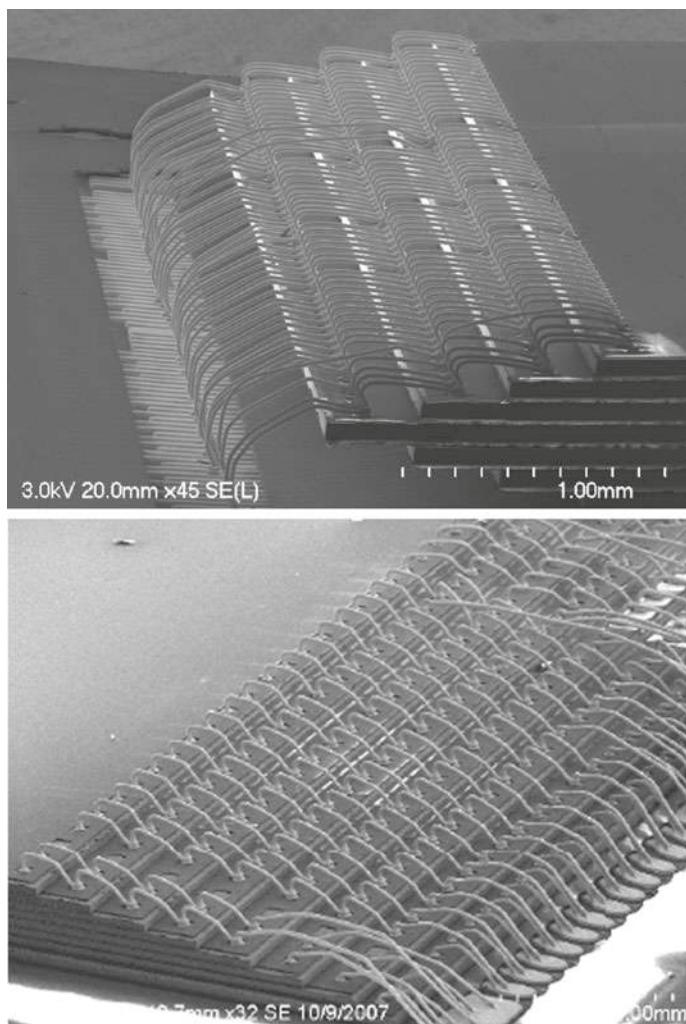


Fig. 11.7 Advanced packaging: substrates size and pin-count on substrate

### 11.7.1 Wire Bonding

Today, driven by cost, more than 50% of the wires have been shifted from gold (Au) to copper (Cu) or even some silver (Ag) materials [5–8]. In wire bonding technology all the wires are bonded along the peripherals (one to two rows) of the chip as shown in Fig. 11.8 [5]. For some niche applications, the wire bonding technology can go down to 35  $\mu\text{m}$ -pitch.

One of the major reliability challenges of Cu wires on Al (aluminum) pad has been overcoming the corrosion sensitivity of the Cu-Al system at elevated temperature in



**Fig. 11.8** Wire bonding

the presence of humidity and under bias [6, 7]. This is especially true for automotive electronic packaging. In [7], palladium coated copper (PCC) and gold-palladium (Au-Pd) coated (APC) copper wires have been developed by Fraunhofer especially to meet the requirements in automotive electronics industry for harsh environments.

Recently, Ag bonding wire has been emerging as a relatively new material for commercialized electronic products because of moderate hardness, high ductility, best thermal and electrical conductivities among metals and low growth rate of intermetallic compounds (IMCs) [8]. For Al pads,  $\text{Ag}_2\text{Al}$  and  $\text{Ag}_3\text{Al}$  have been identified as the interfacial IMCs. However, the softness, fracture toughness and corrosion resistance of  $\text{Ag}_2\text{Al}$  are much better than those of  $\text{Ag}_3\text{Al}$ . Therefore,  $\text{Ag}_3\text{Al}$  and its interfaces between adjacent phases become weak part in terms of long term reliability. In [8], UC-Irvine showed that with a new An-10In alloy, the  $\text{Ag}_3\text{Al}$  can be eliminated during the inter-diffusion and is replaced by a ternary phase. This new phase is considered to be much tougher and more corrosion resistant compared to  $\text{Ag}_3\text{Al}$ .

### 11.7.2 SMT

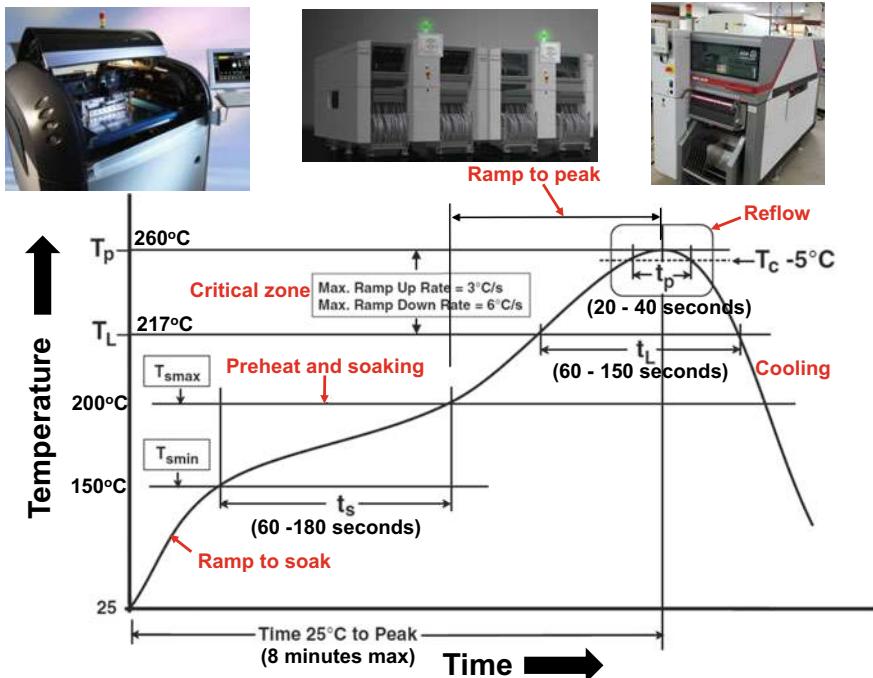
Among others, the key elements of SMT as discussed in Chap. 2 are stencil printing, chip shooter and chip pick and place (P&P), and reflow as shown in Fig. 11.9. The profit margin of SMT is very low and thus cost pressure is relatively high. In recent years, with the development of many electronic products in the direction of miniature discrete and components, high density, and ultra-fine pad pitch, they have presented severe challenges to SMT. Also; no-clean solder paste has been widely used. All these have put forward new requirements for the reflow soldering process, which requires more advanced heat transfer for reflow soldering to achieve energy saving and uniform temperature.

With Industry 4.0, the degree of automation of SMT has become higher and higher, labor costs have been greatly reduced, and personal output has been increased. The trends of SMT will be to develop high miniaturization, high performance, high reliability, high efficiency, and environmental friendly.

### 11.7.3 Wafer Bumping for Flip Chip Technology

Wafer bumping, as discussed in Chap. 2, is the mother of flip chip technology. At least, there are two different kinds of bumps, namely C4 (controlled collapse chip connection) bump and C2 (chip connection) bump and their processes are shown in Figs. 11.10a, b, respectively. Their trends will be finer pitch: the minimum pitch for C4 bumps, in the next 5 years, will be 50  $\mu\text{m}$  and that for C2 bumps will be 20  $\mu\text{m}$ .

Figure 11.10c shows Amkor's Double-POSSUM TM package [9]. It can be seen that the package is actually defined by two levels of nesting die. The three daughter

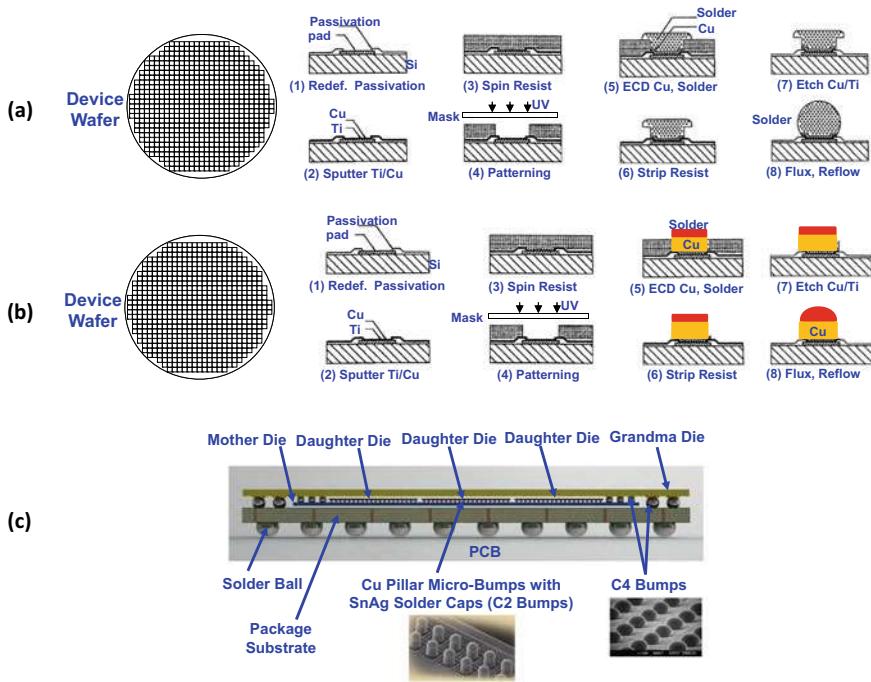


**Fig. 11.9** SMT: stencil printing, chip shooter, chip P&P, and reflow

dies are flip-chip attached to the larger mother die which is then attached to the largest grandma die. The grandma die is then flip-chip attached to the package substrate. The bumps between the daughter dies and the mother die are microbumps (Cu-pillar with solder cap). C4 bumps are used between the mother die and grandma die, and between the grandma die and package substrate.

#### 11.7.4 Flip Chip on Organic Substrates

Recent advances and trends of flip chip technology have been provided in, for example [10]. Flip chip on organic substrates have been discussed in Chap. 2 (Fig. 2.33). In the next 5 years, flip chip mass reflow of C4 bumps with CUF is still the most used (60 $\mu\text{m}$ -pitch minimum). The use of TCB with low-force and reflow of C2 bumps and then CUF will be increased (50 $\mu\text{m}$ -pitch minimum) because the use of thin chips and thin package substrates is increased. Flip chip TCB with large force of C2 bump (30 $\mu\text{m}$ -pitch minimum) and NCP/NCF is frequently used for high pin-count and density applications.



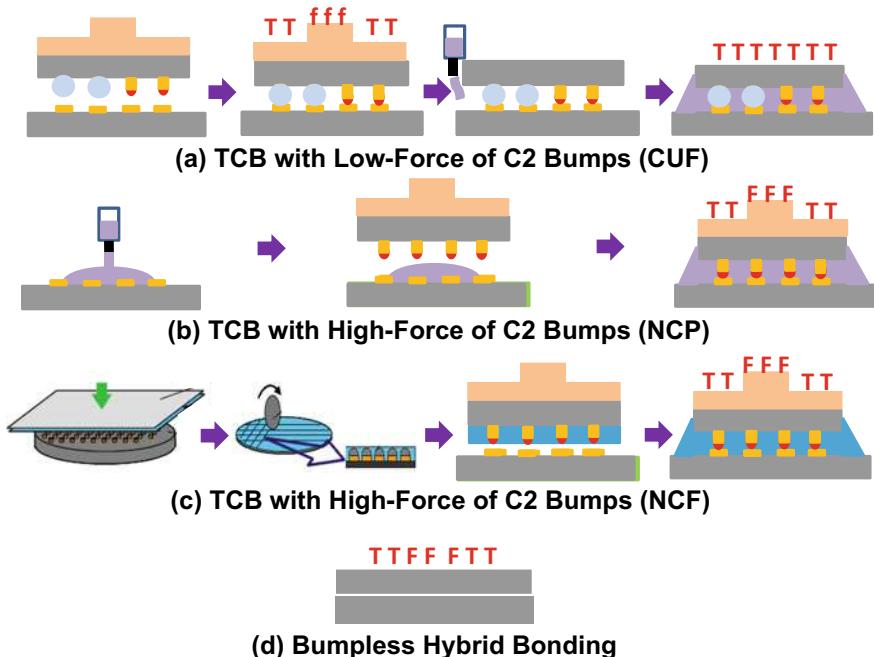
**Fig. 11.10** a and b C4 and C2 wafer bumping. c The Amkor double-POSSUM package

### 11.7.5 CoC, CoW, and WoW TCB and Hybrid Bonding

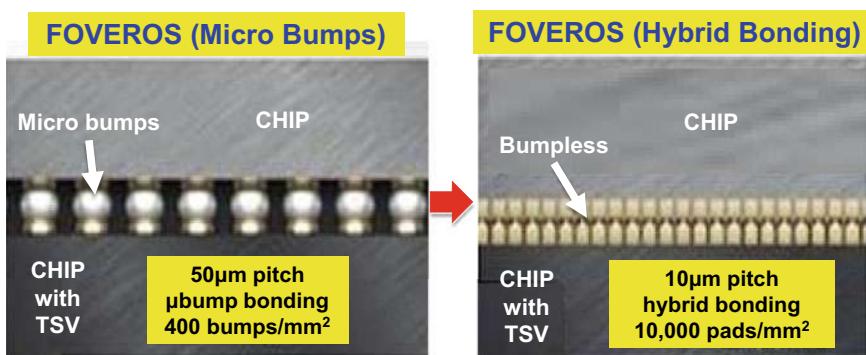
Silicon-to-silicon flip chip face-to-face or face-to-back bonding is usually performed by TCB and Cu-Cu bumpless hybrid bonding as shown in Fig. 11.11. The interconnect bump structure is either C2 bump or bumpless. TCB is with C2 bumps while hybrid bonding is bumpless as shown in Fig. 11.12 by Intel.

WoW bonding has the most throughputs. However, yield is an issue, i.e., good chip bonds on bad chip. Usually, WoW bonding applies to two wafers. A stack of 4 wafers such as the HBM (high bandwidth memory), the yield loss is prohibited, e.g., the assembly yield is 12.96% if the yield of the fresh DRAM wafer is 60%; 40.96% if the yield of the DRAM is 80%; and is 65.61% if the yield of the DRAM wafer is 90%. Also, different sizes of chips may be another issue.

Today, the MEMS (micro electro mechanical system) device wafer and the cap (or ASIC) wafer TCB with C2 bumps are in HVM by a few companies. The only HVM of WoW by bumpless hybrid bonding is Sony's processing wafer and CMOS image sensors (CIS) pixel wafer. The trend of WoW bonding in the next 5 years is WoW bumpless hybrid bonding (still two wafers), which will be used more than today.

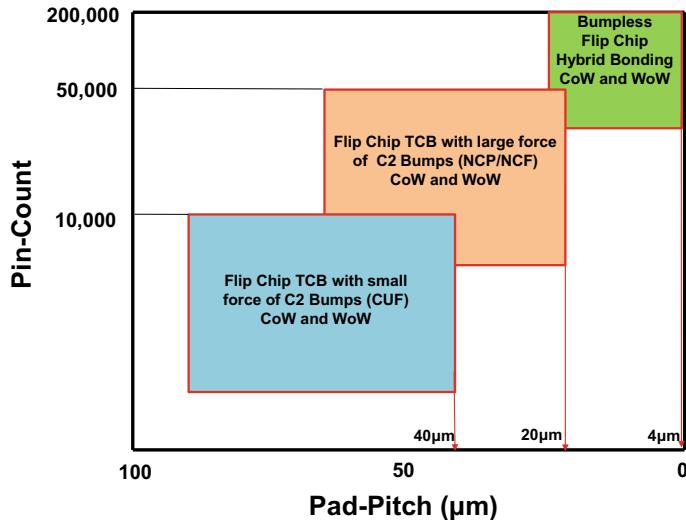


**Fig. 11.11** Flip chip (silicon-to-silicon) assembly processes: **a** TCB with low-force of C2 bumps (CUF), **b** TCB with high-force of C2 bumps (NCP), **c** TCB with high-force of C2 bumps (NCF), and **d** bumpless hybrid bonding



**Fig. 11.12** Intel's microbump bonding versus bumpless hybrid bonding

Today, CoW with C2 bump by TCB method is the most used assembly method for silicon-to-silicon flip chip face-to-face or face-to-back bonding. In the next few years, however, CoW flip chip face-to-face or face-to-back by bumpless hybrid bonding method will be increased.



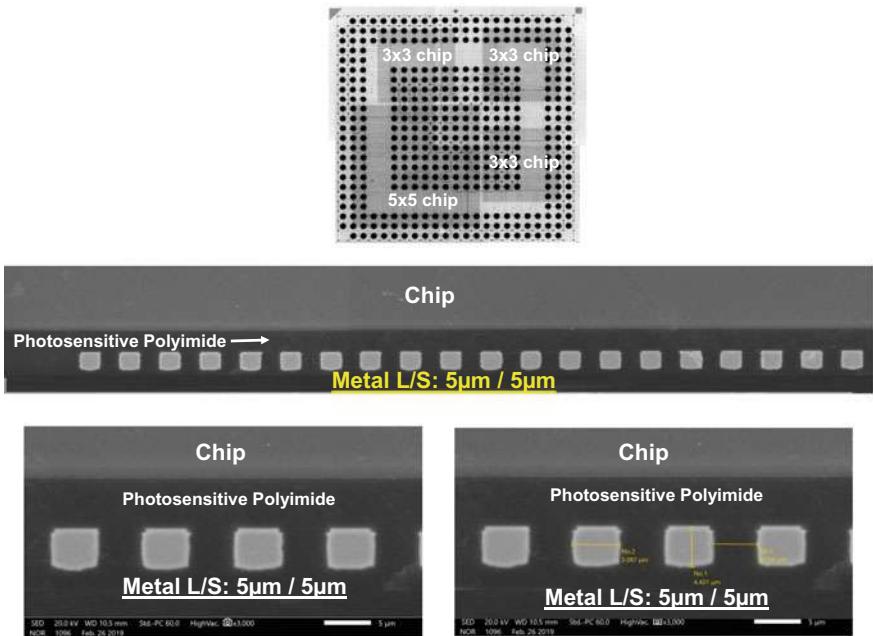
**Fig. 11.13** Flip chip (silicon-on-silicon) CoW and WoW by TCB with low-force of C2 bumps (CUF), TCB with high-force of C2 bumps (NCP/NCF), and by bumpless hybrid bonding

Because of the throughput issue, CoC bonding w/o bumps will not be popular. Figure 11.13 shows the roadmap of flip chip CoW and WoW w/o bumps bonding.

## 11.8 Fan-Out Chip-First (Face-up), Chip-First (Face-Down), and Chip-Last

There are many fan-out formations [11]. Basically, there are three: (1) fan-out with chip-first and die face-down (Fig. 11.14), (2) fan-out with chip-first and die face-up (Fig. 11.15), and (3) chip-last (Fig. 11.16). Table 11.1 shows the comparison between these three formations. It can be seen that chip-first with die face-down (Fig. 11.15) is the most simple and low cost, while chip-last or redistributed-layer (RDL)-first (Fig. 11.16) is the most complex and high cost (Chip-last requires wafer bumping, chip-to-RDL-substrate bonding, underfilling or molded underfilling, and package substrate). Chip-first with die face-up (Fig. 11.15) requires slightly more process steps (and therefore slightly more costly) than chip-first with die face-down.

Chip-first fan-out packaging can perform more than what fan-in wafer-level packaging (Chap. 3) can do. However, some of the things that the conventional plastic ball grid array (PBGA) package can do, but chip-first fan-out packaging cannot are: (1) larger die size ( $\geq 12 \text{ mm} \times 12 \text{ mm}$ ), and (2) larger package size ( $\geq 25 \text{ mm} \times 25 \text{ mm}$ ). This is due to the thermal expansion mismatch and warpage limitations of the fan-out chip-first packaging. In this case, fan-out chip-last (RDL-first) can extend



**Fig. 11.14** Fan-out chip-first with die face-down

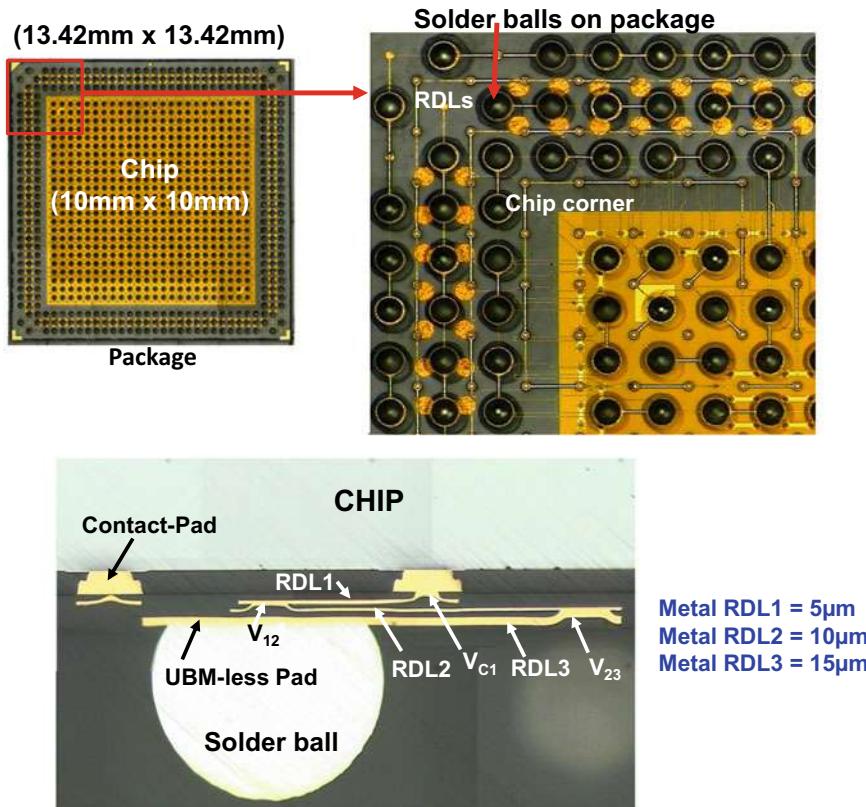
the application boundary to a die size with the range of  $\leq 20 \text{ mm} \times 20 \text{ mm}$  and a fan-out package size of  $\leq 45 \text{ mm} \times 45 \text{ mm}$ .

Fan-out chip-first is a good choice for packaging semiconductor ICs such as baseband, RF/analog, PMIC, AP, low-end ASIC, CPUs (central processing units) and GPUs (graphics processing units) for portable, mobile, and wearable products. While fan-out chip last (RDL-first) is suitable for packaging IC devices such as HBM, high-end CPUs, GPUs, ASICs, and FPGAs (field programmable grid arrays) for servers, networking, and telecommunication products.

In the next 5 years, fan-out chip-first with face-down is still and will be the most used; fan-out chip-first with face-up will be used the second; while chip-last will be used the less.

## 11.9 Bridges Versus TSV-Interposer

Figure 11.17 shows Intel's EMIB (embedded multi-die interconnect bridge) in the top layer of a build-up package substrate. EMIB is a piece of dummy silicon with fine metal L/S RDLs to allow horizontal interconnection of chips [12, 13]. Their objective is to eliminate the TSV-interposer. One of their patents is shown in Fig. 11.18a.

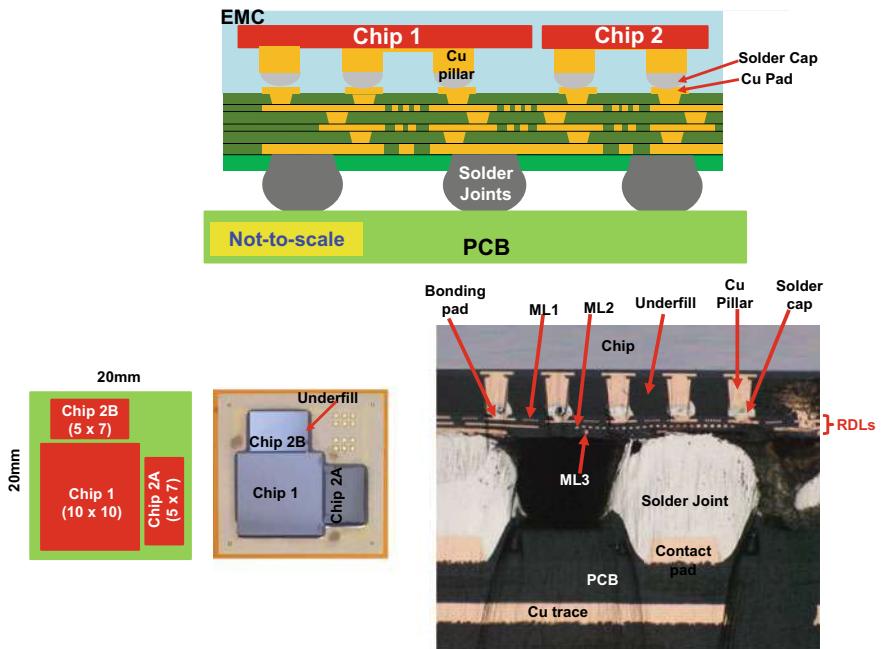


**Fig. 11.15** Fan-out chip-first with die face-up

On December 8, 2017, Applied Materials proposed to embed the bridge in an EMC (epoxy molding compound) with fan-out packaging method as shown in Fig. 11.18b [14]. It can be seen that the circuitries of the chips are fanned out with the RDLs and connected horizontally through the bridge. The vertical interconnects are through the TMV [14].

During TSMC's Annual Technology Symposium (August 25, 2020), TSMC announced their LSI (local Si interconnect) technology as shown in Fig. 11.19. It can be seen that the LSI technology is very similar to Applied Materials' except the LSI may not be just a piece of TSV-less interposer but may include TSVs or even CMOS devices.

Because of the popularity of the chiplets heterogeneous integration, the use of bridge technology to connect chips mainly in the horizontal direction such as EMIB, LSI, and Applied Materials' will be increased.

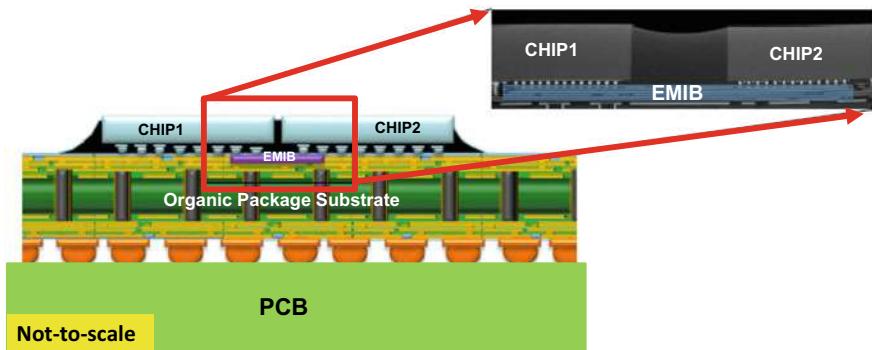


**Fig. 11.16** Fan-out chip-last or RDL-first

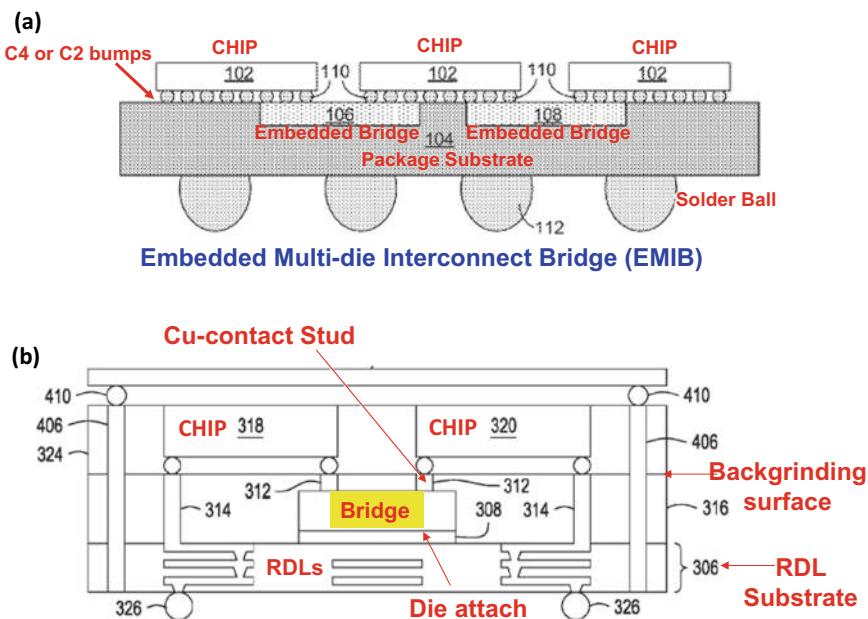
**Table 11.1** Comparison between fan-out chip-first (face-down), chip first (face-up), and chip-last (or RDL-first)

	Chip-first (face-down), e.g., eWLB	Chip-first (face-up), e.g., In_FO	Chip-last (RDL-first), e.g., SiWLP
Chip size	$\leq 5 \times 5 \text{ mm}^2$ <sup>1</sup>	$\leq 12 \times 12 \text{ mm}^2$ <sup>1</sup>	$\leq 20 \times 20 \text{ mm}$
Package size	$\leq 10 \times 10 \text{ mm}^2$ <sup>2</sup>	$\leq 25 \times 25 \text{ mm}^2$ <sup>2</sup>	$\leq 45 \times 45 \text{ mm}$
RDL (Metal L/S)	$\geq 10 \mu\text{m}$	$\geq 5 \mu\text{m}$	$\geq 2 \mu\text{m}$ or $< 1 \mu\text{m}$ <sup>3</sup>
RDL (Layers)	$\leq 3$	$\leq 4$	$\leq 6$
Wafer bumping	No	No	Yes
Chip-to-substrate bonding	No	No	Yes
Underfill or MUF	No	No	Yes
Build-up package substrate	No	No	Yes
Process steps	Simple	Slightly more	More
Cost	Low	Middle	High
Performance	Low	Middle	High
Applications	Baseband, MCU, RF/analog, PMIC, etc.	Apple's application processor chipset	Very high-performance and high-density (Not in HVM)

<sup>1</sup>Limited by die shift; <sup>2</sup>Limited by warpage; <sup>3</sup>With PECVD + Cu damascene + CMP



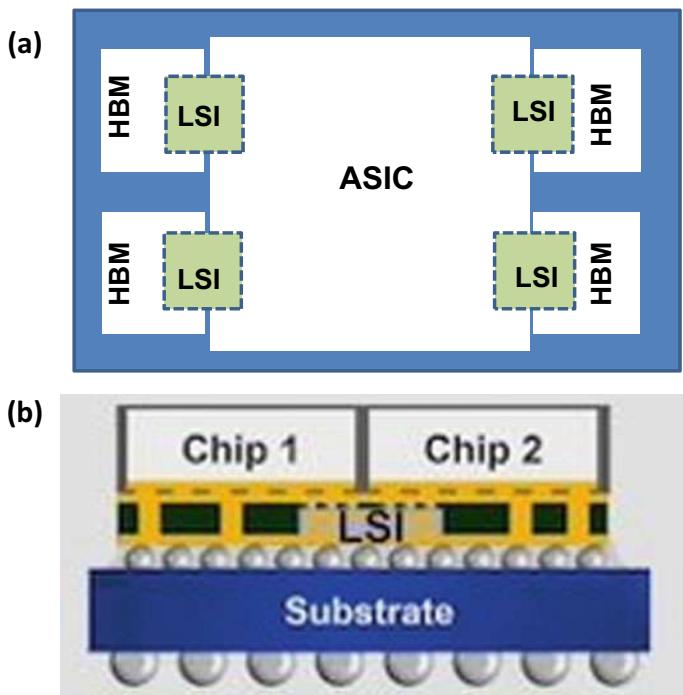
**Fig. 11.17** Intel's EMIB [13]



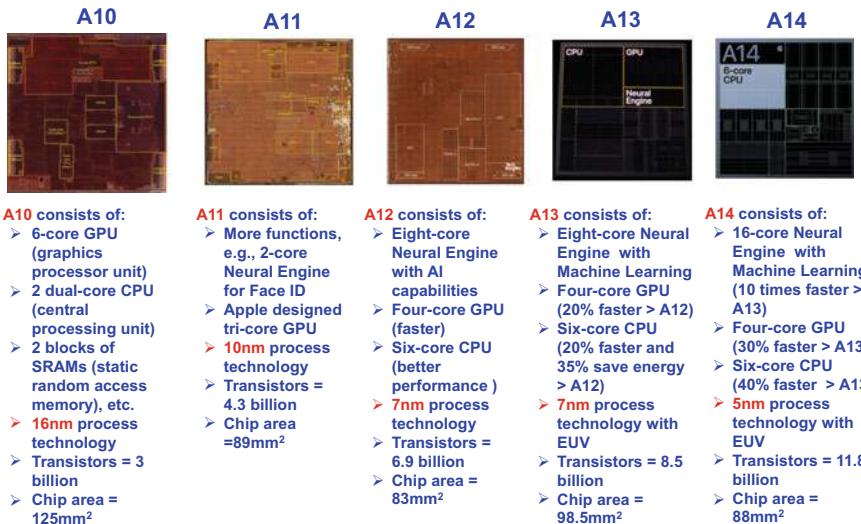
**Fig. 11.18** **a** Intel's EMIB embedded in the top of a build-up package substrate. **b** Applied Materials' bridge embedded in an epoxy molding compound

## 11.10 SoC Versus Chiplets

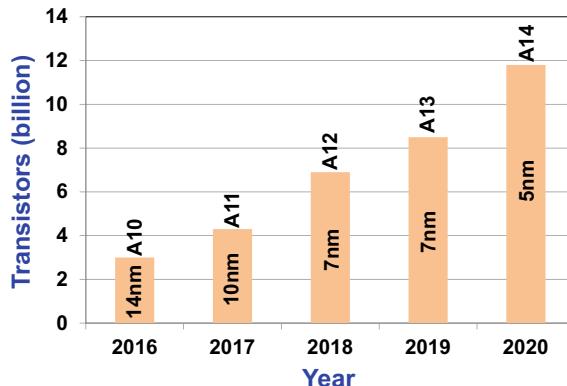
SoC integrates ICs with different functions into a single chip for a system or subsystem. Figure 11.20 shows Apple's application processor (AP) from A10 through A14. The number of transistor versus year with various feature size is shown in Fig. 11.21. It can be seen that the number of transistors and functionalities increase



**Fig. 11.19** TSMC's bridge—Local silicon interconnect (LSI)



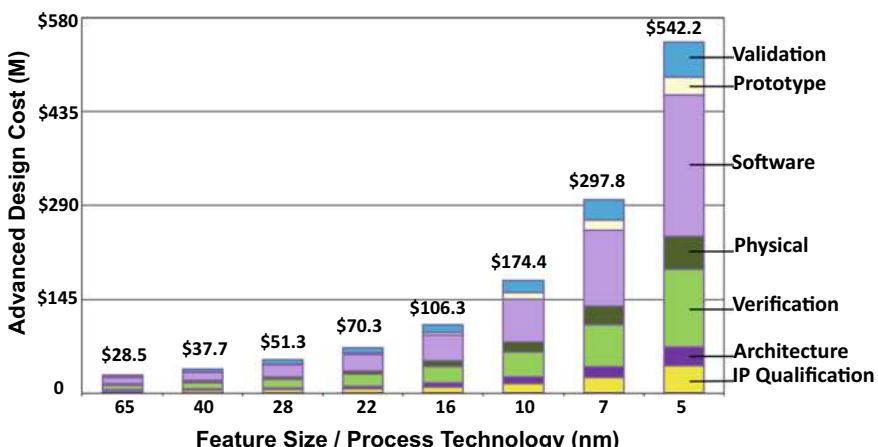
**Fig. 11.20** Apple's application processors A10 through A14



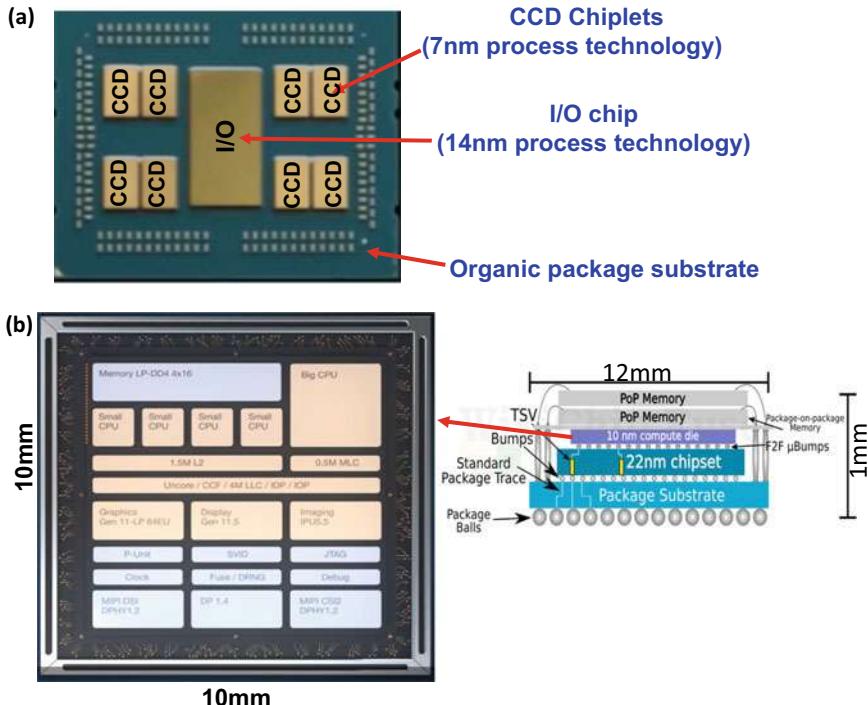
**Fig. 11.21** Apple’s application processor: transistors versus year

with a reduction of feature size. Unfortunately, according to International Business Strategies, Fig. 11.22 shows the advanced design cost versus feature size through 5 nm. It can be seen that it will take more than \$500 million to just design the 5 nm feature size. For the 5 nm process technology development it will take another \$1 billion.

Heterogeneous chiplet integration contrasts with SoC. Chiplet heterogeneous integration redesigns the SoC into smaller chiplets and then uses packaging technology to integrate dissimilar chiplets with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem [15, 16]. A chiplet is a functional integrated circuit (IC) block that is often made of reusable IP (intellectual property) blocks.



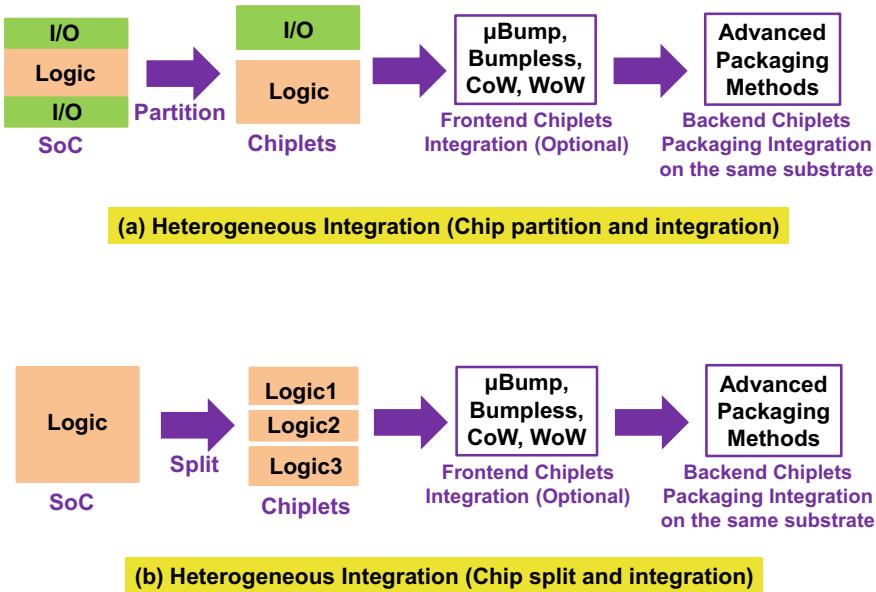
**Fig. 11.22** Advanced design cost versus feature size



**Fig. 11.23** **a** AMD EPYC processor with chiplets [17]. **b** Intel's Lakefield processor with chiplets

Figure 11.23a shows AMD EPYC processors [17–19]. It can be seen that there are 4 pairs of chiplets (fabricated with 7 nm process technology) on each side of a larger I/O chip (fabricated by a 14 nm process technology) tightly coupled on an organic build-up substrate with underfill. Figure 11.23b shows Intel mobile (notebook) processor “Lakefield”, which is based on their FOVEROS technology. The SoC is partitioned (e.g., CPU, GPU, LPDDR4, etc.) and split (e.g., the CPU is split into one big CPU and 4 smaller CPU) into chiplets. These chiplets are then face-to-face bonded (stacked) on an active TSV-interposer (a large 22FFL base chip) with a CoW method.

There are at least two different chiplet heterogeneous integrations as shown in Fig. 11.24, namely chip split and integration (driven by cost and yield) and chip partition and integration (driven by cost and technology optimization). In chip split and integration, the SoC such as logic is split into smaller chiplets such as logic1, logic2, and logic3. These chiplets can be stacked (integrated) by the frontend CoW or WoW methods [20–23] and then assembled (integrated) on the same substrate of a single package by using advanced packaging techniques. It should be emphasized that the frontend chiplets integration can yield a smaller package area and better electrical performance but is optional. In chip partition and integration, the SoC such as the logic and I/Os are partitioned into functions: logic and I/O, and then integrated



**Fig. 11.24** Chiplets by partition and split

(stacked) by frontend CoW or WoW methods. It is followed by using advanced packaging methods to assemble the logic and I/O chiplets on the same substrate of a single package. Again, the frontend integration of chiplets is optional.

The key advantages of chiplet heterogeneous integrations comparing with SoCs are yield improvement (lower cost) during manufacturing, time-to-market, and cost reduction during design. Figure 11.25 shows the plots of yield (percent of good dies) per wafer versus chip size for monolithic design and 2-, 3-, and 4-chiplet design [24].

SoCs with chip scaling are here to stay. However only a handful of companies such as Apple and Samsung can afford them at finer feature size (advanced nodes). Usually, there are some reasons for them to do so. Take Apple for example, there are at least three reasons: (a) on April 23, 2008, Apple acquired Palo Alto Semiconductor and has been building their chips with lots of IPs and coupled (integrated) with their software development, (b) breaking their SoC design up into chiplets would not be an attractive prospect because the additional chip-to-chip interconnection and communication overhead would create more headaches than it's worth, and (c) the world's number one foundry (TSMC) is Apple's loyal partner and they committed to Apple's schedule, e.g., the application processor (A16) will be manufactured with TSMC's 3 nm process technology in the second half of 2022.

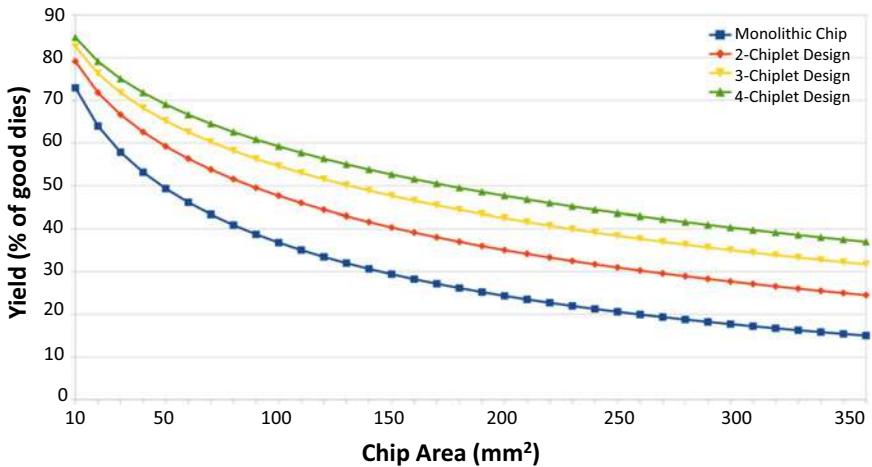


Fig. 11.25 Yield versus chip area for various chiplets and SoC

## 11.11 Material Requirement for HS/HF Applications

Driven by 5G, in order to meet the requirements for boosting signal transmission speed/rate and managing a huge data flood, advanced packaging materials are necessary. With respect to the electrical performance of insulation materials, low loss Df (dissipation factor or loss tangent) and Dk (dielectric constant or permittivity) materials are highly preferred for 5G applications [25–40] and their roadmaps are shown in Figs. 11.26 and 11.27.

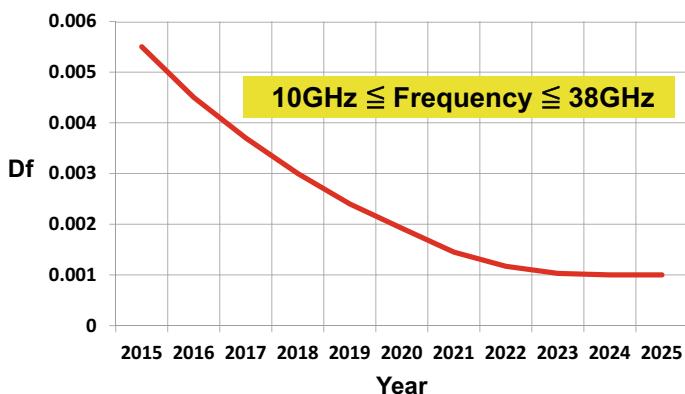


Fig. 11.26 Roadmap for dissipation factor or loss tangent (Df)

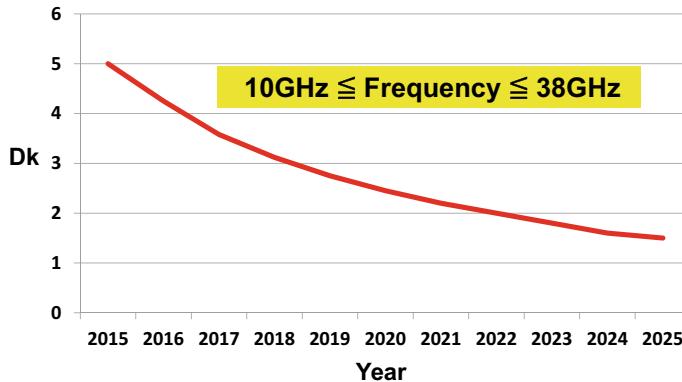


Fig. 11.27 Roadmap for dielectric constant or permittivity (Dk)

## 11.12 Summary and Recommendation

Some important results and recommendations are summarized in the follows.

- The impact of COVID-19 on the investment, growth, and adoption of the 5G, AI, IoTs, and autonomous vehicles is positive.
- The impact of COVID-19 on the semiconductor foundry, OSAT, and EMS (electronic manufacturing services) is positive.
- The key advantages of chiplet comparing with SoCs are yield improvement (lower cost) during manufacturing, time-to-market, better thermal management, and cost reduction during design. One of the disadvantages is to increase packaging cost.
- SoCs with chip scaling are here to stay. Chiplets provide alternatives (options) to SoCs, especially for advanced nodes, which most companies cannot afford.
- With Industry 4.0, the degree of automation of SMT has become higher and higher, labor costs have been greatly reduced, and personal output has been increased. The trends of SMT will be to develop high automation, high miniaturization, high performance, high reliability, high efficiency, and environmental friendly.
- More than 75% of the flip chip applications are for C4 bumps mass reflowed on organic package substrates. TCB of C2 bumps with small-force and CUF is getting traction because of the interest in using the thin chips and thin organic substrate.
- No more than 25% of the flip chip applications are for silicon-to-silicon, face-to-face or face-to-back, and very high performance and high density. Because of the yield issue, WoW bonding is limited to two wafers and CoW is the mainstream. The interconnect material/structure is mainly C2 bumps (by TCB), however bumpless (by hybrid bonding) is getting traction.

## References

1. <https://advisory.kpmg.us/articles/2020/impact-of-covid-19-on-semiconductor-industry.html>.
2. <https://www.statista.com/statistics/867210/worldwide-semiconductor-foundries-by-revenue/>.
3. <https://www.counterpointresearch.com/foundry-industry-revenue-growth-continue-2021/>.
4. <https://www.globenewswire.com/news-release/2021/02/02/2167973/0/en/OSAT-Market-was-valued-at-USD-31-64-billion-in-2020-and-is-expected-to-reach-USD-49-71-billion-at-a-CAGR-of-7-3-over-the-forecast-period-2021-2026.html>.
5. Qin, I., O. Yauw, G. Schulze, A. Shah, B. Chylak, and N. Wong, "Advances in Wire Bonding Technology for 3D Die Stacking and Fan Out Wafer Level Package", *IEEE/ECTC Proceedings*, May 2017, pp. 1309–1315.
6. Qin, W., T. Anderson, D. Barrientos, H. Anderson, and G. Chang, "Corrosion Mechanisms of Cu Wire Bonding on Al Pads", *IEEE/ECTC Proceedings*, May 2018, pp. 1446–1454.
7. Klengel, S., R. Klengel, J. Schischka, T. Stephan, M. Petzold, M. Eto, N. Araki, and T. Yamada, "A new reliable, corrosion resistant gold-palladium coated copper wire material", *IEEE/ECTC Proceedings*, May 2019, pp. 175–182.
8. Wu, J., and C. Lee, "Eliminating harmful intermetallic compound phase in silver wire bonding by alloying silver with indium", *IEEE/ECTC Proceedings*, May 2018, pp. 2224–2230.
9. Sutanto, J., "POSSUM Die Design as a Low Cost 3D Packaging Alternative," *3D Packaging*, 2012, pp. 16–18.
10. Lau, J. H., "Recent Advances and New Trends in Flip Chip Technology", *ASME Transactions, Journal of Electronic Packaging*, September 2016, Vol. 138, Issue 3, pp. 1–23.
11. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1–27.
12. Chiu, C., Z. Qian, and M. Manusharow, "Bridge interconnect with air gap in package assembly," *US Patent No. 8,872,349*, 2014.
13. Mahajan, R., R. Sankman, N. Patel, D. Kim, K. Aygun, Z. Qian, et al., "Embedded multi-die interconnect bridge (EMIB) – a high-density, high-bandwidth packaging interconnect," *IEEE/ECTC Proceedings*, May 2016, pp. 557–565.
14. Hsiung, C., and a. Sundarrajan, "Methods and Apparatus for Wafer-Level Die Bridge", US 10,651,126 B2, Filed on December 8, 2017, Granted on May 12, 2020.
15. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.
16. Lau, J. H., "Recent Advances and Trends in Heterogeneous Integrations", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 16, April 2019, pp. 45–77.
17. Naffziger, S., K. Lepak, M. Paraschour, and M. Subramony, "AMD Chiplet Architecture for High-Performance Server and Desktop Products", *IEEE/ISSCC Proceedings*, February 2020, pp. 44–45.
18. Naffziger, S., "Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs", *Symposia on VLSI Technology and Circuits*, June 2020, pp. 1–39.
19. Stow, D., Y. Xie, T. Siddiqua, and G. Loh, "Cost-Effective Design of Scalable High-Performance Systems Using Active and Passive Interposers", *IEEE/ICCAD Proceedings*, November 2017, pp. 1–8.
20. Chen, M. F., C. S. Lin, E. B. Liao, W. C. Chiou, C. C. Kuo, C. C. Hu, C. H. Tsai, C. T. Wang and D. Yu, "SoIC for Low-Temperature, Multi-Layer 3D Memory Integration", *IEEE/ECTC Proceedings*, May 2020, pp. 855–860.
21. Chen, Y. H., C. A. Yang, C. C. Kuo, M. F. Chen, C. H. Tung, W. C. Chiou, and D. Yu, "Ultra High Density SoIC with Sub-micron Bond Pitch", *IEEE/ECTC Proceedings*, May 2020, pp. 576–581.
22. Chen, F., M. Chen, W. Chiou, D. Yu, "System on Integrated Chips (SoIC<sup>TM</sup>) for 3D Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2019, pp. 594–599.
23. Lin, J., C. Chung, C. Lin, A. Liao, Y. Lu, J. Chen, and D. Ng, "Scalable Chiplet package using Fan-Out Embedded Bridge", *IEEE/ECTC Proceedings*, May 2020, pp. 14–18.
24. <https://en.wikichip.org/wiki/chiplet>, March 27, 2020.

25. Sato, J., S. Teraki, M. Yoshida, and H. Kondo, "High Performance Insulating Adhesive Film for High-Frequency Applications", *Proceedings of IEEE/ECTC*, May 2017, pp. 1322–1327.
26. Tasaki, T., "Low Transmission Loss Flexible Substrates using Low Dk/Df Polyimide Adhesives", *TechConnect Briefs*, V4, May 2018, pp. 75–78.
27. Hayes, C., K. Wang, R. Bell, C. Calabrese, J. Kong, J. Paik, L. Wei, K. Thompson, M. Gallagher, and R. Barr, "Low Loss Photodielectric Materials for 5G HS/HF Applications", *Proceeding of International Symposium on Microelectronics*, October 2019, pp. 1–5.
28. Hayes, C., K. Wang, R. Bell, C. Calabrese, M. Gallagher, K. Thompson, and R. Barr, "High Aspect Ratio, High Resolution, and Broad Process Window Description of a Low Loss Photodielectric for 5G HS/HF Applications Using High and Low Numerical Aperture Photolithography Tools", *Proceedings of IEEE/ECTC*, May 2020, pp. 623–628.
29. Matsukawa, D., N. Nagami, K. Mizuno, N. Saito, T. Enomoto, and T. Motobe, "Development of Low Dk and Df Polyimides for 5G Application", *Proceeding of International Symposium on Microelectronics*, October 2019, pp. 1–4.
30. Ito, H., K. Kanno, A. Watanabe, R. Tsuyuki, R. Tatara, M. Raj, and R. Tummala, "Advanced Low-Loss and High-Density Photosensitive Dielectric Material for RF/Millimeter-Wave Applications" *Proceedings of International Wafer Level Packaging Conference*, October 2019, pp. 1–6.
31. Nishimura, I., S. Fujitomi, Y. Yamashita, N. Kawashima, and N. Miyaki, "Development of new dielectric material to reduce transmission loss", *Proceedings of IEEE/ECTC*, May 2020, pp. 641–646.
32. Araki, H., Y. Kiuchi, A. Shimada, H. Ogasawara, M. Jukei, and M. Tomikawa, "Low Df Polyimide with Photosensitivity for High Frequency Applications", *Journal of Photopolymer Science and Technology*, V33, 2020, pp. 165–170.
33. Araki, H., Y. Kiuchi, A. Shimada, H. Ogasawara, M. Jukei, and M. Tomikawa, "Low Permittivity and Dielectric Loss Polyimide with Patternability for High Frequency Applications", *Proceedings of IEEE/ECTC*, May 2020, pp. 635–640.
34. Tomikawa, M., H. Araki, M. Jukei, H. Ogasawara, and A. Shimada, "Low Temperature Curable Low Df Photosensitive Polyimide", *Proceeding of International Symposium on Microelectronics*, October 2019, pp. 1–5.
35. Tomikawa, M., H. Araki, M. Jukei, H. Ogasawara, and A. Shimada, "Hsigh Frequency Dielectric Properties of Low Dk, Df Polyimides", *Proceeding of International Symposium on Microelectronics*, October 2020, pp. 1–5.
36. Takahashi, K., S. Kikuchi, A. Matsui, M. Abe and K. Chouraku, "Complex Permittivity Measurements in a Wide Temperature Range for Printed Circuit Board Material Used in Millimeter Wave Band", *Proceedings of IEEE/ECTC*, May 2020, pp. 938–945.
37. Han, K., Y. Akatsuka, J. Cordero, S. Inagaki, and D. Nawrocki, "Novel Low Temperature Curable Photo-Patternable Low Dk/Df for Wafer Level Packaging (WLP)", *Proceedings of IEEE/ECTC*, May 2020, pp. 83–88.
38. Yamamoto, K., S. Koga, S. Seino, K. Higashita, K. Hasebe, E. Shiga, T. Kida, and S. Yoshida, "Low Loss BT resin for substrates in 5G communication module", *Proceedings of IEEE/ECTC*, May 2020, pp. 1795–1800.
39. Kakutani, T., D. Okamoto, Z. Guan, Y. Suzuki, M. Ali, A. Watanabe, M. Kathaperumal, and M. Swaminathan, "Advanced Low Loss Dielectric Material Reliability and Filter Characteristics at High Frequency for mmWave Applications", *Proceedings of IEEE/ECTC*, May 2020, pp. 1795–1800.
40. Guo, J., H. Wang, C. Zhang, Q. Zhang, and H. Yang, "MPPE/SEBS Composites with Low Dielectric Loss for High-Frequency Copper Clad Laminates Applications", *Polymers*, V12, August 2020, pp. 1875–1887.

# Index

## Symbols

- 2D chiplet heterogeneous integration on organic substrate, 418
- 2D fan-out (chip-first) IC integration, 239, 242, 469
- 2D flip chip IC integration, 4, 7, 18, 239, 469
- 2.1D chiplet heterogeneous integration on organic substrate, 419
- 2.1D fan-out IC integration with bridges, 4, 11, 19, 239
- 2.1D flip chip IC integration, 4, 9, 19, 239, 469
- 2.1D flip chip IC integration with bridges, 4, 11, 19
- 2.1D IC integration, 4, 239, 240, 249, 294
- 2.3D chiplet heterogeneous integration on organic substrate, 420
- 2.3D fan-out (chip-first) IC integration, 4, 9, 12, 19, 239, 469
- 2.3D fan-out (chip-last) IC integration, 4, 13, 19, 239, 469
- 2.3D flip chip IC integration, 4, 12, 19, 239
- 2.3D IC integration, 4, 239, 257, 294, 469
- 2.5D (C2 bump) IC integration, 4, 14, 19, 469
- 2.5D (C4 bump) IC integration, 4, 13, 19, 469
- 2.5D chiplet heterogeneous integration on silicon substrate (passive TSV-interposer), 421
- 2.5D IC integration, 4, 299, 313, 336
- 3D chiplet heterogeneous integration on silicon substrate (active TSV-interposer), 420
- 3DFabric technology, 368, 431
- 3D IC integration, 4, 343, 362, 372

- 3D IC packaging, 343, 346, 356, 360, 371
- 3D-MCM, 29
- 5G, 362, 441, 462, 465, 468, 486, 487
- 5G mmWave, 2, 30, 441
- 5-side molded W/PLCSP, 78
- 6-side molded W/PLCSP, 78, 115, 120, 138

## A

- Accumulated creep strain, 112, 136, 138
- Accumulated equivalent creep strain, 137
- Active TSV-interposer, 4, 299, 366, 423, 428
- Adhesion strength, 444, 446
- Advanced Driver-Assistance Systems (ADAS), 78, 115
- Advanced Interface Bus (AIB), 367
- AirPods Pro, 30
- Ajinomoto Build-up Film (ABF), 89, 93, 114, 122, 169
- Aliphatic, 445
- Ambient temperature, 309
- Annealing temperature, 381
- Antenna, 2
- Antenna-in-Package (AiP), 30
- Apple watch, 29
- Application Processor (AP), 7, 55, 243, 346, 356, 357, 414
- Application Specific Integrated Circuits (ASICs), 54, 262, 299, 311
- Aromatic, 445
- Arrayed Waveguide Gratings (AWG), 332
- Artificial Intelligence (AI), 1, 18, 362, 465, 466, 487
- Arylalkyl thermoset polymer, 446
- Atomic Force Microscopy (AFM), 406
- Audio transcoders, 30

Automated Optical Inspection (AOI), 39, 40, 44  
 Automotive, 2, 77, 115  
 Autonomous, 441, 465, 487

**B**

Back End Of Line (BEOL), 381  
 Backside chipping, 77, 115  
 Backside Illuminated CMOS Image Sensor (BI-CIS), 345, 392, 407  
 Back-to-back, 343, 346  
 Ball-pitch, 35  
 Bare chips, 29  
 Baseband modem, 243  
 Beamforming circuits, 30  
 Benzocyclobutene (BCB), 79  
 Big data, 441  
 Bismaleimide Triazine (BT), 316, 456  
 Bond Head (BH), 57  
 Boundary-value problem, 82  
 Bridges, 11, 256, 423, 478  
 Broadband, 1  
 Build-up package substrate, 7, 9, 11, 12, 251, 256, 336, 343, 425  
 Bulk solders, 108, 137, 160  
 Bumpless, 17, 368, 371, 399, 407, 430, 475  
 Bump-On-Lead (BOL), 57  
 Bump-On-Pad (BOP), 57  
 Buried Oxide (BOX), 385

**C**

Cameras, 30  
 Capacitors, 35  
 Capillary Underfill (CUF), 51, 55, 474  
 Carbon dioxide (CO<sub>2</sub>) laser, 95, 114  
 Cavities, 89, 92  
 Cellular, 1  
 Central Processing Unit (CPU), 2, 27, 29, 315, 326, 336, 366, 369, 414  
 Ceramic, 29  
 Characteristic life, 105, 129, 201  
 Chemical-Mechanical Polishing (CMP), 242, 318, 381, 389, 404, 406, 407  
 Chip connection (C2) bump, 7, 49, 50, 55, 56  
 Chip-first (face-down), 115, 147, 150  
 Chip-first (face-up), 477  
 Chip-last (or RDL-first), 245, 259, 268, 359, 425  
 Chiplets, 17, 343, 413, 416–421, 423–425, 427, 429, 431, 435, 484, 487  
 Chip-On-Board (COB), 4, 75

Chip-on-Chip (CoC), 4, 58, 365, 371, 399, 465, 470, 475  
 Chip-on-Substrate (CoS), 57  
 Chip-on-Wafer (CoW), 4, 17, 19, 180, 330, 371, 399, 407, 416, 429, 465, 470, 475  
 Chip-on-Wafer-on-Substrate (CoWoS), 320, 326, 329, 330, 336, 399, 421, 426, 433  
 Chip-Package-Interaction (CPI), 399  
 Chip partition and integration, 416  
 Chip shooter, 40  
 Chip split and integration, 416  
 Chlorofluorocarbons, 36  
 Cloud computing, 1, 18, 441  
 C-mode Scanning Acoustic Microscopy (C-SAM), 157, 163  
 CMOS Image Sensor (CIS), 379, 390  
 Coefficient of Thermal Expansion (CTE), 135, 154, 165  
 Collective bonding, 365  
 Common Heterogeneous integration and Intellectual Property reuse Strategies (CHIPS), 366, 414  
 Complementary Metal Oxide Semiconductor (CMOS), 299, 365, 421, 423  
 Compound Annual Growth Rate (CAGR), 468  
 Compound Semiconductor Materials On Silicon (COSMOS), 413  
 Compression molding, 148  
 Concave shape, 111, 136  
 Conductor, 32  
 Conductor loss, 442  
 Conductor skin resistance, 442  
 Confidence level, 105, 129  
 Consumer products, 27, 29  
 Controlled collapse chip connection (C4) bump, 7, 45, 48, 50, 54, 266, 280, 325, 347, 356  
 Convex shape, 111, 136  
 Copper-low-k pads, 307  
 Copper pillar, 325  
 Copper pillar with solder cap, 49  
 Copper pumping, 300  
 Coreless organic interposer, 260, 262, 263, 273, 294  
 Coreless substrate, 257, 294, 420  
 Corrosion sensitivity, 472  
 COVID-19, 465, 466, 468, 487  
 Creep analysis, 82  
 Creep shear strain, 88  
 Creep strain energy density, 112

Critical energy release rate, 380  
Critical interfacial adhesion energy, 380  
Cu–Cu bonding, 379  
Cu–Cu thermocompression bonding (TCB), 379  
Cycle-to-failure, 102, 129  
Cycloaliphatic, 445

**D**

Daisy chains, 90, 102  
Data Acquisition System (DAS), 100, 197  
Data center, 2  
Deep Reactive Ion Etching (DRIE), 303, 318  
Deep Trench Capacitor (DTC), 330  
Deep Ultraviolet (DUV), 468  
Defense Advanced Research Projects Agency (DARPA), 366, 413, 435  
Deflection, 84  
Deformed shape, 111, 135  
Desmear, 89, 93, 168  
Dielectric constant or permittivity ( $\epsilon_0$ ), 441, 452, 486  
Dielectric layer, 77, 79, 115, 150, 184  
Dielectric loss, 442  
Dielectric materials, 441  
Dielectric-to-dielectric, 387  
Die shift, 148  
Direct Bond Interconnect (DBI), 379, 387, 407  
Direct Chip Attach (DCA), 4, 75  
Dishing gap, 388  
Dispensing, 51  
Dissipation factor or loss tangent ( $D_f$ ), 442, 452, 486  
Distance to Neutral Point (DNP), 110, 136  
Diverse Accessible Heterogeneous Integration (DAHI), 413  
Double Data Rate type-2 (DDR2), 344  
Double-POSSUM, 347  
Double-sides PCB, 33  
Drop spectrum, 100, 160  
Dry-film EMC, 148, 153, 163, 164  
Dry film lamination, 89  
Dual-damascene, 249  
Dwell-at-cold, 111, 135  
Dwell-at-hot, 111, 135  
Dynamic Random-Access Memory (DRAM), 7, 56, 262, 313, 364, 368, 427

**E**

ECM-panel, 166

Edge computing, 1, 18, 441  
Effective creep strain, 84  
Effective stress, 84  
Electrical resistivity, 50  
Electrochemical Deposition (ECD), 154, 186, 246  
Electroless copper, 89  
Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG), 93, 114  
Electronic Design Automation (EDA), 435  
Electronic Manufacturing Services (EMS), 487  
Embedded fluidic microchannels, 311  
Embedded Multi-Die Interconnect Bridge (EMIB), 11, 255, 294, 423, 478  
Embedded Stiffness (e-STF), 255  
Embedded Trace Substrate (ETS), 346, 356  
Embedded Wafer-Level Ball grid array (eWLB), 115, 147  
Encapsulant, 53  
Encapsulated WLCSP (eWLCSP), 115  
Environmental friendly, 45, 487  
Epoxy Molding Compound (EMC), 5, 11, 54, 116, 122, 123, 138, 148, 177, 239  
EPYZ, 413, 418, 427  
eXtended-Cube (X-Cube), 366  
Extreme Ultraviolet (EUV), 466  
Exynos, 27

**F**

Fabless design houses, 29  
Face-to-back, 352, 369, 381  
Face-to-face, 343–346, 355, 368, 381, 400, 429  
Failure analysis, 89  
Failure criterion, 102, 129, 199  
Failure location, 108, 114, 131, 136, 138, 204  
Failure mode, 108, 114, 131, 136, 138, 204  
Failure order number, 102  
Failure rank, 105  
Fan-in Panel-Level Chip-Scale Packages (PLCSP), 78, 89, 109, 114, 120, 135, 138, 147  
Fan-in Wafer-Level Chip-Scale Packages (WLCSP), 78, 114, 147  
Fan-in Wafer/Panel-Level Chip-Scale Packages (W/PLCSP), 75, 114, 147  
Fan-Out (chip-first and face-down) Panel-Level Packaging (FOPLP), 4, 7, 12, 147, 163, 175, 477  
Fan-Out (chip-first and face-down) Wafer-Level Packaging (FOWLP), 4, 7, 12, 147, 163, 173, 174, 477

Fan-out (chip-last or RDL-first) panel-level packaging, 182, 477  
 Fan-out (chip-last or RDL-first) wafer-level packaging, 176, 477  
 Fan-out flip chip, 263  
 Fan-Out wafer-level Chip-on-Substrate (FOCoS), 266, 271  
 Fan-Out Wafer/Panel-Level Packaging (FOW/PLP), 147  
 Fast Atom Beam (FAB), 404  
 Feature size, 27, 414  
 Feed Through Interposer (FTI), 176  
 Field Programmable Gate Array (FPGA), 2, 322, 347, 420, 423, 466  
 Finite element method, 82  
 Flame Retardant (FR)-4, 32, 98  
 Flexible Copper Clad Laminate (FCCL), 446  
 Flexible Printed Circuit board (FPC), 449  
 Flexible substrate, 355  
 Flip chip, 4, 19, 27, 45, 75, 402, 474  
 Flip chip-Chip Scale Package (fcCSP), 4  
 Flowability, 53  
 Flux, 35, 49, 50, 54, 80, 156  
 Focused Ion Beam Scanning Electron Microscopy (FIB-SEM), 406  
 Foundries, 29, 299, 362, 371  
 FOVEROS, 366, 368, 406, 423, 484  
 Frequency, 442  
 Fused silica, 51

**G**

Gaming systems, 29  
 Garofalo-Arrhenius constitutive equation, 83, 135  
 Glass interposer, 334  
 Glass-reinforced epoxy, 32  
 Glass transition temperature, 446  
 Global Semiconductor Alliance (GSA), 465  
 Gold-palladium (Au-Pd) coated (APC) copper wires, 473  
 Graphics Double Data Rate 5 (GDDR5), 362  
 Graphics Processing Unit (GPU), 2, 14, 27, 29, 326, 336, 366, 414, 466

**H**

Hardwares, 2  
 Heat resistance, 449  
 Heat sink, 308  
 Heat spreader, 308, 309  
 Heterogeneous integration, 4, 7, 29, 148, 163, 243  
 High-band spectrum, 2

High Bandwidth Memory (HBM), 263, 325, 326, 336, 362, 368, 420  
 High frequency, 441  
 High-Performance Computing (HPC), 1, 18, 179, 336, 362, 399, 441, 466  
 High speed, 441  
 High Volume Manufacturing (HVM), 12, 29, 294, 299, 407  
 Human intelligence, 2  
 Hybrid bonding, 4, 17, 368, 379, 391, 399, 400, 402, 404, 406, 407, 430, 465, 475  
 Hybrid Bond Terminal (HBT), 402  
 Hybrid interface, 404  
 Hybrid RDLs, 242, 248  
 Hybrid Wafer Bonding (HWB), 403  
 Hybrid wafer bonding interface, 403

**I**

Industry 4.0, 487  
 Infrastructure, 2  
 Inorganic RDLs, 242  
 Insertion loss, 399  
 Instant data, 1, 18, 441  
 Insulating film, 442  
 Integrated Fan-Out (InFO), 357, 368, 399, 424, 433  
 Integrated Fan-Out on Substrate (InFO\_oS), 266  
 Integrated Fan-Out with Memory on Substrate (InFO\_MS), 268  
 Integrated Passive Devices (IPDs), 313, 357  
 Integrated Thin film High density Organic Package (i-THOP), 251, 419  
 Interfacial delamination, 380  
 Interlayer adhesive, 442  
 Interlayer delamination, 442  
 Intermetallic Compound (IMC), 60, 473  
 Internet of Things (IoTs), 1, 18, 29, 441, 465, 487  
 Interstrata Vias (ISVs), 387  
 iPhone, 30, 52, 356, 466  
 Isothermal fatigue, 137

**K**

Kinematic boundary condition, 109, 133  
 Kinetic boundary condition, 111, 135  
 Known Good Dies (KGDs), 116, 147, 148, 175

**L**

- Lakefield processor, 367, 413, 429  
Laser Direct Imaging (LDI), 89, 93, 114, 171  
Laser drilling, 89  
Laser grooving, 122  
Laser Induced Deep Etching (LIDE), 334  
Lateral communication, 251  
Lead-frame, 4, 148  
Lead-free reflow profile, 40  
Lead-free solder alloys, 82  
Leakage current, 330  
 $\text{Li}_2\text{TiO}_3$ -Copper Clad Laminate (LT-CCL), 460  
Light-Emitting Diodes (LEDs), 311  
Light-To-Heat-Conversion (LTHC) layer, 154, 163  
Linear acceleration factor, 206  
Liquid Phase Contact (LPC), 59  
Liquidus time, 61  
Local Si Interconnect (LSI), 257, 294, 479  
Logic, 29  
Logic-on-memory, 369

**M**

- Management Data Input/Output (MDIO), 367  
Mask aligner, 79  
MCM on Laminated substrate (MCM-L), 29  
Mean life, 131, 138  
Median rank, 102, 201  
Memory, 2, 27, 29, 54, 343  
Memory-on-logic, 369  
Metal layer, 90, 182, 184  
Metal oxide, 393  
Metal-to-metal, 388  
Microbump, 9, 12, 14, 15, 251, 266, 320, 322, 367, 371  
Micro-Electro-Mechanical System (MEMS), 299, 347, 475  
Microprocessor, 413  
Microstrip lines, 33  
Micro vias, 89  
Mid-band spectrum, 2  
Miniaturization, 45  
Mobile, 18, 441  
Modified Poly Phenylene Ether (MPPE), 460  
Moisture absorption, 442  
Molded Core embedded Package (MCeP), 356  
Molded Underfill (MUF), 53, 54, 177  
Molded WLCSP (mWLCSP), 115, 117, 118

**Molecular mobility, 452**

- Molecular structure, 457  
Monolithic, 417  
Moore's law, 27, 414  
M-Series, 175  
Multichip, 4  
Multichip Module (MCM), 29  
Multilayers PCB, 33

**N**

- NAND, 7  
Networks, 1  
No-clean fluxes, 36  
Non-Conductive Film (NCF), 56, 273, 364  
Non-Conductive Paste (NCP), 55  
Non-destructive fault isolation, 331  
Non-TSV Interposer (NTI), 268  
Notebooks, 1, 27, 29, 76, 441  
Number of failures, 133

**O**

- Omni-Directional Interconnect (ODI), 367  
Optical channels, 332  
Optical Printed Circuit Board (OPCB), 332  
Optical TSV, 332  
Organic interposer, 253, 254  
Organic RDLs, 242  
Organic Solderability Preservative (OSP), 99, 124, 158  
Organic substrate, 29, 35, 51, 251, 418–420, 474  
Original Equipment Manufacturers (OEMs), 468  
Outsourced Semiconductor Assembly and Tests (OSAT), 75, 360, 371, 468, 487  
Oxidation, 389

**P**

- Package-on-Package (PoP), 4, 7, 18, 52, 343, 356, 357, 424, 469  
Package substrate, 7, 75, 148  
Pad pitch, 39  
Palladium Coated Copper (PCC), 473  
Panel-Level Chip-Scale Package (PLCSP), 78  
Passivation, 150  
Passivation opening, 48, 89  
Passive TSV-interposer, 4, 14, 299, 300, 305, 336, 421  
PCB-Copper Clad Laminate (P-CCL), 460  
Peel strength, 169

Peripheral pads, 78, 89, 344  
 Photodiode (PD), 332  
 Photoimageable Dielectric (PID), 185  
 Photonics interposer, 332  
 Photo-patterning, 446  
 Photoresist, 79, 154  
 Photosensitive polyimide, 80, 154, 447  
 Physical Failure Analysis (PFA), 331  
 Physical vapor deposition, 154, 180  
 Pick and Place (P&P), 40, 44, 89  
 Pixel chip, 390  
 Planarization, 383  
 Plasma activation, 384  
 Plasma Enhance Chemical Vapor Deposition (PECVD), 242  
 Plasma etching, 48, 123  
 Plastic Ball Grid Array (PBGA), 4, 35, 37, 40, 42  
 Plastic Leaded Chip Carrier (PLCC), 35  
 Plastic Quad Flat Pack (PQFP), 4, 35, 37, 40, 42  
 Plating Through-Hole (PTH), 262  
 Polybenzo-bisoxazole (PBO), 79  
 Polyimides, 77, 115  
 Population, 105  
 Post Mold Cure (PMC), 152, 165  
 Power Management IC (PMIC), 7, 175, 299  
 Printed Circuit Board (PCB), 4, 5, 7, 32, 37, 42, 44, 75, 81, 88, 98, 110, 114, 124, 138, 158, 181, 195, 309, 336, 343, 418, 426  
 Probability, 105  
 Processors, 30, 54

## Q

Quad-Flat No-leads (QFN), 35, 40

**R**  
 Radar, 2  
 RDL-first, 176, 269  
 RDL-interposer, 12, 271, 276  
 Reconstituted carrier, 116, 165  
 Redistribution-Layer (RDL), 5, 9, 75, 88–90, 114, 116, 118, 138, 147, 148, 150, 154, 163, 164, 171, 180, 188, 239, 241, 294, 299, 313, 319, 343, 357, 418, 442  
 Reliability, 51, 336  
 Resistors, 35  
 Reticle size, 329  
 Re-work, 42, 44  
 Rome server, 427

Room temperature, 388  
 Rosin fluxes, 36  
 Router chip, 347

**S**  
 Sacrificial release layer, 180, 242  
 Sample size, 105  
 Saw street, 147  
 Scaling, 415  
 Scanning Electron Microscope (SEM), 9, 155, 163, 176, 188, 255, 275, 313, 320, 383, 391, 404, 446  
 Seams, 380  
 Self-alignment, 51  
 Self-driving cars, 1, 441  
 Semi-Additive Process (SAP), 259, 262  
 Semi-embedded TSV-interposer, 315  
 Sensor chip, 355  
 Server, 2  
 Shear strain rate, 81  
 Shear stress, 81  
 Shock (drop) test, 100, 197  
 Sidewall cracking, 77, 115  
 Si-less RDL interposer, 269  
 Silicon, 29  
 Silicon-Less Integrated Module (SLIM), 179, 246  
 Silicon substrate, 420, 421  
 Silicon-to-silicon, 379  
 Silicon Wafer Integrated Fan-Out Technology (SWIFT), 177, 246  
 Single-side PCB, 33  
 Skin effect, 442  
 Small Outline Integrated Circuit (SOIC), 4, 35  
 Smart energy, 29  
 Smart factory, 1  
 Smart health, 1  
 Smart home, 29  
 Smart industrial automation, 29  
 Smartphones, 1, 27, 29, 76, 441  
 Smartwatches, 1, 7, 27, 76, 441  
 Snapdragon, 27, 30  
 Softening point, 445  
 SoIC + CoWoS, 435  
 SoIC + InFO, 435  
 Solder balls, 5, 35, 152, 343  
 Solder bump, 47  
 Solder joint, 9  
 Solder joint crack, 101  
 Solder joint defects, 42, 44  
 Solder joint reliability, 39

- Solder mask, 90  
Solder mass reflow, 51  
Solder metal powder, 36  
Solder-On-Pad (SOP), 58  
Solder paste, 35, 37, 44  
Solder reflow, 40  
Solder Resist Opening (SRO), 93, 185, 193  
Solvent, 36  
Squeegee, 37  
Stainless steel, 37  
Stand-off height, 59  
State-of-the-art Heterogeneous Integrated Packaging (SHIP), 414  
Stencil, 37, 156  
Stencil printing, 37, 44  
Stencil thickness, 39  
Stepper, 79, 154  
Stress relief gap, 315  
Stress relief (reliability) buffer, 306  
Strip lines, 33  
Styrene-Ethylene/Butylene-Styrene (SEBS), 460  
Sub-6 GHz 5G, 2  
Supercomputer, 1, 441  
Supercomputing, 441  
Surface Mount Devices (SMDs), 32, 35, 40, 44  
Surface Mount Technology (SMT), 4, 19, 27, 30, 32, 40, 44, 77, 99, 114, 115, 126, 196, 336, 418, 465, 470, 473, 487  
Surface roughness (Ra), 169, 442  
Switch, 2  
Synchronous Dynamic Random Access Memory (SDRAM), 345  
System-in-Package (SiP), 4, 7, 18, 27, 29, 30, 45, 309, 355, 469  
System-in Wafer-Level Package (SiWLP), 176  
System-on-Chip (SoC), 27, 29, 313, 322, 336, 362, 367, 399, 414, 435, 465, 485, 487  
System on Integrated Chips (SoIC), 17, 368, 399, 432  
System-on-Wafer (SoW), 299  
System-technology drivers, 1
- T**  
Tablets, 1, 27, 29, 76, 441  
Temporary carrier, 89, 116, 147, 180  
Test-Element-Group (TEG), 404  
Tetraethylorthosilicate (TEOS) oxide, 406  
Thermal Conduction Module (TCM), 7  
Thermal conductivity, 50  
Thermal cycling, 109, 129, 201  
Thermal Expansion Coefficient (TEC), 301  
Thermal fatigue life, 137  
Thermal Interface Material (TIM), 309  
Thermal management, 308, 408  
Thermal release tape, 114  
Thermal resistance, 307  
Thermocompression Bonding (TCB), 4, 54, 276, 356, 364, 465  
Thin-chip, 56  
Thin-film layer, 9, 251  
Thin Small Outline Package (TSOP), 35  
Thin-substrate, 56  
Through Glass Via (TGV), 333, 334, 347  
Through Mold Via (TMV), 355  
Through Package Via (TPV), 349  
Throughput, 54  
Through-Silicon Hole-Interposer (TSI-Interposer), 318  
Through-Silicon Vias (TSVs), 29, 239, 311, 313, 315, 317, 343, 362, 365, 390, 401, 421  
Trace, 32  
Transceiver, 2, 324  
Transfer molding, 53  
Transimpedance Amplifiers (TIA), 332  
Transmission Electron Microscopy (TEM), 400, 406  
Transmission loss, 442, 457  
Transmission speed, 4  
True Weibull slope, 108  
True wireless stereo, 27  
TSV-interposer, 4, 11, 12, 263, 305, 308, 326  
TSV-less-interposer, 257, 262, 265  
Two-side assembly, 32
- U**  
UltraCSP, 75  
Ultra Format Organic Substrate (uFOS), 255  
Ultraviolet (UV) laser, 93, 114, 171  
Undeformed shape, 111, 135  
Under Bump Metallurgy (UBM), 48, 79, 89, 118, 180, 266, 319, 367  
Underfill, 7, 12, 51, 83, 191, 316, 336, 343, 418  
Under-the-hood, 78, 88, 115  
Uni-Substrate-Integrated Package (Uni-SIP), 163  
Unit Per Hour (UPH), 60

**V**

Vacuum, 53, 93  
VCSEL, 332  
Via-last, 371  
Via-middle, 371, 401

**W**

Wafer And Board level Embedded package (WABE), 355  
Wafer bumping, 45, 46, 148, 180, 189, 343, 470, 473  
Wafer-Level Chip-Scale Package (WLCSP), 75, 79, 88  
Wafer Level Packaging (WLP), 75  
Wafer-on-Wafer (WoW), 4, 17, 19, 303, 371, 399, 407, 416, 465, 475  
Wafer sizes, 29  
Warpage, 165, 259, 336, 407, 442  
Water soluble fluxes, 36  
Wearables, 1, 27, 441

**Weibull distribution, 105**

Weibull slope, 105, 131, 201  
Weibull slope error, 108  
White-Light Interferometry (WLI), 406  
Wide-bandwidth memory, 29  
Wire bond, 4, 19, 75, 239, 344, 465, 470  
Wire interconnects, 49

**X**

X-ray image, 99, 158, 163  
X-ray inspection, 40, 44

**Y**

Year-over-Year (YoY), 466  
Young's modulus, 86, 135, 452

**Z**

ZiBond, 379