



**2021 Edition**

## **Chapter 21: SiP and Module System Integration**

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## Chapter 21: SiP and Module

### Executive Summary and Scope

The past decade has seen a rush towards advanced semiconductor nodes along with market growth from smart mobile, AI and cloud at the edge, autonomous automotive, IoT, health and wearables. The functionalities of systems and devices have increased with respect to performance, energy consumption and – with System on a Chip (SoC) – the marriage of digital, analog and even MEMS and sensors; this has brought system-level performance to small form factors such as in smart phones, health monitors and smart homes. The advance in smaller feature sizes and the resulting billions of transistors on a chip bring together the benefits of different worlds of manufacturing, but such complex, monolithic devices result in high NRE costs; physical and cost constraints, as well as market needs, suggest an alternative is needed.

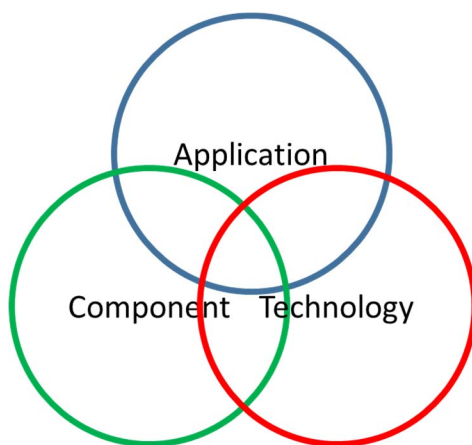
Heterogenous integration through SiP (System-in-Package) can leverage the advanced capabilities of packaging technology to create systems close to the SoC form factor but with better yield, lower overall cost, higher flexibility, and faster time to market; the latter has especially shifted the paradigm from SoC-centric to SiP-centric in the recent past even for volume products. Among SiPs introduced to the market are high volume, low power products like integrated camera modules, mobile device microprocessor units and IoT subsystems. Emerging, integrated power devices are starting to enter the market. This chapter highlights the market needs, technology paths, difficult challenges and potential solutions when addressing high-density system integration with advanced packaging materials, tools and techniques, with projections on required developments over the next 10 to 15 years.

### Introduction

**System in Package (SiP)** – SiP is a combination of multiple active electronic components of different functionality, assembled in a single unit, and providing multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components, and other packages and devices (see especially the Board Assembly section, and other Sections, in Chapter 8).

SiP typically refers to standard packages (such as SO, QFP, BGA, CSP, LGA) that can include dice of different semiconductors (e.g. Si, SiGe, SiC, III/Vs such as GaAs or GaN) and semiconductor technology generations (e.g. CMOS 65 nm, 45 nm, 28 nm, 14 nm, etc.).

The roadmapping effort for SiP concentrates on an approach based on current and emerging generations of packages and technologies. Currently, more than 1000 package families with sub-groups and specialties can be found in the market. Some of these packages are highly specialized to niche markets, while others are generic to serve multiple applications. Since most technology developments have initiated several optimization paths towards the needs of respective applications, a partitioning (classification) is extremely challenging. We need to select the right SiP concept based on the needs of applications and the available components, which we can then integrate into a SiP using the appropriate technologies (see Figure 1).



*Figure 1: Three-leaf range of influence for the selection of the right SiP approach*

The fundamental vision of SiP is to merge different functionalities (which may even come from different physical domains) into one package, thereby offering system-level performance in the form factor of a single package. Figure

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2 and Figure 3 demonstrate a breaking down of technologies into sub-groups indicative of the main distinctions seen in current SiP implementations.

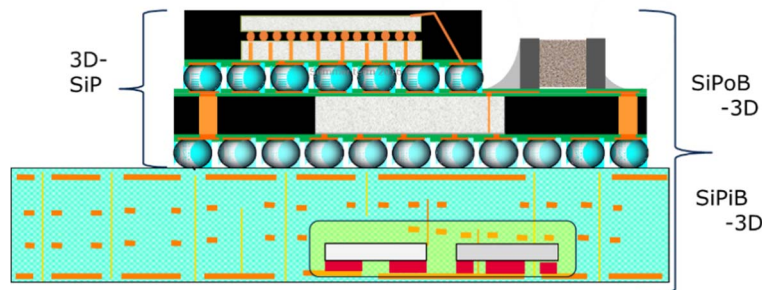


Figure 2: Multi-Level Representation of an SiP differentiating SiP-on-Board (SiPoB) and SiP-in-Board (SiPiB) [courtesy INFINEON AG]

The respective boundaries in the value chain are not clearly separated. The selected method for roadmapping to assess the challenges for heterogeneous integration concepts and implementation into SiPs is set up by distinguishing between 1) the technical challenges for the integration itself, and 2) the challenges imposed by the respective applications for the SiP implementation. Figure 3 shows the respective “packaging toolbox” and the application areas, mediated by the (standardized) package form factor.

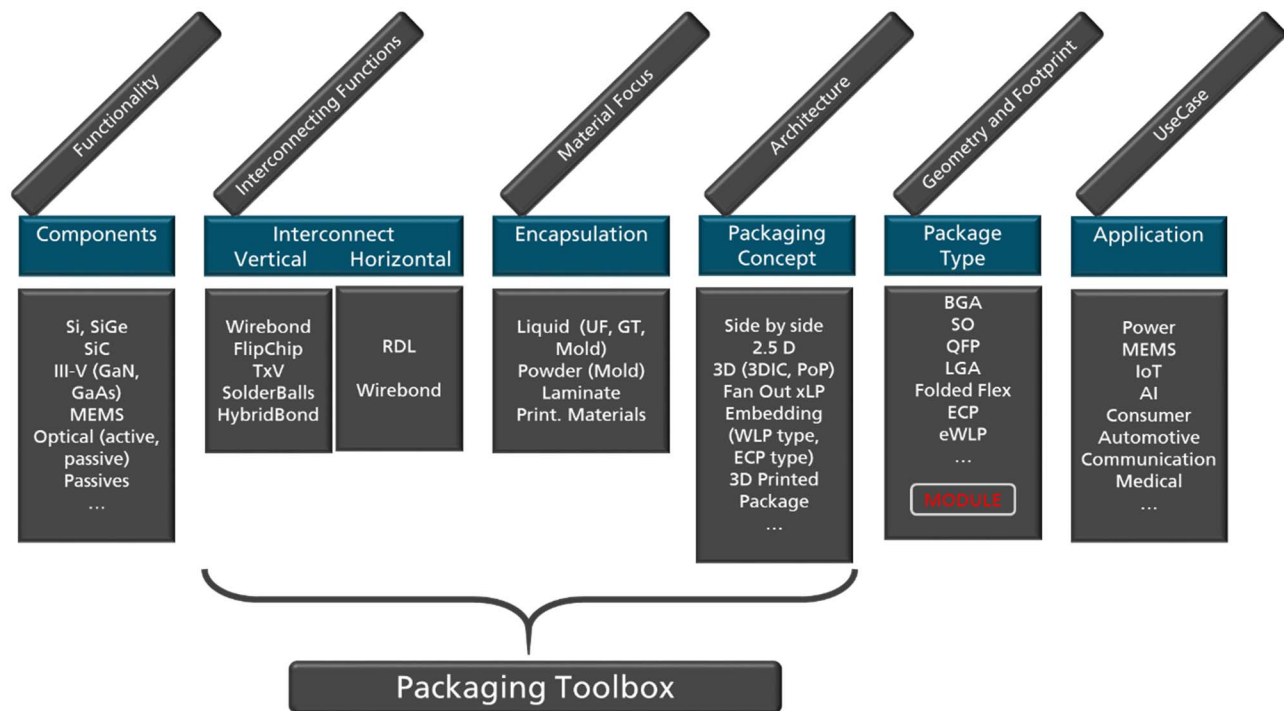


Figure 3: Concept of the "Packaging Toolbox", including interconnects, encapsulations, and packaging concepts and architectures as toolbox elements.

This chapter is organized as follows:

- First we present the technology portfolio available as of today (end of 2021) – with a focus on “interconnects” including the respectively used encapsulation processes and packaging concepts.
- Next we describe the challenges associated with using the required components to address some hallmark applications. These offer – in conjunction with the toolbox approaches – a methodology for selecting the most appropriate implementation.
- Finally we introduce the challenges driven by physics and by cross-cutting needs, including legislation.

For future SiPs there is – in accordance with the 2018 Joint European *Strategic Research Agenda* (SRA) by AENEAS, ARTEMIS-IA and EPoSS – a growing understanding that the current distinction between the hitherto separate value chains (*chip, package, and board/system*) is diffused. This includes, for example, chip manufacturers

offering minimum packaging form-factors, OSATs offering HDI-PCB with embedded chips, and EMS's using bare die for functionality increase on their products.

As shown in Figure 4, heterogeneous integration can appear on three levels: i) at the chip level, e.g. as monolithic SoC (System on Chip) or heterogeneously integrated “chiplet” concept; ii) at the package level, e.g. as SiP or PoP (Package on Package); and iii) at the board level, e.g. chip embedding in a PCB.

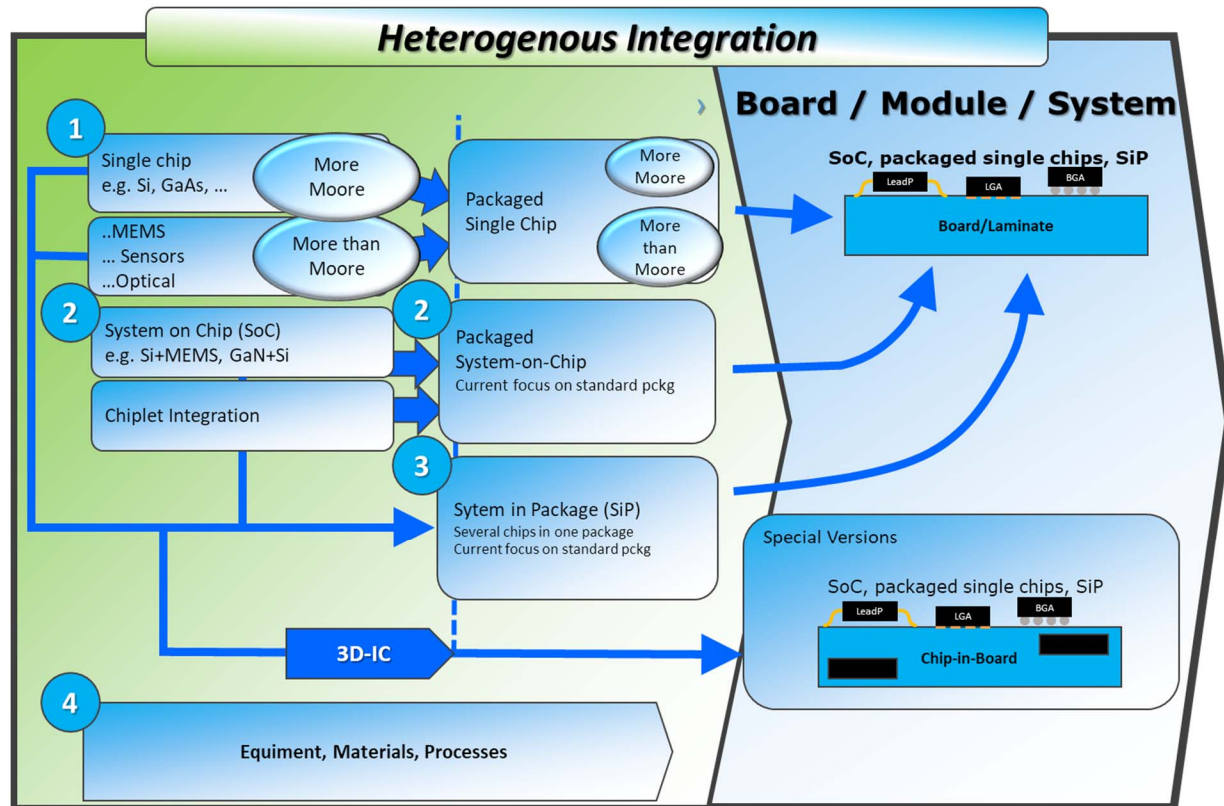


Figure 4: Transition from Chip to System; see also Joint Electronic Components & Systems (ECS) Strategic Research Agenda 2018. Heterogeneous integration can appear in all three domains: chip, package, and board/system.

Notably, aside from today's interconnect workhorses such as wirebonding and flip-chip bonding (which will be used for a long time to come), novel and highly promising technology innovations will be addressed in this chapter. In this context, *3D stacking* (3D-IC), *W/P-level fan-out packages*, and *embedded chip packages* (ECP or Chip in Board, with the associated Chip Embedding Technology – CET), along with extreme high-density interconnect approaches such as *hybrid bonding*, are considered *platform technologies* which will serve future needs.

There is also a growing requirement for accurate assembly technologies at the Package, Module, Board and System level; this technology requirement is also addressed as part of a packaging toolbox.

Using key applications for future markets – such as power, autonomous systems, sensor-integrated systems and bio-integrated devices – an approach for merging components with appropriate technologies to address their respective challenges is provided, to enable a holistic perspective in SiP implementation, selecting from the next-generation technology tool box.

## Toolbox Perspective

### 1. Technology toolbox description

For setting up a SiP toolbox, we distinguish between **interconnect technologies** (vertical and horizontal), **encapsulation technologies** (protection and stabilization), and **architectures** (stacking and packaging concepts) – see Figure 3. The number of available technologies for SiP implementation has grown and includes not only side-by-side integration, but has also moved to 3D with the advent of stacked-chip assemblies and vertical electrical contacts such as through-silicon via (TSV) technology. SiP integration includes, on the one hand, core technologies like wirebonding or flip chip bonding, and on the other hand hybrid integration concepts. Examples for hybrid integration concepts are package-on-package (PoP) or embedded-chip technologies which bring together hitherto separated value chains to realize highly functional systems.



## 1.1 Interconnects

For setting up an SiP, we distinguish between:

- *Vertical electrical contacts*, like TxV (*Through-X-Vias*, with X representing silicon (S) or glass (G), as well as encapsulant (E) or molding (M)), flip chip (e.g. as part of 3D IC), and solder bump interconnect (for Package-on-Package – PoP).
- *Horizontal electrical interconnects* (e.g. Redistribution Layers – RDLs – in case of single or of multiple interconnect layers).

Today's workhorse, wirebonding, has the advantage that it can provide horizontal (chips side-by-side) as well as vertical (e.g. Chinese tower architecture) interconnects. But this technology reaches severe limits: for example, with respect to high parasitics and low manufacturing tolerances.

Table 1 summarizes some of the current existing technologies, with their state-of-the-art in volume production.

Table 1: SiP Interconnect Technologies (as of 2020)

Technology Toolbox					
State of the Art	suitable for chipsize	chip I/O magnitude	feasible chip pitch	served chip count	max. # of domains served
	[mm]	[10s, 100s, 1000s]	[ $\mu$ m]	[#]	[electrical, optical, mechanical, biochem, ...]
Wirebonding	<40mm	100s	20	8	4
FlipChip Bonding	<40mm	1000s	15	8 (TSV stack)	4
RDL Redistribution Layer	<40mm	100s	5	3	2
TxV's	n/a	1000s	10	2	2
Solder Ball	n/a	1000s	25	2	1
Hybrid Bonding Interconnect	<25mm	1000s	1	8 (TSV stack)	4
suitable chip size: Interconnect technology already demonstrated					
chip I/O magnitude: capability derived from technical feasibility, e.g. "100s" covers anything up to 999 I/Os					
feasible chip pitch: derived from currently demonstrated implementations					
served chip count: derived from currently demonstrated implementations, including different chip technologies, stack or side-by-side concept					
domains served: derived from currently demonstrated implementations, merging electrical signal, optical signal, MEMS sensing and actuation, RF wireless and power					

In subsequent sections, the individual technologies are briefly described to show both current state-of-the-art as well as their future evolution.

### Interconnect toolbox elements:

#### a. Wirebonding including stacked chips (HORIZONTAL and VERTICAL)

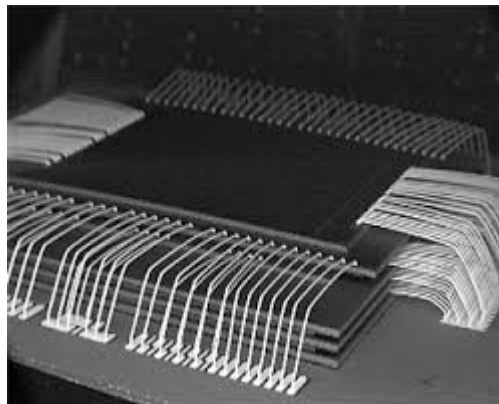


Figure 5: Stacked chips using wirebonding [1]

Wire bonding is still the most cost-effective and flexible interconnection technology in microelectronics. The wire bonding process utilizes force, ultrasonic power, and temperature to produce a metallurgical joint. A large range of wire diameters, typically from 15  $\mu$ m to 500  $\mu$ m, are available. Round wires and ribbons of various metallic materials, such as Au, Al, Ag, Cu, Cu-Pd, and Pt, can be used. 3-dimensional system packages, e.g. stacked chip assemblies, can be connected with high throughput and automated adjustment to chip misalignments. The loop shapes of the wire bonds are highly reproducible. This is a key demand for highly integrated connection schemes. See the *Wirebond* section in Chapter 8.

Driven by the advent of thin-chip technology, processes for chip stacking (including die attach film – DAF – and multi-level fine pitch wirebonding) have become state of the art. They allow a shift from horizontal to vertical interconnect strategies. Sophisticated wire routing in three dimensions and the adaption of mold materials to flow through the densely arranged wire mesh for optimum encapsulation, have since developed as workhorses for SiP applications. This wirebond approach is mostly limited to serving the electrical domain only (i.e. memory- and memory-logic stacks). On a coarser integration level, MEMS components with their logic elements have been built, especially to serve mobile device and automotive use cases.

#### b. FlipChip including Chip-on-Chip via TSV (VERTICAL)

While wirebonding has adapted established technologies in an evolutionary approach, using Through Silicon Vias (TSVs) offers a much more radical innovation path. Whether using via-first, via-middle or via-last approaches, all of these provide a direct path from the active frontside to the chip's backside, allowing a direct chip-to-chip integration in flip-chip bonding. Microbump formation (solder or Cu pillars) as well as direct bonding processes have evolved accordingly, so today a large number of contacts distributed over the chip area can be accommodated for 3D stacking of components.

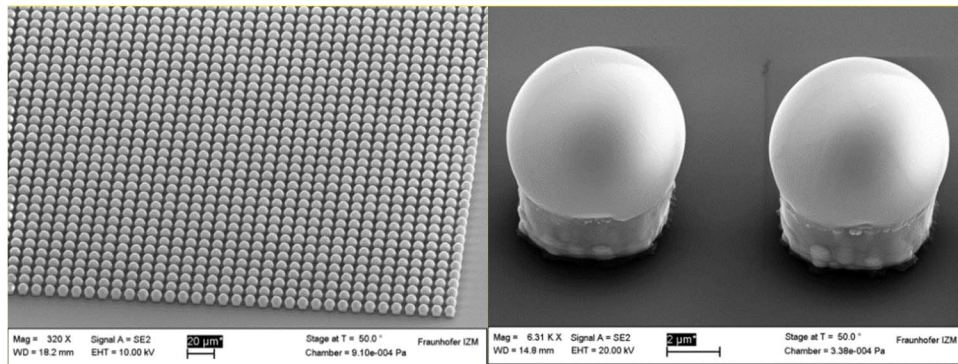


Figure 6: Flip chip bumps for 10um pitch area array interconnect [courtesy TU Berlin]

However, due to the fact that the need for similarly sized chips and matched I/Os are omnipresent, currently this high-tech implementation is limited to several niche applications such as high-density flash memory and high-bandwidth memory-logic integration (e.g. Hynix [2], Intel [3]).

#### c. Hybrid Bonding interconnect (VERTICAL)

Using advances in wafer bonding techniques and TSVs, an emerging technology for chip integration for SiP is hybrid bonding. The technology has proven its merits already in wafer-to-wafer bonding, offering the highest level of integration so far for camera chipsets (e.g. Sony). The principle is that the wafers to be connected are fine-polished to allow direct bonding of the joined surfaces (i.e. without any intermediate layer), as developed for MEMS packaging. Here, with TSV's in place, the contacts are precision aligned and joined, and the Van-der-Waals forces forming the bond via the dielectric surface pull the wafers together on an atomic-scale. An annealing process enables metal diffusion between the contacts, forming direct interconnects. The precision of the alignment of the equipment and the required contact area for the nominal current density is the limiting factor for the interconnect pitch. Currently a minimum pitch of 1um on a full area array scale for 300mm wafers can be achieved, with the possibility of multi-wafer stacking as well. [4]

However, as the technology requires access to full wafers for the wafer-scale preparation, as well as wafer-wafer bonding, its use is restricted to specific use cases with the manufacturer controlling all aspects of wafer fabrication and subsequent interconnect processes.

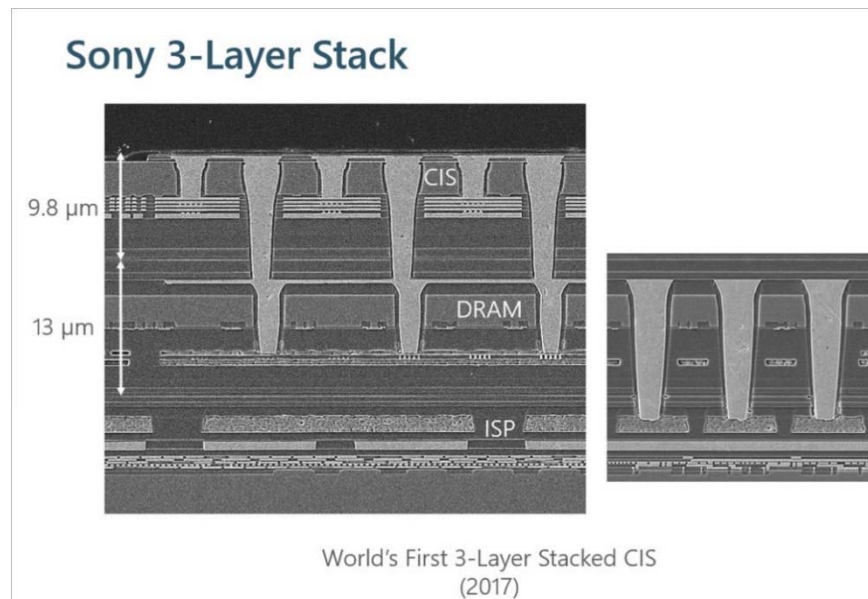


Figure 7: Stacked chips using hybrid bonding [5]

#### d. Redistribution Layer (RDL) Interconnect (HORIZONTAL)

Redistribution layers have emerged as enablers for wafer-level packaging, offering fan-in redistribution of peripheral contacts across the full area of the chip. Initially seen as an intermediate step between the era of wirebond and flip chip, the WLPs have since established themselves as the third workhorse of today's semiconductor packaging industry, enabling cost-effective, reliable, small size (chip-scale) packages. RDLs however, are also being used to interconnect adjacent chip sets in a more complex setting. RDLs started out with lithographically defined structures, building on the technologies of thin film substrates: seed layer deposition, resist deposition and lithographic structuring, electrodeposition, strip and etch. With this technique,  $\mu\text{m}$ -scale features with adequate line thickness were made possible, i.e. larger than 1:1 aspect ratio using high aspect ratio (HAR) resists – see Figure 8.

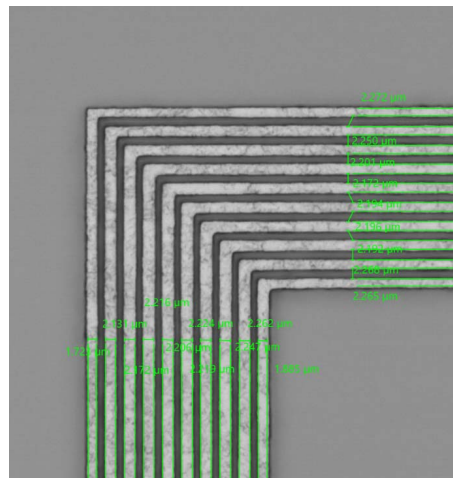


Figure 8: RDL technology with 2  $\mu\text{m}$  L/S [courtesy TU Berlin]

Multi-layer capability has been readily demonstrated, overcoming planarity issues and stress-induced wafer warpage up to 6 layers. Recently, direct deposition by aerosol jet printing, silver ink printing or even *Laser Induced Forward Transfer* (LIFT) have emerged, without the need of a mask set, thus reducing the setup and infrastructure cost.

### 1.2 Encapsulation Technologies

Traditionally, encapsulation has been used to protect the sensitive wirebonds from environmental influences (i.e. *molded package* or *glob top* protected chip-on-board). Also, encapsulation allowed flip chip contacts on ceramic or laminate to achieve high reliability under critical operating conditions using capillary-flow underfill materials. For these legacy processes, both liquid encapsulants (usually silica-filled epoxy materials) as well as pellet-type electronic mold compounds, liquefied during the mold process, have been used. With the advent of single-chip *Molded Array*



*Packages* and subsequently *Large Area Molding*, granular and powder materials used for compression molding were developed and are now used not only for protective encapsulation, but also to offer the mechanical basis for modern packaging concepts like eWLP and Fan-Out Panel-Level Packaging.

Aside from these technology innovations emerging from the chip packaging needs, another pathway coming from printed circuit board manufacturing has found its application in encapsulating chips and (sub)systems. The core layer of a PCB is populated with active and passive dies and subsequently co-encapsulated during the vacuum lamination step where b-stage epoxy resin sheets are liquefied and bond the individual laminate (prepreg) layers of the PCB to each other. With state-of-the-art micro-via technology, these components are connected to the outer wiring layers in the same fashion as the inner routing layers (see Chip Embedding Technology section 1.3.2), while the binding resin serves simultaneously as protective encapsulant and mechanical bond between component and PCB layers.

Encapsulants have been designed for their intended use, i.e. EMCs were designed for subsequent assembly processes, while globtops had to withstand the rigors of everyday use. An indicator for their use in SiP manufacturing processes and prospective caveats is given by the moisture sensitivity level (MSL, see IPC/JEDEC J-STD-020D-01 [6]).

Table 2 shows the current state of the art for industry grade materials.

Table 2: Encapsulants for protection (MSL: Moisture sensitivity level, 1:best, 3:worst)

Encapsulant	provisioning	filled	SiP application area		MSL
GlobTop	liquid	x	CoB-Wirebond	chip protection	3
Underfill	liquid	x	FlipChip	chip protection	3
Pre-Applied Underfill	film	o	FlipChip	chip protection	3
EMC	pellet	x	standard pck.	chip protection	1
MAP-EMC	granule	x	BGA, QFN	package structure	1
FO-xLP EMC	powder	x	eWLP, FO-PLP	package structure	1
Laminate	film/sheet	o	ECP	package structure	3

As either of the encapsulation processes described is an intrinsic part of a given package concept, details on their use will be provided in the respective portions of the next section 1.3.

### 1.3. Architectures and package concepts

#### 1.3.1 Package-on-Package (PoP)

TSV-FlipChip technologies have shortcomings with respect to inherent difficulties for testing, processing cost and I/O matching. Package on Package (PoP) is a concept using finished and standardized packages, which are stacked on top of each other, as in Figure 9. Each single package can be tested alone. The possibility for long-term planning with respect to I/O footprint, as well as the known cost situation and established infrastructures with the OSATs, has been a focus of technology evolution.

The advent of thin chips in combination with thin, high-density substrates and minimum capping mold encapsulation has offered the opportunity to leverage the advantages of PoP to serve many application requirements at target cost.

PoP has since seen the transition from mimicking the function of stack-chip integration by using wirebonding via peripheral BGA concepts towards through-mold vias – replicating vertical die-to-die stacks. This enables OSATs to provide a solution with substantially higher compatibility with established infrastructures, EDA tools and testability.

A major trend for PoP is ongoing miniaturization and integration of more functionality into a smaller volume. Thinner chips and thinner packages will drive currently applied materials combinations (e.g. in memory stacks) to their limits, as uncontrolled warping and thermomechanical deformation will impact fabrication and product reliability.

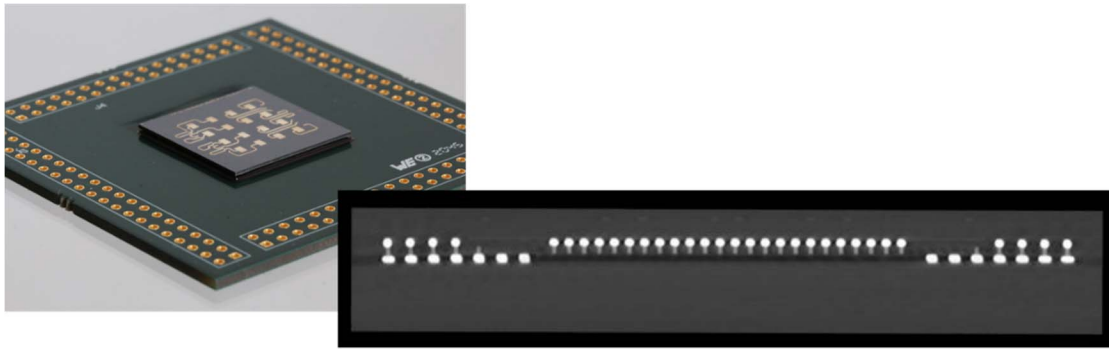


Figure 9: Package on Package Architecture [courtesy of Würth Electronic]

### 1.3.2. Chip Embedding Technologies (CET)

#### a. Active chip

While the initial concept of using active circuitry embedded into the substrate had seen its first conceptions as early as 1970, it took nearly 30 years to be picked up by academia and industry's R&D. The tipping point was actually the availability of additive HDI substrate technology and thin active chips with compatible pad metallization at a decent quality level.

From that point on, OSAT and PCB manufacturers alike have pushed forward with the advance of structure sizes, alignment precision, tolerance compensation, chemistries for the collective wiring, and test/design strategies. In principle, the mainstream technological approach used nowadays follows the process of HDI substrate processing.

Firstly, the respective layers are defined (typically by LDI) and then the thinned active chips are placed and fixed in their target positions. The full stack to realize the different laminate layers is built by vacuum-lamination, ensuring a full encapsulation of the thin chips. Laser via-hole drilling, similar – and in parallel – to the creation of blind vias, exposes the pads for the subsequent chemical deposition of the interconnect metal, fully compatible with BU-HDI technology (see Figure 10).

This concept requires known-good die (KGD), or at least a quality level acceptable to the target yield figure, for successful commercialization. For this technology, testing can only identify defective assemblies and mark them for discard, without repair options. Building a multi-die SiP with this technology is thus limited to the use of ICs with adequate quality level, somewhat limiting its acceptance to high-volume, low-IC-number SiPs.

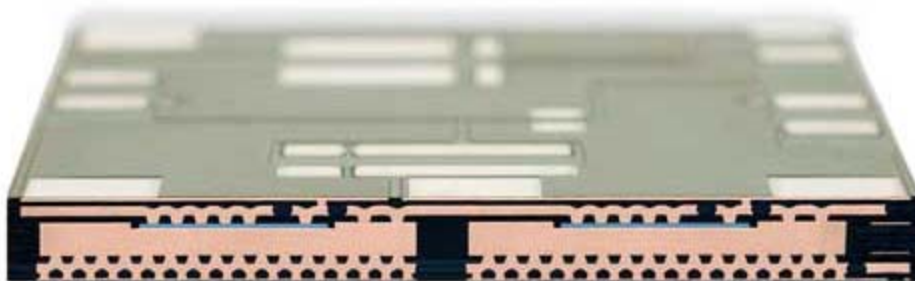


Figure 10: Embedded Chip Technology (CET) Architecture [courtesy Schweizer, Continental & Infineon]

#### b. Passive chip and integrated passive device (IPD)

Typically, a large number of passive components is required for combining the different functionalities in a SiP. This includes inductors and capacitors in larger numbers than active dies. Passives are especially needed for radio frequency (RF) circuits to provide impedance matching, but also for chips that require decoupling and noise blocking, etc. For implementation of passive devices (as in Figure 11 a-g), we distinguish between:

- embedding of passive chips,
- embedding of standard passive components, and
- design of so-called integrated passive devices (IPD).

Passive silicon chips are devices without active transistors. A high-ohmic silicon substrate is used for implementation of capacitors, resistors and inductors in the BEOL. This technology today still is challenged to meet viable cost targets.

The other possibility is the use of embedded standard passive devices, which are integrated in the laminate stack – mimicking the CET process steps. The shrinking of MLCC components from 0805 to 0201 sizes, and most recently to 01005 and 008004, allows mounting large numbers of passives on a given footprint. With these small and thin components, high yield at low cost becomes more and more of a challenge with current assembly processes.

The third possibility are IPDs, which have attracted a lot of interest during previous years due to their compact size and high level of integration. Foundries are using this packaging technology already to integrate inductors, capacitors and resistors in the same die to provide one or more required circuit functions. Examples are passive component banks, matching devices, filters, multiplexers, couplers, transformers, baluns, antennas, etc. These embedded passives are suited for wireless RF front-end systems, as they result in better system performance than with SMD components. They also can be designed at lower cost compared to passives integrated onto active ICs.

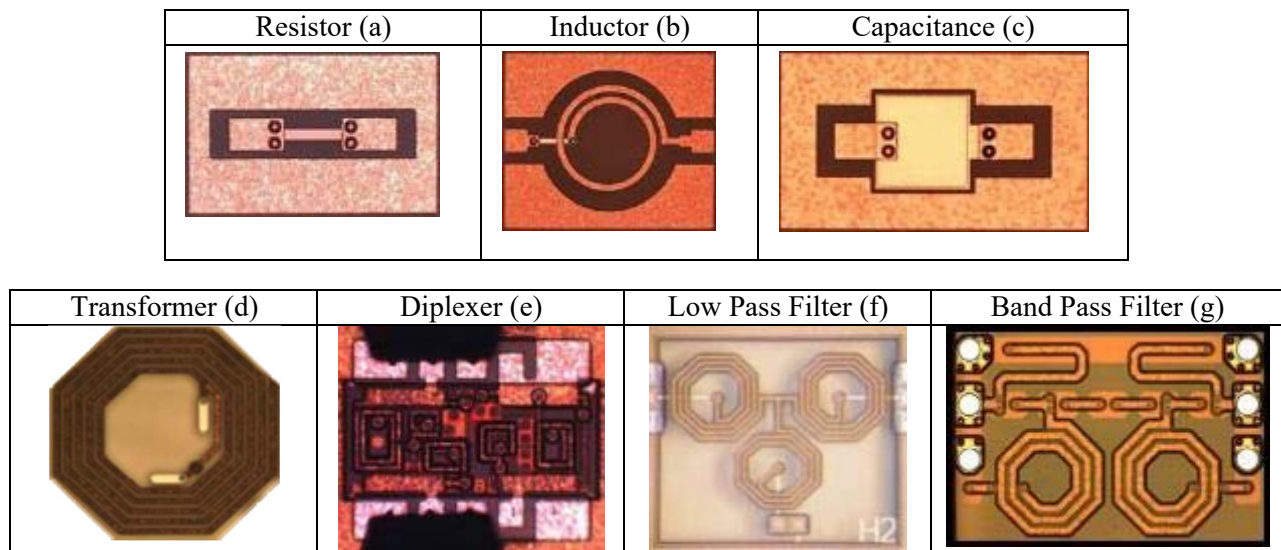


Figure 11: Integrated Passive Devices

Some implementations of the mentioned integration techniques are provided in Figure 11a-g. As before, the technology for integration into the PCB is identical to what has been described in the previous section.

IPD component technology is simultaneously migrating from 2D (multi-RDL) inductor to FO (-Inductor and -3D) tall-pillar inductor platform for high-integration requirements. More and more customers are starting to design the inductor in the FO layer, helping to reduce SMD quantity and package size. 3D tall-pillar inductors not only can achieve high Q quality, but also the pillar height can be designed for chip embedding in the same layer (Figure 12).

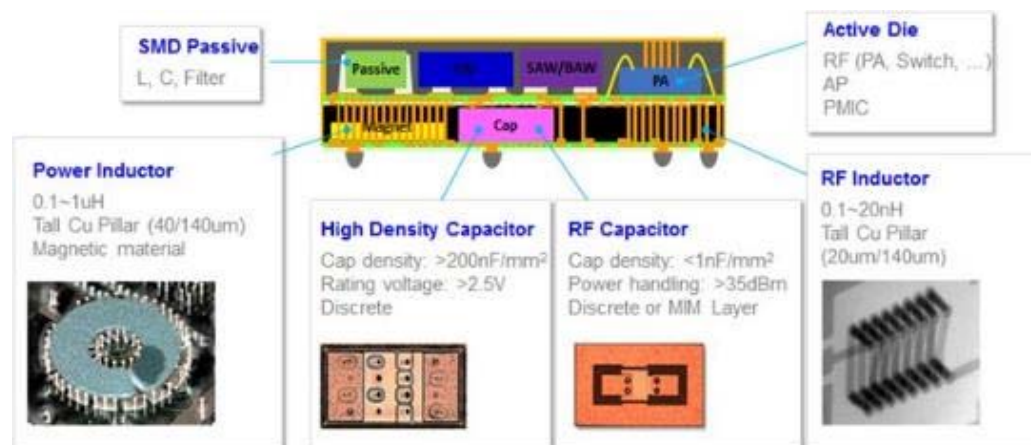


Figure 12: Next gen IPD moving from 2D to 3D [courtesy ASE]

### c. Non-functional interposer chips (EMIB)

As the routing density of even HDI substrates is limited by current advanced PCB processing capability – especially with high-pin-count chips – these laminates are currently challenged beyond their limits. For the case of parallel data transfer buses, connecting two IC's with high-bandwidth requirements via a large number of interconnect I/Os, alternatives are required to the capabilities of HDI. RDL-on-silicon plays an enabling role in this concept. With hybrid integration concepts such as Intel's Embedded Multi-die Interconnect Bridge (EMIB) [7], this challenge can be addressed without the requirement of a silicon interposer spanning beyond the chip footprint of the (multiple) connecting dies. With EMIB, the aforementioned technology for CET is reduced to embedding a high-density interposer element in the top layer of the SiP laminate board, in the area where the high-density interconnects are needed, bringing together the best of the two worlds while adding only the cost for the EMIB high-density interposer (see Figure 13).

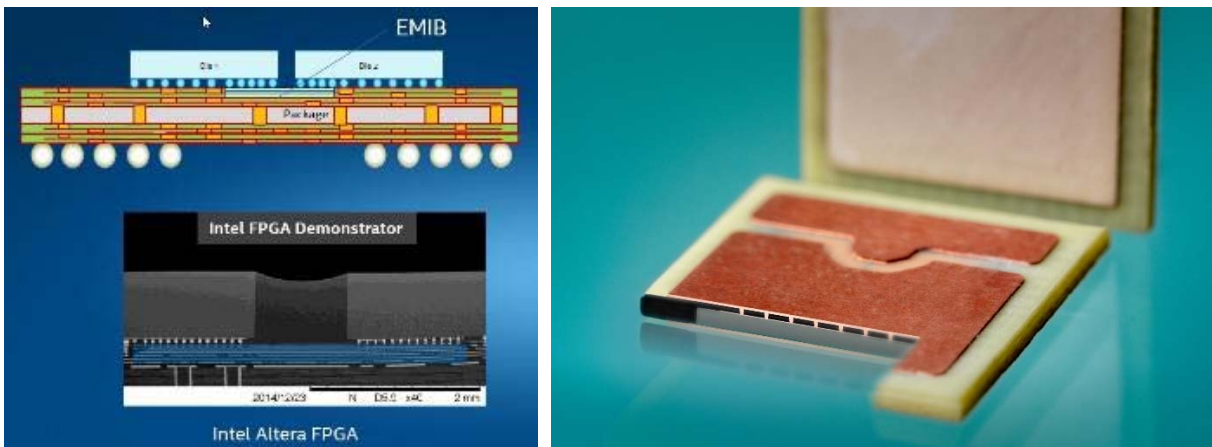


Figure 13: CET for horizontal integration [courtesy INTEL Corp.]  
Integration of Power IC into Laminate [courtesy Fraunhofer IZM]

### 1.3.3. Fan-out Wafer Level Packaging (FOWLP)

For Fan-out Wafer Level Packaging, the two basic process flows involve the Mold-first or the RDL-first approach. For the Mold-first process, a face-down and a face-up option also exist. Both variants are already in mass production.

FOWLP has a high potential for significant package miniaturization, affecting not only package volume but also thickness. The main advantages of FOWLP are the substrate-less package, lower thermal resistance, higher performance due to shorter interconnects, together with direct IC connection with thin-film metallization instead of wire bonds or flip chip bumps, and lower parasitic effects. The inductance of the FOWLP is much lower compared to FC-BGA packages, making it ideally suited for RF applications. In addition, the redistribution layer can provide embedded passives (R, L, C) as well as antennas, using a multi-layer structure (e.g. 2L and 3L RDL).

Heterogeneous system integration for SiP also includes 3D routing of electrical signals and double-sided redistribution layers for package-on-package (PoP) stacking. Different technologies are available for through-package or through-mold vias. Available solutions include plated Cu pillars applied before molding, integration of vertical interconnect elements made from printed circuit boards, Si or molded wafers, and laser-drilled and direct-metallized vias.

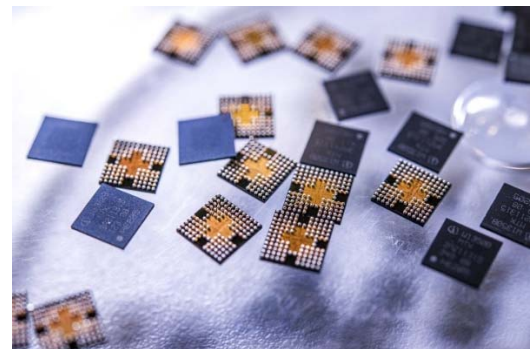
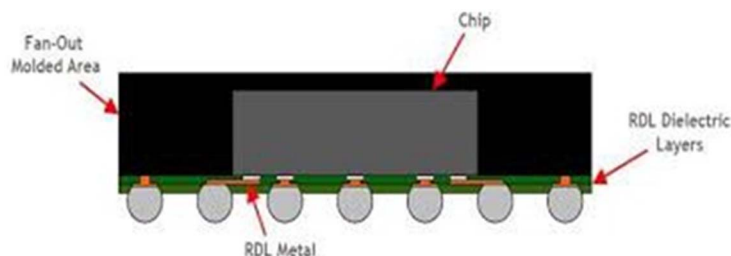


Figure 14: eWLP for a fan out wafer level package (FO-WLP) concept [courtesy of Infineon]



The fan-out WLP technology allows broad use for system integration. Figure 15 shows an example of two dies stacked with their backside bonded. The bottom die has its active layer to the bottom RDL; the upper die has its active side to the upper RDL. On the upper RDL, passive SMD devices are included for this system. The upper and lower dice are connected with a TEV (Through-Encapsulant-Via).

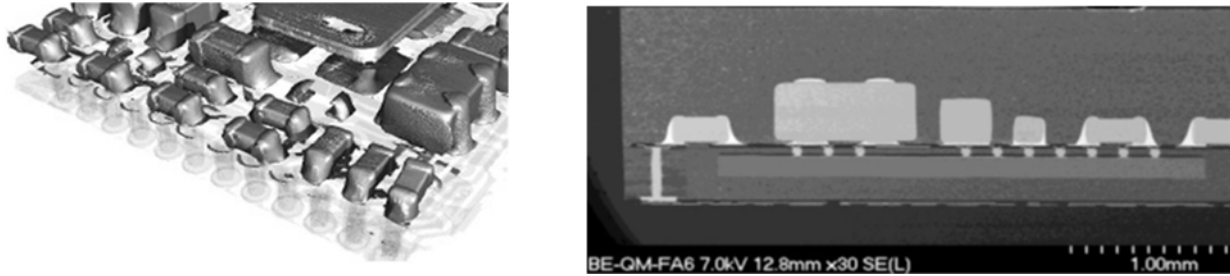


Figure 15: Example of a stack of two backside bonded dies.  
On the upper RDL, passive SMD devices are included for this system (courtesy Infineon).

### 1.3.4 Fan-Out Panel Level Packaging (FOPLP)

Fan-out Wafer Level Packaging (FOWLP) is one of the latest packaging trends in microelectronics. Manufacturing is currently done on wafer level up to 300 mm and 330 mm respectively. For higher productivity and thus lower costs, larger form-factors have been introduced. Instead of following the wafer-level roadmaps to 450 mm, panel-level packaging (PLP) is perceived as a lower cost alternative and the next big step, with many companies, including Samsung SEMCO, Nepes, Powertech and Deca with ASE, having already announced that they are preparing for PLP in volume manufacturing and having brought first products to market [8]. Sizes considered for the panel range from 300x300 mm to 457x610 mm or 510x510 mm up to 600x600 mm or even larger, influenced by different technologies coming from printed circuit board, solar or LCD manufacturing (Figure 16).

Key indicators derived from these architecture level/package concepts of 1.3.1-1.3.4 are summarized in Table 3:

Table 3: Overview of key indicators for package concepts (in alignment with Table 1 for “Interconnects”)

Technology Toolbox					
State of the Art	suitable for chip size	chip I/O magnitude	feasible chip pitch	served chip count	max. # of domains served
	[mm]	[10s, 100s, 1000s]	[ $\mu$ m]	[#]	[electrical, optical, mechanical, biochem, ...]
Package on Package	<20mm	100s	depending on internal	6	4
Embedded Chip Technology	<40mm	100s	50	6	3
FO-W/PLP	<40mm	100s	20	4	4
suitable chip size: Interconnect technology already demonstrated					
chip I/O magnitude: capability derived from technical feasibility, e.g. “100s” covers anything up to 999 I/Os					
feasible chip pitch: derived from currently demonstrated implementations					
served chip count: derived from currently demonstrated implementations, including different chip technologies, stack or side-by-side concept					
domains served: derived from currently demonstrated implementations, merging electrical signal, optical signal, MEMS sensing and actuation, RF wireless and power					

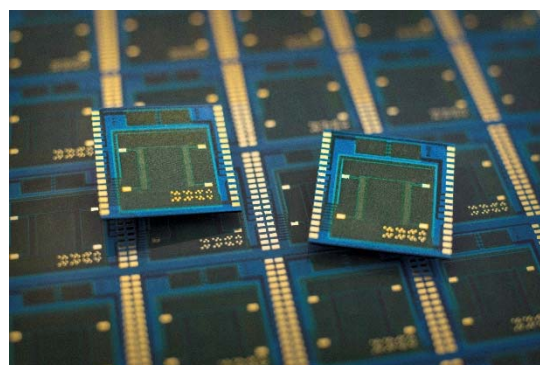


Figure 16: FO-PLP for System in Package integration.



### 1.3.5 Chiplet Technology

As a leg bridging the application and technology side, chiplets have been in discussion since the late 1980s. With the advent of the before-mentioned interconnect technologies and package concepts, the approach has gained new impetus. While “Chiplet” by itself cannot be classified either into the elements of the interconnect toolbox or the architectural concepts, the concept both makes use of these building blocks as well as drives elements of these.

Differentiation needs to be done on the side of IP partitioning (mostly driven by novel business models) and technology partitioning, the latter combining the elements of the toolbox in a processing combination, while the former focuses on the physical implementation of individual IP building blocks and combining these into a whole system.

DARPA’s CHiPs program [9] represents this concept (Figure 17), being agnostic to the final integration process but ensuring that critical IP building blocks can be combined, typically via silicon HD interposers.

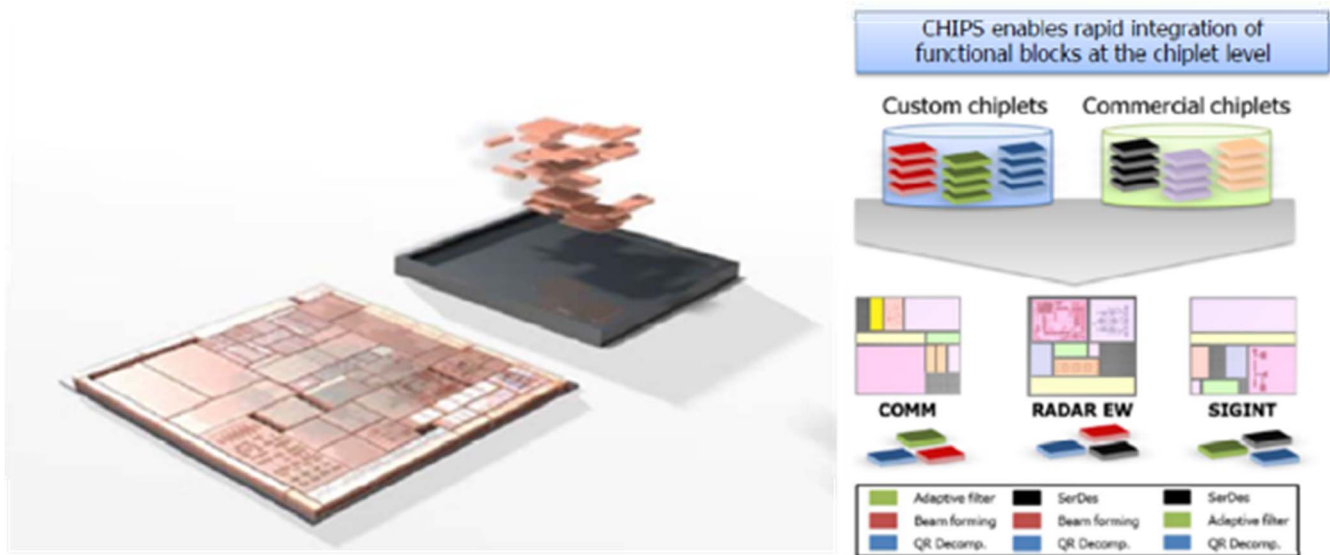


Figure 17: Chiplet concept as described by DARPA

This approach offers the following features:

- modular and reusable IP-block in physical form;
- complying with electrical and physical interface standards;
- to be assembled with existing and emerging industry standards; and
- tries to leverage the best aspects of both SoC and SiP.

With the advent of 7nm nodes and beyond, there is a need to merge CMOS cores from different fabrication (i.e. node) techniques, plus non-CMOS technology has become necessary for cost and performance reasons. However, larger physical IP blocks can no longer be easily built on a single HD Si interposer because manufacturing these is limited to ~ 1 inch (2.5 cm) in size due to cost/yield reasons. To overcome this issue, the OSDA initiative [10], Intel [11], LETI [12] and ULCA [13] have independently suggested merging PCB and HD Si interposer concepts to form the carrier for these IP building blocks, gaining the advantages of both worlds with respect to cost, performance and size.



Figure 18: HD Si Active Interposer Technology for IntACT Chiplet realization (courtesy CEA Leti [14]).

With these considerations in mind, Figure 18 depicts the Chiplet approach with the definition of being *functional, verified, re-usable physical IP blocks embedded in an eco system defining interface standards and assembly standards for rapid implementation of integrated systems with performance level of SoCs*. It is expected to bring advanced semiconductor technology and high-end integration and packaging into an intertwined value chain, with the prospect of high-performance and energy-efficient modules.

### 1.3.6 Modules

Modules have since evolved with the promise to bring maximized functionality for specific use cases not only into a package form factor ready for use by, for example, an OEM/ODM, but to integrate the functionality to the level of the end user. While previously such a product was built leveraging all aspects of the established value chain from component to the housed product, the push towards maximum integration limits the manufacturing options towards technology contenders with the most advanced integration technologies – typically highly vertically integrated manufacturers. Yole has broken down one of current hallmark products and identified the functional integration to be as densely packed as to validate the definition of a SiP (see [15]).

If this perspective is adopted, the acronym “SiP” may become a self-referring description for highly integrated functions, leveraging:

- Highly integrated electronic functionalities (including electronic-only SiP components – level 1);
- Miniaturized integration of non-electronic functionalities (i.e. sensors, actuators – level 1);
- With contained functionality of the entire system’s internal and external functions (embedded system – level 2);
- Fully contained for immediate integration into the system housing (level 3).

This example strengthens the roadmap depicted in Figure 4.

Going beyond this module form factor, the scope of the SiP concept may expand to envelop the entire system, i.e., as soon as full functionality is provided by one service provider within the value chain, to leverage all needed technologies for system creation. An example for this could be current next-generation smart cards with a wireless interface for communication and power, crypto-controllers, and biometrics (sensor and controller) functions, as shown in Figure 19.

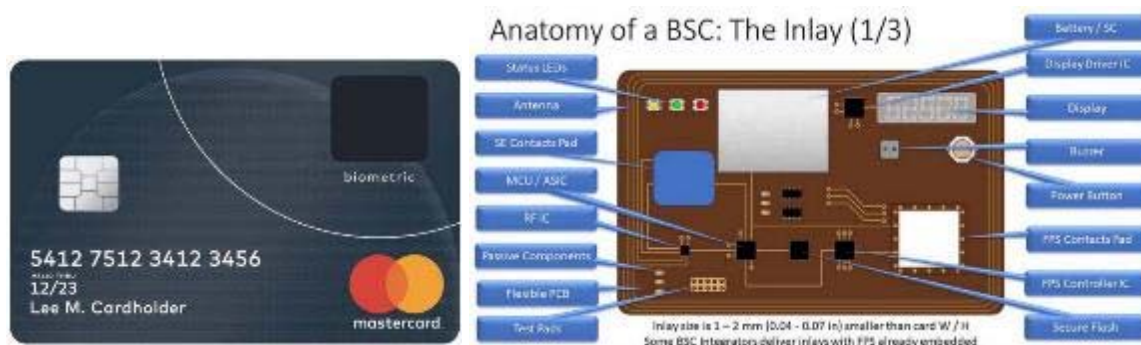


Figure 19: Biometry (fingerprint) enhanced pay-card [16]

In such a context, precision assembly as well as flex-fold assembly, micropart assembly and handling of batteries would also become part of the subsequent value chain for SiP assembly, meaning that the current distinction between OSAT, EMS and OEM, blurring for many years, is now reflected also in the packaging family.

### 1.3.7 Precision Assembly

In addition to the Packaging Toolbox details described in 1.1 to 1.3.6, many of the concepts rely on **Precision Assembly and Processing**, since with a growing number of parts in a SiP/module, this aspect becomes mission critical.

Generally speaking, assembly had been the domain of EMS or OEM service providers, who are challenged to move down the supply chain towards the BEOL. With the advent of SiP, there is an observed shift in the value chain, where – for example for FO-xLP or passive components – precision assembly with tight tolerances and critical process parameter compliance has become a domain of IDMs and OSATs who have started to move up the value chain towards the system. For example, in order to provide a FO-xLP SiP, the manufacturer needs to accurately place the chipset and the passive components in their positions, allowing for a suitable interconnect technology to be used (eg, RDL-first), or collective wiring within tight tolerances (RDL-last) to maximize the achievable routing density.

With Chip Embedding Technology, processing parameters need to be suitable not only for the components processed, but must anticipate as well the subsequent process steps such as reflow soldering or snap-in interconnects to the next packaging level.

This trend set by the advent of SiP is expected to impact the traditional supply chain, with technology leaders in packaging (even foundries) expanding their domain towards hitherto shared workflows.

## 2. Challenges for the Toolbox

The recent acceptance of SiP in the market, with its capability to fulfil the needs of challenging applications, has led to the situation that not only electrical systems are implementing SiP cases, but many other domains (optical, mechanical, biochem) are embracing the SiP concept. While currently this can be addressed over a wide variety of “more than Moore” approaches, roadmaps and application requirements (e.g. reliability, EDA integration, process compatibility) are typically not aligned for a straightforward integration but need to be engineered for each individual requirement. This situation will become more pronounced during the next years of tech evolution, as more application diversity, with their individual roadmap visions and complexity, will call upon SiP to fulfill their needs.

Tables 4 summarizes some key findings for future challenges, in comparison to the state of the art, derived from the earlier individual sections on interconnect (a) and package concept (b).

Table 4a: Future Challenges seen from a toolbox perspective (Interconnect)

Technology Toolbox expectations	chipsize	chip I/O magnitude	chip pitch	chip count	max. # of domains served
	[mm]	[10s, 100s, 1000s]	[μm]	[#]	[electrical, optical, mechanical, biochem, ...]
Wirebonding	<40mm	100s	15	8	4
FlipChip Bonding	<40mm	1000s	10	8 (TSV stack)	4
RDL Redistribution Layer	<40mm	100s	5	3	2
TxV's	n/a	1000s	25	2	2
Solder Ball	n/a	1000s	10	2	1
Hybrid Bonding Interconnect	<25mm	1000s	1	10 (TSV stack)	4
suitable chip size: Interconnect technology already demonstrated					
chip I/O magnitude: capability derived from technical feasibility, e.g. "100s" covers anything up to 999 I/Os					
feasible chip pitch: derived from currently demonstrated implementations					
served chip count: derived from currently demonstrated implementations, including different chip technologies, stack or side-by-side concept					
domains served: derived from currently demonstrated implementations, merging electrical signal, optical signal, MEMS sensing and actuation, RF wireless and power					

Table 4b: Future Challenges seen from a toolbox perspective (Package Architecture)

Technology Toolbox expectations	chipsize	chip I/O magnitude	chip pitch	chip count	max. # of domains served
	[mm]	[10s, 100s, 1000s]	[μm]	[#]	[electrical, optical, mechanical, biochem, ...]
Package on Package	>30mm	100s	depending on internal routing	6	4
Embedded Chip Technology	<40mm	1000s	25	6	3
FO-W/PLP	<40mm	1000s	2	4	4
Precision Assembly and Processing	<0,05mm, >40mm	10...1000s	10	>10	>3
suitable chip size: Interconnect technology already demonstrated					
chip I/O magnitude: capability derived from technical feasibility, e.g. "100s" covers anything up to 999 I/Os					
feasible chip pitch: derived from currently demonstrated implementations					
served chip count: derived from currently demonstrated implementations, including different chip technologies, stack or side-by-side concept					
domains served: derived from currently demonstrated implementations, merging electrical signal, optical signal, MEMS sensing and actuation, RF wireless and power					

The omnipresent imperative to *reduce pad-to-pad distance and pad size* will pose a continuing challenge, as was seen in the past. Notably, some technology approaches find it easier than others to address this challenge (e.g. flip chip with micro-bumps, hybrid bonding interconnects) while other approaches (e.g. FO-xLP and wirebond) will see challenges due to the process constraint itself or the exponential increase in new infrastructure cost to go to smaller feature sizes (i.e. from ~10s of μm to ~1μm).

All tools, however, will need to deal with growing chip sizes to cover the larger functionalities offered by the chips, and thus *larger numbers of I/O* to be routed between the SiP's components. At this point, novel components such as IPD's or integrated energy storage do not increase the challenge for the evolutionary aspects of packaging,

but instead do add challenges to the processing itself – e.g. with thermal constraints limiting the package stress effect on a component’s performance.

Another aspect unique to SiP is the “more than Moore” perspective offered. In addition to the electrical domain, *multiple additional functionalities* (e.g. non-electronic sensing, optical, even bio-chemical) will emerge as SiP functionalities with inherent multi-domain data fusion, driven by Internet-of-Things (IoT) and edge computing. Here, individualization needs of the SiP implementation will likely prevent any standard approach, but the technology toolbox will be open for this kind of diversification.

Opportunities to push electronics packaging via this toolbox approach are challenging, since the vast range of sensors will not allow immediate ultraminiature integration – so in order to achieve a small, flat target form factor of the entire SiP’s functionality, electronics will need to be integrated with the best-of-class technologies.

This has implications for the choice of toolbox technologies for such multi-domain SiPs – e.g. due to the required loop geometry, wirebonding can only achieve a certain minimum thickness. Fan-out technologies will be challenged to deal with warp and controlled mold material flow in ultrathin scenarios. Since over the next five years more product-driven challenges than technology-provided solutions (for one given process) exist, we can anticipate that there will be a healthy and dynamic mix of technologies within an SiP package.

Tables 4a and b will be – in the evolution of fine-line structuring on any kind of substrate, e.g. *improved lithography* tools, *improved resists* and *electrodeposition (ED) technologies* – benefitting from past developments derived from the semiconductor industry. However, this approach will put an emphasis on process speed and cost benefits over the extreme precision required by the current generation of semiconductors.

The *next generation of wirebonds* will make use of novel materials with improved mechanical strength and process properties, which allow the achievement of finer pitches.

*Flip chip assembly with finer pitch* may need to move away from melting solder bumps and toward copper pillar bumps with, for example, reactive contacts to ensure similar process speeds as are currently established for mass reflow processes, but at much smaller pitch.

*Thin chips* with currently 30 to 50µm thickness *will eventually be thinned down to 15µm* in order to comply with future thinner dielectric layers used for the embedded-chip packages. This will allow stacking more chips per volume and maximizing functionality. In order to achieve the routing density necessary for connecting the increased number of IOs, not only lines/spaces need to be decreased but also the size of vias and alignment precision of blind- and through-via fabrication will have to improve. Laser processes that dynamically adapt to die shifts and tolerances will enable this future.

The main challenge at the moment for *panel integration* (section 1.3.4) is – aside from technology evolution set to overcome die-shift, warpage, massive die number assembly, multi-layer RDL on Panel – the missing standardization on panel formats. SEMI has now started an initiative on the standardization topic. After conducting a costumer survey on preferred panels sizes, a task force has been established working on a first proposal of a standard.

However, an easy upscaling of technology when moving from wafer-level to panel-level is not possible. *Materials, equipment and processes* have to be further developed or at least adapted. Consider the carrier material selection for a chip-first approach: not only the thermo-mechanical behavior but also properties such as weight and stability need to be considered. Pick-and-place assembly on carrier is independent from wafer or panel formats and causes a bottleneck. Here new equipment or even *new approaches for high-speed but also high-accuracy assembly* are required. Compression molding is typically used for chip embedding and to form the reconfigured wafer or panel. Liquid, granular and sheet-type molding compounds are available. All allow chip embedding with pros and cons in cost, processability and also cleanroom compatibility. For redistribution layer formation, a large variety of lithography tools and dielectric material options exist. For dielectrics, photosensitive as well as non-photosensitive or liquid versus dry-film materials can be considered. Mask-based lithography such as stepper technology, as well as maskless-based tools such as laser direct imaging (LDI), are available for panel sizes. Both offer different capabilities and strategies to overcome challenges such as die placement accuracy and die shift after molding. Finally, solutions for grinding, balling and singulation are needed. Manual and *especially automated handling of molded large panels* including their storage and transport is still an open topic, since until now only custom-designed solutions exist. However, there are many process flow options applicable to different applications. But still the question on “where is the sweet spot” taking performance, yield, cost and panel size into account has not yet been answered.

Aside from the grand challenges, technological details in each aspect may prove critical showstoppers, e.g. Cu low-k at fine pitch, and should not be neglected. In many areas, future development will be necessary.



In summary, while each subset of technologies made available by the toolbox will offer solutions to individual challenges, the success of a given implementation will rely not only on technical feasibility, but also on the cost for implementation, future material development, and preferred choice of architecture (i.e., a platform for a target application). Table 5 summarizes some of the considerations.

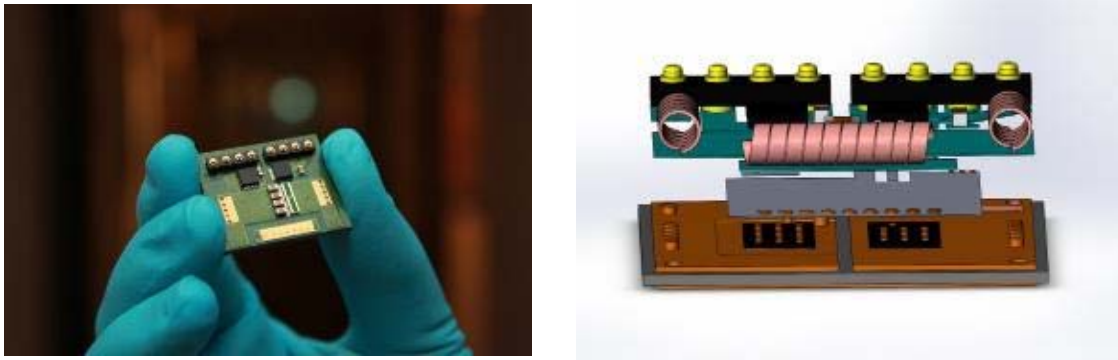
*Table 5: Some key influential parameters for the adoption of a given innovation for future SiP.  
("Expected Impact" is based on expert assessment from the TWG group's perspective.)*

#	Challenge	Influential Factors	Expected Impact Value (1 lowest, 10 highest)
1	Materials	Cost, Properties, Architectural Implications	5
2	Cost of SiP	Cost vs. Benefit	6
3	Technical Feasibility	Future-proof, cost, manufacturing infrastructure, scalability	7
4	Platform Requirement	Application driven, manufacturing infrastructure	8
5	Performance	Minimum size, maximum functionalities	2

### ***Application Perspective and Market Needs***

While obvious technological challenges persist in the evolution of SiP, the requirements and challenges are expected to come from the large diversity of applications. Some highlight applications, with their current state-of-the-art implementation into SiP (or at least miniature system), are provided in this section, with trends addressing the challenge of SiP integration.

**Power Functionalities:** With the introduction of Wide-Band-Gap (WBG) power semiconductors such as silicon carbide (SiC) and gallium-nitride (GaN), power systems in a package are becoming available (Figure 20). Including part of the driver and the DC-link in the package, plus an output inductor and/or a transformer, helps to make full use of the possibilities offered by very fast-switching devices and thus high switching frequencies. To enable fast switching (at up to 500 kHz) and yet keep losses and EMI issues small, packages with very low and well-known parasitic characteristics are needed. Besides the electrical package design, thermal management is another big challenge. High power densities like 200 W/cm<sup>3</sup> demand a careful construction of thermal paths, EMI compatible design and careful materials selection.



*Figure 20: Example for an EMI-optimized SiC package with part of the driver and the DC-link included.  
[courtesy Fraunhofer IZM]*

**MEMS Functionalities:** Autonomous driving, smart homes and buildings are some of the main drivers for sensor modules. MEMS and sensor packaging in general entails many challenges including stress sensitivity, open access to sensor surfaces, and material and process compatibility to the sensing functionality. For multi-sensor and heterogeneous integration, these challenges gain even more importance as different demands come together. These demands strongly move MEMS packaging solutions from the traditional wire-bonding (WB) package to a wafer-level package (WLP). When MEMS packaging evolves into 3D WLP, the key approach of vertical integration to replace traditional WB interconnections is the through-silicon-via (TSV) technology.

As recent examples, a MEMS gyroscope and accelerometer package including a signal processing ASIC from BOSCH used in the Apple Watch 3 is shown in Figure 21, featuring a fully contained solution for inertial navigation in a 2.5x3x0.6mm package using wirebonding on active circuitry and an HDI substrate for an LGA-type overmolded package.



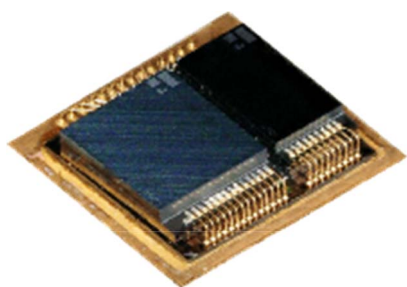


Figure 21: BOSCH SPI8382 IMU [courtesy of SystemPlus, France]

Another innovative approach leveraging multiple interconnect technologies from the above toolbox is given in Figure 22, featuring a 6-axis accelerometer, which is composed of a MEMS die stacked on top of the ASIC die, with both dies connected through gold wire. Additionally, it's worth mentioning that the output was routed through TSVs inside the ASIC die with solder balls as terminal attachments. In this way unsurpassed miniaturization is achieved while maintaining flexibility with respect to ASIC and MEMS dimensions.

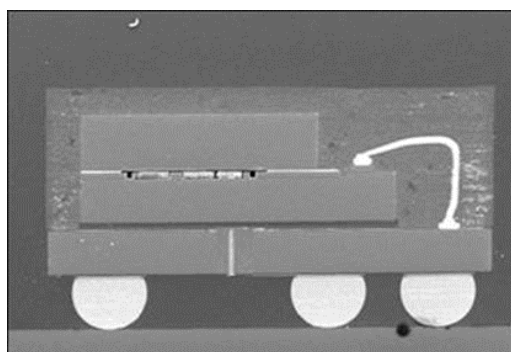
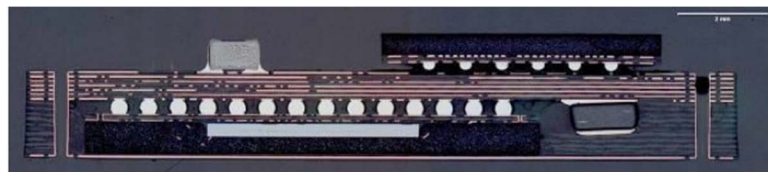


Figure 22: MEMS based accelerometer system with TSV, WL-overmold and stack wirebond

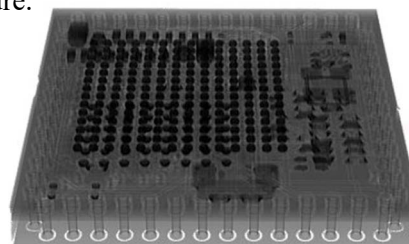
**Complex IoT devices, Edge Computing:** Devices forming the “internet of things” consist not only of a processor with an IP stack and RF interface, but also a need for sensing and interacting with the ambient. Currently, devices like IoT cameras, smart speakers, and smart home appliances are dedicated products on their own, but are due to be integrated into everyday appliances – this means that OEMs will ask for added functionalities such as power outlet integration, lamp/lighting integration, and interactive devices in the medical field. One attractive example, showing image sensors integrated with DSP/ $\mu$ C solutions for autonomous vehicles, makes use of embedded chip technology (chip in package, CET) and adds the camera chip/optics to complement the system – as small as a quarter dollar (Figure 23). In this example, challenges faced include:

- Wiring density in 3D
- Thermal management
- COTS (custom off-the-shelf) and bare-die co-assembly and processing
- Multi-domain testing challenges

This example neatly showcases how future SiP applications will push the envelope not only on the technology side, but also for adjacent tech fields, sourcing and manufacturing infrastructure.



cross-section of embedded module



x-ray image of singulated modules

Figure 23: Fully integrated camera/DSP solution as IoT security device [courtesy TecVenture GmbH]

A fully silicon integration strategy may be a way for applications to target for maximum integration and performance (Figure 24).

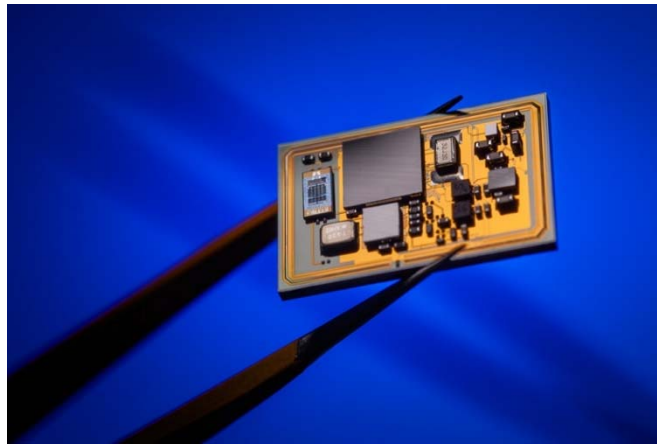


Figure 24: Fully integrated IoT device. [courtesy TU Berlin]

### Artificial Intelligence Integration into SiP:

Artificial Intelligence (AI) is currently associated with cloud services running large databases and supercomputers. With Nvidia, Intel, AMD and Qualcomm pushing into that area with number-crunching GPU architectures, it is only a matter of time until the trend towards “mobile AI” (i.e. like Google’s TPU) becomes a mainstream technology and will offer specific challenges to a SiP integration. Currently, car makers and drone manufacturers look for AI to overcome the problem that, in a dynamically changing surrounding, hard-coded routines cannot ensure proper operation. AI chip sets initiated from these application areas will expand into everyday devices. As these “brains” will have to be ultramobile, miniature and with dedicated sensor interfaces for their specific ambient, a SiP implementation may allow AI to work better, faster and with lower power requirements than a non-dedicated approach using standard components built together in a joint housing. Thus, from the point of view of the SiP toolbox, TSV chip stacks in combination with flip chip and embedded chip technology, merging memory cubes with multiple chip technologies (CMOS, post-CMOS) and chip architectures (CPU, NPU, etc) will serve as the packaging tools of choice, with variations in the combination growing with the application diversity (Figures 25 a and b).

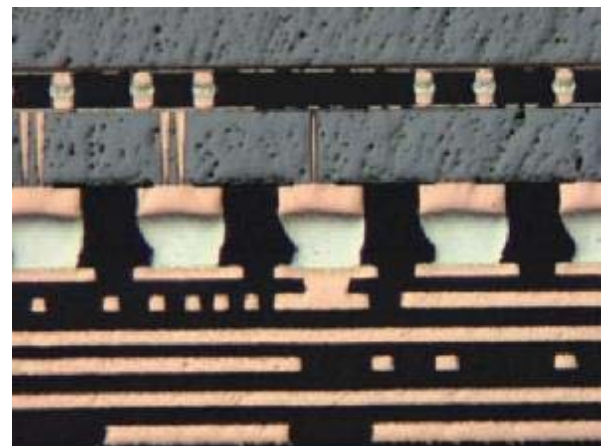
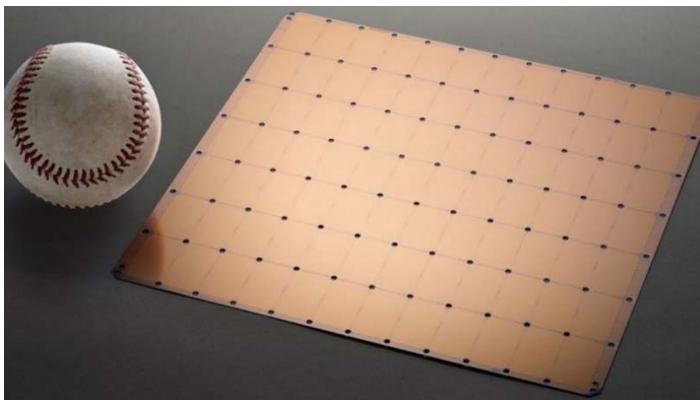


Figure 25: (a) AI engine built at wafer level using advanced RDL and integration techniques [courtesy CEREBRAS, inc.] and (b) laminate package integration of NVIDIA’s Pascal SiP Package suitable for next-gen AI processors [17]

**Modules:** Applications using an SiP as a highly functional component – as described in the previous setting – are becoming mainstream. However, identical integration pathways and system integration depth may lead to the SiP serving as the main (and only) functional part in the system itself. Here, the SiP combines microprocessor, memory, sensors, RF and even other SiP components into a functional unit with a defined set of interface elements – but instead being used as a highly functional component, only some periphery items (e.g. battery, display) are added for the full product. Modules, as described as part of the Packaging Toolbox in 1.3.7, are simultaneously pushing the envelope for applications and thus need to be looked at also from this perspective. For example, as depicted in Figure 26, the distinction between the level 1, level 2 and even level 3 packaging hierarchies are blurred in the example of a smart watch, showing the high specificity a SiP can offer for a given product.

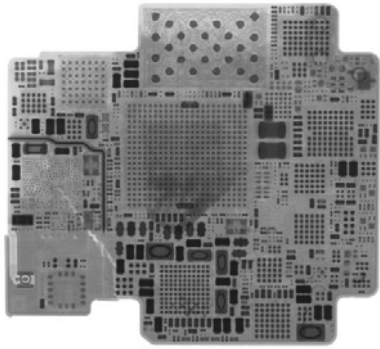


Figure 26: Apple Watch Gen 7 as an example for a module type of SiP (courtesy iFixit 2021)

## Main Challenges from the Application Perspective towards SiP Adoption

### *Direct application-related challenges*

#### **1. Functionality will increase**

Due to the growing level of diverse functionalities, co-design becomes both more relevant as well as more difficult; functionalities may have an influence on each other.

#### **2. Non-electronics will become a major part of functions**

Co-Design of non-electronic functionalities (i.e. gas or fluidic channels, optical elements) which in the past had been done by separate stakeholders for large systems, now have to be integrated by manufacturers earlier in the value chain. Here, neither adequate EDA tools nor engineering experience is available.

#### **3. Assembly processes will change**

The challenge in SiP manufacturing – especially for multi-domain (more than Moore) functionalities – lies in the assembly process itself. Touted as the next-level multi-chip module (MCM) assembly technology, it requires the ability to assemble and interconnect several die not only horizontally (with die placed side by side), but vertically as well (wherein several die are placed on top of each other), while taking due consideration to specific challenges like signal integrity, hardware built-in security features and media access.

#### **4. Reliability requirements have to be adapted seamlessly to application needs**

New and hitherto unaddressed reliability challenges as for automotive (autonomous vehicles offering Mobility as a Service), aerospace (e.g. drone delivery), and satellite (microsatellites with unprecedented performance) will drive the technology and materials evolution, calling for a close interaction between service providers (who will take the role of the end-user), product manufacturers (who will be more and more driven by services) and technology providers (who need to know earlier about the challenges their implementations will face). While there are some clear trends for future customer needs, such as for AI and the mobile revolution, business models of service providers will also have an influence on the choice of a target implementation for SiP.

Current reliability standards adhere to today's application-oriented environmental and operational challenges. Future applications may require a drastically different approach. While current automotive scenarios need to consider multiple on-off cycles under various circumstances, future autonomous always-on mobility services will operate a car 24/7 without significant temperature changes, but under varied power loads and long-term exposure to contaminants. Medical devices will not only be used for a span of years, but may need to maintain their operation from birth to death of a human, asking for 80+ years of proven reliability. New power-generation schemes (decentralized, as for offshore wind, solar farms) pose substantial opportunities for the electronics industry, but – as critical infrastructure – become extremely sensitive to reliability issues for their diverse fields of deployment.

### **Materials**

#### **5. Materials improvements are needed**

While the electronics industry and the beforementioned toolbox build on evolutionary improvements of the materials (i.e. Al->Au->Cu->CuPd wires, nano-filled epoxies, ...), novel materials may change significantly the impact factor indicated in Table 3, shifting the favor for a given platform completely and thus upending established industries. This has been observed with materials evolutions (e.g. standard molded packages giving way to high-density multi-chip modules due to high-flow materials) and will be more difficult to deal with by industry if disruptive innovations are adopted. For example, new materials will enable the package to provide a functionality on its own, such as compensating for thermal mismatches, managing thermal transients, addressing reliability aspects (e.g. self-

repair and failure indication) or allowing high-performance individual packages to be printed on demand from 3D print materials and technology.

### ***Physics-related challenges***

#### **6. Thermal Management becomes a mainstream challenge**

Heat dissipation is another challenge in the development of SiPs. Taking chips off-the-shelf and using them in SiPs can result in junction temperatures beyond their specification, since these chips were designed to dissipate heat through their own packages. Crowding them together inside a SiP can generate enough heat to be of major concern in the field. Pursuing the path towards compressing more functions in a smaller volume, thermal dissipation and heat management become thus a stronger issue. This is especially relevant in the context of the trend to put SiPs in the core of mobile devices, where traditional heat management concepts (heat pipes, ducts, heavy heat sinks) fail to work. This is further addressed in Chapter 20.

#### **7. Empirics/statistics is needed in reliability assessment for a deeper understanding**

While previous aspects of reliability focused on changes in operating conditions, reliability considerations also need to shift their basis from the current empirical and statistically assessed prediction towards a physics-of-failure related model, which anticipates the core reliability affecting parameters encountered in an SiP. Since simple approaches for geometry and material combinations will not adequately reflect the situation that a structure experiences under operation, a thorough understanding of the root causes for failures and the use of computer-assisted modeling will be required to deal with the diversity encountered in future SiPs.

#### **8. Form-factor challenges will persist**

SiP form factors will diversify with the need to shrink well established functionalities (e.g. accelerometers and intelligent micro-actuators), but also growing in size to address significantly higher complexity levels as well as intrinsic application needs (camera systems, autonomous processing of large data amounts, ...). SiP modules will take over the mainstream from single-chip BGAs. Although integration technologies will limit the obtainable form factor to the maximum size of the largest component itself, cost and performance considerations will dominate this aspect beyond the maximum obtainable, and toward a “system-level optimum”.

#### **9. Signal integrity becomes critical**

Currently, signals on a package are more or less governed by the clock frequency of the microcontroller used. While this is true for single-chip packages, a SiP that include RF radio and power-control components critically needs an integrated design flow that anticipates such factors as power surges to the transceiver and microcontroller. Consideration of signals will not necessarily relate only to electrical signals; optical communications in the package, or fluidic transfer bearing the “target signal”, may also be affected and in turn may affect the system’s function if not properly addressed early in the SiP design phase.

#### **10. Power increase will be omnipresent**

The need for increasing power – both in “smart power devices” (logic and power combined) but also with devices merging stronger computing power with additional functions like sensing – pushes technologies to their limits, as conductor line width and thickness are both governed by the current-carrying capacity as well as routing-density needs.

In addition to these changes and challenges, cross-cutting aspects will also have to be addressed to enable future novel products.

#### **11. Testing and functional verification become more difficult**

SiP manufacturing not only offers assembly challenges, but test challenges as well (see chapter 17 on Test). SiPs combine microelectromechanical systems, optoelectronic devices, various sensors, linear and digital circuits, etc., which were built on different wafer fab process technologies and therefore have varying excitation requirements. Add to this the fact that each of these system blocks requires special test methods of its own. A test solution to meet the various test resources and methods required by a complex SiP can turn out to be expensive:

- Application-specific functions (includes mixed signal, media, etc.) can be complex and costly – currently best assigned to the end customer who knows the SiP functional requirements best, but may call for an intermediate level of testing in the value chain, challenging assembly partners to serve all needs because of limitations of an end-user in building up a non-value-generating function in the enterprise.
- Electrical, mechanical and thermal aspects need to be tested simultaneously and in interdependence.



- Currently, most tests are done step-by-step; future test equipment may need to offer modularity to address testing co-dependencies for a multitude of applications.
- Self-testing, including built-in self-test (BIST), may be a preferred solution for individual component performance, but will likely not allow for a joint testing of all functionalities comprising the SiP's function.

## 12. EDA-assisted co-design will become a necessity

Heterogeneous integration includes a mixture of more than one chip and different assembly technologies, which leads to significant increase in design complexity. This complexity can be handled properly only by an enhanced design environment and extensive use of electronic design automation (EDA). Just as the SiP design concept exploits modularization by putting best-in-class components of different, optimized technologies together, a SiP design system needs to be based on multi-dimensional modularization as well: Modularization in configuration (like assembly design kits), modularization in data exchange and data storage (standardized file formats, design databases and data management), and modularization in design environments (even across company boundaries). A comprehensive co-design flow approach for the overall design system allows staying independent from proprietary solutions of individual EDA vendors. Development of heterogeneously integrated systems also requires a heterogeneous, versatile design environment.

Speeding up the design flow can be achieved by introducing assembly design kits (ADKs), just like process design kits (PDKs) for chip technologies decades ago. A versatile co-design flow supports the configuration of several ADKs and PDKs for a complete chip-package-PCB design project (see Figure 27).

Such a development environment needs to enable and support various steps in chip-package-board co-design including connectivity (schematic) entry, concurrent layout design both in fully automated digital place-and-route as well as in full-custom manual style, assembly design rule checks (DRC), overall connectivity checks (layout-versus-schematic LVS even across chip, package, and PCB domain), and 3D model generation for subsequent package parasitic extraction and electro-magnetic and electro-thermal field simulation.

Besides the support of ADKs, a SiP co-design environment needs to be based on a modular approach for data exchange between the different EDA software tools of different vendors. It is impossible to align on only one tool suite of one EDA vendor within a chip-package-PCB co-design project: On the one hand, this is due to missing features; on the other hand it is due to the fact that several companies along the value chain need to cooperate tightly together, all having their own legacy in EDA tool setup and experience, which needs to be put in synergy to the benefit of the customer, ie using XML-based schemes, enabling cross boundary DRCs and LVS validation. In addition, there is a clear need to improve and further automate the link between 2.5D EDA tools and true 3D mechanical CAD tools.

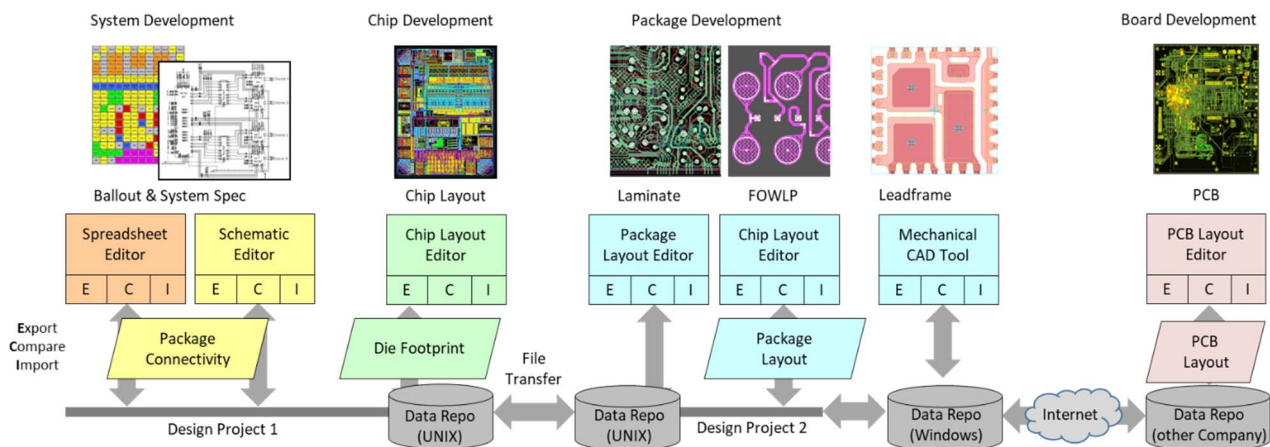


Figure 27: Modular data exchange between distributed design teams working with a co-design backbone [18]

Additional details are given in Chapter 13: Co-Design for Heterogeneous Integration.

## 13. WEEE and other environmental factors will remain in effect

Laws to protect the environment have focused their perspective and implementation possibilities according to existing value chains. This has led to the situation that current devices, which are not yet classifiable as SiP but more as “complex systems”, are neither re-usable, repairable, or re-cyclable without tremendous effort. With highly integrated multi-domain-encompassing SiPs, the situation will deteriorate. One can envision that multiple contradictory laws affecting a multi-domain SiP will require compliance.



#### **14. Inter-Industry Communication**

Traditionally, a company with an application reaches out to technology providers to assess which technologies might suit their requirements best. This approach originates from the diversified supply chain and the traditional buyer-seller role-sharing. With SiP, the situation is both more complex as well as more satisfying – the application perspectives can be addressed early with the supply chain, and optimally served. However, this emphasizes the need to communicate at an early stage with the SiP integrator. This in turn has a strong impact on the way design teams from the application and the supply side need to interact, which as of today are still tied to traditional work-sharing routines.

#### **15. Standardization expected to focus on tool box instead of package type**

While SiPs – as for other technologies as well – will be driven by miniaturization needs, no standard approach will fit a unique customer's requirements. This is because no single functionality is offered (as for single-chip packaging), but a customer-specific application must be designed from a system perspective. However, some technologies lend themselves better than others to serve as a founding family with the capability to minimize NRE efforts and cost. Here, platform technologies may be useful to serve a majority of needs, but eventually a methodology that includes EDA capabilities to predict performance, cost, reliability and ecological footprint will be required. Even with platform-level standardization as a technology basis, an engineering model embracing this holistic approach will need to be part of a standardization process.

#### **16. Safety and Security (S&S) aspects need to be addressed at the level of design and manufacturing**

As of today, S&S aspects are delegated to the software running on the SiP's functionality. The hardware itself can serve with its physically unclonable features (PUF), with specific tamper proofing technologies designed into the hardware and Hardware-Software-CoDesign will pave the way to more secure, safer future products. See further discussion in Chapter 19.

#### **17. Cost reduction needs are omnipresent**

Complex systems in combination with many different options are inherently non-cost effective. With new platforms such as Fan Out Packaging or EMIB, the cost for SiPs serving new applications can be reduced while retaining functionality needs. But increased functions will also inherently come with an increase in cost; a balance must be struck to maximize functionality so the target application remains cost-effective, which may preclude a fully integrated SiP implementation in favor of a more modular approach. Since the cost target is ultimately defined by the end-user, the total partitioning of the system efficiency and cost will call for a closer cooperation between semiconductor manufacturers and the package (SiP) provider to meet these goals, e.g. use of novel approaches in the semiconductor sector may alleviate issues on the SiP integration side (for example, integrated power modules, where the advent of SiG and GaN have significantly reduced the size and properties of passive components, making small footprint SiP possible). Notably, customer requirements and cost-reduction needs thus will provide additional issues to be considered, while materials innovations and platform concepts may ease issues which seem to pose significant hurdles for technology and application evolution.

Table 7 provides a high-level synopsis of the foreseeable challenges outlined above, leading toward a SiP future.

Table 7: Key Challenges for the adoption of SiP in the mass market

	Challenge	State of the Art	Future Perspective
<b>Application Related</b>			
1	Functionality Increase	Single domain functionality	Multi domain functionality
2	Non-electric functions	Separate SiP approach, separated value chain segment	Integrated in one flow of value chain creation
3	Assembly	Single technology use	Choice from a technology menu built from a compatible tool box
4	Reliability	Standards derived from “typical applications” and adapted to actual use case	Novel applications driven by new business models may render current standards obsolete
<b>Material Related</b>			
5	Material	Material evolution driven by integration requirements (e.g. high flow epoxies, CuPd wire)	Material revolution driving integration, disrupting industries’ value chains
<b>Physics Related</b>			
6	Thermal Management	passive and active cooling built after simulation/validation assessment	Thermal-Electric and Mechanical Co- Design including the SiP integration site via CAD Tool
7	Reliability	Empirically derived statistical models	Physics of Failure Modeling
8	Form Factor	SiP design targeting maximum package efficiency limited by physical geometry	SiP design with as-needed efficiency, limited by cross-cutting aspects, interdependencies
9	Signal Integrity	Individual design and test	Building blocks for S.I.
10	Power requirements	<50W/cm <sup>3</sup>	200W/cm <sup>3</sup>
<b>Cross Cutting Aspects</b>			
11	Test	Single-domain testing, sequential test of multiple-domain functions	Simultaneous testing of multi-domain features to assess cross influences; testing specifically for target application
12	EDA assisted CoDesign	Different, incompatible EDA suites	EDA suites with a common referral language and APIs
13	WEEE	Electronics-only functionalities well addressed	Multi-domain functionalities difficult to address
14	Inter-Industry Communication	Applications reach out to select feasible technologies deemed suitable	Application needs to be matched with technology capabilities already in the conceptual phase
15	Standardization	Standards in formfactor of individual packages	Platform technology with interface to EDA tools (“VHDL for SiP”)
16	Security Aspects	No built-in security features	Depending on application, specific security features built into hardware may be needed
17	Cost Reduction	Cost challenges are addressed only on one level in the value chain	System level perspective to leverage synergies surpassing individual levels of value chain

**SiP and Module System Integration Technical Working Group Contributors**

Klaus Pressel (Infineon), Rolf Aschenbrenner (Fraunhofer IZM), Erik Jung (Fraunhofer IZM), Harrison Chang (ASE), Hannes Stahr (AT&S), Key Chung (SPIL), Peter Machiels (Philips), Thomas Zerna (TU Dresden), Hugo Pristauz (BESI), Paul Wesling (Roadmap editor)

**Glossary**

BGA	ball grid array	MCM	multi chip module
BIST	built in self test	MEMS	micro electro mechanical system
CET	chip embedding technology	MSL	moisture sensitivity level
CMOS	complementary metal oxide semiconductor	NRE	non recurring engineering
COTS	custom of the shelf	ODM	original device manufacturer
CSP	chip scale package	OEM	original equipment manufacturer
ED	electrodeposited	OSAT	outsources semiconductor assembly and test
EDA	electronic design automation	PoP	package on package
EMI	electromagnetic interference	PUF	physical uncloneable feature
EMS	electronic manufacturing service	QFP	quad flat package
eWLP	embedded wafer level package, <sup>TM</sup> Infineon	RDL	redistribution layer
FOPLP	fan out panel level package	RF	radio frequency
FOWLP	fan out wafer level package	SiC	silicon carbide
GaAs	gallium arsenide	SiGe	silicon germanium
GaN	gallium nitride	SiP	system in package
GPU	graphic processing unit	SiPiB	system in package in board
HAR	high aspect ratio	SiPoB	system in package on board
HDI PCB	high density integrated printed circuit board	SMD	surface mounted devices
IoT	internet of things	SO	small outline (package)
IPD	integrated passive devices	SoC	system on chip
KGD	known good die	TPU	tensor processing unit
LDI	laser direct imaging	TxV	through-x-via, with x being silicon, glass or polymers
LGA	land grid array	WLP	wafer level package

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