Ansys Redhawk-SC Electrothermal (CPA Feature) Training

V2020R2.0

CPS PE

Agenda

- CPA Introduction
- General setup and usage in Redhawk-SC Electrothermal

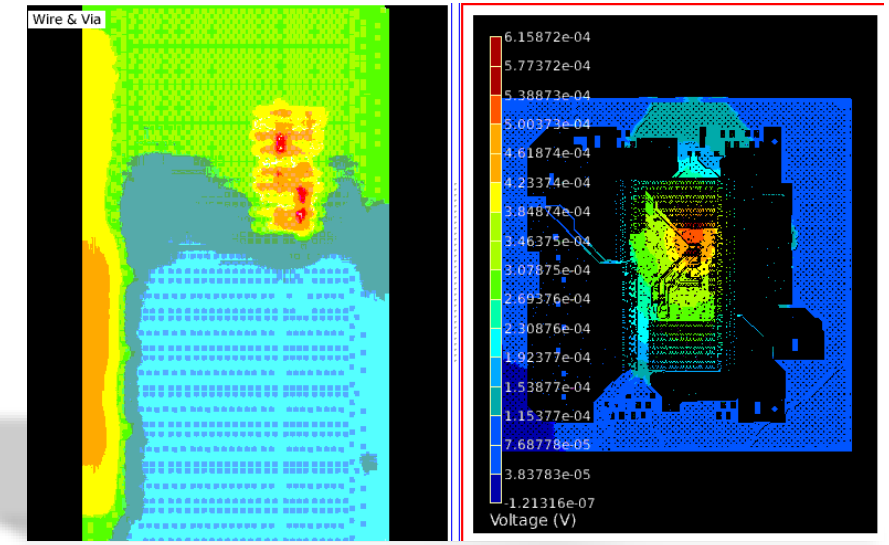
CPA overview

Chip-Package-Analysis

PKG Model Generation

DC-Cosim

Package Edits



Per-Bump RL Maps

HTML Reporting

Per-Bump Modeling

Impedance Plotting

CPA Solver Highlights

Technology

- Uses 3D FEM and 3D MoM solvers
- Similar to PSI and Q3D solvers
- Extracts RLCG netlist
- Frequency dependency
- Ground bounce preserved

Accuracy

- PDN analysis with FEM solver
- Select MoM solver (Q3D) for better accuracy
- Performance-Accuracy trade-off

System Flow and Usage

- Integrated into Ansys Chip tools
- Integrated into Ansys SIwave
- Very easy to use and detailed reports

Performance/Capacity

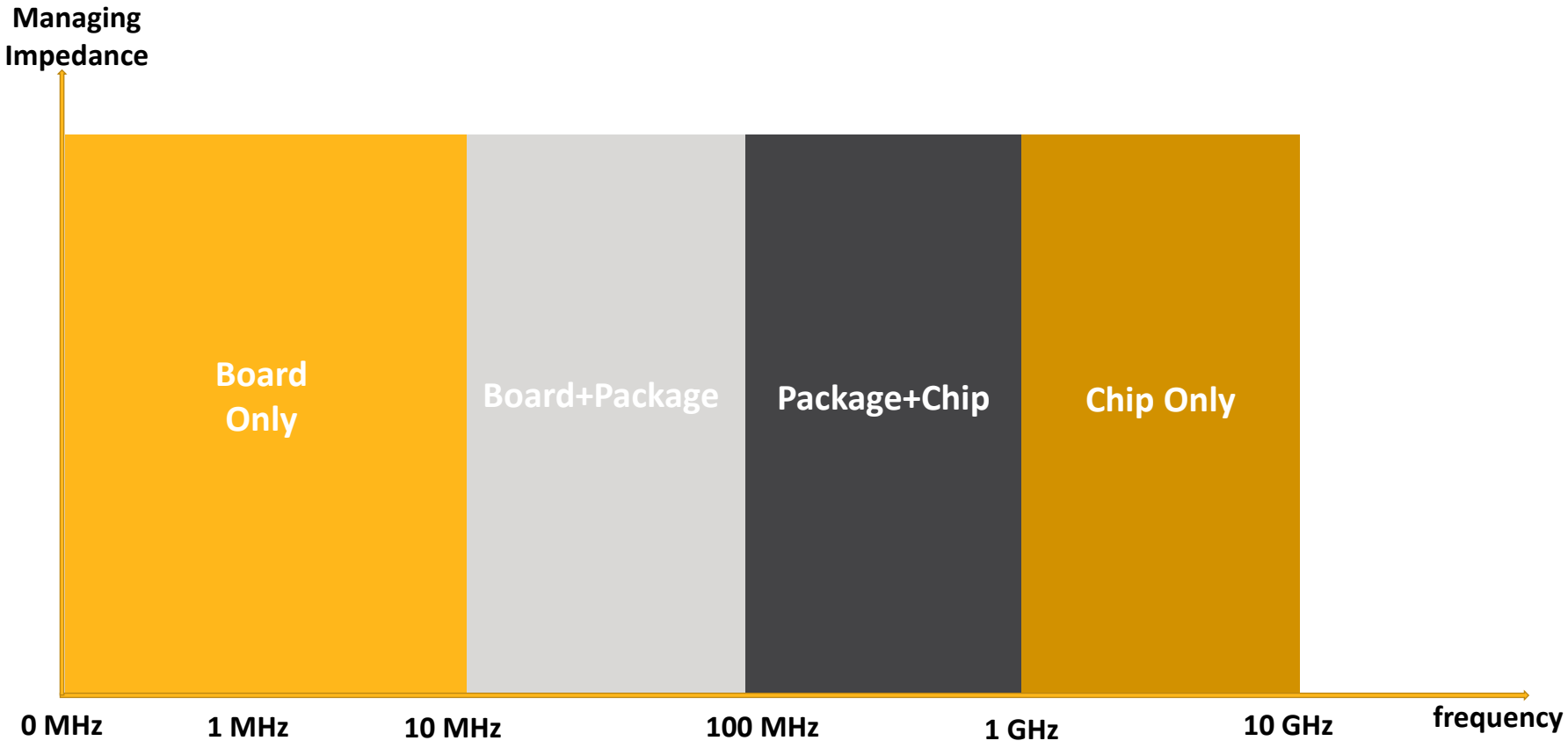
- Very high capacity FEM solver – full package and PCB structures – 10,000's of sources/sinks
- Fast extraction (minutes to a few hours – even for extremely large packages with over 30K bumps)

Applications

- Silicon Interposer and RDL
- Thru Silicon Via (TSVs) structures
- Packages, PCBs
- Supports decaps, and embedded components
- PI and SI analysis
- IBIS modeling
- Wideband Spice models

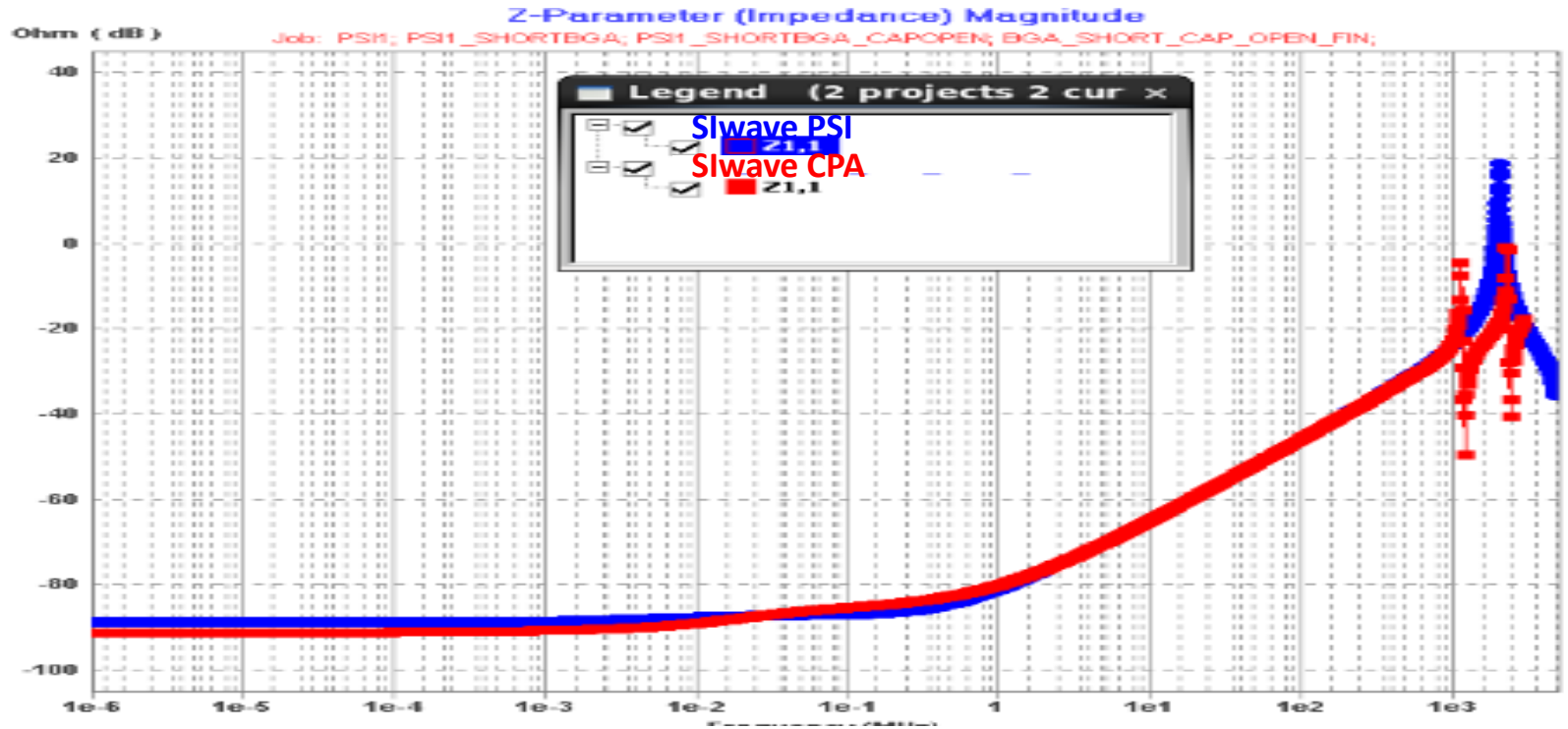
PDN(Power Delivery Network) vs. Frequency

- CPA and RedHawk Chip level extraction (up to 2GHz) is enough for PDN extraction



sourced by Power Integrity Modeling and Design for Semiconductors and Systems, p65, Madhavan Swaminathan and A.Ege Engin

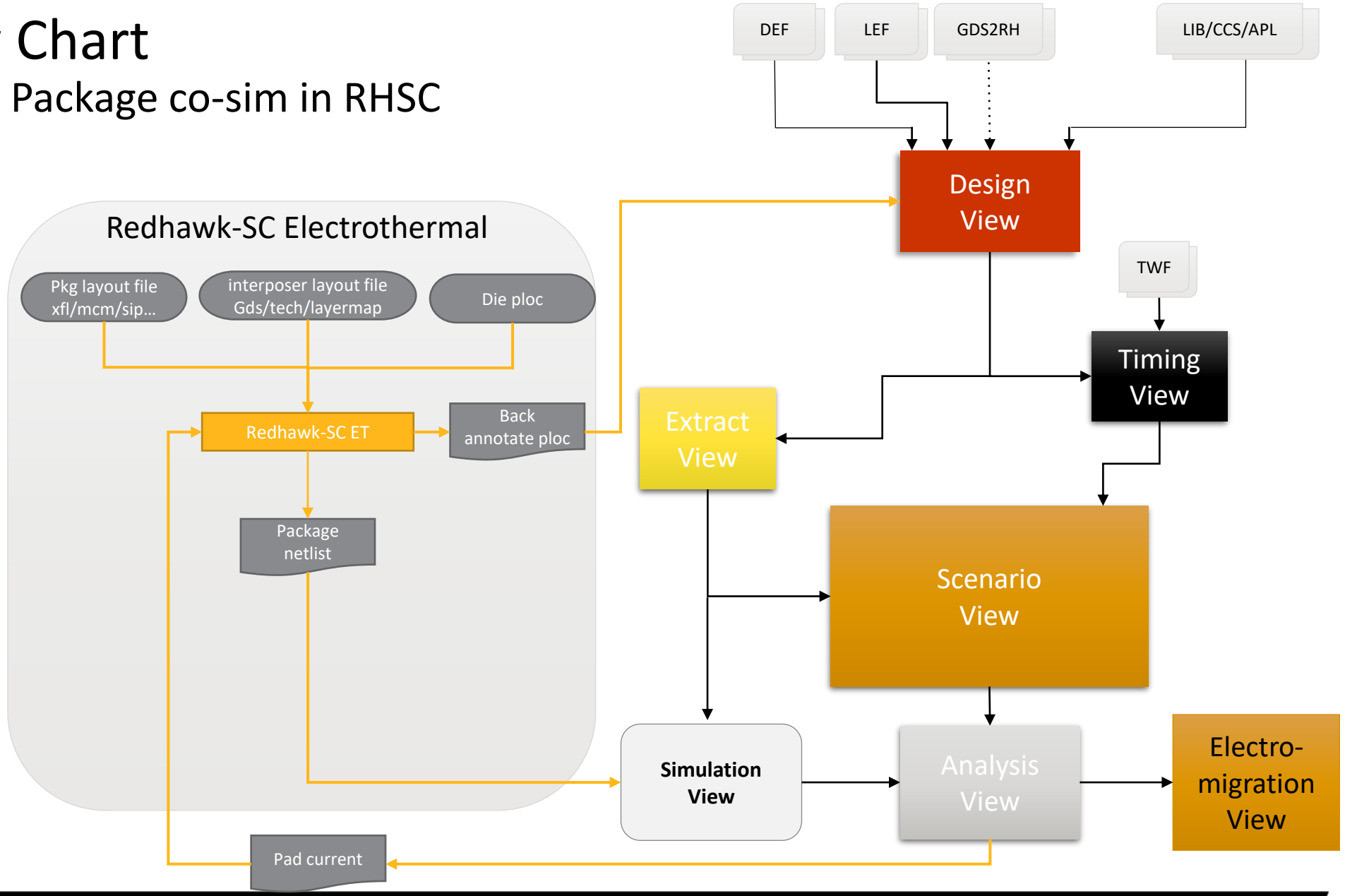
CPA vs. PSI Solver, Power Nets of Si Interposer



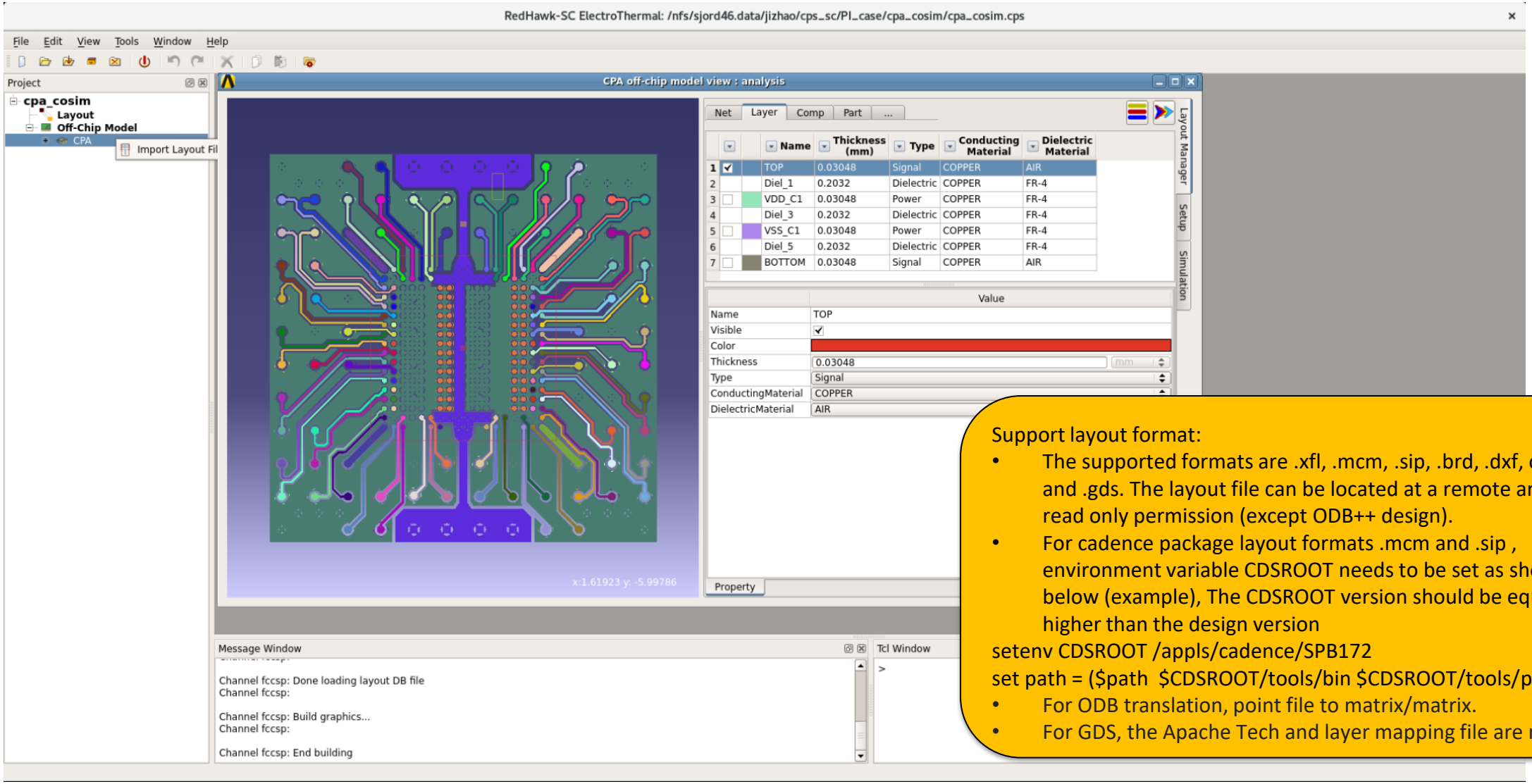
Solver Types	Parasitic Extraction Time vs. # of Power Networks			
	1 by 1 Grouping	10 x 10 Grouping	Per Pin (4000 ports)	HPC
CPA Solver	32.5 min.	40 min.	2 hrs. 30 min.	4 ea
PSI Solver	3 hrs. 8 min.	6 hrs.	N/A	32 ea

Flow Chart

Chip + Package co-sim in RHSC



GUI Overview



Support layout format:

- The supported formats are .xfl, .mcm, .sip, .brd, .dxf, odb++, and .gds. The layout file can be located at a remote area with read only permission (except ODB++ design).
- For cadence package layout formats .mcm and .sip , environment variable CDSROOT needs to be set as shown below (example), The CDSROOT version should be equal or higher than the design version

setenv CDSROOT /appls/cadence/SPB172

set path = ($path $CDSROOT/tools/bin $CDSROOT/tools/pcb/bin)

- For ODB translation, point file to matrix/matrix.
- For GDS, the Apache Tech and layer mapping file are needed.

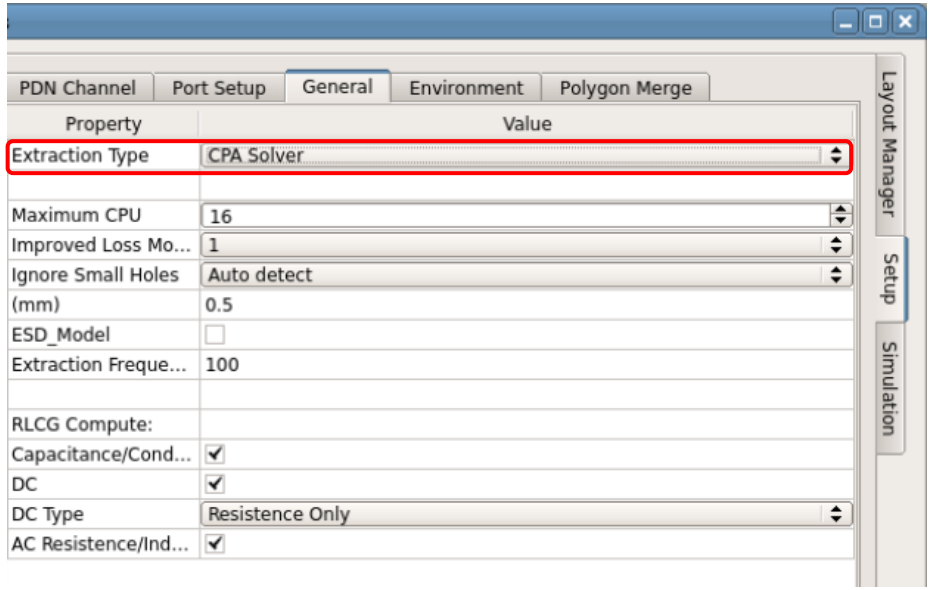
Solver Selection Recommendation

FEM CPA Solver

- No limit on number of sources and sinks
- Packages and PCBs with well defined ground planes
- Large scale PDN structures
- RDL, Silicon Interposers, TSVs
- No limit on number of Signal lines

MoM Q3D Solver

- Limited number of sources and sinks
- Leadframe designs
- Wirebond packages
- Smaller flip-chip designs
- SI analysis with “fewer” lines
- Can handle larger designs – based on memory/run time requirements

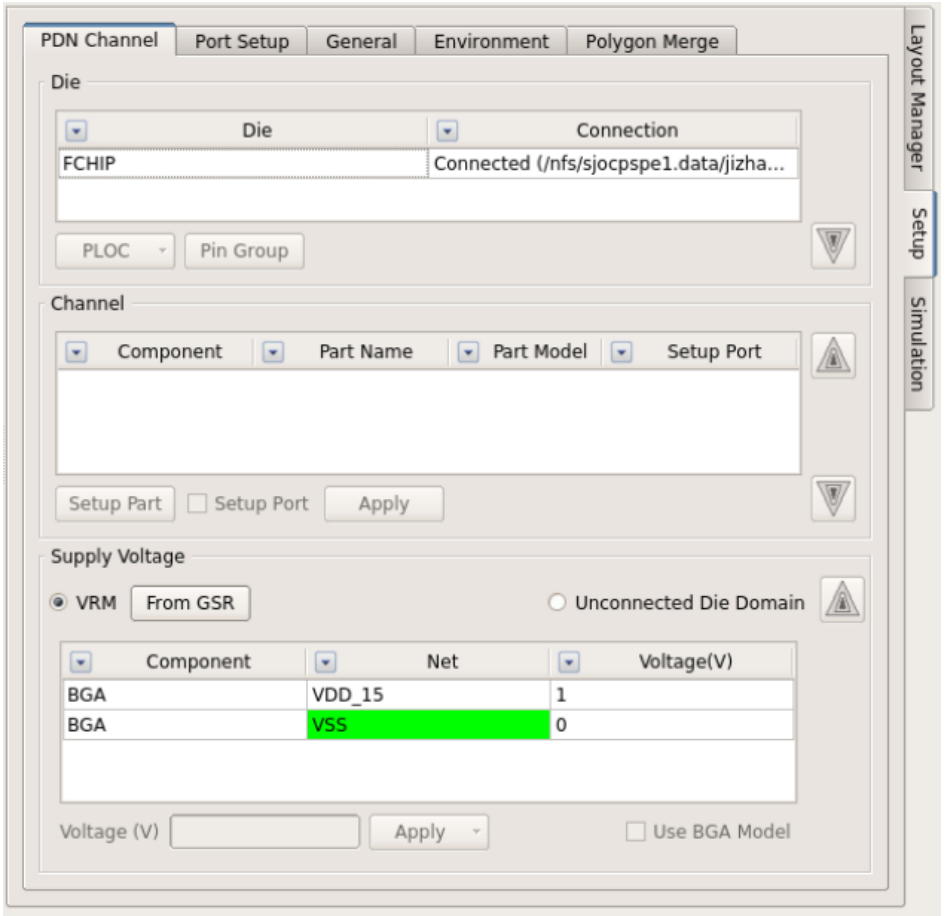


- ***We use FEM solver by default, unless Q3D solver is selected***
- ***For High-speed Signal net extraction, user can select PSI solver***

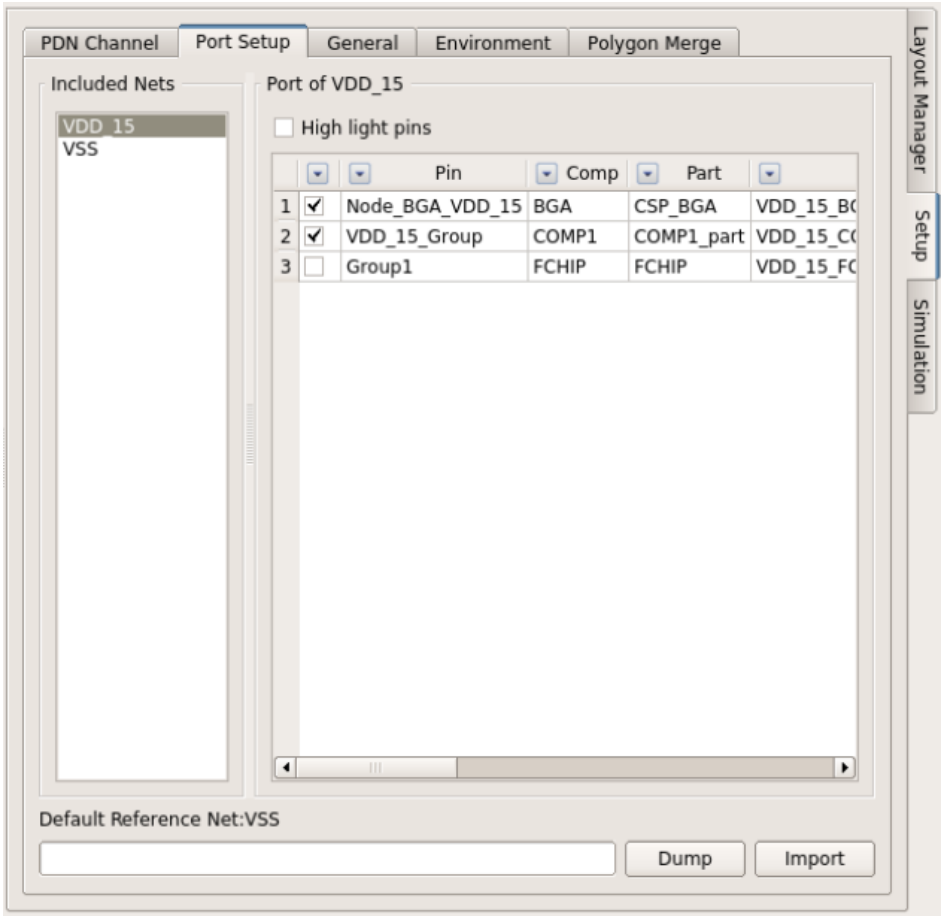
Note: Do not compare partial RLCG data between FEM and MoM solvers. They use different global reference. We can only compare Loop-RLCG results across solvers.

Channel (Port) Setup

Traditional CPA setup using PLOC

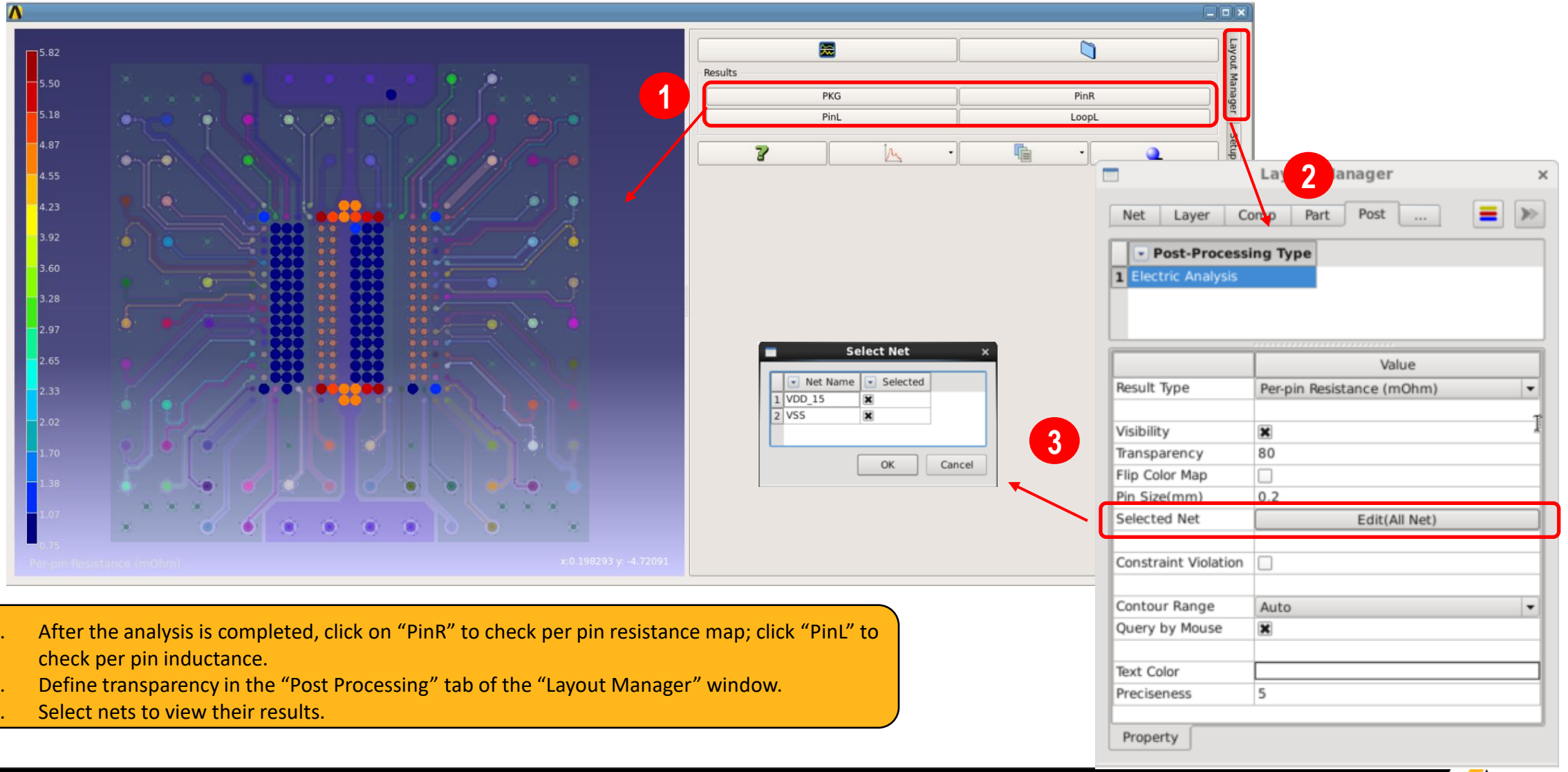


Port setup for multiple dies and PSI solver



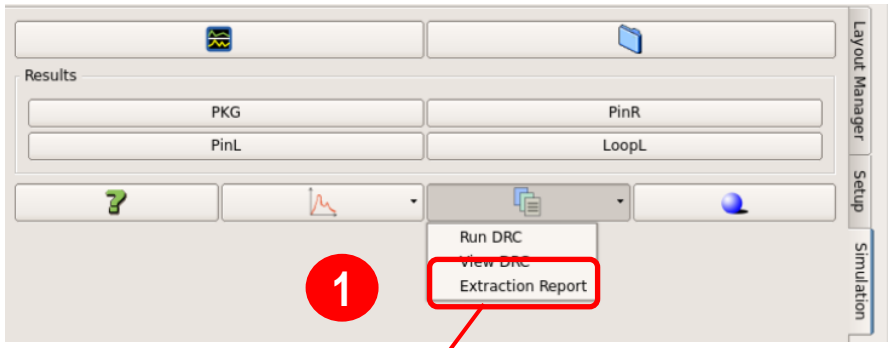
Note: If ploc has the grouping info in 6th column, CPA also can this pin grouping to do extraction.

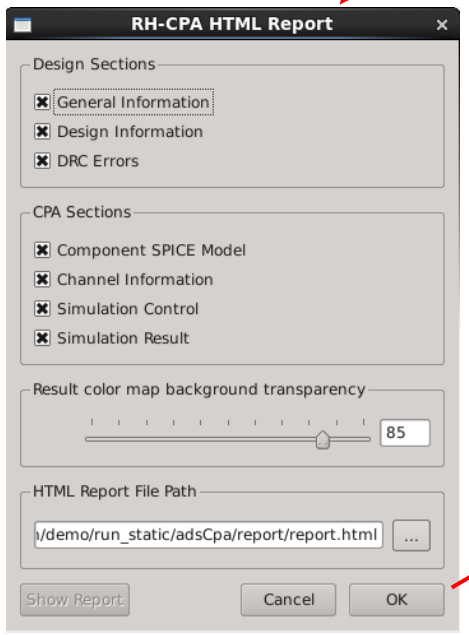
Extraction Results – Pin R/L Map

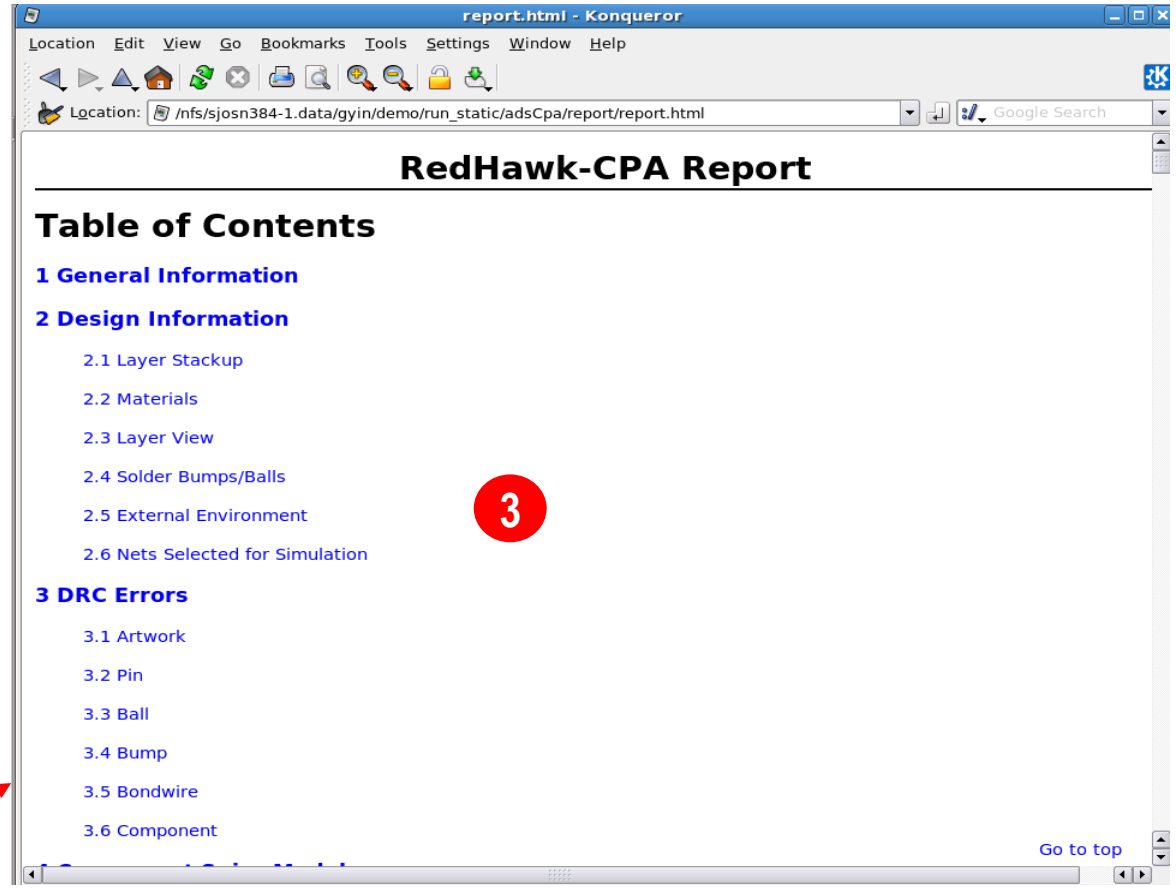


1. After the analysis is completed, click on “PinR” to check per pin resistance map; click “PinL” to check per pin inductance.
2. Define transparency in the “Post Processing” tab of the “Layout Manager” window.
3. Select nets to view their results.

HTML Report Generation







1. Click on “Report->Extraction Report”
2. Select the report sections to be included and HTML report file path, when the tool generates HTML file, click OK to the GUI message box.
3. View the HTML report in any web browser.

HTML Report – Lumped R/Partial L and Capacitance Matrix

7.6 Lumped Resistance and Partial Inductance matrix

S.No.	Net	Net	R (mOhm)	L (pH)
1	VDD_15	VDD_15	3.14256	445.491
2	VSS	VDD_15		87.6378
3	VSS	VSS	0.0910571	169.371

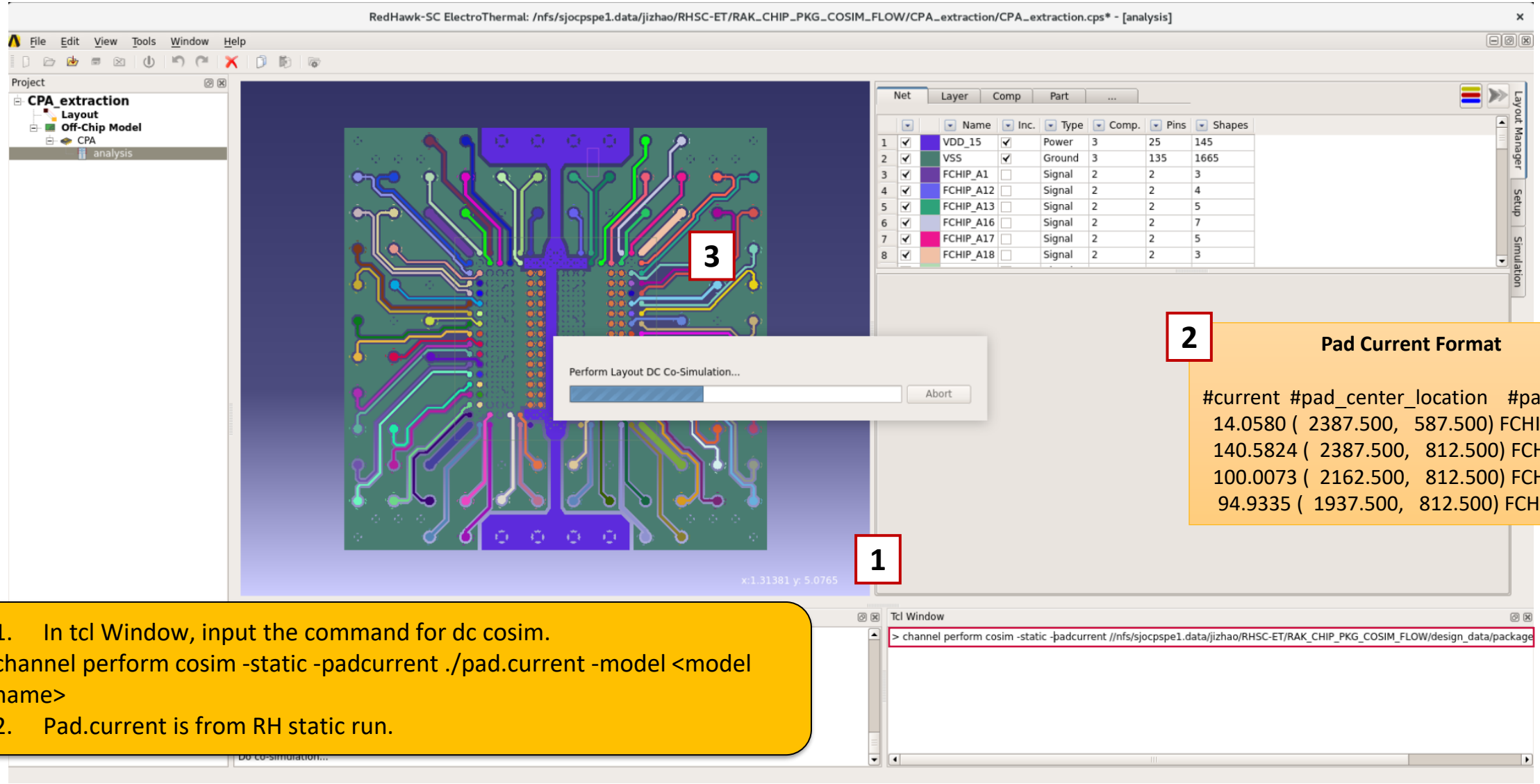
7.7 Per-domain Capacitance matrix

S.No.	Net	Net	C (pF)
1	VDD_15	VDD_15	0.047212
2	VDD_15	VSS	3.00085
3	VSS	VSS	0.395195

Go to top

User can review the Lumped R/Partial L and Cap per domain in this section.

Chip + Package DC Co-sim



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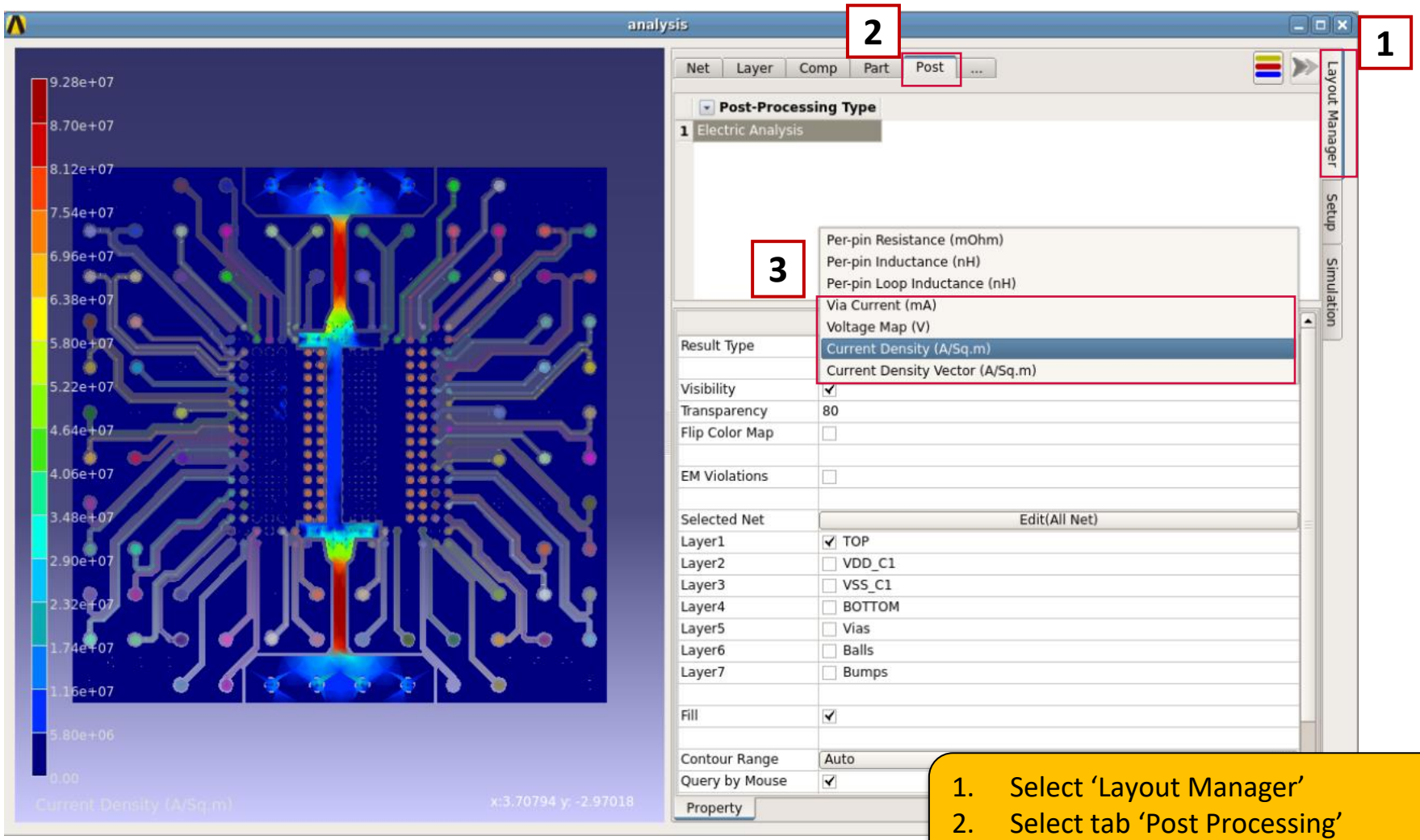
Pad Current Format

```
#current  #pad_center_location    #pad_name
  14.0580 (  2387.500,   587.500) FCHIP-V9
 140.5824 (  2387.500,   812.500) FCHIP-U9
 100.0073 (  2162.500,   812.500) FCHIP-U8
  94.9335 (  1937.500,   812.500) FCHIP-U7
```

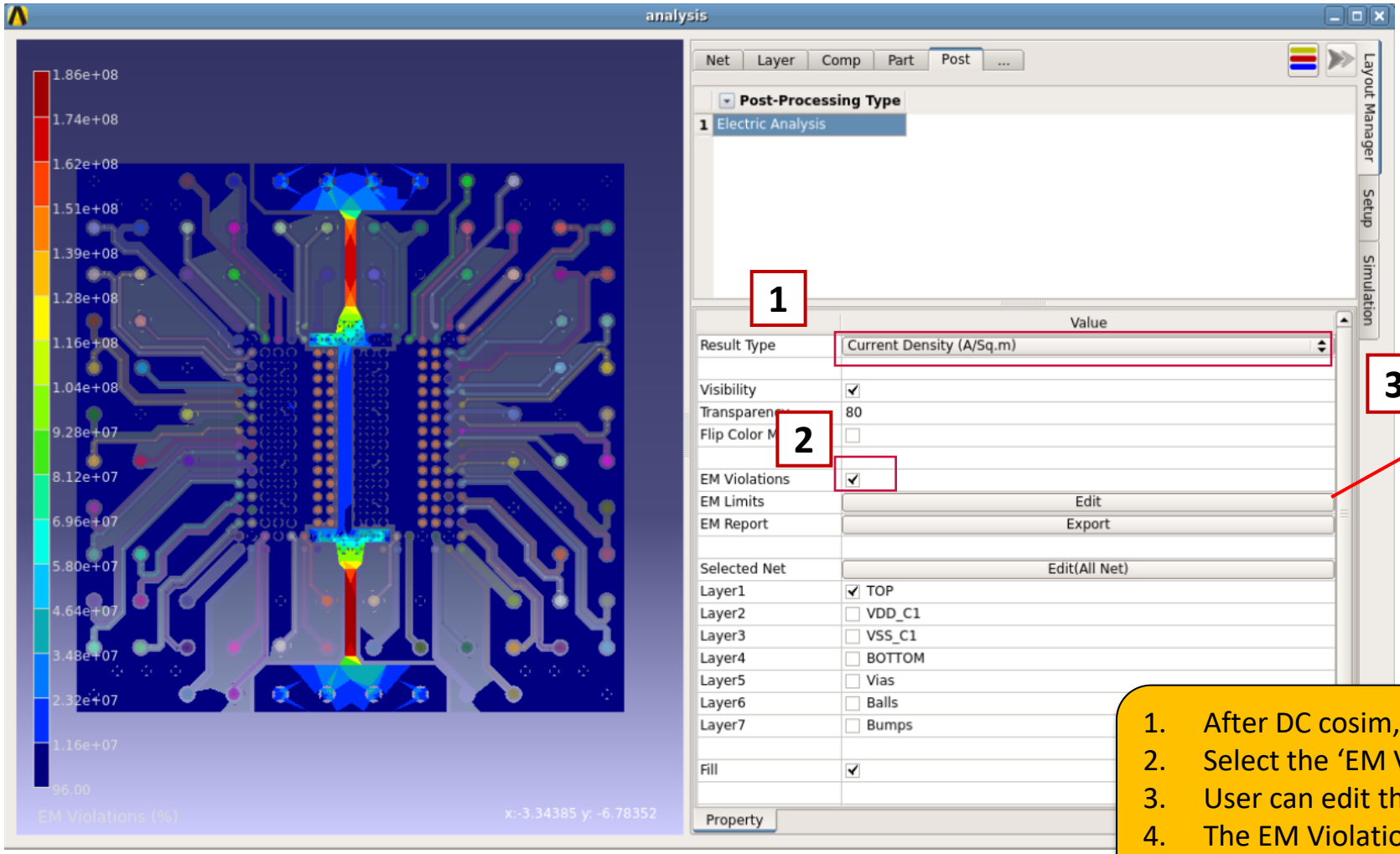
1. In tcl Window, input the command for dc cosim.
channel perform cosim -static -padcurrent ./pad.current -model <model name>
2. Pad.current is from RH static run.

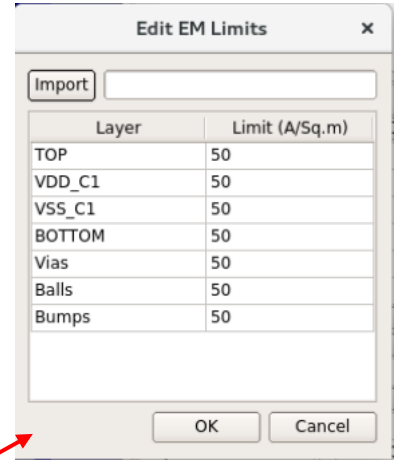
Package DC Co-sim Results Check



1. Select ‘Layout Manager’
2. Select tab ‘Post Processing’
3. User can check the DC results for each layer and each nets

Package EM Check





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1. After DC cosim, select the “Current Density”
2. Select the ‘EM Violations’
3. User can edit the EM Limit for each layer
4. The EM Violations will be show in the layout view immediately.

Tool Installation

- **Set Redhawk-SC Electrothermal path and license :**
  - setenv CPSROOT <choose the version installed on your server>
  - set path = ($CPSROOT/bin $path)
  - setenv LM_LICENSE_FILE <To your redhawk_sc_Electrothermal license>
- **To execute Redhawk-SC Electrothermal :**
  - redhawk_sc_et -3dic (et license)
  - Or redhawk_sc_et (cpa license)
- **Evaluation Package(include product/demo/testcase/material)**

https://download.ansys.com/Semiconductor%20Products

RedHawk-SC ElectroThermal Downloads

Product Name	Size (Bytes)	md5sum	Details
RedHawk-SC ElectroThermal 2020R2.0 Evaluation Package	864,899,758	d7b91e923a08d3aed85b369ff5d70e7f	


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