RedHawk Training - SoC Power, Noise & Reliability

June 16, 2020

Ansys

ANSYS Technologies for Electronic Systems

Power Budgeting

PowerArtist™
RTL Power Analysis, Reduction

PDN, RV

RedHawk™
PDN planning, In-rush, Power Integrity, EM, Integrated pkg

IC→System

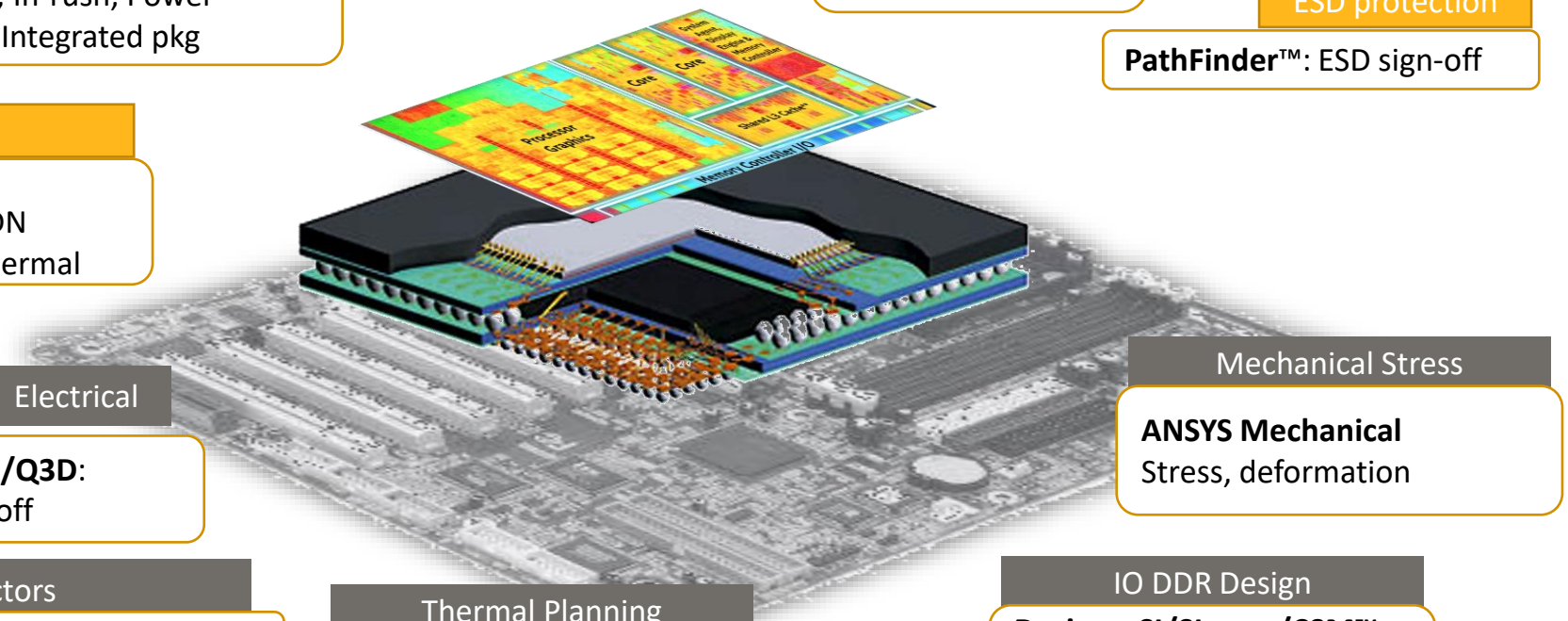
CPM™:
- System PDN
- System Thermal

IP Validation

Totem™:
- IR, EM and DvD
- Model for SoC

ESD protection

PathFinder™: ESD sign-off



Package/PCB Electrical

SIwave/HFSS/Q3D:
Early to sign-off

Mechanical Stress

ANSYS Mechanical
Stress, deformation

Connectors

HFSS/Q3D

Thermal Planning

Icepak
Chip-aware system thermal

IO DDR Design

DesignerSI/SIwave/CSM™:
- IO ring verification
- System jitter prediction

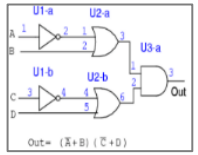
ANSYS Semiconductor Products in Flow

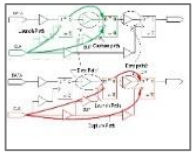
RTL & Gate Power:
- Power reduction
- Power analysis
- Power regression

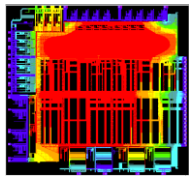
Place & Route:
- Early convergence of PI
- PI aware placement
- Fixing and optimizing

Timing Signoff:
- Spice accurate timing
- Variability/aging aware timing
- DvD aware timing

Power/Reliability Signoff:
- Dynamic voltage drop
- Electromigration
- Chip-aware package design







Architectural spec

Microarchitecture RTL Design

Logic Synthesis

Place and Route

Timing Signoff

Power/Reliability Signoff

Tape-out

PowerArtist™

RedHawk™ - Fusion

Path-FX™

Totem™

RedHawk™

RedHawk-SC™

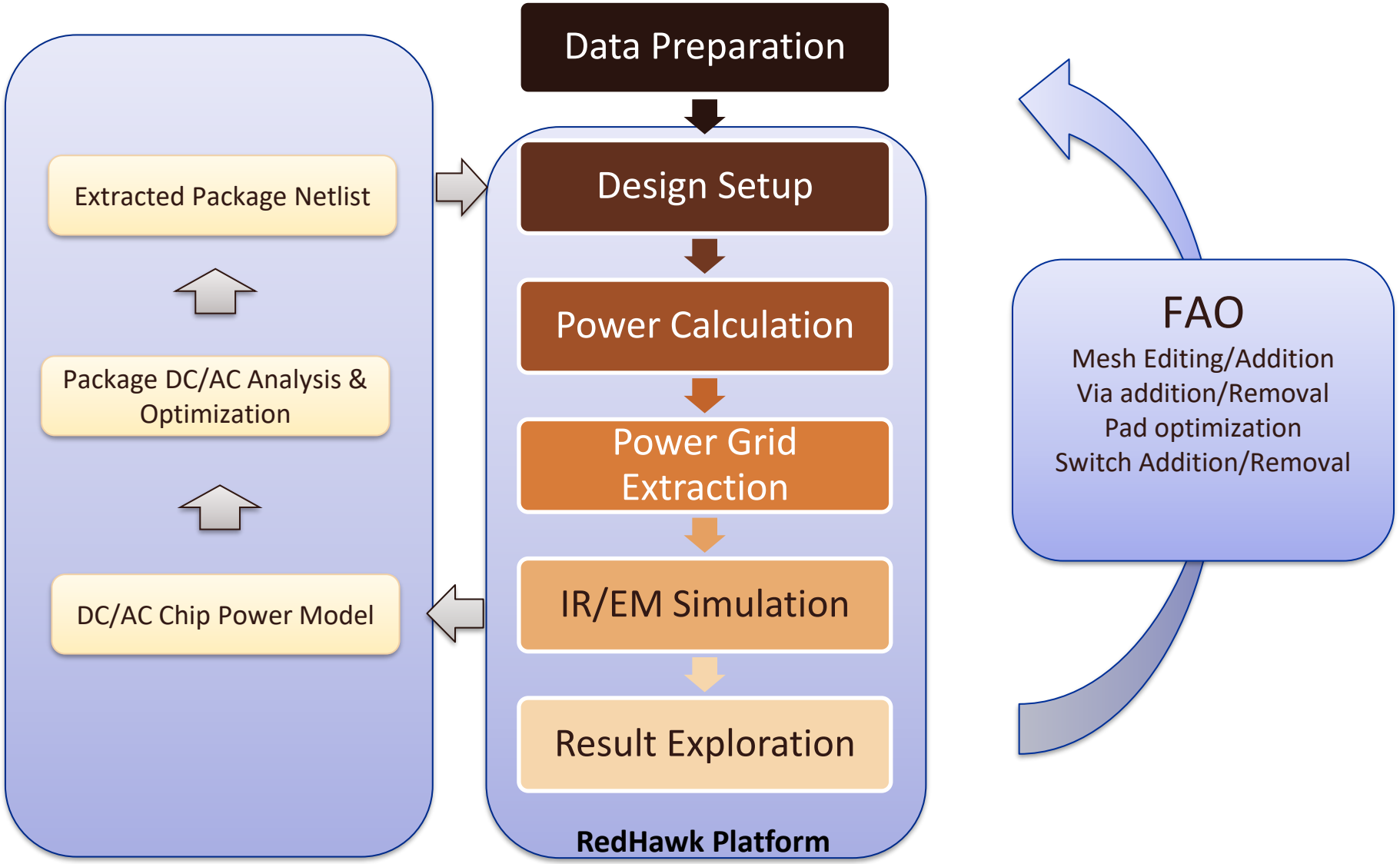
Training Agenda

- RedHawk Static/Dynamic analysis theory
- Input data preparation & IP/Standard cell modelling
- Package handling in RedHawk
- GUI and Tcl commands in RedHawk : Demo
- Result Analysis and Root Cause identification using RedHawk Explorer (RHE)
- Chip Power Model (CPM) generation and Chip-Package-System(CPS) analysis
- Distributed Machine Processing (DMP) for large designs

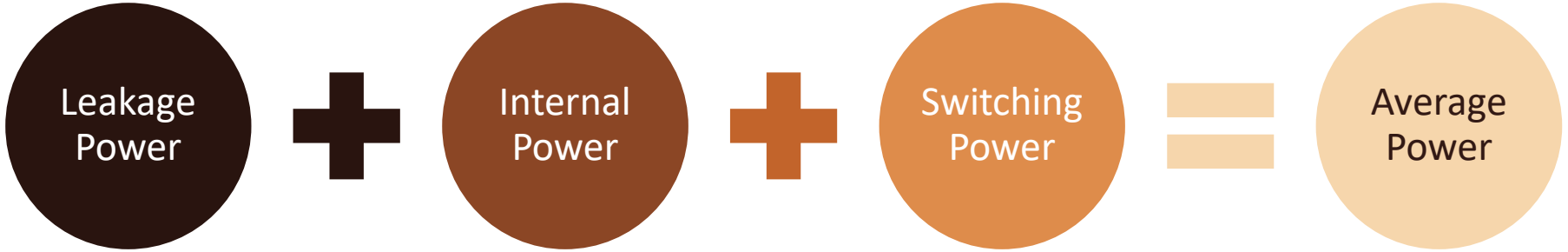
RedHawk Static/Dynamic analysis theory

Ansys

RedHawk Analysis Flow



Gate-level Average Power Calculation




```
leakage_power () {
  value : 0.000000E+00;
  when : "A&!B";
  power_level : "VDDNW";
}

leakage_power () {
  value : 4.430000E+02;
  when : "A&!B";
  power_level : "VDD";
}
```

From .lib

```
internal_power () {
  power_level : "VDDNW";

  rise_power (inputpower_trans4) {
    index_1 ("25.0000,50.0000,625.0000,1250.0000");
    values ("0.0040,  0.0040,  0.0040,  0.0040");
  }

  fall_power (inputpower_trans4) {
    index_1 ("25.0000,50.0000,625.0000,1250.0000");
    values ("0.0040,  0.0040,  0.0040,  0.0040");
  }
}
```

From .lib

Internal Power = Internal Energy(in .lib) * Freq * TR

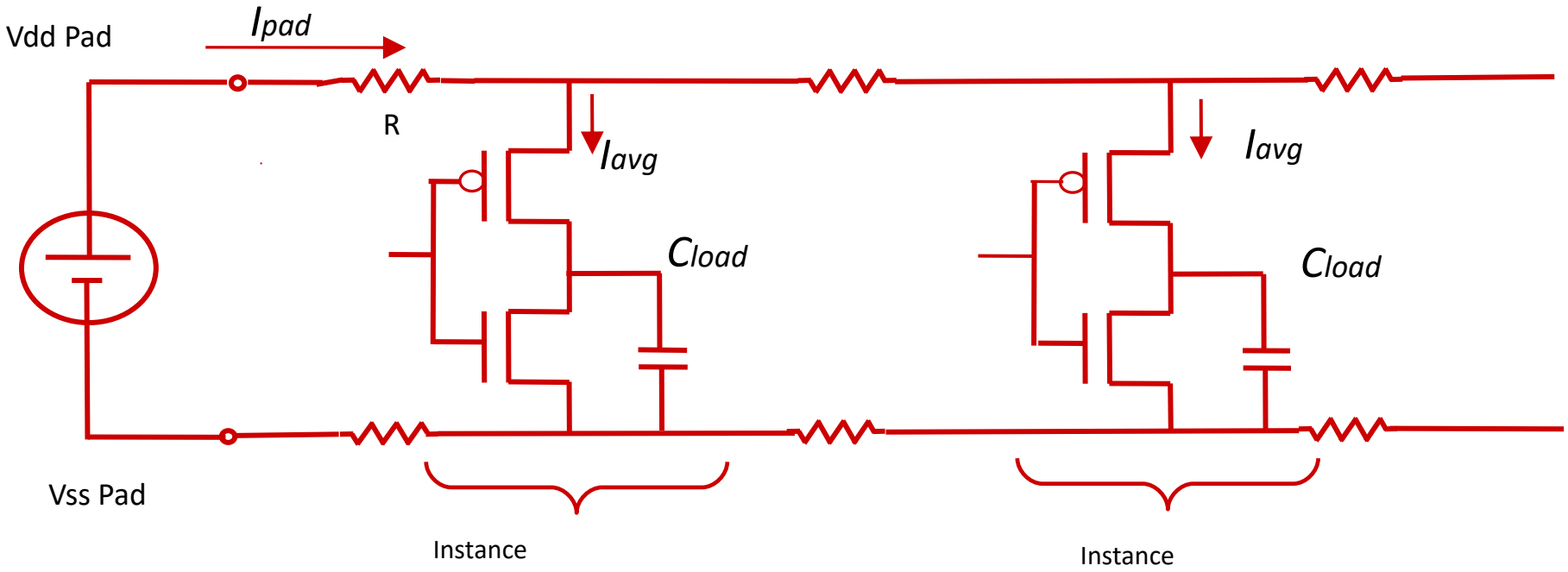
Switching Power = ½ * Cap * V^2 * Freq * TR

From SPEF

From Timing File

P(total) = P(Leakage) + ½ * (Internal-energy * Freq * TR) + ½ * C * V^2 * Freq * TR

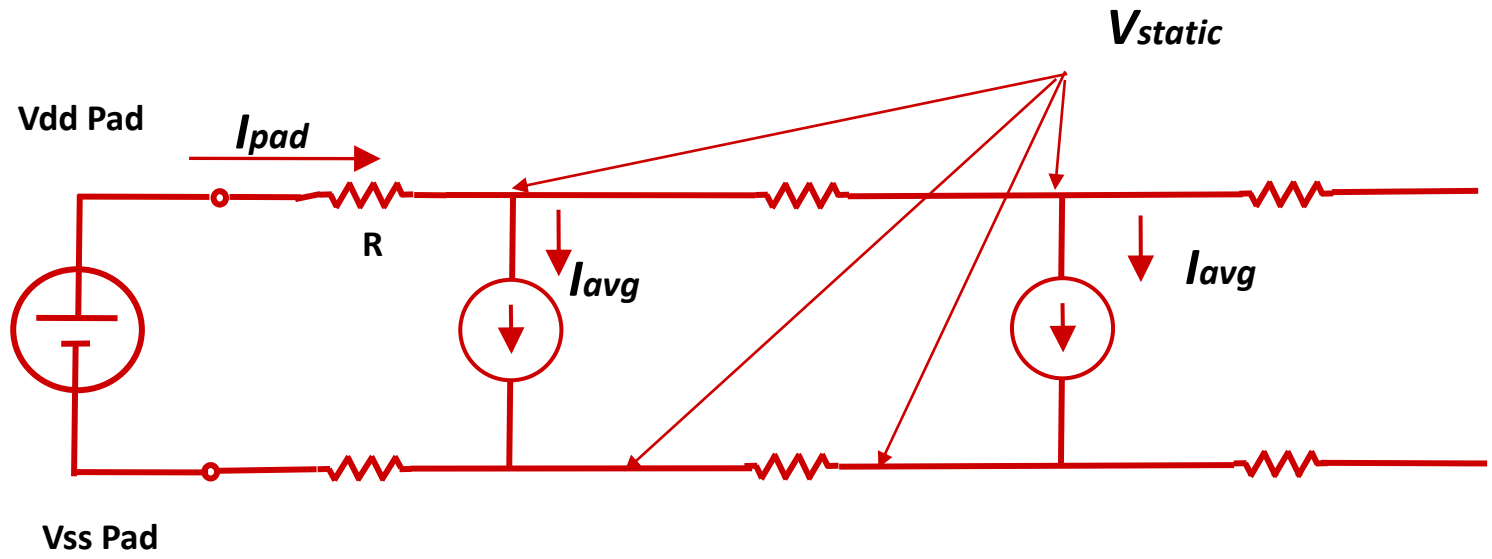
Static Voltage Drop Background



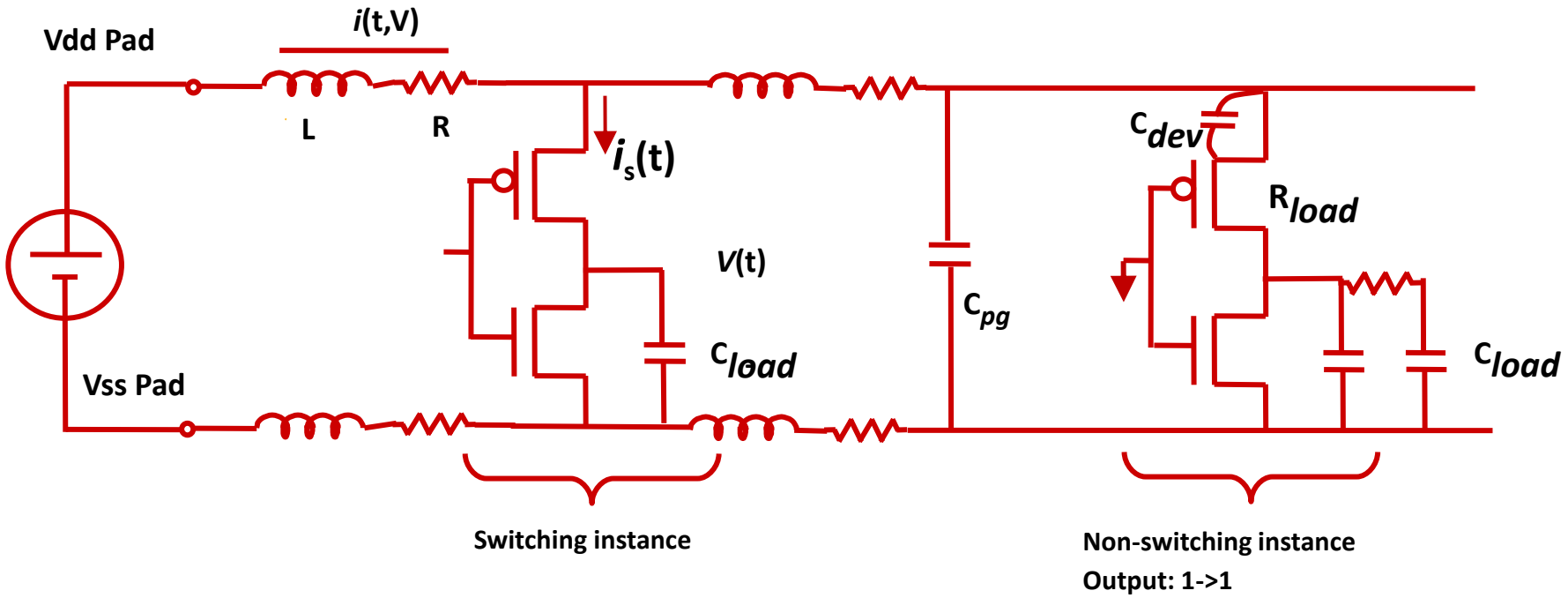
- On-chip power/ground network ➔ mesh of resistors
- Average current (Iavg) of instances is estimated from Average power
- Instances ➔ DC current sources

Static Voltage Drop on P/G Network

- Average current is calculated for each instance
- V_{static} is computed at every node (Ohm's law ...)
- Wire / via electromigration (*EM*) is post-processed from static current density



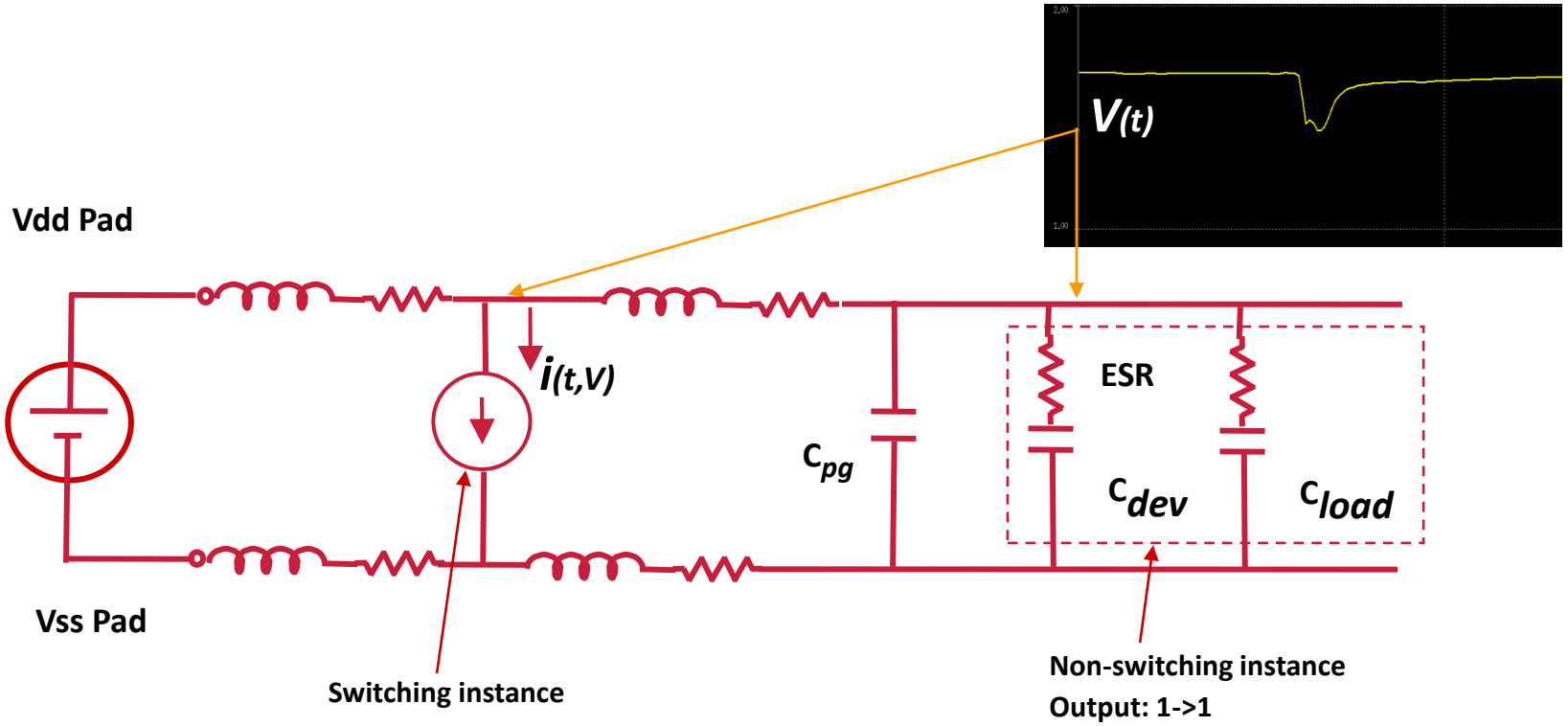
Dynamic Voltage Drop Problem Definition



- On-chip power/ground network ➔ R,L,C mesh
- Switching instances ➔ i(t,V) sources
- Non-switching instances ➔ Effective decaps, ESR and leakage

Dynamic Voltage Drop on P/G Network

- PWL current for each instance
- Vdynamic waveform is computed at every node by transient simulation



Difference Between Static and Dynamic

Static	Dynamic
All instances will draw an average current (DC)	Switching instances will draw transient current (AC) Non-switching instances will draw only leakage
Total Average demand will be much less than real peak demand current for the chip	Dynamic will see the real peak demand current
Demand current is completely supplied by battery	Portion of the demand current is supplied by decaps (Intrinsic / Intentional / PG caps)
Doesn't matter when an instance switches Instances will draw the current all the time	Instances will draw transient current only when it switches Simultaneous switching causes huge peak current demand
No drop across package due to Ldi/dt effects (Current is constant)	Ldi/dt drop across package and die inductance

Input data preparation & IP/Standard cell modelling

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RedHawk Input Data Requirement

Library Data

- LEF
- LIB
- GDS
- APL*
- TECH*

Design Data

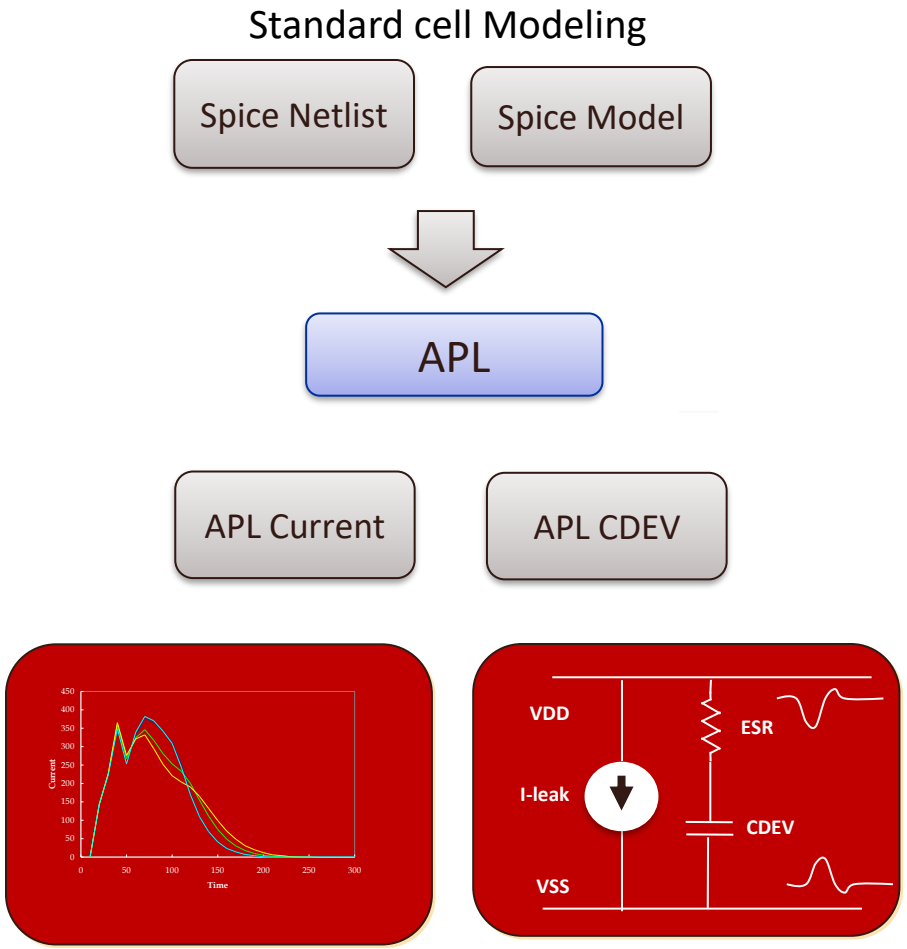
- DEF
- SPEF
- STA*
- VCD
- Package
- Pad Files

Redhawk Data

- GSR
- Command File
- GSC

* : *These inputs are created using Ansys utilities*

RedHawk Modeling for Standard Cells



- Current Model
  - Look up table for current waveforms based on three variables : load, slew and voltage
- Cap Model
  - Captures effective series resistance(ESR) and effective series capacitance(ESC) and leakage

RedHawk Modeling of Memories and IPs

Physical Modeling from GDS

GDS

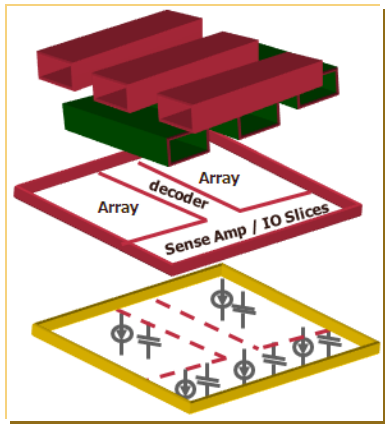
LEF

Layer map

GDS2RH

LEF

DEF



Current Modeling From Simulation W/f

Simulation Waveform Data
(FSDB,PWL etc)

Sim2iprof

APL Current

Cap Modeling Through ACE

Spice Netlist

Spice Model

ACE

APL CDEV

Current/CAP Modeling Through AVM

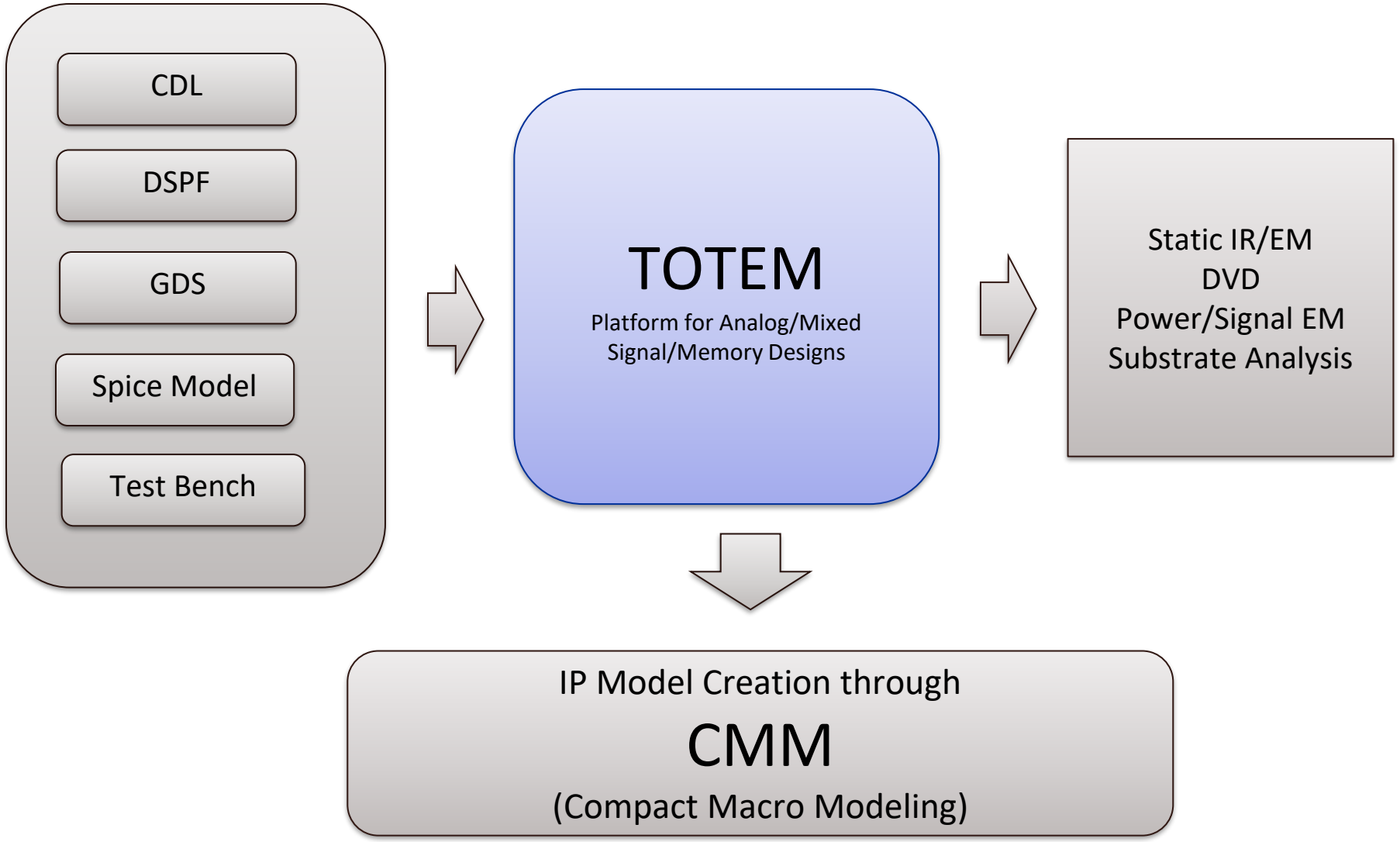
Synopsys LIB/ Datasheet
Parameters

AVM

APL Current

APL CDEV

Transistor Level IP Modeling Using Totem



What is Inside STA File ?

- Instance Frequency
  - Required for static and dynamic
- Clock domain info
  - Required for static and dynamic
- Timing Windows
  - Not required for static
- Slew
  - Required for Static (Power calculation uses Slew)
  - Required for Dynamic (Current w/f is dependent on Slew)

Specifying Voltage Source Locations

Option-1
Redhawk automatically identifies the voltage source locations from PINS section in DEF

Option-2
User can specify the master cell name for P/G pads through a file

Option-3
User can specify the P/G pad instance names through a file

Option-4
User can specify the P/G pad (x,y) locations through a file

Most commonly used

See RedHawk manual for details

GSR (Global System Requirement) File

```
TECH_FILE <path to TECH File>

LIB_FILES {
<Path to LIB Files>
}

LEF_FILES {
<Path to LEF files>
}

GDS_CELLS  {
<Path to Gds2def models>
}

APL_FILES  {
<Path to APL models>
}

CMM_CELLS {
<Path to CMM models>
}
```

Library File Pointers

```
DEF_FILES {
<Path to the DEF files>
}

STA_FILE  {
<Path to timing file>
}

CELL_RC_FILE  {
<Path to Spef file>
}

VCD_FILE  {
<VCD file details>
}

PAD_FILES  {
<Path to Pad File>
}
```

Design Data Pointers

Commonly Used GSR Keywords

```
FREQUENCY 70e6
```

Dominant Frequency of the design

Frequency	% of Total Power	Cumulative % of power
100 MHz	80%	80%
70 MHz	10%	90%
20 MHz	10%	100%

- Important input for Vectorless engine
- Dominant frequency is NOT the frequency with highest % of power
- It is the frequency above which 90% of the power is present
  - Arrange frequency in descending order
  - Start adding up cumulative power
  - Frequency at which we achieve 90% cumulative power is selected as dominant frequency
- Script is available to automatically set this

Commonly Used GSR Keywords

```
TOGGLE_RATE 0.15 1.5

INSTANCE_TOGGLE_RATE {
  instance_name toggle_rate
}

BLOCK_TOGGLE_RATE {
  block_name toggle_rate
}
```

Global Toggle Rate Used
(BPFS will override this)

```
TEMPERATURE 125
```

To specify the P/G Extraction Temperature

```
VDD_NETS {
 VDD 1.2
 inst_129973/VDD_INT 1.2
}
GND_NETS {
 VSS 0
}
```

Nets being analyzed and Ideal Voltage

Commonly Used GSR Keywords

```
DYNAMIC_SIMULATION_TIME 10e-9

DYNAMIC_PRESIM_TIME -1

DYNAMIC_TIME_STEP 10e-12
```

Dynamic Simulation Settings

```
INPUT_TRANSITION 100e-12
```

Default Slew value used
(Used for instances missing in STA File)

```
IGNORE_TECH_ERROR 1
IGNORE_DEF_ERROR 1
IGNORE_UNDEFINED_LAYER 1
IGNORE_LEF_DEF_MISMATCH 1
```

Option to proceed even with Errors

Commonly Used GSR Keywords

BLOCK_POWER_FOR_SCALING (BPFS)

- Used for defining power target values
- RH will scale the toggle rate to meet user specified power target
- Scaling can be done at Full-chip/Block level. It can be master cell specific too
- Can define pin specific power for multi-vdd cells

```
BLOCK_POWER_FOR_SCALING  {

  FULLCHIP FULLCHIP 1.2

  FULLCHIP BLOCK_INST_NAME 0.5

  CELLTYPE MEM_1024x768 0.1

  FULLCHIP INST1 0.005 VDD1
  FULLCHIP INST1 0.006 VDD2
}
```

INSTANCE_POWER_FILE (IPF)

- Can be used to import instance power numbers from 3rd party tools
- RH will assign the power number from this file as it is
- Instances missing in this file will get zero power
- Supports pin specific assignment

```
INSTANCE_POWER_FILE design.ipf
```

```
#Format of design.ipf
Inst1/inst_100 0.0123
Inst1/inst_102 0.0123
Inst1/inst_104 0.0123
Inst1/inst_105 0.0123
Inst1/inst_106 0.0123
Inst1/inst_107 0.0123
Inst1/inst_108 0.0123
Inst1/inst_108 0.0123
Inst1/inst_109 0.0123 VDD
```

Command File Overview

```
# Import data
import gsr GENERIC.gsr
setup design

# Calculate power
perform pwrcalc

# Power/Ground grid extraction
perform extraction -power –ground


# Static IR analysis
perform analysis –static

# Exporting the DB for future use
export db static.db
```

Static command file

```
# Import data
import gsr GENERIC.gsr
setup design

# Calculate power
perform pwrcalc

# Power/Ground grid extraction
perform extraction -power –ground -c


# Dynamic IR analysis
perform analysis –dynamic

# Exporting the DB for future use
export db dynamic.db
```

Dynamic command file

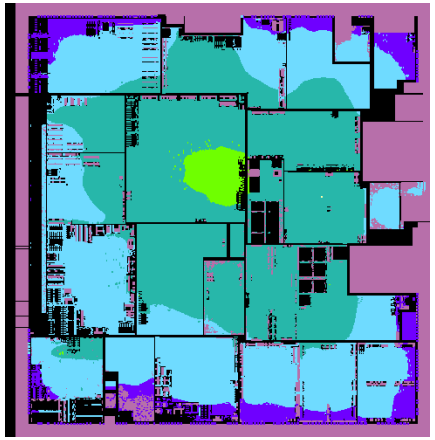
Vector based analysis

- RedHawk supports various simulation output formats
  - VCD (Value change dump) File
  - FSDB (Fast signal database)
- VCD/FSDB can be generated at two stages
  - RTL Level : contains only Flop and primary I/O activity
  - Gate Level : contains activity for all nets in the design
- Cycle selection can be done based on
  - Power : Pick cycle with worst power
  - Change in power : Pick cycle with worst change in power

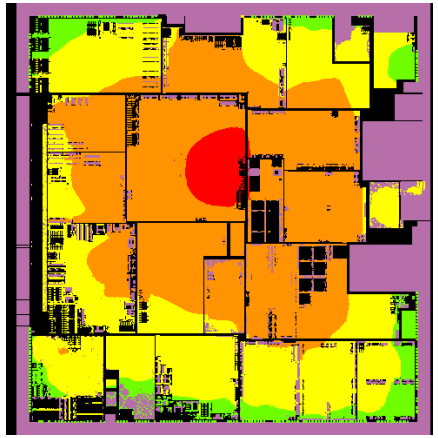
Package Handling in RedHawk

Ansys

Package Impact on Dynamic Voltage Drop



Without Package Model



With Package Model

Inclusion of package effects

- Ldi/dt noise and hence higher drops
- Choice of package capacitance

Different methods for annotating Package

- Using lumped values through command file
  - Setup package/wirebond/pad constraints
- Using package spice netlist
  - In the form of RLCK models
  - In the form of S-Parameter form

GSR Settings Requirements

```
DYNAMIC_SIMULATION_TIME 5e-9

DYNAMIC_TIME_STEP 10e-12

DYNAMIC_PRESIM_TIME 20e-9
```

→ Sufficient presim to charge internal nodes

```
CPA_FILES {
PACKAGE <package_layout_filename>

MODEL <project_path>
}
```

→ Package layout to be extracted & displayed in GUI

→ CPA package model with ploc file

If CPA model is not available

```
PAD_FILES {
  GENERIC.ploc
}
PACKAGE_SPICE_SUBCKT_INFO {
  PATH GENERIC.package.spi
}
```

→ Ploc files with package hooked up

→ Wrapped Package spice netlist

Q & A Session

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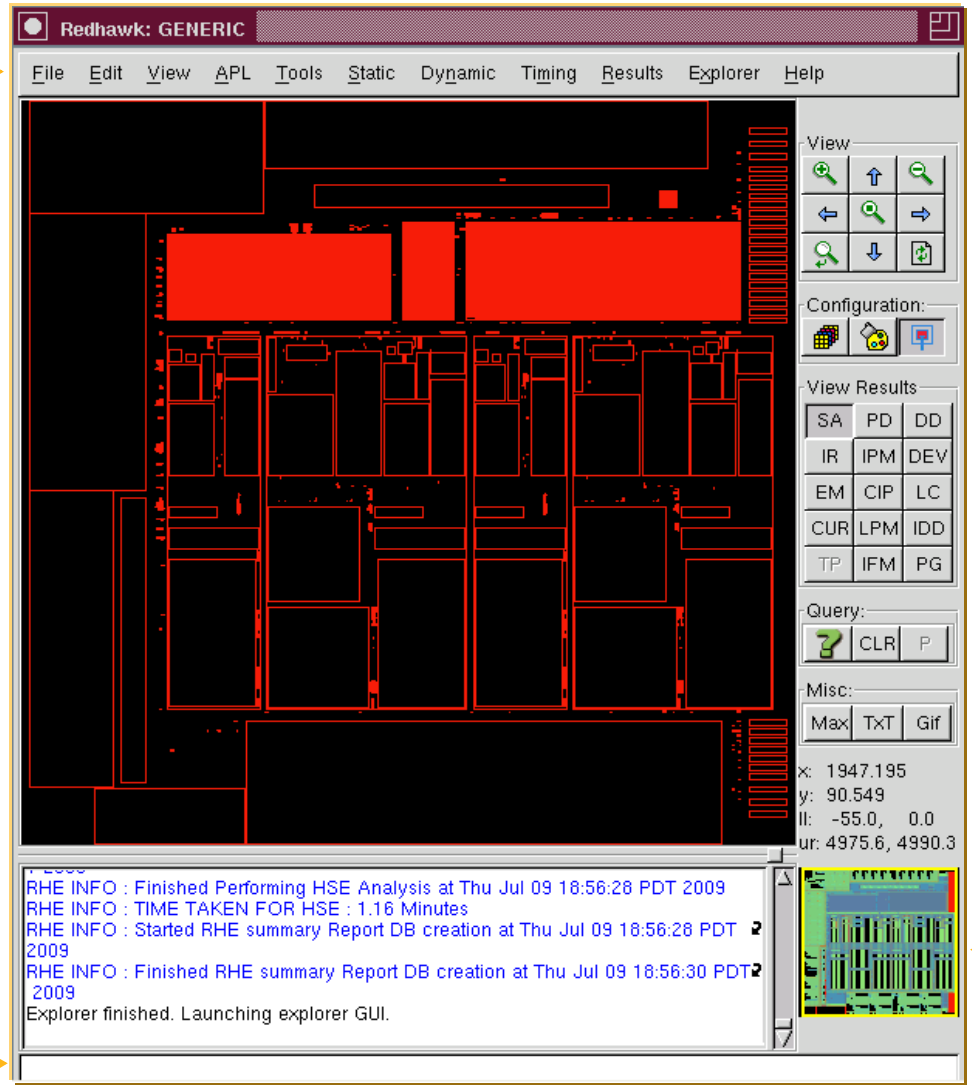
GUI and Tcl commands in RedHawk : Demo

Ansys

RedHawk GUI Overview



Pull-down Menu

Layout Window

Message Window

TCL Console

Navigation Menu

Layer/Legend Selection

Maps

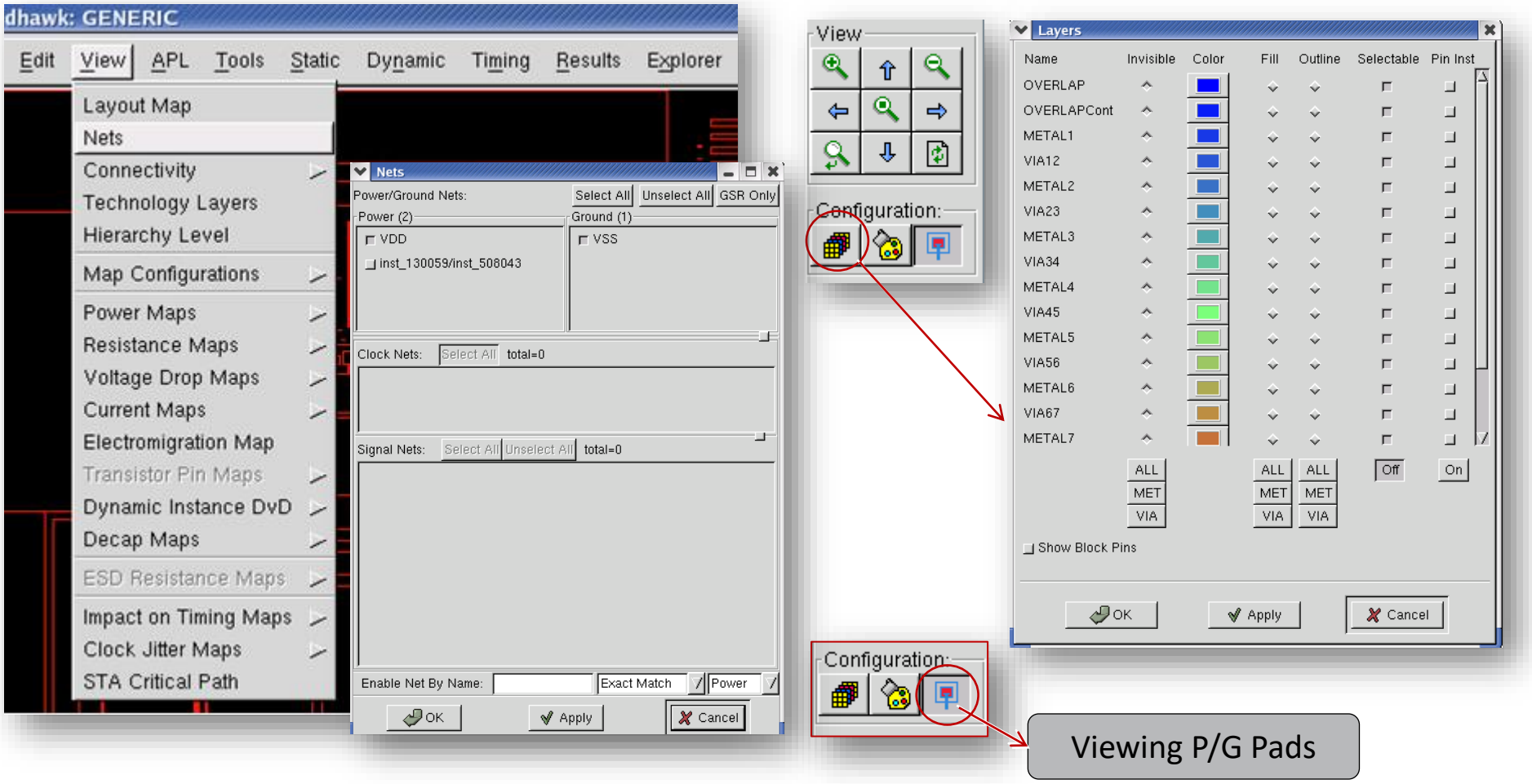
Query/Search

Bird's eye view

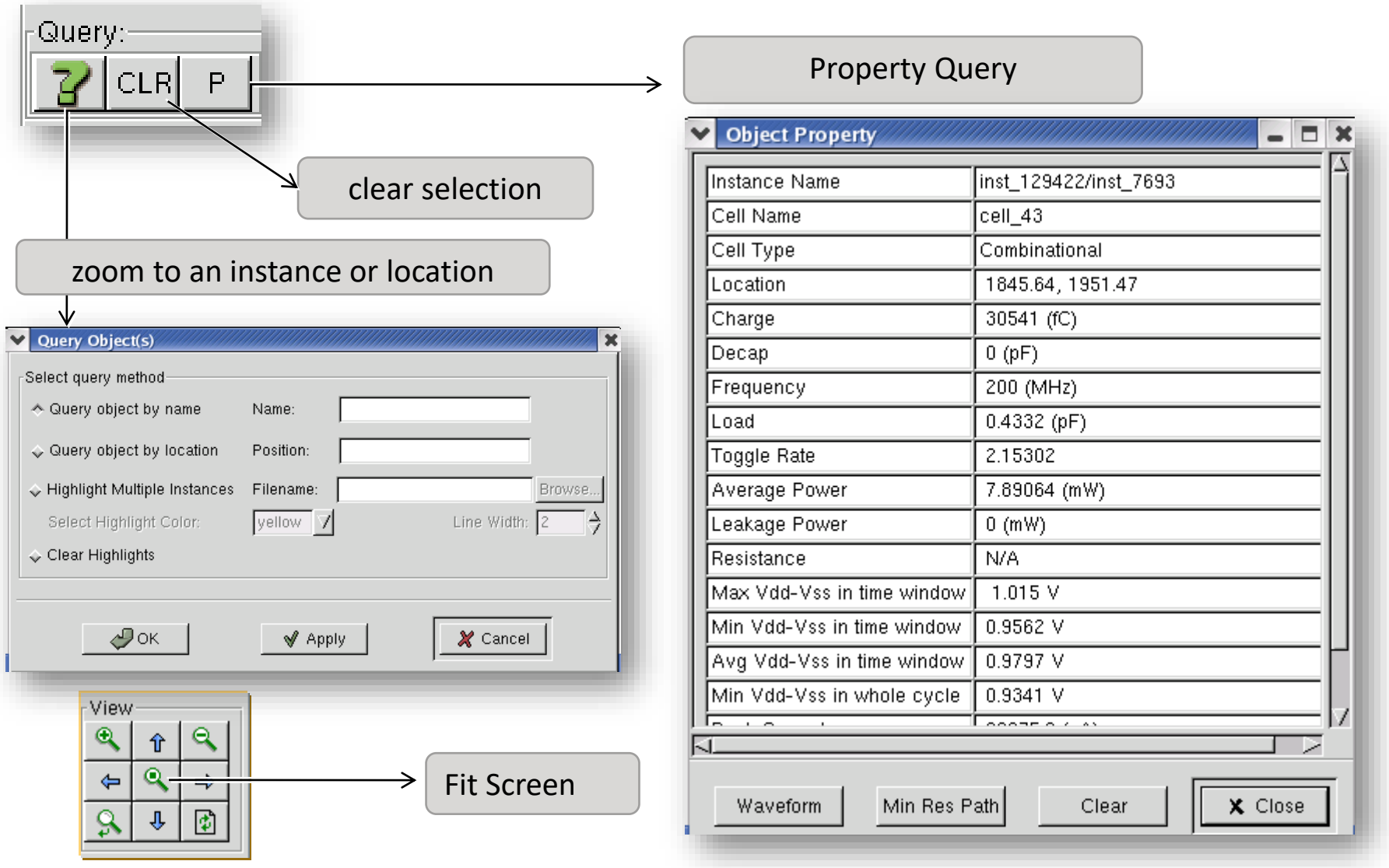
GUI Basic Operations

Viewing Selective Nets

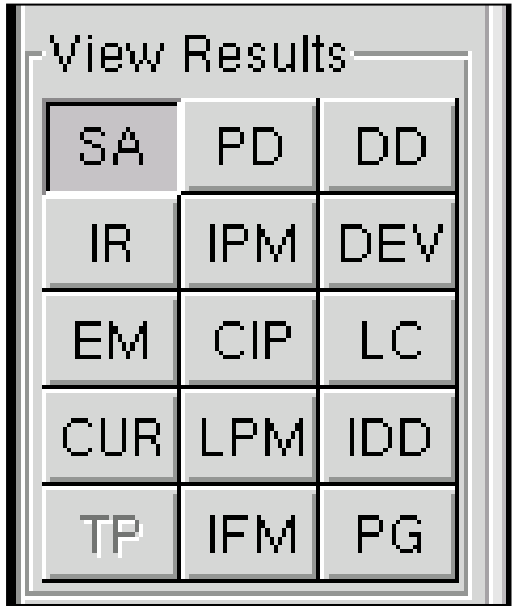
Viewing Selective Layers



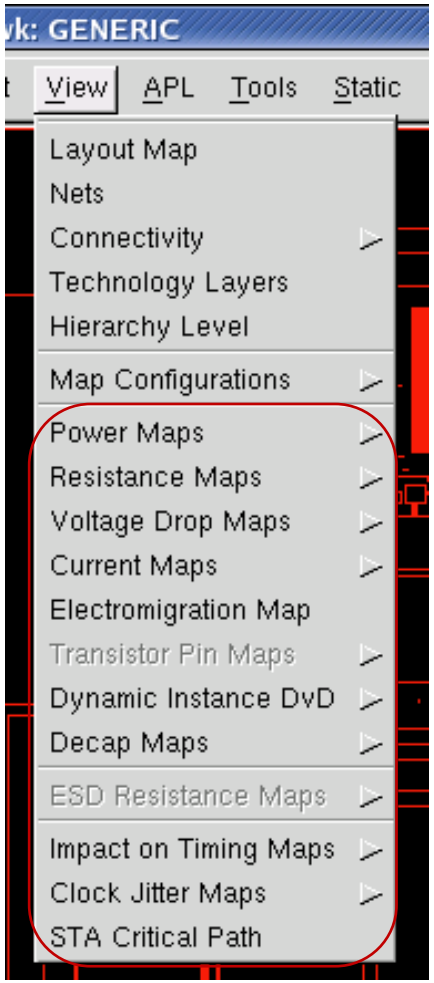
Search / Query Options



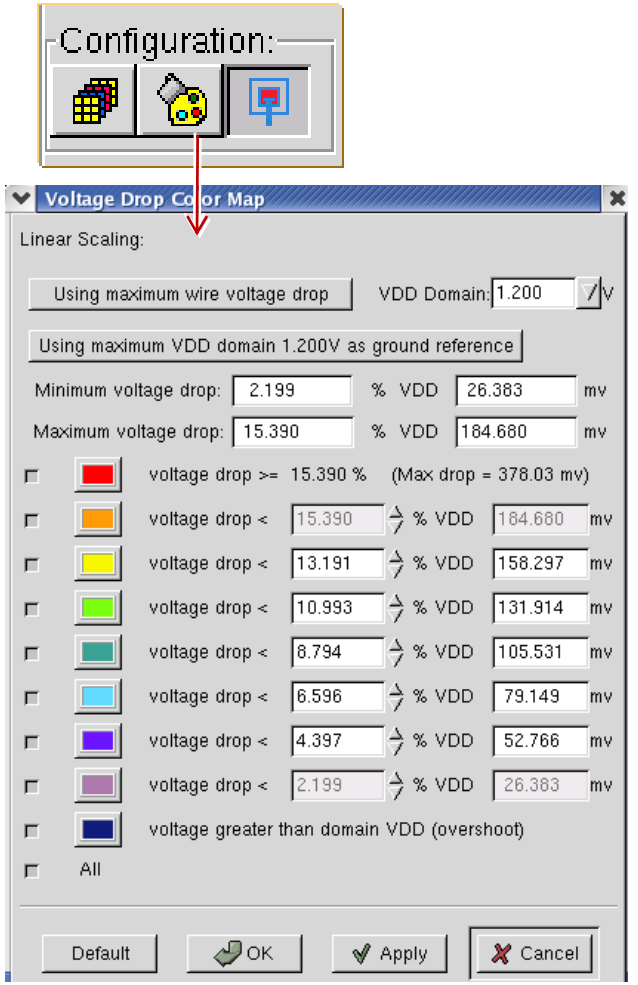
Viewing Different Maps



Map Shortcuts

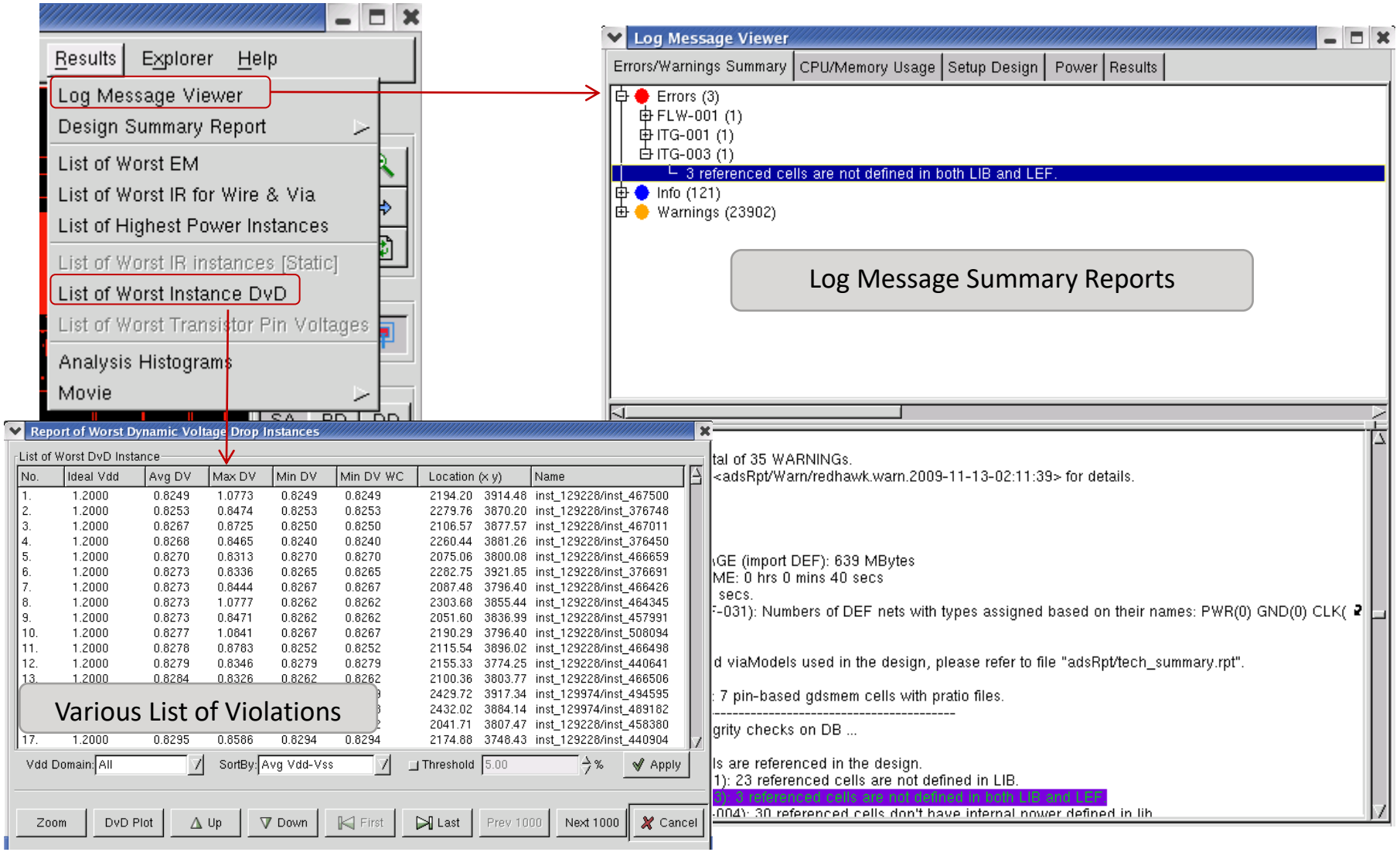


Complete List of Maps

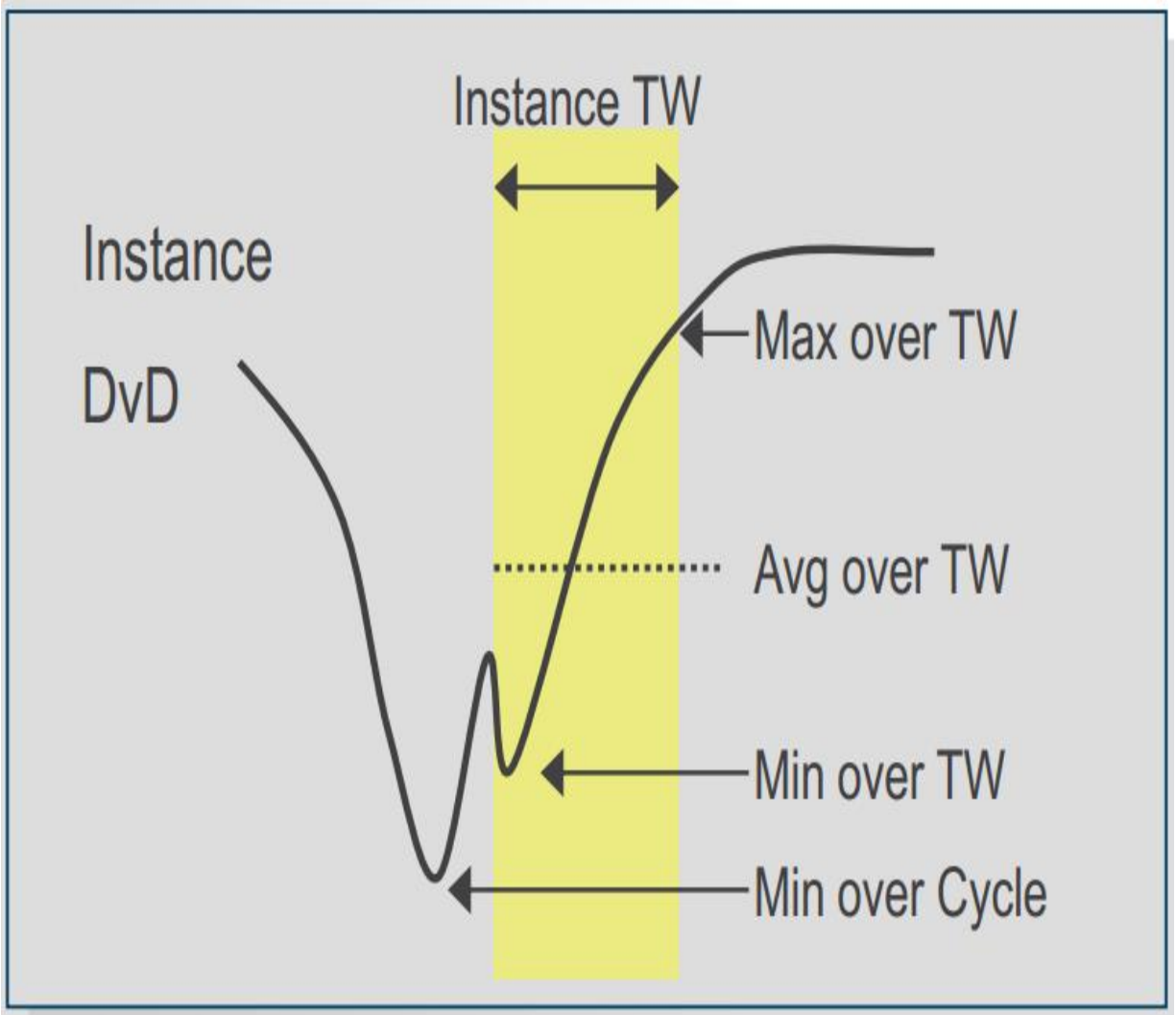


Controlling Map Color Legends

Viewing Different GUI Reports



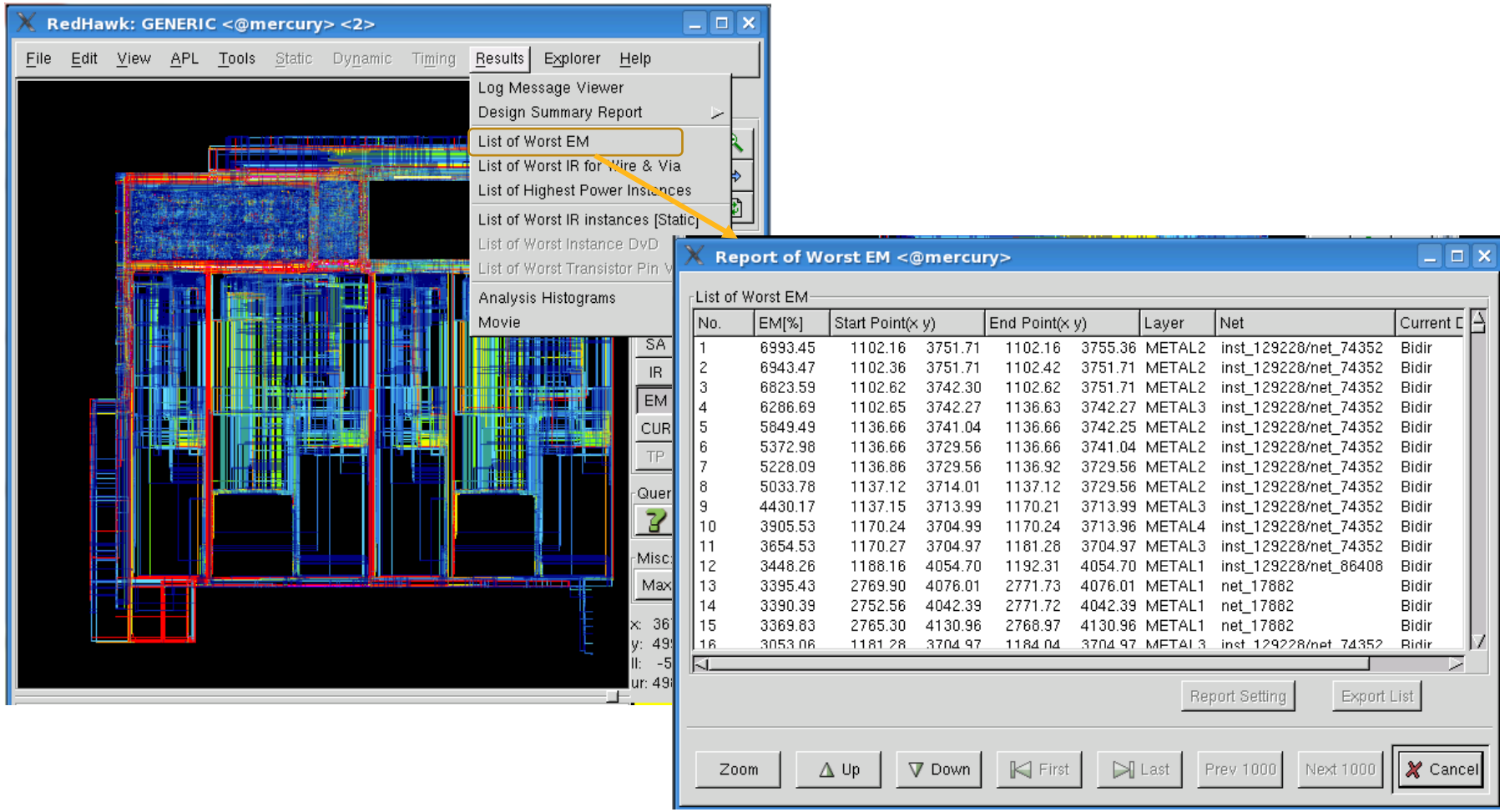
Types of Voltage drop



- Min over Cycle : MinWC : Worst drop for the whole simulation time
- Min over TW : MinTW : Worst drop within timing window of the instance .Worst drop when instance is switching
- Avg over TW : AvgTW : Average drop within timing window . AvgTW is typically used to give feedback to timing tool
- Max over TW : Max TW : Best drop in TW; Not much used

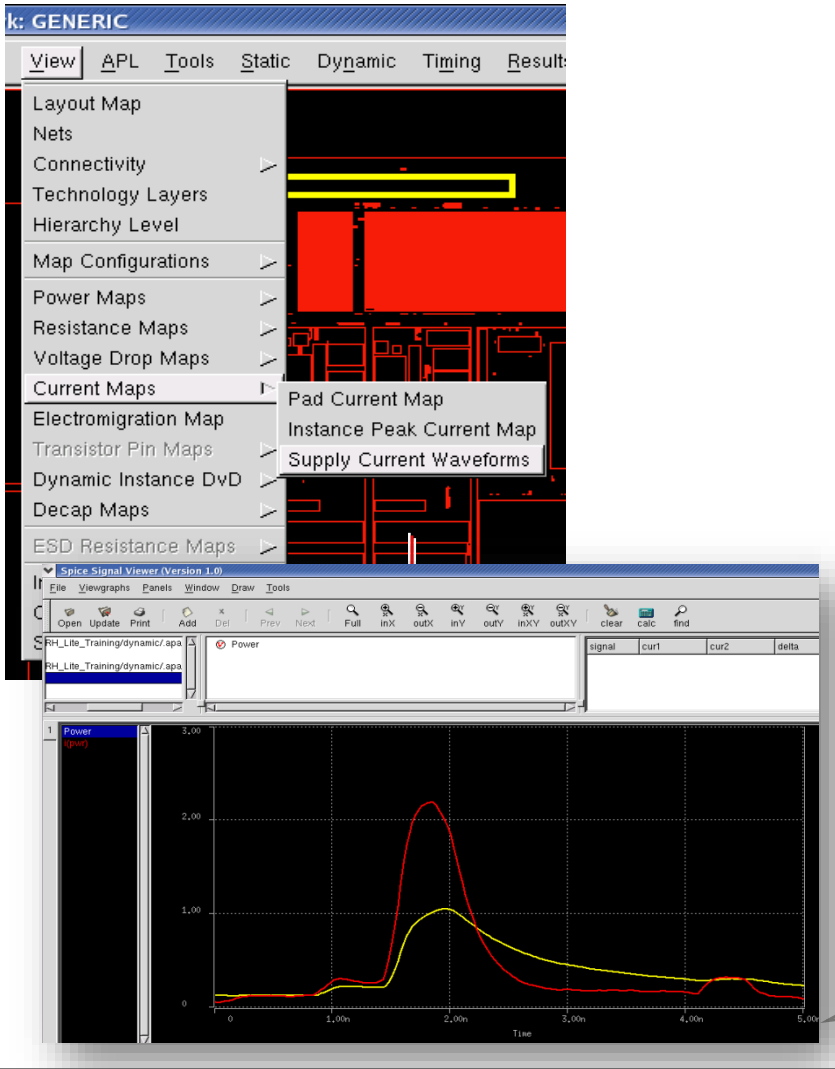
Electromigration Analysis

List of Worst EM report



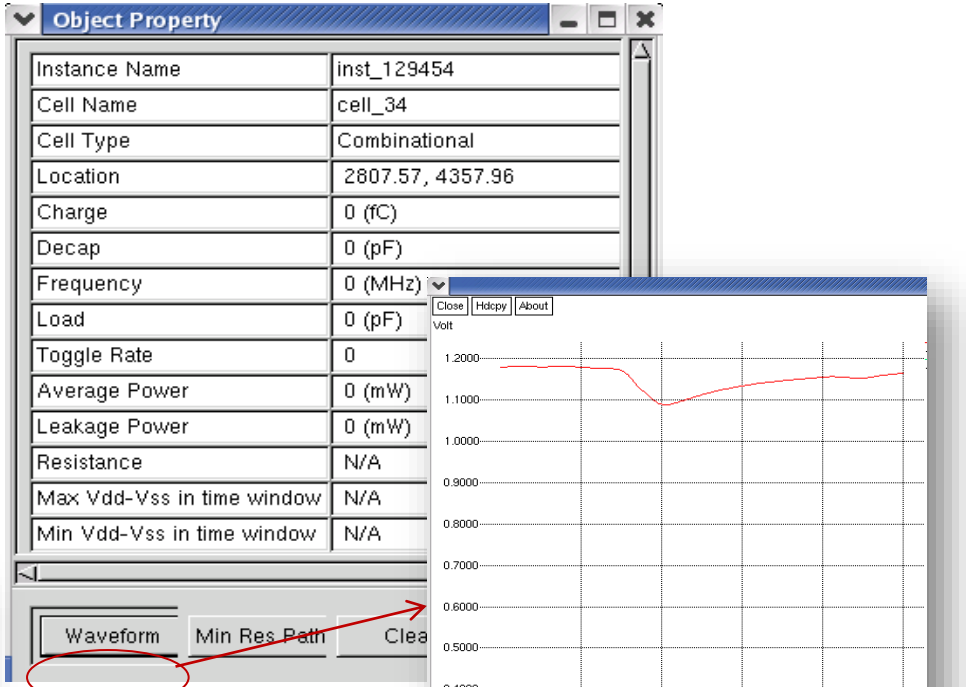
Viewing Different Waveforms

Current w/f



TCL command:
plot current <options>

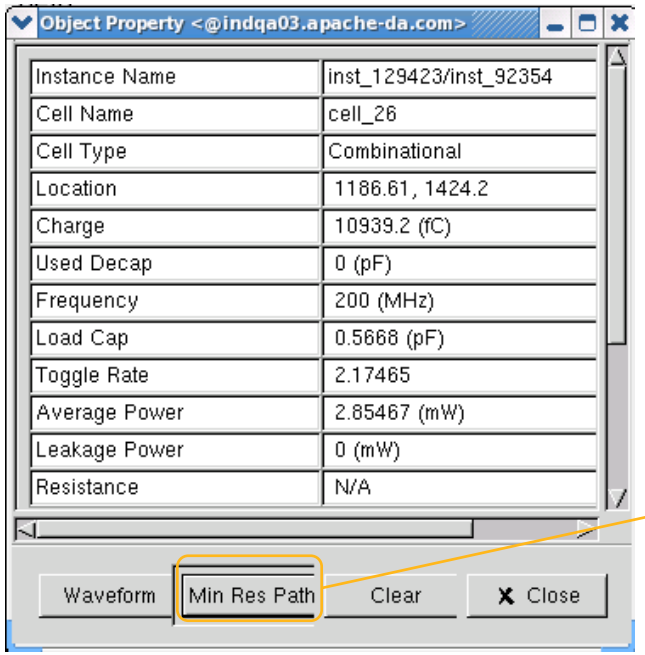
Voltage w/f

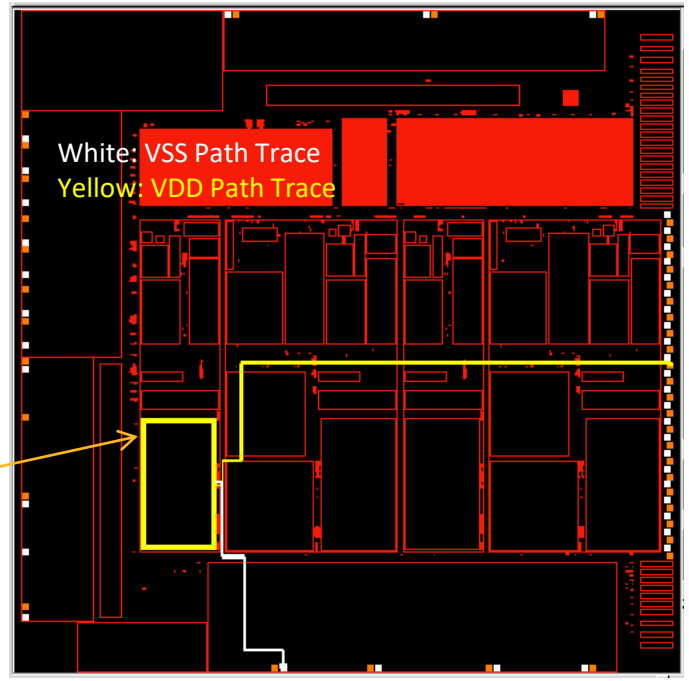


TCL command:
plot voltage <options>

Minimum Resistance Path Tracing

- Traces the minimum resistance path to an instance from the electrically nearest voltage source point
- Can be invoked using Tcl Command : **'perform min_res_path path -inst <instName>'**
  - Displays minimum res path for all P/G pins in GUI
  - Generates a resistance report which will give the break-up of resistance and voltage drop across different wire/via segments in the path
- **Can also be invoked from Instance Property box window**





Important Text Reports

File	Description
adsRpt/redhawk.log	RedHawk log file
adsRpt/power_summary.rpt	Power Summary Report
adsRpt/<design>.power.rpt	Detailed Power Report
adsRpt/Static/<design>.inst.worst	Instance Static IR Report
adsRpt/Dynamic/<design>.dvd	Instance DVD Report
adsRpt/Static/<design>.em.worst	Wire EM Report

Commonly used TCL Commands

Command	Description
import db/export db	For importing and exporting the database
help	To get help on any TCL command
print type	Prints the cell type wise switching statistics
plot switching	Plots switching histogram
plot analysis	Plots analysis histograms
gsr get / gsr set	Queries / Assigns a GSR keyword parameter (supported only for selected keywords)
condition set –time/-xy/-type	Filters the analysis results to specified time/bbox or cell type

Instance & Cell Attribute Query Commands

Command	Switch
get inst $inst	-master
	-freq
	-power
	-peak_current
	-resistance
	-decap
	-switching_status
	-bbox
	-location
	-orientation
	-voltage
get inst * -glob	Loops through all instances in the design

Command	Switch
get cell $cell	-type
	-height
	-width
	-pins
	-pgarcs
get cell * -glob	Loops through all master cells in the library

Net & Pad Attribute Query Commands

Command	Switch
get net $net	-ideal_voltage
	-worst_drop
	-worst_em
get net * -glob	Loops through all nets in the design

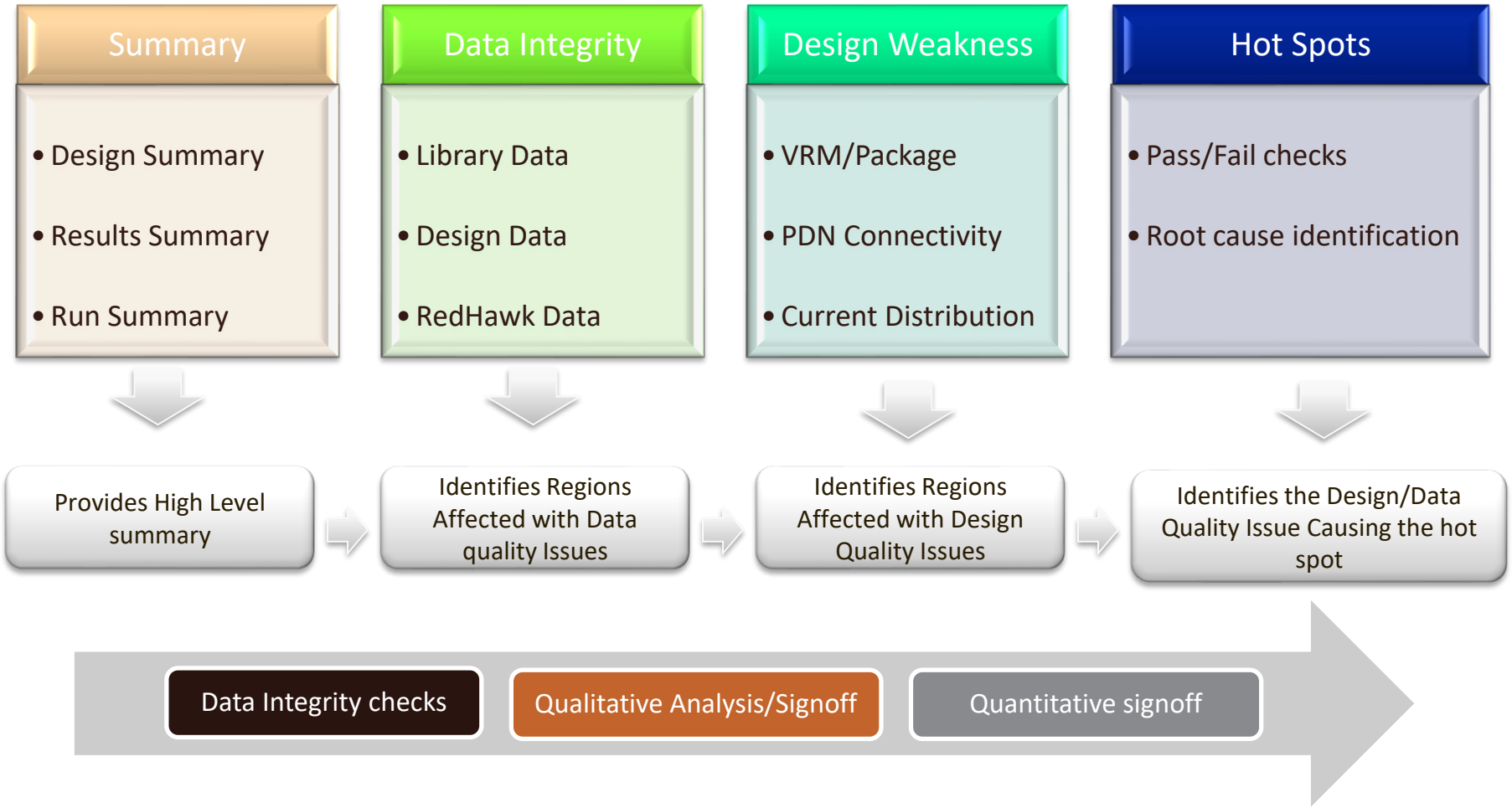
Command	Switch
get pad $pad	-info
	-voltage
	-current
	-layer
	-location
	-net
get pad * -glob	Loops through all pads in the design

Result Analysis and Root Cause identification using RedHawk Explorer

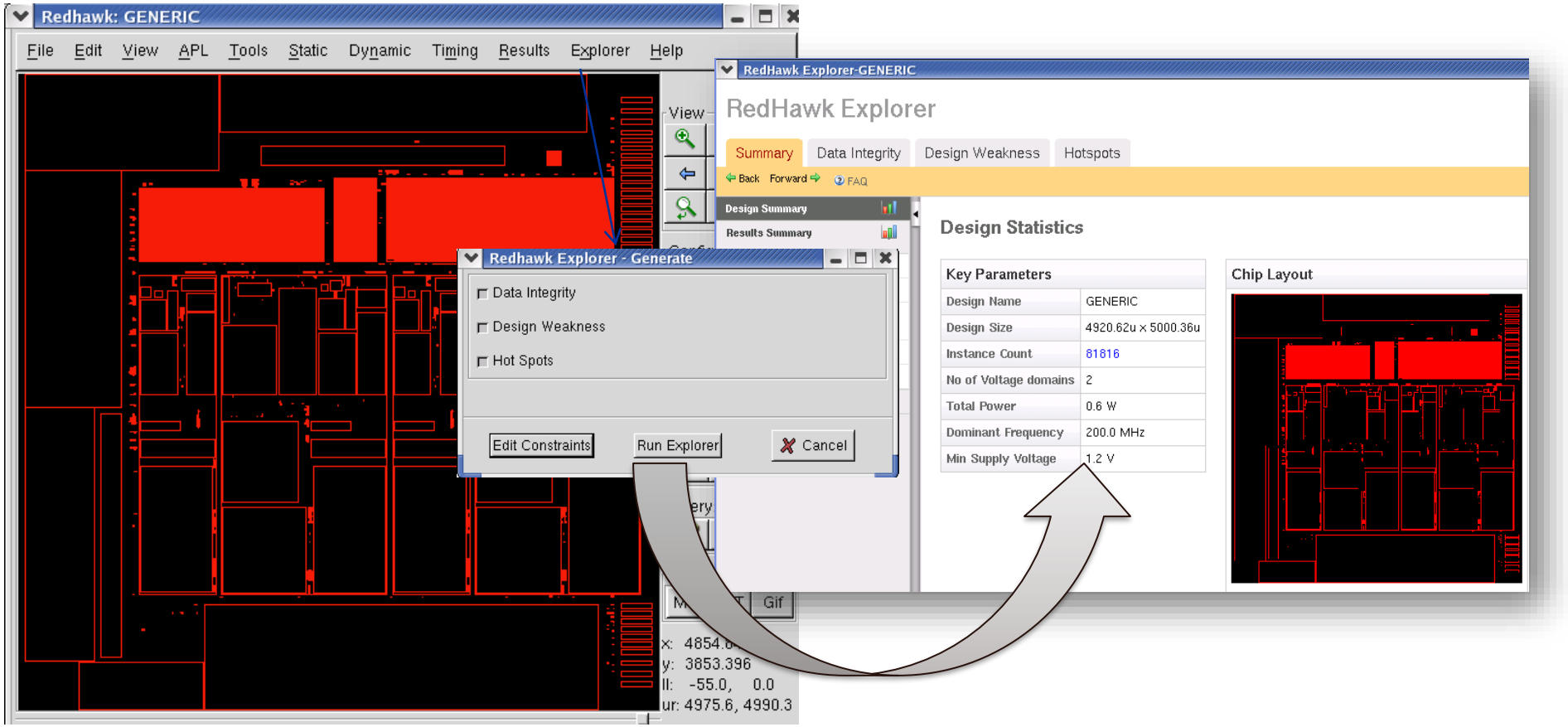
Ansys

RedHawk Explorer Goals

- Explorer is a tool which helps in locating, isolating, understanding and resolving design/data issues causing hot-spots
- Tightly integrated with Redhawk GUI – Provides easy cross-probing capabilities

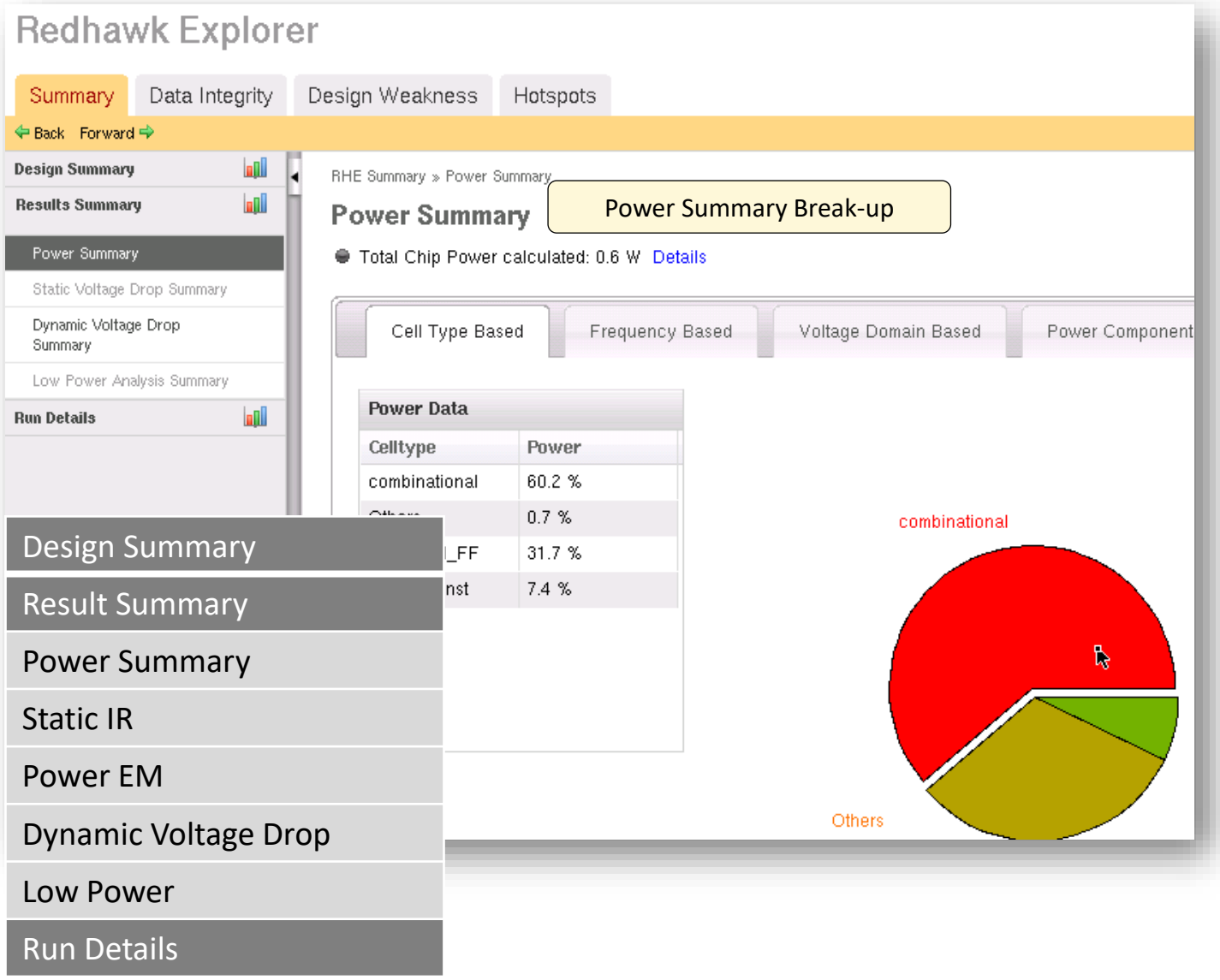


How do I run RedHawk Explorer ?



TCL Command: *explore design*
(can be executed at any stage after *"setup design")*

Summary Section



Power Summary Break-up

Design Summary

Result Summary

Power Summary

Static IR

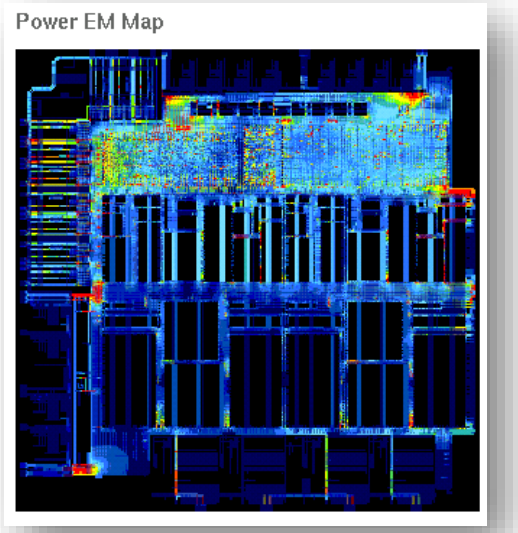
Power EM

Dynamic Voltage Drop

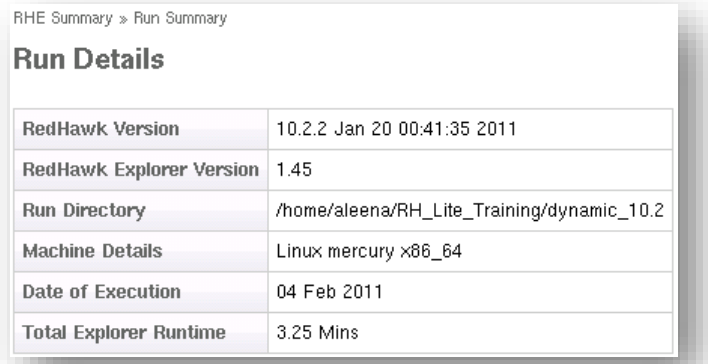
Low Power

Run Details

Various Maps



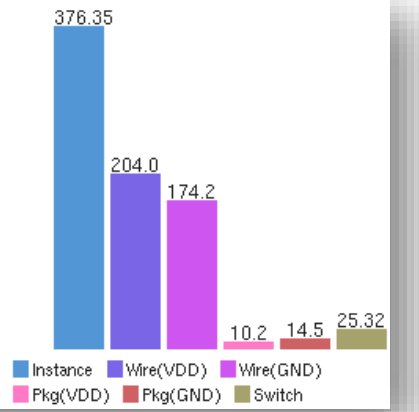
Run Details



Summary Section

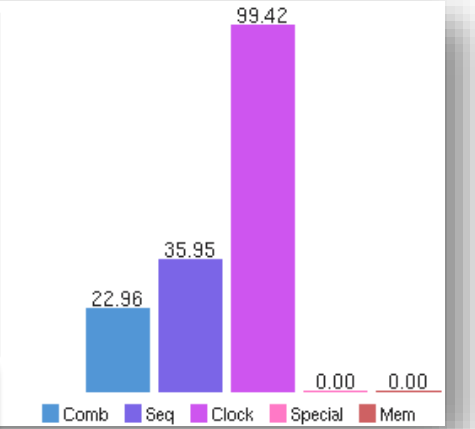
RHE Summary » DVD Summary

Worst Voltage Drop Data	
Parameter	**Value**
Instance	376.35 mV (31.36 %)
Wire(VDD)	204.0 mV (17.0 %)
Wire(GND)	174.2 mV (14.51 %)
Pkg(VDD)	10.2 mV (0.8 %)
Pkg(GND)	14.5 mV (1.2 %)
Switch	25.32 mV (2.11 %)



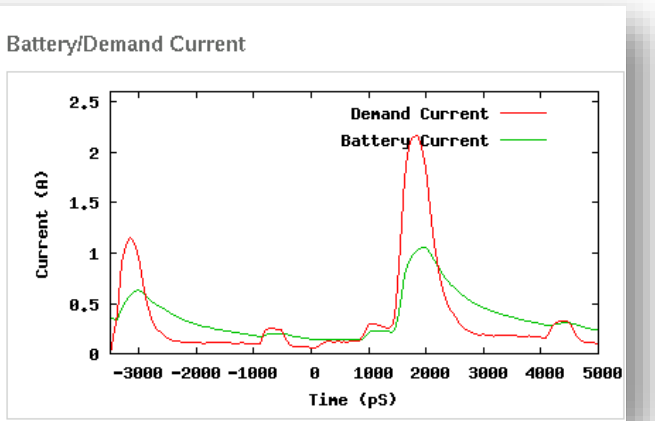
Voltage Drop Break up

Switching Activity	
Type	**Switching (%)**
Combinational	13077/56964 (22.96%)
Sequential	5948/16547 (35.95%)
Clock	7324/7367 (99.42%)
Special	0/0 (0.00%)
Memory/IP	0/0 (0.00%)
Total	26349/80878 (32.58%)

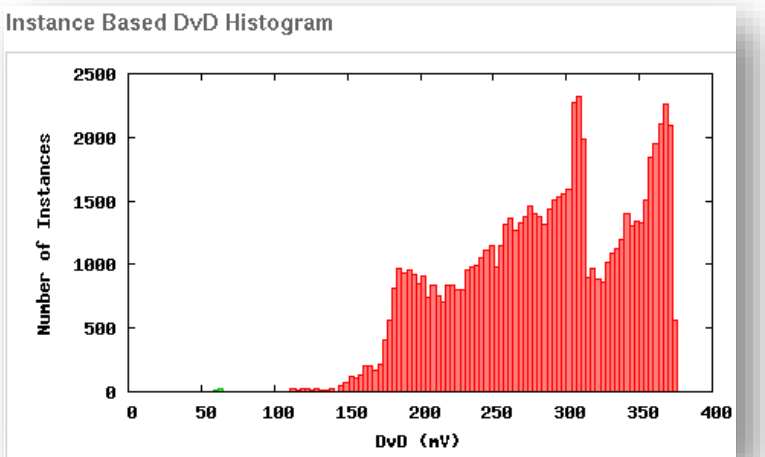


Tells what % of instances are switching in dynamic simulation

Waveform Data	
Type	**Peak Value (mA)**
Battery Current	1058.71
Demand Current	2170.39

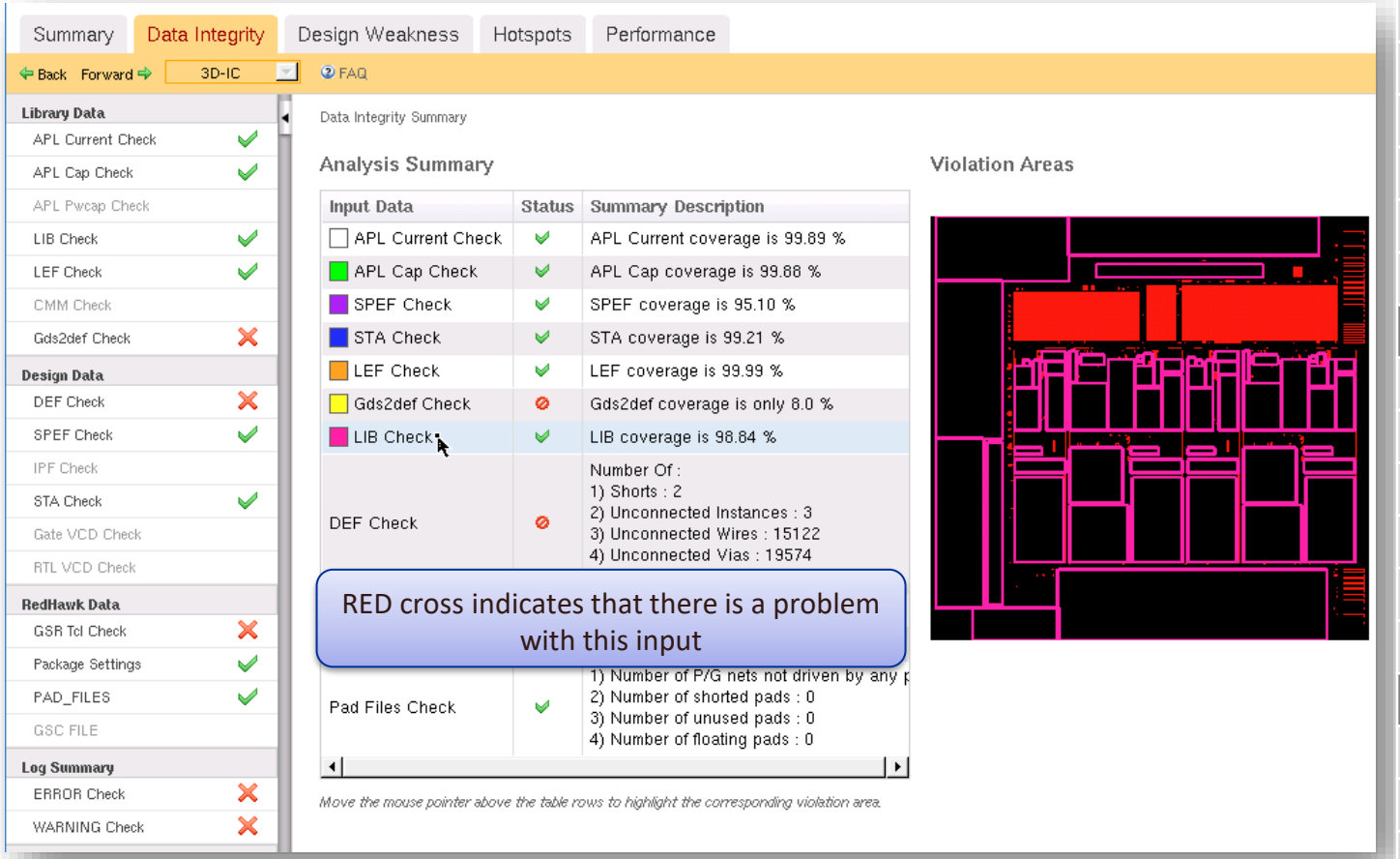


Demand Current and Battery current
Difference indicates decap current contribution



Shows Analysis Histograms

Data Integrity Check Summary



- Design specific data integrity check
- Helps to identify and understand impact of missing data
- Breaks design into regions and presents missing data for each region

Data Integrity Check Example : APL Cap Check

Data Integrity » Apl Cap Check

APL Coverage Details

Apl Cap Check

- Checks whether the APL Cap coverage in the design is at least 95%

- Number of instances with APL cap coverage: 80816/80917 (99.88 %)
- Number of cells with APL cap coverage: 199/234 (85.0 %)
- Apl Cap Area Coverage : 1.61722e+06/17342000.0 (9.32 %)

Highlights Regions with violations

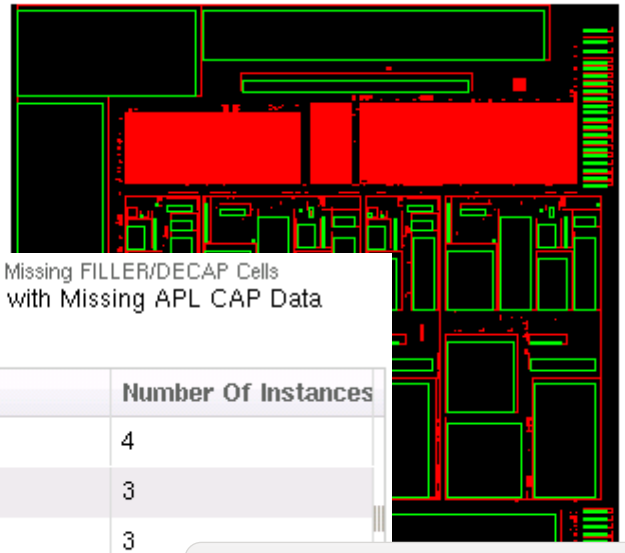
Celltype Wise Coverage | Cross Probing

Celltype Wise Apl Cap Coverage

CellType	% Coverage/Total
Memory	- % (-/-)
Combinational	99.86 % (56910/56989)
Sequential	99.95 % (16542/16550)
Clock	100.00 % (7364/7364)
Others	- % (-/-)
FILLER/DECAP	0.00 % (0/14)
Decap	- % (-/-)
Total	99.88 % (80816/80917)

Apl Cap Coverage Violations Displayed

Highlighting Regions with APL cap coverage less than 95 % in GUI



Data Integrity » Apl Cap Check » Missing FILLER/DECAP Cells

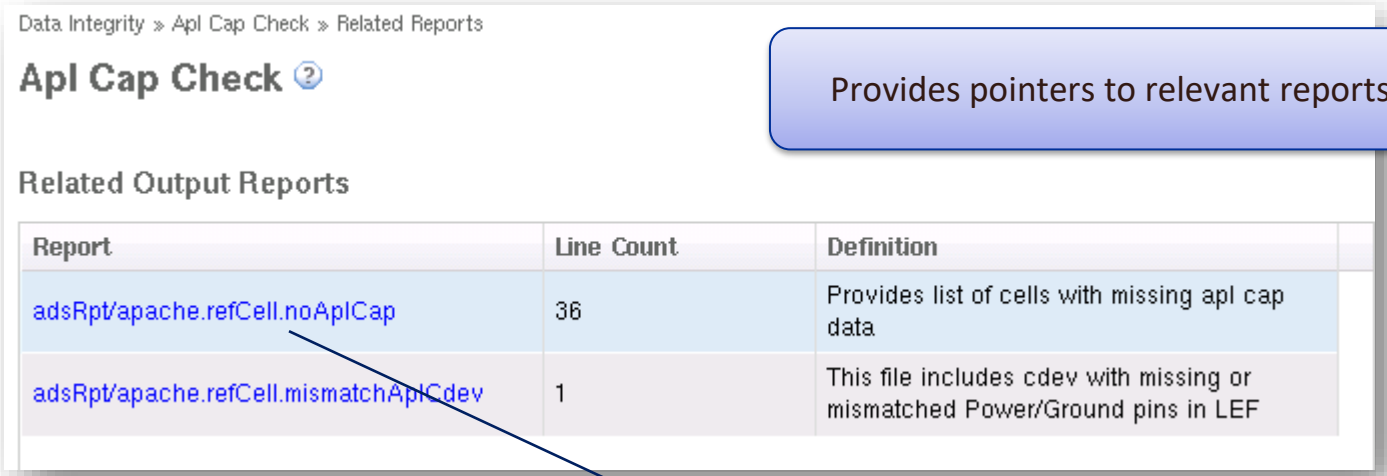
List of FILLER/DECAP Cells with Missing APL CAP Data

Cell	Number Of Instances
inst_92230_prog	4
cell_186	3
cell_189	3
inst_7642	2
inst_7644_prog	2

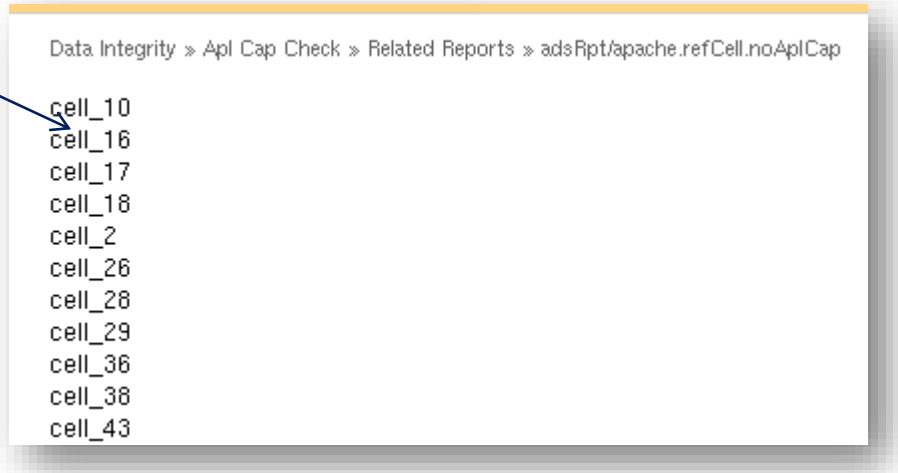
Provides cell-type wise classification

Provides a sorted list of cells based on number of instances

Related Output Reports Section

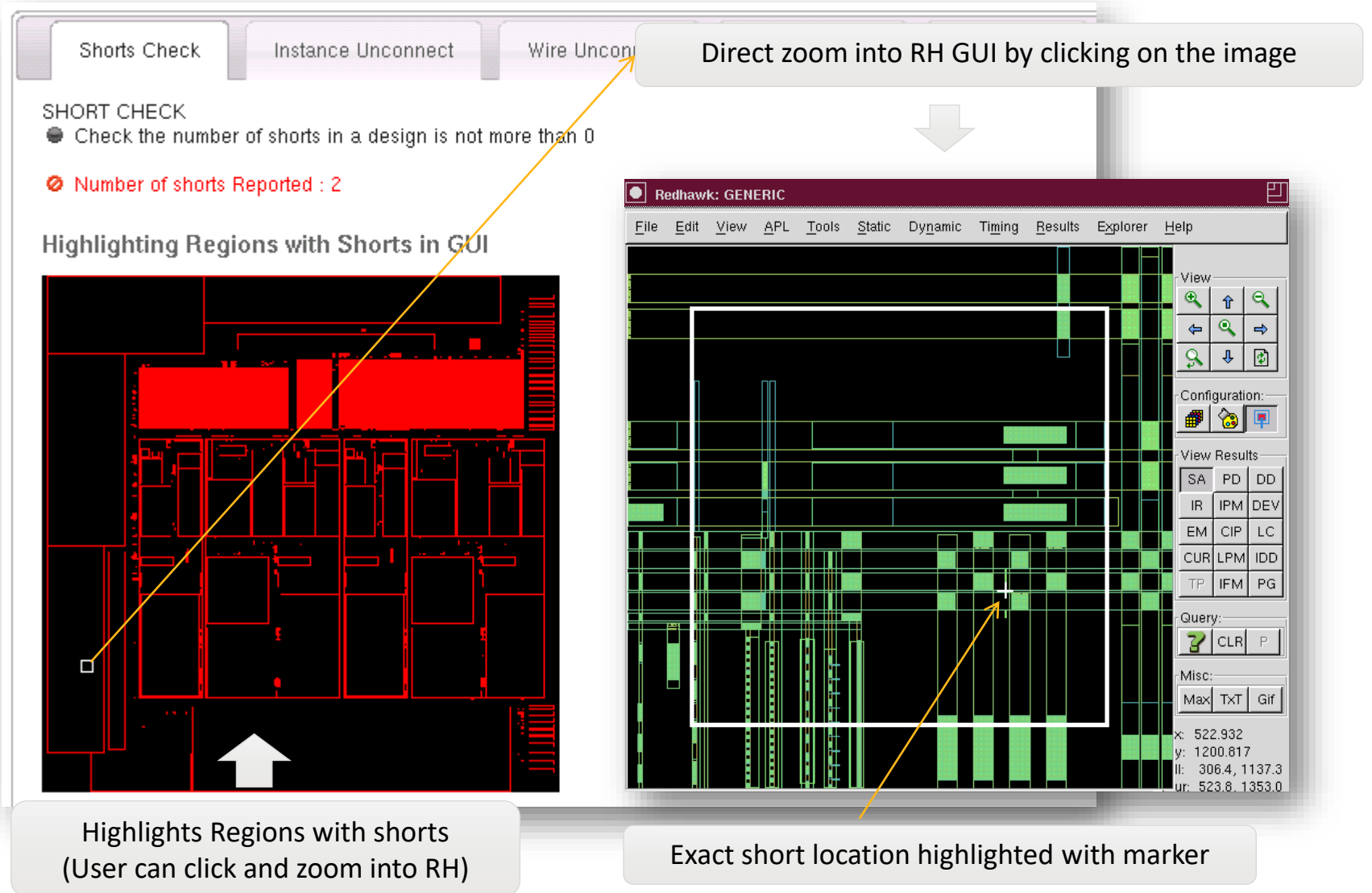


Provides pointers to relevant reports in adsRpt



- Presents relevant files in hyperlinked manner
- Describes and provides their content

DEF Check Example : Short Debug

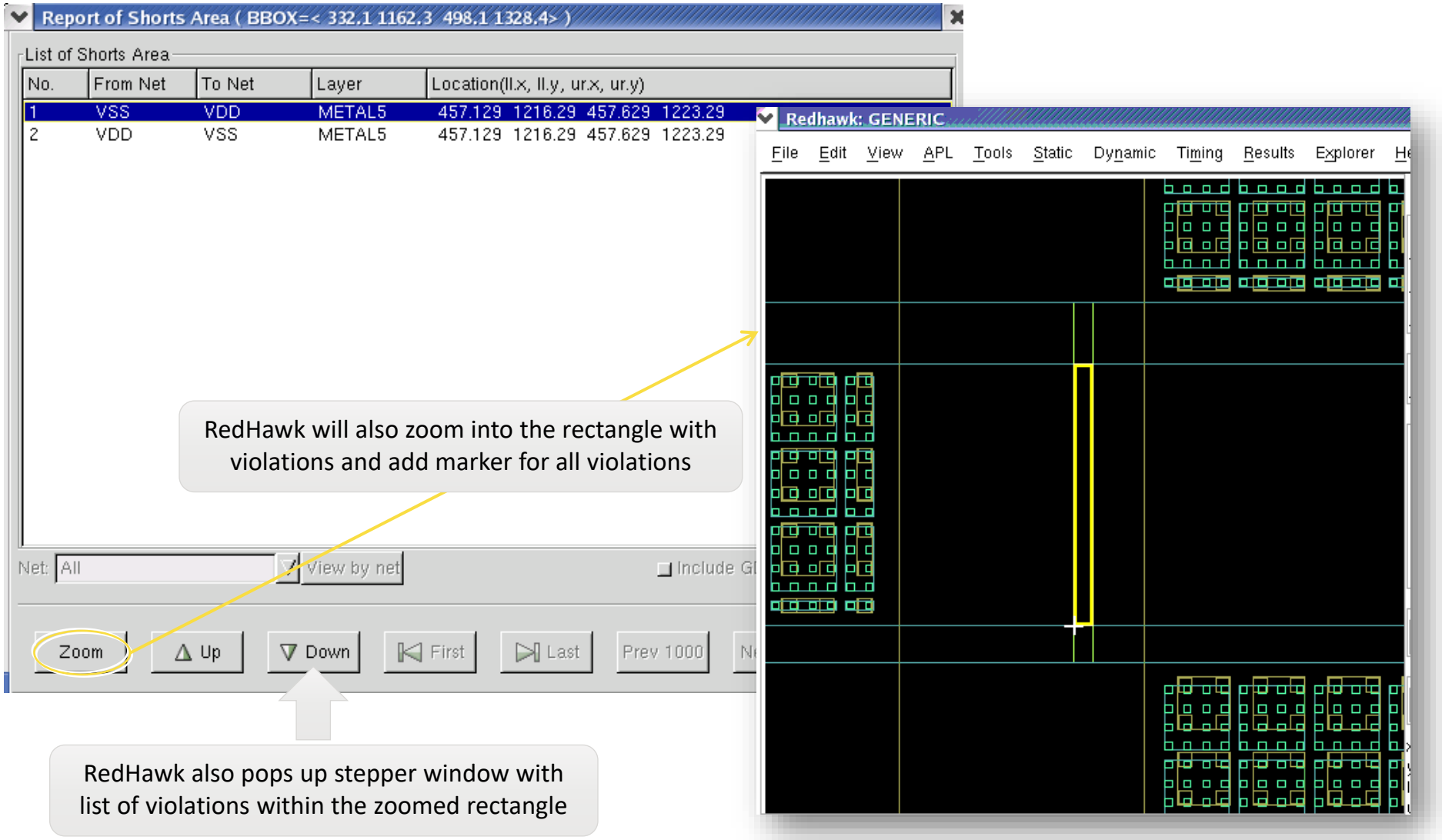


Direct zoom into RH GUI by clicking on the image

Highlights Regions with shorts
(User can click and zoom into RH)

Exact short location highlighted with marker

DEF Check Example : Short Debug



GSR / TCL Setting Checks

Data Integrity » GSR TCL Check

GSR TCL Check

Performs Checks on GSR/TCL Parameters

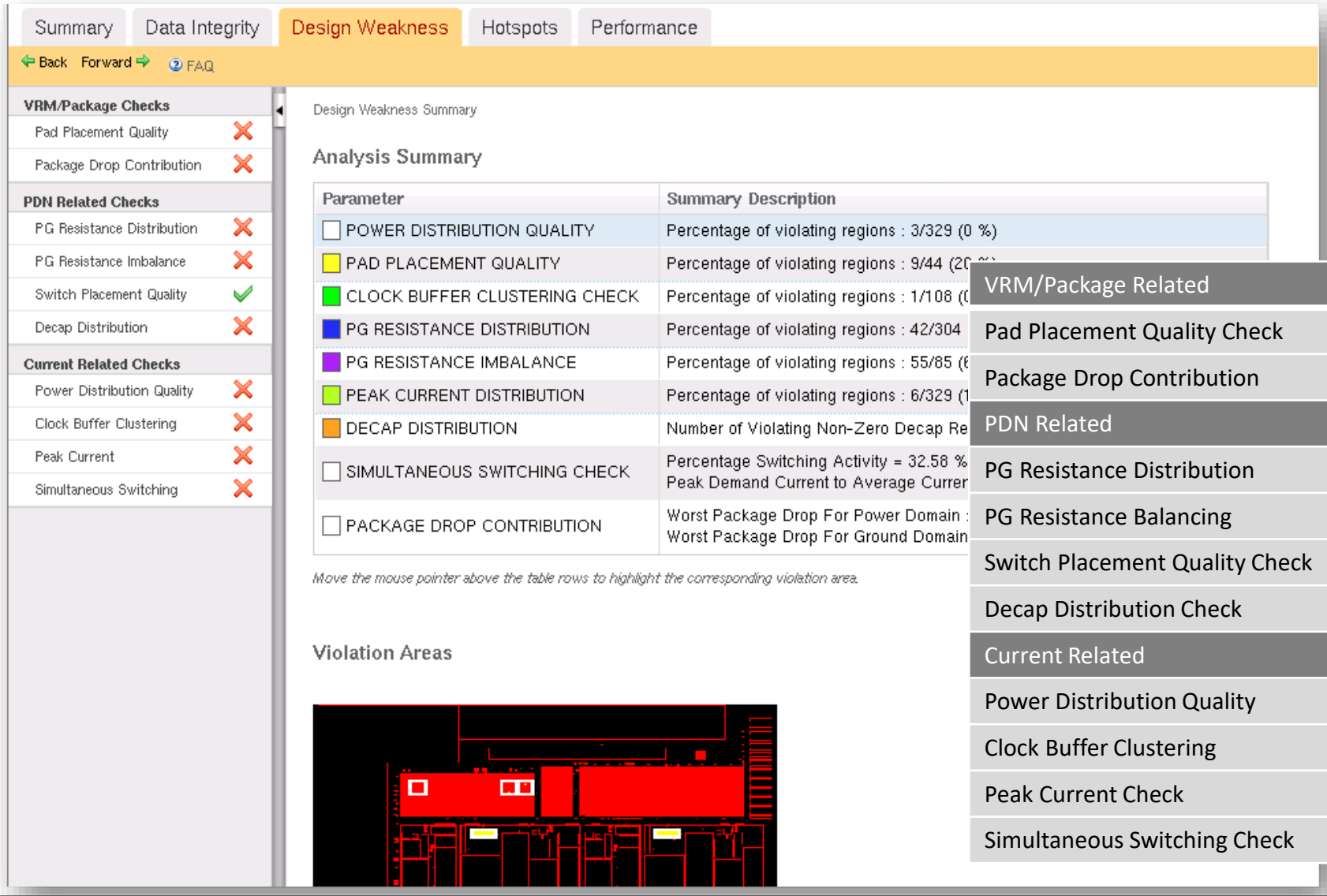
GSR ::Parameter	Given Value/Total	Recommended Value/Total	Status
GSR::DYNAMIC_SIMULATION_TIME	5.0 ns	> 5.0 ns	✓
GSR::DYNAMIC_TIME_STEP	25 ps	5 ps - 100 ps	✓
GSR::DYNAMIC_PRESIM_TIME	3 ns	1 ns - 50 ns	✓
GSR::FREQUENCY	200.0 MHz	~= 200.0 MHz	✓
GSR::CACHE_MODE	0	Set it to 1 if memory usage is a concern	✗
GSR::DYNAMIC_SAVE_WAVEFORM	1		
GSR: DECAP_CELLS	NOT GIVEN/COMMENTED		
GSR: INPUT_TRANSITION	3e-10		
GSR::TOGGLE_RATE	AVG_CLOCK_TOGGLE_RATE : 1.21 AVG_SIGNAL_TOGGLE_RATE : 0.24		

Related GSR Keywords

GSR Keyword	Status
BLOCK_POWER_FOR_SCALING	DETAILS
BLOCK_POWER_FOR_SCALING_FILE	-
BLOCK_POWER_ASSIGNMENT	-
INSTANCE_POWER_FILE	-
TOGGLE_RATE	0.15
INSTANCE_TOGGLE_RATE	-
INSTANCE_TOGGLE_RATE_FILE	-
BLOCK_TOGGLE_RATE	-
BLOCK_TOGGLE_RATE_FILE	-
SCALE_CLOCK_POWER	0
SCALE_TOGGLE_RATE	0
VCD_FILE	-
GSC_FILE	-
GSC_OVERRIDE_IPF	0
STATE_PROPAGATION	-
BLOCK_VCD_FILE	-
BLOCK_TOGGLE_FILE	-

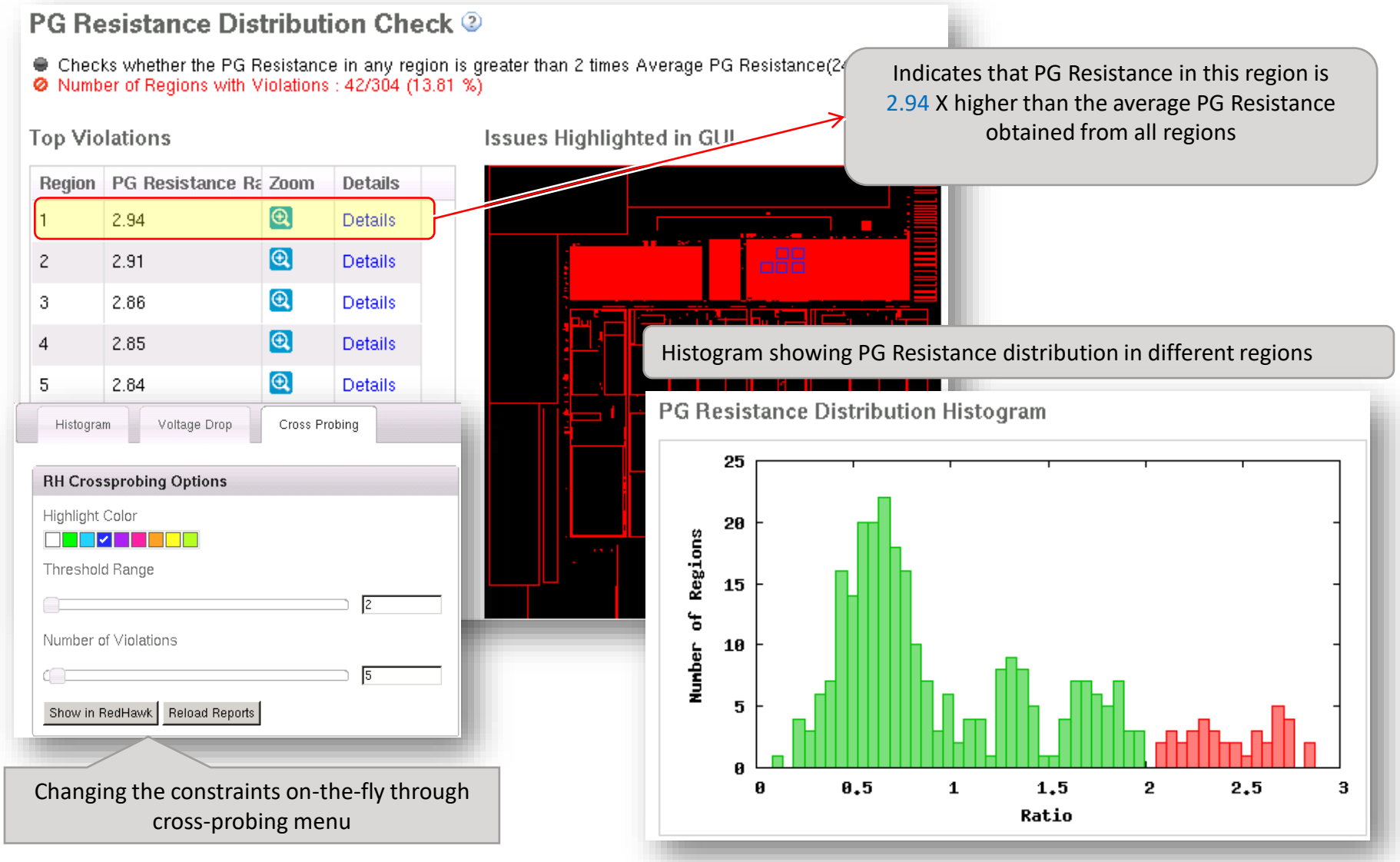
Common mistakes made in GSR/TCL are identified here

Design Weakness Exploration



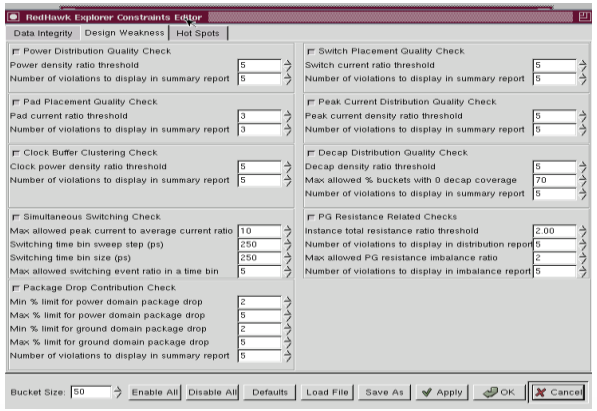
VRM/Package Related
Pad Placement Quality Check
Package Drop Contribution
PDN Related
PG Resistance Distribution
PG Resistance Balancing
Switch Placement Quality Check
Decap Distribution Check
Current Related
Power Distribution Quality
Clock Buffer Clustering
Peak Current Check
Simultaneous Switching Check

Design Weakness Analysis Example : PG Resistance Distribution Check

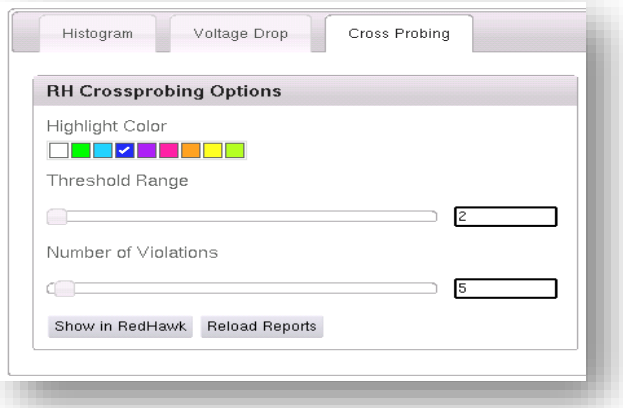


Changing the Constraints

Using constraint editor
(Before running RHE)



Using RHE GUI
(After running RHE)



Using Text Editor
(Before running RHE)

- vi adsRHE/rhe_threshold.rpt
- Edit the constraints you want
- explore design –constraint_file <new_thresh_file>

```
set rhe_bucket_size 50
set rhe_enable_DWE 1
set rhe_enable_DIE 1
set rhe_enable_HSE 1
set rhe_dvd_check_type minWC

############################## DWE Thresholds ########


# Power_distribution_quality_check
# Checks whether the power density in any bucket is


set rhe_enable_power_distribution_check 1
set rhe_bucket_power_density_ratio 5
set rhe_num_violations_power_density_max 5
```

Cross-probing violations in RedHawk GUI

PG Resistance Distribution Check

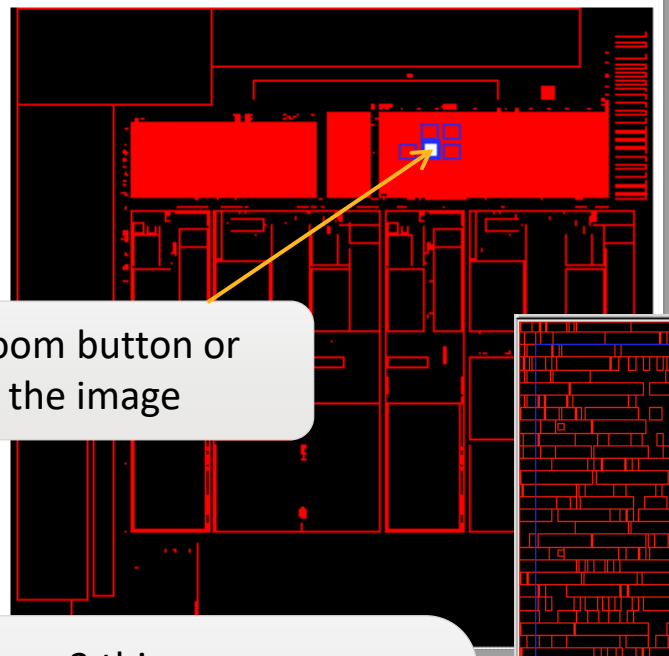
Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.350 ohm)
Number of Regions with Violations : 42/304 (13.81 %)

Top Violations

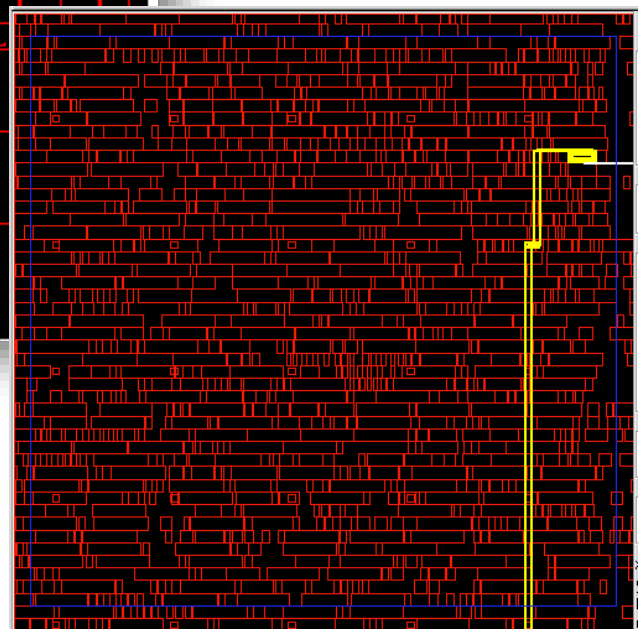
Region	PG Resistance Ra	Zoom	Details
1	2.94		Details
2	2.91		Details
3	2.86		Details
4	2.85		Details
5	2.84		

Move the mouse pointer
to highlight the correspo

Issues Highlighted in GUI



User can click on zoom button or directly click on the image

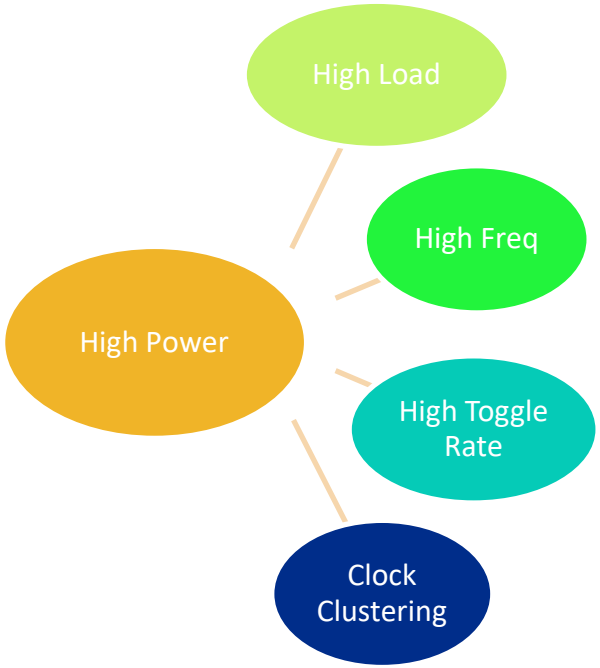


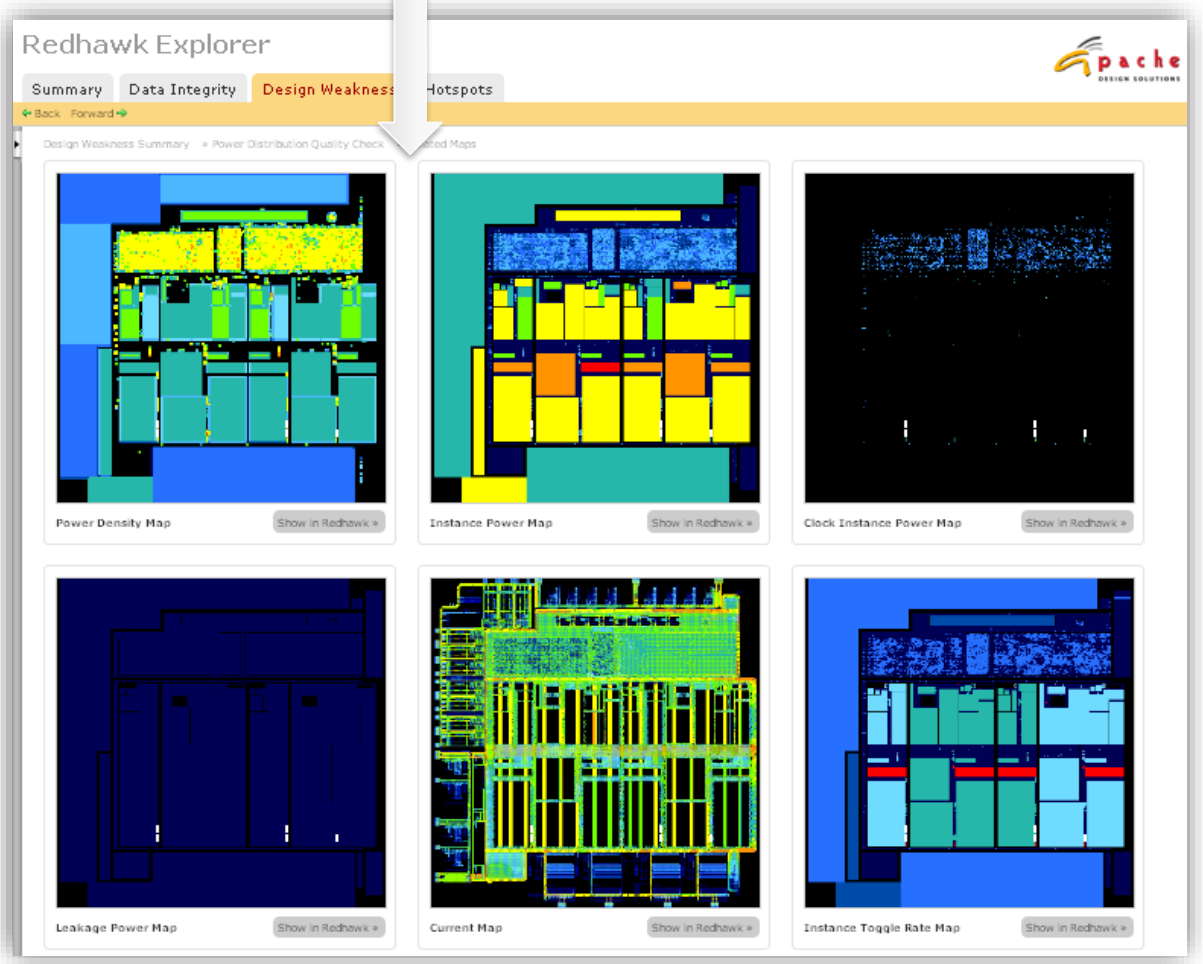
When you click on the image, RH/RHE does 3 things:

- Zooms into the violating regions
- Highlights the worst instance within the regions
- Update the map with some relevant views
  - Example, PG resistance map will display SPT for the worst instance

Design Weakness Analysis : Related Maps Section

Design Weakness -> Power Distribution Quality -> Related Maps



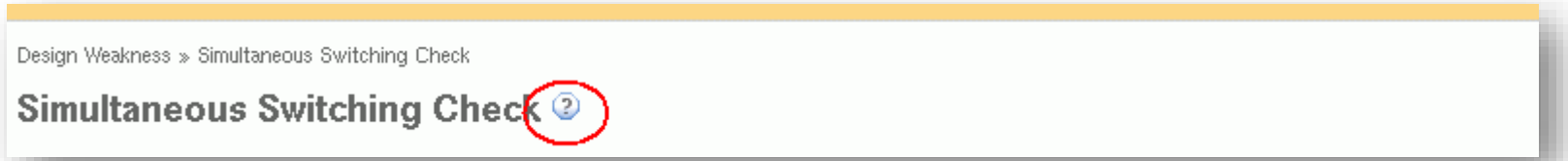


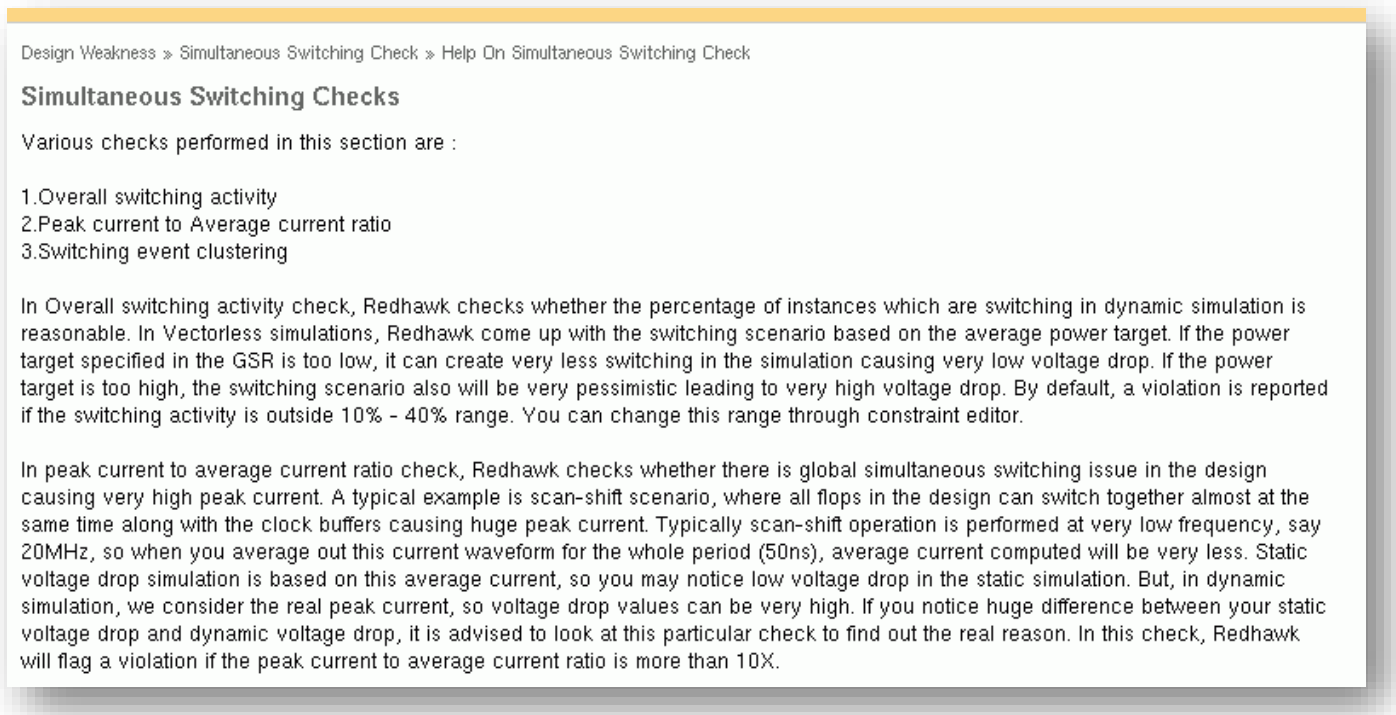
Related maps section helps identifying the exact cause for a weakness

Q & A Session

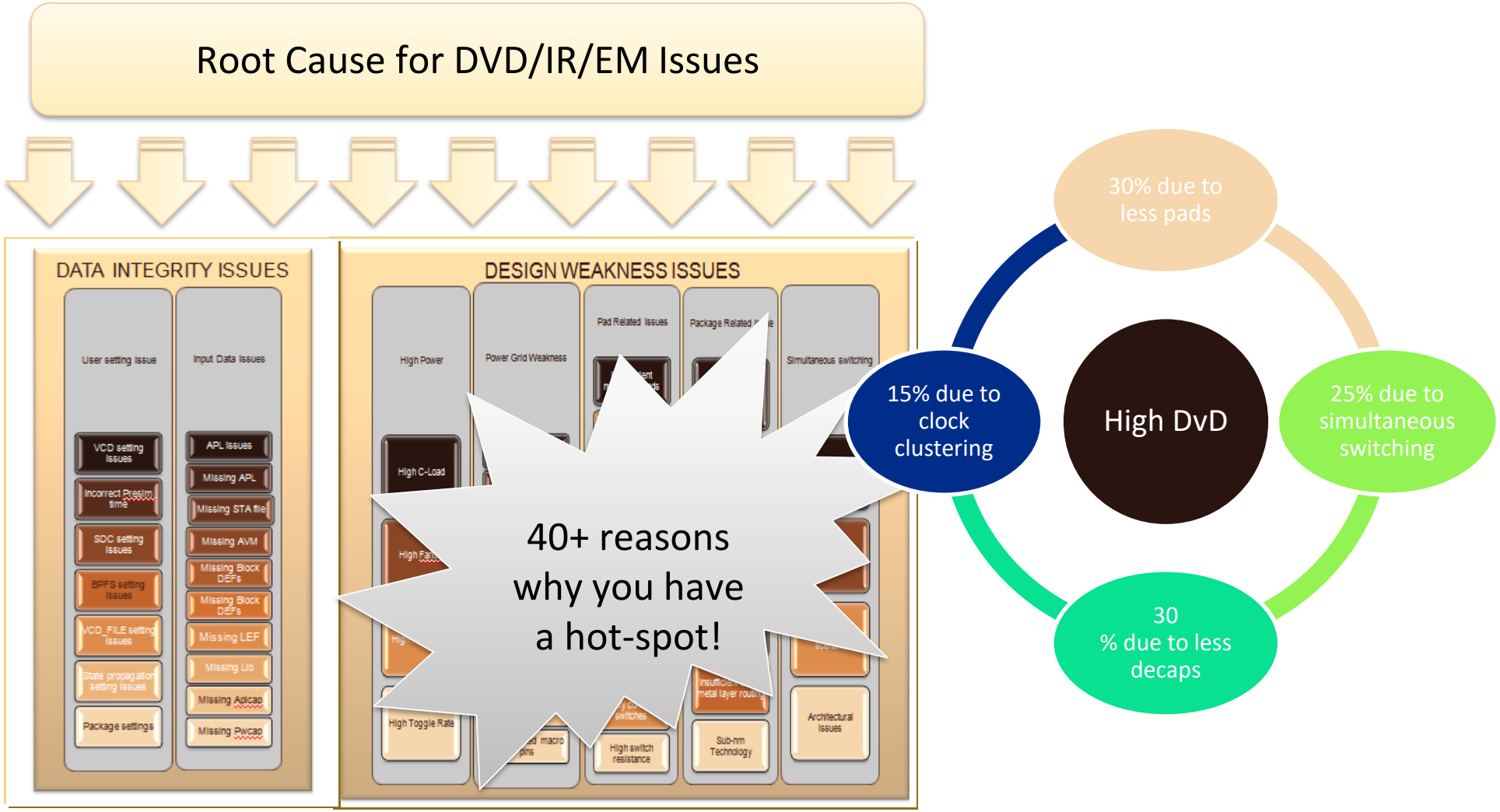
Ansys

Getting Help on a Specific Item

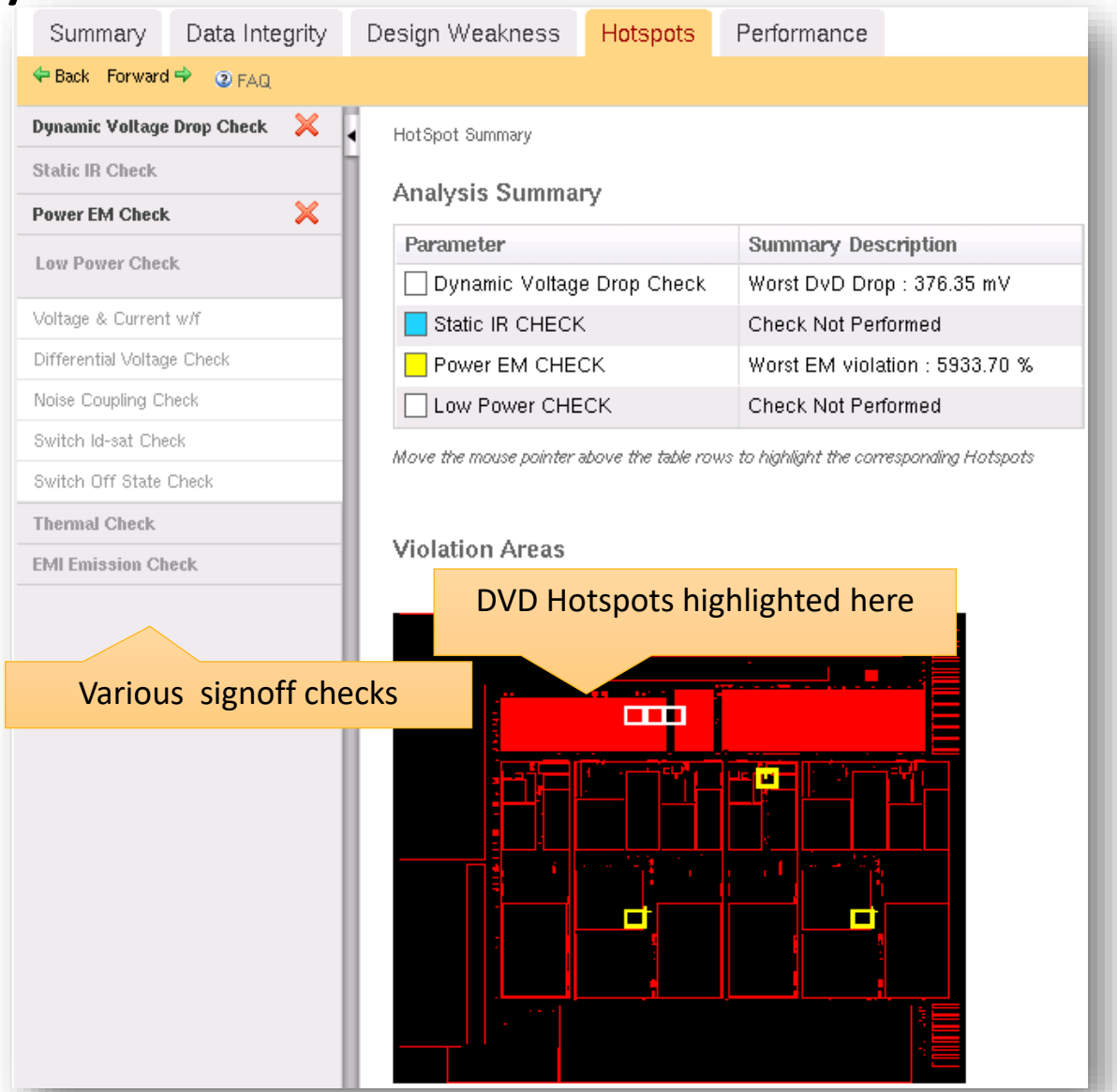




Power Noise : Root Cause Identification



Hot Spot Analysis



Hot Spot Analysis

RedHawk Explorer

Summary | Data Integrity | Design Weakness | Hotspots | Performance

Back Forward FAQ

- Dynamic Voltage Drop Check
- Static IR Check
- Power EM Check
- Low Power Check
- Voltage & Current w/f
- Differential Voltage Check
- Noise Coupling Check
- Switch Id-sat Check
- Switch Off State Check
- Thermal Check
- EMI Emission Check

Hot Spot Summary » DvD Check

DvD Check

- Dynamic Hot Spot Exploration
- Analysis Type : minWC
- Highlighting Top 3 DVD Hot spots in the design
- DVD Threshold used for PASS/FAIL : 100 mV

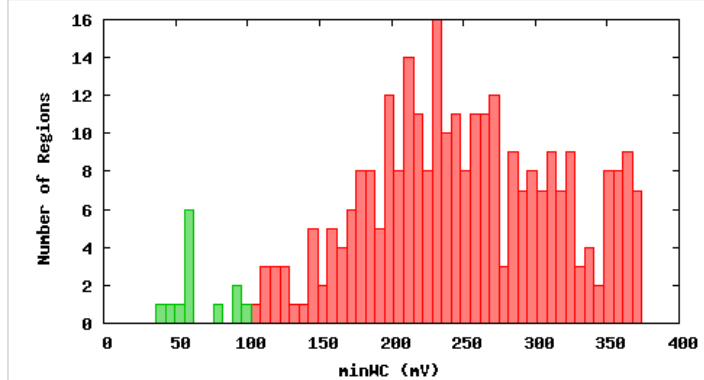
Driven by Pass/Fail Criteria

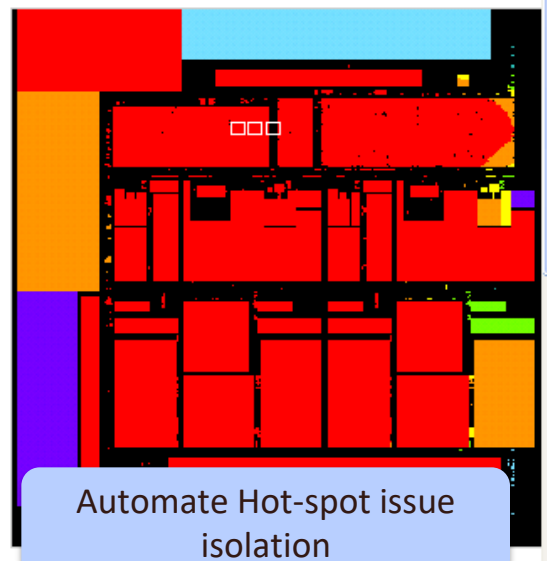
- Number of failing regions : 287/300 (95.66 %)
- Number of failing instances : 75568/75614 (99.9392 %)

Top Violations

Region	Drop (mV)	Failed Instances	Status
Hot Spot : 1	376.35 (31.36 %)	993/993 (100.0 %)	✗
Hot Spot : 2	375.29 (31.27 %)	377/377 (100.0 %)	✗
		884/884 (100.0 %)	✗

DvD Distribution Histogram

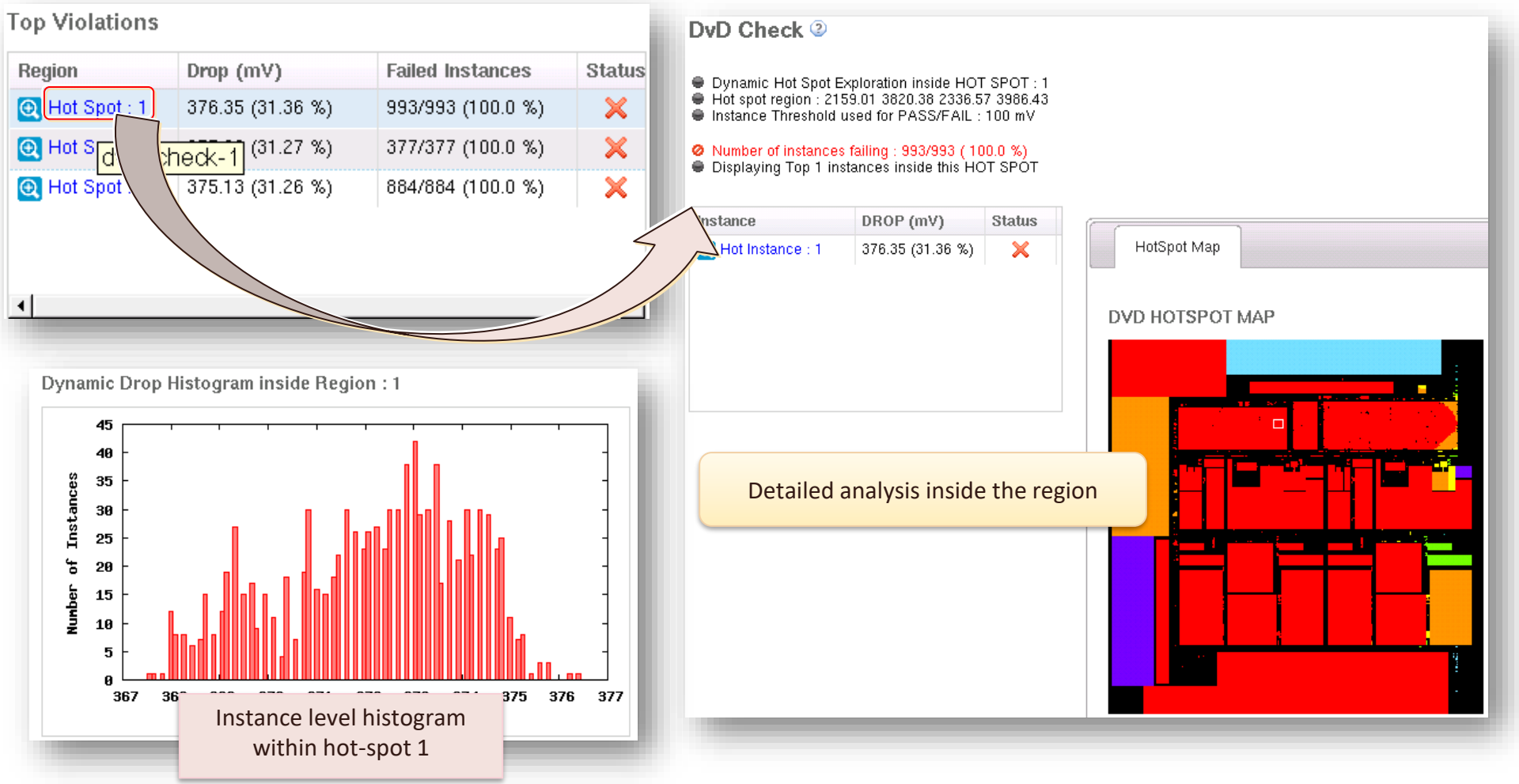




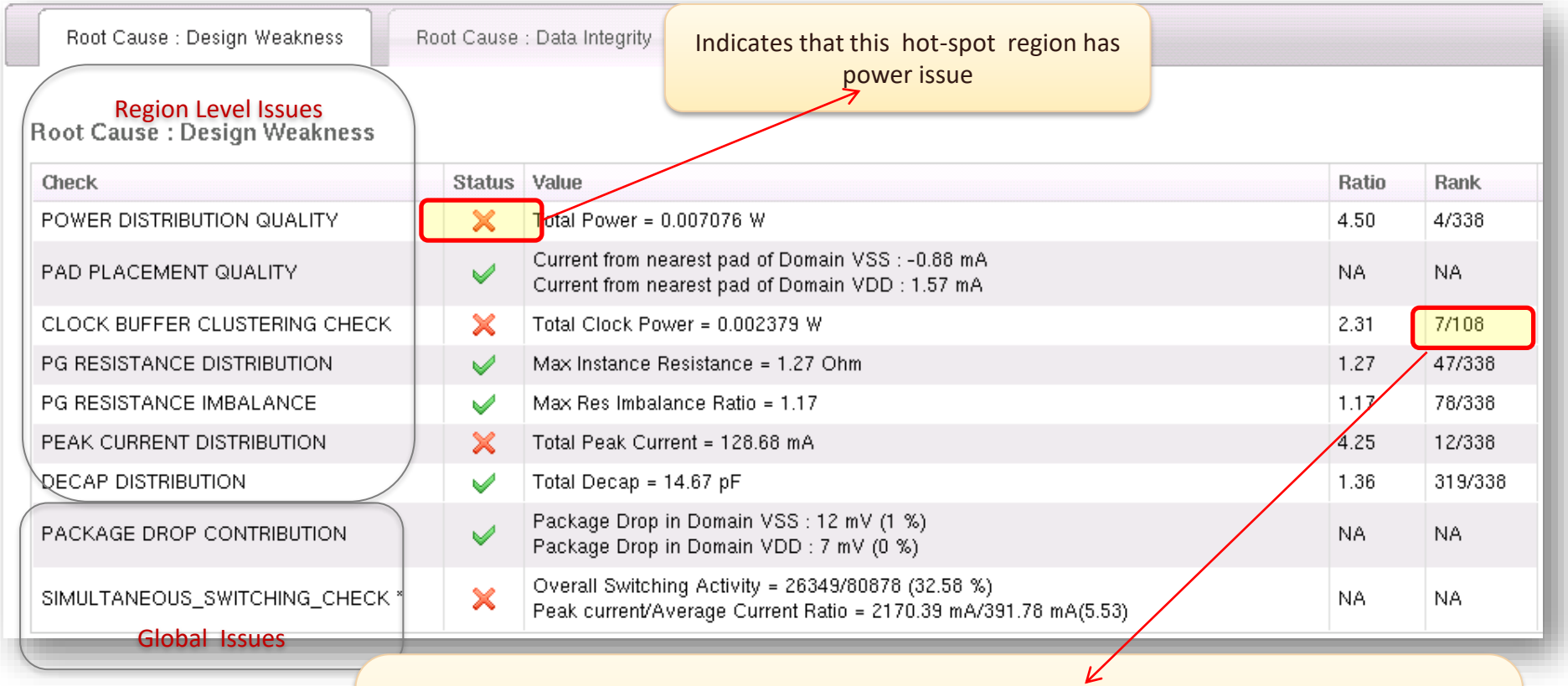
Automate Hot-spot issue isolation

Show in RedHawk »

Hot Spot Analysis : Checking Hot-spot #1



Root Cause Identification : Design Weakness Analysis



Check	Status	Value	Ratio	Rank
POWER DISTRIBUTION QUALITY	✗	Total Power = 0.007076 W	4.50	4/338
PAD PLACEMENT QUALITY	✓	Current from nearest pad of Domain VSS : -0.88 mA Current from nearest pad of Domain VDD : 1.57 mA	NA	NA
CLOCK BUFFER CLUSTERING CHECK	✗	Total Clock Power = 0.002379 W	2.31	7/108
PG RESISTANCE DISTRIBUTION	✓	Max Instance Resistance = 1.27 Ohm	1.27	47/338
PG RESISTANCE IMBALANCE	✓	Max Res Imbalance Ratio = 1.17	1.17	78/338
PEAK CURRENT DISTRIBUTION	✗	Total Peak Current = 128.68 mA	4.25	12/338
DECAP DISTRIBUTION	✓	Total Decap = 14.67 pF	1.36	319/338
PACKAGE DROP CONTRIBUTION	✓	Package Drop in Domain VSS : 12 mV (1 %) Package Drop in Domain VDD : 7 mV (0 %)	NA	NA
SIMULTANEOUS_SWITCHING_CHECK *	✗	Overall Switching Activity = 26349/80878 (32.58 %) Peak current/Average Current Ratio = 2170.39 mA/391.78 mA(5.53)	NA	NA

Design Weakness Ranking

This hot-spot region ranks 7 among all regions in the design based on Total Clock Power
(Rank-1 indicates the weakest region)

Root Cause Identification : Data Integrity Checking

Region Level Data Integrity Analysis

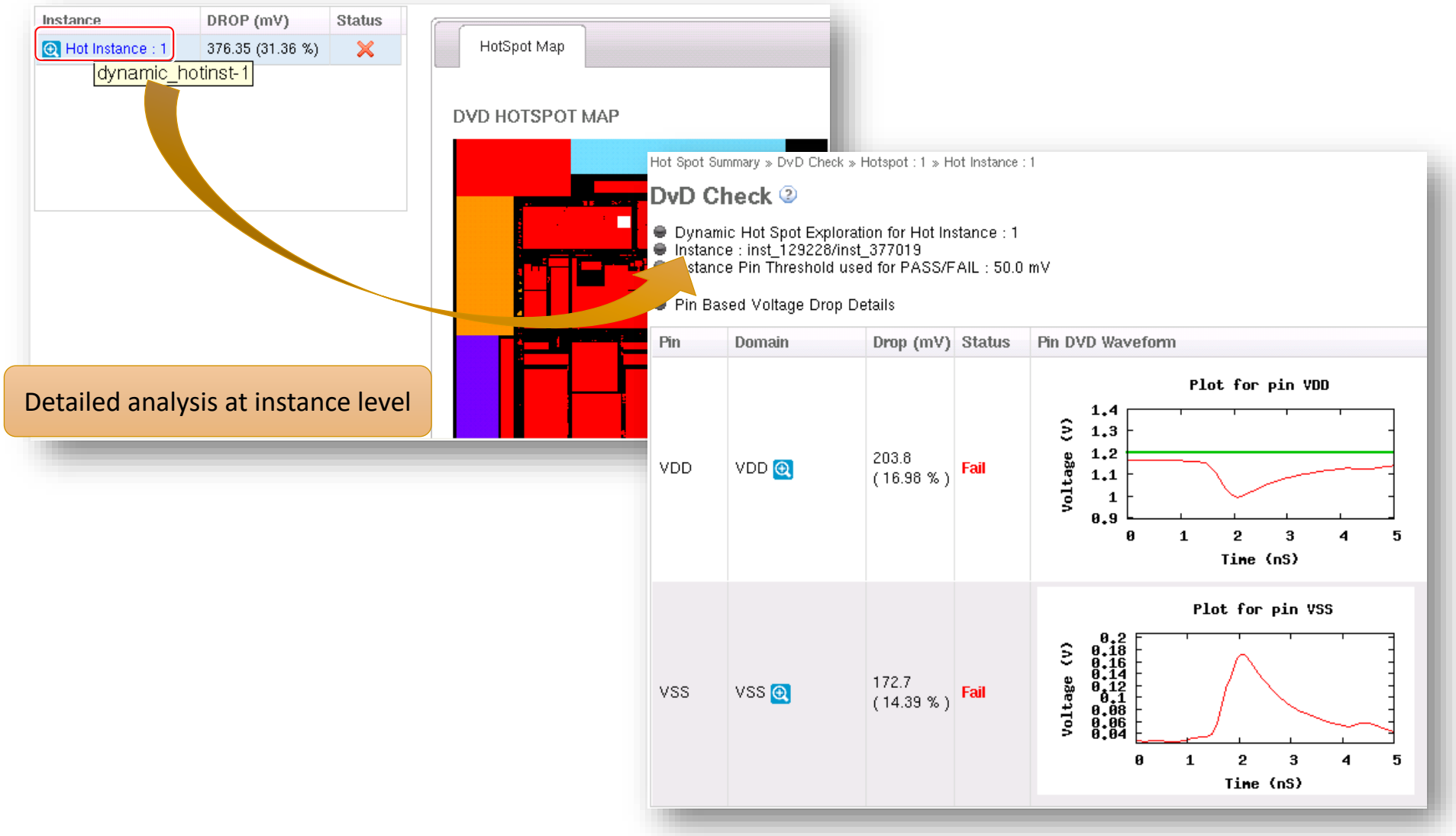
Root Cause : Design Weakness | Root Cause : Data Integrity | Histogram

Root Cause : Data Integrity

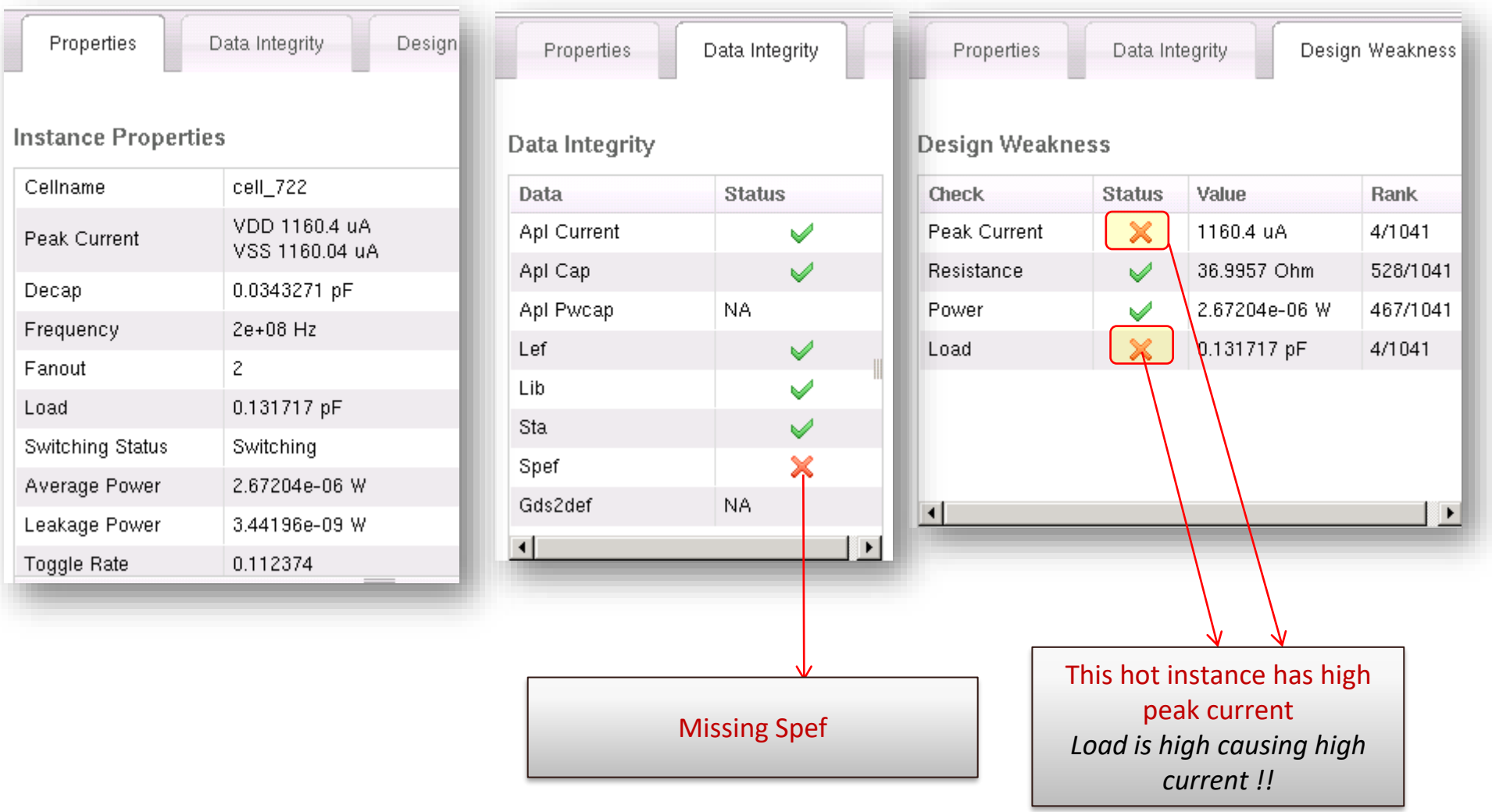
Check	Result	Value	Percentage
APL CURRENT CHECK	✓	1035/1041	99.42
APL CAP CHECK	✓	1041/1041	100.00
SPEF CHECK	✓	968/1041	92.99
STA CHECK	✓	1034/1041	99.33
LEF CHECK	✓	1041/1041	100.00
LIB CHECK	✓	1041/1041	100.00

SPEF coverage in this region is only 93 %

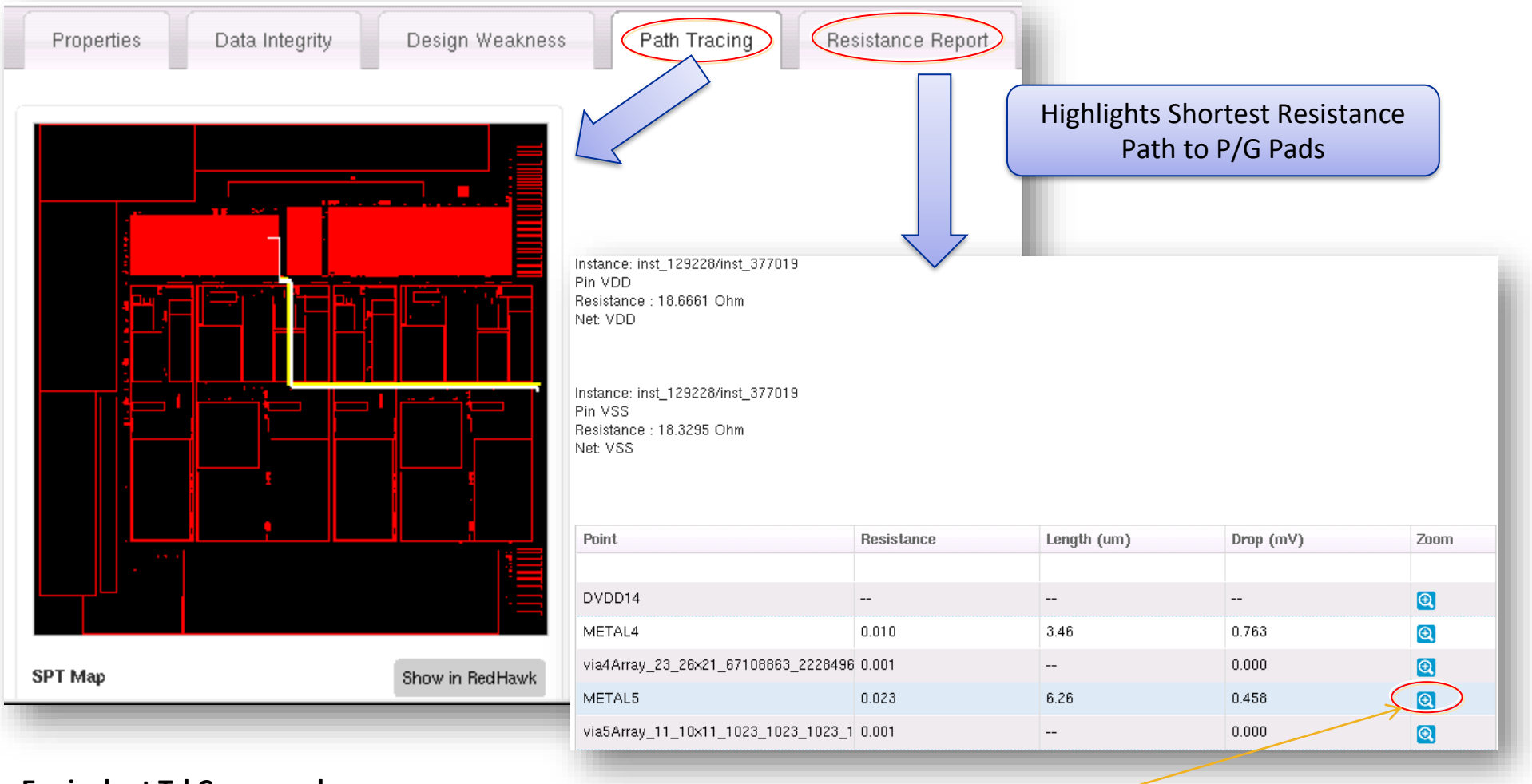
Hot Spot Analysis at Instance Level



Hot Spot Analysis : Instance Level Debug



Shortest Path Tracing



Highlights Shortest Resistance Path to P/G Pads

Equivalent Tcl Command:

perform min_res_path –o res_path.rpt

User can directly zoom into the bottleneck segments

Explorer Command Line Options and Log Details

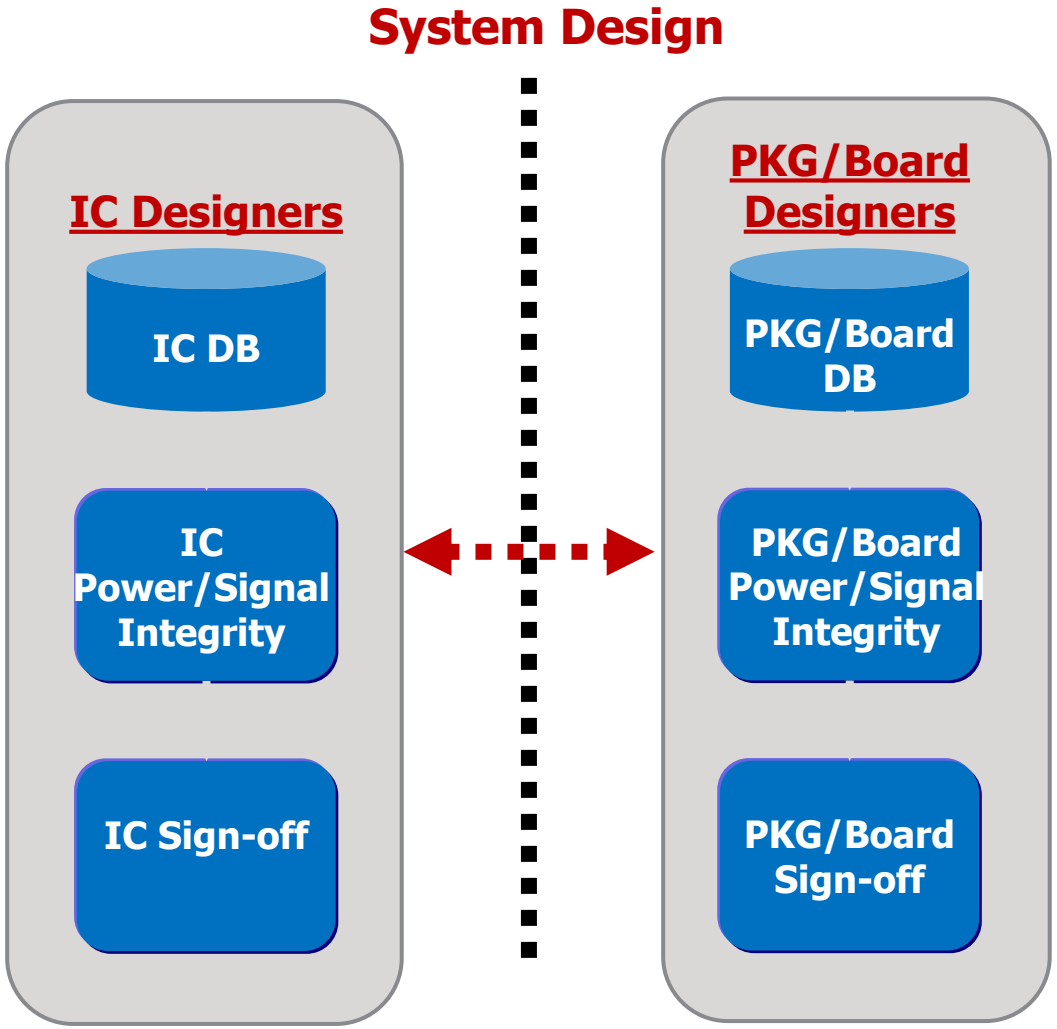
Command	Description
explore design	Runs Explorer and Pops up GUI
explore design -view	Pops up Explorer GUI
explore design -off	Closes Explorer GUI
explore design –constraint_file <cons_file>	Runs Explorer with a user specified constraint file

Log File	Description
adsRHE/adsRHE.log	Central summary Log
adsRHE/adsDWE/adsDWE.log	Design Weakness Analysis Log
adsRHE/adsDIE/adsDIE.log	Data Integrity Analysis Log
adsRHE/adsHSE/adsHSE.log	Hot Spot Analysis Log

Chip Power Model (CPM) generation and Chip-Package-System(CPS) analysis

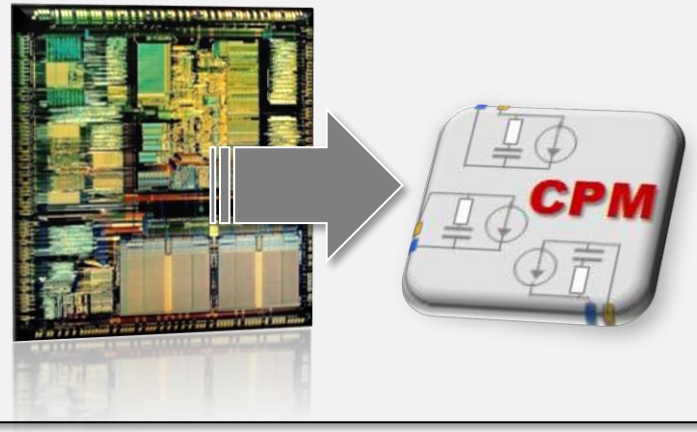
Ansys

IC-Package-PCB Co-Design Challenges



- Longer System Design Cycle
  - Chip is the source of noise
  - Lack of noise budgeting at board & package
  - Possible die-package resonance
  - Package re-spin
- Higher PKG / Board Cost
  - Over-design
  - Excessive decap

What's in a CPM?



- ✓ Cdie/Rdie for every domain
- ✓ I(t) for every domain
- ✓ Open SPICE netlist format

- VCD based and Vectorless switching scenario
- Multi-domain, distributed model
- Full chip frequency domain simulation and model order reduction
- DC to multi-GHz validity
- Silicon correlated

Ansys's CPS Solutions

RedHawk Totem

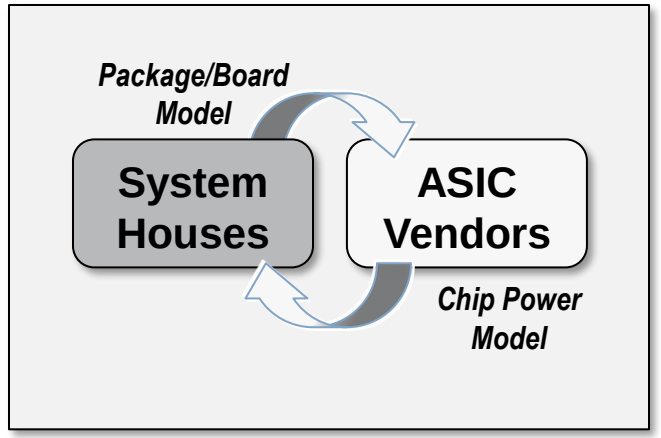
Package/PCB Aware PDN Sign-off
CPM Generation

CPM

S-Parameter
RLCK

SiWave

Chip-Package-System AC, DC, Trans
EMI/EMC
SSO Timing Analysis
Thermal Integrity



Chip Power Modeling Flow

```
# Import data
import gsr GENERIC.gsr
setup design

# Calculate power
perform pwrcalc

# Power grid extraction
perform extraction -power -ground -c

# Package, wirebond, pad setup
setup pad
setup package
setup wirebond

# CPM Creation
perform pwrmodel -nx 5 -ny 5 -o design.cpm
```

Exactly same inputs and steps used in dynamic simulation (Add keyword GENERATE_CPM 1 in GSR ; Package netlist is ignored)

CPM Generation Command

Distributed Machine Processing (DMP) for large designs

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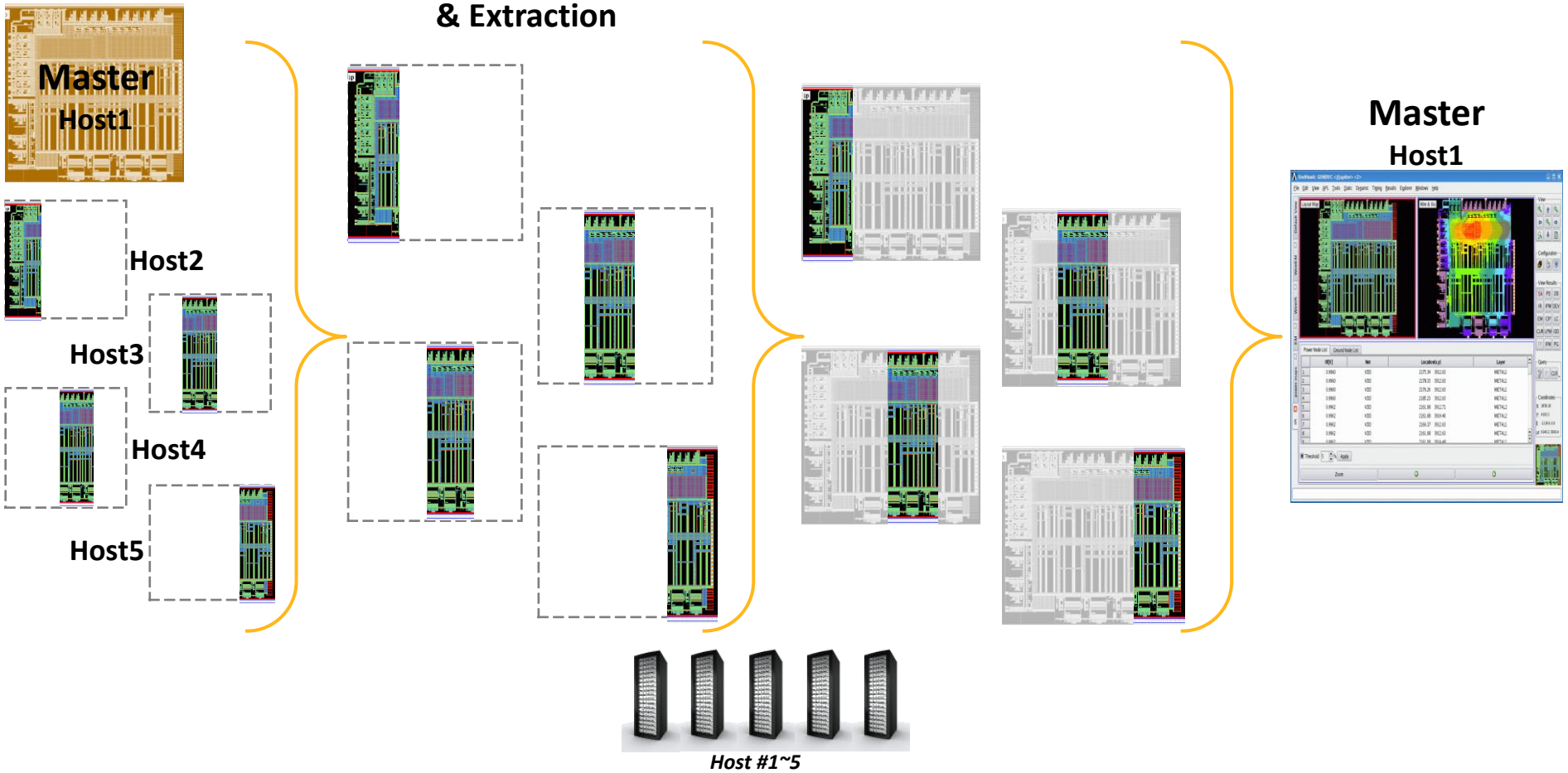
DMP Flow

Step 1:
Distributed Setup Design

Step 2:
Distributed Power Calculation & Extraction

Step 3:
Distributed Simulation

Step 4:
Unified Result Analysis



Launching RedHawk DMP

- Command to launch DMP
  - redhawk -lmwait -dmp <DMP_Config_file> -f <tcl_command_file>
  - DMP config file is required to provide information like Number of partitions, Grid type, launch constraints etc.
  - Sample DMP Config file:

    NUMBER_OF_JOBS 16

    GRID_TYPE **LSF/SSH/RTDA/SGE**

    QUEUE_NAME dmp_queue

    ARGUMENTS_FOR_LARGE_JOBS " -q dmp_queue -R "rusage[mem=130000]“
- No other changes required in GSR/Tcl files

Q & A Session

- QA session will be for 15 mins
- For queries which are unanswered by end of this session , please email to dileesh.jostin@ansys.com or contact local Ansys AE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