Table of Contents

1. Introduction

This application note describes several methods in Redhawk to identify issues causing high static or dynamic voltage drop in the design. It explains you how effectively you can use the GUI features in Redhawk to identify the PG design issues.

2. What are the different reasons which can cause high voltage drop in my design?

If your design is showing high static or dynamic voltage drop, it could be due to one of the following reasons:

- High current flowing through the power grid: Can affect static as well as dynamic drop.
- High PG grid impedance: Can affect static as well as dynamic.
- High Package parasitics: Can affect static as well as dynamic.
- Insufficient number of voltage sources: Can affect static as well as dynamic.
- Inadequate amount of decaps available: Can affect only dynamic.
- Simultaneous switching: Can affect only dynamic.

2a. How do I find out whether the drop is caused by high current flowing through the PG grid?

Static or dynamic voltage drop is proportional to the current flowing through the power grid. In static analysis, high average current can cause high drop. Similarly in dynamic analysis, high transient current can lead to high voltage drop.

Average current is proportional to the average power of the design. High average power can affect both static and dynamic voltage drop results. Redhawk power summary report file (adsRpt/power_summary.rpt) will give you the details of power consumption of the design. Power summary report will give you the power consumption for each voltage domain, frequency domain and for each cell type in the design.

Instance power file (adsRpt/<design>.power.rpt) will contain instance specific power values. You can also click on any instance in the GUI to get more details of power calculation for that instance. In Redhawk GUI, you can see the sorted list of high power instances in the design using "Results -> List of Highest Power Instances for Static Simulation" menu.

```
Power of different cell types in Watt:

cell_type       total_power     leakage_power   internal_power  switching_power
combinational       0.002555        2.9608e-05        0.00097332        0.001552
latch_and_FF       0.0011546        1.7848e-05        0.00094938        0.00018734
memory                  0          0          0          0
I/O                     0          0          0          0
clocked_inst       0.0011895        3.1601e-06        0.00097024         0.00021607
decap           0.00048512        0.00048512          0          0

Total chip power, 0.0053841 Watt including core power and other domain power.
Total clock network only power, 0.0022074 Watt. Total clock power including
clock network and FF/latch clock pin power, 0.0030004 Watt.
```

Fig 2.1: Redhawk report (adsRpt/power_summary.rpt) showing power calculation summary.

You can use the Power Density map (PD) to get the power density distribution in the design. Similarly, Instance power map (IPM) will show you the instance power distribution. Similarly, clock power map (CPM) will show power distribution separately for clock related instances in the design.

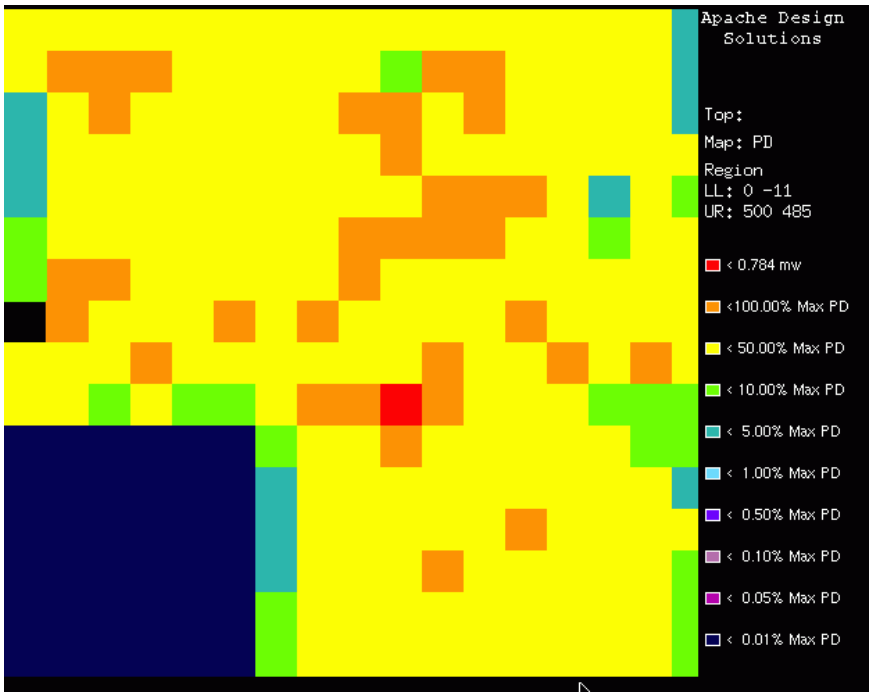

Fig 2.2: Power density map created using “PD” button.

Average power has both static and dynamic components. Static component is the leakage power.

- You can look at the leakage power map (LPM) in the results panel to see whether there are any cells with excessive leakage.
- From the instance power file (adsRpt/<design>.power.rpt) you can find leakage power component for any instance.

Dynamic component is contributed by internal power and the switching power. This component is proportional to the frequency, load and toggle rate. Reason for high dynamic power could be one of the following:

- High frequency of switching.
- High Load capacitance.
- High toggle rate or BLOCK_POWER_FOR_SCALING used in the analysis.

From the instance power file, you can get the of the power calculation.

- You can analyze the Instance Frequency Map (IFM) to see whether high frequency is causing high power in some region.
- Load Cap map (LC) will tell you whether high load is causing the dynamic component of power. High load issue normally happens when you have un-synthesized clock tree or scan chains, with some buffers driving huge fanout load.
- High toggle rate can also cause high dynamic power. RedHawk derives the toggle rate from one of the following ways:

    - Toggle rate is defined in GSR using the keyword TOGGLE_RATE.
    - You can also specify instance or block specific toggle rates using one of the following keywords.
        - INSTANCE_TOGGLE_RATE
        - BLOCK_TOGGLE_RATE
        - BLOCK_TOGGLE_RATE_FILE
        - INSTANCE_TOGGLE_RATE_FILE
    - If you are doing VCD guided analysis using VCD_FILE keyword in GSR, toggle rates will be derived from the actual transitions in the VCD.

- User can scale the power values computed by scaling the TOGGLE_RATE using the GSR keyword BLOCK_POWER_FOR_SCALING. Values specified in this section directly affect your static and dynamic results.

You can also click on any metal / via segments to see the amount of current flowing through the geometry. Static analysis shows the average current and dynamic analysis shows peak current. In static analysis, it will also show you the current direction. "CUR" Map shows the current distribution throughout the chip.

High transient current can be caused by simultaneous switching in the design. This is explained later in this application note.

2b. How do I know whether high PG impedance is causing my drop?

High Power grid resistance will impede the current flow in the power grid causing high static or dynamic voltage drop. You can use PG Resistance Map (View -> Resistance Maps) to highlight areas with high PG resistance. Also, you can write out the PG Resistance report using the Redhawk command "perform gridcheck". More details on PG Weakness analysis can be found in the application note "Analyzing PG Weakness Results in RedHawk GUI".

RedHawk has several features to analyze the structural weakness issues in the power grid. You can use "View -> Connectivity" menu to analyze PG structural issues such as:

- Disconnected instances
- Disconnected wires/vias
- Shorts
- Missing vias

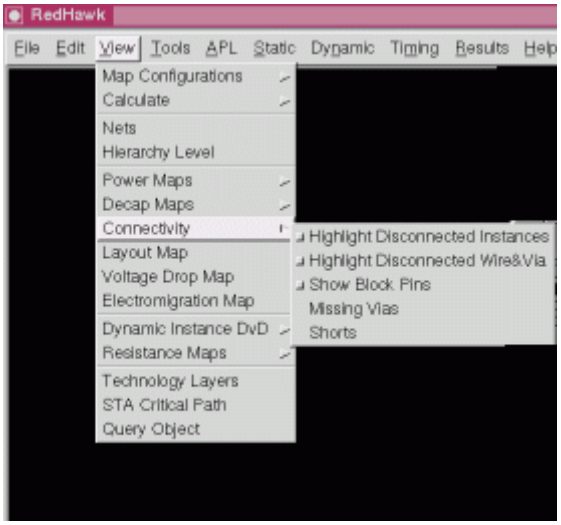

Fig 2.3: Connectivity analysis options

When you highlight disconnected instances in Redhawk GUI, instances with VSS disconnect will get highlighted in Blue, VDD disconnect will get highlighted in Green and both VDD/VSS disconnect will get highlighted in Yellow.

Corresponding text reports are also available inside adsRpt directory (adsRpt/*.unconnect, adsRpt/apache.missingVias etc).

If there is any major disconnect in the power grid, it will affect the current flow in the design. You can use the current map (CUR button) to review the current flow through the power grid to see whether there are any surprises.

If you are performing RLC extraction on the power grid, high inductance can also cause high dynamic drop. You can perform a dynamic analysis based on RC extraction and compare the results to see whether L component is causing the high drop.

2c. How do I debug whether high package parasitics are causing high drop in the design?

If you are including package parasitics in your analysis you need to look at the voltage drop caused by the package to see whether this is causing high voltage drop issues. You can click on the pad in GUI to query the voltage at the pads. If you notice a high drop at the pad itself, it is an indication of high package parasitics used in the analysis. To confirm this, you can perform an analysis by removing the package parasitics and compare the results. When you do analysis with no package parasitics, pads should show ideal voltage values while querying.

Static drop will get affected only by the package resistance component. But, the dynamic analysis can get affected by both resistance and inductance components. The more the (di/di), the more the drop caused by inductance component. You can view the battery current waveform through Redhawk TCL command “plot current –vdd –sv” to see the rate of change in current.

In the log file, Redhawk will report the summary of package parasitics used in the analysis while performing static or dynamic simulation.

```
** Pad/WireBond/Package RLC Setting Summary **
   Pad Vdd Resistance = 0 ohm
   Pad Vdd Cap = 0 pF
   Pad Gnd Resistance = 0 ohm
   Pad Gnd Cap = 0 pF
   Wirebond Vdd Resistance = 0 ohm
   Wirebond Vdd Inductance = 0 pH
   Wirebond Vdd Cap = 0 pF
   Wirebond Gnd Resistance = 0 ohm
   Wirebond Gnd Inductance = 0 pH
   Wirebond Gnd Cap = 0 pF
   Package Vdd Resistance = 0.005 ohm
   Package Vdd Inductance = 0.0005 pH
   Package Gnd Resistance = 0.005 ohm
   Package Gnd Inductance = 0.0005 pH
   Package Vdd-to-Gnd Cap = 0.001 pF
```

Typical values for pad/wirebond/package inductance values for a wirebond design are given here:

```
setup wirebond : 2 - 8 nH
setup pad : 50 pH
setup package : 250 - 500 pH
```

You need to make sure that the values you are specifying are somewhere close to this range. If there is excessive inductance coming from the package, it can also cause some ringing in the battery current waveform.

2d. How do I know whether the drop is caused by insufficient number of PG pads?

If there is not enough number of power ground pads in the design, it may lead to high static and dynamic voltage drop issues. You can highlight the voltage pads in GUI using "Show Power Pad" button. A power pad will get highlighted in Orange color and a ground

pad will get highlighted in White color. You can query the details of any pad by clicking on it in the GUI. Or, you can use “get pad” command in RH TCL prompt to see the details. After PG extraction, Redhawk will also report the list of Power ground pads in file adsRpt/PG.ploc.

If there are not enough power/ground pads in some regions of your design, pads sitting in the nearby region will be supplying more current than the other power ground pads in the design. In static analysis, you can get the average current supplied by each pad inside adsRpt/Static/pad.current file. In dynamic analysis, Redhawk will report the peak current supplied by each pad in the file adsRpt/Dynamic/pad.current. You can sort these files to identify the pads which are driving higher current than the rest of the pads. You can also plot the current waveform through each pad in the design using “plot current –pad” command.

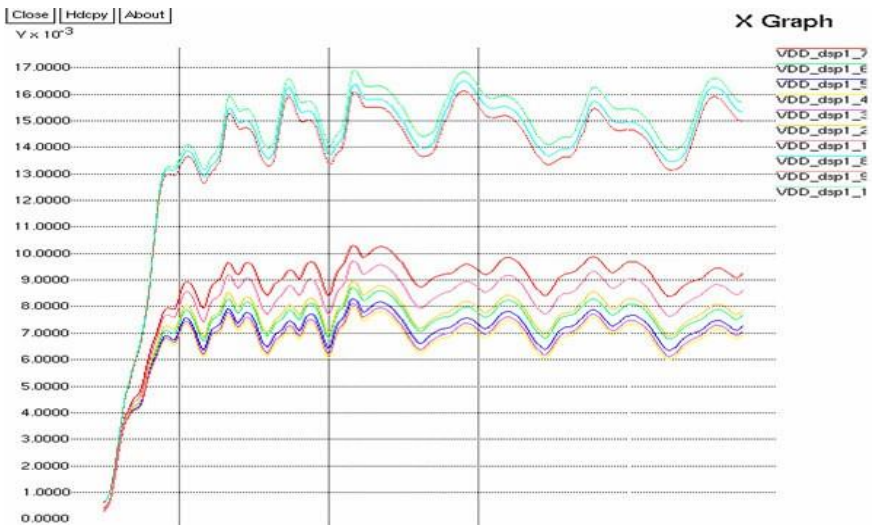

Fig 2.4: Pad current waveforms created using “plot current –pad” command.

If your design contains header or footer switches, then these switches will be acting as the voltage sources for the internal (switched) power domain. If you are seeing high voltage drop issues in the switched power domain, you need to review the switch cell placement in Redhawk GUI using select command. Here is an example command to highlight all switches in the design

```
select add [get instofcell SWITCH_CELL]
```

If there are insufficient number of switches in some regions in the design, switches sitting in the neighboring regions will be supplying more current than the rest of the switches. This can also cause excessive voltage drop across these switches. In Static analysis, Redhawk will report the voltage drop and current for every switch inside the file adsRpt/Static/switch_static.rpt. Similarly, in dynamic analysis peak current and maximum voltage drop is reported inside file adsRpt/Dynamic/switch_dynamic.rpt.

2e. How do I make sure that the drop is not caused by inadequate decoupling capacitance?

In order to analyze the details of decap distribution in the design, you can use various decap density maps in Redhawk.

DD: Total decap density map
DEV: Device decap density map
IDD: Intentional decap density map
LC: Load capacitance map.

You can also get the decap report through the TCL command “print decap”.

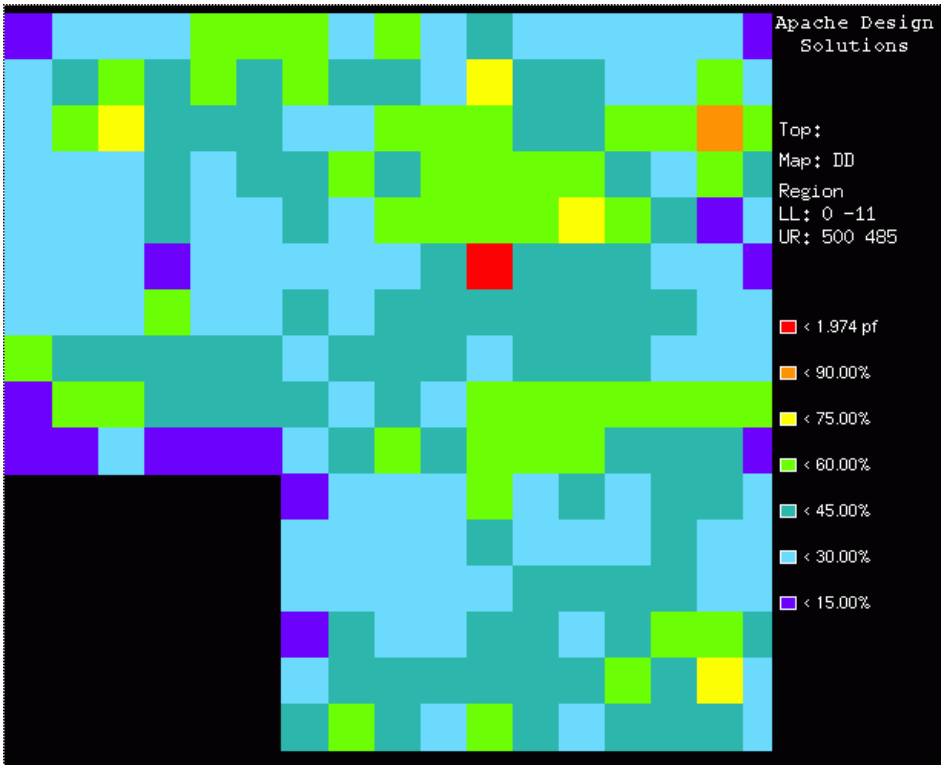

Fig 2.5: Decap density Map showing total decap distribution in the design

RedHawk will use the device decap values in the analysis only if you are importing the APL cdev files. You can review `adsRpt/apache.refCell.noAplCap` file to see cells with missing cdev data. Also, in-order to view IDD map, you need to specify the DECAP_CELL keyword through the GSR.

Package can also contribute some decaps. You can review the annotated package parasitics in the log file to make sure that they are reasonable.

You can analyze the effectiveness of your decaps by looking at the difference between the battery current waveform and demand current waveform. When there is a simultaneous switching in the design, the demand current will be more than the current supplied by the battery. Extra demand current is supplied by decaps in the design. You can plot the battery current using Redhawk command “plot current –vdd –sv” and the demand current using “plot current –pwr –sv”. Difference will tell you how much current is contributed by decaps.

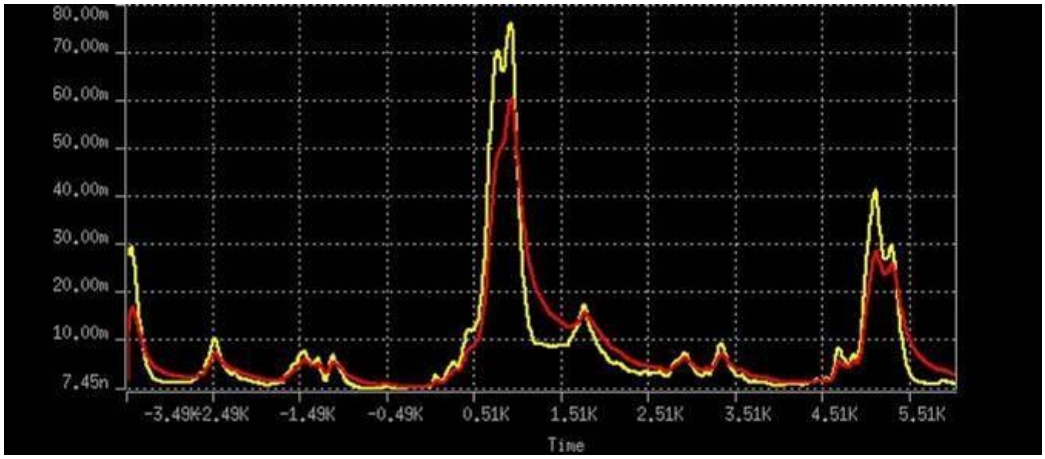

Fig 2.6: Battery and demand current waveforms created using “plot current” command

If you are using “DYNAMIC_REPORT_DECAP 1” in GSR, Redhawk will write out a decap report file (adsRpt/Dynamic/decap.rpt), which will give you the maximum current contributed by each decap instance in the design to its neighboring switching cells. From this file you can find out the decap instances which are effective in the design.

# decap_name		max_decap_current	min_rail
C714501	0.000061	1.117773	
C708251	0.000021	1.124485	
C705964	0.000056	1.127384	
C706706	0.000008	1.125248	
C706555	0.000082	1.124180	
C706042	0.000044	1.124485	
C708252	0.000031	1.124485	
C708939	0.000035	1.130282	
C710092	0.000026	1.129367	

Fig 2.7: Decap report (adsRpt/Dynamic/decap.rpt)

Also, it is very important to do a pre-simulation before the actual simulation to initialize the capacitance elements in the design. If decaps are not initialized to some realistic voltage value, there will be some high current flow during the start of real simulation. Pre-simulation will be automatically done by Redhawk if you are using “DYNAMIC_PRESIM_TIME” keyword in GSR.

2f. How do I identify whether there is simultaneous switching in the design causing high voltage drop?

Simultaneous switching can lead to high peak current consumption in the design causing high dynamic voltage drop. There are several ways in Redhawk to analyze the simultaneous switching effects.

You can look at the switching histogram TCL command: “plot switching” to analyze the number of cells switching as a function of time. “plot charge” command will show you the corresponding switching charge histogram. If there is a simultaneous switching, you will observe a sharp peak in the histogram plot.

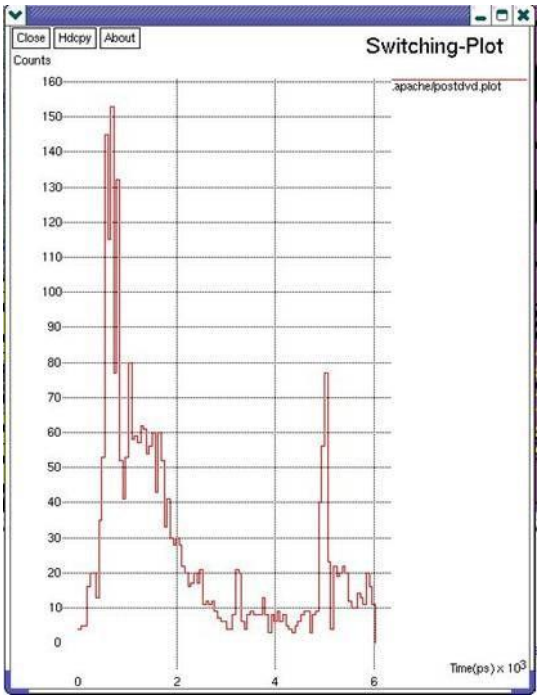

Fig 2.8: Switching histogram created using “plot switching” command

- Same effect can be observed in the current waveform also. You can plot the battery current and the demand current waveforms using “plot current” command. You should be able to see high current peaks in the waveform whenever there is a high amount of switching in the design. After the dynamic simulation, Redhawk will

also report the peak power value in the log file, which is a measure of the amount of simultaneous switching in the design.

```
************************************************************
**** Dynamic Result Summary
************************************************************
Peak Power: 0.609013 mW
```

- You can get the summary of switching using the tcl command “print type”. It will tell you the percentage of cells switching in each cell type category. High simultaneous switching could be caused by lot of memories or clock buffers switching at the same time. You can analyze the details using this report.

```
Type           Switch    Total      Switch %
-------------------------------------------
Combinational  1210      25742      4.70%
Sequential     354       6408       5.52%
Clock          592       855        69.24%
Special        0         0          0.00%
Memory/IP      0         1          0.00%
```

- You can dump out the switching status of every instance in the design using “print instance” command. From the output of this command, you can filter out the switching instances and highlight them in the GUI using “select addfile” command. If you want to analyze the switching scenario for a particular time interval, you can set the time condition using “condition set –time” command. Similarly, if you want to restrict the analysis to a specific region in the design, you can set the xy conditions using “condition set –xy” command.

  Here is an example sequence of commands which will help you highlighting the switching instances in the design for a given time interval and xy condition.

```
condition set –xy 50 200 150 300
condition set –time 2000 3000
print instance –o inst.txt
awk ‘{if($1 == 1) {print $2}}’ inst.txt > swInst.list
select addfile swInst.list
```

In vectorless analysis, simultaneous switching happens when there is high overlap between timing windows for different instances in the design. If you are doing, VCD based true timing simulation, it is important to make sure that the VCD is annotated with correct SDF during the verification run.

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