

RedHawk Training - SoC Power, Noise & Reliability

June 16, 2020



ANSYS Technologies for Electronic Systems

Power Budgeting

PowerArtist™
RTL Power Analysis, Reduction

RedHawk™

PDN planning, In-rush, Power Integrity, EM, Integrated pkg

PDN, RV

IC→System

CPM™:

- System PDN
- System Thermal

Package/PCB Electrical

SIwave/HFSS/Q3D:
Early to sign-off

Connectors

HFSS/Q3D

Thermal Planning

Icepak
Chip-aware system thermal

IP Validation

Totem™:

- IR, EM and DvD
- Model for SoC

ESD protection

PathFinder™: ESD sign-off

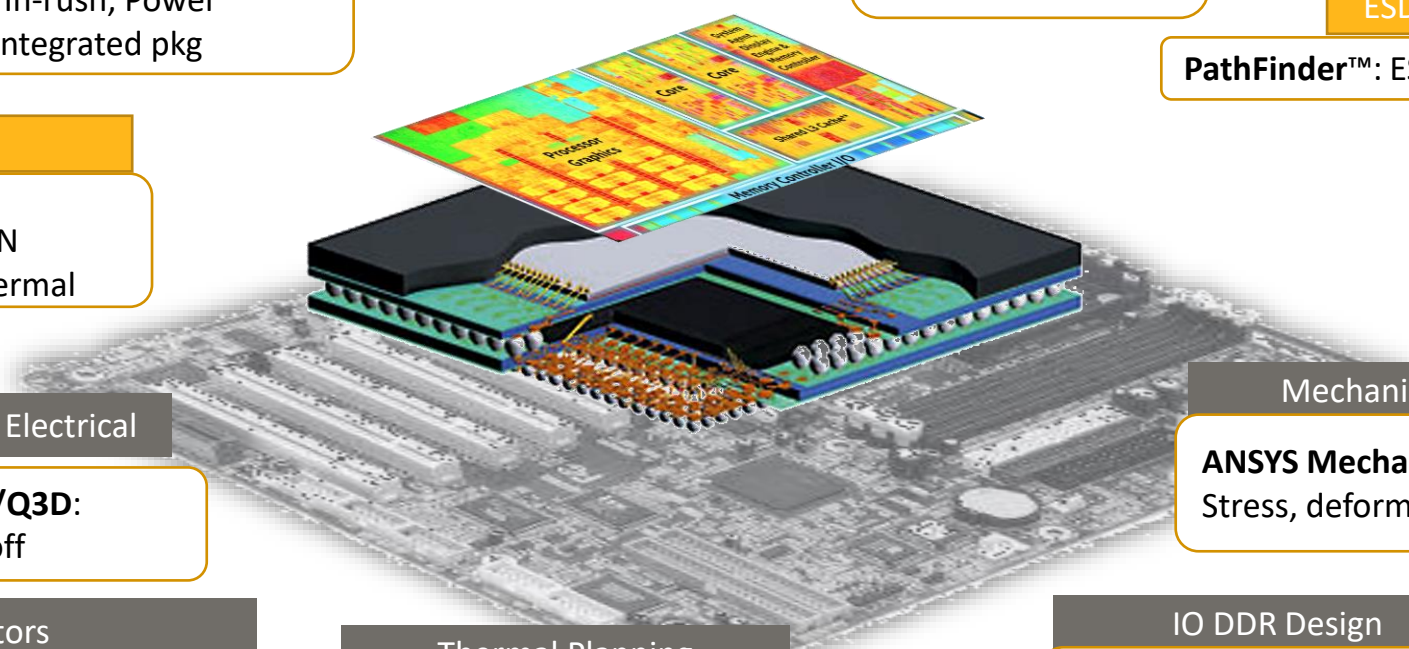
Mechanical Stress

ANSYS Mechanical
Stress, deformation

IO DDR Design

DesignerSI/SIwave/CSM™:

- IO ring verification
- System jitter prediction

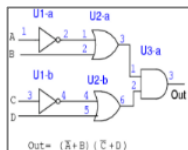


ANSYS Semiconductor Products in Flow

RTL & Gate Power:

- Power reduction
- Power analysis
- Power regression

```
define spec 0
define real 1
define real 2
// state assignment
module reduce (clk, reset, in, out);
input clk, reset, in;
output out;
reg out;
reg [1:0] state; // state variables
always @(posedge clk)
if (reset) state = 'b00;
else state = next_state;
endmodule
```



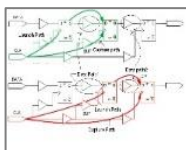
Place & Route:

- Early convergence of PI
- PI aware placement
- Fixing and optimizing



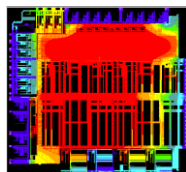
Timing Signoff:

- Spice accurate timing
- Variability/aging aware timing
- DvD aware timing



Power/Reliability Signoff:

- Dynamic voltage drop
- Electromigration
- Chip-aware package design



Architectural spec

Microarchitecture
RTL Design

Logic Synthesis

Place and Route

Timing Signoff

Power/Reliability
Signoff

Tape-out

PowerArtist™

RedHawk™ - Fusion

Path-FX™

Totem™

RedHawk™

RedHawk-SC™

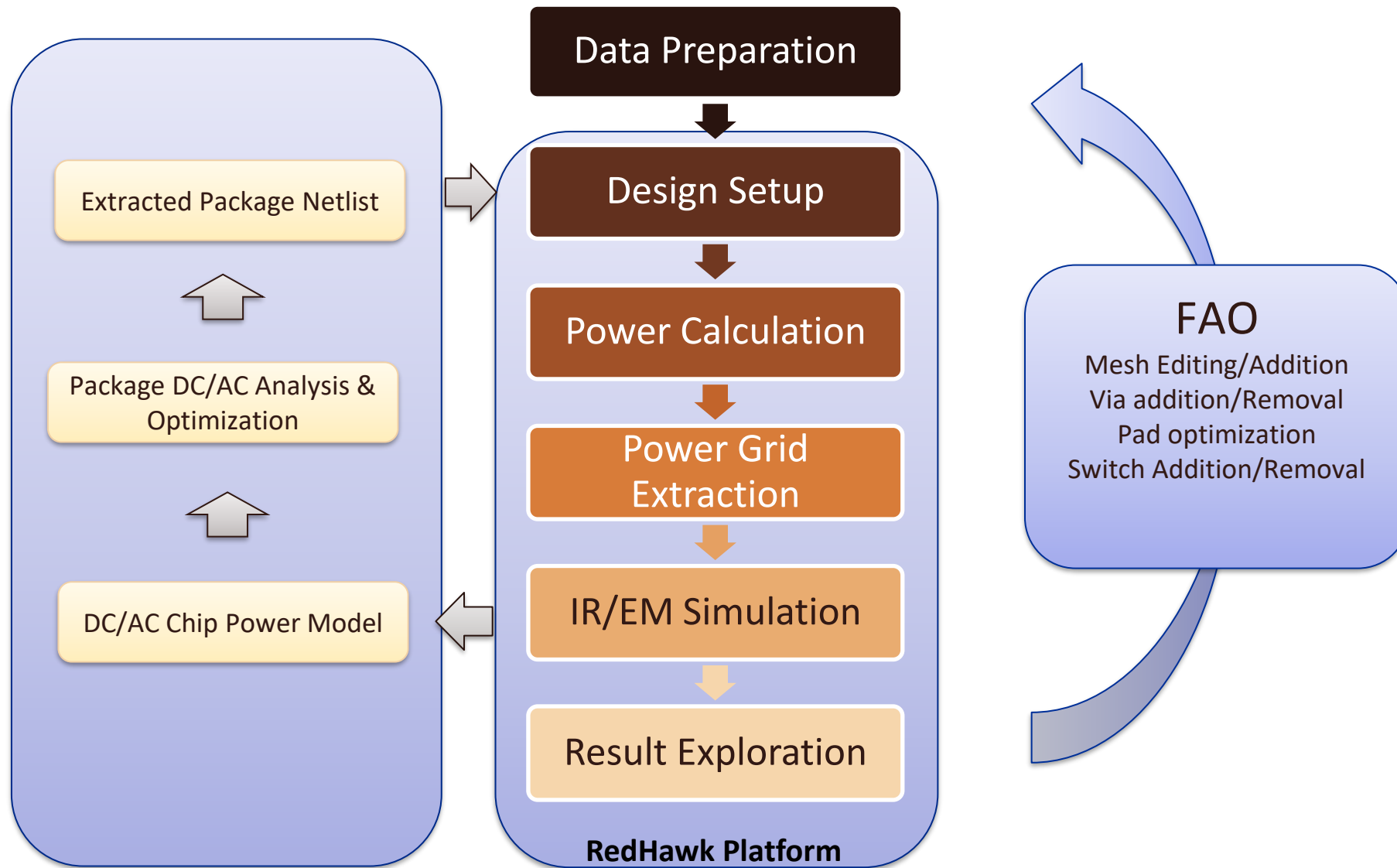
Training Agenda

- RedHawk Static/Dynamic analysis theory
- Input data preparation & IP/Standard cell modelling
- Package handling in RedHawk
- GUI and Tcl commands in RedHawk : Demo
- Result Analysis and Root Cause identification using RedHawk Explorer (RHE)
- Chip Power Model (CPM) generation and Chip-Package-System(CPS) analysis
- Distributed Machine Processing (DMP) for large designs

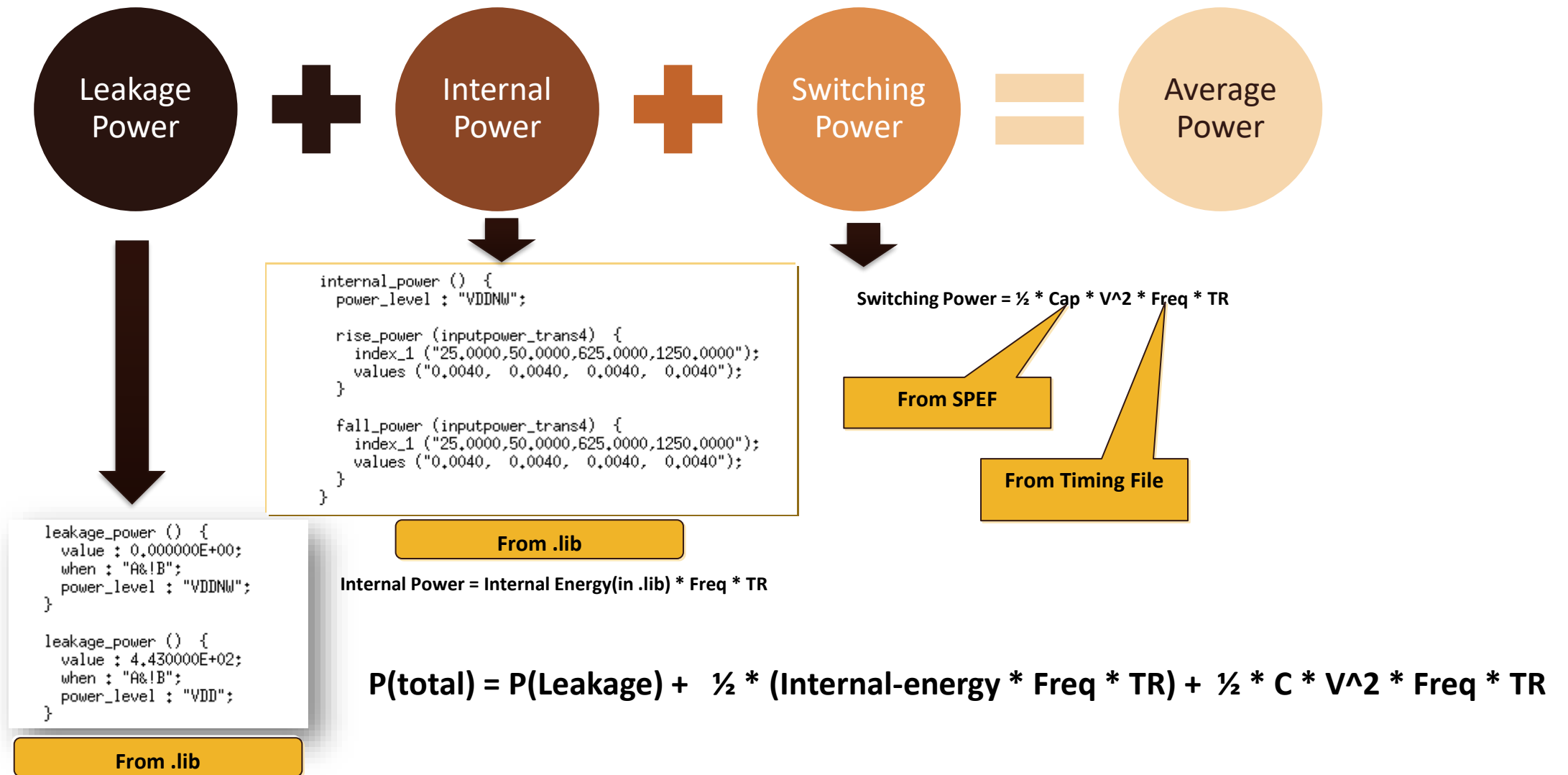
RedHawk Static/Dynamic analysis theory



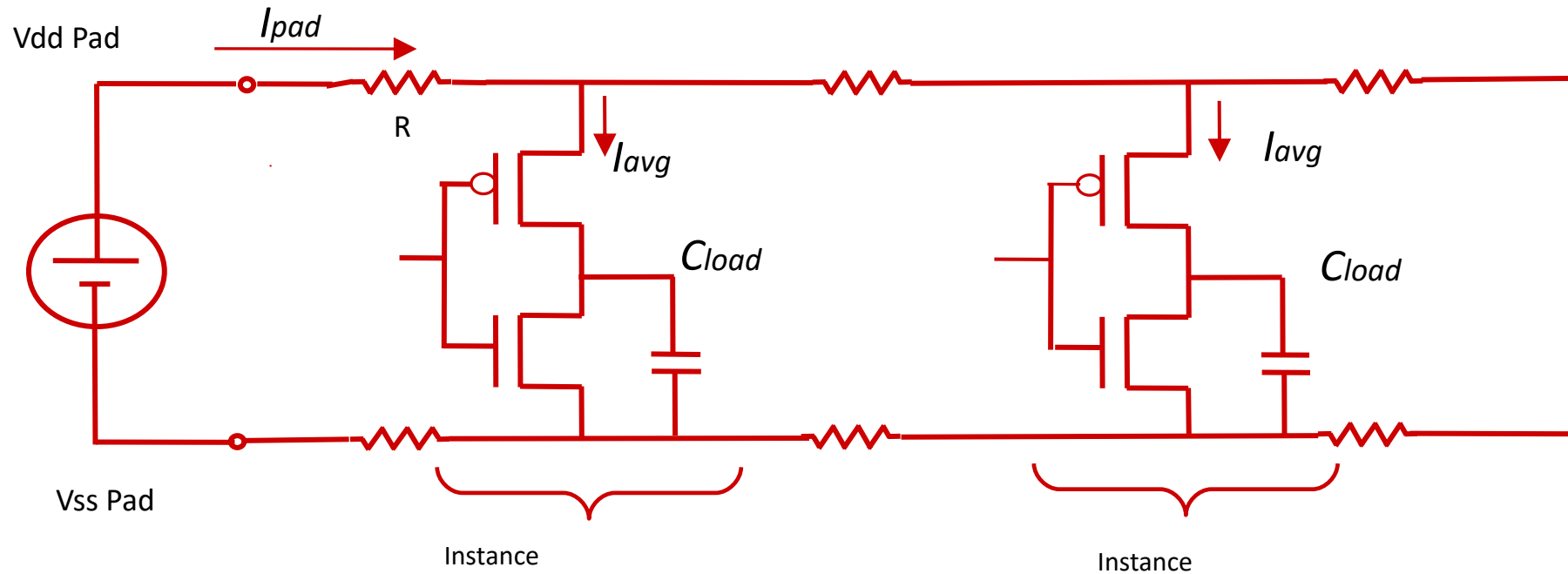
/ RedHawk Analysis Flow



Gate-level Average Power Calculation



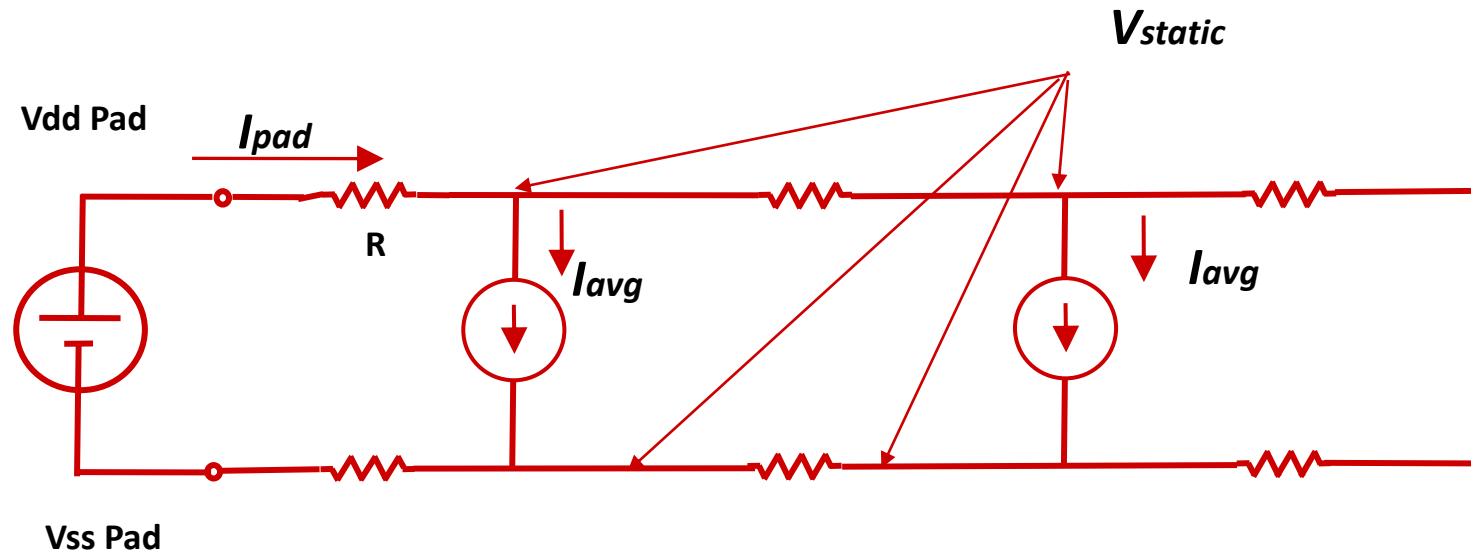
/ Static Voltage Drop Background



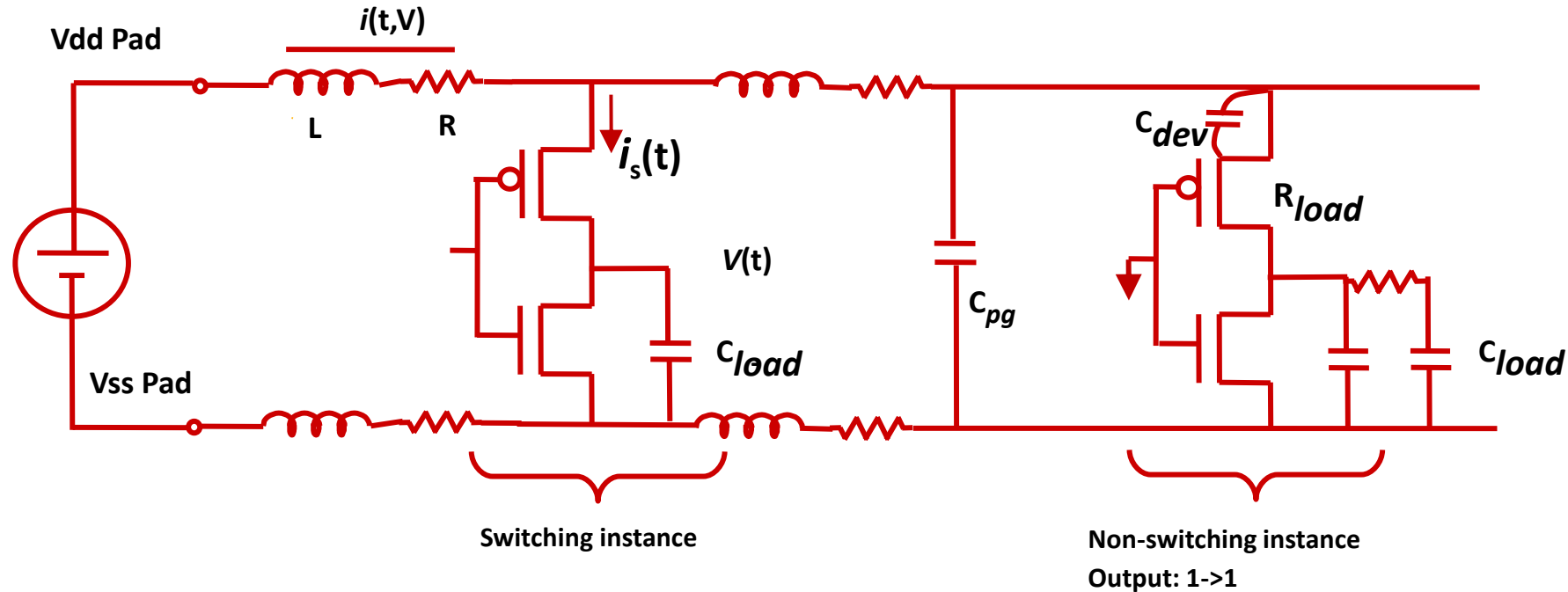
- On-chip power/ground network → mesh of resistors
- Average current (I_{avg}) of instances is estimated from Average power
- Instances → DC current sources

/ Static Voltage Drop on P/G Network

- Average current is calculated for each instance
- V_{static} is computed at every node (Ohm's law ...)
- Wire / via electromigration (EM) is post-processed from static current density



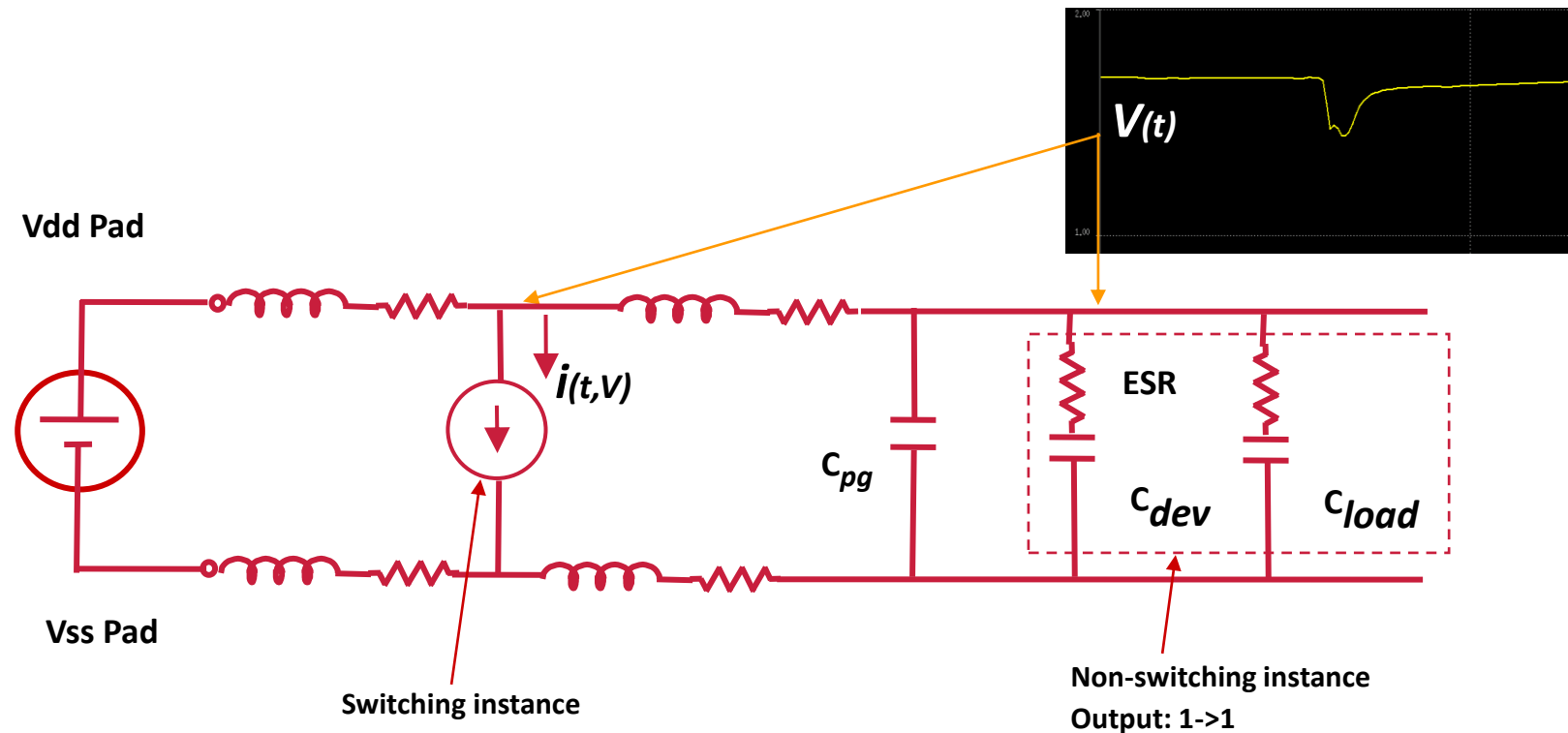
Dynamic Voltage Drop Problem Definition



- On-chip power/ground network → R,L,C mesh
- Switching instances → $i(t,V)$ sources
- Non-switching instances → Effective decaps, ESR and leakage

Dynamic Voltage Drop on P/G Network

- PWL current for each instance
- Vdynamic waveform is computed at every node by transient simulation



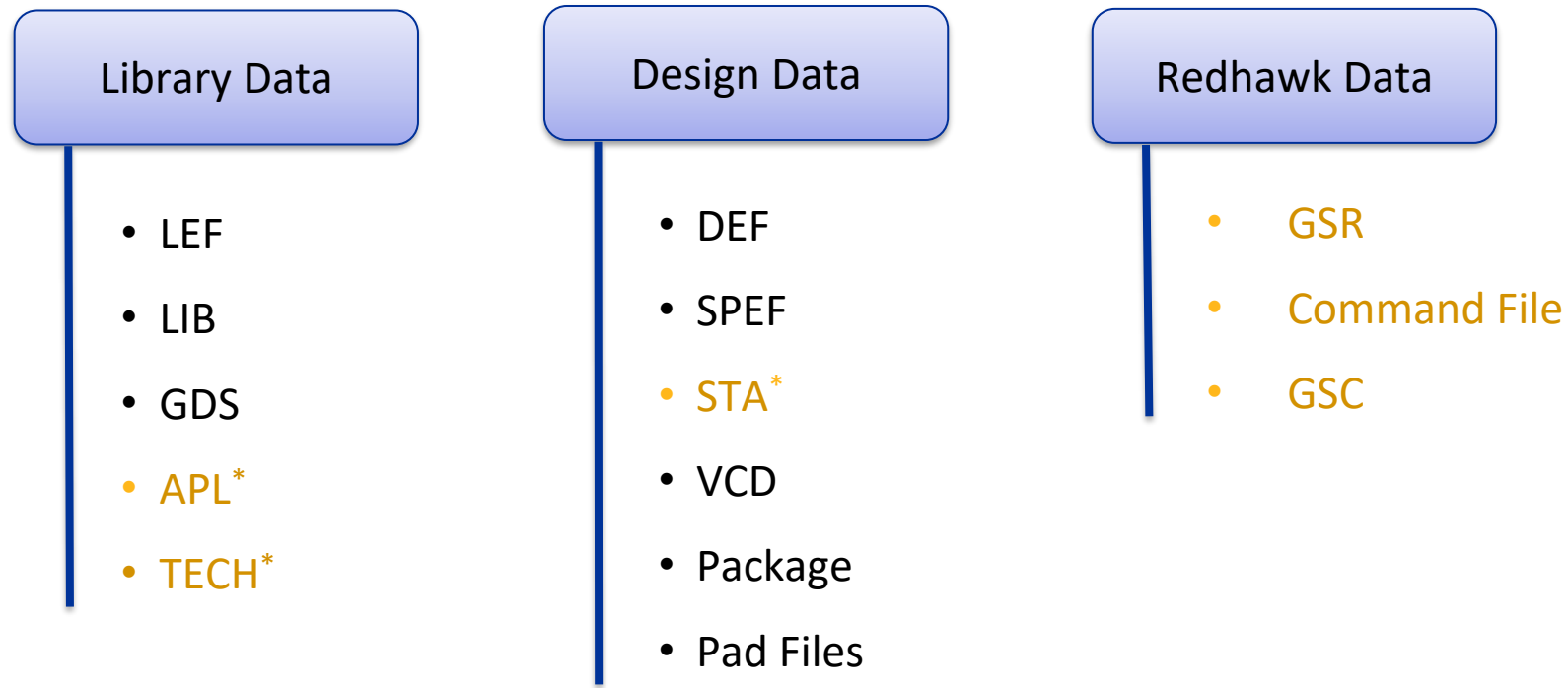
/ Difference Between Static and Dynamic

Static	Dynamic
All instances will draw an average current (DC)	Switching instances will draw transient current (AC) Non-switching instances will draw only leakage
Total Average demand will be much less than real peak demand current for the chip	Dynamic will see the real peak demand current
Demand current is completely supplied by battery	Portion of the demand current is supplied by decaps (Intrinsic / Intentional / PG caps)
Doesn't matter when an instance switches Instances will draw the current all the time	Instances will draw transient current only when it switches Simultaneous switching causes huge peak current demand
No drop across package due to Ldi/dt effects (Current is constant)	Ldi/dt drop across package and die inductance

Input data preparation & IP/Standard cell modelling



/ RedHawk Input Data Requirement



* : These inputs are created using Ansys utilities

/ RedHawk Modeling for Standard Cells

Standard cell Modeling

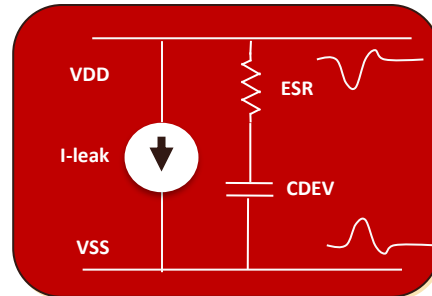
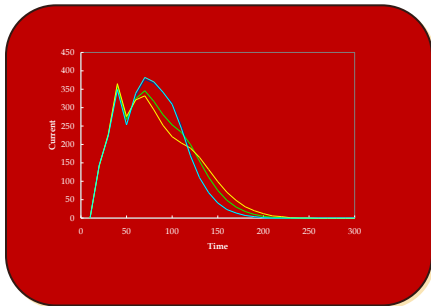


- Current Model

- Look up table for current waveforms based on three variables : load, slew and voltage

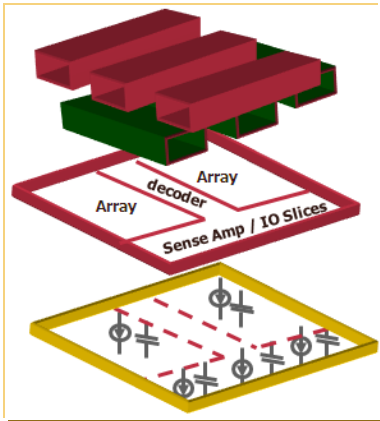
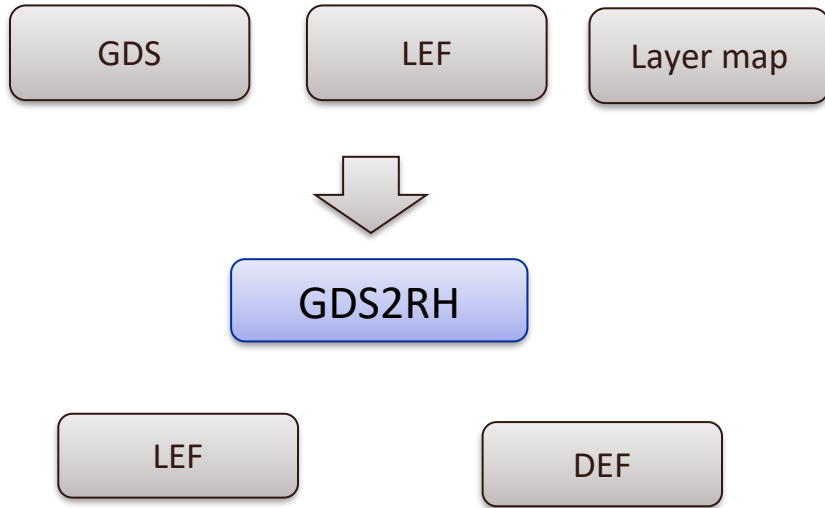
- Cap Model

- Captures effective series resistance(ESR) and effective series capacitance(ESC) and leakage

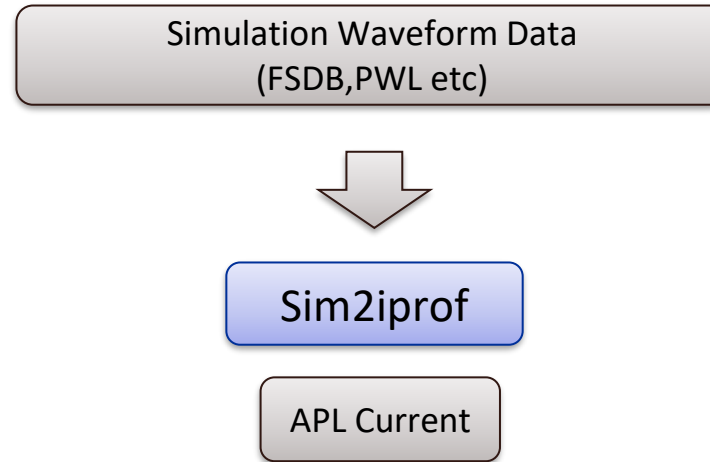


RedHawk Modeling of Memories and IPs

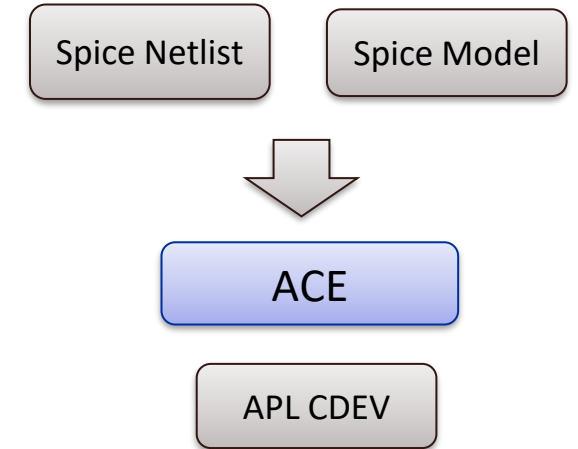
Physical Modeling from GDS



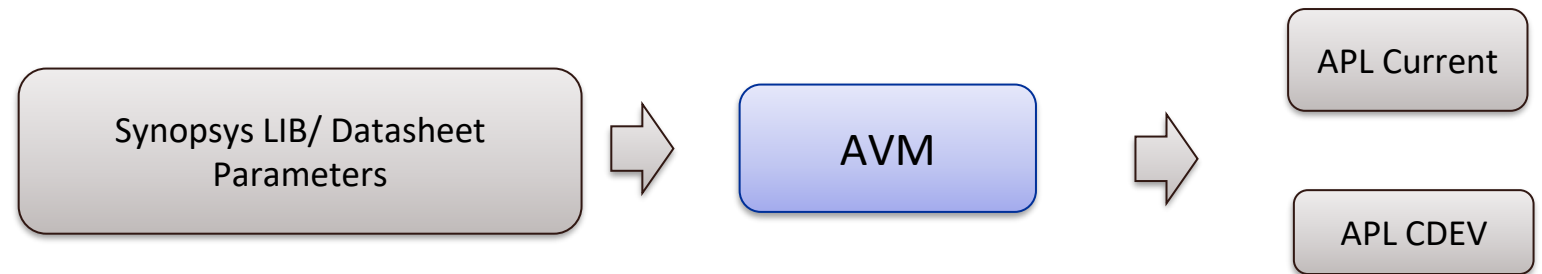
Current Modeling From Simulation W/f



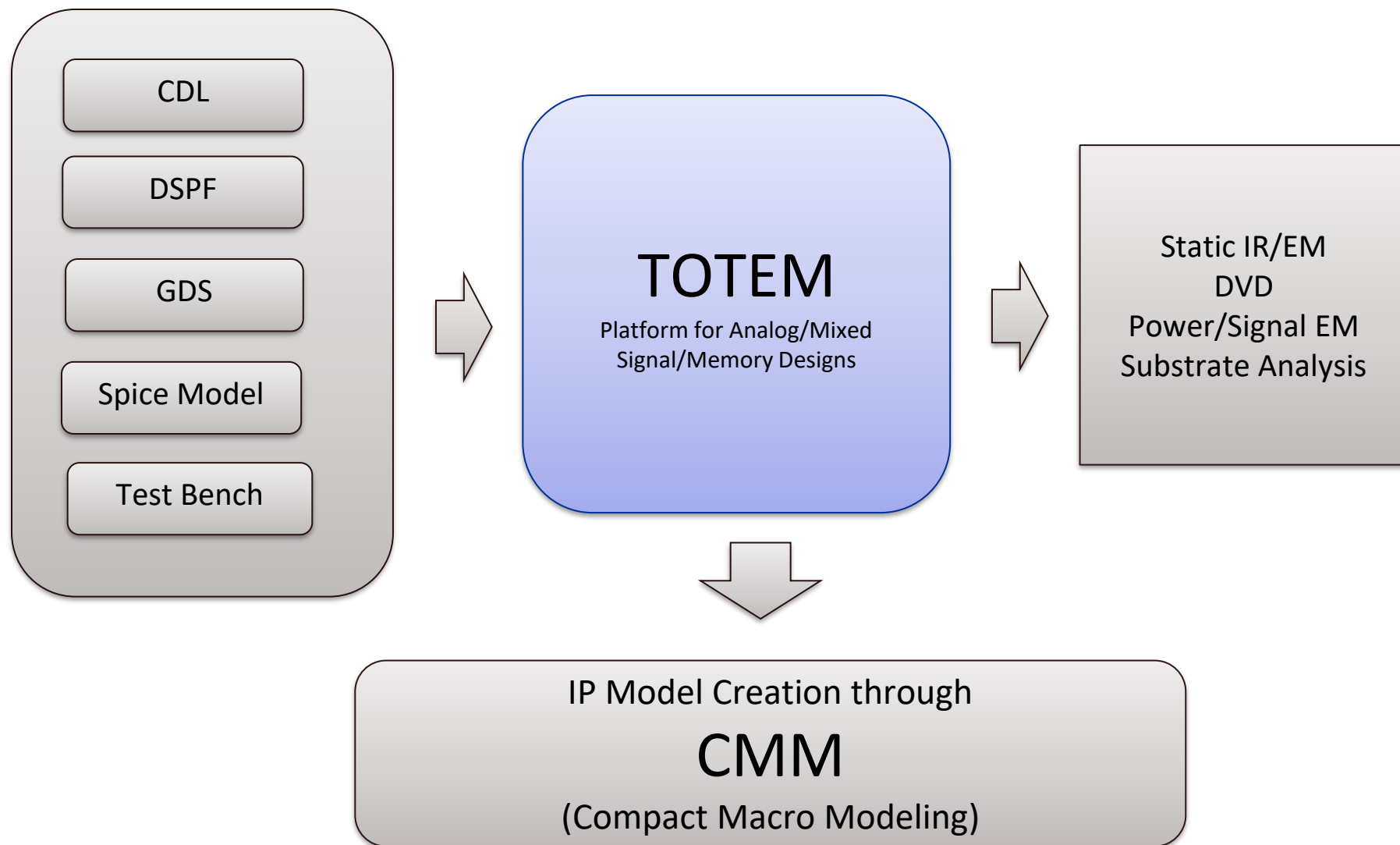
Cap Modeling Through ACE



Current/CAP Modeling Through AVM



/ Transistor Level IP Modeling Using Totem



/ What is Inside STA File ?

- Instance Frequency
 - Required for static and dynamic
- Clock domain info
 - Required for static and dynamic
- Timing Windows
 - Not required for static
- Slew
 - Required for Static (Power calculation uses Slew)
 - Required for Dynamic (Current w/f is dependent on Slew)

/ Specifying Voltage Source Locations

Option-1

Redhawk automatically identifies the voltage source locations from PINS section in DEF

Option-2

User can specify the master cell name for P/G pads through a file

Option-3

User can specify the P/G pad instance names through a file

Option-4

User can specify the P/G pad (x,y) locations through a file

← Most commonly used

See RedHawk manual for details

/ GSR (Global System Requirement) File

```
TECH_FILE <path to TECH File>
```

```
LIB_FILES {  
  <Path to LIB Files>  
}
```

```
LEF_FILES {  
  <Path to LEF files>  
}
```

```
GDS_CELLS {  
  <Path to Gds2def models>  
}
```

```
APL_FILES {  
  <Path to APL models>  
}
```

```
CMM_CELLS {  
  <Path to CMM models>  
}
```

Library File Pointers

```
DEF_FILES {  
  <Path to the DEF files>  
}
```

```
STA_FILE {  
  <Path to timing file>  
}
```

```
CELL_RC_FILE {  
  <Path to Spef file>  
}
```

```
VCD_FILE {  
  <VCD file details>  
}
```

```
PAD_FILES {  
  <Path to Pad File>  
}
```

Design Data Pointers

Commonly Used GSR Keywords

`FREQUENCY 70e6`

Dominant Frequency of the design

Frequency	% of Total Power	Cumulative % of power
100 MHz	80%	80%
70 MHz	10%	90%
20 MHz	10%	100%

- Important input for Vectorless engine
- Dominant frequency is NOT the frequency with highest % of power
- It is the frequency above which 90% of the power is present
 - Arrange frequency in descending order
 - Start adding up cumulative power
 - Frequency at which we achieve 90% cumulative power is selected as dominant frequency
- Script is available to automatically set this

/ Commonly Used GSR Keywords

```
TOGGLE_RATE 0.15 1.5

INSTANCE_TOGGLE_RATE {
  instance_name toggle_rate
}

BLOCK_TOGGLE_RATE {
  block_name toggle_rate
}
```

Global Toggle Rate Used
(BPFS will override this)

```
TEMPERATURE 125
```

To specify the P/G Extraction Temperature

```
VDD_NETS {
  VDD 1.2
  inst_129973/VDD_INT 1.2
}
GND_NETS {
  VSS 0
}
```

Nets being analyzed and Ideal Voltage

/ Commonly Used GSR Keywords

```
DYNAMIC_SIMULATION_TIME 10e-9  
DYNAMIC_PRESIM_TIME -1  
DYNAMIC_TIME_STEP 10e-12
```

Dynamic Simulation Settings

```
INPUT_TRANSITION 100e-12
```

Default Slew value used
(Used for instances missing in STA File)

```
IGNORE_TECH_ERROR 1  
IGNORE_DEF_ERROR 1  
IGNORE_UNDEFINED_LAYER 1  
IGNORE_LEF_DEF_MISMATCH 1
```

Option to proceed even with Errors

Commonly Used GSR Keywords

BLOCK_POWER_FOR_SCALING (BPFS)

- Used for defining power target values
- RH will scale the toggle rate to meet user specified power target
- Scaling can be done at Full-chip/Block level. It can be master cell specific too
- Can define pin specific power for multi-vdd cells

```
BLOCK_POWER_FOR_SCALING {  
  
    FULLCHIP FULLCHIP 1.2  
  
    FULLCHIP BLOCK_INST_NAME 0.5  
  
    CELLTYPE MEM_1024x768 0.1  
  
    FULLCHIP INST1 0.005 VDD1  
    FULLCHIP INST1 0.006 VDD2  
}
```

INSTANCE_POWER_FILE (IPF)

- Can be used to import instance power numbers from 3rd party tools
- RH will assign the power number from this file as it is
- Instances missing in this file will get zero power
- Supports pin specific assignment

```
INSTANCE_POWER_FILE design.ipf
```

```
#Format of design.ipf  
Inst1/inst_100 0.0123  
Inst1/inst_102 0.0123  
Inst1/inst_104 0.0123  
Inst1/inst_105 0.0123  
Inst1/inst_106 0.0123  
Inst1/inst_107 0.0123  
Inst1/inst_108 0.0123  
Inst1/inst_108 0.0123  
Inst1/inst_109 0.0123 VDD
```


/ Command File Overview

```
# Import data
import gsr GENERIC.gsr
setup design

# Calculate power
perform pwrcalc

# Power/Ground grid extraction
perform extraction -power -ground

# Static IR analysis
perform analysis -static

# Exporting the DB for future use
export db static.db
```

Static command file

```
# Import data
import gsr GENERIC.gsr
setup design

# Calculate power
perform pwrcalc

# Power/Ground grid extraction
perform extraction -power -ground -c

# Dynamic IR analysis
perform analysis -dynamic

# Exporting the DB for future use
export db dynamic.db
```

Dynamic command file

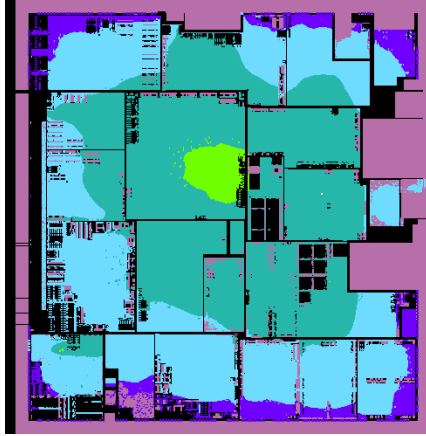
/ Vector based analysis

- RedHawk supports various simulation output formats
 - VCD (Value change dump) File
 - FSDB (Fast signal database)
- VCD/FSDB can be generated at two stages
 - RTL Level : contains only Flop and primary I/O activity
 - Gate Level : contains activity for all nets in the design
- Cycle selection can be done based on
 - Power : Pick cycle with worst power
 - Change in power : Pick cycle with worst change in power

Package Handling in RedHawk



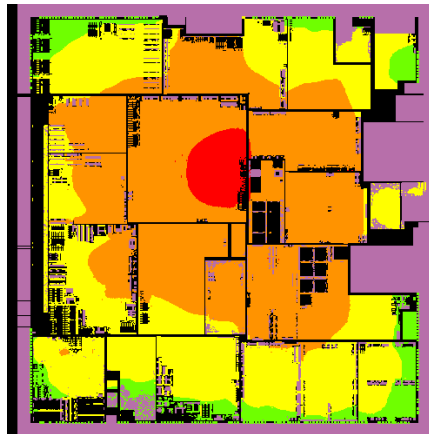
/ Package Impact on Dynamic Voltage Drop



Without Package Model

Inclusion of package effects

- Ldi/dt noise and hence higher drops
- Choice of package capacitance



With Package Model

Different methods for annotating Package

- Using lumped values through command file
 - Setup package/wirebond/pad constraints
- Using package spice netlist
 - In the form of RLCK models
 - In the form of S-Parameter form

/ GSR Settings Requirements

```
DYNAMIC_SIMULATION_TIME 5e-9
```

```
DYNAMIC_TIME_STEP 10e-12
```

```
DYNAMIC_PRESIM_TIME 20e-9
```

→ Sufficient presim to charge internal nodes

```
CPA_FILES {  
  PACKAGE <package_layout_filename>
```

```
  MODEL <project_path>  
}
```

→ Package layout to be extracted & displayed in GUI

→ CPA package model with ploc file

If CPA model is not available

```
PAD_FILES {  
  GENERIC.ploc  
}
```

```
PACKAGE_SPICE_SUBCKT_INFO {  
  PATH GENERIC.package.spi  
}
```

→ Ploc files with package hooked up

→ Wrapped Package spice netlist

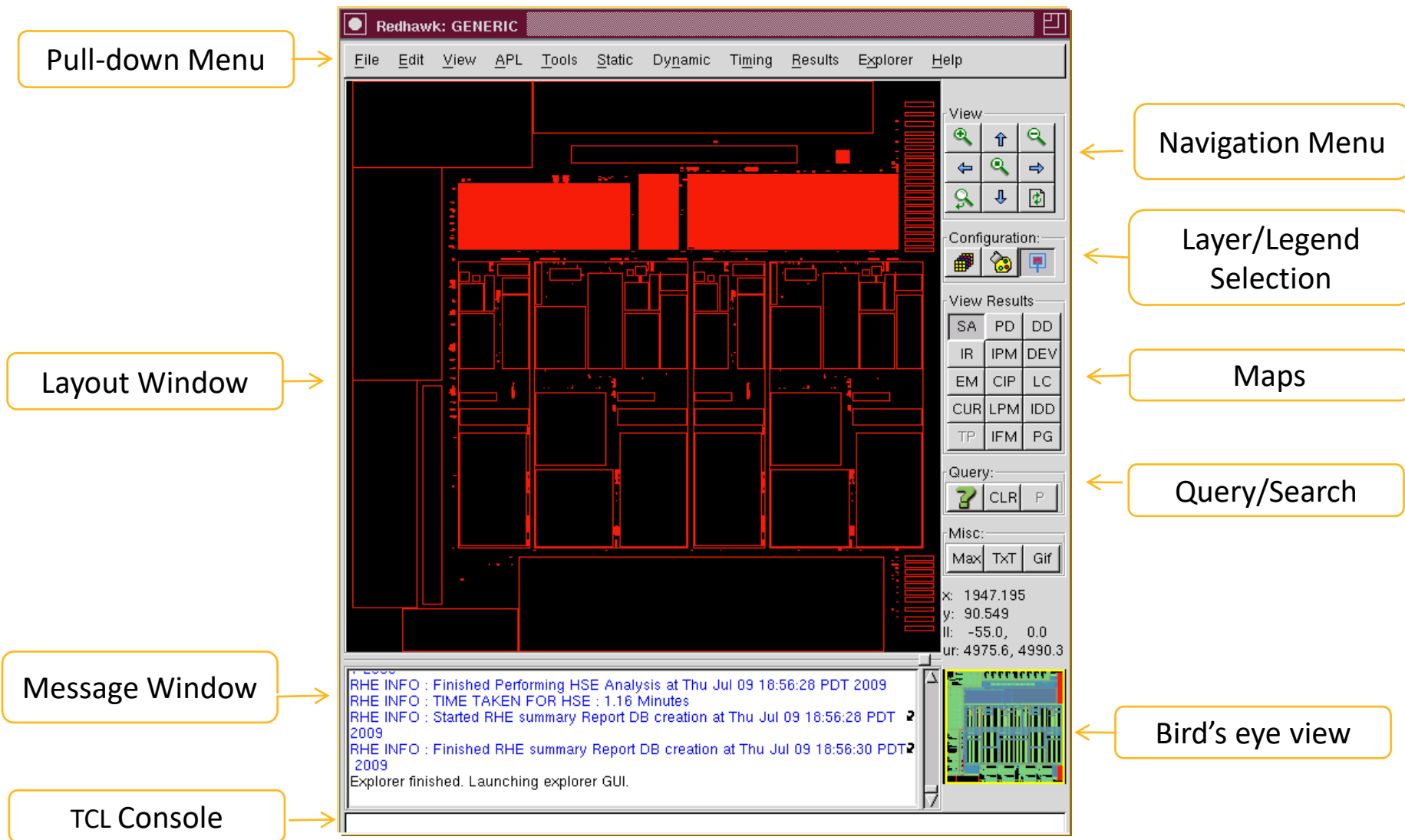
Q & A Session



GUI and Tcl commands in RedHawk : Demo

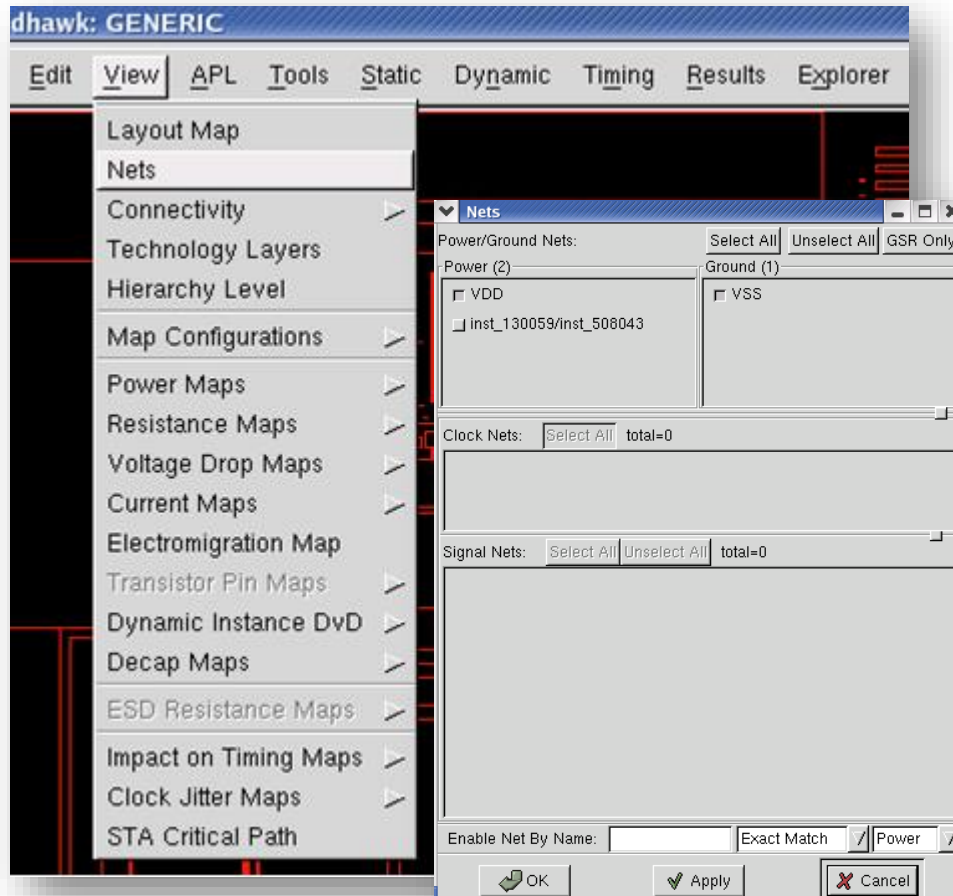


RedHawk GUI Overview

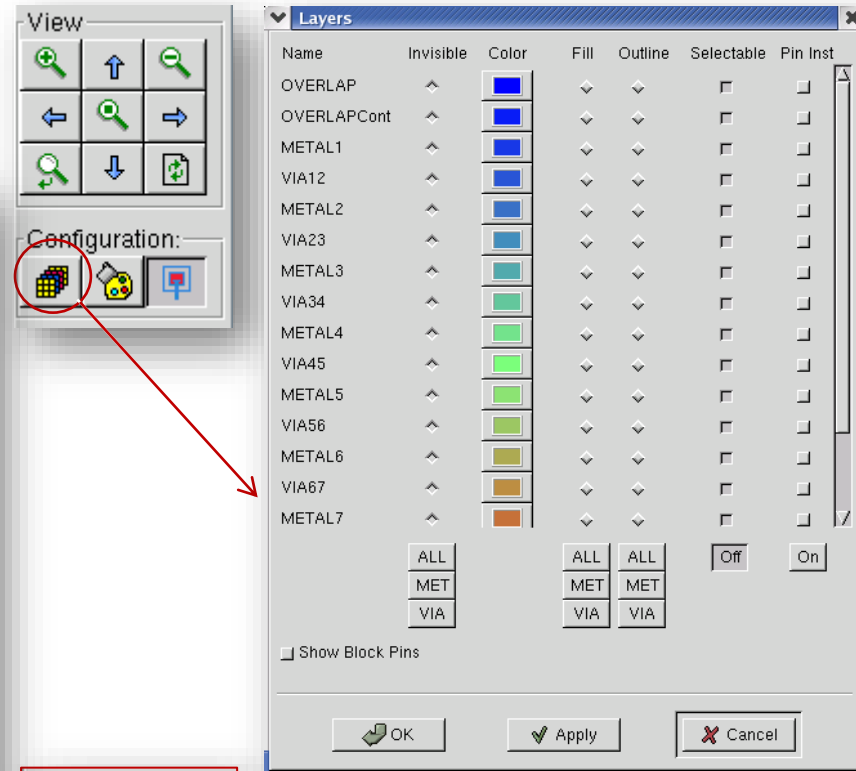


GUI Basic Operations

Viewing Selective Nets



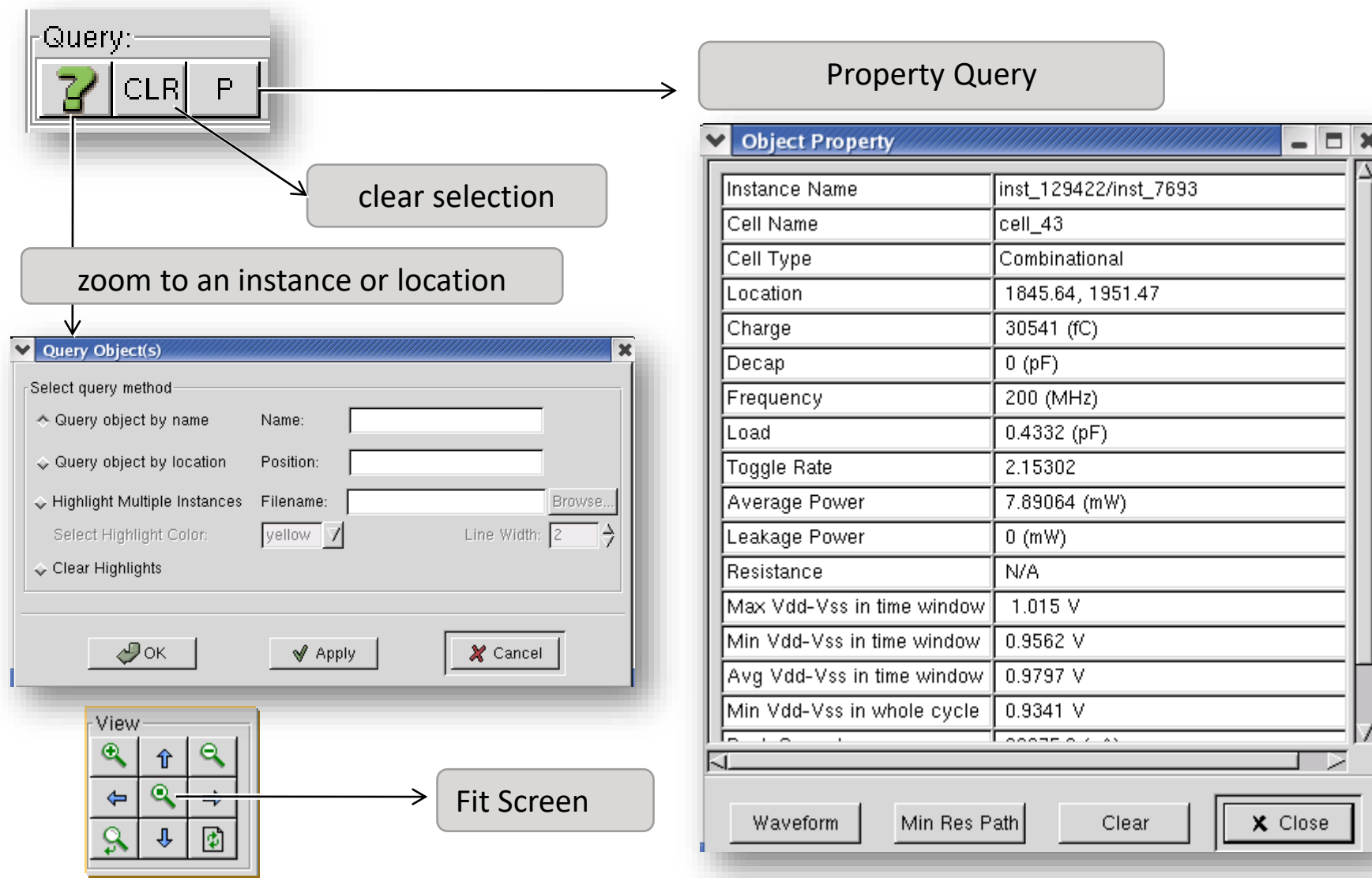
Viewing Selective Layers



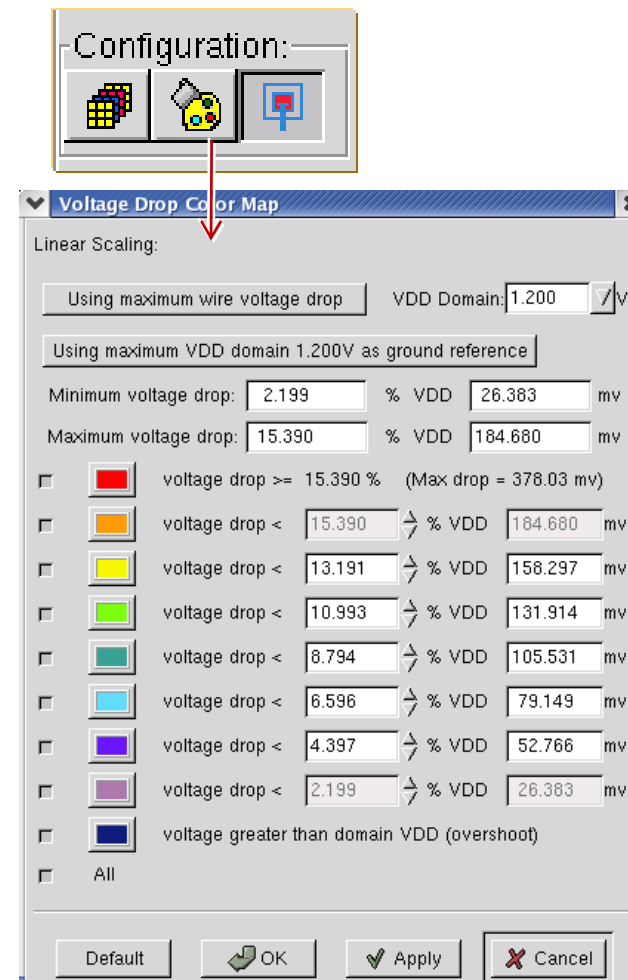
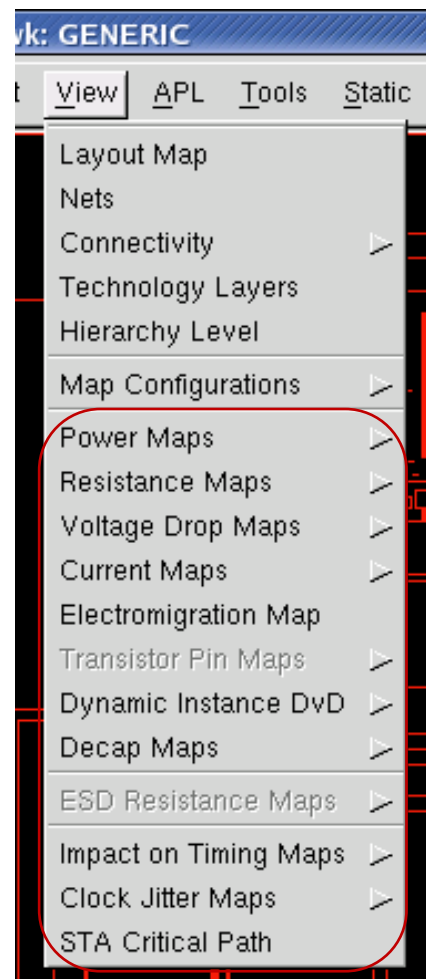
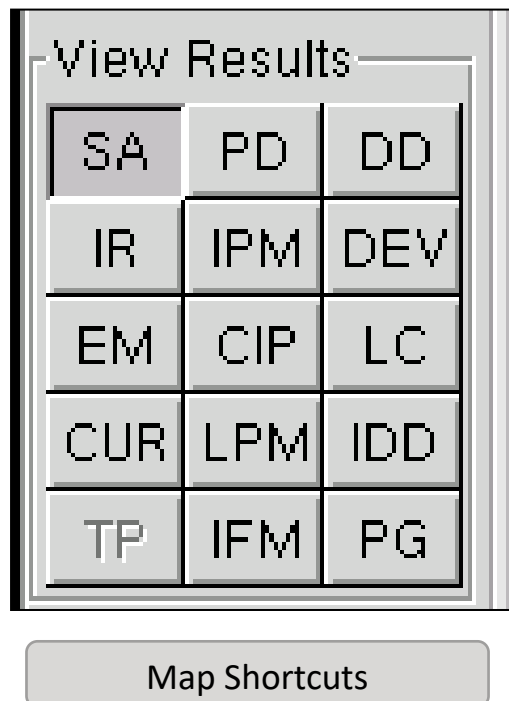
Viewing P/G Pads



/ Search / Query Options



Viewing Different Maps



Viewing Different GUI Reports

Log Message Viewer

Errors/Warnings Summary | CPU/Memory Usage | Setup Design | Power | Results

- Errors (3)
 - FLW-001 (1)
 - ITG-001 (1)
 - ITG-003 (1)
 - 3 referenced cells are not defined in both LIB and LEF.
- Info (121)
- Warnings (23902)

Log Message Summary Reports

Report of Worst Dynamic Voltage Drop Instances

List of Worst DvD Instance

No.	Ideal Vdd	Avg DV	Max DV	Min DV	Min DV WC	Location (x y)	Name
1.	1.2000	0.8249	1.0773	0.8249	0.8249	2194.20 3914.48	inst_129228/inst_467500
2.	1.2000	0.8253	0.8474	0.8253	0.8253	2279.76 3870.20	inst_129228/inst_376748
3.	1.2000	0.8267	0.8725	0.8250	0.8250	2106.57 3877.57	inst_129228/inst_467011
4.	1.2000	0.8268	0.8465	0.8240	0.8240	2260.44 3881.26	inst_129228/inst_376450
5.	1.2000	0.8270	0.8313	0.8270	0.8270	2075.06 3800.08	inst_129228/inst_466659
6.	1.2000	0.8273	0.8336	0.8265	0.8265	2282.75 3921.85	inst_129228/inst_376691
7.	1.2000	0.8273	0.8444	0.8267	0.8267	2087.48 3796.40	inst_129228/inst_466426
8.	1.2000	0.8273	1.0777	0.8262	0.8262	2303.68 3855.44	inst_129228/inst_464345
9.	1.2000	0.8273	0.8471	0.8262	0.8262	2051.60 3836.99	inst_129228/inst_457991
10.	1.2000	0.8277	1.0841	0.8267	0.8267	2190.29 3796.40	inst_129228/inst_508094
11.	1.2000	0.8278	0.8783	0.8252	0.8252	2115.54 3896.02	inst_129228/inst_466498
12.	1.2000	0.8279	0.8346	0.8279	0.8279	2155.33 3774.25	inst_129228/inst_440641
13.	1.2000	0.8284	0.8326	0.8262	0.8262	2100.36 3803.77	inst_129228/inst_466506
14.	1.2000	0.8284	0.8326	0.8262	0.8262	2429.72 3917.34	inst_129974/inst_494595
15.	1.2000	0.8284	0.8326	0.8262	0.8262	2432.02 3884.14	inst_129974/inst_489182
16.	1.2000	0.8284	0.8326	0.8262	0.8262	2041.71 3807.47	inst_129228/inst_458380
17.	1.2000	0.8295	0.8586	0.8294	0.8294	2174.88 3748.43	inst_129228/inst_440904

Vdd Domain: All SortBy: Avg Vdd-Vss Threshold: 5.00 % Apply

Zoom DvD Plot Up Down First Last Prev 1000 Next 1000 Cancel

Various List of Violations

total of 35 WARNINGS.
<adsRpt/Warn/redhawk.warn.2009-11-13-02:11:39> for details.

GE (import DEF): 639 MBytes
ME: 0 hrs 0 mins 40 secs
secs.
F-031): Numbers of DEF nets with types assigned based on their names: PWR(0) GND(0) CLK(0) ...

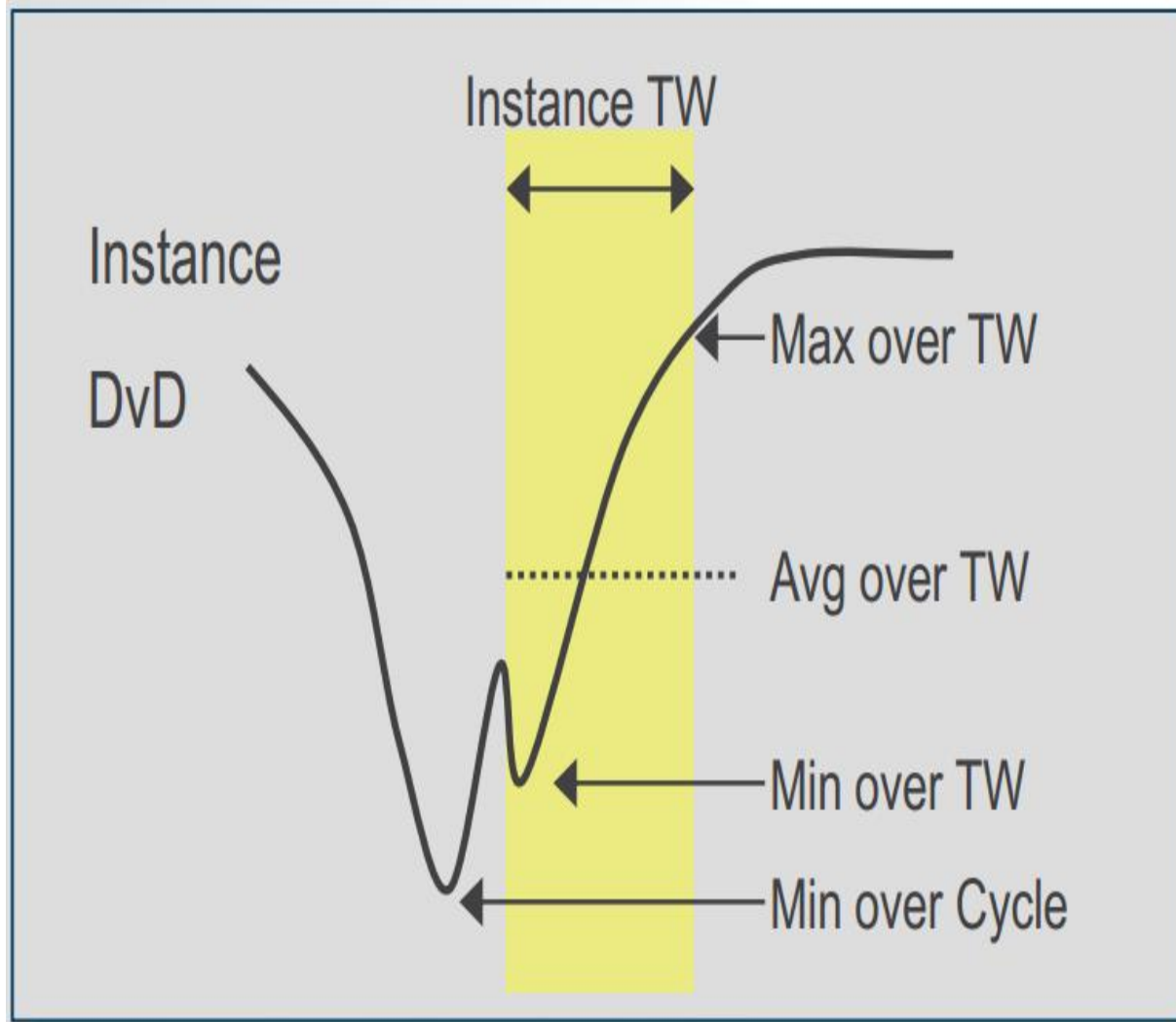
d viaModels used in the design, please refer to file "adsRpt/tech_summary.rpt".

: 7 pin-based gdsmem cells with pratio files.

grity checks on DB ...

Is are referenced in the design.
1): 23 referenced cells are not defined in LIB.
2): 30 referenced cells are not defined in both LIB and LEF.
3): 30 referenced cells don't have internal power defined in lib.

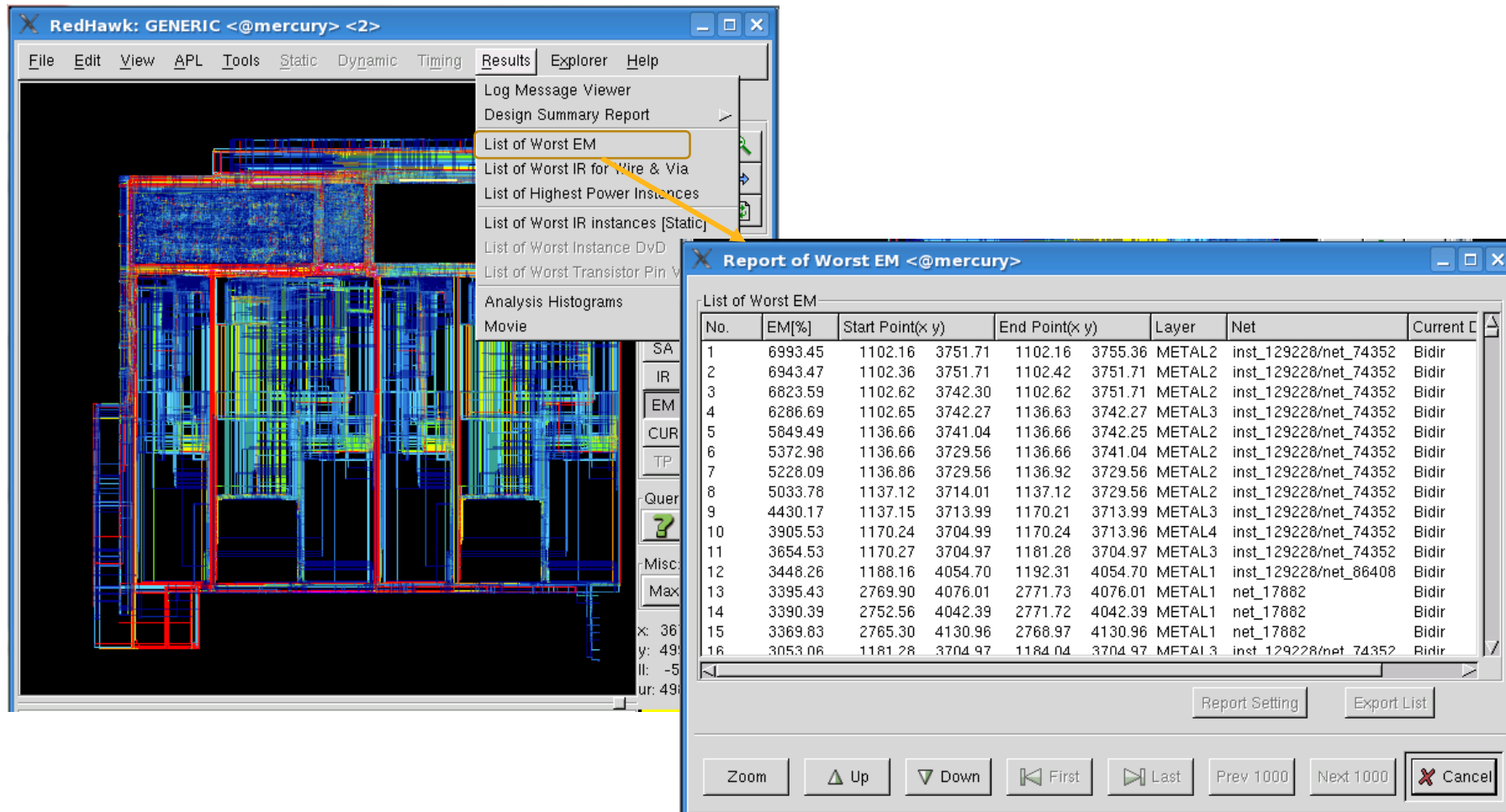
/ Types of Voltage drop



- Min over Cycle : MinWC : Worst drop for the whole simulation time
- Min over TW : MinTW : Worst drop within timing window of the instance .Worst drop when instance is switching
- Avg over TW : AvgTW : Average drop within timing window . AvgTW is typically used to give feedback to timing tool
- Max over TW : Max TW : Best drop in TW; Not much used

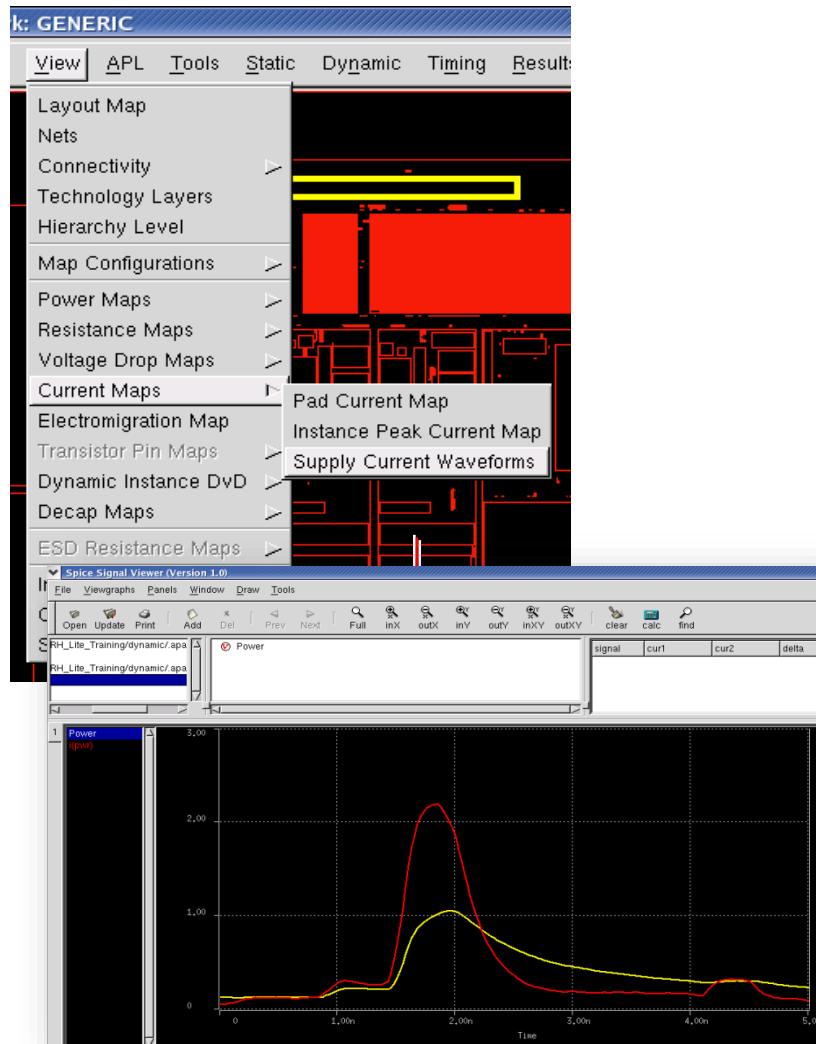
Electromigration Analysis

List of Worst EM report

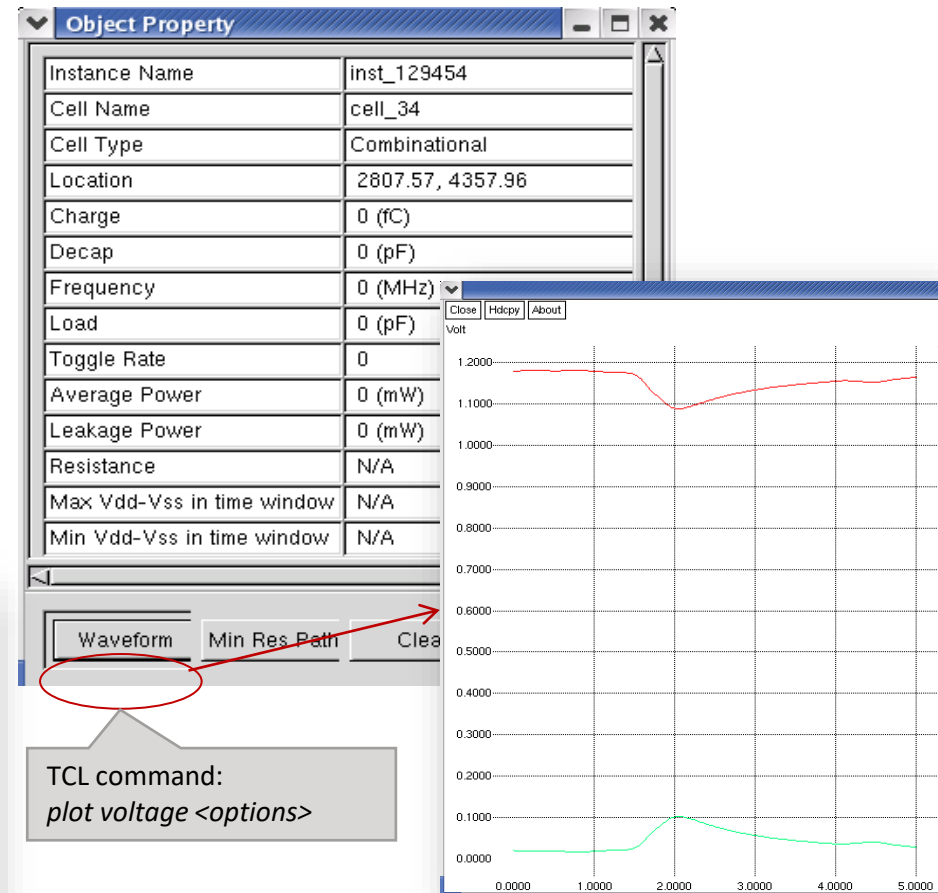


Viewing Different Waveforms

Current w/f



Voltage w/f

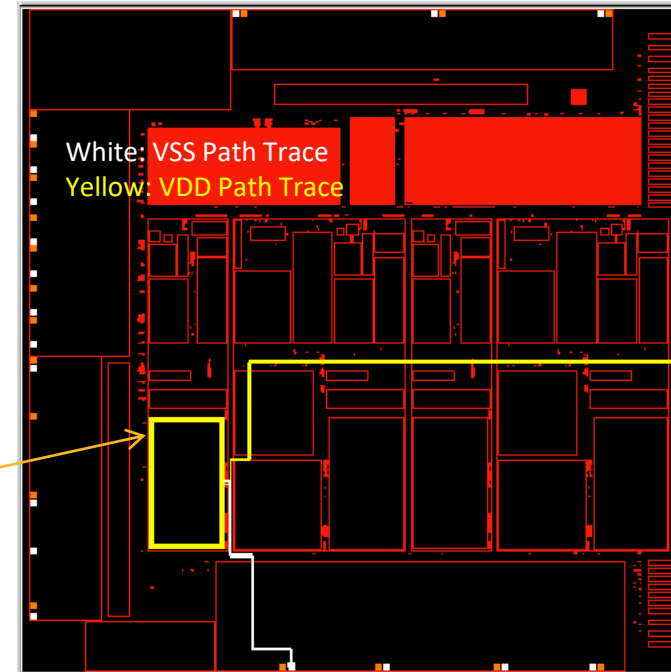
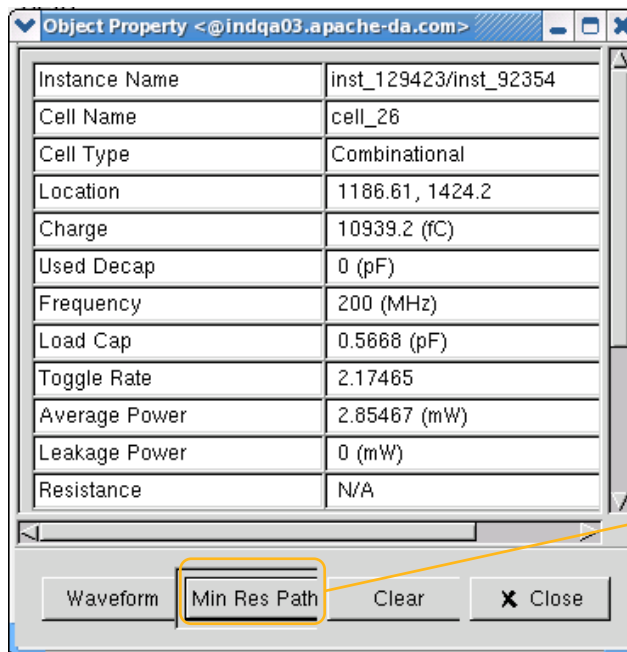


TCL command:
plot voltage <options>

TCL command:
plot current <options>

Minimum Resistance Path Tracing

- Traces the minimum resistance path to an instance from the electrically nearest voltage source point
- Can be invoked using Tcl Command : **'perform min_res_path path -inst <instName>'**
 - Displays minimum res path for all P/G pins in GUI
 - Generates a resistance report which will give the break-up of resistance and voltage drop across different wire/via segments in the path
- **Can also be invoked from Instance Property box window**



Important Text Reports

File	Description
adsRpt/redhawk.log	RedHawk log file
adsRpt/power_summary.rpt	Power Summary Report
adsRpt/<design>.power.rpt	Detailed Power Report
adsRpt/Static/<design>.inst.worst	Instance Static IR Report
adsRpt/Dynamic/<design>.dvd	Instance DVD Report
adsRpt/Static/<design>.em.worst	Wire EM Report

/ Commonly used TCL Commands

Command	Description
import db/export db	For importing and exporting the database
help	To get help on any TCL command
print type	Prints the cell type wise switching statistics
plot switching	Plots switching histogram
plot analysis	Plots analysis histograms
gsr get / gsr set	Queries / Assigns a GSR keyword parameter (supported only for selected keywords)
condition set -time/-xy/-type	Filters the analysis results to specified time/bbox or cell type

/ Instance & Cell Attribute Query Commands

Command	Switch
get inst \$inst	-master
	-freq
	-power
	-peak_current
	-resistance
	-decap
	-switching_status
	-bbox
	-location
	-orientation
	-voltage
get inst * -glob	Loops through all instances in the design

Command	Switch
get cell \$cell	-type
	-height
	-width
	-pins
	-pgarcs
get cell * -glob	Loops through all master cells in the library

/ Net & Pad Attribute Query Commands

Command	Switch
get net \$net	-ideal_voltage
	-worst_drop
	-worst_em
get net * -glob	Loops through all nets in the design

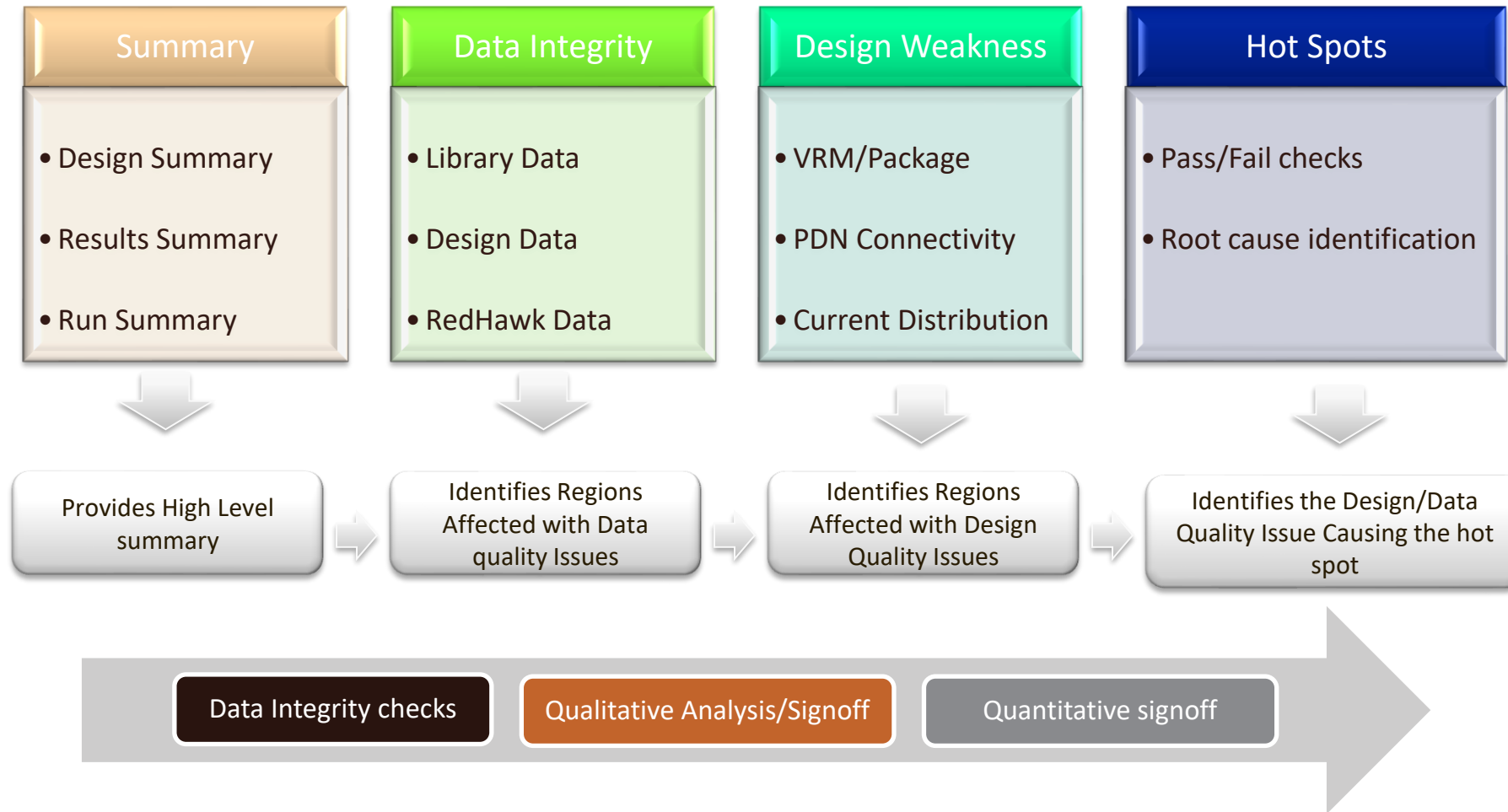
Command	Switch
get pad \$pad	-info
	-voltage
	-current
	-layer
	-location
	-net
get pad * -glob	Loops through all pads in the design

Result Analysis and Root Cause identification using RedHawk Explorer

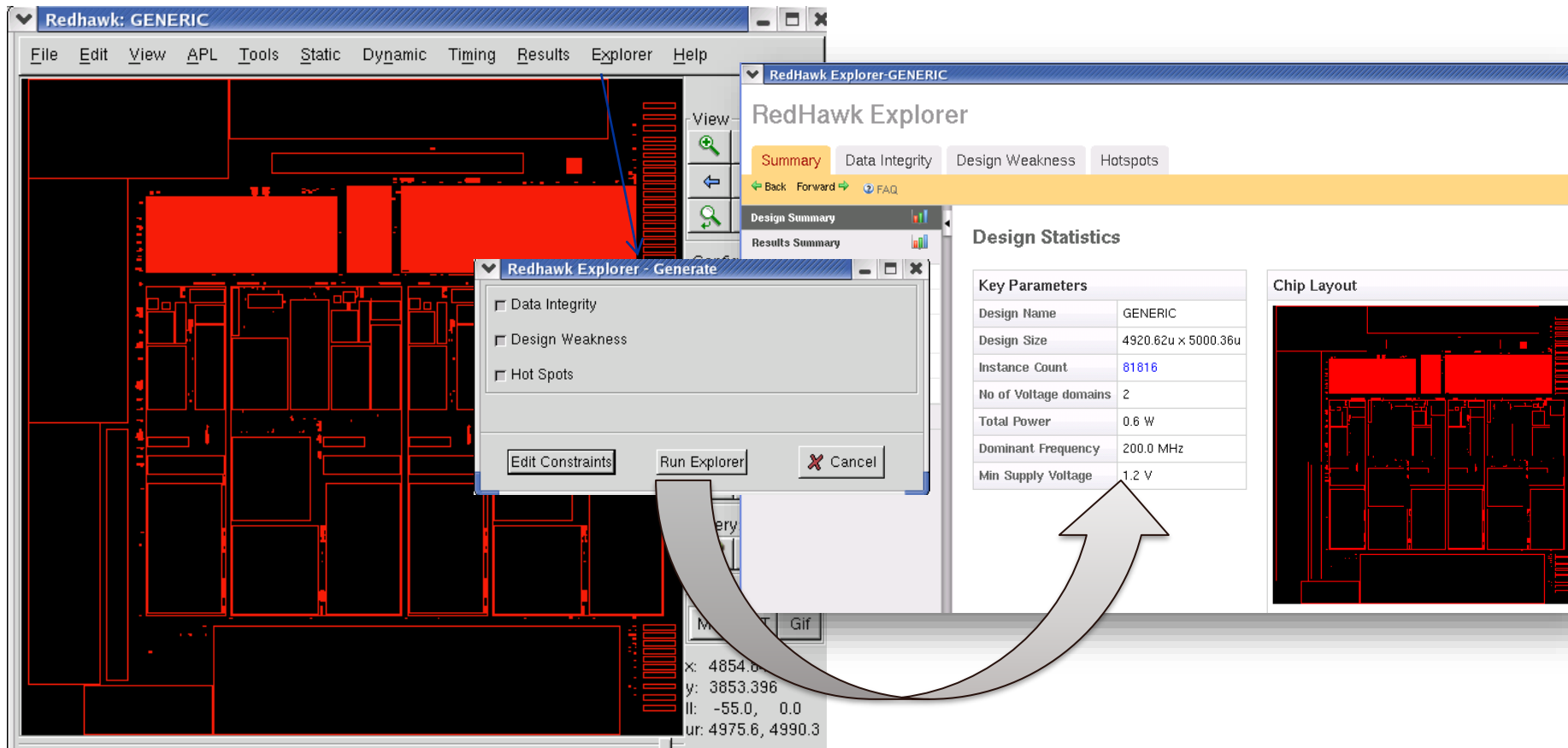


/ RedHawk Explorer Goals

- Explorer is a tool which helps in locating, isolating, understanding and resolving design/data issues causing hot-spots
- Tightly integrated with Redhawk GUI – Provides easy cross-probing capabilities



How do I run RedHawk Explorer ?



TCL Command: *explore design*
(can be executed at any stage after "*setup design*")

Summary Section

Redhawk Explorer

Summary

Data Integrity

Design Weakness

Hotspots

Back Forward

Design Summary

Results Summary

Power Summary

Static Voltage Drop Summary

Dynamic Voltage Drop Summary

Low Power Analysis Summary

Run Details

RHE Summary » Power Summary

Power Summary

Power Summary Break-up

Total Chip Power calculated: 0.6 W [Details](#)

Cell Type Based

Frequency Based

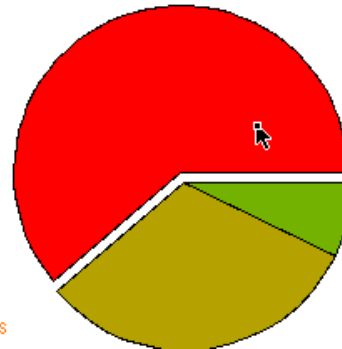
Voltage Domain Based

Power Component

Power Data

Celltype	Power
combinational	60.2 %
Others	0.7 %
_FF	31.7 %
inst	7.4 %

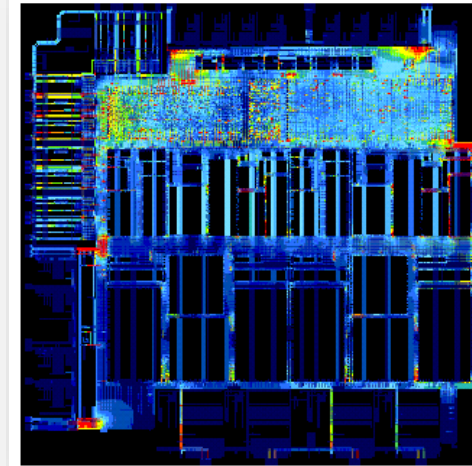
combinational



Others

Various Maps

Power EM Map



Run Details

RHE Summary » Run Summary

Run Details

RedHawk Version	10.2.2 Jan 20 00:41:35 2011
RedHawk Explorer Version	1.45
Run Directory	/home/aleena/RH_Lite_Training/dynamic_10.2
Machine Details	Linux mercury x86_64
Date of Execution	04 Feb 2011
Total Explorer Runtime	3.25 Mins

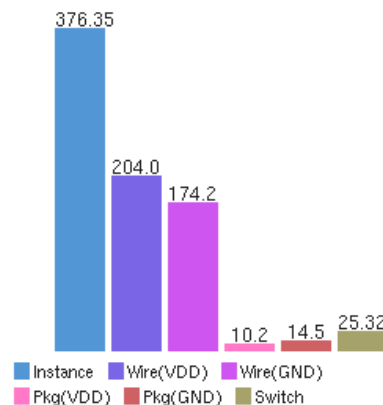
Summary Section

RHE Summary » DVD Summary

Worst Voltage Drop Data

Parameter	Value
Instance	376.35 mV (31.36 %)
Wire(VDD)	204.0 mV (17.0 %)
Wire(GND)	174.2 mV (14.51 %)
Pkg(VDD)	10.2 mV (0.8 %)
Pkg(GND)	14.5 mV (1.2 %)
Switch	25.32 mV (2.11 %)

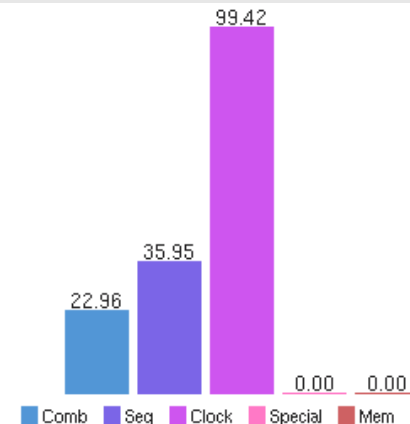
Voltage Drop Break up



Switching Activity

Type	Switching (%)
Combinational	13077/56964 (22.96%)
Sequential	5948/16547 (35.95%)
Clock	7324/7367 (99.42%)
Special	0/0 (0.00%)
Memory/IP	0/0 (0.00%)
Total	26349/80878 (32.58%)

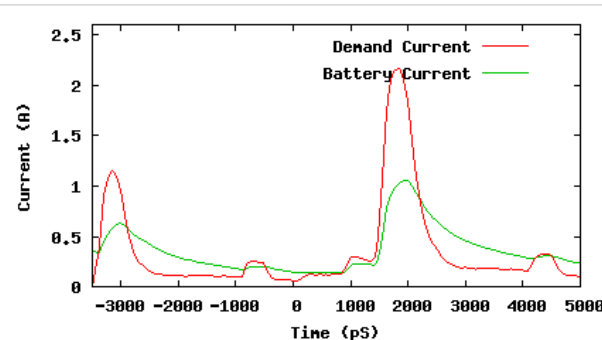
Tells what % of instances are switching in dynamic simulation



Waveform Data

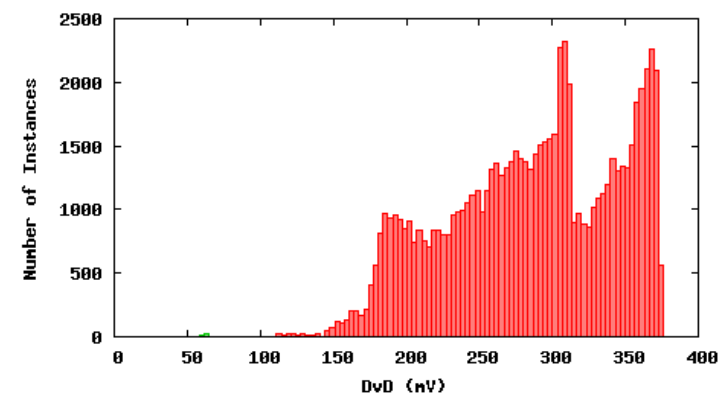
Type	Peak Value (mA)
Battery Current	1058.71
Demand Current	2170.39

Battery/Demand Current



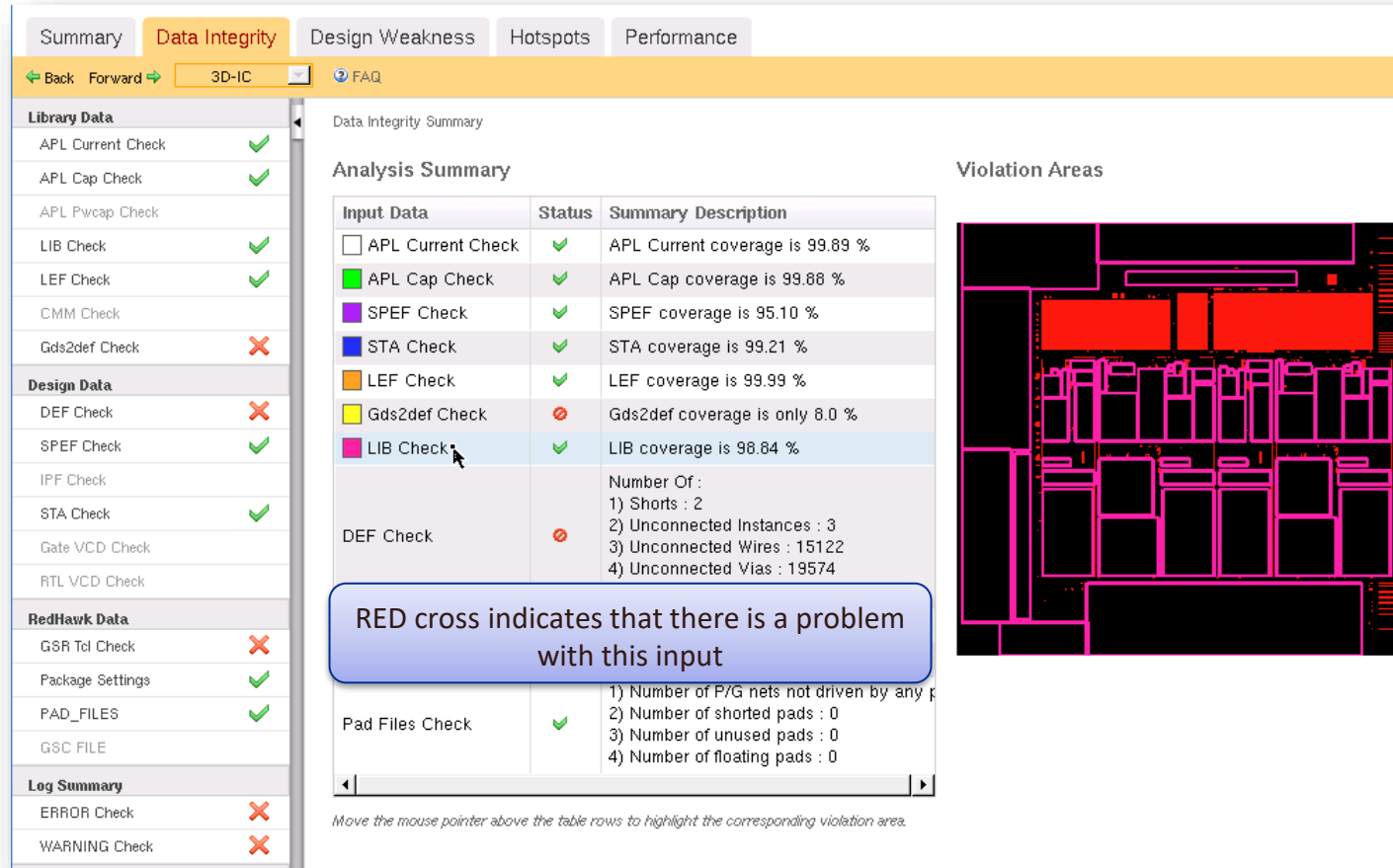
Demand Current and Battery current
Difference indicates decap current contribution

Instance Based DvD Histogram



Shows Analysis Histograms

Data Integrity Check Summary



- Design specific data integrity check
- Helps to identify and understand impact of missing data
- Breaks design into regions and presents missing data for each region

Library Data

APL Current Check

APL Cap Check

APL Pwcap Check

LIB Check

LEF Check

CMM Check

Gds2def Check

Design Data

DEF Check

SPEF Check

IPF Check

STA Check

Gate VCD Check

RTL VCD Check

RedHawk Data

GSR & TCL

Package Settings

PAD_FILES

GSC_FILE

Log Summary

ERROR Check

WARNING Check

Data Integrity Check Example : APL Cap Check

Data Integrity » Apl Cap Check

APL Coverage Details

Apl Cap Check ?

- Checks whether the APL Cap coverage in the design is at least 95%
- ✓ Number of instances with APL cap coverage: 80816/80917 (99.88 %)
- ✗ Number of cells with APL cap coverage: 199/234 (85.0 %)
- Apl Cap Area Coverage : 1.61722e+06/17342000.0 (9.32 %)

Highlights Regions with violations

Celltype Wise Coverage | Cross Probing

Celltype Wise Apl Cap Coverage

CellType	% Coverage/Total
Memory	- % (-/-)
Combinational	99.86 % (56910/56989)
Sequential	99.95 % (16542/16550)
Clock	100.00 % (7364/7364)
Others	- % (-/-)
FILLER/DECAP	0.00 % (0/14)
Decap	- % (-/-)
Total	99.88 % (80816/80917)

Provides cell-type wise classification

Data Integrity » Apl Cap Check » Missing FILLER/DECAP Cells
List of FILLER/DECAP Cells with Missing APL CAP Data

Cell	Number Of Instances
inst_92230_prog	4
cell_186	3
cell_189	3
inst_7642	2
inst_7644_prog	2

Provides a sorted list of cells based on number of instances

Apl Cap Coverage Violations Displayed
Highlighting Regions with APL cap coverage less than 95 % in GUI

Related Output Reports Section

Data Integrity » Apl Cap Check » Related Reports

Apl Cap Check ?

Provides pointers to relevant reports in adsRpt

Related Output Reports

Report	Line Count	Definition
adsRpt/apache.refCell.noAplCap	36	Provides list of cells with missing apl cap data
adsRpt/apache.refCell.mismatchAplCdev	1	This file includes cdev with missing or mismatched Power/Ground pins in LEF

- Presents relevant files in hyperlinked manner
- Describes and provides their content

Data Integrity » Apl Cap Check » Related Reports » [adsRpt/apache.refCell.noAplCap](#)

cell_10
cell_16
cell_17
cell_18
cell_2
cell_26
cell_28
cell_29
cell_36
cell_38
cell_43

DEF Check Example : Short Debug

Shorts Check Instance Unconnect Wire Uncon

SHORT CHECK
● Check the number of shorts in a design is not more than 0
❗ Number of shorts Reported : 2

Highlighting Regions with Shorts in GUI

Direct zoom into RH GUI by clicking on the image

Highlights Regions with shorts
(User can click and zoom into RH)

Exact short location highlighted with marker

Redhawk: GENERIC

File Edit View APL Tools Static Dynamic Timing Results Explorer Help

View

Configuration:

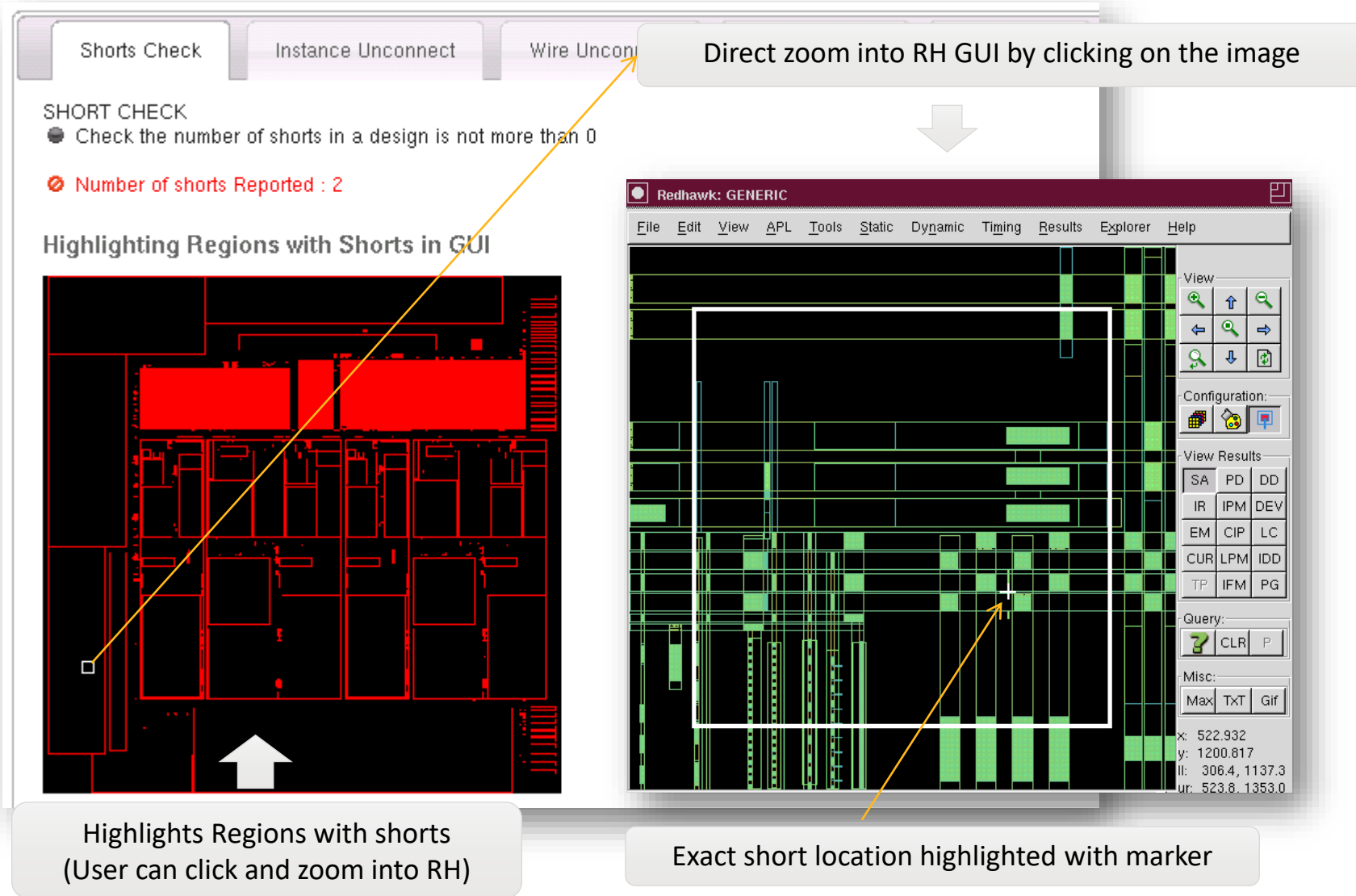
View Results

SA	PD	DD
IR	IPM	DEV
EM	CIP	LC
CUR	LPM	IDD
TP	IFM	PG

Query:

Misc:

x: 522.932
y: 1200.817
li: 306.4, 1137.3
ur: 523.8, 1353.0



DEF Check Example : Short Debug

Report of Shorts Area (BBOX=< 332.1 1162.3 498.1 1328.4>)

List of Shorts Area

No.	From Net	To Net	Layer	Location(II.x, II.y, ur.x, ur.y)
1	VSS	VDD	METAL5	457.129 1216.29 457.629 1223.29
2	VDD	VSS	METAL5	457.129 1216.29 457.629 1223.29

RedHawk: GENERIC

File Edit View APL Tools Static Dynamic Timing Results Explorer He

Net: All View by net Include G

Zoom Up Down First Last Prev 1000

RedHawk will also zoom into the rectangle with violations and add marker for all violations

RedHawk also pops up stepper window with list of violations within the zoomed rectangle

/ GSR / TCL Setting Checks

Data Integrity » GSR TCL Check

GSR TCL Check

● Performs Checks on GSR/TCL Parameters

GSR ::Parameter	Given Value/Total	Recommended Value/Total	Status
GSR::DYNAMIC_SIMULATION_TIME	5.0 ns	> 5.0 ns	✓
GSR::DYNAMIC_TIME_STEP	25 ps	5 ps - 100 ps	✓
GSR::DYNAMIC_PRESIM_TIME	3 ns	1 ns - 50 ns	✓
GSR::FREQUENCY	200.0 MHz	≈ 200.0 MHz	✓
GSR::CACHE_MODE	0	Set it to 1 if memory usage is a concern	✗
GSR::DYNAMIC_SAVE_WAVEFORM	1		
GSR: DECAP_CELLS	NOT GIVEN/COMMENTED		
GSR: INPUT_TRANSITION	3e-10		
GSR::TOGGLE_RATE	AVG_CLOCK_TOGGLE_RATE : 1.21 AVG_SIGNAL_TOGGLE_RATE : 0.24		

Related GSR Keywords

GSR Keyword	Status
BLOCK_POWER_FOR_SCALING	DETAILS
BLOCK_POWER_FOR_SCALING_FILE	-
BLOCK_POWER_ASSIGNMENT	-
INSTANCE_POWER_FILE	-
TOGGLE_RATE	0.15
INSTANCE_TOGGLE_RATE	-
INSTANCE_TOGGLE_RATE_FILE	-
BLOCK_TOGGLE_RATE	-
BLOCK_TOGGLE_RATE_FILE	-
SCALE_CLOCK_POWER	0
SCALE_TOGGLE_RATE	0
VCD_FILE	-
GSC_FILE	-
GSC_OVERRIDE_IPF	0
STATE_PROPAGATION	-
BLOCK_VCD_FILE	-
BLOCK_TOGGLE_FILE	-

Common mistakes made in GSR/TCL
are identified here

Design Weakness Exploration

Summary

Data Integrity

Design Weakness

Hotspots

Performance

Back

Forward

FAQ

VRM/Package Checks

Pad Placement Quality

Package Drop Contribution

PDN Related Checks

PG Resistance Distribution

PG Resistance Imbalance

Switch Placement Quality

Decap Distribution

Current Related Checks

Power Distribution Quality

Clock Buffer Clustering

Peak Current

Simultaneous Switching

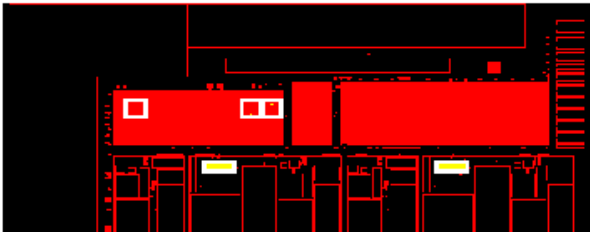
Design Weakness Summary

Analysis Summary

Parameter	Summary Description
<input type="checkbox"/> POWER DISTRIBUTION QUALITY	Percentage of violating regions : 3/329 (0 %)
<input checked="" type="checkbox"/> PAD PLACEMENT QUALITY	Percentage of violating regions : 9/44 (20 %)
<input checked="" type="checkbox"/> CLOCK BUFFER CLUSTERING CHECK	Percentage of violating regions : 1/108 (0 %)
<input checked="" type="checkbox"/> PG RESISTANCE DISTRIBUTION	Percentage of violating regions : 42/304 (13 %)
<input checked="" type="checkbox"/> PG RESISTANCE IMBALANCE	Percentage of violating regions : 55/85 (65 %)
<input checked="" type="checkbox"/> PEAK CURRENT DISTRIBUTION	Percentage of violating regions : 6/329 (1 %)
<input checked="" type="checkbox"/> DECAP DISTRIBUTION	Number of Violating Non-Zero Decap Regions : 1/108 (0 %)
<input type="checkbox"/> SIMULTANEOUS SWITCHING CHECK	Percentage Switching Activity = 32.58 % Peak Demand Current to Average Current Ratio : 1.5
<input type="checkbox"/> PACKAGE DROP CONTRIBUTION	Worst Package Drop For Power Domain : 0.000000 V Worst Package Drop For Ground Domain : 0.000000 V

Move the mouse pointer above the table rows to highlight the corresponding violation area.

Violation Areas



VRM/Package Related

Pad Placement Quality Check

Package Drop Contribution

PDN Related

PG Resistance Distribution

PG Resistance Balancing

Switch Placement Quality Check

Decap Distribution Check

Current Related

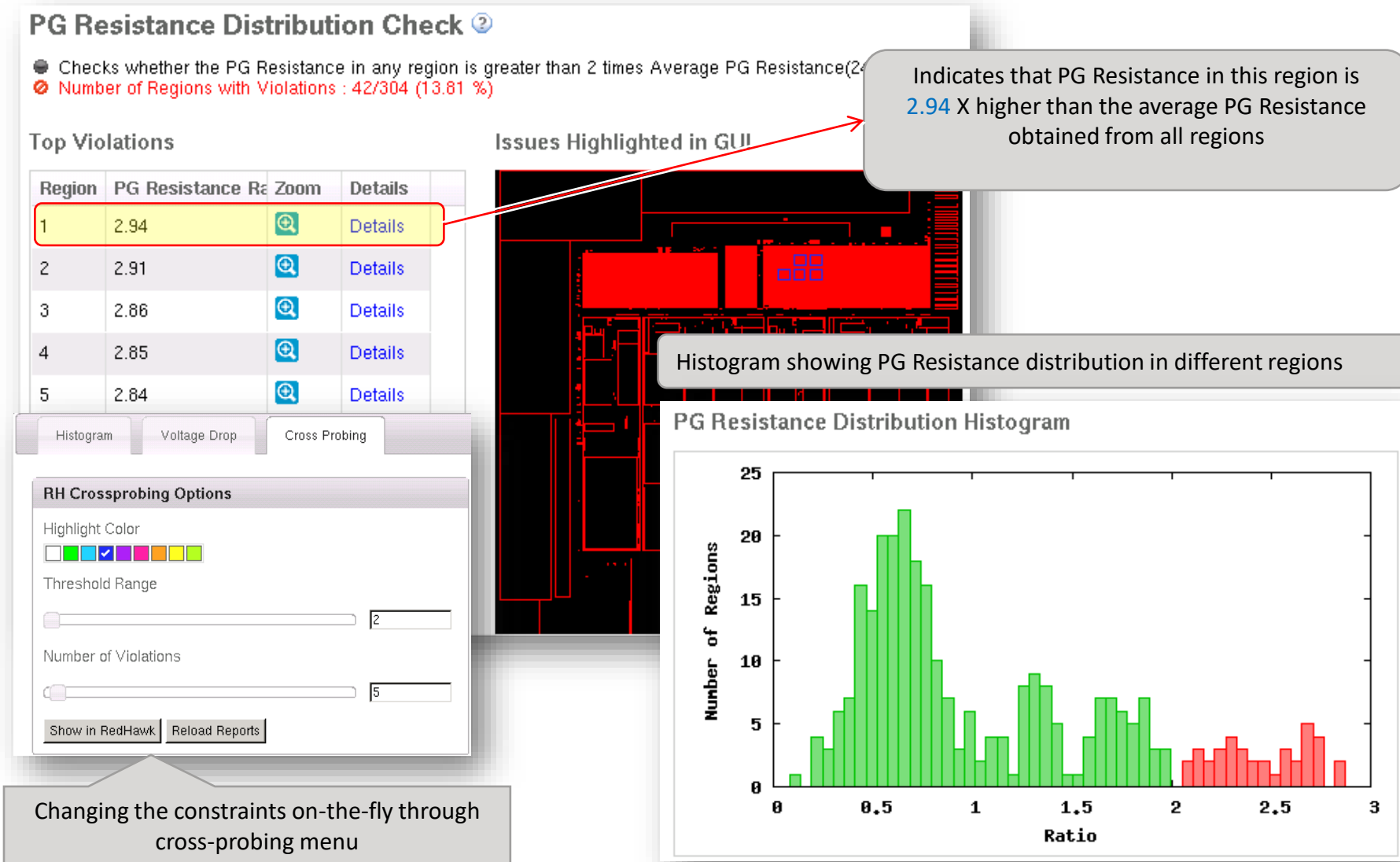
Power Distribution Quality

Clock Buffer Clustering

Peak Current Check

Simultaneous Switching Check

Design Weakness Analysis Example : PG Resistance Distribution Check



Changing the Constraints

Using constraint editor
(Before running RHE)



Using RHE GUI
(After running RHE)



Using Text Editor
(Before running RHE)

- vi adsRHE/rhe_threshold.rpt
- Edit the constraints you want
- explore design -constraint_file <new_thresh_file>



```
set rhe_bucket_size 50
set rhe_enable_DWE 1
set rhe_enable_DIE 1
set rhe_enable_HSE 1
set rhe_dvd_check_type minWC

##### DWE Thresholds #####

# Power_distribution_quality_check
# Checks whether the power density in any bucket is

set rhe_enable_power_distribution_check 1
set rhe_bucket_power_density_ratio 5
set rhe_num_violations_power_density_max 5
```





Cross-probing violations in RedHawk GUI

PG Resistance Distribution Check ?

● Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.350 ohm)

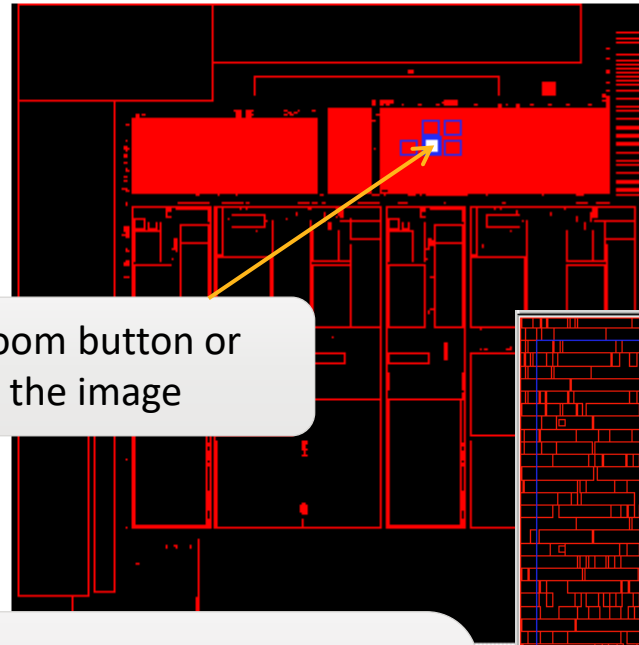
❗ Number of Regions with Violations : 42/304 (13.81 %)

Top Violations

Region	PG Resistance Ratio	Zoom	Details
1	2.94		Details
2	2.91		Details
3	2.86		Details
4	2.85		Details
5	2.84		

Move the mouse pointer
to highlight the corresponding region

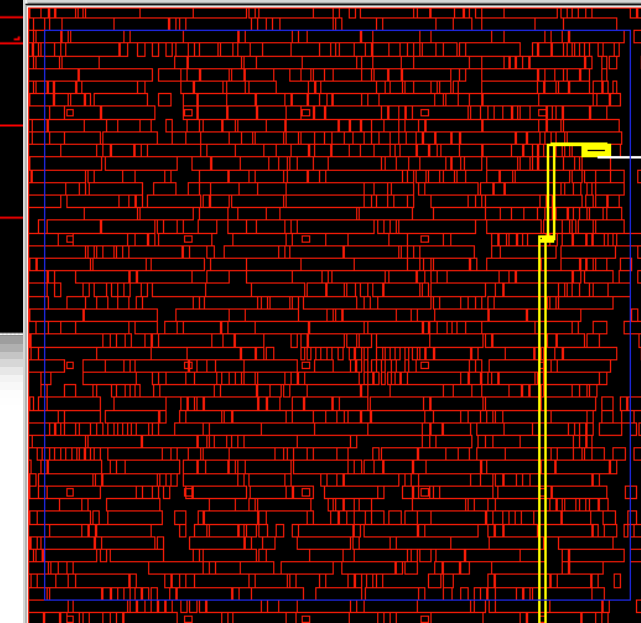
Issues Highlighted in GUI



User can click on zoom button or
directly click on the image

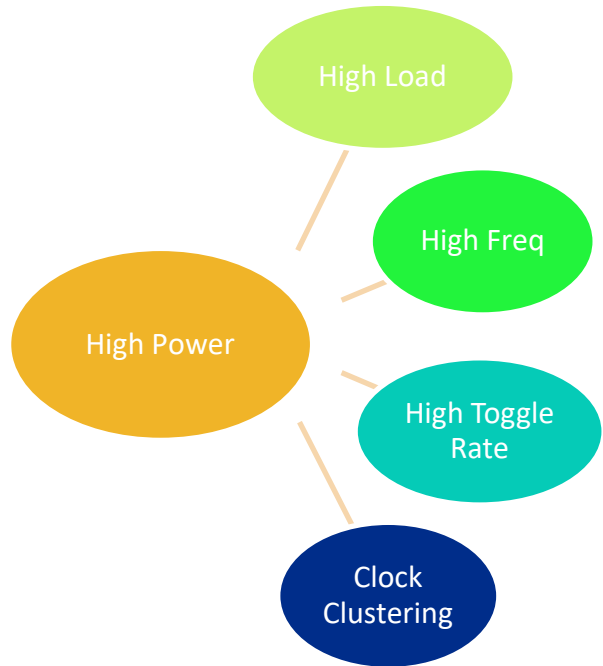
When you click on the image, RH/RHE does 3 things:

- Zooms into the violating regions
- Highlights the worst instance within the regions
- Update the map with some relevant views
 - Example, PG resistance map will display SPT for the worst instance

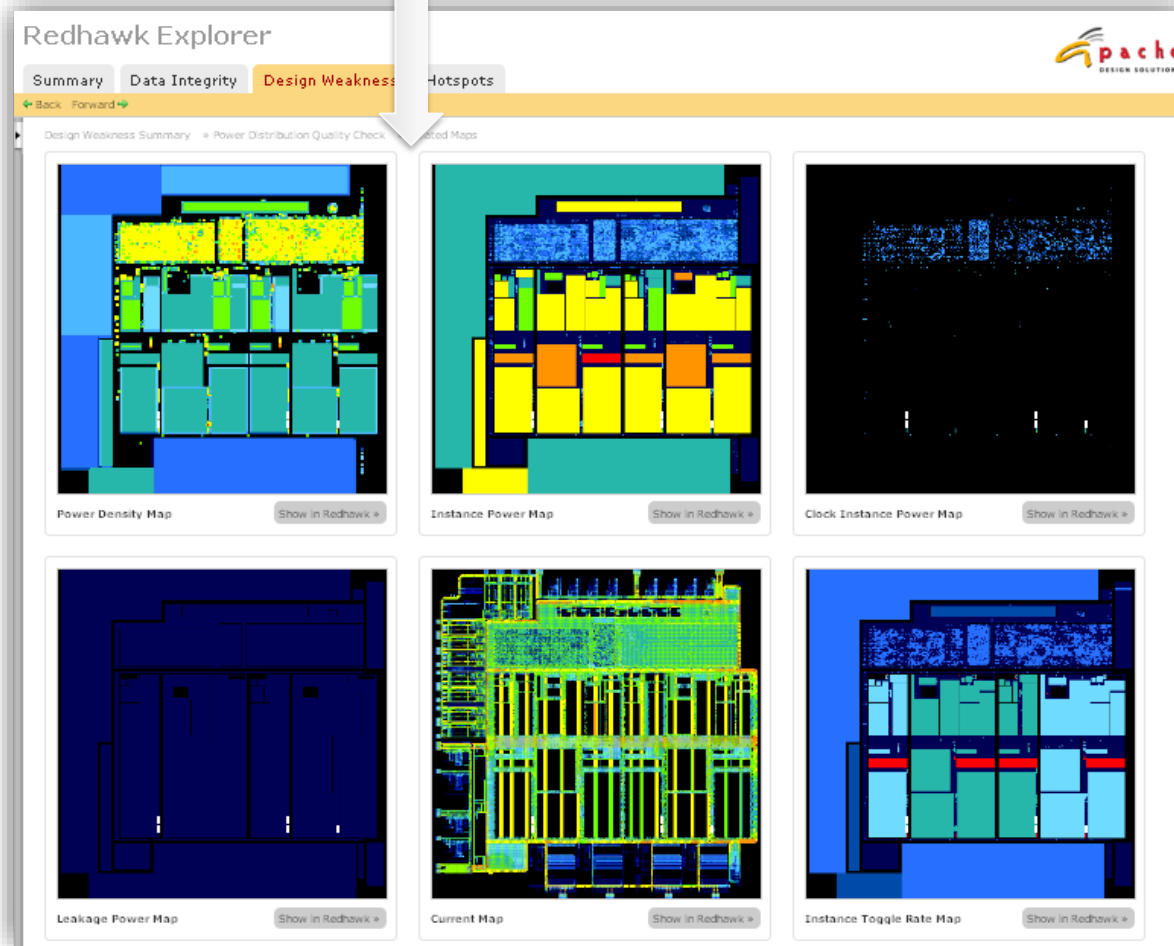


/ Design Weakness Analysis : Related Maps Section

Design Weakness -> Power Distribution Quality -> Related Maps



Related maps section helps identifying the exact cause for a weakness



Q & A Session



Getting Help on a Specific Item

Design Weakness » Simultaneous Switching Check

Simultaneous Switching Check



Design Weakness » Simultaneous Switching Check » Help On Simultaneous Switching Check

Simultaneous Switching Checks

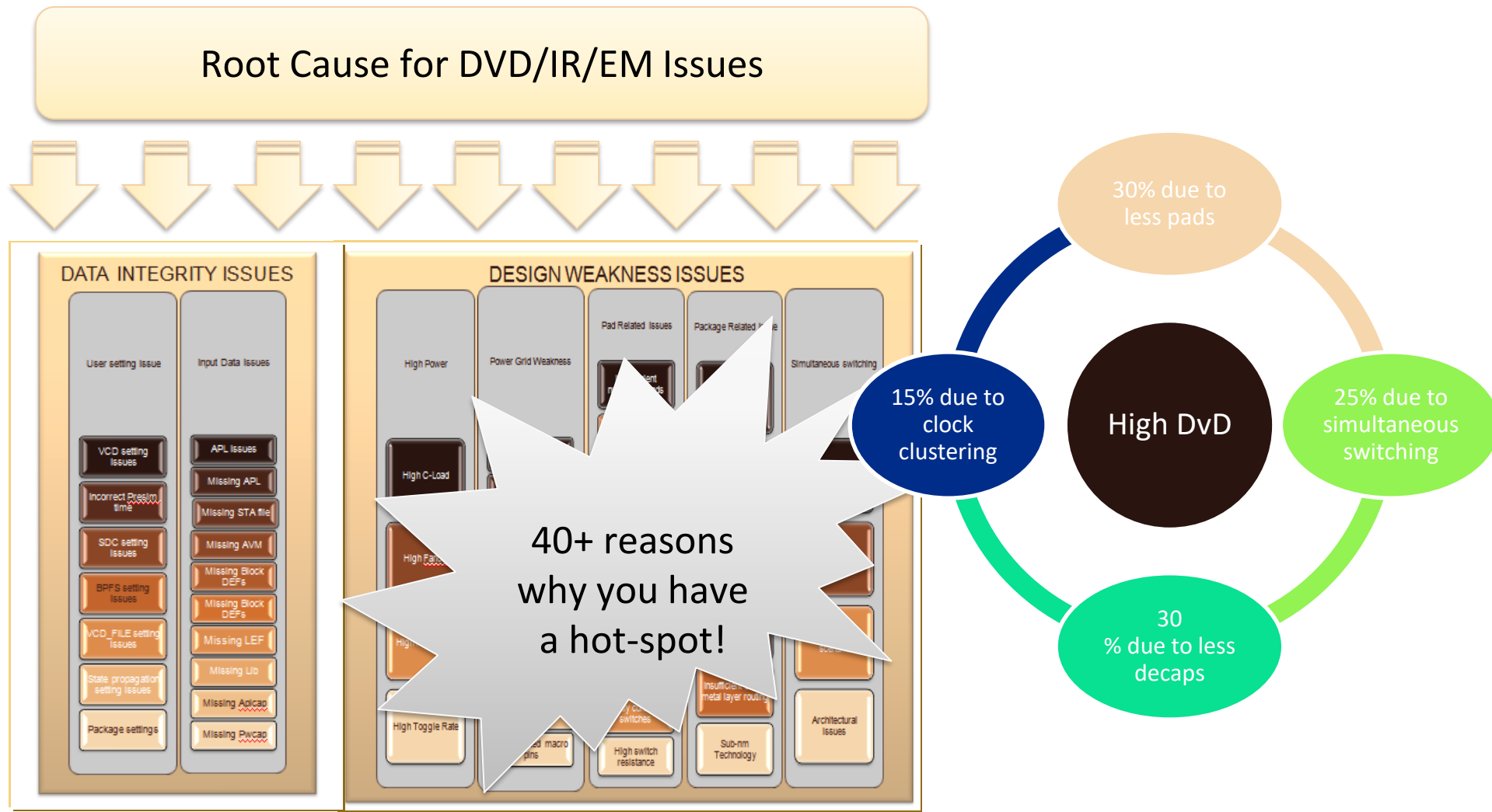
Various checks performed in this section are :

1. Overall switching activity
2. Peak current to Average current ratio
3. Switching event clustering

In Overall switching activity check, Redhawk checks whether the percentage of instances which are switching in dynamic simulation is reasonable. In Vectorless simulations, Redhawk come up with the switching scenario based on the average power target. If the power target specified in the GSR is too low, it can create very less switching in the simulation causing very low voltage drop. If the power target is too high, the switching scenario also will be very pessimistic leading to very high voltage drop. By default, a violation is reported if the switching activity is outside 10% - 40% range. You can change this range through constraint editor.

In peak current to average current ratio check, Redhawk checks whether there is global simultaneous switching issue in the design causing very high peak current. A typical example is scan-shift scenario, where all flops in the design can switch together almost at the same time along with the clock buffers causing huge peak current. Typically scan-shift operation is performed at very low frequency, say 20MHz, so when you average out this current waveform for the whole period (50ns), average current computed will be very less. Static voltage drop simulation is based on this average current, so you may notice low voltage drop in the static simulation. But, in dynamic simulation, we consider the real peak current, so voltage drop values can be very high. If you notice huge difference between your static voltage drop and dynamic voltage drop, it is advised to look at this particular check to find out the real reason. In this check, Redhawk will flag a violation if the peak current to average current ratio is more than 10X.

Power Noise : Root Cause Identification



Hot Spot Analysis

The screenshot displays the 'Hotspots' tab in a software interface. On the left, a sidebar lists various signoff checks: Dynamic Voltage Drop Check (marked with a red X), Static IR Check, Power EM Check (marked with a red X), Low Power Check, Voltage & Current w/f, Differential Voltage Check, Noise Coupling Check, Switch Id-sat Check, Switch Off State Check, Thermal Check, and EMI Emission Check. An orange callout box labeled 'Various signoff checks' points to this list.

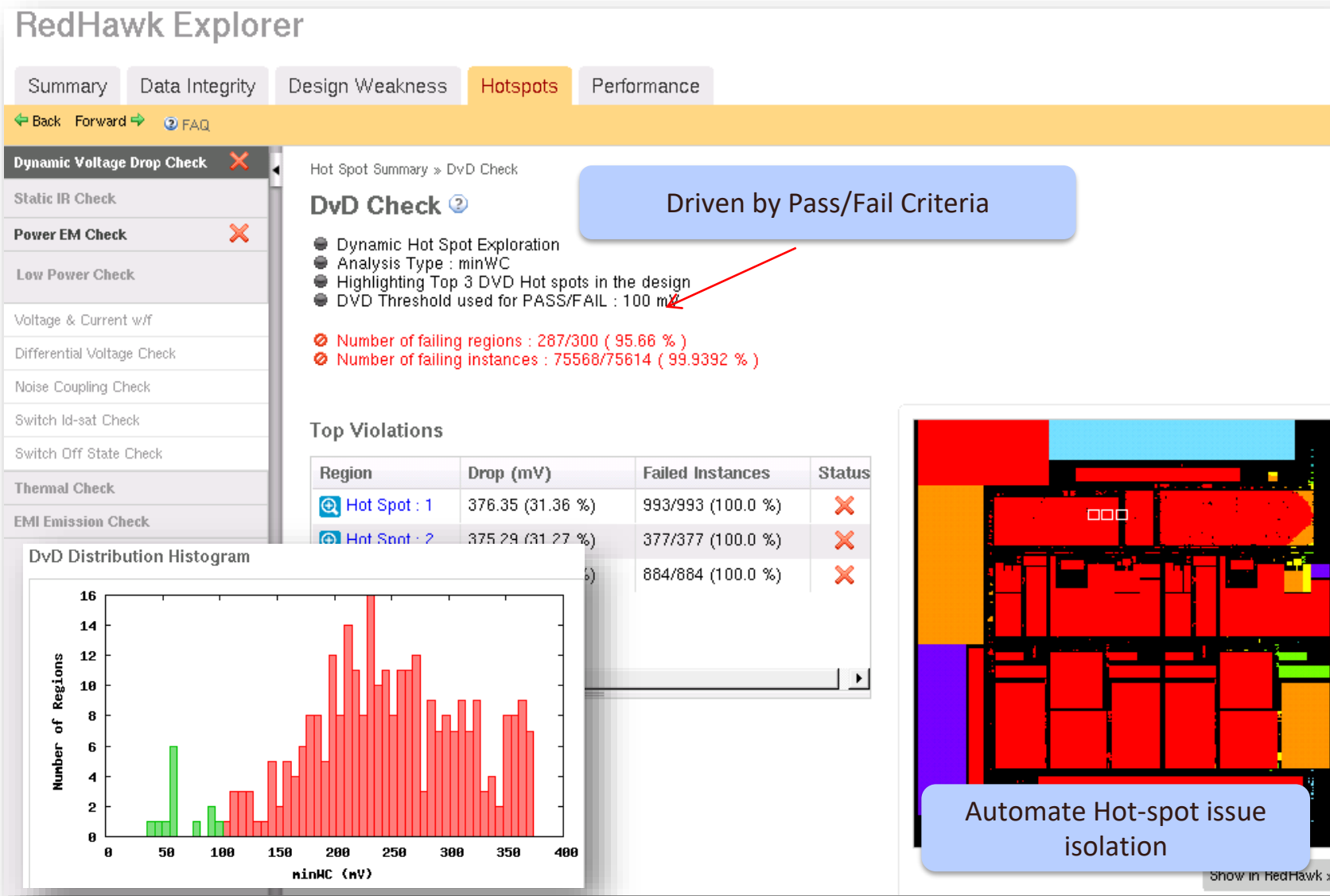
The main panel shows the 'HotSpot Summary' and 'Analysis Summary' sections. The 'Analysis Summary' table is as follows:

Parameter	Summary Description
<input type="checkbox"/> Dynamic Voltage Drop Check	Worst DvD Drop : 376.35 mV
<input checked="" type="checkbox"/> Static IR CHECK	Check Not Performed
<input checked="" type="checkbox"/> Power EM CHECK	Worst EM violation : 5933.70 %
<input type="checkbox"/> Low Power CHECK	Check Not Performed

Below the table, a note states: 'Move the mouse pointer above the table rows to highlight the corresponding Hotspots'.

The 'Violation Areas' section shows a heatmap of a circuit board layout. An orange callout box labeled 'DVD Hotspots highlighted here' points to a large red rectangular area at the top of the layout. Several yellow squares are also visible on the layout, indicating other violation areas.

Hot Spot Analysis



Hot Spot Analysis : Checking Hot-spot #1

Top Violations

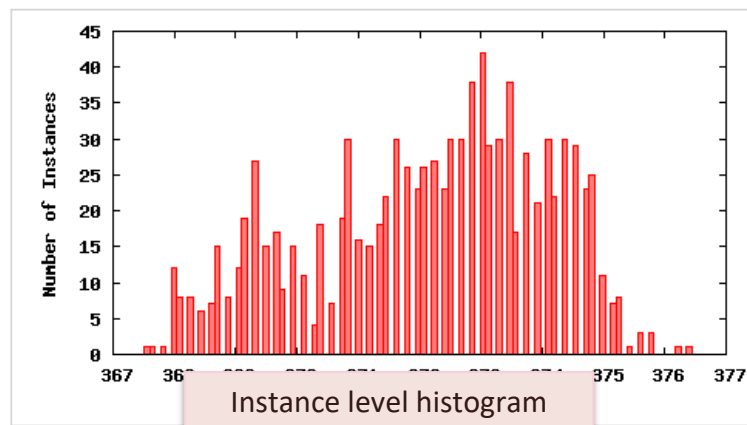
Region	Drop (mV)	Failed Instances	Status
Hot Spot : 1	376.35 (31.36 %)	993/993 (100.0 %)	✗
Hot Spot : 2	375.13 (31.27 %)	377/377 (100.0 %)	✗
Hot Spot : 3	375.13 (31.26 %)	884/884 (100.0 %)	✗

DvD Check

- Dynamic Hot Spot Exploration inside HOT SPOT : 1
- Hot spot region : 2159.01 3820.38 2336.57 3986.43
- Instance Threshold used for PASS/FAIL : 100 mV
- ✗ Number of instances failing : 993/993 (100.0 %)
- Displaying Top 1 instances inside this HOT SPOT

Instance	DROP (mV)	Status
Hot Instance : 1	376.35 (31.36 %)	✗

Dynamic Drop Histogram inside Region : 1



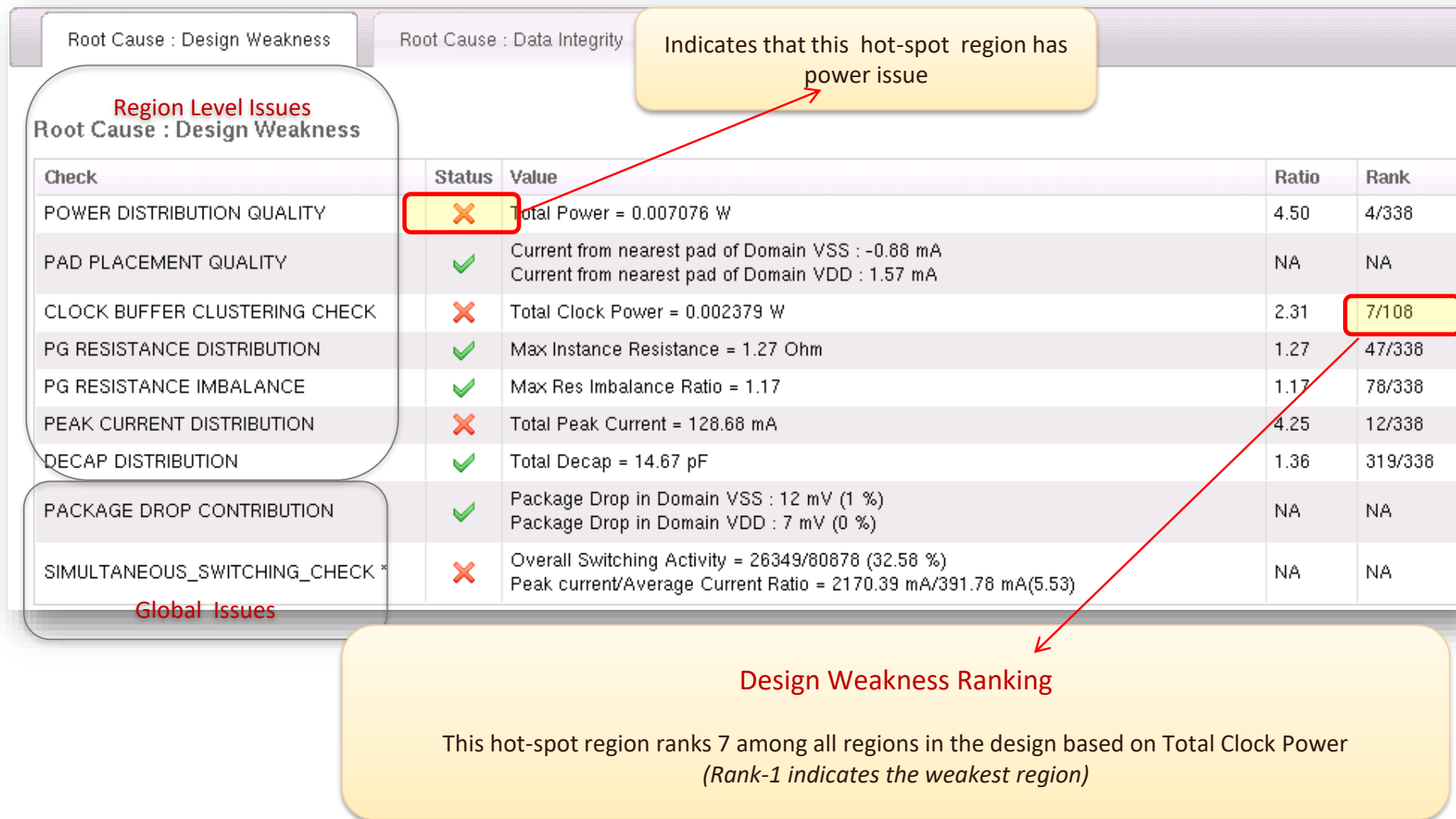
Detailed analysis inside the region

HotSpot Map

DVD HOTSPOT MAP



Root Cause Identification : Design Weakness Analysis



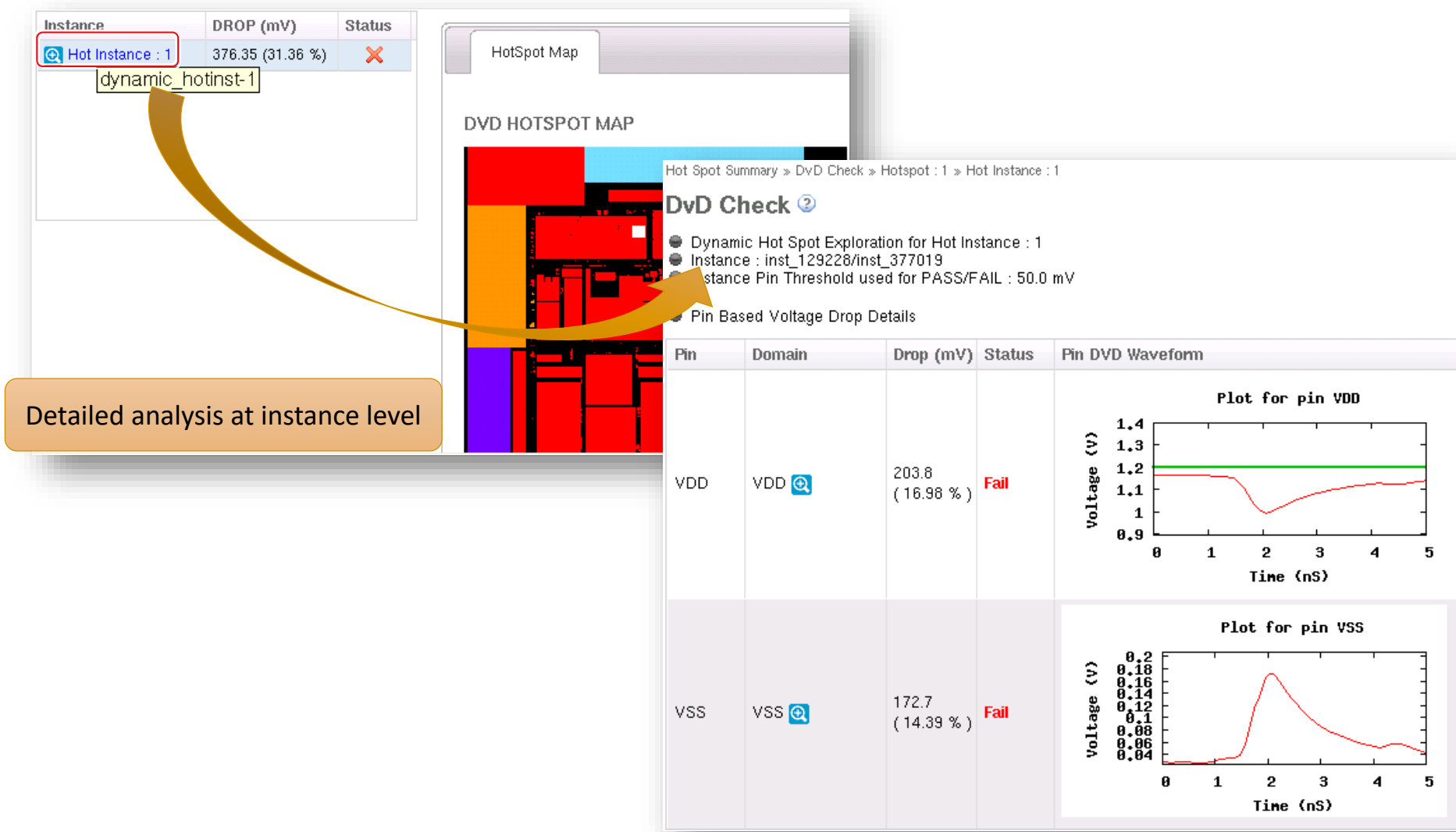
/ Root Cause Identification : Data Integrity Checking

Region Level Data Integrity Analysis

Root Cause : Design Weakness			
Root Cause : Data Integrity			
Histogram			
Root Cause : Data Integrity			
Check	Result	Value	Percentage
APL CURRENT CHECK	✓	1035/1041	99.42
APL CAP CHECK	✓	1041/1041	100.00
SPEF CHECK	✓	968/1041	92.99
STA CHECK	✓	1034/1041	99.33
LEF CHECK	✓	1041/1041	100.00
LIB CHECK	✓	1041/1041	100.00

SPEF coverage in this region is only 93 %

Hot Spot Analysis at Instance Level



Hot Spot Analysis : Instance Level Debug

Properties		Data Integrity	Design
Instance Properties			
Cellname	cell_722		
Peak Current	VDD 1160.4 uA VSS 1160.04 uA		
Decap	0.0343271 pF		
Frequency	2e+08 Hz		
Fanout	2		
Load	0.131717 pF		
Switching Status	Switching		
Average Power	2.67204e-06 W		
Leakage Power	3.44196e-09 W		
Toggle Rate	0.112374		

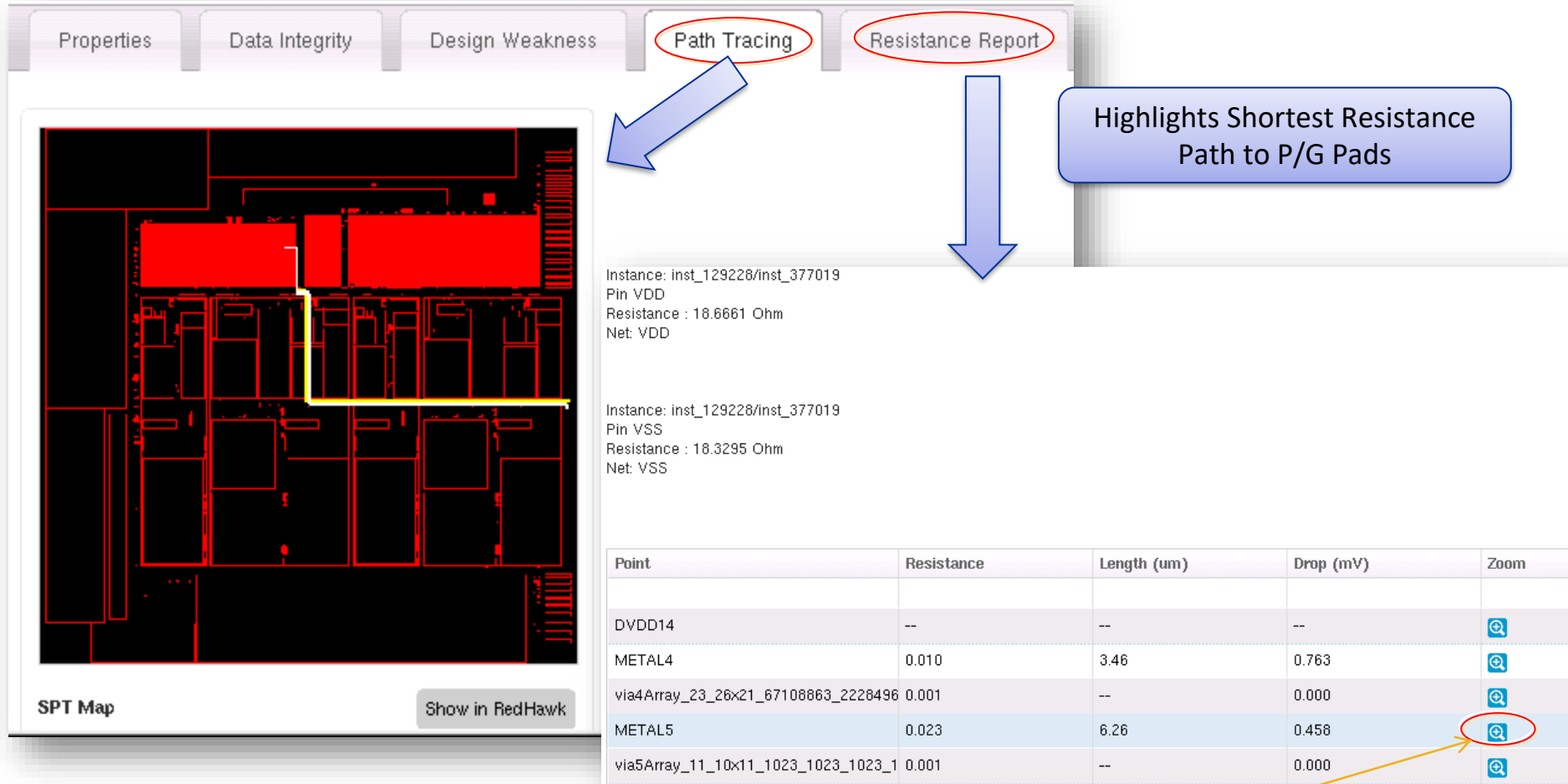
Properties		Data Integrity
Data Integrity		
Data	Status	
Apl Current	✓	
Apl Cap	✓	
Apl Pwcap	NA	
Lef	✓	
Lib	✓	
Sta	✓	
Spf	✗	
Gds2def	NA	

Properties		Data Integrity	Design Weakness
Design Weakness			
Check	Status	Value	Rank
Peak Current	✗	1160.4 uA	4/1041
Resistance	✓	36.9957 Ohm	528/1041
Power	✓	2.67204e-06 W	467/1041
Load	✗	0.131717 pF	4/1041

Missing Spf

This hot instance has high
peak current
Load is high causing high
current !!

Shortest Path Tracing



Equivalent Tcl Command:

```
perform min_res_path -o res_path.rpt
```

/ Explorer Command Line Options and Log Details

Command	Description
explore design	Runs Explorer and Pops up GUI
explore design -view	Pops up Explorer GUI
explore design -off	Closes Explorer GUI
explore design -constraint_file <cons_file>	Runs Explorer with a user specified constraint file

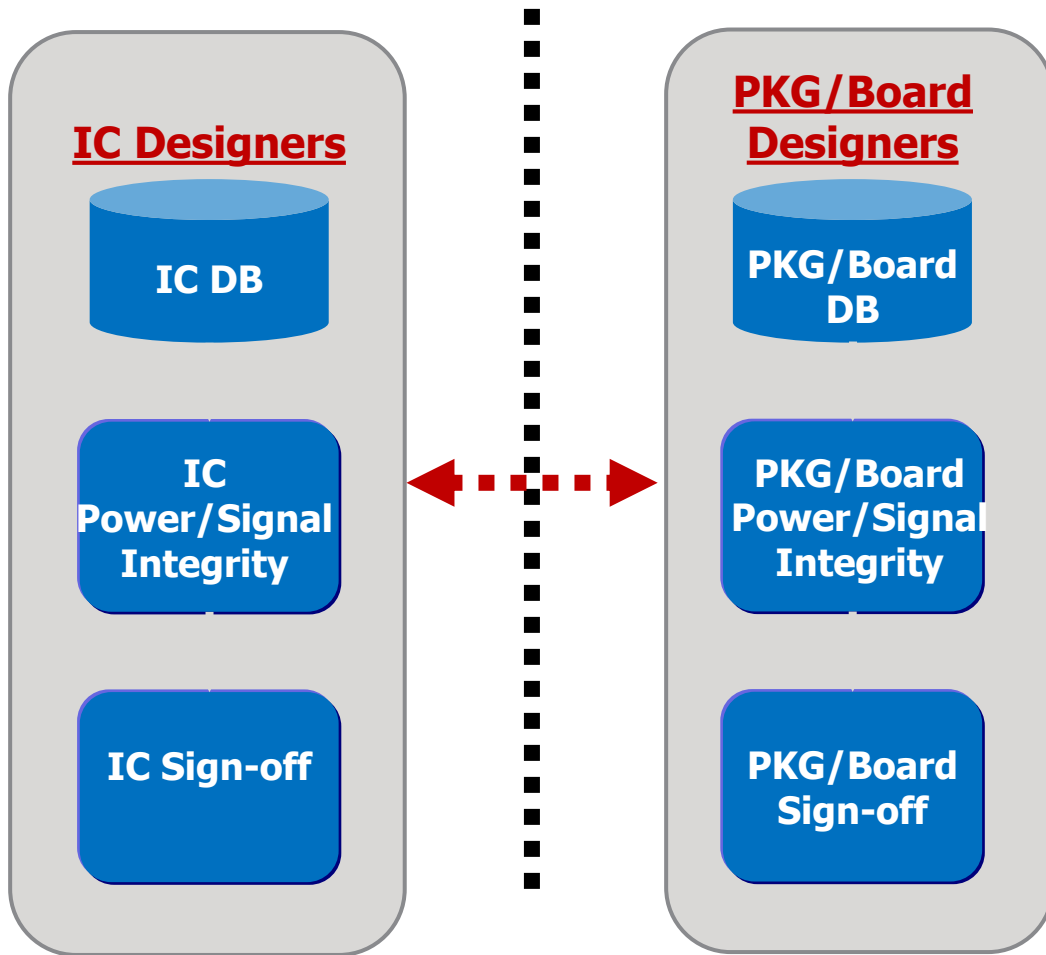
Log File	Description
adsRHE/adsRHE.log	Central summary Log
adsRHE/adsDWE/adsDWE.log	Design Weakness Analysis Log
adsRHE/adsDIE/adsDIE.log	Data Integrity Analysis Log
adsRHE/adsHSE/adsHSE.log	Hot Spot Analysis Log

Chip Power Model (CPM) generation and Chip-Package- System(CPS) analysis



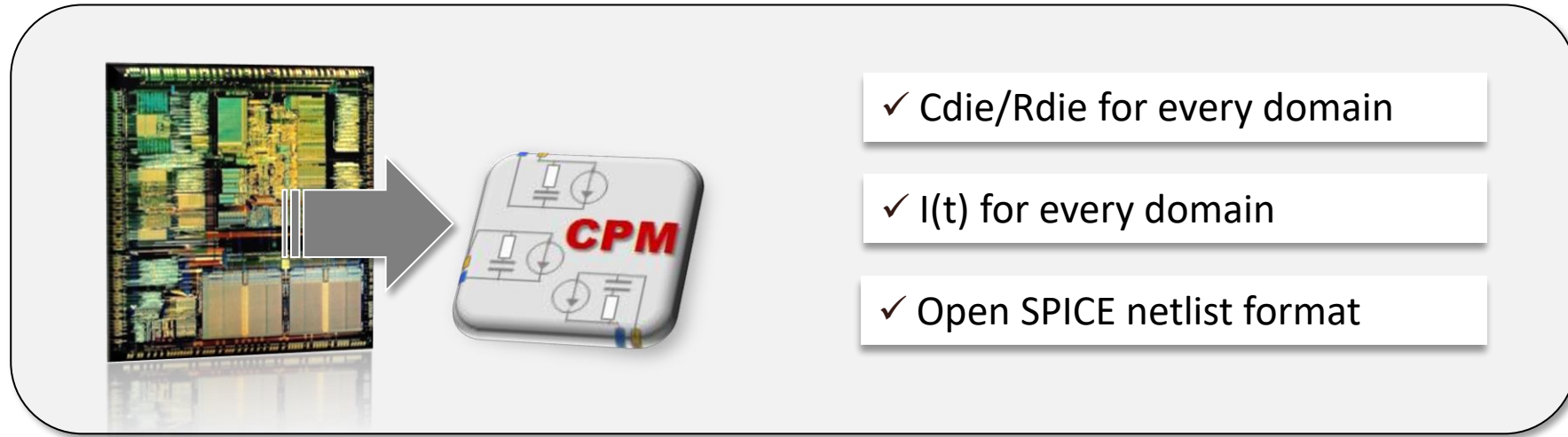
/ IC-Package-PCB Co-Design Challenges

System Design



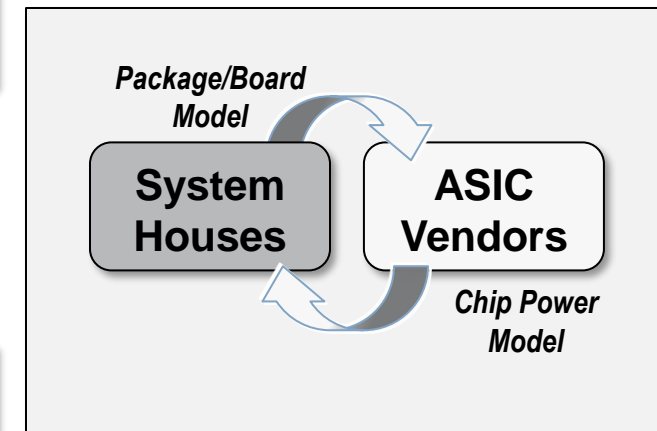
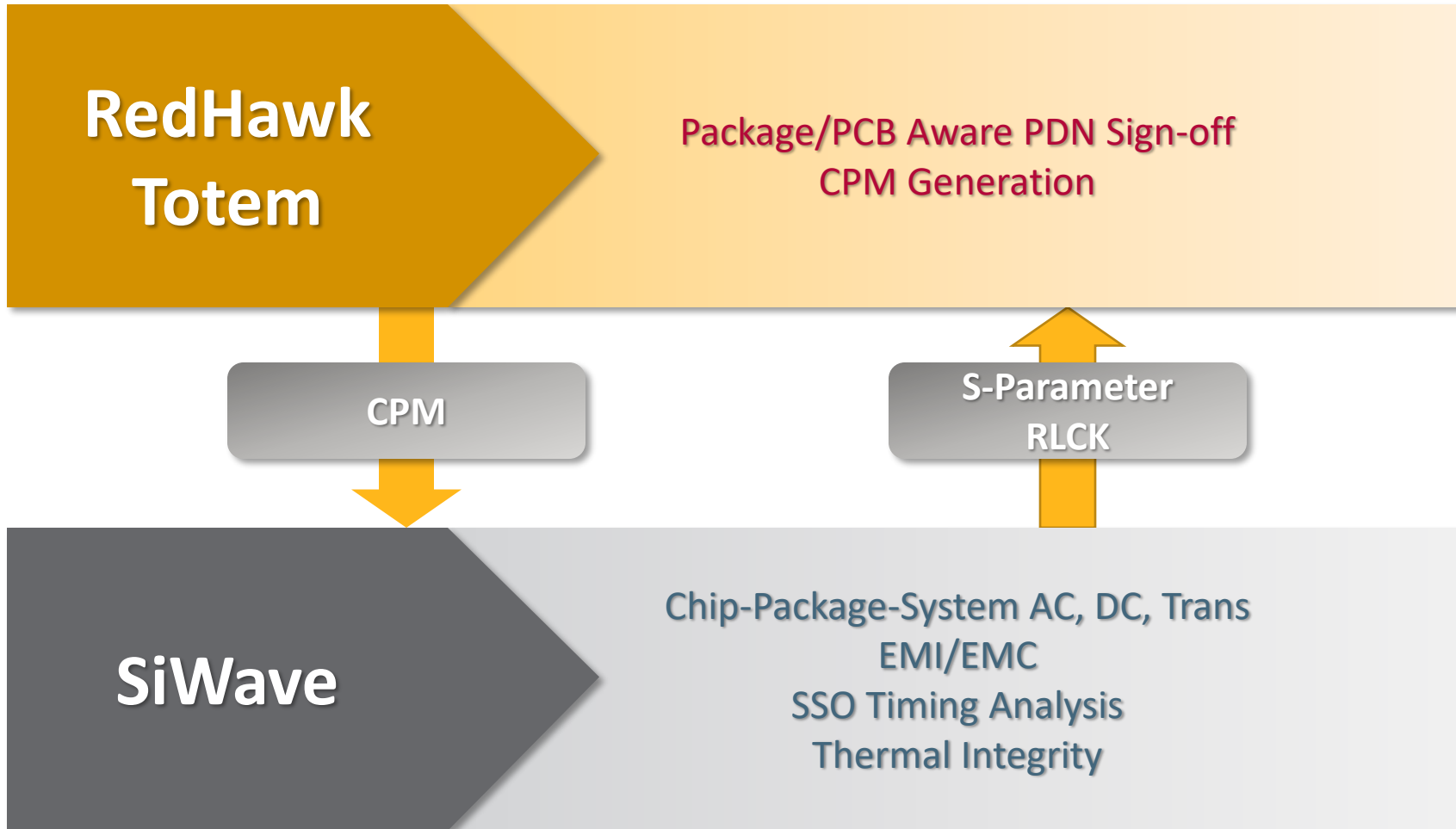
- Longer System Design Cycle
 - Chip is the source of noise
 - Lack of noise budgeting at board & package
 - Possible die-package resonance
 - Package re-spin
- Higher PKG / Board Cost
 - Over-design
 - Excessive decap

/ What's in a CPM?



- VCD based and Vectorless switching scenario
- Multi-domain, distributed model
- Full chip frequency domain simulation and model order reduction
- DC to multi-GHz validity
- Silicon correlated

/ Ansys's CPS Solutions



Chip Power Modeling Flow

```
# Import data
import gsr GENERIC.gsr
setup design

# Calculate power
perform pwrcalc

# Power grid extraction
perform extraction -power -ground -c

# Package, wirebond, pad setup
setup pad
setup package
setup wirebond

# CPM Creation
perform pwrmodel -nx 5 -ny 5 -o design.cpm
```

Exactly same inputs and steps used in dynamic simulation (Add keyword GENERATE_CPM 1 in GSR ; Package netlist is ignored)

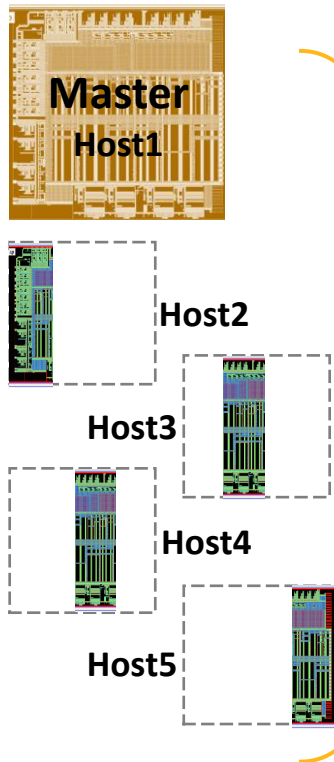
CPM Generation Command

Distributed Machine Processing (DMP) for large designs

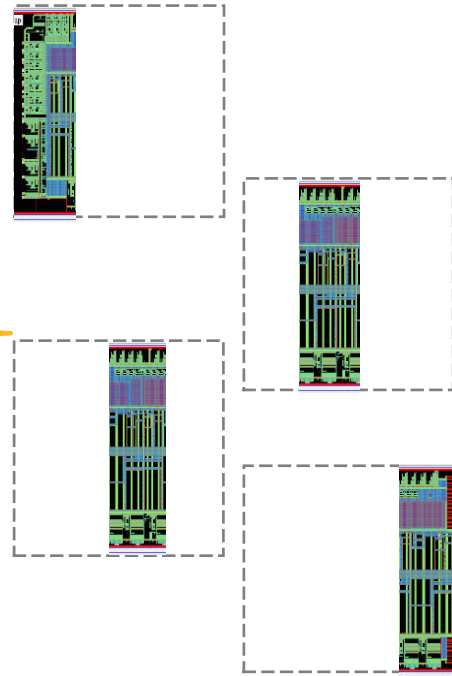


DMP Flow

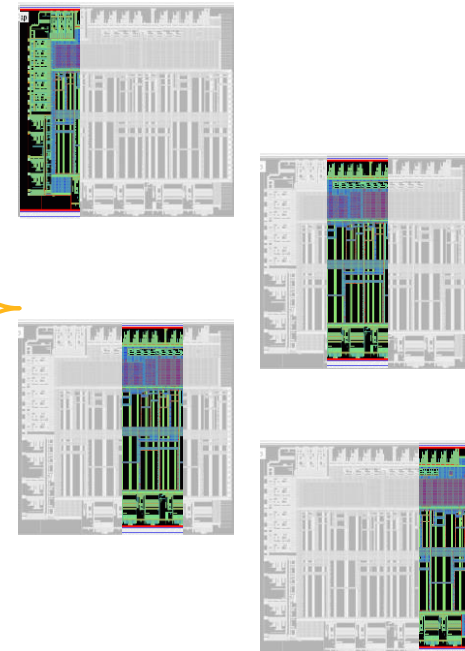
Step 1: Distributed Setup Design



Step 2: Distributed Power Calculation & Extraction

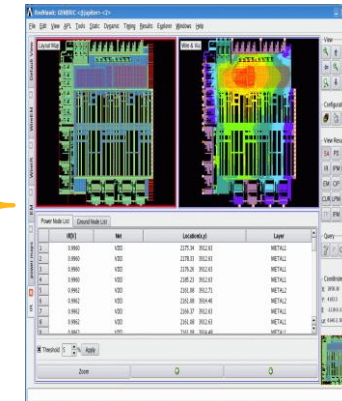


Step 3: Distributed Simulation



Step 4: Unified Result Analysis

Master Host1



/ Launching RedHawk DMP

- Command to launch DMP
 - `redhawk -lmwait -dmp <DMP_Config_file> -f <tcl_command_file>`
 - DMP config file is required to provide information like Number of partitions, Grid type, launch constraints etc.
 - Sample DMP Config file:

```
NUMBER_OF_JOBS 16
GRID_TYPE LSF/SSH/RTDA/SGE
QUEUE_NAME dmp_queue
ARGUMENTS_FOR_LARGE_JOBS " -q dmp_queue -R "rusage[mem=130000]"
```
- No other changes required in GSR/Tcl files

Q & A Session

- QA session will be for 15 mins
- For queries which are unanswered by end of this session , please email to dileesh.jostin@ansys.com or contact local Ansys AE

 **Ansys**

