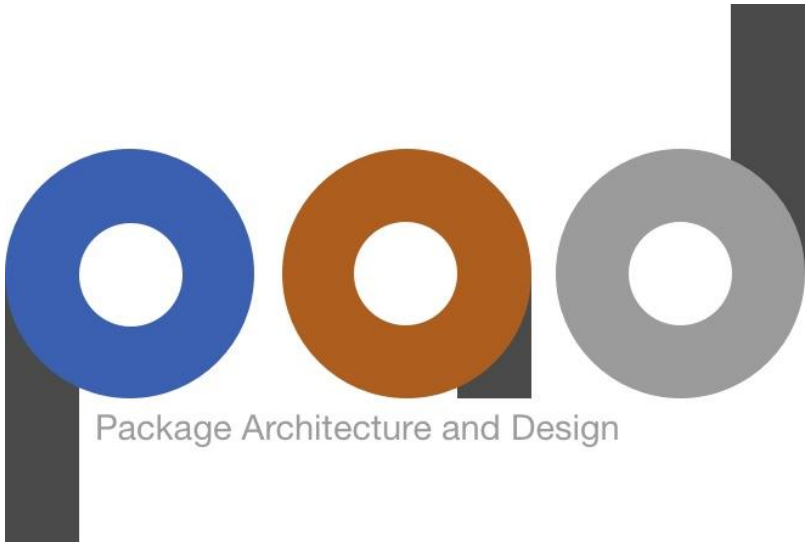
High-Level Module Design Guidelines and Design Trade-offs (Ver. 1)



- 9/10/2018
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Overview

- Objective
- Links to PMIC Reference Design Documents
- High-Level Component Placement Guidelines
- High-level Design Trade-offs
- Component Placement Examples
  - Based on Wailua and MakuaA Reference Designs
- Backup

Objective

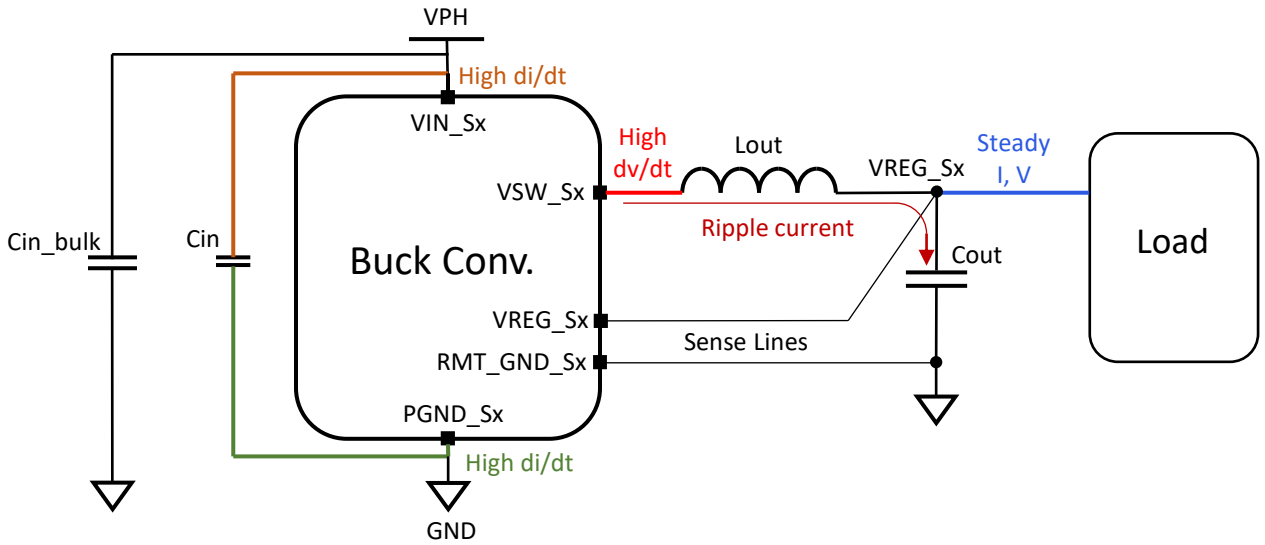
- **Provide high-level module design guidelines and design tradeoffs**
  - Includes a summary of component placement guidelines based on information provided by PMIC Systems Team
  - For comprehensive PMIC related information refer to documents on PMIC sharepoints - see the next slides for links
  - For detailed SDM information refer to BBSYS reference designs and electrical specs
  - For additional information on module design refer to Module_Design_BKM and other documents at Kern Module Sharepoint

Links to PMIC Reference Design Documents and Specs

- PMIC Systems Team provides Reference Design material for Qualcomm PMICs
- Each PMIC has a Sharepoint which contains: PCB layout requirements checklist, PCB layout example, reference design guide, etc.
- PMIC Reference Design Guide/Checklist should be followed wherever possible, especially for the “High Priority” requirements
- This should start with the component placement and layer assignments
- Wailua Reference Design documents can be found at: http://go/refPM855
- Included in Wailua Sharepoint are:
  - Checklist: “PMIC_PCB_Layout_Requirements_Wailua.xlsx”
  - Reference Design Layout Guide: “PM855_ReferenceDesign.pdf”
  - PA109_a_LDA design: “Archived_Design_Folder_PA109.zip”
- Similarly, MakuaL and MakuaA Reference Design documents can be found at:
  - http://go/refPM855L
  - http://go/refPM855A
- For VPH electrical targets refer to: http://go/vphspecs
- For links to TDOS, MDOS, Power Grid and more go to: http://go/wailua
- For PMIC Support Team FAQ and introductory technical/training material refer to: http://go/PST

High-level Component Placement Guidelines: Bucks, XO, Decoupling Caps

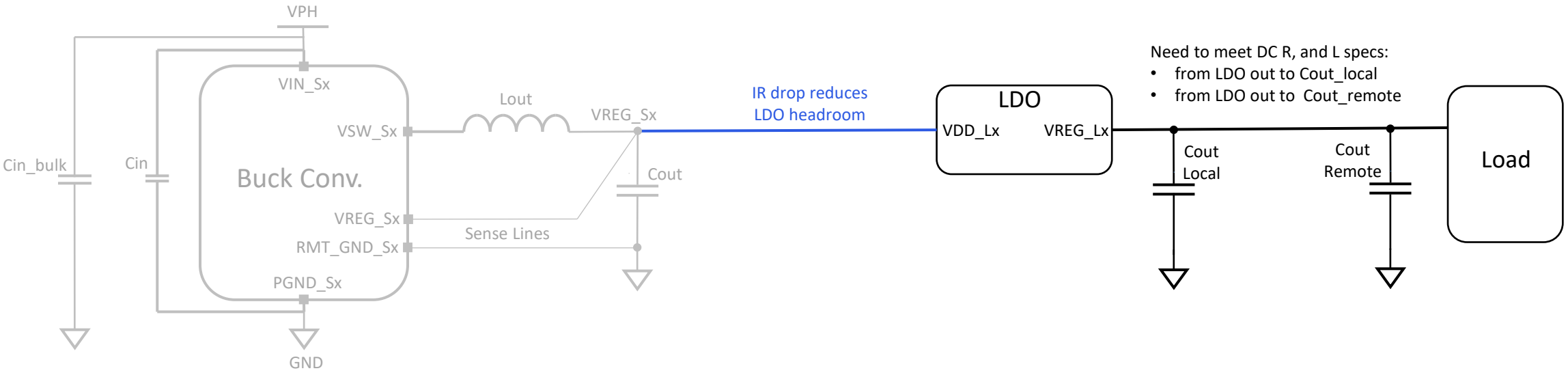
- Buck Converters
  - Inductor - place close to PMIC
    - VSW_S* nets are noisy (high dv/dt)
    - Keep sensitive signals away
    - Shield VSW* nets with GND planes above/below
  - Cin - place close to PMIC pins
    - Place Cout close to PMIC pins for boost converters
    - Place Cin and Cout close to PMIC pins for BoB
  - Cout
    - Ripple current is absorbed at Cout
    - Reduce DC Resistance from VSW_S* to load to improve efficiency
  - Sense lines
    - Noise sensitive (keep away from VSW_S*)
    - Connect to Cout (current PMIC guidelines)



- XO
  - Not too close to PMIC
  - Sensitive to temperature variations, noise and parasitic capacitance
  - Narrow trace connections for thermal isolation
  - Metal plane opening below XO for reduced thermal transfer
- Decoupling Caps
  - Decoupling caps should be placed close to load to minimize loop inductance
  - In many cases optimal placement of decoupling capacitors is directly below corresponding SDM power pins (or as close as possible)
  - 22uF 3T caps may serve two functions:
    - Buck output caps
    - SDM decoupling caps
- Main GND Plane
  - Low impedance main GND plane is critical for good electrical performance
  - Limit plane perforation due to via antipads
  - Do not route signals on main GND plane
- VPH Plane
  - Low impedance plane and good connection to board is required
  - Refer to module specific VPH electrical specs at: http://go/vphspecs

High-level Component Placement Guidelines: LDOs

- **LDO** (Low Drop-Out Voltage Regulator)
  - **Input**
    - **DC R** between buck output at sense point and LDO input is not compensated
    - Voltage drop reduces LDO headroom, which degrades performance (PSRR, load regulation)
    - NMOS and LV PMOS LDO input is connected to buck output as shown in simplified block diagram below. MV PMOS LDO input is connected to BOB or VPH – see MDOS document for details.
  - **Output**
    - **Cout Local** – place close to PMIC pin to meet DC R and L specs
    - **Cout Remote** – place close to load
      - Pseudo-capless LDOs have remote output caps only, which also serve as decoupling caps for the load
      - DC R and L specs from LDO output to remote cap need to be met (DC R spec was more challenging to meet in Kern module)
      - In some cases local and remote 1uF caps can be replaced with one local 2.2uF cap (adds cost)
    - Voltage drop from LDO out to load is not compensated



High-level Module Design Trade-offs

Design trade-offs due to single design variable change

- Dielectric Thickness ↑
  - Longer vias
    - Via inductance/resistance ↑
    - Cross-talk ↑
  - Plane inductance ↑
    - Increases with PWR-GND plane separation
  - Transmission line impedance ↑
    - Easier to meet typical Zdiff specs
- Metal Plane Thickness ↑
  - Plane DC resistance ↓
  - Transmission line impedance ↓
    - Harder to meet typical Zdiff specs

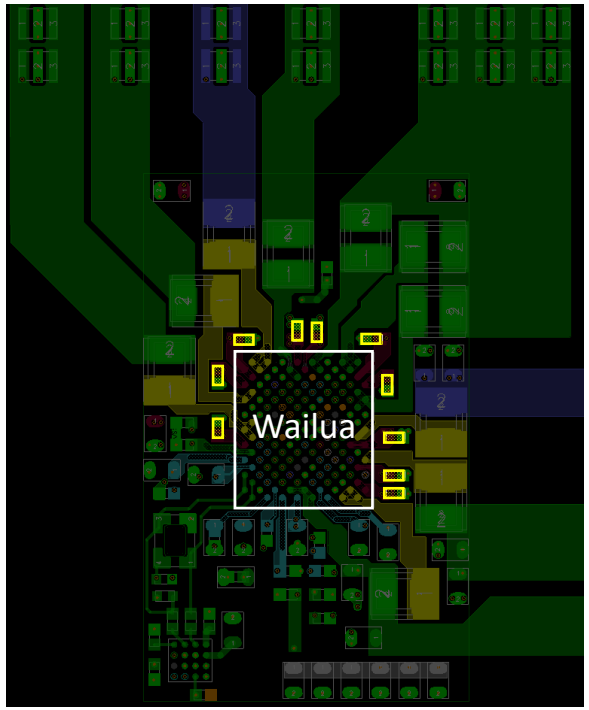
- Number of Layers ↑
  - DC Resistance ↓
    - More routing area, wider trace/shape connections
  - Longer top to bottom vias
    - Via inductance/resistance ↑
    - Cross-talk ↑
- Module Area ↓
  - Optimal placement of decoupling capacitors ↓
    - Limited area under SDM pins
  - DC Resistance ↑
    - Narrow trace/shape PWR net connections due to limited routing area
  - Cross-talk ↑
    - Reduced spacing between victim nets and aggressors (components, vias and traces)

- Input:
  - ↑ / ↓ - single design variable increased / decreased
- Result:
  - ↑ / ↓ - parameter increased / decreased, performance improved
  - ↑ / ↓ - parameter increased / decreased, performance degraded

Buck Components: Cin, Lout,Cout

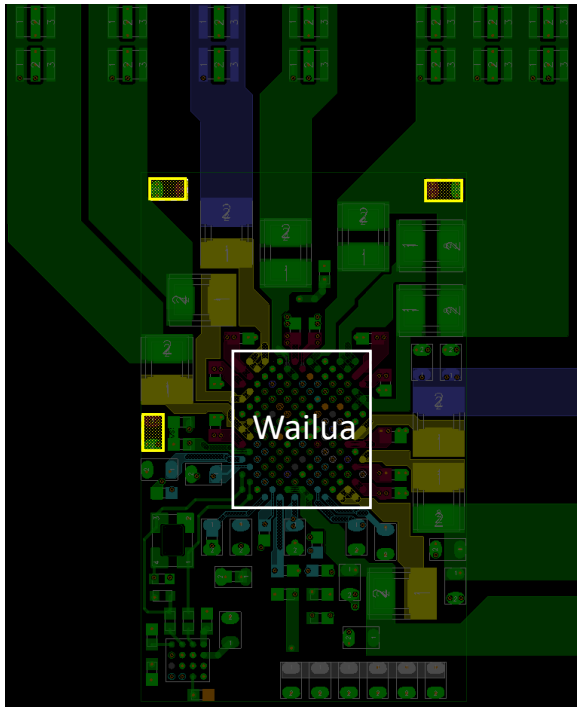
(http://go/refPM855)

Input Caps



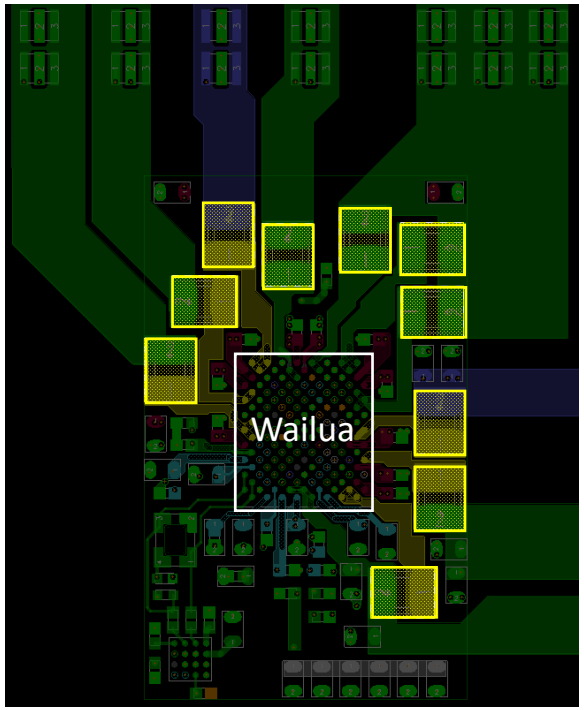
- 1uF, 0201
- One per buck with dedicated vias:
  - reduce coupling between bucks
  - reduce coupling to sensitive nets
- Place Cin close to PMIC pins to minimize loop inductance and reduce voltage spikes due to high di/dt at input pins

Input Caps - Bulk



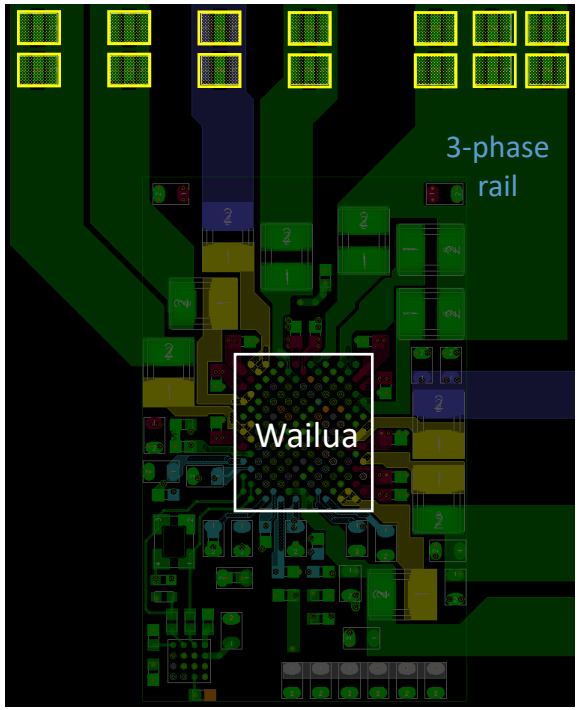
- 10uF, 0402
- ~3 per PMIC
- Can be further away from PMIC pins

Output Inductors



- **VSW_S*** nets between PMIC pins and inductors are NOISY (high dv/dt)!
  - Place Lout close to PMIC
  - Keep sensitive signals away
- 3 overlapping inductor footprints used in Wailua ref design (2016 highlighted)
- Kern module has:
  - 0.47uH, 2012, 0.8mm
  - 0.47uH, 1608, 0.8mm

Output Caps

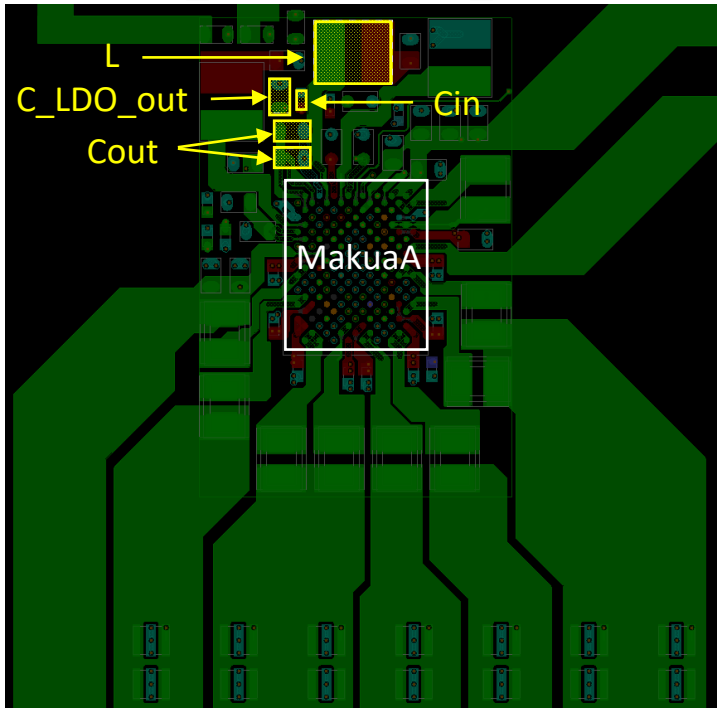


- 22uF, 3T
- 2 caps per phase
- Also serves as decoupling cap for SDM in many cases
- VREG_S* nets between inductor and output cap
- Output cap absorbs ripple current
- Reduce DC R between PMIC output and load to improve efficiency

OLED, BoB

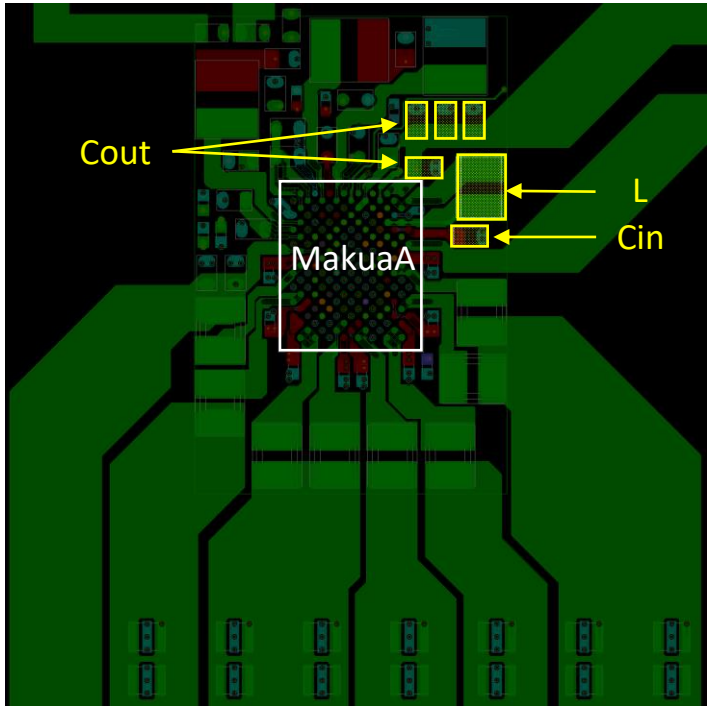
(http://go/refPM855A)

VSW_OLEDB, VREG_OLEDB



- **Cout** (10uF, 0402), **close to PMIC pins VREG_OLEDB**
  - Second Cout can be further from PMIC
- **PGND_OLEDB** is NOISY – isolate from other GND domains
- **Cin** (1uF, 0201), close to PMIC pins (lower priority)
- **C_LDO_out** (10uF, 0402), close to PMIC pins LDO_OUT_OLEDB
- **VSW_OLEDB** is NOISY – high dv/dt
  - Place inductor (0.47uH, 2520, 0.8mm) close to PMIC
  - Keep sensitive signals away

VBOB

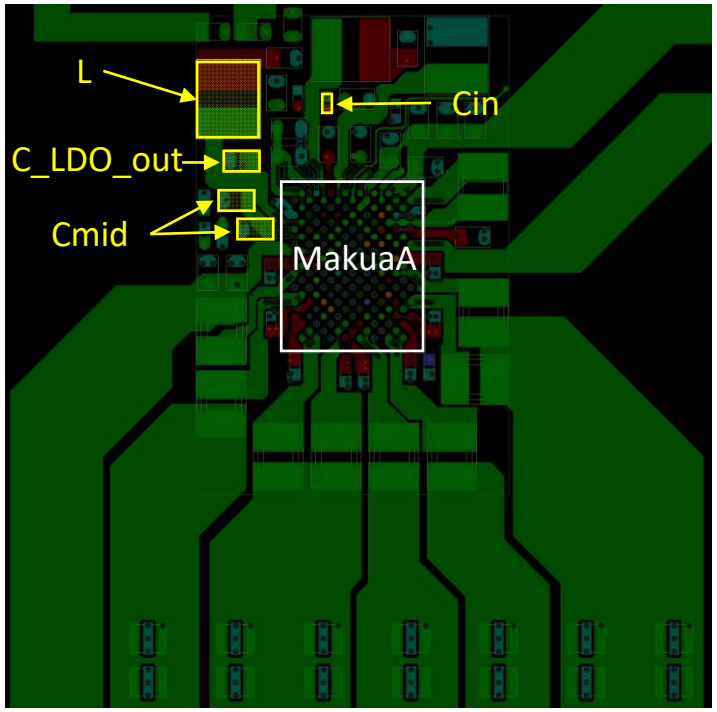


- **Both Cin and Cout close to PMIC pins**
  - One Cout close to PMIC, others can be further from PMIC
- **PGND_BOB** is NOISY – isolate from other GND domains
- **VSW_BOB** is NOISY – high dv/dt
  - Place inductor (L = 0.47uH, 2012, 0.8mm in Kern) close to PMIC
  - Keep sensitive signals away

ELVDD, ELVSS

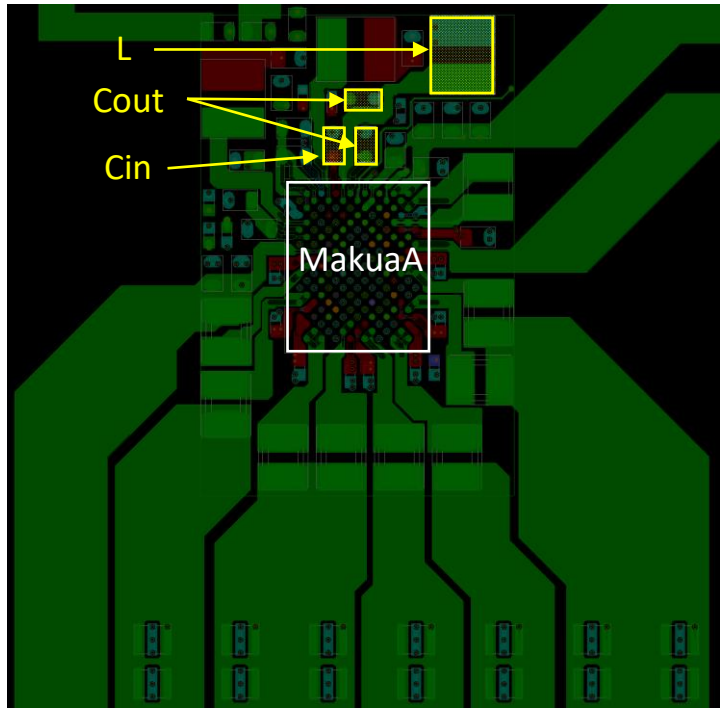
(http://go/refPM855A)

ELVDD



- **Cmid close to PMIC pins (MID_ELVDD, LDO_IN_ELVDD)** - boost conv output cap
  - Second Cmid can be further from PMIC
- **PGND_OLEDB** is NOISY – isolate from other GND domains
- **C_LDO_out** close to PMIC pins (VREG_ELVDD) – LDO output cap
- **Cin** (1uF, 0201), close to PMIC pins (lower priority)
- **VSW_ELVDD** is NOISY – high dv/dt
  - Place inductor (4.7uH, 2520, 0.8mm) close to PMIC
  - Keep sensitive signals away

ELVSS

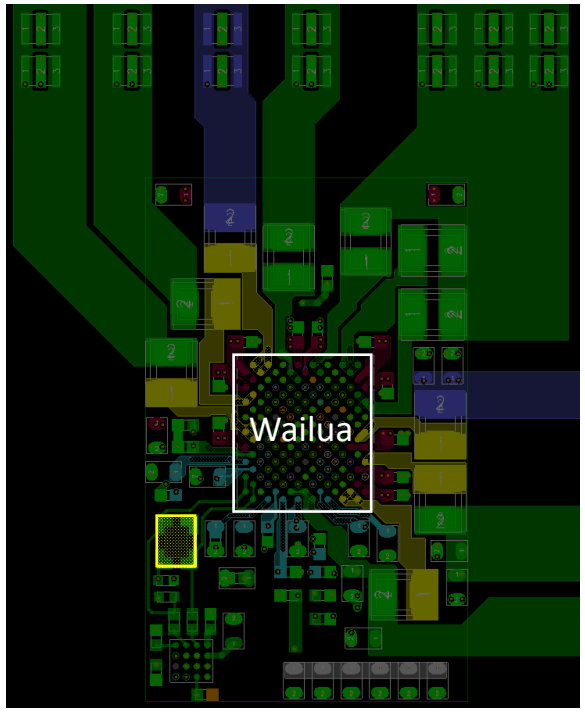


- **Both Cin and Cout close to PMIC pins**
  - Second Cout can be further from PMIC
- **VSW_ELVSS** is NOISY – high dv/dt
  - Place inductor (4.7uH, 2520, 0.8mm) close to PMIC
  - Keep sensitive signals away

XO, Clock Buffer LDOs, REF_BYP, AVDD_BYP

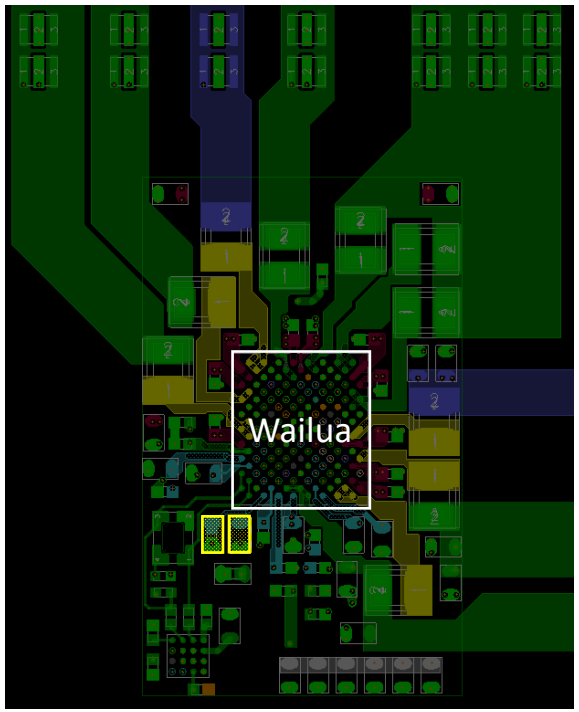
(http://go/refPM855)

XO



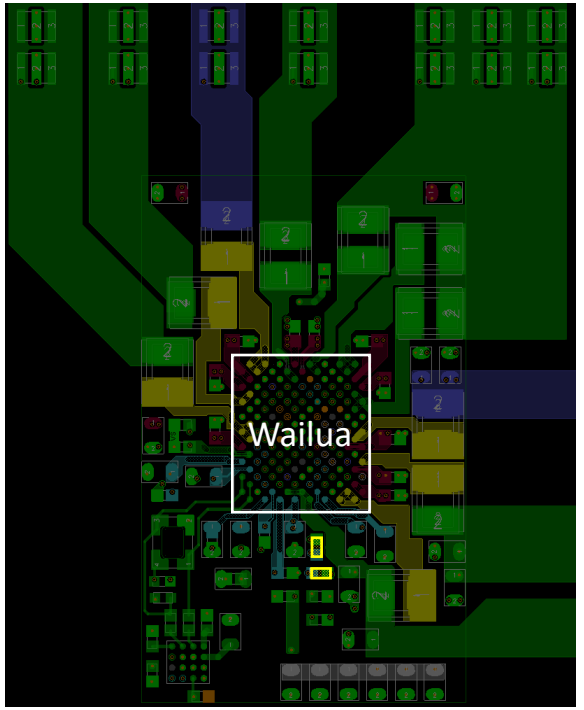
- XO not too close to PMIC
- **Sensitive to temperature variations, noise and parasitic capacitance**
  - Narrow trace connections for thermal isolation
  - Metal plane opening below XO for reduced thermal transfer
  - Dedicated vias to main GND
  - Reduce parasitic capacitance to GND and signals

VREG_XO, VREG_RF



- Short connections to PMIC pins
- Dedicated vias
- Noise sensitive

REF_BYP, AVDD_BYP

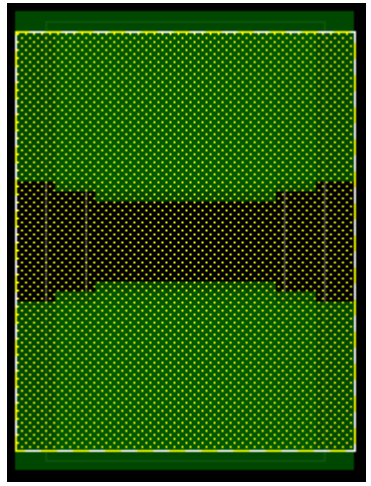


- REF_BYP, Cap 0.1uF, 0201
  - Reference voltage for PMIC
  - Noise sensitive
- AVDD_BYP, Cap 1uF, 0201
  - Voltage supply to PMIC analog circuits
  - Noise sensitive

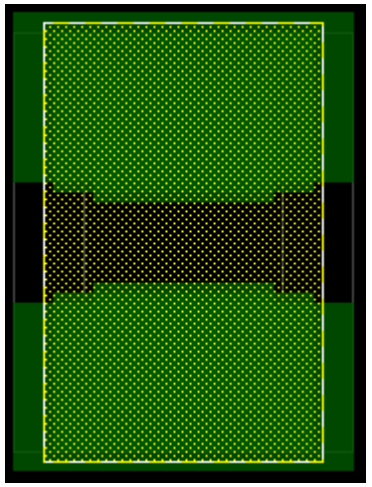
Backup

Buck Output Inductors

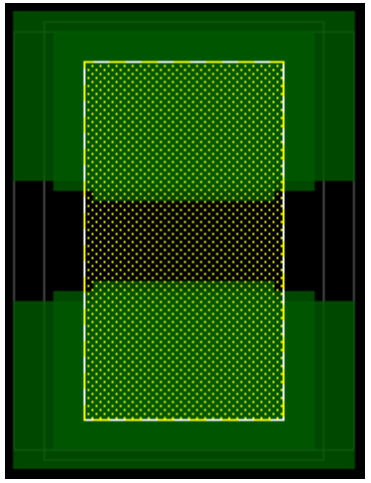
Buck Output Inductors (0.47uH) in PMIC Reference Designs



- ❑ **2016, 0.65mm**
- ❑ 110-86880-0471



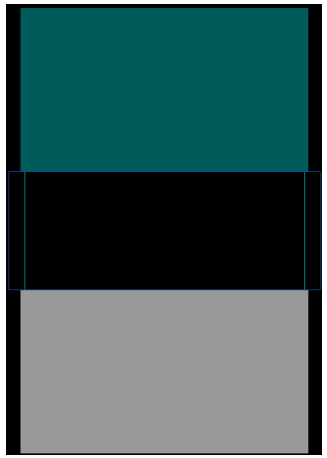
- ❑ **2012, 0.8mm**
- ❑ 110-86876-0471



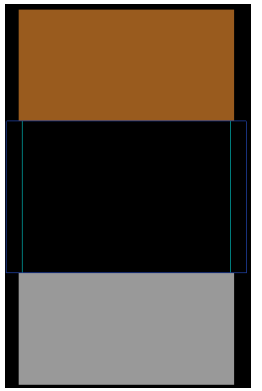
- ❑ **1608, 0.8mm**
- ❑ 110-83371-0471

- PMIC Reference Designs provide options for three types of buck output inductors with overlapping footprints

Buck Output Inductors (0.47uH) in Kern Module



- ❑ **2012, 0.8mm**
- ❑ 110-91600-0471

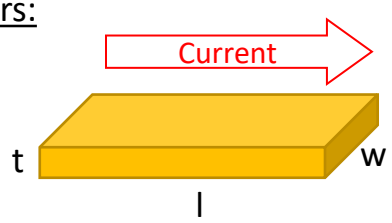


- ❑ **1608, 0.8mm**
- ❑ 110-86816-0471

- Kern module has two types of buck output inductors:
  - 2012 high-current rails
  - 1608 lower current rails

Metal Plane Sheet Resistance

Metal plane parameters:
ρ – resistivity
t – thickness
w – width
l – length



$$R = \rho \frac{l}{S} = \rho \frac{l}{wt} = \frac{\rho}{t} \frac{l}{w}$$

Sheet Resistance: $R_s = \frac{\rho}{t}$

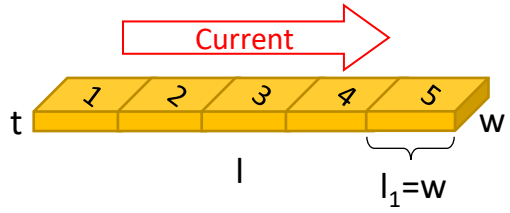
Number of Squares: $N_{sq} = \frac{l}{w}$

$$R = R_s \times N_{sq}$$

Easy way to estimate DCR

Example:
ρ_copper = 1.72E-8 [Ωm], t=15µm => R_s=1.2[mΩ/sq]

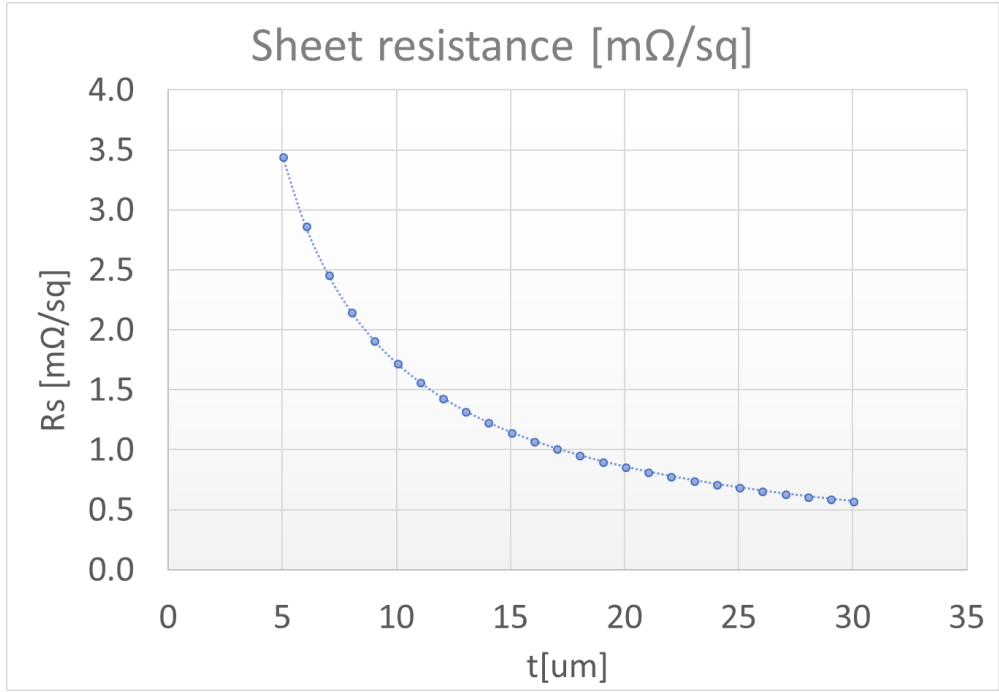
If N_{sq}=5 then:
R = 5 sq * 1.2[mΩ/sq] = 6[mΩ]



Temperature dependence (not included):

R_0 – resistance at T_0
α – temp coefficient of resistance

$$R(T) = R_0[1 + \alpha(T - T_0)]$$



Assumption: ρ = 1.72E-8 [Ωm] – copper

Metal Thickness [µm]	Sheet Resistance [mΩ/sq]	Delta relative to t=15um [%]
5	3.4	200%
10	1.7	50%
15	**1.2**	
20	0.9	-25%
25	0.7	-40%
30	0.6	-50%

Kern nominal parameters shown in blue.