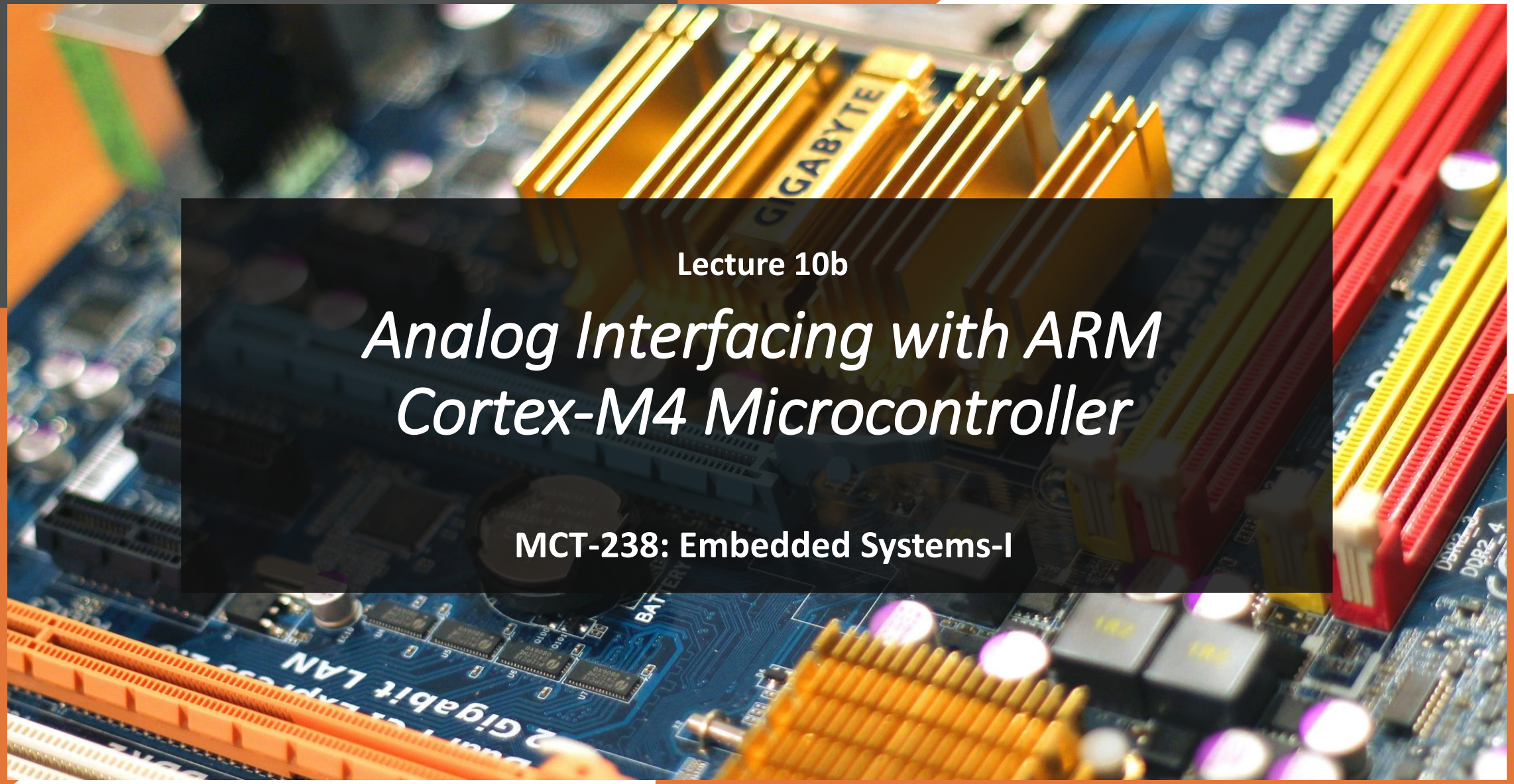


Lecture 10b

Analog Interfacing with ARM Cortex-M4 Microcontroller

MCT-238: Embedded Systems-I

Analog Interfacing

ARM Cortex-M4 Microcontroller

- ADC on TM4C123G Microcontroller
- GPIO Pins Mapping for ADC
- ADC Block Diagram
- Configuration Steps for ADC Module
  - ADC Clock Gating Control Configuration
  - GPIO Configuration as ADC input
  - ADC Module Configuration
  - ADC Sample Sequencer Configuration
  - ADC Interrupt Configuration

ADC Details

TM4C123 Microcontroller

- TM4C123 Microcontroller contains 2 successive approximation-based ADCs
- Each ADC can operate independently with following features:
  - Maximum sampling rate of 1 Msps
  - 12-bit sample resolution
  - 12 external AI channels (ANI_0 to ANI_11)
  - 1 internal temperature sensor
  - Multiple triggering sources for starting process
  - Single ended or differential analog inputs
  - Hardware sample averaging capability up 64 samples
- Four programmable sample sequencers (SS0, SS1, SS2, SS3)
  - enable flexible sampling of multiple AI
  - reduces microcontroller overhead to handle each conversion

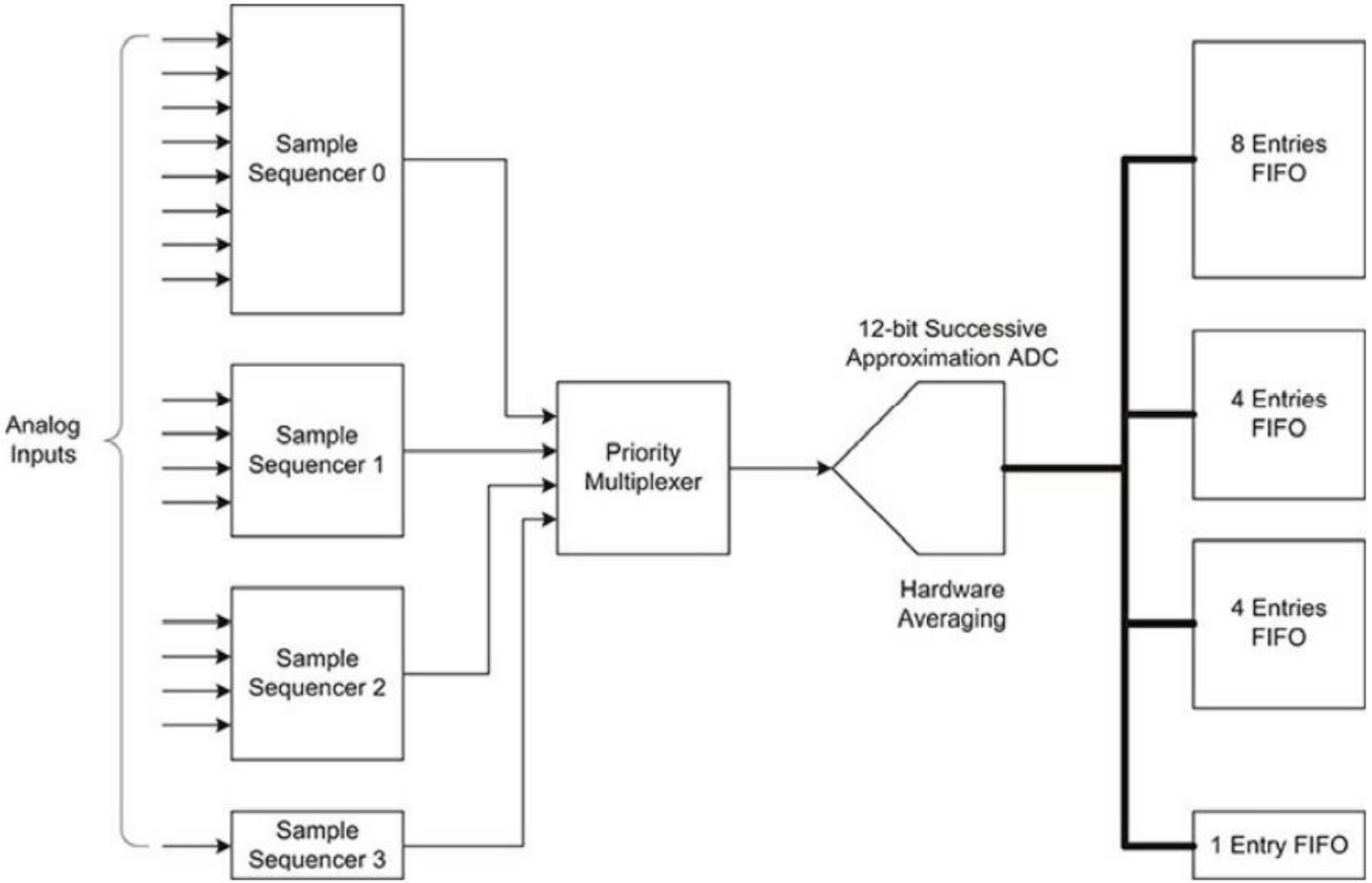
GPIO Pins Mapping for ADC

TM4C123 Microcontroller

#	Analog Input Channel	GPIO Pin Assignment
1	ANI_0	Port E pin 3 (PE3)
2	ANI_1	Port E pin 2 (PE2)
3	ANI_2	Port E pin 1 (PE1)
4	ANI_3	Port E pin 0 (PE0)
5	ANI_4	Port D pin 3 (PD3)
6	ANI_5	Port D pin 2 (PD2)
7	ANI_6	Port D pin 1 (PD1)
8	ANI_7	Port D pin 0 (PD0)
9	ANI_8	Port E pin 5 (PE5)
10	ANI_9	Port E pin 4 (PE4)
11	ANI_10	Port B pin 4 (PB4)
12	ANI_11	Port B pin 5 (PB5)

ADC Block Diagram

TM4C123 Microcontroller



Configuration Steps for ADC Module

TM4C123 Microcontroller

Five steps process

- Step 1: ADC Clock Gating Control Configuration
- Step 2: GPIO Configuration as ADC input
- Step 3: ADC Module Configuration
- Step 4: ADC Sample Sequencer Configuration
- Step 5: ADC Interrupt Configuration

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- *Run Mode Clock Gating Control Register* **RCGC_ADC_R** (*Address Value = 0x400FE638*) is used to enable clock to ADC modules
- Bit 0 of **RCGC_ADC_R** corresponds to **ADC0** module, while bit 1 to corresponds **ADC1** module
- Writing 1 to the bit enables and provides clock to corresponding ADC module
- After clock enabling, 3-clock cycles delay required before accessing the ADC register
- e.g. writing 0x02 to **RCGC_ADC_R** will enable clock on ADC1 module

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- 12 analog inputs (ANI_0 to ANI_11) to TM4C123 Microcontroller are multiplexed to GPIO pins
- To enable analog functionality on a GPIO Pin
  - Enable clock on GPIO using **RCGC_GPIO_R** (*Address Value = 0x400FE608*)
  - Disable digital function by clearing corresponding bit in **GPIO_DEN_R** (*Offset Value = 0x51C*)
  - Set corresponding bit in *GPIO Analog Mode Select Register* **GPIO_AMSEL_R** (*Offset Value = 0x528*) to enable analog (by disabling analog isolation circuit)
- e.g. for configuring PortB (*Base Address = 0x40005000*) pin 4 (**ANI_10**) as an ADC analog input we will clear bit 4 in **GPIO_DEN_R** and set it in **GPIO_AMSEL_R**

Configuration Steps for ADC Module

TM4C123 Microcontroller

GPIO Port Configurations

#	Configuration	Register	Offset	Register Address	Configuration Setting
1	GPIO Clock Gating Control	**RCGC_GPIO_R**	-	0x400FE608	Set bit to enable clock on GPIO Port
2	Pad Control Config.	**GPIO_DEN_R**	0x51C	-	Clear bit to disable digital function of GPIO Pin
3	Analog Mode Select	**GPIO_AMSEL_R**	0x528	-	Set the bit to enable analog mode

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

The key configuration steps for an ADC Module are:

- Clock Source Config.
- Sampling Rate Config.
- Sequencer Triggering Source Config.
- Sequencer Priority Config.
- Hardware Averaging Config.
- Control Config.

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ **Clock Source Config.**
- ❑ Sampling Rate Config.
- ❑ Sequencer Triggering Source Config.
- ❑ Sequencer Priority Config.
- ❑ Hardware Averaging Config.
- ❑ ADC Control Config.

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- 4 LSB of Clock *Source Configuration Register* **ADC_CLK_CONFIG_R** (*Offset Value = 0xFC8*) are used for ADC clock source selection.
- For a value of 0, the system clock is used for sampling
- For a value of 1, precision internal oscillator (***PIOSC***) running at 16 MHz as clock source and the ADC module can continue to operate in Deep-Sleep Mode

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ **Sampling Rate Config.**
- ❑ Sequencer Triggering Source Config.
- ❑ Sequencer Priority Config.
- ❑ Hardware Averaging Config.
- ❑ ADC Control Config.

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- ADC sampling rate is configured using *ADC Peripheral Configuration Register* ***ADC_PERI_CONFIG_R*** (*Offset Value = 0xFC4*)
- Only these values can be configured by using this register
  - **0x01**: configures **125 ksps** sample rate
  - **0x03**: configures **250 ksps** sample rate
  - **0x05**: configures **500 ksps** sample rate
  - **0x07**: configures **1000 ksps** (1 Msps) sample rate (default value)
- When attempt, to configure ADC with sample rate not supported by the device, is made then ADC either continue with default or more recently used sample rate

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ **Sequencer Triggering Source Config.**
- ❑ Sequencer Priority Config.
- ❑ Hardware Averaging Config.
- ❑ ADC Control Config.

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- Each ADC sequencer can be triggered by processor, GPIO, timer, PWM or comparator
- *ADC Event Multiplexer Select Register* **ADC_E_MUX_R** (*Offset Value = 0x014*) can be configured for selection
- Using different triggering sources at different rates for Sample Sequencer allow to sample analog inputs at different sampling rates
- Each triggering source has its own register for triggering the sample sequencer
  - **ADC_PROC_INIT_SS_R** (*Offset Value = 0x028*): when using Processor as triggering source
  - **ADC_PWM_TRIGGER_R** (*Offset Value = 0x01C*): used when triggering source is PWM

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ **Sequencer Triggering Source Config.**
- ❑ Sequencer Priority Config.
- ❑ Hardware Averaging Config.
- ❑ ADC Control Config.

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

Bit field	Description
SS0 Trigger Mux, SS1 Trigger Mux, SS2 Trigger Mux, SS3 Trigger Mux	Each of these bit fields selects the triggering source for the corresponding sample sequencer. The configurable values for these bit fields and the resulting selections for ADC triggering are listed below. • Configuring a value of 0 makes the processor as ADC triggering source. • Configuring a value of 1 or 2 makes the analog comparator 0 or 1 as the trigger source using analog comparator control configuration. • Configuring a value of 4 makes the GPIO pin as the trigger source. • Configuring a value of 5 makes the timer as the trigger source. To use timer as trigger source timer output trigger enable bit must be set. • Configuring a value of 6, 7, 8 or 9 makes the PWM generator 0, 1, 2 or 3 as trigger source. • Configuring a value of 0xF enables continuous sampling mode, which does not require triggering.

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ **Sequencer Priority Config.**
- ❑ Hardware Averaging Config.
- ❑ ADC Control Config.

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- Order of sampling among the active sequencers is decided based on assigned priority
- Each active sequencers should be assigned a unique priority using ADC *Sample Sequencer Priority Register* **ADC_PRI_SS_R** (*Offset Value = 0x020*)
- Out of reset, Sequencer 0 has the highest priority, and Sequencer 3 has the lowest priority.
- When reconfiguring sequence priorities, each sequence must have a unique priority for the ADC to operate properly

Bit field	Description
SS0 Priority, SS1 Priority, SS2 Priority, SS3 Priority	All the sequencer priority bit fields follow a common definition. Configuring a value of 0 makes the corresponding sequencer highest priority, while a value of 3 corresponds to lowest priority.

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ **Hardware Averaging Config.**
- ❑ ADC Control Config.

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- Hardware averaging is used for improved resolution
- ADC performs over sampling to average multiple samples
- *ADC Sample Averaging Control Register* **ADC_SAC_R** (*Offset Value = 0x030*) is used to configure magnitude of hardware averaging
- Only bit 0-2 of this register can be written as following
  - **0x0** : No hardware oversampling
  - **0x1** : 2x hardware oversampling
  - **0x2** : 4x hardware oversampling
  - **0x3** : 8x hardware oversampling
  - **0x4** : 16x hardware oversampling
  - **0x5** : 32x hardware oversampling
  - **0x6** : 64x hardware oversampling

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ *Hardware Averaging Config.*
- ❑ **ADC Control Config.**

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- Choice of ADC voltage reference source using *ADC Control Register* **ADC_CONTROL_R** (*Offset Value = 0x038*)
  - Set bit 0 to enable voltage at analog supply pins ***VddA*** & ***GndA*** as reference voltage
  - Values set in this register apply to both ADC modules
- Enable or disable each sample sequencer individually using ADC Active Sample Sequencer Register **ADC_ACTIVE_SS_R** (*Offset Value = 0x000*)
  - Bit 0 to 3 corresponds to SS0 to SS3
  - Setting a bit to 1 enables the corresponding sample sequencer
  - Bit 16 (read only) of the register reads 1 if the ADC is busy

Configuration Steps for ADC Module

TM4C123 Microcontroller

ADC Module Configurations

- ADC0 base address: 0x40038000 & ADC1 base address: 0x40039000
- Step 1: Enable ADC Clock using **RCGC_ADC_R** (address value 0x400FE638)
  - writing 1 (to bit 0 for ADC0 and bit 1 for ADC1)

#	Configuration	Register	Offset	Configuration Setting
2	ADC Peripheral Config.	**ADC_PERI_CONFIG_R**	0xFC4	Set ADC sample rate by writing predefined value
3	ADC Event Mux. Select	**ADC_E_MUX_R**	0x014	Select ADC trigger by writing predefined value
4	ADC Sample Sequencer Priority	**ADC_PRI_SS_R**	0x020	Write 0 for highest and 3 for lowest priority
5	ADC Sample Averaging Control	**ADC_SAC_R**	0x030	Select hardware averaging level by writing predefined value
6	ADC Control Register	**ADC_CONTROL_R**	0x038	Select the voltage reference for ADC
7	ADC Active SS Register	**ADC_ACTIVE_SS_R**	0x000	Enable individual SS by setting corresponding bit
8	ADC Triggering Source Register	-	-	Register selected based on **Step 3**

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ *Hardware Averaging Config.*
- ❑ *ADC Control Config.*

Step 4: ADC Sample Sequencer Config.

Step 5: ADC Interrupt Configuration

- Each Sample Sequencer (SS) can be configured independently using its associated registers
  - Selection of an analog input channel is completely independent and can be performed separately
  - Same analog input can be configured for multiple channels of the same SS
  - Sample sequencer analog input can be configured as single ended or differential type
  - Not necessary to use all the channels of a sample sequencer
- Always disable the appropriate sample sequencer before modifying the ADC configurations

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

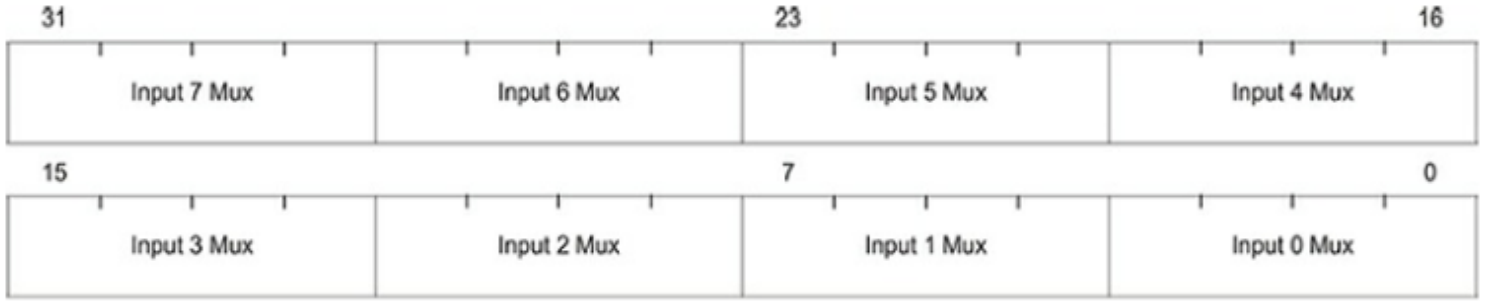
- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ *Hardware Averaging Config.*
- ❑ *ADC Control Config.*

Step 4: ADC Sample Sequencer Config.

- ❑ **Input Multiplexing Config.**
- ❑ Sequencer Control Config.
- ❑ Sample Sequencer Result

Step 5: ADC Interrupt Configuration

- Analog inputs to ADC sequencer can be configured using *ADC Sample Sequencer Input Multiplexer Register* (**ADC_SSxIN_MUX_R**, where x represents the sequencer number and can be 0 to 3)
  - **ADC_SS0IN_MUX_R** (*Offset Value = 0x040*) 8 channels
  - **ADC_SS1IN_MUX_R** (*Offset Value = 0x060*) 4 channels
  - **ADC_SS2IN_MUX_R** (*Offset Value = 0x080*) 4 channels
  - **ADC_SS3IN_MUX_R** (*Offset Value = 0x0A0*) 1 channel



Bit field	Description
Input7 Mux - Input0 Mux	Each of these bit fields is used to configure an analog input channel for the corresponding sequencer. Configuring a value of 2 to bit field Input0 Mux, assigns analog input channel 2 as the first input to the sequencer 0. The possible values that can be configured are 0 to 11, which correspond to the 12 analog input channels.

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ *Hardware Averaging Config.*
- ❑ *ADC Control Config.*

Step 4: ADC Sample Sequencer Config.

- ❑ *Input Multiplexing Config.*
- ❑ **Sequencer Control Config.**
- ❑ Sample Sequencer Result

Step 5: ADC Interrupt Configuration

- *ADC Sample Sequencer Control Register* (**ADC_SSx_CONTROL_R**, where **x** represents the sequencer number and can be 0 to 3) contains the configuration information for a sample executed with Sample Sequencer
  - **ADC_SS0_CONTROL_R** (*Offset Value = 0x044*) 8 channels
  - **ADC_SS1_CONTROL_R** (*Offset Value = 0x064*) 4 channels
  - **ADC_SS2_CONTROL_R** (*Offset Value = 0x084*) 4 channels
  - **ADC_SS3_CONTROL_R** (*Offset Value = 0x0A4*) 1 channel
- For example, SS3 can be configured for the following settings
  - **Bit 0 (D0): Sample Differential Input Select**
    - Set to consider analog input as differential input
  - **Bit 1 (END0): End of Sequence**
    - 1 means end of sequence and 0 means sampling and conversion continues
  - **Bit 2 (IE0): Sample Interrupt Enable**
    - When set, interrupt signal is asserted at the end of sample's conversion
  - **Bit 3 (TS0): 1st Sample Temperature Sensor Select**
    - If set, read the internal temperature sensor during first sample of SS
- When configuring a sample sequencer, END bit must be set.

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ *Hardware Averaging Config.*
- ❑ *ADC Control Config.*

Step 4: ADC Sample Sequencer Config.

- ❑ *Input Multiplexing Config.*
- ❑ *Sequencer Control Config.*
- ❑ **Sample Sequencer Result**

Step 5: ADC Interrupt Configuration

- *ADC Sample Sequencer Result FIFO* (**ADC_SSx_FIFO_DATA_R**, where **x** represents the sequencer number and can be 0 to 3) contains the conversion results for Sample Sequencer
  - **ADC_SS0_FIFO_DATA_R** (*Offset Value = 0x048*) 8 channels
  - **ADC_SS1_ FIFO_DATA _R** (*Offset Value = 0x068*) 4 channels
  - **ADC_SS2_ FIFO_DATA _R** (*Offset Value = 0x088*) 4 channels
  - **ADC_SS3_ FIFO_DATA _R** (*Offset Value = 0x0A8*) 1 channel
- This register contains 12-bit conversion result of sample
- Reads of this register return conversion result data in the order sample 0, sample 1, and so on, until the FIFO is empty

Configuration Steps for ADC Module

TM4C123 Microcontroller

Sample Sequencer Configurations

- ADC0 base address: 0x40038000
- ADC1 base address: 0x40039000

Register label	Offset	Reset value	Brief description
ADC_SS0_IN_MUX_R	0x040	0x00000000	SS0 analog input selection register.
ADC_SS0_CONTROL_R	0x044	0x00000000	SS0 control register.
ADC_SS0_FIFO_DATA_R	0x048	-	SS0 FIFO data register.
ADC_SS0_FIFO_STATUS_R	0x04C	0x00000100	SS0 FIFO status register.
ADC_SS1_IN_MUX_R	0x060	0x00000000	SS1 analog input selection register.
ADC_SS1_CONTROL_R	0x064	0x00000000	SS1 control register.
ADC_SS1_FIFO_DATA_R	0x068	-	SS1 FIFO data register.
ADC_SS1_FIFO_STATUS_R	0x06C	0x00000100	SS1 FIFO status register.
ADC_SS2_IN_MUX_R	0x080	0x00000000	SS2 analog input selection register.
ADC_SS2_CONTROL_R	0x084	0x00000000	SS2 control register.
ADC_SS2_FIFO_DATA_R	0x088	-	SS2 FIFO data register.
ADC_SS2_FIFO_STATUS_R	0x08C	0x00000100	SS2 FIFO status register.
ADC_SS3_IN_MUX_R	0x0A0	0x00000000	SS3 analog input selection register.
ADC_SS3_CONTROL_R	0x0A4	0x00000000	SS3 control register.
ADC_SS3_FIFO_DATA_R	0x0A8	-	SS3 FIFO data register.
ADC_SS3_FIFO_STATUS_R	0x0AC	0x00000100	SS3 FIFO status register.

Configuration Steps for ADC Module

TM4C123 Microcontroller

Step 1: ADC Clock Gating Control Config.

Step 2: GPIO Config. as ADC input

Step 3: ADC Module Configuration

- ❑ *Clock Source Config.*
- ❑ *Sampling Rate Config.*
- ❑ *Sequencer Triggering Source Config.*
- ❑ *Sequencer Priority Config.*
- ❑ *Hardware Averaging Config.*
- ❑ *ADC Control Config.*

Step 4: ADC Sample Sequencer Config.

- ❑ *Input Multiplexing Config.*
- ❑ *Sequencer Control Config.*
- ❑ *Sample Sequencer Result*

Step 5: ADC Interrupt Configuration

- Each AI channel interrupt configuration can be performed separately by using ADC Sequencer Control Configuration Register
- Each Sample Sequencer can also be a source of interrupt that can be configured using ADC Interrupt Control Register
- 4 LSB of below registers are used for masking, status, and clearing of interrupts from the four sequencers

Register label	Offset	Reset value	Brief description
ADC_INT_MASK_R	0x008	0x00000000	Interrupt mask register.
ADC_RIS_R	0x004	0x00000000	Interrupt raw status register.
ADC_INT_STATUS_CLR_R	0x00C	0x00000000	Interrupt status and clear register.

THANK YOU

Any Questions???