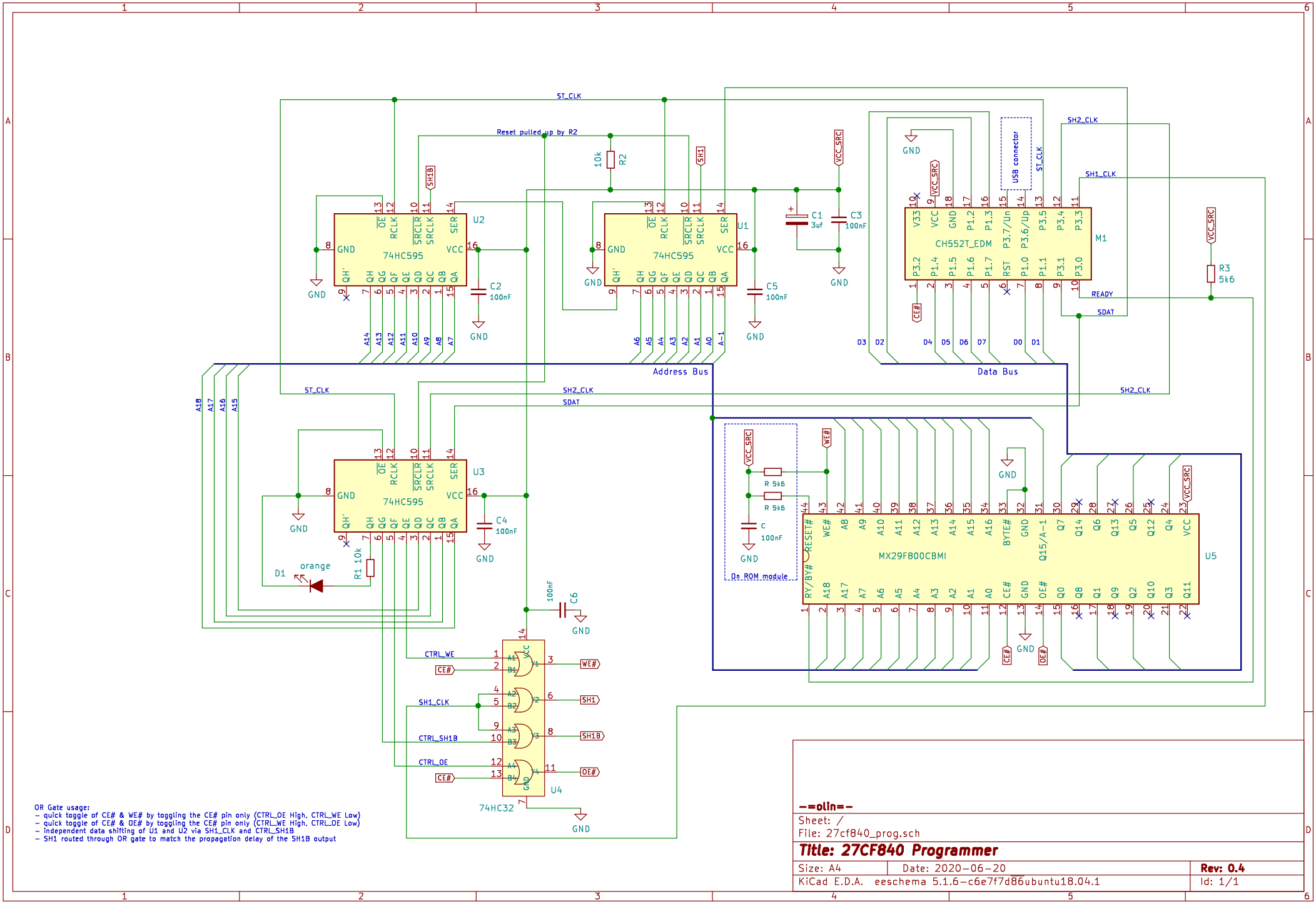
ST_CLK
Reset pulled up by R2
10k
R2
SH1B
SH1
VCC_SRC
C1
3uf
C3
100nF
SH2_CLK
SH1_CLK
USB connector
ST_CLK
GND
U2
U1
U3
74HC595
OE
RCLK
SRCLR
SRCLK
SER
QH'
QH
QG
QF
QE
QD
QC
QB
QA
VCC
C2
100nF
C5
100nF
C4
100nF
M1
CH552T_EDM
V33
P3.2
P1.4
P1.5
P1.6
P1.7
RST
P1.0
P1.1
P3.1
P3.0
P3.7/Un
P3.6/Up
P3.5
P3.4
P3.3
P1.2
P1.3
CE#
READY
SDAT
R3
5k6
D3
D2
D4
D5
D6
D7
D0
D1
Address Bus
Data Bus
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
A-1
A18
A17
A16
A15
SH2_CLK
SDAT
D1
orange
R1 10k
100nF
C6
CTRL_WE
CTRL_SH1B
CTRL_OE
WE#
OE#
U4
74HC32
A1
B1
A2
B2
A3
B3
A4
B4
Y1
Y2
Y3
Y4
VCC
GND
R 5k6
R 5k6
C
100nF
On ROM module
MX29F800CBMI
U5
RESET#
RY/BY#
WE#
BYTE#
Q15/A-1
CE#
OE#
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
OR Gate usage:
- quick toggle of CE# & WE# by toggling the CE# pin only (CTRL_OE High, CTRL_WE Low)
- quick toggle of CE# & OE# by toggling the CE# pin only (CTRL_WE High, CTRL_OE Low)
- independent data shifting of U1 and U2 via SH1_CLK and CTRL_SH1B
- SH1 routed through OR gate to match the propagation delay of the SH1B output
-=olin=-
Sheet: /
File: 27cf840_prog.sch
Title: 27CF840 Programmer
Size: A4
Date: 2020-06-20
Rev: 0.4
KiCad E.D.A. eeschema 5.1.6-c6e7f7d86ubuntu18.04.1
Id: 1/1