

N-Channel 250-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
250	0.155 at $V_{GS} = 10$ V	3.0
	0.162 at $V_{GS} = 6.0$ V	2.9

FEATURES

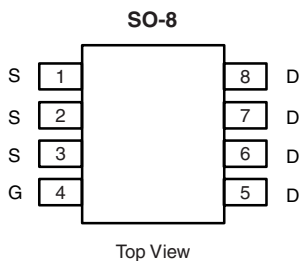
- Halogen-free According to IEC 61249-2-21 Definition
- PWM-Optimized TrenchFET® Power MOSFET
- 100 % R_g Tested
- Avalanche Tested



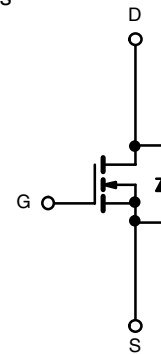
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Primary Side Switch In:
 - Telecom Power Supplies
 - Distributed Power Architectures
 - Miniature Power Modules



Ordering Information: Si4434DY-T1-E3 (Lead (Pb)-free)
Si4434DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	250		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	3.0	2.1	A
		2.4	1.7	
Pulsed Drain Current	I_{DM}	30		
Continuous Source Current (Diode Conduction) ^a	I_S	2.6	1.3	
Avalanche Current	I_{AS}	13		mJ
Single Pulse Avalanche Energy	E_{AS}	8.4		
Maximum Power Dissipation ^a	P_D	3.1	1.56	W
		2.0	1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	33	40	$^\circ\text{C/W}$
		65	80	
Maximum Junction-to-Foot (Drain)	R_{thJF}	17	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

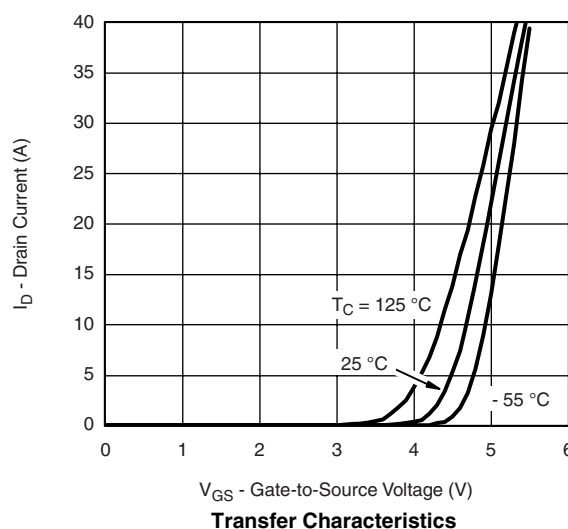
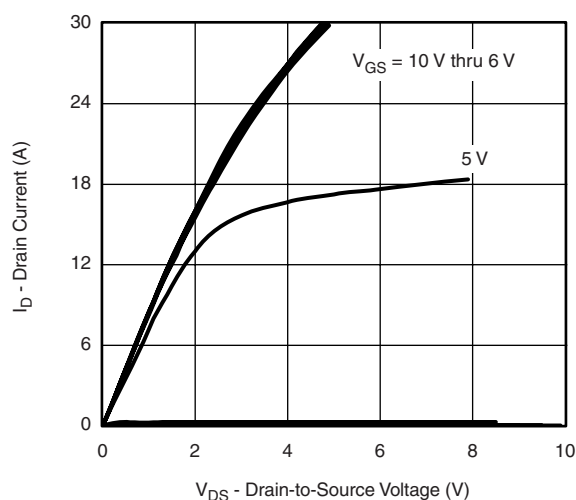
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2.0		4.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 250\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			15	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 3.0\ \text{A}$		0.129	0.155	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 2.9\ \text{A}$		0.131	0.162	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 3.0\ \text{A}$		14		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.8\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 100\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 3.0\ \text{A}$		34	50	nC
Gate-Source Charge	Q_{gs}			6.8		
Gate-Drain Charge	Q_{gd}			10.5		
Gate Resistance	R_g		0.6	1.2	1.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\ \text{V}$, $R_L = 25\ \Omega$ $I_D \cong 4.0\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		16	25	ns
Rise Time	t_r			23	35	
Turn-Off Delay Time	$t_{d(off)}$			47	70	
Fall Time	t_f			19	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.8\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		100	150	

Notes:

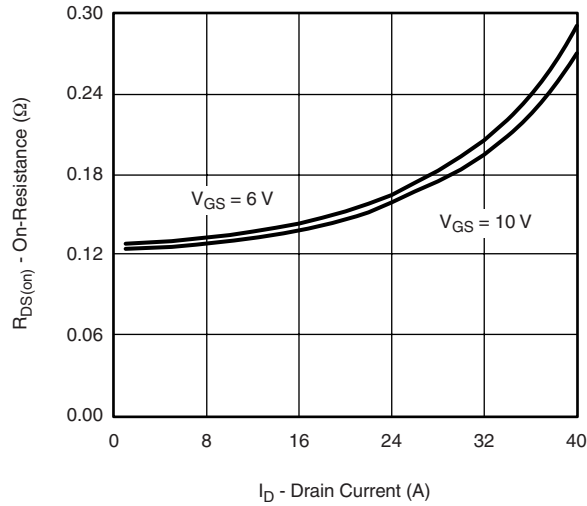
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

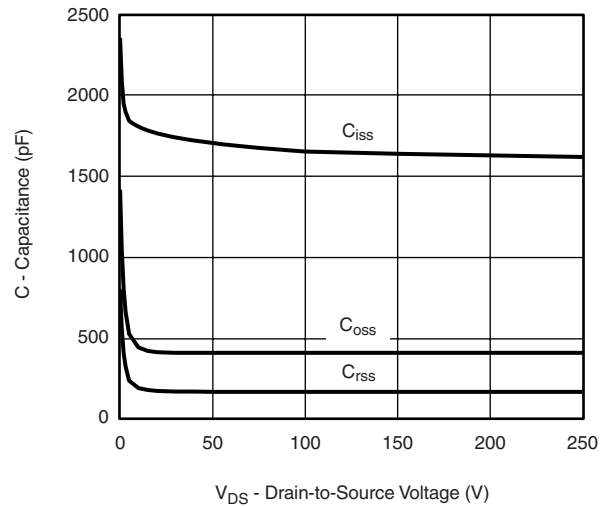
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

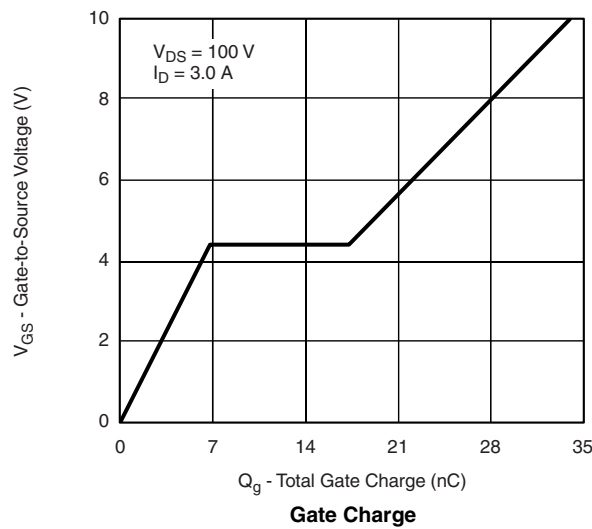
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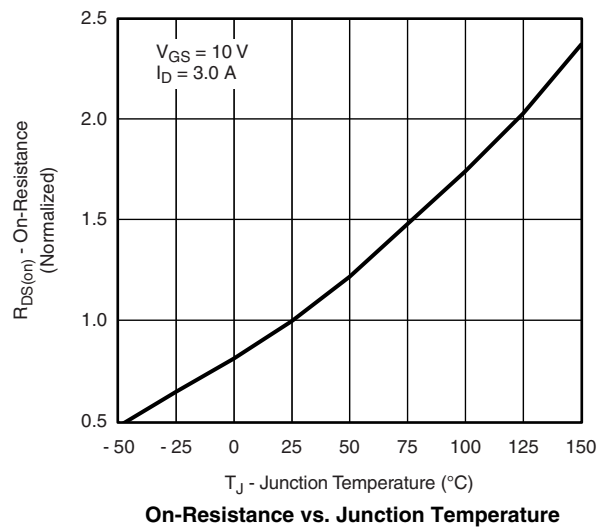
On-Resistance vs. Drain Current



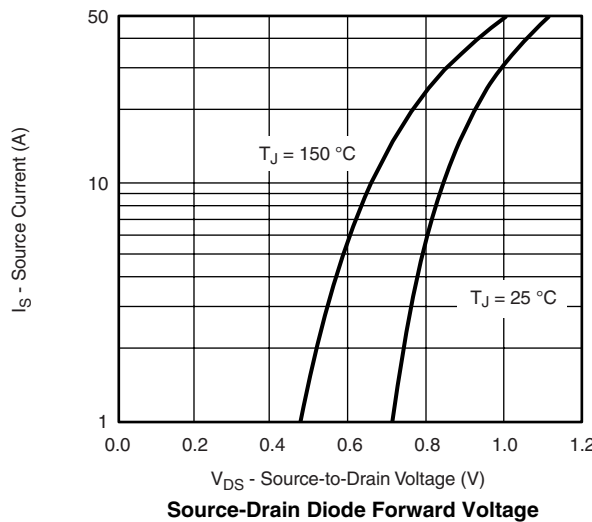
Capacitance



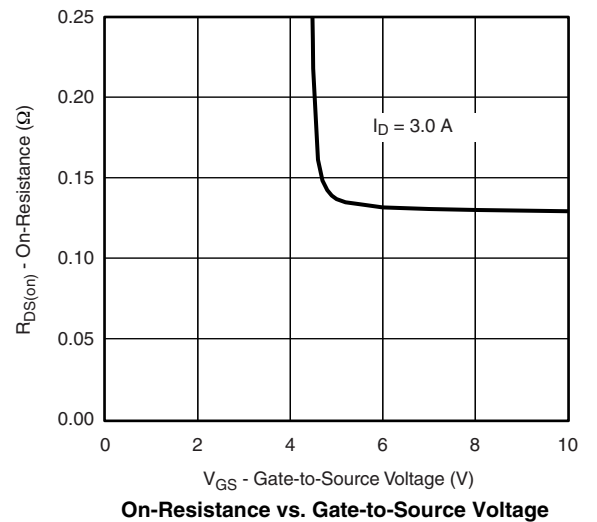
Gate Charge



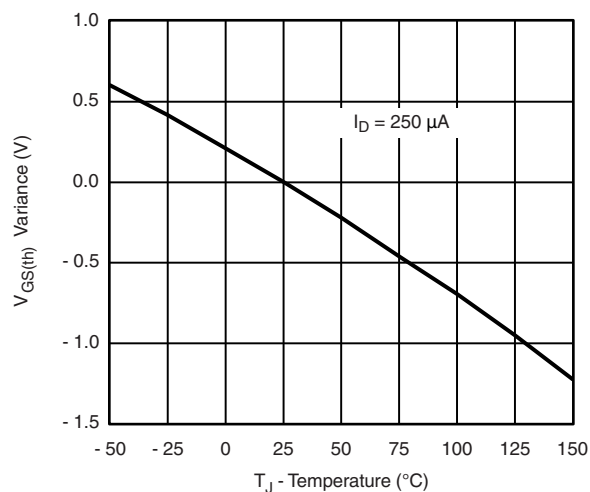
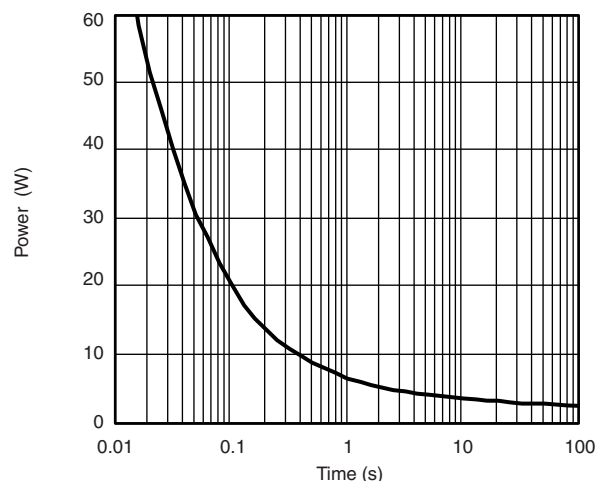
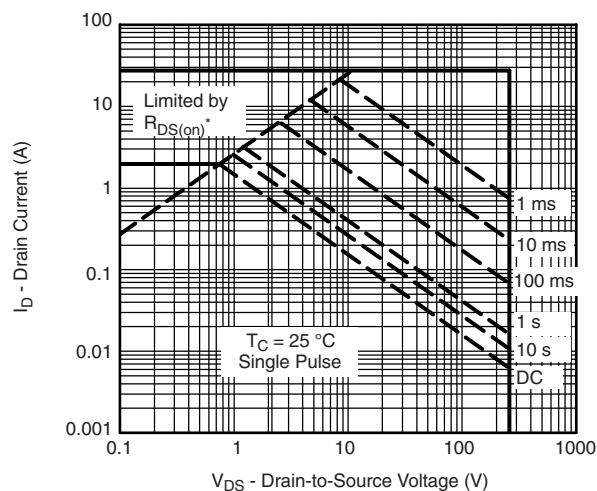
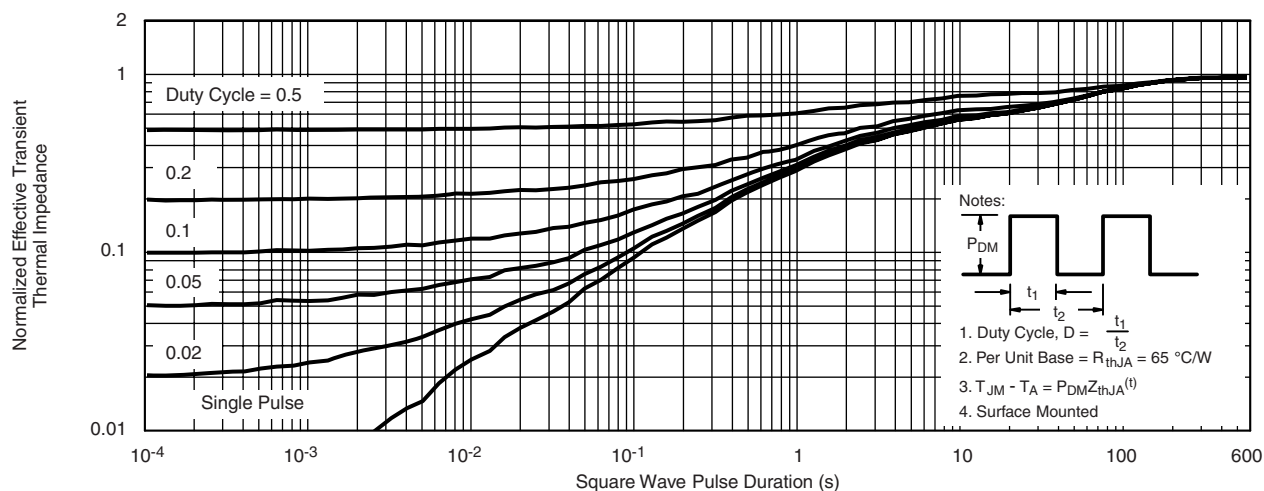
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



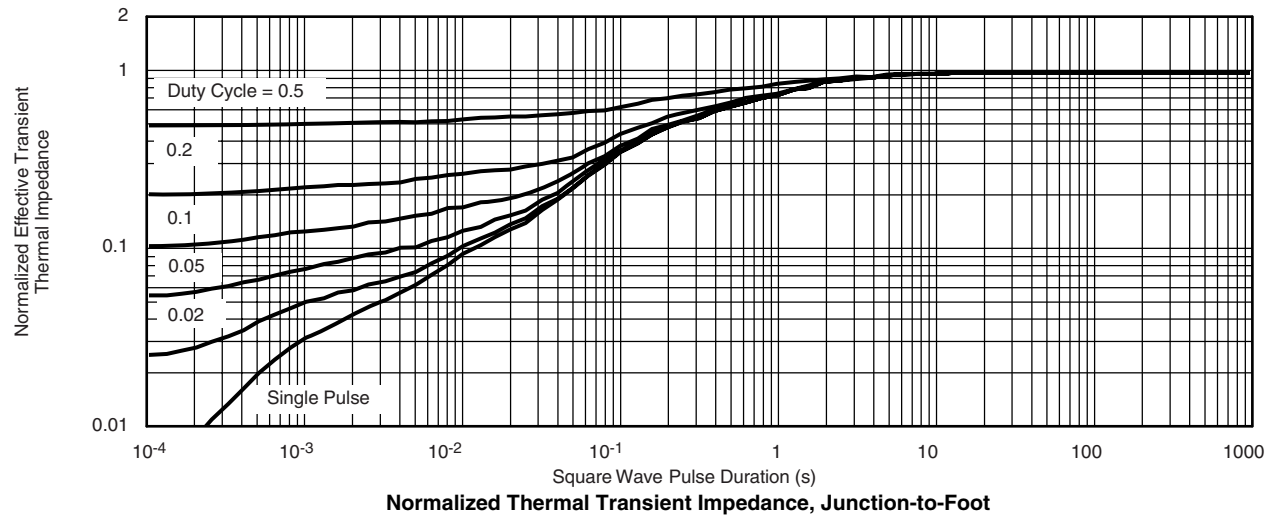
On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Threshold Voltage****Single Pulse Power*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Case****Normalized Thermal Transient Impedance, Junction-to-Ambient**

- Notes:
1. Duty Cycle, $D = \frac{t_1}{t_1 + t_2}$
 2. Per Unit Base = $R_{thJA} = 65 \text{ °C/W}$
 3. $T_{JM} - T_A = P_{DM} Z_{thJA}^{(t)}$
 4. Surface Mounted



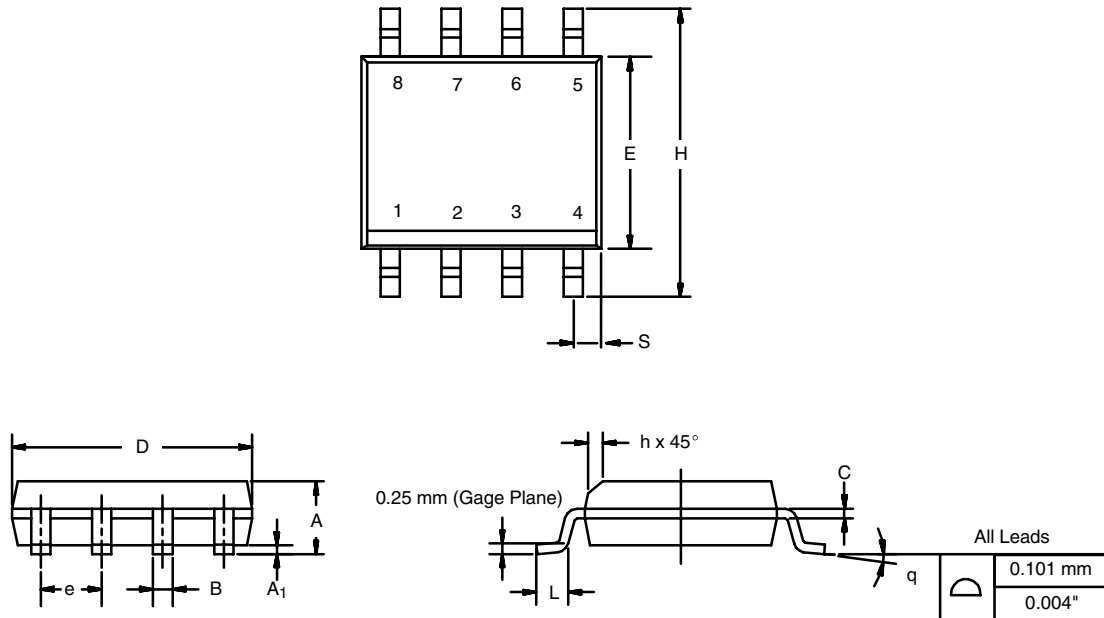
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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