



Article

Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging [†]

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Abstract: State-of-the-art ultra-fast battery chargers for electric vehicles simultaneously require high efficiency and high power density, leading to a challenging power converter design. In particular, the grid-side filter, which ensures sinusoidal current absorption with low pulse-width modulation (PWM) harmonic content, can be a major contributor to the overall converter size and losses. Therefore, this paper proposes a complete analysis, design and optimization procedure of a three-phase LCL filter for a modular DC fast charger. First, an overview of the basic LCL filter modeling is provided and the most significant system transfer functions are identified. Then, the optimal ratio between grid-side and converter-side inductance is discussed, aiming for the maximum filtering performance. A novel design methodology, based on a graphical representation of the filter design space, is thus proposed. Specifically, several constraints on the LCL filtering elements are enforced, such that all feasible design parameter combinations are identified. Therefore, since in low-voltage high-power applications the inductive components typically dominate the overall filter volume, loss and cost, the viable LCL filter design that minimizes the total required inductance is selected. The proposed design procedure is applied to a 30 kW, 20 kHz 3-level unidirectional rectifier, employed in a modular DC fast charger. The performance of the selected optimal design, featuring equal grid-side and converter-side 175 μ H inductors and 15 μ F capacitors, is verified experimentally on an active front-end prototype, both in terms of harmonic attenuation capability and current control dynamics. A current total harmonic distortion (THD) of 1.2% is achieved at full load and all generated current harmonics comply with the applicable harmonic standard. Moreover, separate tests are performed with different values of grid inner impedance, verifying the converter control stability in various operating conditions and supporting the general validity of the proposed design methodology.



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1. Introduction

Even though the performance of Li-ion batteries is constantly increasing, their weight and cost still pose a major barrier to a widespread vehicle electrification [1]. Nevertheless, the limited range of electric vehicles (EVs) can be addressed with a distributed DC ultra-fast charging infrastructure, which would allow charging times comparable with the refueling of an internal combustion engine (ICE) vehicle, thus providing a solution to the infamous EV range anxiety for most of the population. The present and future challenges for implementing such an infrastructure are mainly related to available power electronics technology, competing industry standards and the impact on the grid of widespread high power charging stations [2–4]. In spite of the challenges, the electric mobility market is expanding exponentially and thousands of DC fast-charging stations are currently being installed around the world [5,6], making this topic of particular interest for both industry and academia.

State of the art DC ultra-fast chargers (UFCs) are typically connected to the low-voltage grid, thus leveraging the industrial power electronics expertise and availability [3,7–9]. The charger generally consists of two power converter stages [3], which are schematically represented in Figure 1. The first stage, referred to as active front-end (AFE), is a grid-connected three-phase AC/DC converter with unity power factor correction (PFC) capabilities. This stage must absorb the total charging power from the grid, meanwhile ensuring sinusoidal input current shaping with low distortion and harmonic content [10]. The second stage is an isolated DC/DC converter, which controls the charging process (i.e., the battery-side current) and provides galvanic isolation from the grid [11].

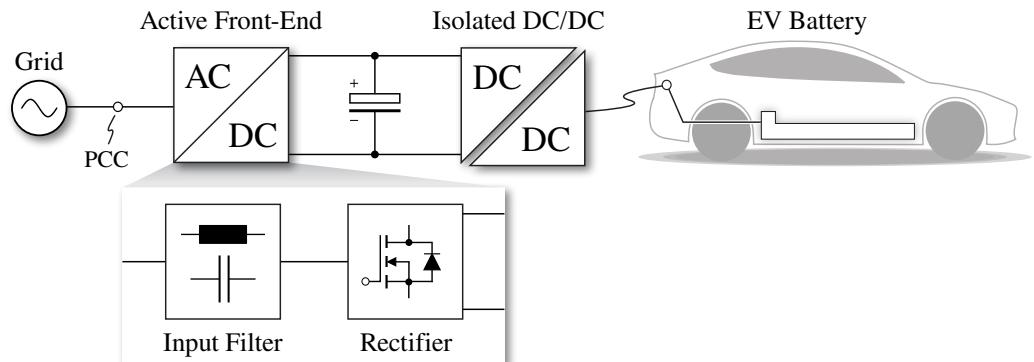


Figure 1. Schematic overview of an electric vehicle (EV) ultra-fast battery charger, with highlight of the active front-end (AFE) structure.

The main requirements of a UFC include (1) high efficiency, (2) high power density, (3) sinusoidal input current absorption, (4) wide input/output voltage range and (5) low battery-side current ripple, which may affect the battery aging process [12]. While requirements (4) and (5) are mainly addressed by the DC/DC stage, (1), (2) and (3) also affect the AC/DC converter, which is the focus of this work.

The most simple and widely adopted topology for active rectification is the 2-level inverter, which benefits from inherent bidirectional capabilities. However, due to its 2-level output voltage waveform and the high voltage rating of the employed semiconductor devices, this converter is affected by a severe performance trade-off between achievable efficiency and power density. In fact, a smaller overall size can only be achieved by increasing the operating switching frequency, thus leading to higher switching losses and lower conversion efficiency [13,14]. An effective approach to simultaneously improve both performance indices of the AC/DC converter is to adopt multi-level topologies, which offer better overall performance in exchange for higher complexity and component count.

Since UFCs only require that the power flows from the grid to the vehicle, 3-level unidirectional rectifiers represent an attractive alternative to their 2-level counterpart, as they achieve an excellent trade-off between efficiency, power density and overall complexity [13–16]. In particular, the multi-level structure of these rectifiers allows them to simultaneously increase the switching frequency (i.e., adopting devices with lower voltage rating) and the number of output voltage levels, notably reducing the stress on the filtering components and thus enabling an improved trade-off between efficiency and power density. Moreover, due to their unidirectional nature, 3-level rectifiers ensure minimum converter complexity, as the number of active devices is lower than or equal to 2-level inverters and no switching dead-times are required (i.e., each converter leg features a single 4-quadrant switch).

The main tasks of a 3-level AFE for battery charging are (1) to ensure sinusoidal input current with low distortion and harmonics, (2) to regulate the DC-link voltage according to the DC/DC stage optimal operating conditions [11], (3) to minimize the third-harmonic voltage oscillations of the DC-link mid-point, typical of 3-level converters [17,18], and (4) to fully control the steady-state mid-point voltage deviation [19]. While all of these tasks require a converter control with sufficient dynamical performance [10] and an appropriate

modulation strategy [20], (1) also requires a proper design of the grid-side filter, which may strongly affect the overall converter performance and is thus the subject of this work.

The AFE input filter, schematically represented in Figure 1, must ensure that the converter complies with grid current harmonic restrictions at the point of common coupling (PCC), such as IEEE 519 [21]. The role of the filter is to attenuate the high-frequency harmonics generated by the pulse-width modulation (PWM) operation of the converter, such that they do not flow into the grid and affect other devices connected to the PCC.

The most simple filter topology is the purely inductive L filter, which corresponds to the direct utilization of the AFE boost inductors for filtering purposes. However, despite its simplicity, this filter provides very low harmonic attenuation for a given total inductance (i.e., 20 dB/dec roll-off), thus resulting in excessive volume, weight and power loss [22]. Substantially better performance are achieved with an LCL filter, due to its superior attenuation capability (i.e., up to 60 dB/dec roll-off) and thus reduced filter size and losses [22]. A lower total inductance leads to lower filter cost and enables higher converter dynamical performance, if the filter and the control loop are properly designed. However, the high order of the filter affects the complexity of the design procedure, since multiple degrees of freedom are available and several constraints of different nature must be enforced. Furthermore, the filter resonance may amplify unwanted harmonics and may negatively affect the closed-loop current control gain and phase margins, even leading to instability [23,24]. Therefore, the resonance peak must be mitigated either by passive or active damping methods [25,26], which add further complexity to the filter design and/or to the converter control [27].

It is worth noting that in modern high-frequency power converters, the LCL filter generally represents the first element of a multi-stage differential-mode EMI filter [28], as it provides the required attenuation for the current harmonics with highest energy content, i.e., situated in the lower part of the 0.15–30 MHz CISPR range [29]. Nevertheless, high-frequency EMI filtering is a complex and broad topic and does not represent the scope of this work, therefore it is not discussed further in this paper.

Due to the complexity and the importance of the input filter in grid-connected converters, several design procedures have been proposed in literature [22,30–37]. Most of these approaches are based on iterative step-by-step solutions [22,30,32–35], which require the verification of either the filter parameter constraints, the attenuation results or the converter control stability within the design procedure itself, leading to a not straightforward solution. In the following paragraphs each reference is analyzed individually, to better highlight the contributions of the present work.

Among the above mentioned design approaches, [22] aims at minimizing the total energy stored by the LCL filter. However, the energy minimization criteria ensures neither the total volume nor the total loss minimization, since the energy storage density of inductors and capacitors can differ by multiple orders of magnitude [38] and inductor losses tend to dominate over capacitor ones, especially in high power applications.

The design methodologies adopted in [30,32] determine the converter-side inductance from a maximum current ripple target, select the filter capacitance to achieve a fixed reactive power generation and determine the grid-side inductance from the harmonic attenuation requirement. These procedures particularly fail to identify the role of the ratio between the grid-side and the converter-side inductance values in the filter size and loss minimization, thus leading to sub-optimal filter designs.

This issue is addressed in [33], where the advantages of having equal grid-side and converter-side inductance values are leveraged to minimize the filter size, however the filter resonance frequency is fixed from active-damping considerations, severely limiting the filter design space and thus leading to sub-optimal results.

The most promising optimization approach is proposed in [34,35], which also leverages equal grid-side and converter-side inductance values, meanwhile taking into account several design constraints on the filter parameters. This procedure achieves optimal design results with minimum total inductance and capacitance, however no constraint on the minimum converter-side inductance value is applied, which can lead to excessive

inductor current ripple and losses, translating in low overall efficiency. Moreover, a partial graphical approach is attempted to identify the required total inductance as function of the switching-to-resonance frequency ratio. However, not all filter constraints are here displayed, thus inhibiting the full view of the actual filter design space.

Besides considering the filter size, the design procedures proposed in [31,36,37] also take into account the filter losses, either generated by passive damping resistors or by the filtering components (i.e., inductors, capacitors). In particular, in [31] a conventional filter design procedure is followed, however the inductance and capacitance values that minimize the overall filter losses, meanwhile complying with the attenuation requirements, are selected. Nevertheless, this design methodology is based on a fixed resonance frequency (i.e., selected from control bandwidth considerations), resulting in sub-optimal design results. In [36,37], instead, a Pareto-optimization approach is undertaken, sweeping the filter component values and searching for an optimal design trade-off between filter size and losses. Nevertheless, no direct design procedure is provided, as the design results are found by means of a parametric sweep.

Even though the literature on LCL filters and their applications is extensive and well established, according to the authors' best knowledge, no direct (i.e., non-iterative) optimization procedure aiming at minimizing the filter size and losses, meanwhile taking into account all relevant constraints, has yet been presented. In particular, all found design methodologies either miss some parameter constraints, achieve sub-optimal design results or do not provide a step-by-step repeatable approach. Moreover, no procedure provides a clear overview of the filter degrees of freedom and their boundaries, which may prove extremely useful to both experienced designers and engineers unfamiliar with the topic. As a further note, none of the mentioned LCL filter design procedures has been applied to 3-level unidirectional rectifiers.

Therefore, this work proposes a novel non-iterative design procedure for LCL filters, based on a complete graphical representation of the filter design space. This simple and straightforward approach, first proposed in [39] (i.e., applied to differential-mode EMI filters for switch-mode AC power sources), allows for a better understanding of the degrees of freedom available to the designer and the constraints that must be enforced, thus simplifying the identification of the optimal design results. In particular, this work is an extension of [40], where the design procedure has only been briefly described. The major contribution of this paper is to present exclusive experimental results, aimed at validating the proposed design methodology with a purposely built LCL filter for a 30 kW 3-level unidirectional AFE unit for EV ultra-fast charging.

This paper is structured as follows. In Section 2 the equivalent circuit model of the system under consideration is reported and the most significant LCL filter transfer functions are discussed. In Section 3 the filter degrees of freedom and parameter constraints are identified and the proposed graphical design methodology is described. This procedure is then applied to the input filter of a 30 kW, 20 kHz 3-level AFE for EV ultra-fast charging, identifying the feasible LCL filter design with lowest total inductance. In Section 4 the performance evaluation of the designed filter is performed both in simulation environment and experimentally, verifying the PCC current distortion and the closed-loop control stability on a converter prototype. Finally, Section 5 summarizes and concludes this paper.

2. Filter Model

The system under consideration consists of a three-phase active rectifier, an LCL filter and the grid. The equivalent circuit of the complete system is reported in Figure 2. The grid is modeled by three sinusoidal voltage sources u_{abc} , each in series with an inductive impedance L_g , representing the sum of the line inductance and the leakage inductance of the distribution transformer. The active rectifier is modeled by two three-phase sets of voltage sources, representing the grid-frequency (i.e., low-frequency) voltage components $v_{abc,LF}$ and the switching-frequency (i.e., high-frequency) voltage components $v_{abc,HF}$, respectively. Additionally, the LCL filter may include a set of damping resistors in series with the filtering capacitors, depending whether passive damping needs to be provided.

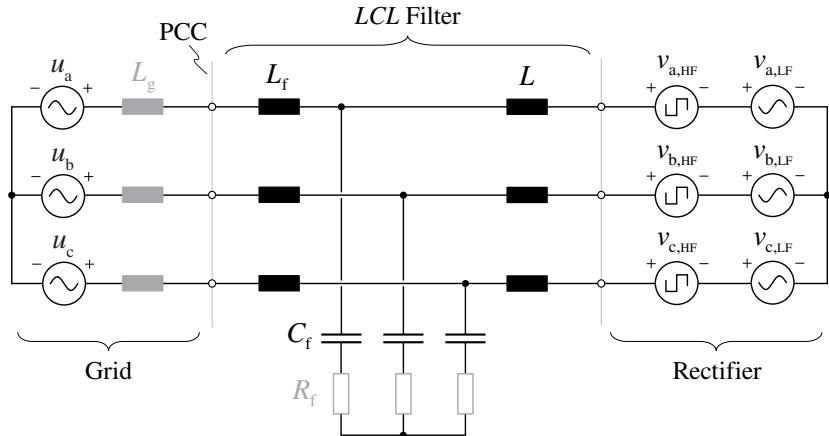


Figure 2. Equivalent circuit of the considered three-phase system, consisting of the active rectifier, the LCL filter and the grid. L is the converter-side inductance, C_f is the filter capacitance and L_f is the grid-side filter inductance. Additionally, L_g represents the grid internal inductance and R_f is the filter damping resistance. Since these components are not always present or quantitatively meaningful to the analysis, they are shown in grey.

Due to its symmetrical three-phase properties, the considered model can be represented with the single-phase equivalent circuit illustrated in Figure 3. It must be noted that the low-frequency voltage sources of Figure 2 appear as short circuits, both from a high-frequency harmonic perspective (i.e., filter attenuation) and from a small-signal stand point (i.e., closed-loop control stability).

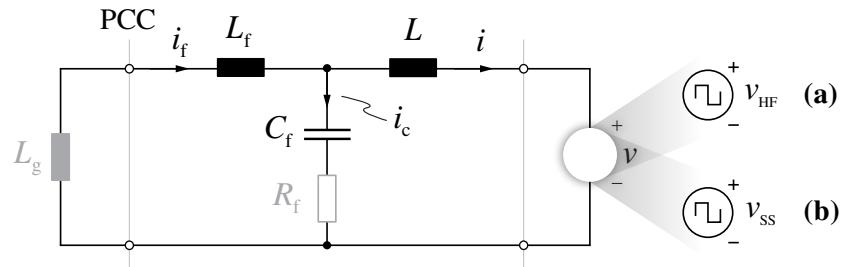


Figure 3. Single-phase equivalent circuit of the considered system, where the converter is represented by the voltage source v . The circuit is valid both from (a) a high-frequency harmonic perspective ($v = v_{HF}$) and from (b) a small-signal (i.e., control) stand point ($v = v_{SS}$).

The most relevant system transfer functions for the filter design can be directly derived from an impedance analysis of the derived equivalent circuit. Referring to the naming conventions of Figure 3,

$$Y(s) = \frac{i(s)}{v(s)} = \frac{1}{sL} \frac{s^2 + 2\xi_f \omega_f s + \omega_f^2}{s^2 + 2\xi_0 \omega_0 s + \omega_0^2}, \quad (1)$$

$$Y_c(s) = \frac{i_c(s)}{v(s)} = \frac{1}{L} \frac{s}{s^2 + 2\xi_0 \omega_0 s + \omega_0^2}, \quad (2)$$

$$Y_f(s) = \frac{i_f(s)}{v(s)} = \frac{1}{s(L + L_f + L_g)} \frac{2\xi_0 \omega_0 s + \omega_0^2}{s^2 + 2\xi_0 \omega_0 s + \omega_0^2}, \quad (3)$$

are obtained, where

$$\begin{cases} \xi_f = \frac{\omega_f R_f C_f}{2} \\ \omega_f^2 = \frac{1}{C_f (L_f + L_g)} \end{cases}, \quad (4)$$

$$\begin{cases} \xi_0 = \frac{\omega_0 R_f C_f}{2} \\ \omega_0^2 = \frac{L + L_f + L_g}{C_f L (L_f + L_g)} \end{cases} . \quad (5)$$

The admittance $Y(s)$ links the voltage applied by the converter to the generated (and controlled) converter-side current. This transfer function plays a key role in the closed-loop current control, affecting its performance and the system stability. The admittance $Y_c(s)$ allows to determine the current flowing into the capacitor branch, thus enabling the estimation of the power losses in the damping resistors (if any) and the voltage ripple on the filter capacitors. Finally, $Y_f(s)$ is the actual filter admittance, relating the high-frequency voltage components generated by the converter (i.e., $v_{abc,HF}$) with the current harmonics injected into the grid at the PCC. This transfer function determines the frequency-dependent filter attenuation and is thus essential for the LCL filter design. A qualitative representation of the magnitude Bode plots of $Y(s)$, $Y_c(s)$ and $Y_f(s)$ is provided in Figure 4, where the effect of different damping resistance values is illustrated.

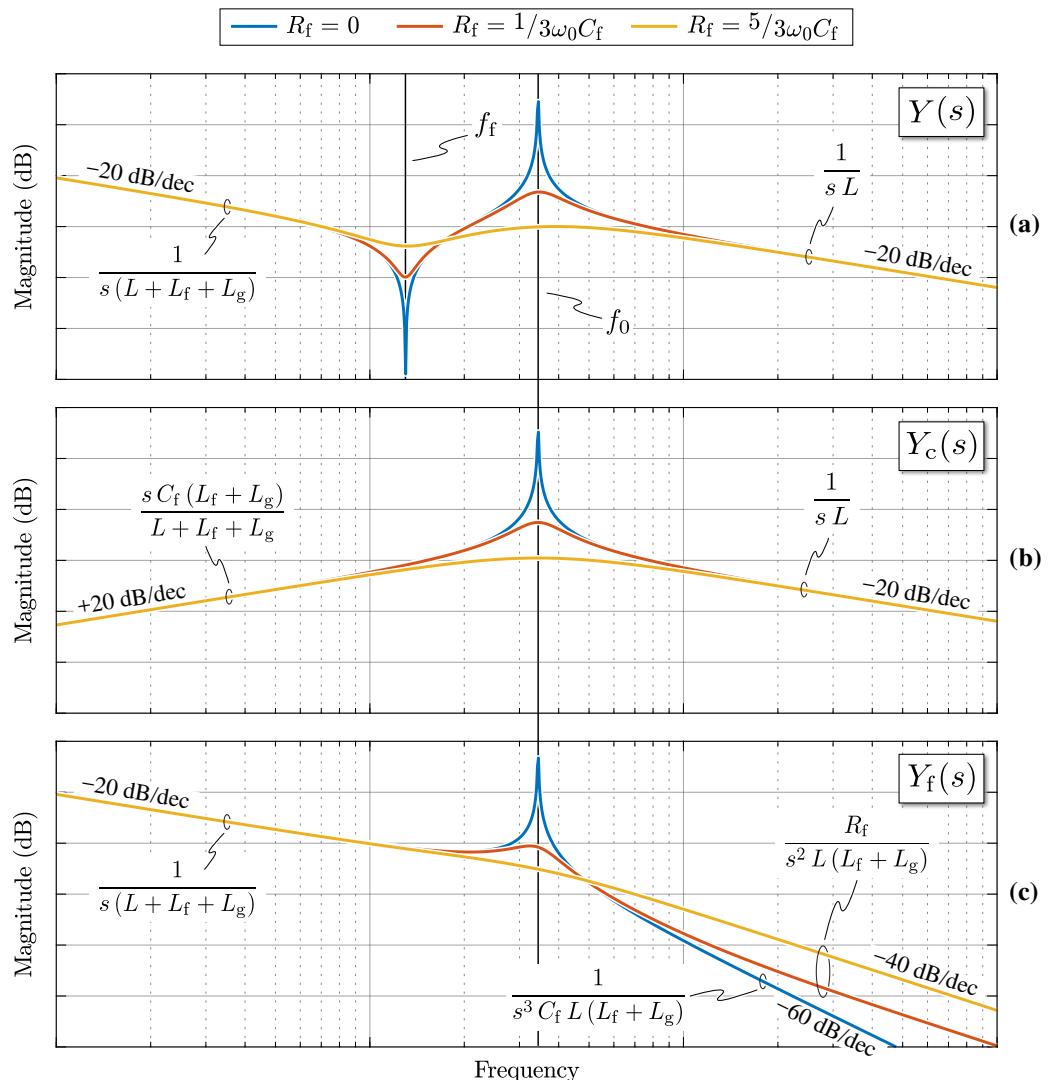


Figure 4. Qualitative representation in the logarithmic scale of the magnitude of $Y(s)$ (a), $Y_c(s)$ (b) and $Y_f(s)$ (c), for different values of damping resistance R_f . The resonance frequencies $f_f = \omega_f/2\pi$ and $f_0 = \omega_0/2\pi$ are indicated, while the asymptotic trends of the transfer functions are noted on the curves.

One parameter that deeply affects the LCL filter performance is the ratio between the grid-side and the converter-side inductance values $k_L = (L_f + L_g)/L$, as reported in [33]. In particular, this ratio can be optimized so that the filter attenuation for a given total amount of inductance $L_{\text{tot}} = L + L_f + L_g$ is maximized. The asymptotic expression of the filter admittance, which corresponds to the inverse of the filter attenuation A , is derived as

$$Y_f(s) \xrightarrow{s \rightarrow \infty} \frac{1}{A(s)} = \begin{cases} \frac{1}{s^3 C_f L_{\text{tot}}^2} \frac{(1+k_L)^2}{k_L} & \text{undamped } (R_f = 0) \\ \frac{R_f}{s^2 L_{\text{tot}}^2} \frac{(1+k_L)^2}{k_L} & \text{damped } (R_f \neq 0) \end{cases}. \quad (6)$$

It can be observed that the minimum filter admittance (i.e., the maximum filter attenuation) is obtained for $k_L = 1$ (i.e., $L = L_f + L_g$), as illustrated in Figure 5.

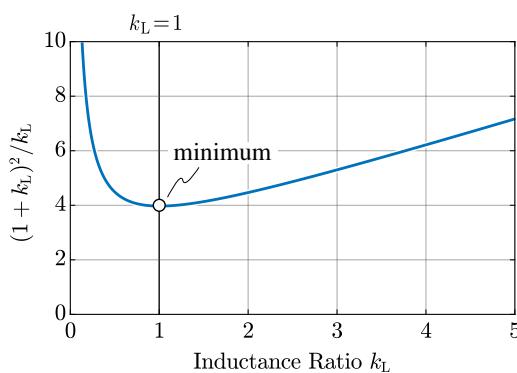


Figure 5. Asymptotic filter admittance trend $\propto (1 + k_L)^2/k_L$ as function of the inductance ratio k_L .

According to (6), for a given attenuation requirement, $k_L = 1$ minimizes the product between the filter capacitance C_f and the total filter inductance L_{tot} , thus resulting in minimum required capacitance for a given total inductance and vice-versa [33,35]. $k_L = 1$ is a necessary condition for the overall LCL filter size minimization, however it is not sufficient: the global minimum must be identified among all possible (L_{tot}, C_f) combinations. Interestingly, two different Pareto optimizations in [37] yield LCL filter designs with equal converter-side and grid-side inductors, indirectly demonstrating the benefits of $k_L = 1$.

In general, the size of both inductive and capacitive components can be assumed to scale proportionally to their stored energy, respectively $\propto LI^2$ and $\propto CV^2$ [38]. Moreover, the energy storage density of inductors (e_L) and capacitors (e_C) typically differs by multiple orders of magnitude, being $e_L \ll e_C$ [38]. Therefore, it can be easily understood that in low-voltage ($V \downarrow\downarrow$) high-power ($I \uparrow\uparrow$) systems, as in the present case, the size of filter inductors largely dominates over the size of filter capacitors.

Moreover, in a first assumption, also filter cost and losses are primarily related to inductive components. This is quantitatively demonstrated in [41] and in [42], where a cost breakdown and a loss breakdown of grid-connected inverter systems are respectively reported.

As a consequence, a direct Pareto optimization is not strictly needed for determining the optimal component values, since a procedure aiming at the minimization of the total filter inductance should be pursued. Nevertheless, since too low inductance values can lead to excessive converter-side current ripple, i.e., generating undesired additional losses in the semiconductor devices and the inductive components themselves, a lower limit to the converter-side inductance value must be set.

Further benefits of minimizing the total filter inductance are minimum voltage drop under load, which allows to minimize the DC-link voltage and thus the semiconductor switching losses, and better dynamic performance, if the control loop is properly designed.

Moreover, $k_L = 1$ (i.e., $L = L_f$ disregarding L_g) allows to adopt equal converter-side and grid-side inductor designs, thus providing substantial effort and cost benefits.

It is worth mentioning that the value of k_L affects the filter sensitivity to the parameter variations, which may in turn affect the converter control stability. One of the most relevant indicators of the LCL filter performance, both from a control and an attenuation perspectives, is the filter resonance frequency f_0 . The per unit sensitivities of f_0 with respect to the per unit filter parameter variations can be obtained from (5), as in [33]:

$$\frac{df_0/f_0}{dL/L} = -\frac{1}{2} \frac{k_L}{1+k_L}, \quad (7)$$

$$\frac{df_0/f_0}{dC_f/C_f} = -\frac{1}{2}, \quad (8)$$

$$\frac{df_0/f_0}{d(L_f + L_g)/(L_f + L_g)} = -\frac{1}{2} \frac{1}{1+k_L}. \quad (9)$$

These expressions are graphically represented in Figure 6, as functions of k_L . While the resonance frequency sensitivity towards the variations of L and C_f (i.e., due to manufacturing tolerances) are of little importance, the sensitivity towards $(L_f + L_g)$ is much more relevant, since the grid inductance L_g may vary depending on the converter installation location and may change with time. This is because L_g reflects the equivalent grid inner impedance at the PCC, which is affected by the distribution grid operating conditions. It is observed from (9) that k_L values higher than unity increase the control robustness against grid impedance variations, as also reported in [33]. Nevertheless, $k_L = 1$ results in a fairly good compromise, as diminishing benefits are obtained by further increasing k_L (see Figure 6).

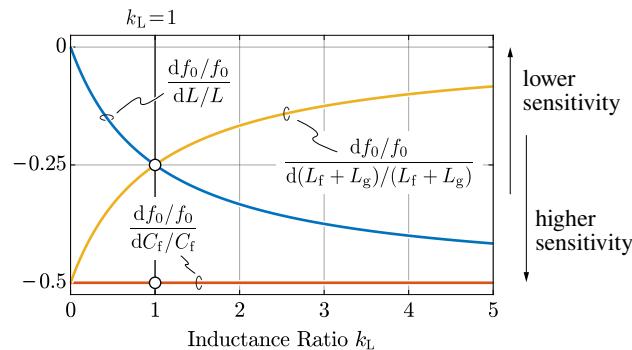


Figure 6. Per unit sensitivities of the LCL filter resonance frequency f_0 with respect to the per unit parameter variations, as functions of the inductance ratio k_L .

The adoption of an LCL filter has a substantial effect on the converter closed-loop control, as the filter resonance strongly affects the system stability. In some cases, depending on the control tuning and the LCL filter component values [23], the control stability may be lost. To avoid this, the most suitable approaches are to reduce the controller bandwidth (if/when allowed) or to adopt active or passive damping solutions [24].

Active damping operates by introducing additional feedback mechanisms inside the control loop, to improve its performance and achieve robust stability [43–46]. On the contrary, passive damping is achieved in a simpler way, by inserting resistors in series with the filter capacitors to directly damp the resonance peak [26], as previously shown in Figure 4, or adopting alternative filter structures with higher complexity [47–51]. Even though passively damped LCL filters are characterized by power losses in the resistors and lower overall asymptotic attenuation (i.e., 40 dB/dec), passive damping is typically preferred, due to its simple implementation, straightforward design and no need for additional measurements and computational overhead (i.e., required instead for active damping).

It is worth noting that the required damping cannot be determined without knowing the current control loop transfer function [26]. Nevertheless, when this is the case, a resistance value similar to the impedance of the filter capacitor at the resonance frequency is normally selected, such as $R_f = 1/(3\omega_0 C_f)$ [32].

As previously mentioned, the grid inductance L_g is generally not known during the filter design process. In fact, the converter installation location is usually undefined and it may witness large inductance variations during the day and/or along the year. In general, the converter control stability can be compromised by a weak grid with high inductive impedance and low short-circuit ratios (SCRs), as the filter resonance frequency f_0 decreases and may interfere with the controller bandwidth [52]. For this reason, a suitable margin must be considered during the filter design and the converter control tuning stages.

3. Design Procedure

In this section, the proposed LCL filter design space optimization procedure is described and applied to the specific requirements of an AFE unit for EV ultra-fast battery charging. Therefore, the specifications and performance targets given by the application are first reported. Then, the constraints affecting the LCL filter parameters are analytically derived and formally expressed, so that the filter design space is identified. Finally, the LCL parameter combination minimizing the total filter inductance is selected among the feasible results, ensuring an optimal filter size/loss trade off (i.e., minimum losses for a fixed volume and vice versa).

3.1. Specifications and Performance Targets

This work considers a modular UFC (consisting of N modules) connected to the European low-voltage grid (i.e., 50 Hz, 400 V line-to-line), schematically illustrated in Figure 7. Each of the N AFE modules consists of a 3-level unidirectional T-type rectifier and an LCL filter, both rated at 30 kW nominal active power. Notably, each module must ensure proper filtering at the PCC by itself, since the number of paralleled modules in one installation is generally not defined. The specifications and nominal operating conditions of a single converter unit are summarized in Table 1.

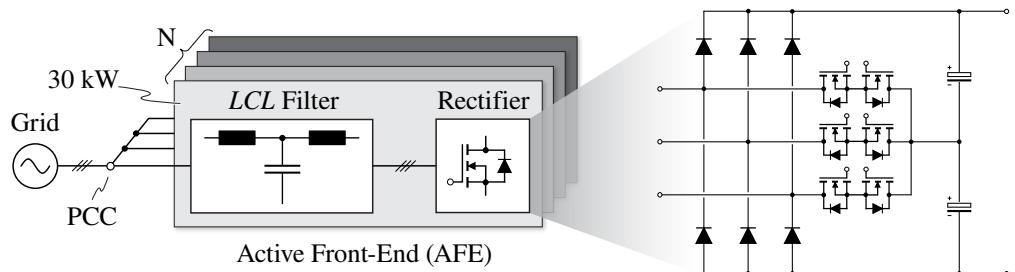


Figure 7. Schematic overview of the considered modular electric vehicle (EV) ultra-fast battery charger with highlight of the active front-end (AFE) T-type converter topology. Each of the N modules is rated at 30 kW nominal active power.

Table 1. Active front-end (AFE) specifications and nominal operating conditions.

Parameter	Description	Value
f	grid frequency	50 Hz
P	nominal active power	30 kW
Q	no-load reactive power	$\leq 3 \text{ kvar}$
V	peak phase voltage	325 V
I	peak phase current	61.5 A
$\cos \varphi$	power factor	≥ 0.995
V_{dc}	DC-link voltage	650–800 V
f_{sw}	switching frequency	20 kHz

The fundamental role of the LCL filter is to achieve the AFE compliance with the harmonic emission standards at the PCC, prescribed by IEEE 519 [21,53]. These standards restrict the maximum amplitude of the current harmonics injected into the grid, varying with the grid voltage level and short-circuit ratio (SCR). In fact, these limits were originally developed to maintain the voltage harmonics at the PCC within a defined percentage of the nominal voltage, considering a purely inductive distribution system [29] (i.e., lower SCR values translate in higher voltage distortion for equal injected current harmonics).

The relevant IEEE 519 harmonic limits for the present application are reported in Table 2 as a percentage of the nominal current. These limits are more stringent for even-order harmonics, which are set to 25% of the odd ones. Since the installation of the converter is not predetermined, as already mentioned, the worst-case SCR ratio (i.e., <20) is considered herein. Moreover, since $f_{sw} = 20$ kHz, all the switching harmonics generated by the converter are higher than the 35th (i.e., 1750 Hz), therefore 0.3% and 0.075% limits apply to odd and even harmonics respectively. Even though IEEE 519 also defines a maximum current total harmonic distortion (THD), the stringent harmonic limits at high frequency allow to directly satisfy the maximum THD constraint by a large margin, given that the low-frequency harmonics are effectively minimized by the converter control.

Table 2. IEEE 519 current harmonic limits for distribution systems with a 0.12–69 kV nominal operating voltage [21]. The reported values refer to the maximum injected odd-harmonic current distortion in percent of I . Even-order harmonics are limited to 25% of the odd-harmonic limits.

I_{sc}/I (SCR)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$
<20	4.0	2.0	1.5	0.6	0.3
20 ... 50	7.0	3.5	2.5	1.0	0.5
50 ... 100	10.0	4.5	4.0	1.5	0.7
100 ... 1000	12.0	5.5	5.0	2.0	1.0
>1000	15.0	7.0	6.0	2.5	1.4

I_{sc} : short-circuit current, I : rated current, h : harmonic number.

3.2. Parameters and Constraints

Due to its high-order structure, an LCL filter has multiple design degrees of freedom, i.e., the filter component values L , L_f , C_f and R_f . Since the grid inner inductance L_g is generally not known, the proposed design procedure considers $L_g = 0$, such that the attenuation performance of the LCL filter are satisfied in every condition.

One design degree of freedom is removed by fixing the ratio between the grid-side inductance and the converter-side inductance at $k_L = 1$ (i.e., $L = L_f$), according to the considerations reported in Section 2. As previously mentioned, this ratio allows to maximize the attenuation performance of the filter for a given amount of total inductance L_{tot} , thus representing a necessary condition for the filter size and loss minimization.

Another degree of freedom is eliminated either by considering an active damping control strategy (i.e., $R_f = 0$) or by selecting the passive damping resistance value as a function of the filter capacitor impedance at the resonance frequency, i.e., $R_f = 1/(3\omega_0 C_f)$ as in [32]. To ease the controller implementation, the passive damping solution is adopted herein.

Therefore, only two design degrees of freedom remain, namely the choice of C_f and of one between L and L_f . Being $k_L = 1$, the parameter $L_{tot} = L + L_f = 2L$ best represents the second degree of freedom.

A three-phase high-power LCL filter for EV ultra-fast battery charging must comply with several design constraints of different nature, namely:

1. The filter resonance frequency f_0 must be higher than 10 times the grid frequency ($f_{0,min} = 10f$), to avoid resonance interactions in the lower part of the harmonic spectrum and allow for a sufficient current control bandwidth (i.e., $f_{bw} < f_0$).
2. The filter resonance frequency f_0 must be lower than half of the switching frequency ($f_{0,max} = f_{sw}/2$), to avoid unwanted amplification of switching harmonics. Even if

damped, the resonance peak tends to amplify the nearby harmonics (see Figure 4c), which may thus exceed the IEEE 519 limits.

3. The current ripple in the converter-side inductor L must be kept below a specified amount to avoid excessive losses in the semiconductor devices (i.e., conduction and switching losses) and in the inductors themselves (i.e., winding and core losses). Moreover, in the present unidirectional case, this current ripple must be limited to narrow the discontinuous conduction mode operation around the waveform zero-crossings, which causes low-frequency harmonic distortion [54]. This limit is set to 20% of the peak nominal current ($\Delta I_{\text{pp,max}} = 0.2 I$).
4. The maximum voltage drop in nominal load conditions must be lower than a specified value depending on the high-line grid voltage ($U_{\text{max}} = 1.1 U_{\text{nom}}$), the maximum modulation index of the active rectifier ($M_{\text{max}} = 2/\sqrt{3} \approx 1.15$, with $M = 2 V/V_{\text{dc}}$) and the minimum DC-link voltage $V_{\text{dc,min}}$, resulting in $\Delta V_{\text{max}} = \sqrt{V_{\text{dc,min}}^2/3 - U_{\text{max}}^2}$.
5. The maximum no-load reactive power generation is set to 10% of the nominal power ($Q_{\text{max}} = 0.1 P$). The reactive current circulation generates losses in the system components (i.e., the LCL filter and the distribution equipment), therefore it must be limited accordingly.
6. The minimum power factor at a specified minimum load condition ($P_{\text{min}} = P/2$) is set to $\cos \varphi_{\text{min}} = 0.995$, taking into account that the unidirectional rectifier cannot generate or absorb reactive power without affecting the low-frequency input current distortion. $P_{\text{min}} = P/2$ is selected taking into account that the adopted modular structure (see Figure 7) allows to turn-off selected converter modules with decreasing load, thus ensuring high power factor over the complete charging range.
7. The minimum filter attenuation $A^*(f_d)$ must ensure that the injected current harmonics comply with the IEEE 519 limits (see Table 2). An additional margin of 50% (i.e., ≈ 3.5 dB), taking into account component tolerances and unmodeled factors, is assumed herein.

Since the LCL filter design space is characterized by two degrees of freedom, all constraints are expressed as functions of C_f and L_{tot} in Table 3.

Table 3. LCL filter design constraints in terms of C_f and L_{tot} , considering $L_g = 0$, $L = L_f$ (i.e., $k_L = 1$) and $R_f = 1/(3\omega_0 C_f)$.

Description	Constraint	Analytical Expression
① minimum resonance frequency	$f_0 \geq f_{0,\text{min}}$	$C_f \leq \frac{1}{\pi^2 f_{0,\text{min}}^2 L_{\text{tot}}}$
② maximum resonance frequency	$f_0 \leq f_{0,\text{max}}$	$C_f \geq \frac{1}{\pi^2 f_{0,\text{max}}^2 L_{\text{tot}}}$
③ maximum inductor current ripple	$\Delta I_{\text{pp}} \leq \Delta I_{\text{pp,max}}$	$L_{\text{tot}} \geq 2 \frac{\Delta \Psi_{\text{pp}}}{\Delta I_{\text{pp,max}}}$
④ maximum load voltage drop	$\Delta V \leq \Delta V_{\text{max}}$	$L_{\text{tot}} \leq \frac{\sqrt{V_{\text{dc,min}}^2/3 - U_{\text{max}}^2}}{2\pi f I}$
⑤ maximum no-load reactive power	$Q \leq Q_{\text{max}} @ P = 0$	$C_f \leq \frac{Q_{\text{max}}}{3\pi f U^2}$
⑥ minimum power factor	$\cos \varphi \geq \cos \varphi_{\text{min}} @ P = P_{\text{min}}$	$C_f \leq L_{\text{tot}} \frac{I_{\text{min}}^2}{U^2} + \frac{P_{\text{min}}}{3\pi f U^2} \frac{\sqrt{1 - \cos^2 \varphi_{\text{min}}}}{\cos \varphi_{\text{min}}}$
⑦ minimum IEEE 519 attenuation	$I_h \leq I_{\text{IEEE,519}}(f_h) \forall h$	$\begin{cases} C_f \geq \frac{A^*(f_d)}{2\pi^3 f_d^3 L_{\text{tot}}^2} & \text{undamped } (R_f = 0) \\ C_f \geq \frac{A^{*2}(f_d)}{36\pi^4 f_d^4 L_{\text{tot}}^3} & \text{damped } (R_f \neq 0) \end{cases}$

The identification of constraints ③ and ⑦ requires either analytical or numerical estimations of the converter voltage waveforms in the time/frequency domains. A numerical approach is pursued herein, implementing a simple and straightforward simulation in MATLAB environment as in [20]. The peak-to-peak converter-side inductor flux ripple $\Delta\Psi_{pp}$ (required by ③) and the full harmonic spectrum of the converter output voltage (required by ⑦) are obtained in post-processing by means of discrete Fourier transforms (DFTs).

A specific 3-level modulation strategy is considered in this work, namely the zero mid-point current modulation (ZMPCPWM) [20]. This strategy practically eliminates the 150 Hz DC-link mid-point voltage ripple typically present in 3-level converters [17,18], thus ensuring minimum DC-link capacitance requirement. Moreover, this feature is particularly needed in EV fast charging, as separate DC/DC units are usually connected to the upper and lower side of the AFE DC-link [55]. In fact, these converter units are subject to the mid-point voltage ripple and they may not be able to reject it [11], allowing for the voltage oscillation to get through and reach the battery-side.

The converter-side inductor flux ripple $\Delta\psi$ is obtained by integration of the high-frequency component of the phase voltage $v_{HF,x}$ (see Figures 2 and 3), assuming that it is completely applied across L (i.e., no voltage ripple at the filter capacitor terminals):

$$\Delta\psi_x(t) = \int_0^t v_{HF,x} dt \quad x = a, b, c. \quad (10)$$

The peak-to-peak flux ripple $\Delta\Psi_{pp}$ is calculated for different values of DC-link voltage within the operating range reported in Table 1. The results are shown in Figure 8 and a maximum value $\Delta\Psi_{pp} = 2.16 \text{ mVs}$ (required by constraint ③) is found for $V_{dc} = 800 \text{ V}$.

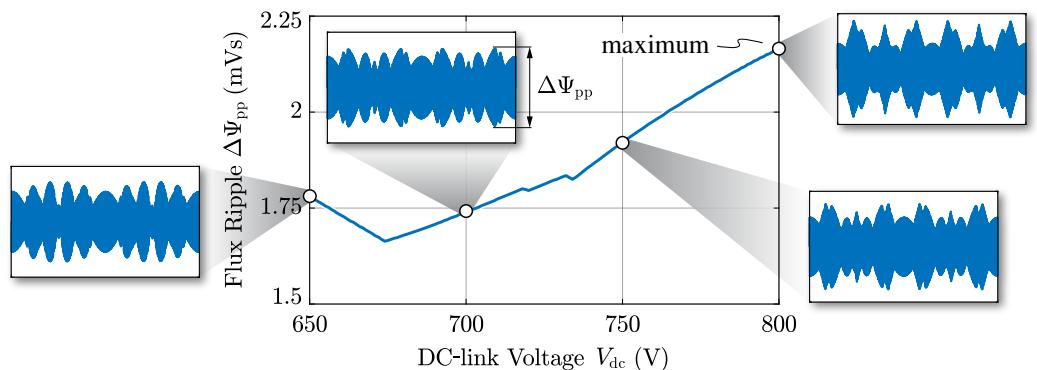


Figure 8. Peak-to-peak grid-side inductor flux ripple $\Delta\Psi_{pp}$ considering zero mid-point current modulation and variable DC-link voltage V_{dc} . A highlight of the time-domain waveforms is provided.

To calculate the minimum attenuation A^* needed to comply with IEEE 519 (i.e., constraint ⑦), the asymptotic filter transfer function expression (6) can be exploited, as the LCL resonance frequency f_0 is sufficiently lower than the switching frequency:

$$A(f_h) = \frac{1}{|Y_{f,S \rightarrow \infty}(j2\pi f_h)|} = \frac{\pi^2 f_h^2 L_{tot}^2}{R_f} \quad f_h \gg f_0. \quad (11)$$

In the present passively damped case, the filter attenuation increases with a 40 dB/dec rate. $A(f_h)$ represents the input-to-output filter impedance at the h -th harmonic, linking the voltage harmonics V_h generated by the converter to the current harmonics I_h injected at the PCC. Therefore, the required harmonic attenuation to satisfy the IEEE 519 limits, including a safety margin, can be described in logarithmic scale (dB) as

$$A_{dB}^*(f_h) = V_{h,dB}(f_h) - I_{h,limit,dB}(f_h) + \text{margin}_{dB}. \quad (12)$$

The harmonic frequency f_h which requires the largest filtering effort to comply with the harmonic limits is referred to as the design frequency f_d :

$$f_d = f_h \iff \max[A^*(f_h) - 40 \log_{10}(f_h)]. \quad (13)$$

This frequency value identifies the worst-case filter design condition, corresponding to the maximum filter component values.

Same as for the flux ripple case, the maximum required attenuation is found for maximum DC-link voltage. The harmonic spectrum of the converter output voltage at $V_{dc} = 800$ V is illustrated in Figure 9, showing an even-order design frequency $f_d = 19.6$ kHz and a required attenuation $A^*(f_d) \approx 570 \Omega \approx 55 \text{ dB } \Omega$ including the 50% design margin.

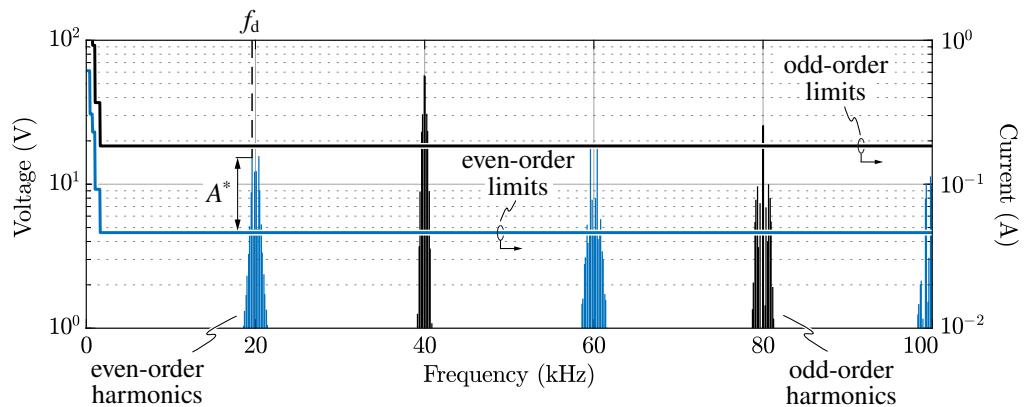


Figure 9. Converter output voltage harmonic spectrum at $V_{dc} = 800$ V and current harmonic limits according to IEEE 519. Odd and even-order harmonics are colored in black and blue respectively. The filter design frequency f_d and the required attenuation A^* (without the margin) are indicated.

It is worth noting that, even though the averaged voltage waveform that is synthesized at the converter output is characterized by half-wave symmetry, the instantaneous PWM waveform is not, thus leading to the generation of both odd and even-order switching harmonics [56]. In particular, the generated harmonic orders can only be odd combinations of the carrier frequency (index m) and the fundamental frequency (index n):

$$f_h = m f_{sw} \pm n f \quad m, n \in \mathbb{N} \text{ and } (m \pm n) = 2k + 1, k \in \mathbb{Z} \quad (14)$$

Therefore, if m is odd, all sideband harmonics with n even disappear and vice-versa. In particular, being $f_{sw} = 20$ kHz an even multiple of $f = 50$ Hz, the h -th harmonic will be an odd or even-order multiple of f only depending on the index n . For instance, the first switching harmonic distribution (i.e., corresponding to $m = 1$) only consists of even-order h harmonics, being n even (i.e., $n = 2, 4, \dots$). On the contrary, the second switching harmonic distribution (i.e., corresponding to $m = 2$) is only made up by odd-order h harmonics, being n odd (i.e., $n = 1, 3, \dots$). This alternating behavior is better illustrated in Figure 9, where odd and even-order harmonics are differently colored.

3.3. Filter Design Space

The proposed design methodology is based on translating the constraints ①–⑦ into boundaries in the filter design space (C_f, L_{tot}), so that the feasible design region can be identified. This representation allows to have a clear view of the available freedom for the filter optimization. Even though multiple different optimization criteria have been proposed in literature (see Section 2), in this work the feasible design with lowest total inductance L_{tot} is considered as the best candidate, since in low-voltage high-power applications inductive components dominate the overall filter size, cost and losses.

The results of the proposed design procedure are illustrated in Figure 10, where the design constraints are graphically represented and bound the available design space. The feasible LCL filter design with minimum total inductance is here found at the intersection between boundaries ③ (i.e., maximum converter-side inductor current ripple) and

⑦ (i.e., minimum required attenuation). The parameters L , C_f , L_f and R_f of the selected optimal design are reported in Figure 10.

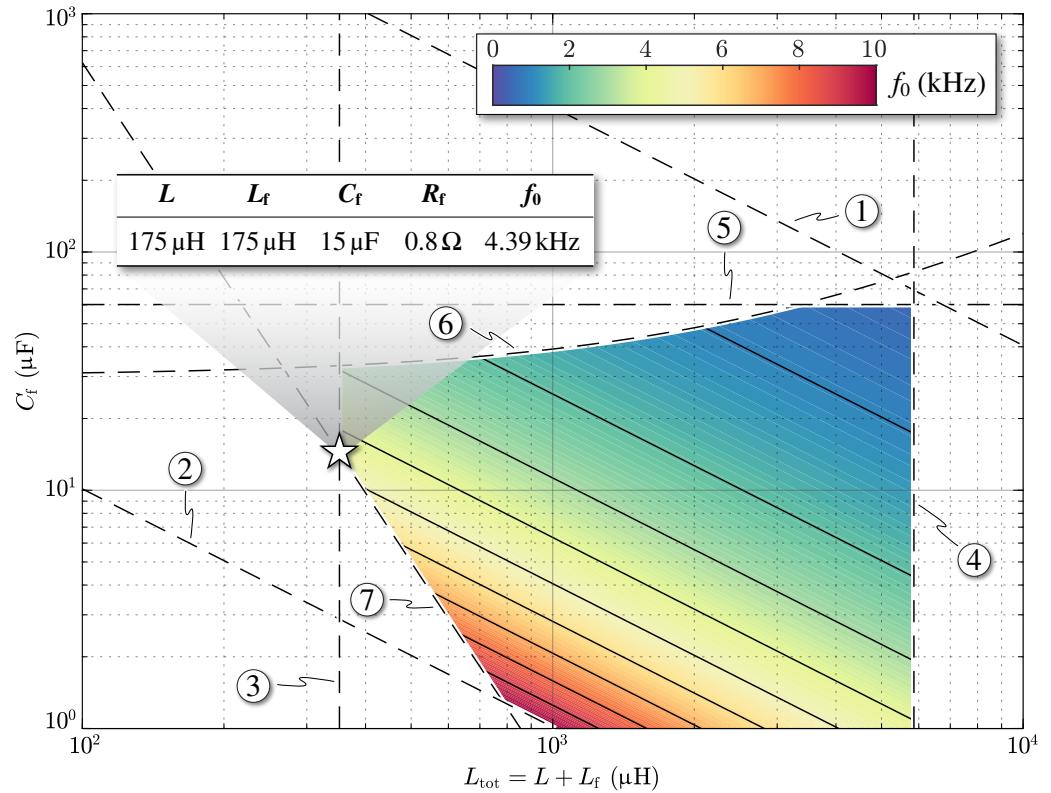


Figure 10. LCL filter design space in the (C_f, L_{tot}) logarithmic plane. Constraints ①–⑦ bound the feasible design region. The design with minimum total inductance is selected and the parameter values of the LCL filter are reported in the highlighted table.

To evaluate the impact of resistor losses on the converter efficiency, they can be calculated by assuming that the high-frequency current ripple Δi_{RMS} completely flows into the capacitor branch (i.e., $\Delta i_{\text{RMS}} = \Delta\psi_{\text{RMS}}/L$) as

$$P_{\text{loss}} = 3 R_f \left[\Delta i_{\text{RMS}}^2 + \frac{U_{\text{RMS}}^2}{[1/(j 2\pi f C_f) + R_f]^2} \right], \quad (15)$$

which are illustrated in Figure 11. In the optimal design point the total damping losses amount to $\approx 13 \text{ W}$, thus yielding a negligible efficiency drop of 0.04%.

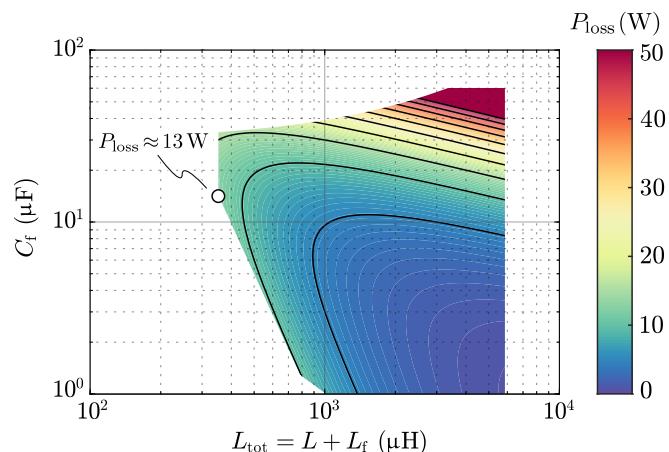


Figure 11. Resistive damping loss as function of L_{tot} and C_f .

4. Simulation and Experimental Results

In this section, the harmonic attenuation achieved by the designed LCL filter and the current control performance of the AFE converter are verified by means of simulation and experimental testing.

The converter-side and grid-side inductors share the same design (i.e., $L = L_f$), which is obtained from an internally developed optimization procedure taking into account a wide database of core geometries, core materials and wire formats/sizes [57]. The adopted loss and thermal models are described in [58].

The resulting inductor design features two stacked EE 6527 cores in XFlux 60 μ powder material from Magnetics [59], with an 18-turn winding of enameled round wire, as illustrated in Figure 12a. The powder material simultaneously provides high saturation flux density and low relative permeability (i.e., $\mu_r = 60$ in the present case), enabling an extremely compact inductor realization. In particular, the low permeability property allows to drastically reduce or even eliminate the air gap between the two core halves. In this way, the inductance value is no longer affected by the gap mechanical tolerance and the unwanted high-frequency winding losses caused by the air gap fringing field (e.g., present in ferrite core implementations) are avoided. However, the complete flux density range of the material (i.e., 0–1.6 T) is not exploited, due to the intrinsic soft saturation characteristics of powder materials [59]. In the present case the inductor is designed to operate between 191 μ H in no-load conditions and 151 μ H at $I_{max} = 61.5$ A, as illustrated in Figure 12b, utilizing only a 0–0.6 T interval to avoid excessive inductance variation during the fundamental line cycle. As a further note, a round wire with large cross-section is used since winding losses are completely dominated by the low-frequency (i.e., 50 Hz) current component. Therefore, the inductor optimization procedure aims to minimize the overall wire DC resistance, clearly avoiding winding arrangements with low window utilization such as litz wire implementations.

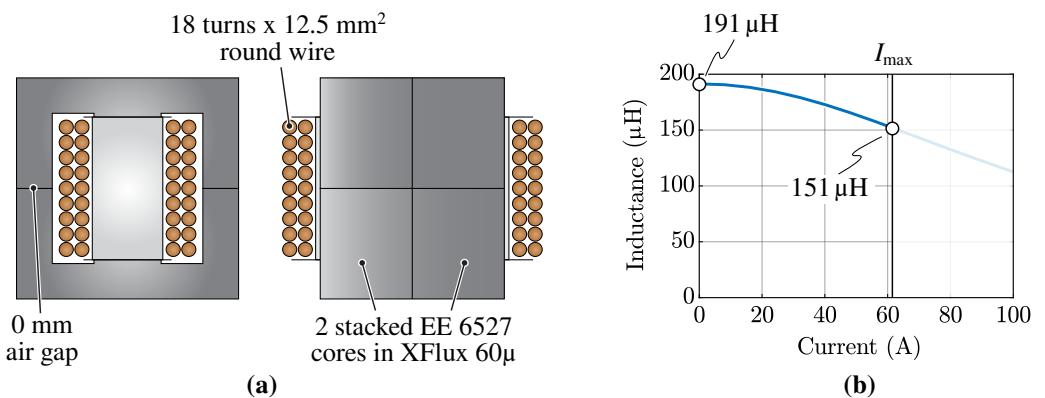


Figure 12. Schematic representation of the designed inductor ($L = L_f$) (a) and differential inductance value dependence on the DC-bias current (b), which highlights the soft saturation characteristic of the selected powder core material.

The AFE converter prototype, including the 3-level unidirectional T-type rectifier and the LCL filter, is shown in Figure 13. The rectifier (see Figure 7) employs 650 V Si MOSFETs switching at 20 kHz and 1200 V Si fast-recovery diodes. The AFE also includes an EMI filter consisting of a three-stage differential-mode filter (including the LCL stage) and a two-stage common-mode filter. Figure 13a,b provide a closer view of the realized filter inductors ($L = L_f$) and the selected filter capacitors (C_f), highlighting the size difference between them.

It is worth noting that the converter prototype is a 60 kW unit consisting of two three-phase sub-units in parallel. In the present case, only one 30 kW three-phase unit is operated and the boost inductors of the other unit are exploited as grid-side filter inductors (L_f).

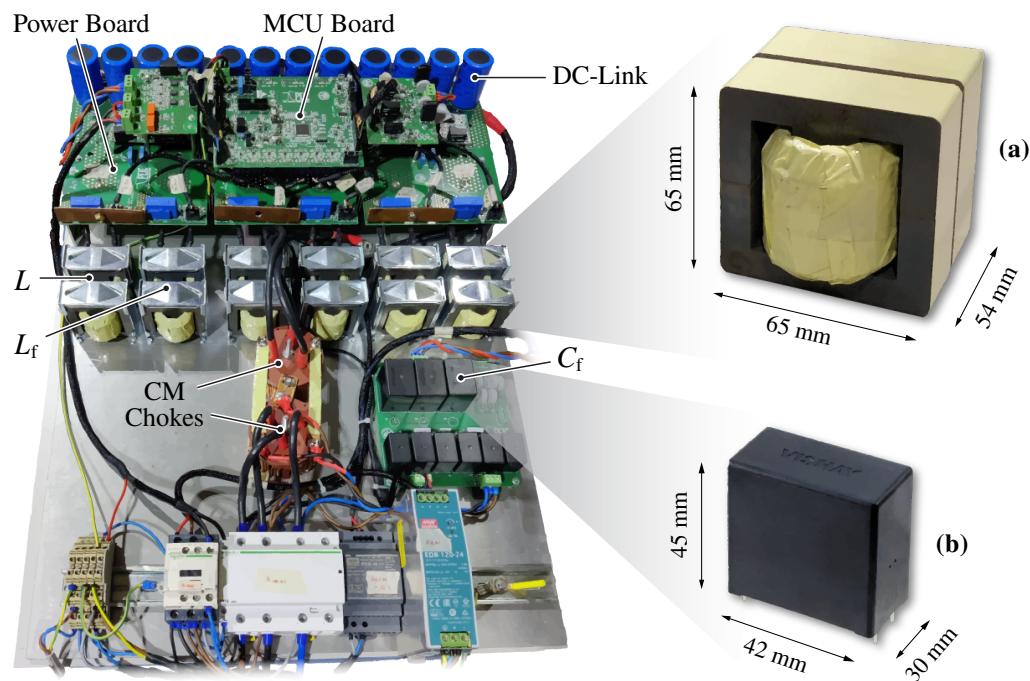


Figure 13. Overview of the active front-end (AFE) prototype utilized for the experimental tests, with highlight of (a) the realized inductor ($L = L_f$) and (b) the selected capacitor (C_f).

4.1. Filter Transfer Functions

The only LCL filter transfer function that can be directly measured is $Y(s)$, which represents the inverse of the filter impedance seen from the converter side. This impedance is measured with the setup illustrated in Figure 14, where a Hioki 5352-50 LCR meter is adopted for the task.

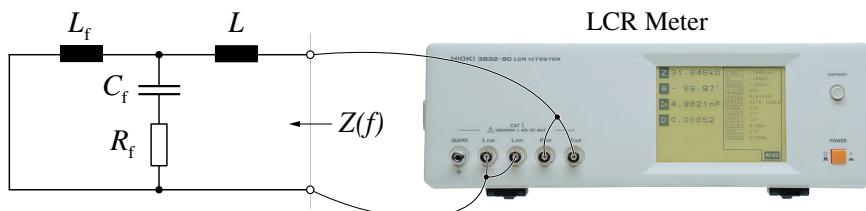


Figure 14. Experimental setup utilized to measure the value of $Y = 1/Z$ (see Figure 15a).

The transfer functions Y , Y_c and Y_f of the designed LCL filter are analytically calculated with the parameters reported in Figure 10 according to (1), (2) and (3), respectively. These transfer functions are illustrated in Figure 15 for both the undamped ($R_f = 0$) and the damped ($R_f = 0.8 \Omega$) cases. The measurement results of Y are reported in Figure 15a for comparison purposes, where a close match with the analytical model is observed. A slight asymptotic deviation between the two transfer functions is mainly attributable to the inductance value of $191 \mu\text{H}$ at zero DC-bias current (i.e., the measurement condition), which differs from the design value of $175 \mu\text{H}$. Another discrepancy is observed around the two resonance frequencies f_f and f_0 , where the experimental results show a stronger damping of the resonance peaks. This is caused by the unmodeled parasitic AC resistance of the filtering elements, mostly given by the inductors (i.e., winding and core losses). In particular, this high-frequency resistance contribution helps to damp the filter resonance, thus improving the converter closed-loop current control stability without generating additional losses at the grid frequency, as opposed to R_f .

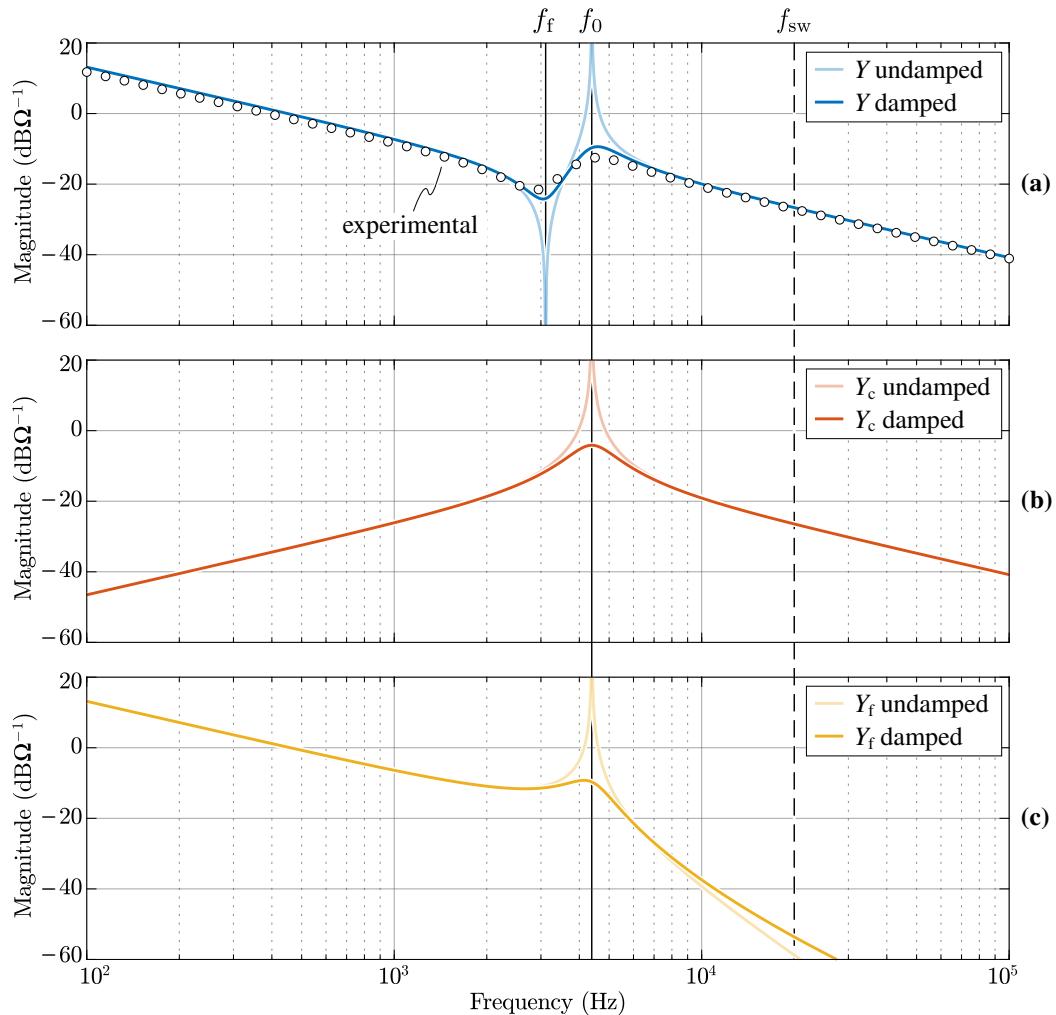


Figure 15. Analytical LCL filter transfer functions (a) Y , (b) Y_c and (c) Y_f , with and without passive damping (i.e., $R_f = 0.8 \Omega$ in the damped case). The value of Y measured experimentally is reported for comparison purposes in (a).

4.2. Filter Attenuation

The filter attenuation performance is verified experimentally by measuring the current injected into the grid and assessing its harmonic distortion.

The experimental setup consists of a grid emulator connected at the input of the LCL filter, emulating the European low-voltage grid (i.e., $U = 230 \text{ V}_{\text{RMS}}$, $f = 50 \text{ Hz}$), and an electronic load connected at the output of the DC-link, emulating the DC/DC stage of the battery charger (i.e., the load). Since the AFE is directly connected to the grid emulator, this setup emulates a stiff grid with negligible inner impedance (i.e., $\text{SCR} \approx \infty$), representing a worst case scenario from the filtering perspective.

The measurements are performed with a Teledyne LeCroy 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope, employing isolated high-voltage differential probes for voltage measurements and standard current probes for current measurements.

The experimental grid-side and converter-side current waveforms in nominal stationary conditions (i.e., $I = 61.5 \text{ A}$ and $V_{\text{dc}} = 800 \text{ V}$) are illustrated in Figure 16. The ripple attenuation provided by the LCL filter is evident, achieving a current THD of 1.2%. A slight distortion of the grid-side current is observed in proximity of the current zero crossings, as the T-type rectifier briefly enters the discontinuous conduction mode. This distortion is limited by the converter closed-loop control, which must be tuned to achieve high disturbance rejection performance [10].

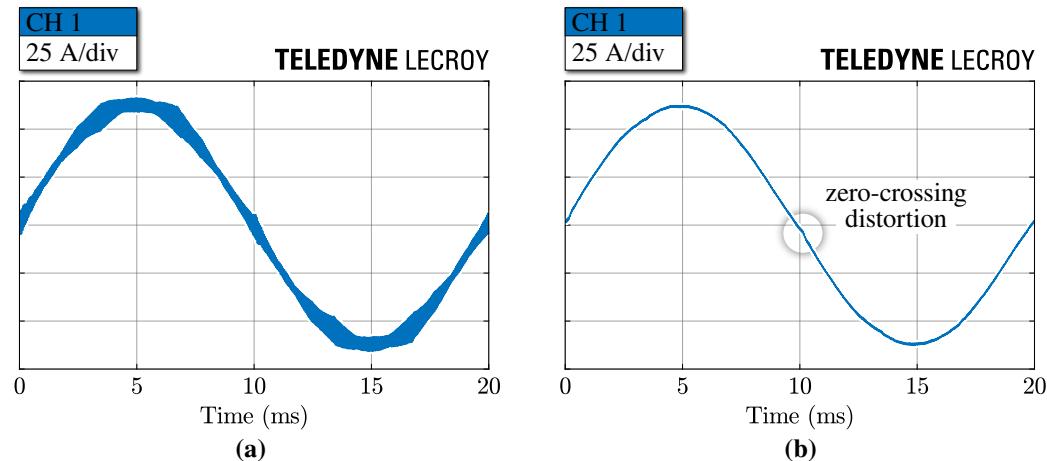


Figure 16. Experimental converter-side current i (a) and filtered grid-side current i_f (b) at $I = 61.5\text{ A}$ and $V_{dc} = 800\text{ V}$. Zero mid-point current modulation (ZMPCPWM) is adopted [20].

The filtered grid current spectrum is calculated by means of a DFT and the results are reported in Figure 17. It is observed that all harmonics comply with the IEEE 519 limits. In particular, the worst-case current harmonic at the design frequency $f_d = 19.6\text{ kHz}$ is attenuated with a 20% margin.

The slight current distortion related to the converter unidirectional operation generates several low-frequency harmonics, nevertheless they are limited by the closed-loop current control. Moreover, a group of harmonics is visible around the resonance frequency $f_0 = 4.39\text{ kHz}$, as the filter transfer function Y_f tends to amplify the local harmonics (see Figure 15c). These harmonics are effectively limited by the filter passive damping.

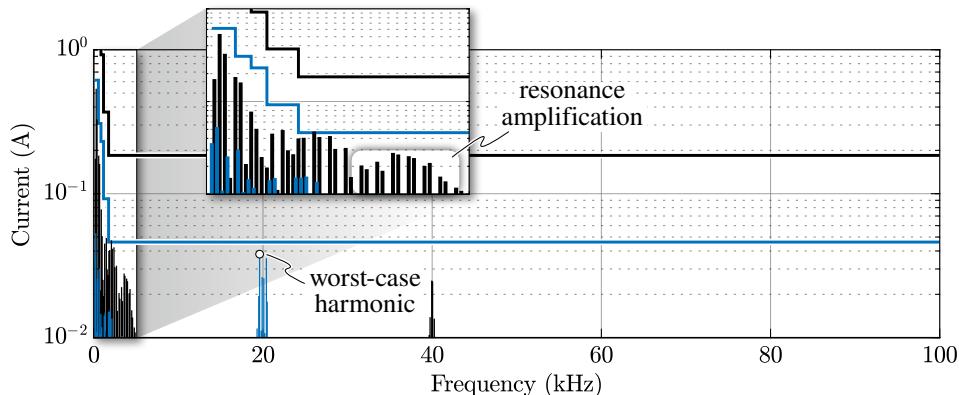


Figure 17. Experimental filtered grid-side current i_f spectrum compared with IEEE 519 odd-order (black) and even-order (blue) harmonic limits. The worst-case harmonic at the design frequency is indicated and the amplification effect around the filter resonance frequency f_0 is highlighted.

It is worth noting that with increasing grid impedance (i.e., $L_g > 0$), the high-frequency filtering results can only improve, as the filter corner frequency f_0 reduces and the asymptotic attenuation increases. Moreover, the high-frequency current harmonics are independent on the load, as they only depend on the PWM voltage harmonics. Therefore, the high-frequency (i.e., asymptotic) attenuation performance of the designed LCL filter can be considered successfully verified in all operating conditions.

The low-frequency harmonic distortion, highlighted in Figure 17, depends on the converter load and is thus analyzed further. In particular, when operating at light load, the closed-loop current control is not able to perfectly compensate the large zero-crossing distortion related to DCM operation. This phenomenon leads to higher current THD at lighter loads, as illustrated in Figure 18a. It is important to keep in mind that the LCL filter is designed to comply with the operational constraints reported in Section 3, taking advan-

tage of the AFE modular structure shown in Figure 7. Specifically, the converter modularity allows to turn-off selected modules at light load (i.e., $P_{\min} = 0.5 P$), thus ensuring the high-power operation of the remaining modules. Figure 18b shows that the current THD is limited below 5% between 20% and 100% of the nominal power (i.e., 6–30 kW), achieving acceptable distortion over the complete design operating range of the converter module.

Another quantity affected by the converter load is the power factor, as illustrated in Figure 18b, where both the displacement power factor ($\cos \varphi$) and the total power factor (PF) are shown. The relation between the two is straightforward:

$$\text{PF} = \frac{\cos \varphi}{\sqrt{1 + \text{THD}^2}} \quad (16)$$

The adopted control strategy, schematically represented in Figure 19, does not compensate for the reactive current generated by the filter capacitors, thus leading to non-unity $\cos \varphi$ operation. This feature, already taken into account during the design phase (i.e., see constraint ⑥), is directly related to the unidirectional operation of the active rectifier, which is not able to produce/absorb any significant amount of reactive power without affecting the input current distortion. Additionally, in this case, the adopted modular structure allows to maintain high power factor values at light load by turning off selected modules and ensuring the high-power operation of the remaining modules. Overall, Figure 18b shows that the total power factor stays above 0.995 between 40% and 100% of the nominal power (i.e., 12–30 kW), thus complying with the design restriction ⑥.

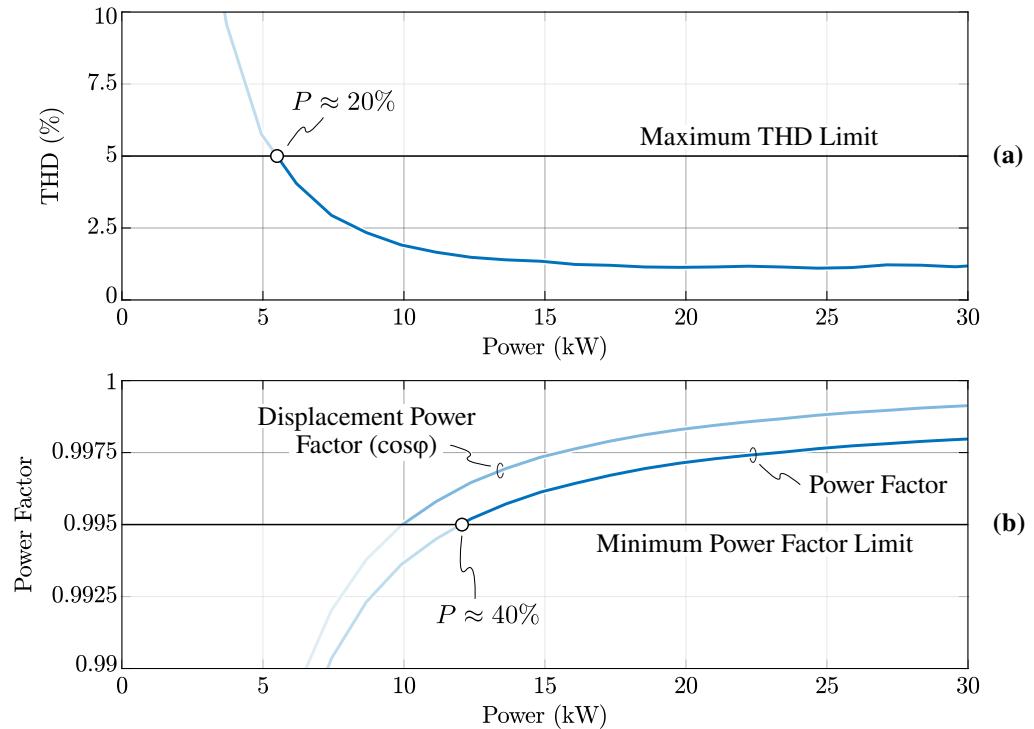


Figure 18. Experimentally measured grid-side current total harmonic distortion (THD) (a) and power factor (b) as functions of the transferred power. The maximum THD limit and the minimum power factor requirement are indicated.

4.3. Converter Control Stability and Dynamic Response

The performance of the converter closed loop control is assessed experimentally with the hardware setup previously described. A conventional voltage-oriented control scheme is adopted [10,22,23,30] and is schematically illustrated in Figure 19.

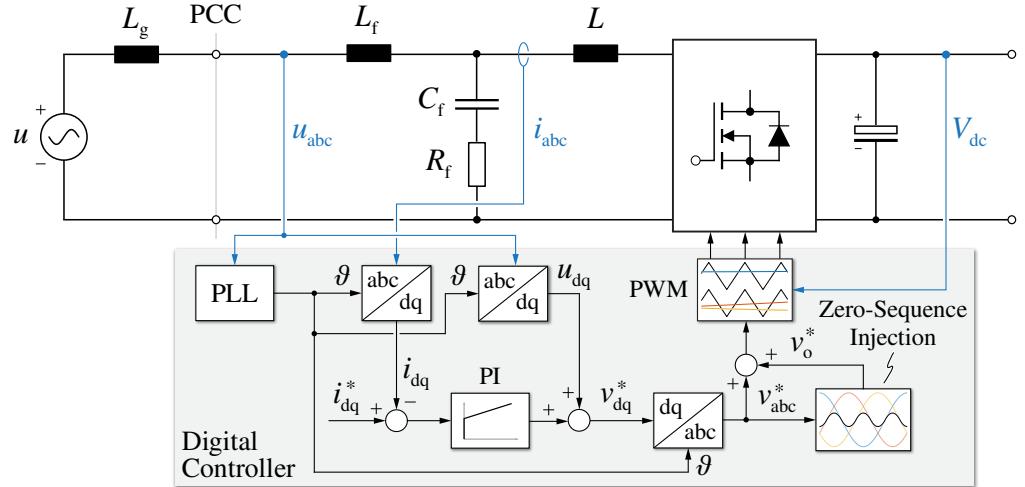


Figure 19. Simplified overview of the converter closed-loop current control: the digital controller schematic is highlighted in grey.

The rotating dq frame is exploited to obtain zero stationary error with a simple PI controller. The PCC voltages are measured to achieve the reference frame synchronization with the grid, which is performed by a phase locked loop (PLL). These voltages are passed through a resonant filter (i.e., the PLL itself) and are then fed forward in the current control loop, to unburden the integral part of the PI regulator. The digital sampling and update process is performed once per switching period ($f_s = f_{sw} = 20\text{ kHz}$), however the current feedback values are obtained by means of oversampling (32 samples per switching period) and averaging, in order to improve the measurement reliability and thus the control performance around the current zero-crossings. In fact, conventional sampling does not yield the correct average current value when discontinuous conduction mode is encountered [60], thus inhibiting the accuracy of the current control and leading to increased low-frequency distortion.

The digital implementation of the control introduces three main delay components, which reduce the achievable control bandwidth and/or decrease the closed-loop stability margin [23]. The first delay contribution is directly related to the digital processing, which generates one sampling period delay ($T_s = 1/f_s$) between the measured quantities and the control signal output. The second component is linked to the PWM modulator, which introduces a zero-order hold (ZOH) effect with a T_s duration. Finally, the last contribution derives from the current oversampling and averaging process, which results in a moving-average delay of $T_s/2$. The complete dq current control block diagram is illustrated in Figure 20.

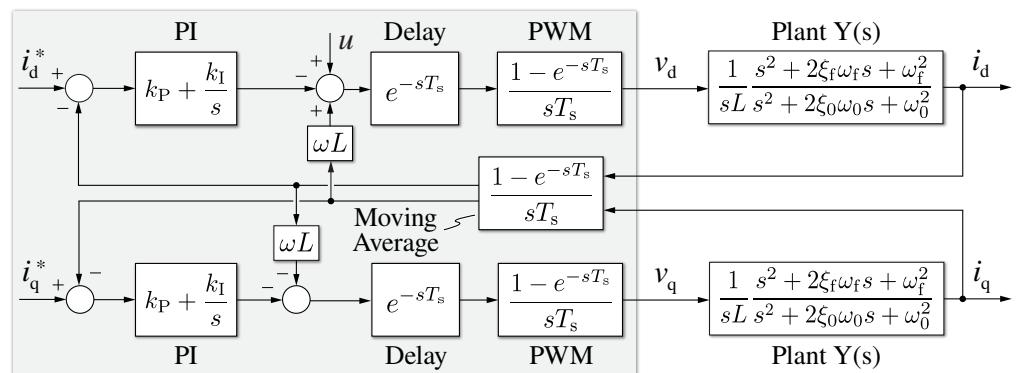


Figure 20. Complete block diagram of the i_d and i_q current control loops [10], including the plant transfer function $Y(s)$.

Since the LCL filter transfer function Y behaves as a pure inductance (i.e., $L_{\text{tot}} = L + L_f + L_g$) up until the first resonance frequency f_f (see Figure 4a), the current control tuning can be performed in a conventional way. The PI regulator is tuned to achieve a 60° phase margin [10], setting the open-loop cross-over frequency f_c to 850 Hz and positioning the PI zero five times lower ($f_z = f_c/5$) to achieve good disturbance rejection capabilities. Since the grid inductance L_g is not known in general, the tuning is performed as

$$\begin{cases} k_P = 2\pi f_c (L + L_f) \\ k_I = 2\pi f_z k_P \end{cases} . \quad (17)$$

The current control open-loop transfer function is derived analytically and its magnitude and phase Bode plots are illustrated in Figure 21, for different values of grid inductance L_g . Three situations are considered, namely an infinitely stiff grid ($L_g = 0 \text{ pu}$, SCR = ∞), a typical grid for an EV fast charging connection ($L_g = 0.01 \text{ pu}$, SCR = 100) and a reasonably weak grid ($L_g = 0.05 \text{ pu}$, SCR = 20).

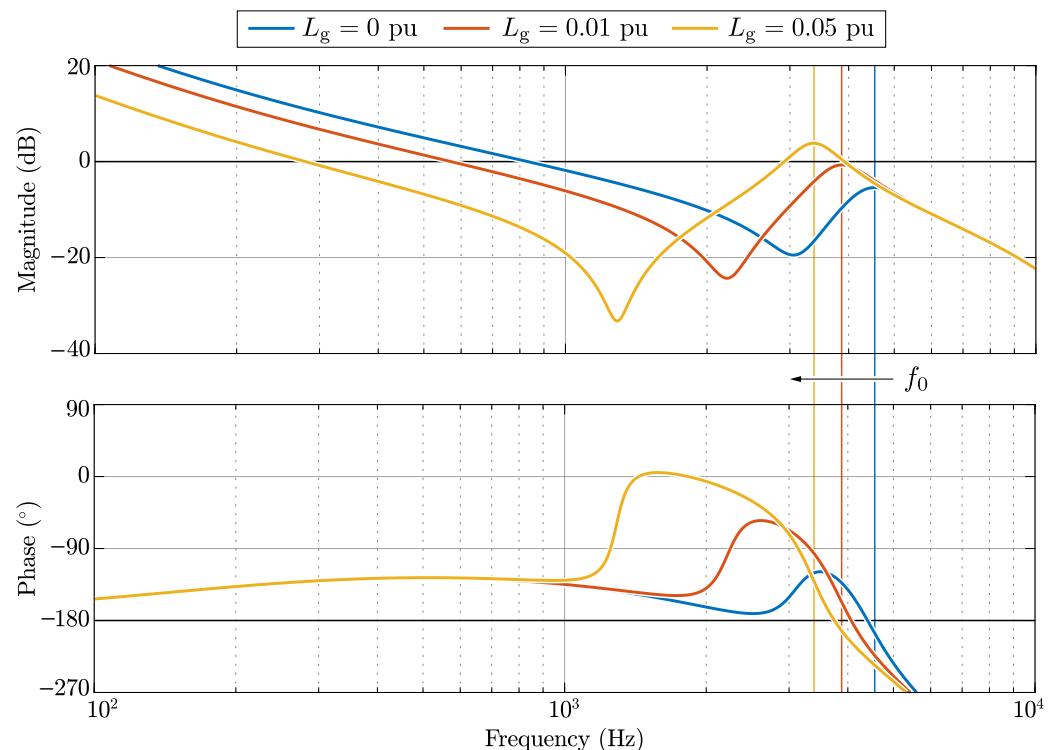


Figure 21. Bode plots of the analytical i_d and i_q compensated loop gains for different values of grid inductance L_g . The PI controllers are tuned according to (17).

In general, to achieve the closed-loop current control stability, the magnitude of the open-loop system transfer function has to be lower than 0 dB when its phase crosses -180° (Nyquist criterion) [25]. From Figure 21 it is observed that the system gain margin decreases for higher values of L_g (i.e., lower SCR), as the system resonance frequency f_0 reduces and the peak magnitude increases. Theoretically, the stability limit is reached around $L_g \approx 0.05 \text{ pu}$ ($\text{SCR} \approx 20$). Figure 21 also shows that a larger L_g simultaneously reduces the converter bandwidth and the distance between f_c and f_z , thus decreasing the low-frequency phase margin and leading to a more nervous control response.

To experimentally verify the closed-loop control stability, the converter response to a reference current step is tested. Different values of grid inductance are emulated by inserting three-phase power inductors between the converter and the grid emulator, approximately achieving $L_g = 0 \text{ pu}$ (i.e., no inductor), $L_g \approx 0.01 \text{ pu}$ and $L_g \approx 0.05 \text{ pu}$.

The results of the tests are illustrated in Figure 22, where the reference step response of both the converter-side current i and the grid-side current i_f are reported. It is observed that the control loop is stable in all conditions, however the converter-side current shows a damped high-frequency oscillation for large values of L_g .

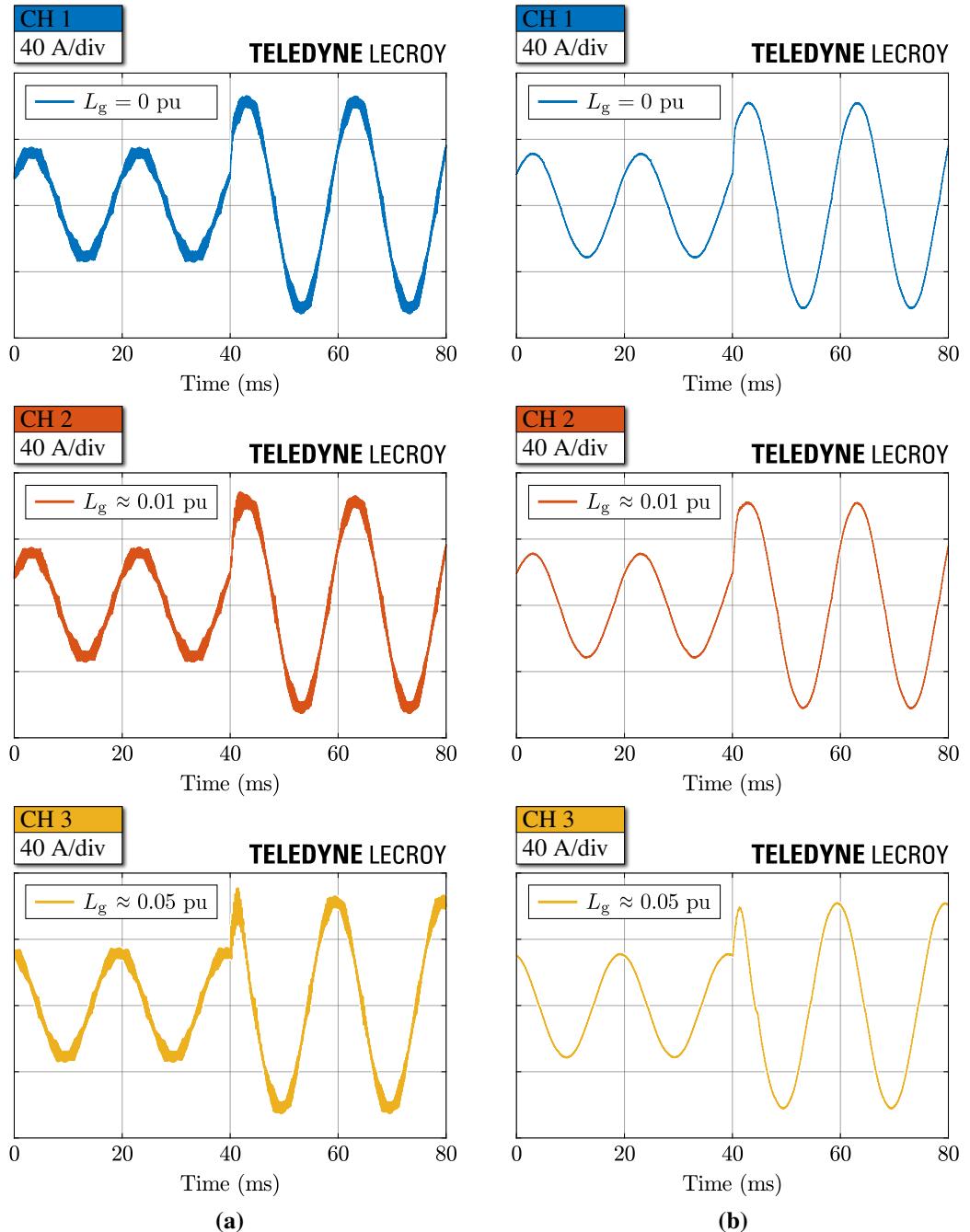


Figure 22. Experimental current control loop step response between 50% and 100% load for different values of grid inductance L_g : (a) converter-side current i and (b) grid-side current i_f .

This is better highlighted in Figure 23, where the step response of the converter-side currents is reported on the d-axis of the rotating dq frame. The value of i_d is obtained from the digital-to-analog converter (DAC) of the microcontroller unit (MCU), therefore it is discretized in time (i.e., with a T_s periodicity) and is characterized by a large noise content. Figure 23 shows that higher grid inductance values cause at the same time a slower response (i.e., lower bandwidth), a higher overshoot (i.e., lower phase margin) and

an increased high-frequency oscillation (i.e., lower gain margin at the phase cross-over frequency). All of these aspects could already be observed from the open-loop control transfer functions analysis previously reported (see Figure 21), nevertheless they have been verified experimentally.

The current reference step responses reported in Figure 23 show that the stability margin is still not reached for $L_g = 0.05 \text{ pu}$, as expected instead from the small-signal transfer function analysis. This is mainly due to the unmodeled AC resistance components of the system, which increase the damping of the resonance peaks (see Figure 15a) and thus lead to a wider control stability range.

In conclusion, the closed-loop current control stability is achieved for all grid SCR values up to 20 (i.e., weak grid connection). Therefore, the proposed LCL filter design and optimization procedure can be considered successfully validated.

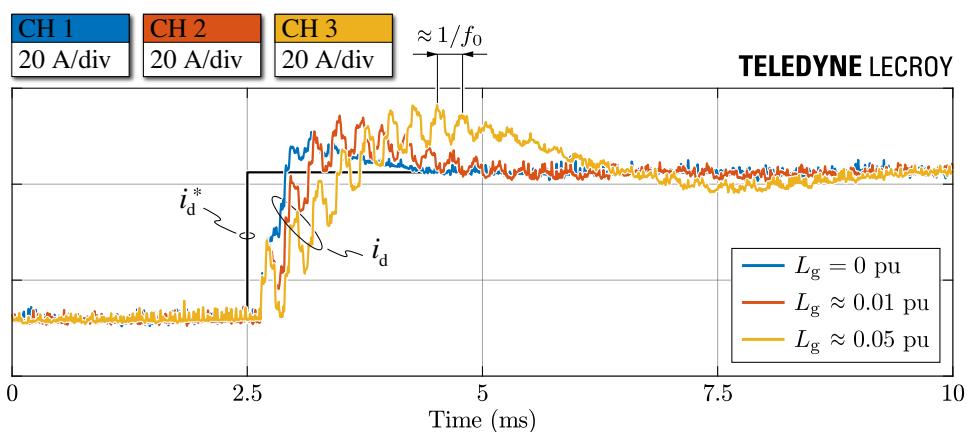


Figure 23. Experimental d-axis current control loop step response between 50% and 100% load for different values of grid inductance. The value of i_d is obtained from the DAC of the MCU (i.e., as a voltage value between 0 and 3.3 V) and then rescaled, thus showing a high amount of noise.

5. Conclusions

This work has presented a complete analysis, design and optimization procedure of a three-phase LCL filter for the active front-end unit of a modular EV ultra-fast battery charger. The proposed novel design methodology is based on the graphical representation of the filter design space in the (C_f, L_{tot}) plane. By translating the constraints on the filter parameters into analytical equations, the design space boundaries are identified and the LCL filter design minimizing the total required inductance (i.e., optimizing the filter size/loss trade off) can be selected.

This design procedure has been applied to the AC-side filter of a 30 kW, 20 kHz T-type unidirectional rectifier for ultra-fast charging applications. The functionality of the selected optimal LCL filter has been first verified in simulation, by checking the filter transfer functions and their effect on the current harmonic attenuation and the system stability. In particular, the LCL filter impedance (seen from the converter side) has been experimentally measured, showing an accurate matching with the analytical expectations and thus providing a preliminary validation of the attenuation capabilities of the filter. Then, the LCL filter has been tested together with an active rectifier prototype, to verify both the filter attenuation performance and the converter closed-loop current control stability. The current spectrum at full load has been shown to comply with the international technical standards, achieving results well within the prescribed limits, both for even and odd harmonics. The system stability has been finally verified with different values of grid impedance, emulating various grid point connections. Therefore, the proposed novel design methodology has been successfully validated.

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