

## Introduction

STM32H573VIT6 is the MCU selected.

## High speed crystal oscillator

Evaluation kit has the following circuit.

### EXTERNAL HSE CLK (OPTIONAL)

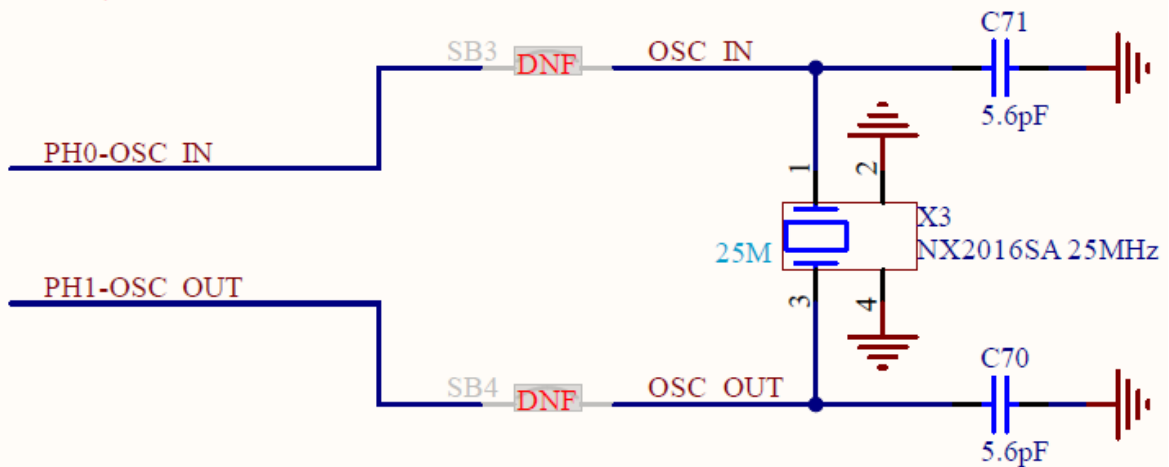


Figure 1: NUCLEO-H563ZI development board for STM32H563ZIT6 MCU

Acceptable external clock frequency range for the MCU is 4 to 50 MHz.

Typical circuit is suggested by the ST Application Note AN5711.

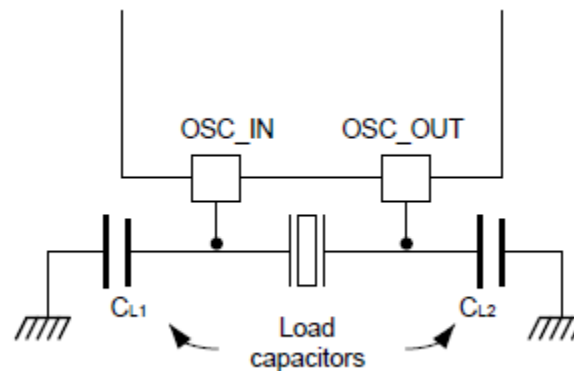


Figure 2: Typical application schematic

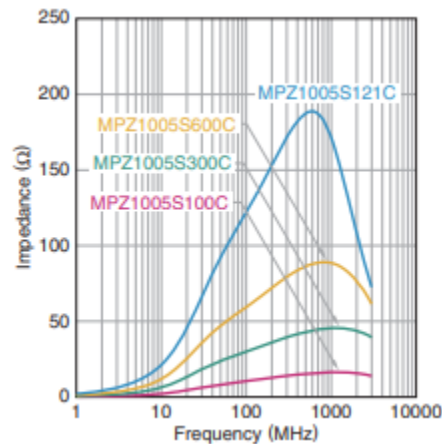
Datasheet suggests 10pF as PCB and MCU parasitic capacitance. This seems much and 6pF is used as approximation. Equation  $C1=C2=2 * (CL - Cstray)$  is used and it gives  $C1=C2=8pF$ . Closest nominal is 8,2pF.

ECS-250-10-37B-CTN-TR was selected from Krakul component library. It's a 25MHz  $\pm 10ppm$  10pF crystal.

## Power supply

VDD – Supply for I/O-s, internal regulator, reset, power management and internal clocks. 1.71 V – 3.6 V.

VDDA – Supply for ADC, DAC. Will be connected to 3,3V trough a ferrite bead.



MPZ1005S121C is selected from Krakul library. Little effect is to be expected against regulator switching noise, but should reduce the RMII effect.

VDDUSB – USB supply 3.0 to 3.6V. Connect to VDD if not used.

VCAP1 and VCAP2 – 1.0 V – 1.2V. Digital core domain supply. Uses internal voltage regulator.



## ADC

Figure 56. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function

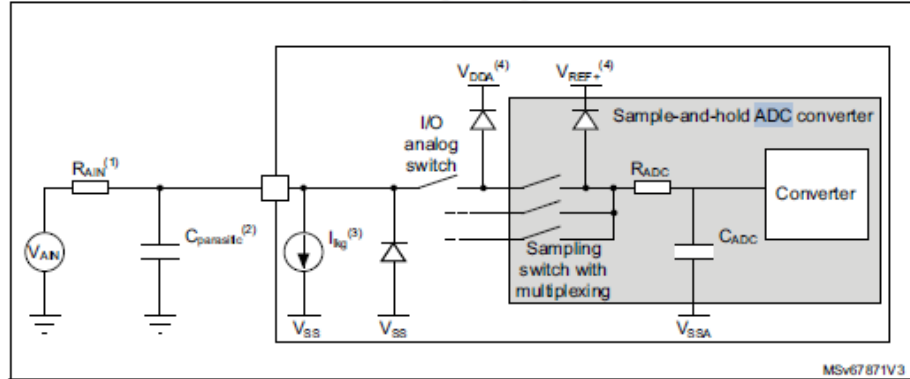


Figure 4: ADC input

Due to limited number of ADC inputs on the STM32H573VIT6 analog multiplexers are used. There are 2 8 channel MUX that are controlled with digital pins. One MUX is for power output current measurement and the other is for power output voltage measurement.

TMUX1208PWR is selected for it's price.

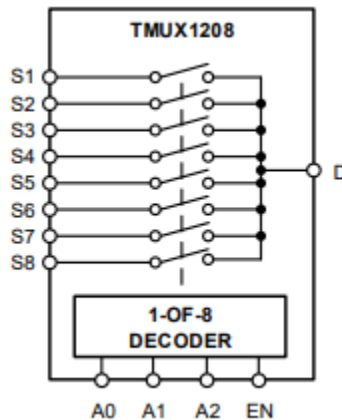
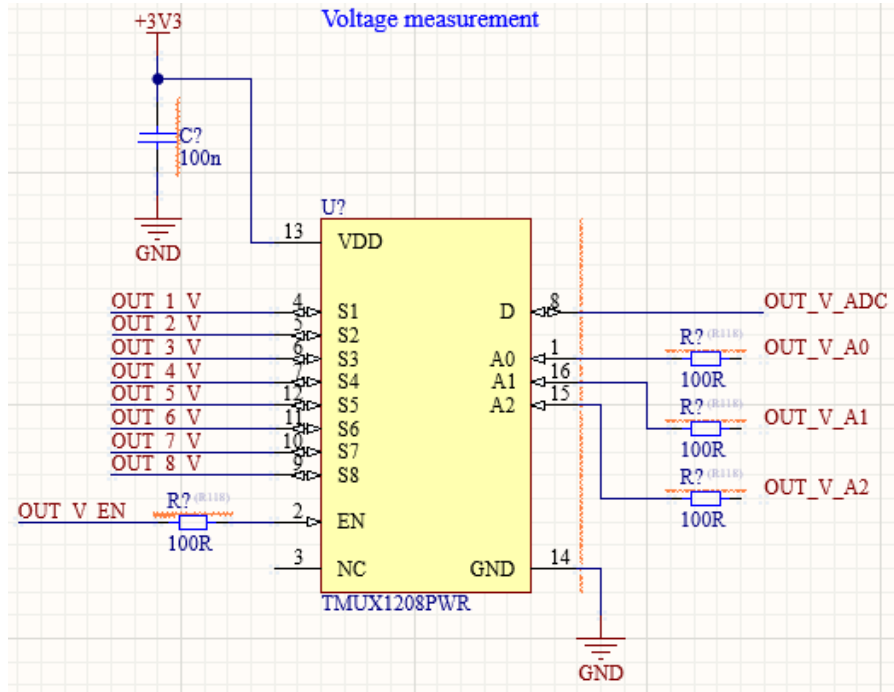


Figure 5: TMUX1208 internal diagram

Besides decoupling capacitor other external components are not mandatory, but 100Ω resistors will be added to encoding and enable pins.



ADC input on the MCU shall not have the usual capacitor that can be used to mitigate the voltage drop created by sample and hold circuit. Extra capacitance on the trace from MUX to MCU creates a need to wait longer until the voltage at ADC stabilizes.

Instead the capacitors will be at the MUX inputs and the trace capacitance from MUX to MCU is kept minimum. This way 100nF capacitors before the MUX will force the ADC input to correct voltage relatively faster. The internal sample and hold capacitor inside this MCU is typically 3pF. Trace parasitic capacitance is likely order of magnitude greater.

## Configuration switch

To set HW mode for the MCU 8 bit dip switch is added.

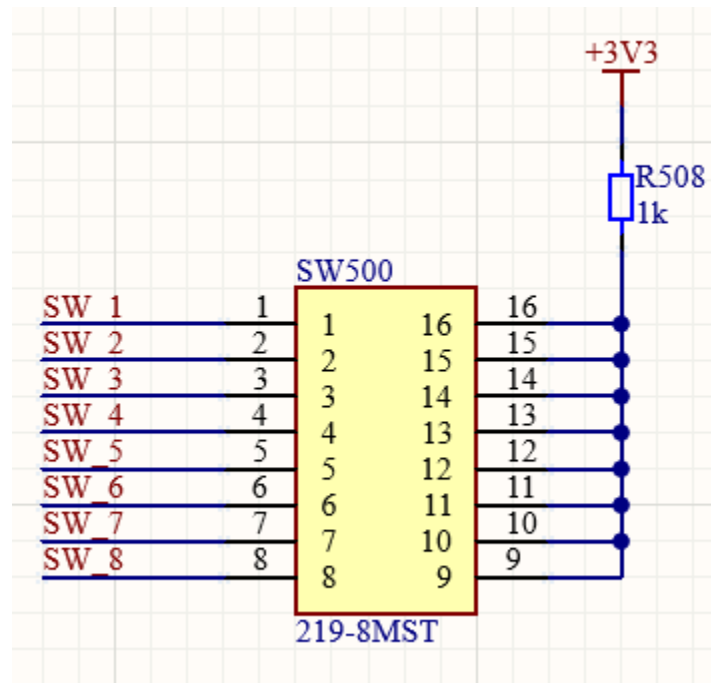


Figure 6: HW configuration switch.

Switch functions TBD.

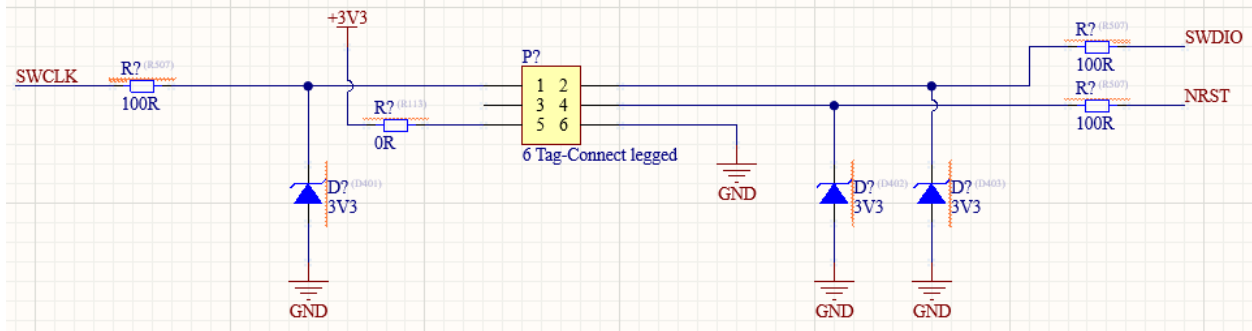
## Programming interface

Serial wire debug (SWD) will be used for firmware download and debugging. It has following signals.

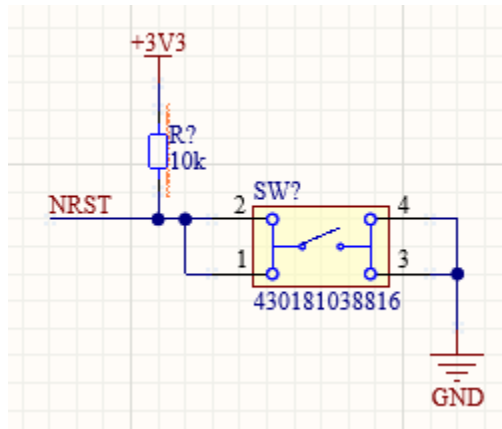
SWD pin	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	Input/Output	Serial-wire data input/output	PA13
SWCLK	Input	Serial-wire clock	PA14

6 pin Tag connect with clamping legs will be used. SWD and reset signals have 100R series resistors and TVS diodes for short circuit and ESD protection.

3.3V connection has a series 0R resistor that can be removed if necessary.



Reset button.



The button is for resetting the MCU manually during development phase.