Introduction

The voltage of each switchable power output must be measured. Also, the input voltage must be measured for reference.
Nominal input voltage range is 24V - 32V. Some overhead should be included.
Accuracy requirement: 0,1% of minimum 24V.

Maximum voltage allowed on MCU pin is 4V.

Circuit

Voltage divider shall be used. MCU VREF+ will be connected to +3,3V. 1:11 voltage divider is used.
To protect the MCU pin from overvoltage rail-to-rail clamping diodes are used. BAT6404WH6327XTSA1 is used. It's two diodes SOT323 package.

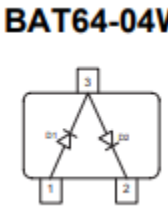

Figure 1: Clamping diodes

The forward voltage drop of this diode is below 0,7V throughout its temperature range for currents under 100mA.

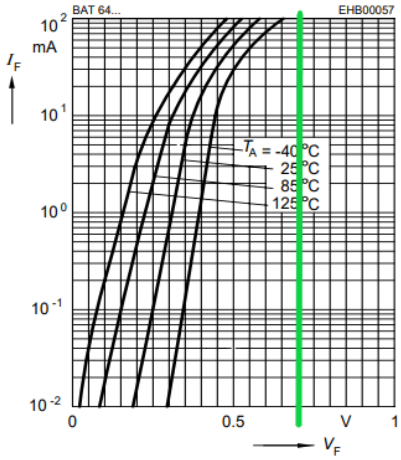

Figure 2: BAT64 forward voltage drop

10kΩ and 1k resistors shall be used for the voltage divider. Even with 60V at the divider input the current trough the diode is limited to ~ 6mA. Higher than nominal voltage levels are likely temporary in nature. A result of sudden load changes, ESD or caused by inductive loads.

ESD is the most dangerous situation and it is modelled with LTSpice. IEC61000_4_2 test with 8kV level is modelled on simplified circuit.

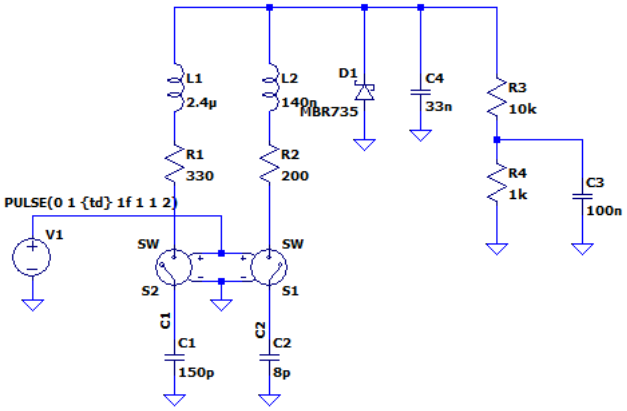

Figure 3: ESD simulation circuit

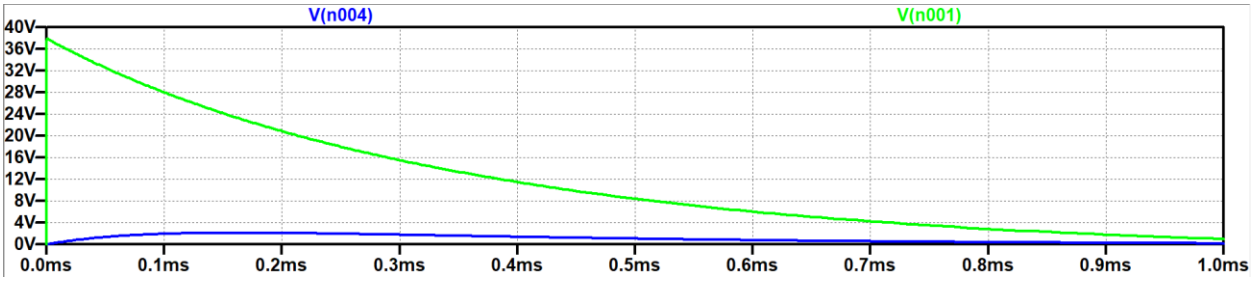

Figure 4: Simulation results.

Green is the voltage at the circuit input. Blue is the voltage on C3 after the voltage divider. This is what MCU pin would see if it had infinite input resistance. Simulation shows voltage in safe limits.

Simulation reveals that 33nF capacitor is needed at the power output. This limits the voltage that the voltage divider resistors see to safe level. ESD strike can damage thick film resistors and increase their resistance. This would result in false voltage measurement readings. The 33nF 0805 MLCC prevents that by absorbing discharge energy.

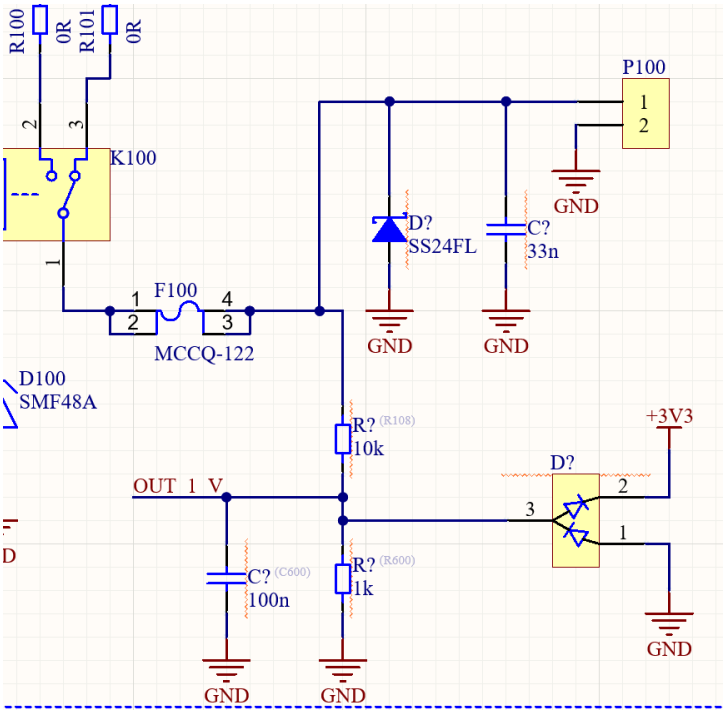

Figure 5: Voltage measurement schematic