1. Introduction

Testing temperatures
Min: -20°C
Max: 65°C
Nominal: 23°C

Testing voltages
Nominal: 24V
Maximum: 32V

2. Ethernet functional test

Firmware hash used for testing: 41b55d6e799b3fa55f30f365ebfebcce77e4a8eb
Ethernet was tested using a loopback configuration, where two Fuseboard UDP sockets were used to ping-pong an incrementing number over the loopback cable. UDP was chosen as it does not have any error correction. Error criteria: A socket receives a corrupt UDP packet, or the packet does not contain the valid value.

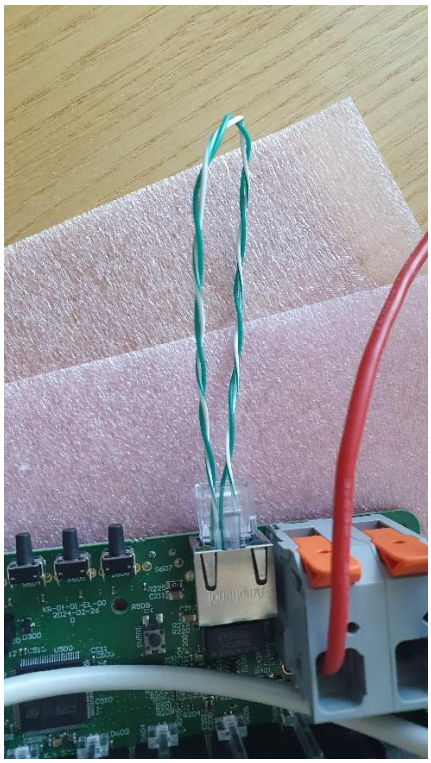

Figure 1: Loopback cable for ethernet test

Result: Pass
5,000,000 UDP packets were transmitted without errors detected.

3. RS485 interface functional test

Firmware hash used for testing: 2acab3907d81a91c5c4b2a2d4f8e2ccd2a1c625f

RS485 interface was tested using a PC script and USB to RS-485 dongle. A string was transmitted back and forth between the fuseboard and PC script in half-duplex mode 20,000 times (~1MiB data). Error criteria: fuseboard/PC reception timeout, or an incomplete string is received.

Result: Pass with notes

If a sufficient response delay* (between receiving a packet from fuseboard, and sending a packet to fuseboard) exists, then all data is transmitted without errors.

- 3ms delay*: ~35% of the strings received by fuseboard were incomplete;
- 5ms delay*: ~3% of the strings received by fuseboard were incomplete;
- 7ms delay*: 0% of the strings received by fuseboard were incomplete;

4. Reverse polarity protection test

Current hardware architecture does not survive error where main power is connected in reverse.

5. 5V SMPS

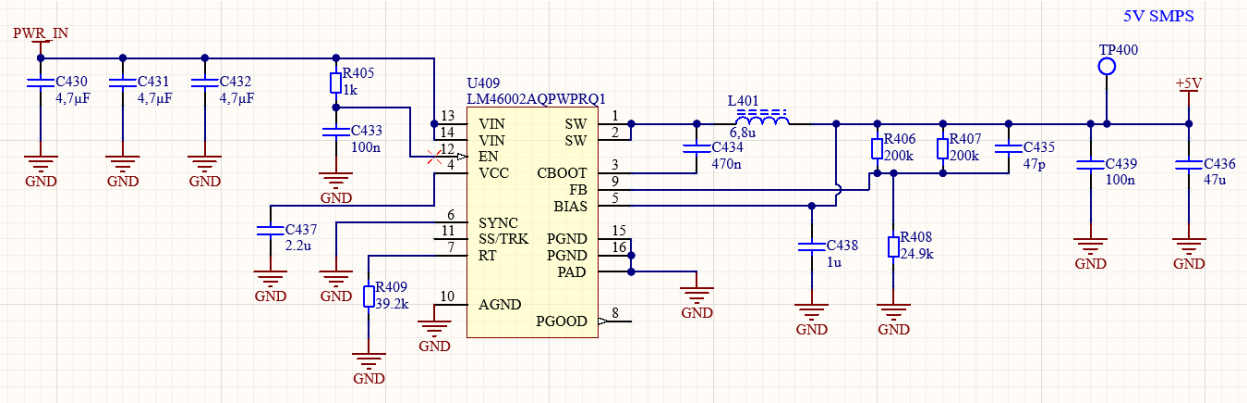

Figure 2: 5V SMPS under test

Regulator loads are removed by cutting traces on locations marked with blue lines. Electronic load is connected at the point of blue circle. Resistor R410 will not be removed. It supplies relay coils and those will not be activated.

Fuse board V0 prototype P03 was used for 5V SMPS testing.

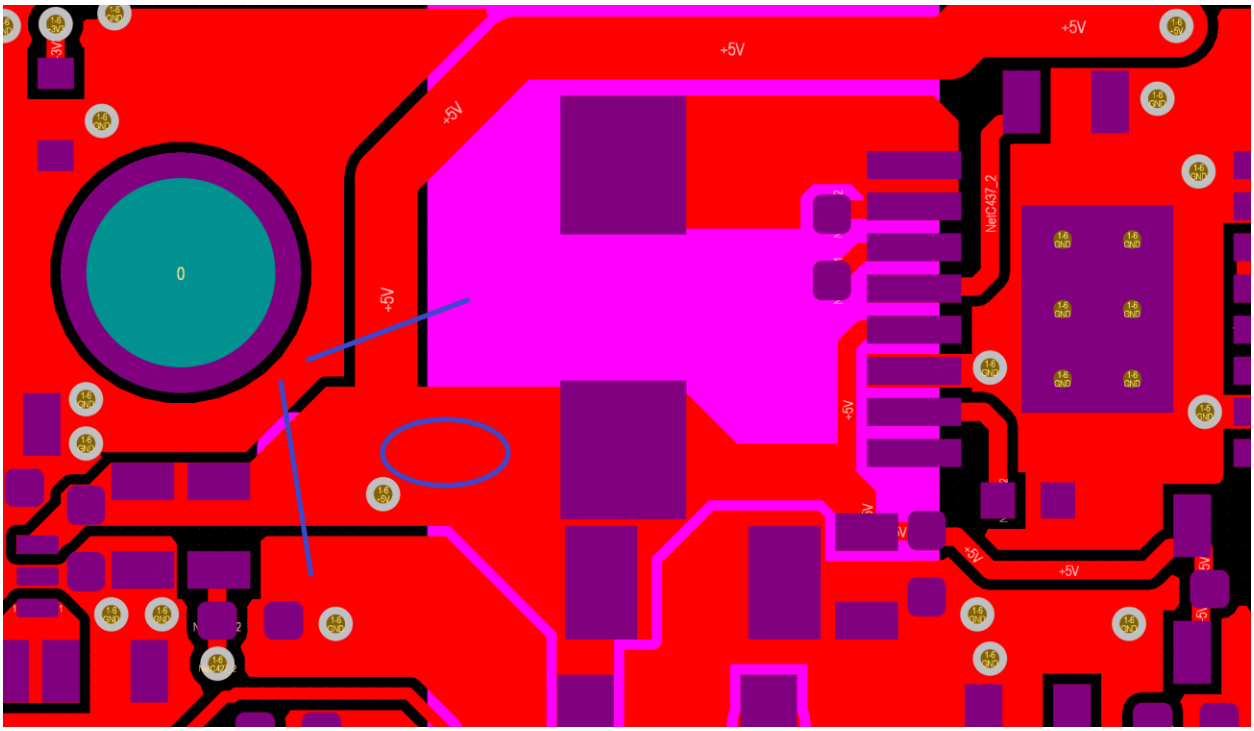

Figure 3: Modifications to PCB for 5V SMPS testing

Figure 4: 5V SMPS test setup

5V SMPS was tested on V0 prototype. The regulator is designed for 1,04A, but tested with 1,5A as well.

5.1. General reliability

Heat dissipation.
Vin = 28V.
Iload = 1,5A.
Time under load was 1,5h.
Room temperature was 24 °C.
Regulator temperature was 48.8 °C

Heat soak.
Ambient temperature was 60 °C.
Time at the ambient temperature was 16h.
Load was 1,5A.
Vin was 32A.
No difference in performance was noted after time on maximum operating temperature.

5.2. Constant load

See results in Table 1. Oscilloscope was set to 20MHz bandwidth.

Table 1: 5V SMPS static load test results

		Input voltage					
		24 V		28 V		32 V	
Temperature [°C]	Load [A]	Vout [V]	Ripple [mVp-p]	Vout [V]	Ripple [mVp-p]	Vout [V]	Ripple [mVp-p]
	0	5,138	20	5,142	23,6	5,141	24,4
	0,1	5,085	21,2	5,102	24	5,109	24,4
	0,5	5,077	26,8	5,077	26,4	5,078	23,6
	1	5,078	47,2	5,078	46,4	5,078	43,6
-20	1,5	5,078	67,2	5,077	64	5,077	62,4
	0	5,138	18	5,138	20,8	5,14	19,6
	0,1	5,08	30,04	5,099	20,8	5,107	20,8
	0,5	5,067	25,2	5,068	28,4	5,068	26,8
	1	5,066	46	5,066	45,2	5,066	44,8
24	1,5	5,064	68,4	5,064	66	5,064	69,2
	0	5,147	17,6	5,146	21,6	5,147	22
	0,1	5,088	27,6	5,104	23,6	5,114	22
	0,5	5,074	30	5,073	29,2	5,073	28,8
	1	5,076	54,8	5,075	50	5,076	55,2
60	1,5	5,078	78,4	5,078	75,6	5,081	77,6

Result: Voltage to load dependence causes output voltage change that's under 2%. This will not result in negative effects to system performance. Test is passed

5.3. Load step

Load was stepped from 0,25A to 1,25A and back to 0,25A. Test was performed with 28V input voltage at -20 °C, 24 °C and 60 °C.

Electronic load was used to create the load curve.

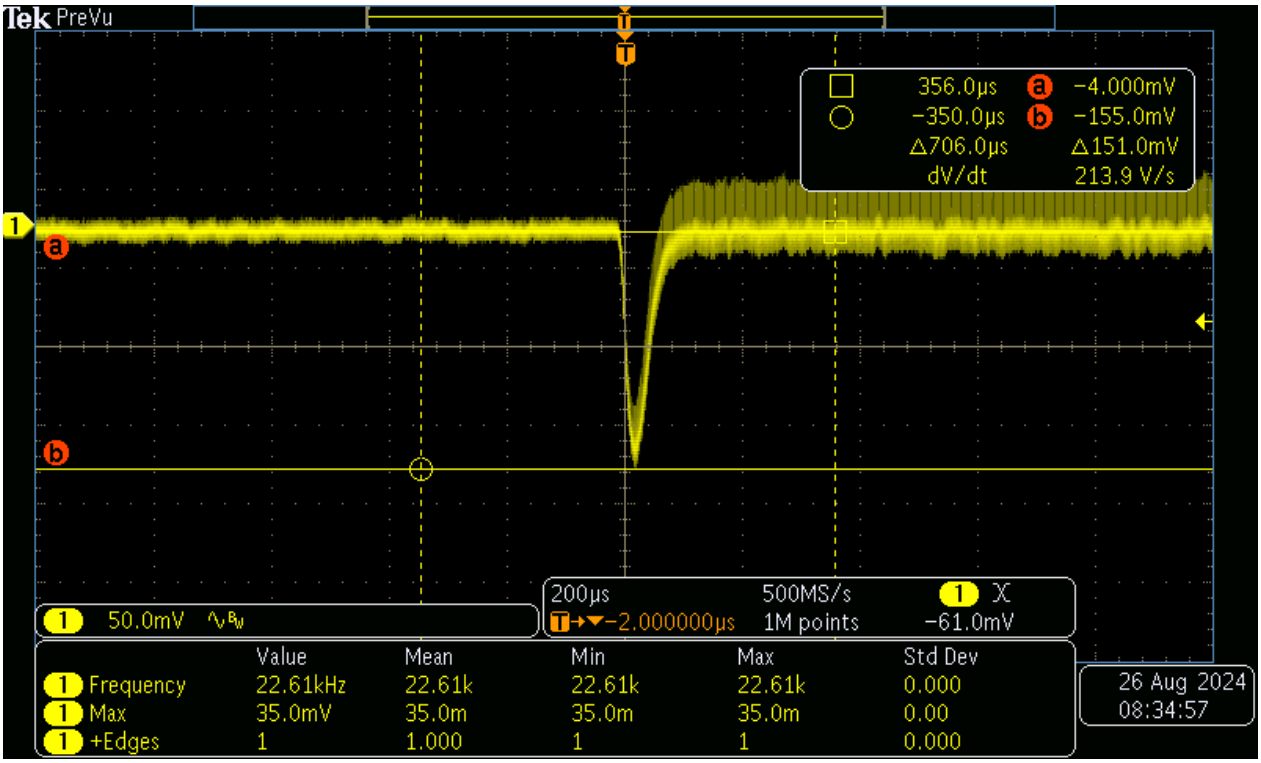

Figure 5: - 20 °C Low to high load

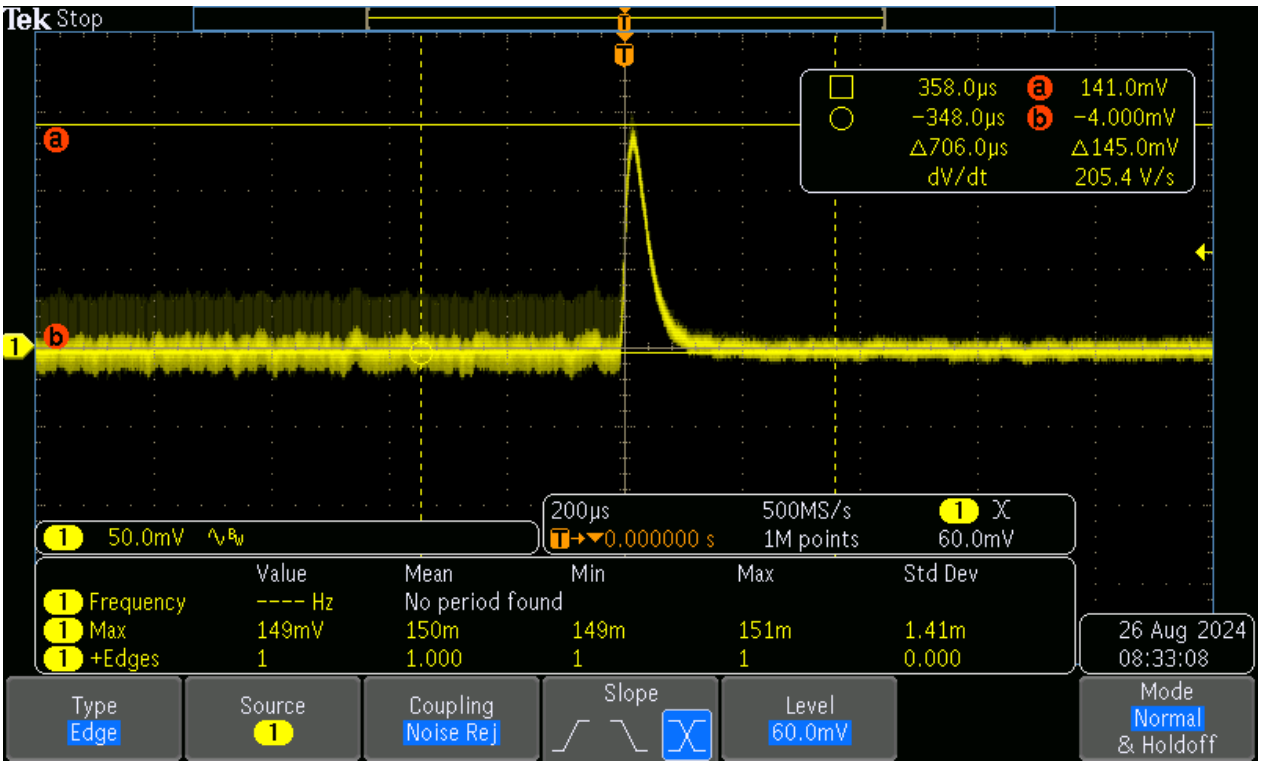

Figure 6: -20 °C High to low load

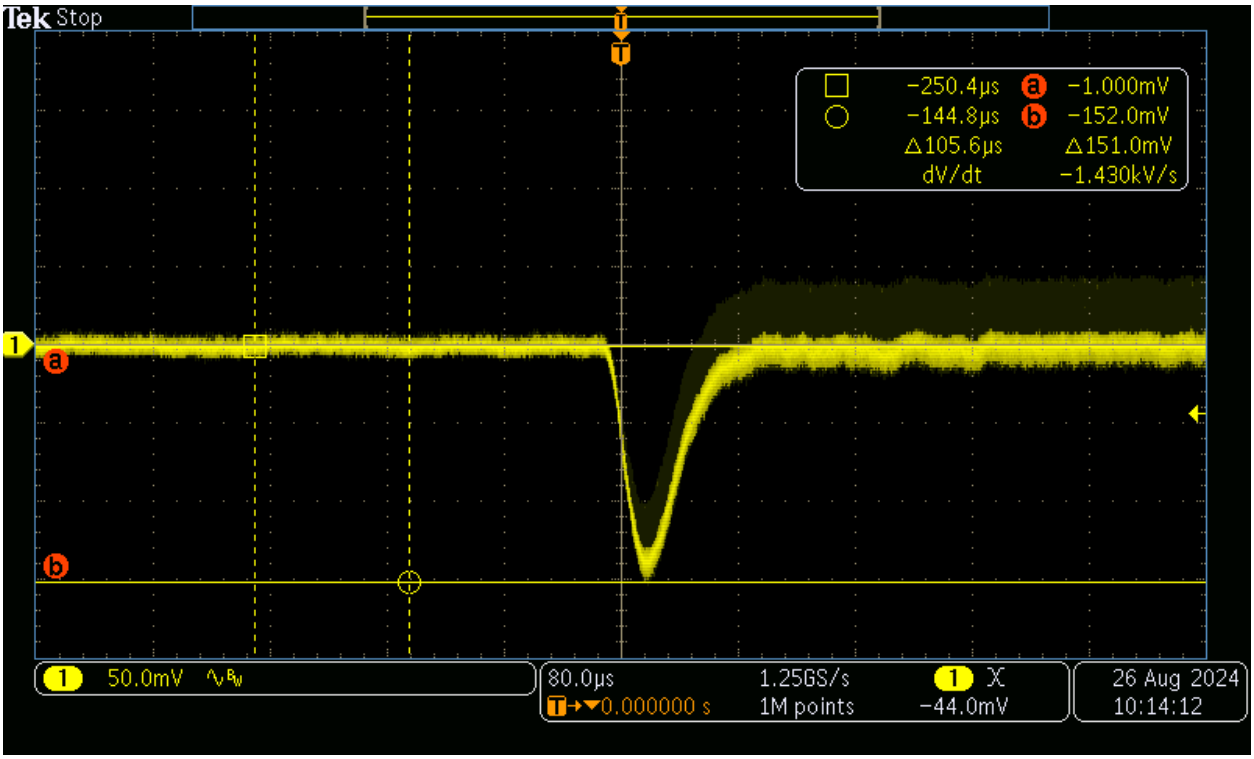

Figure 7: 24 °C Low to high load

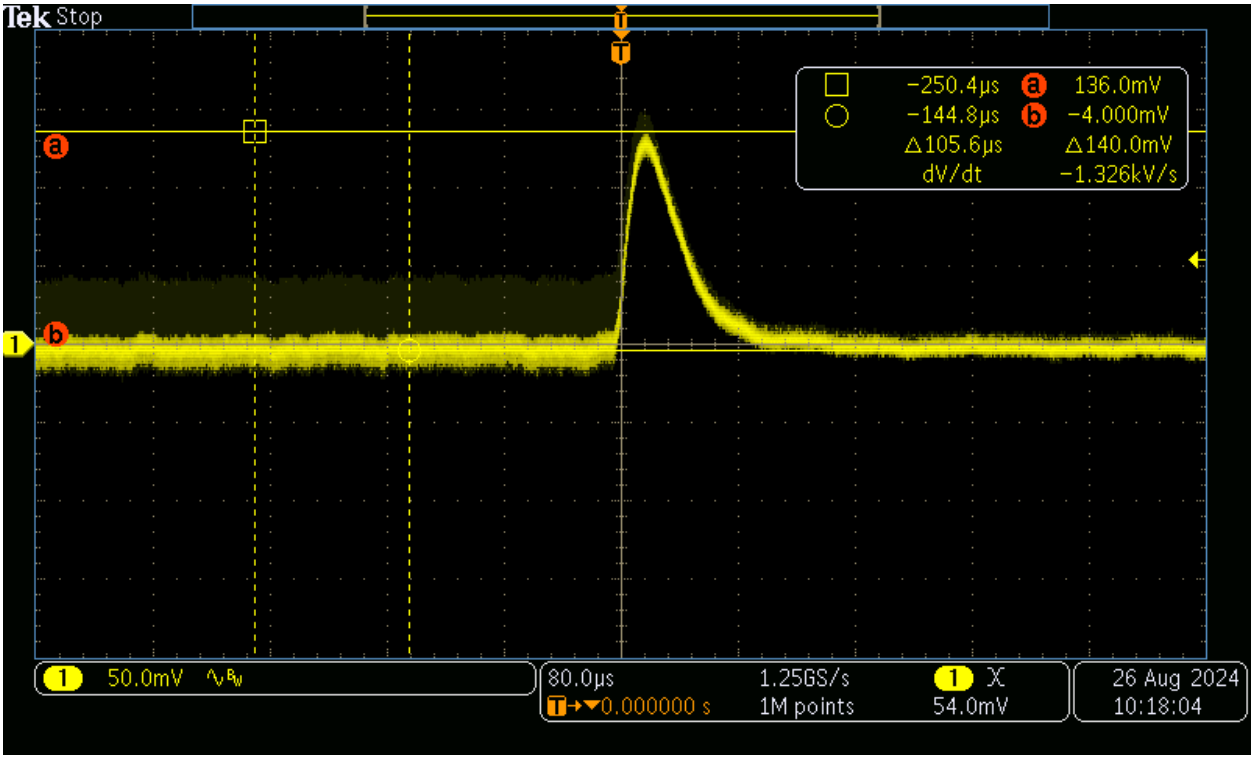

Figure 8: 24 °C High to low load

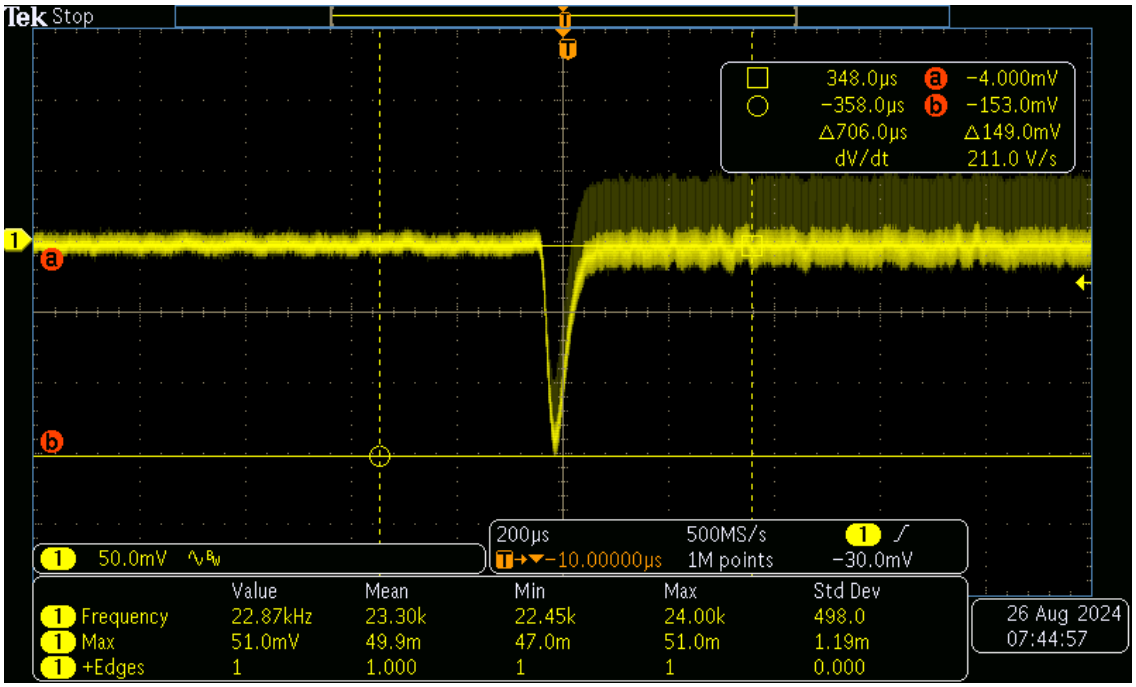

Figure 9: 60 °C Low to high load

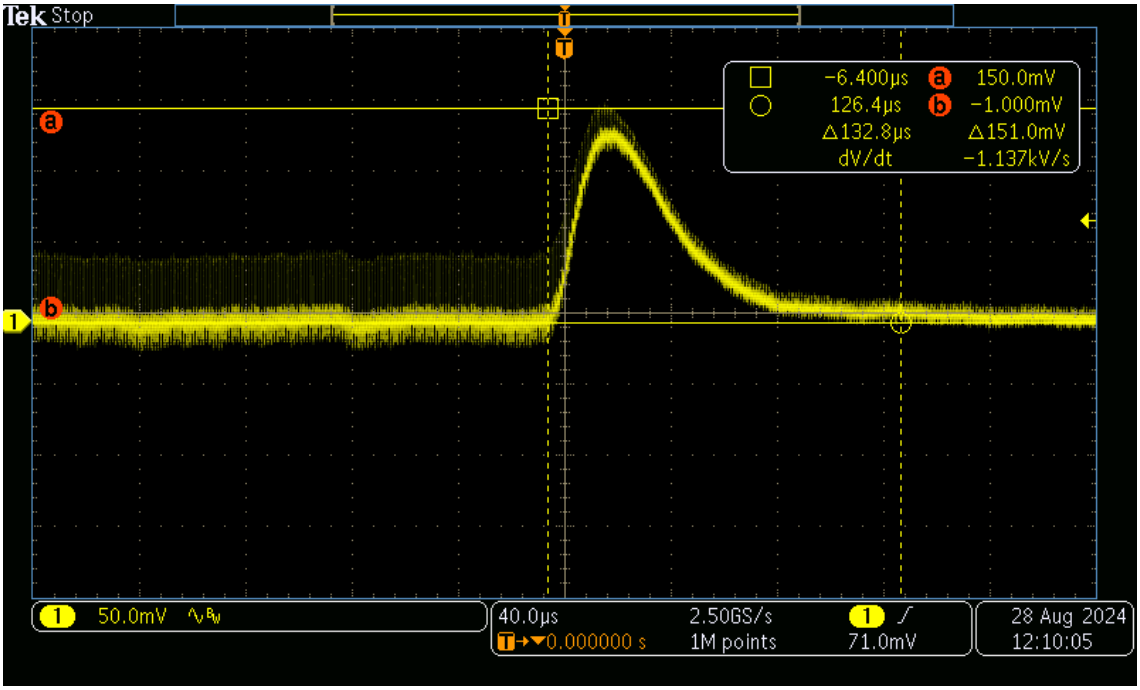

Figure 10: 60 °C High to low load

Result: Sudden change in regulator load causes a voltage deviation around 3% from nominal output voltage. This will not cause negative effects in systems supplied by this regulator. It's shown that the regulator is stable as there is no ringing while the voltage is settling. Test is passed

5.4. Startup under load

It was noted during tests, that if the regulator is loaded before regulation voltage is achieved it may not reach the target voltage. However once regulation voltage is achieved no problem with loading is detected. It's believed that the behavior is caused by the overload protection system reacting to large initial current. It regulates the current down to prevent damage to the regulator IC causing the regulator fall short of the target output current.

In order to make sure the system startup is not negatively effected the following test was performed. All regular system loads were re-attached and additional 10Ω (0,5A) was added to the 5V supply rail. Test was repeated at -20 °C, 24 °C and 60 °C. 3,3V power rail is also monitored.

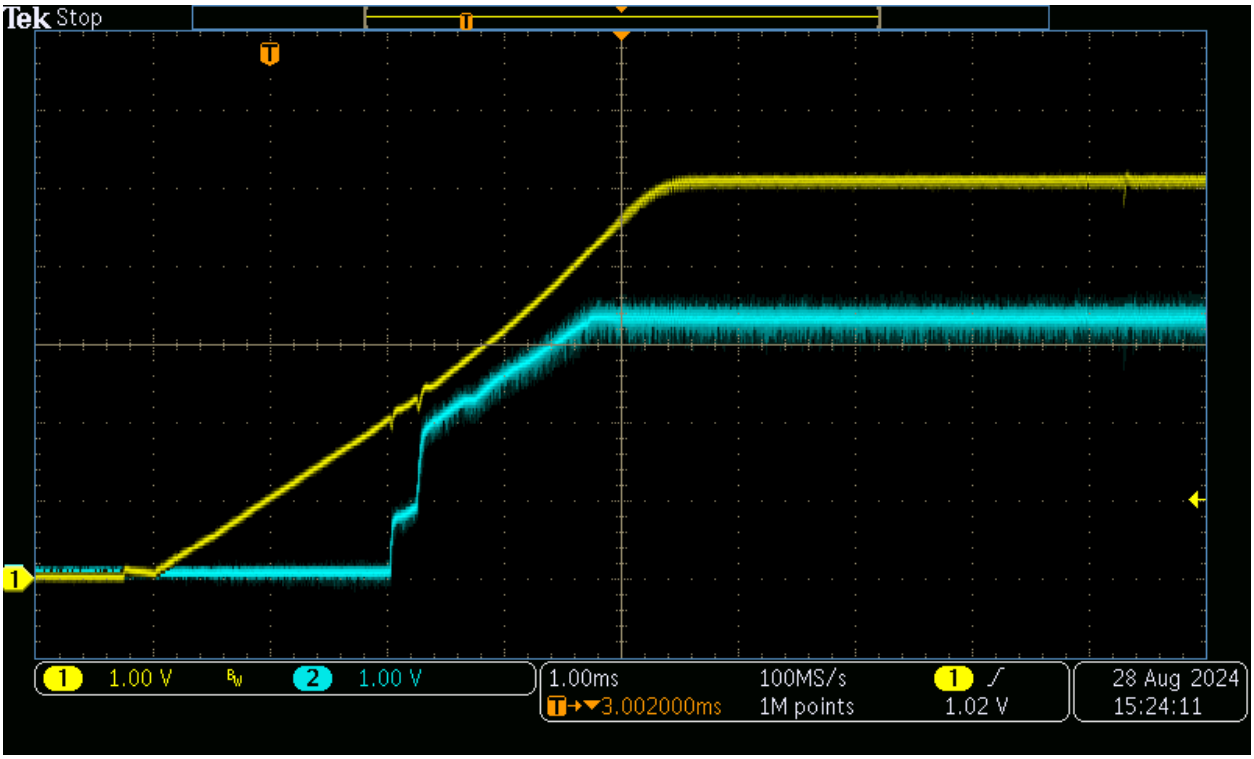

Figure 11: 5V SMPS startup while loaded. T = -20 °C

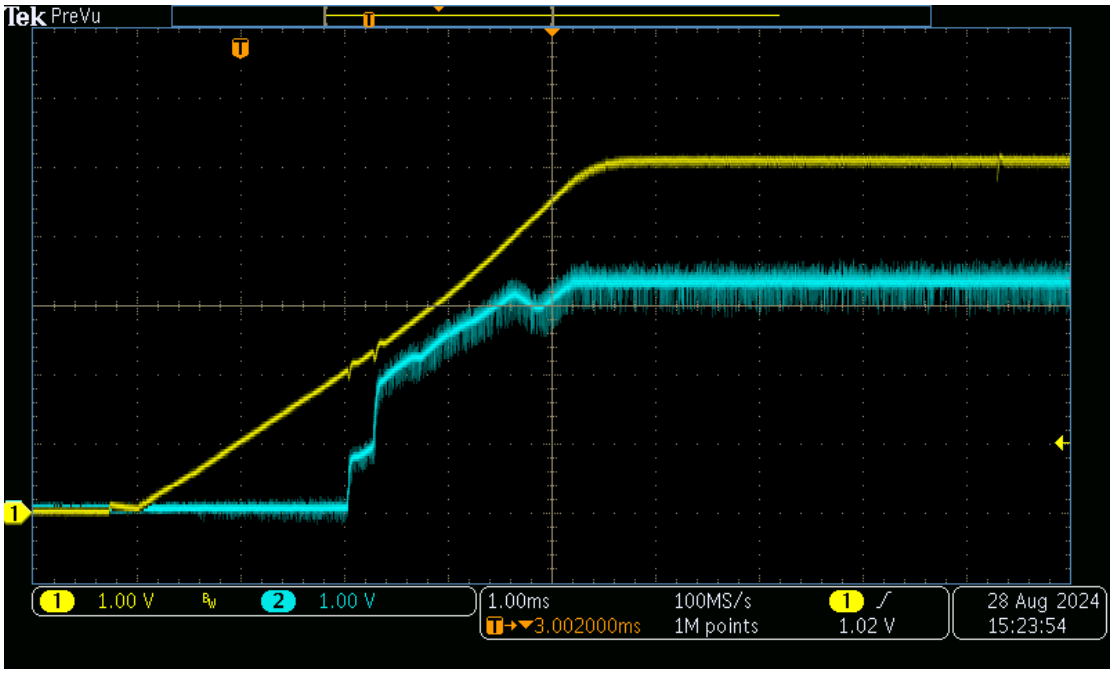

Figure 12: 5V SMPS startup while loaded. T = 24 °C

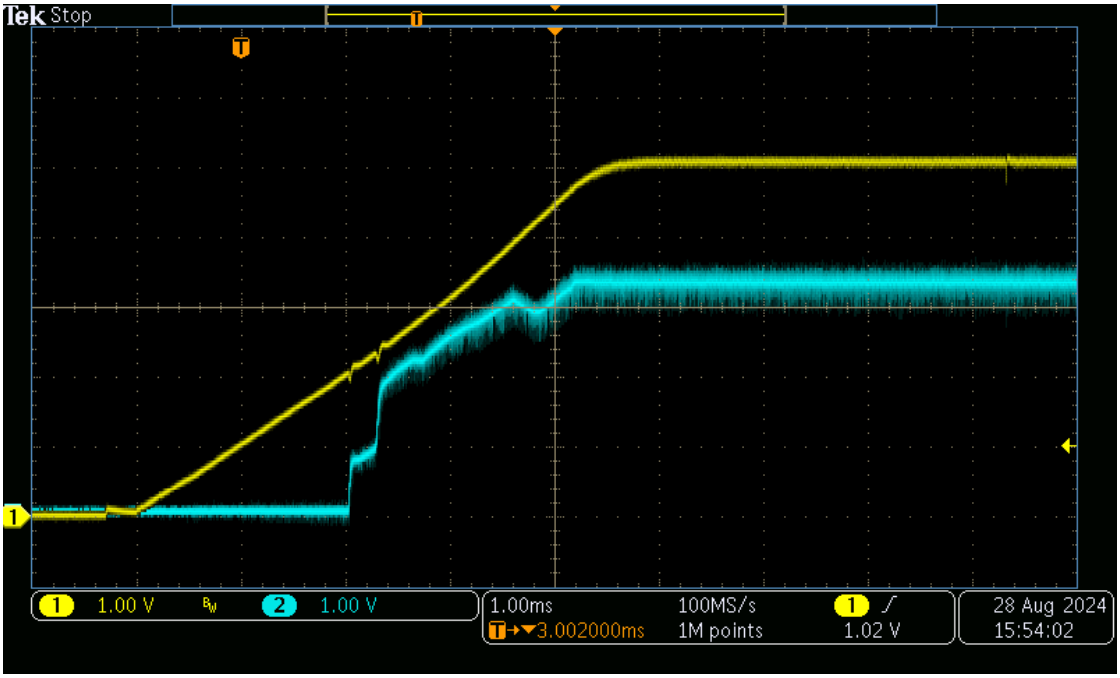

Figure 13: 5V SMPS startup while loaded. T = 60 °C

Result: It was shown, that with regular system loads the 5V regulator has no problems starting and reaching nominal output voltage. Added 10 Ω output load proves that there is enough margin, and the regulator is not close to some performance limit. Test is passed.

6. 3.3V SMPS

Problems were detected with the regulator and these tests will be skipped. They will be performed once design issues are fixed, and new prototypes produced.

6.1. Constant load

6.2. Load step

7. Power output test

Prototype P03 is used for this series of tests

7.1. Output function test

Since the SW development has not reached the level where convenient tools exist to toggle MCU outputs the switching will be done manually. MCU pin will be isolated to prevent damage since the state of the pin is unknown. R106 will be lifted and attached to one PAD only. The switch will be connected to the other R106 terminal.

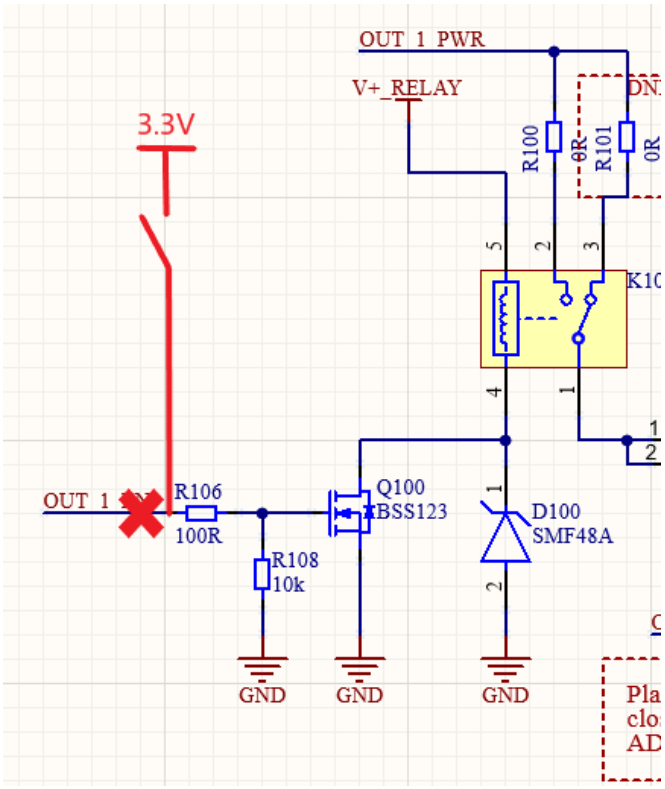

Figure 14: Output switch driver circuit

The voltage at the R106 on the switch side and the output voltage on P100 will be measured. P100 will be measured since it's the furthest from the input. Voltage drop between system input and power output will be measured.

15A fuse will be installed in fuse holder F100. Electronic load is used to load the output with 15A during the test.

Result: Fail

If the load exceeds 5A the relay will be destroyed by the electric arc forming between contacts. Heat from the arc welds the contacts so the relay stays always on.

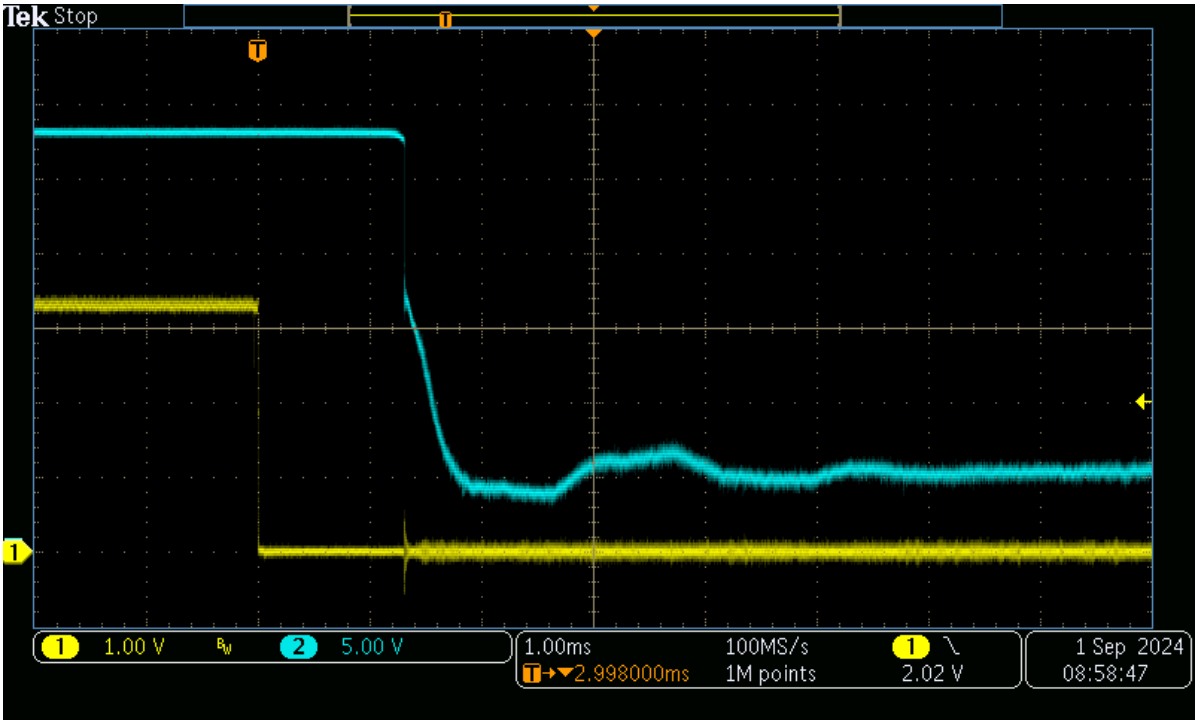

Figure 15: Output relay turn off where arcing occurs

One of the failed relays was opened for inspection.

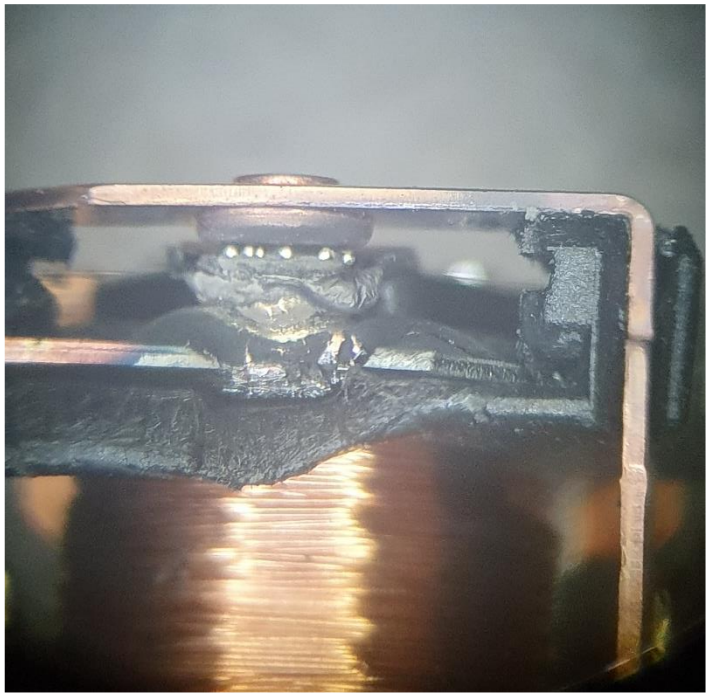

Figure 16: Magnified image of a failed relay

7.2. Output feedback system test

Output voltage and current measurement circuits

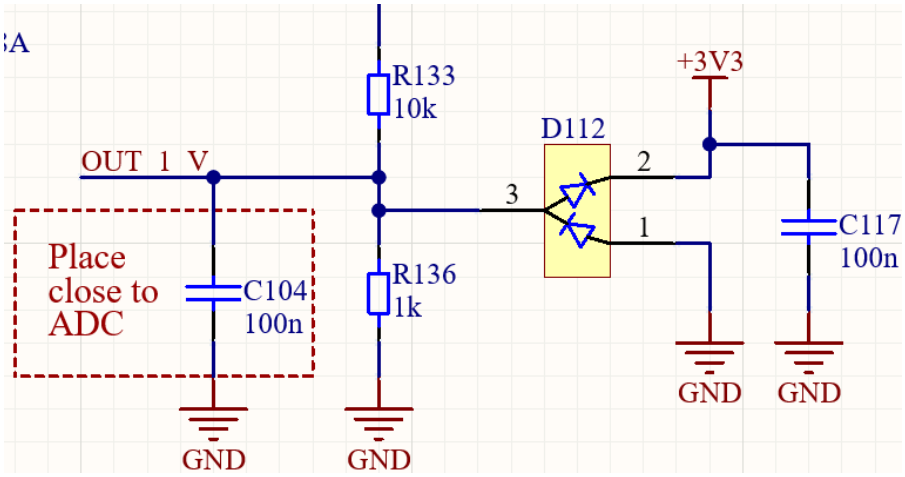

Figure 17: Output voltage measurement circuit

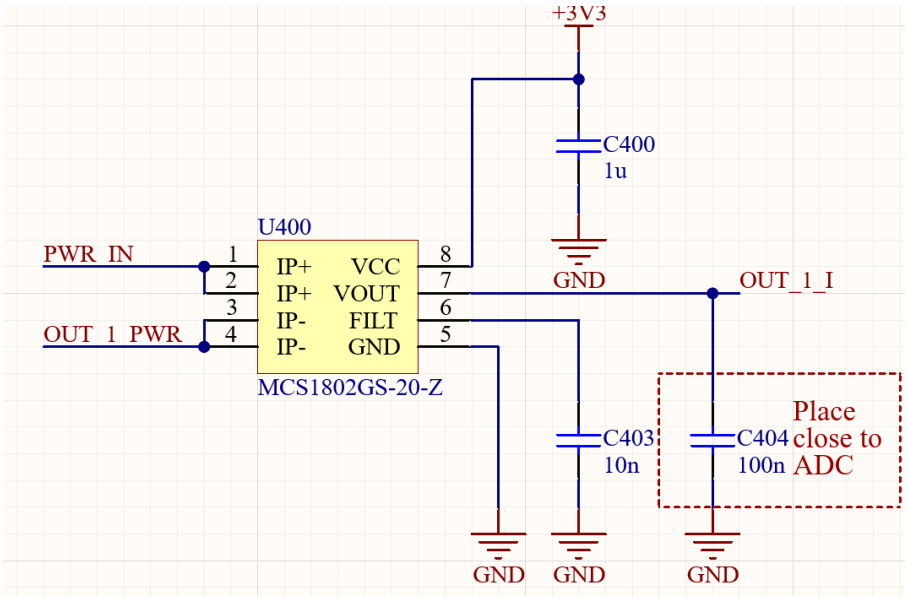

Figure 18: Output current measurement circuit

3,3 V regulator was disabled and 3,3V was supplied straight from adjustable laboratory power supply.

Output voltage was measured at ADC multiplexer input for the channel in use. Tests were performed at room temperature with unloaded output. Results are in Table 2.

Table 2: Voltage measurement circuit performance

Vin [V]	Calculated output [V]	Measured output [V]
24	2,18	2,21
28	2,55	2,58
32	2,91	2,91

Current measurement circuit output is measured at ADC multiplexer input. Tests were performed at room temperature with 28V input voltage. Results are shown in Table 3.

Table 3: Current measurement circuit performance

Iout [A]	Calculated output [V]	Measured output [V]
0	1,65	1,641
1	1,716	1,708
3	1,848	1,841
5	1,98	1,972
10	2,31	2,304
15	2,64	2,635

Result: Pass
Target voltage values and measured values show minimal deviation. The circuits perform as expected and the calculation models used to translate ADC readings to voltage values work.

7.3. Maximum load test for single output

Maximum output load will be drawn at maximum ambient temperature over 2 h period.
28V is supplied to fuse board power input. Electronic load is attached to power output. The relay will be turned on manually by supplying 3,3V to the gate resistor of the relay driving transistor as shown on Figure 14. The load current is increased to 15 A and left there for 2h. 2h is sufficient for board temperature to reach it's maximum.

Figure 19: Output load test setup

Output operation was checked before the test and again after 2h at 60 °C. Output operation is checked with 1A

Result: Passed

After 2h under maximum load under maximum temperature the 15A fuse had not blown, relay operated normally and no signs of excessive heat dissipation on PCB or connectors can be detected.

7.4. Overload test

With gradual load increase

7.5. Output short circuit test

Output overcurrent and short-circuit protection not implemented in SW.

7.6. Fully loaded system with added short circuit.

Draw maximum load and then add short circuit. Will input connector and busbars survive.

8. Diagnostics functions

Functions not yet implemented in SW

9. Functional tests

9.1. Buttons

Each button switches corresponding relay and appropriate LED acts accordingly.

9.2. LED's

LED's show on, off, and fault modes.
Check LED DATA signal shape. Oscilloscope image.