Introduction

This document describes the Ethernet interface for DefSecIntel Fuse Board KR-Df-01-EL-00. To save time reference designed from NUCLEO-144 LEGACY (MB1404) is used with one notable exception. The transceiver used in the evaluation/development kit is LAN8742A-CZ-TR but the one used in Fuse Board is LAN8742AI-CZ-TR. The one with I in part number is for wider temperature range -40°C to +85°C.

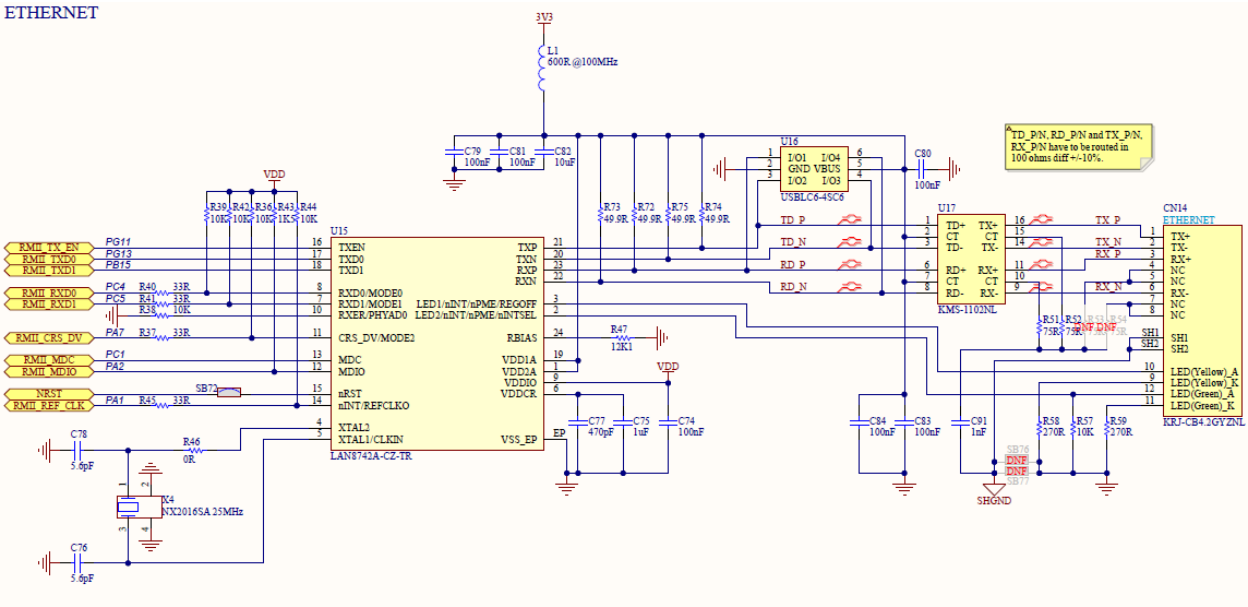

Figure 1: Evaluation kit MB1404 schematic

Oscillator selection

Reference design uses CS11321-25M. Key parameters are:
Frequency: 25MHz.
Load Capacitance: 6pF.
Temperature range: -40°C ~ 125°C.
Information about accuracy or stability is unclear, but the component parameters shown in schematic state ±20 ppm.

It's noteworthy that in the reference design MCU and Ethernet PHY use the same crystal.
ECS-250-10-37B-CTN-TR used for the MCU has the following parameters:
Frequency: 25MHz.
Load Capacitance: 10pF.
Temperature range: -40°C ~ 85°C.

Tolerance: ±10 ppm.
Stability: ±20 ppm.
ESR: 50Ω.
Drive level: 100µW.

LAN8742AI-CZ-TR datasheet shows the following requirements that the ECS-250-10-37B-CTN-TR fulfills.

Parameter	Symbol	Min.	Nom.	Max.	Unit	Note
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance at 25°C	F_{tol}	-	-	±50	ppm	(see Note 1)
Frequency Stability Over Temp	F_{temp}	-	-	±50	ppm	(see Note 1)
Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	ppm	(see Note 2)
Total Allowable PPM Budget		-	-	±50	ppm	(see Note 3)
Shunt Capacitance	C_O	-	-	5	pF	
Load Capacitance	C_L	8	-	12	pF	
Drive Level	P_W	-	100	-	µW	(see Note 4)
Equivalent Series Resistance	R_1	-	-	80	Ω	
XTAL2 Series Resistor	R_S	495	500	505	Ohm	
Operating Temperature Range		(see Note 5)	-	(see Note 6)	°C	
XTAL1/CLKIN Pin Capacitance		-	3 typ	-	pF	(see Note 7)
XTAL2 Pin Capacitance		-	3 typ	-	pF	(see Note 7)

Figure 2: 100 µW crystal specifications

One thing that the development kit ignores is the crystal series resistor. Datasheet suggests the resistor for 100µW crystals. It has a place for it, but it's populated by 0Ω resistor. Ignoring the resistor can cause the crystal to be overdriven. It still functions, but lifetime may be reduced. 499Ω resistor will be included in KR-Df-00 and the system will be tested over its temperature range. If there is no problem with system startup the resistor will be kept. If not there is a mounting option for 0Ω resistor.

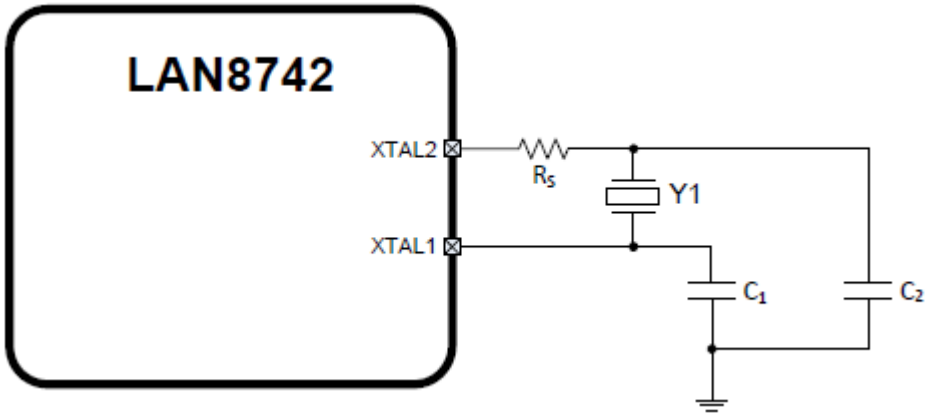

Figure 3: Crystal circuit suggested in LAN8742AI-CS-TR datasheet

The same parasitic capacitance is assumed for trace and terminals and capacitor values will be taken from MCU crystal.

Power circuits

The following circuit is suggested for power in the datasheet.

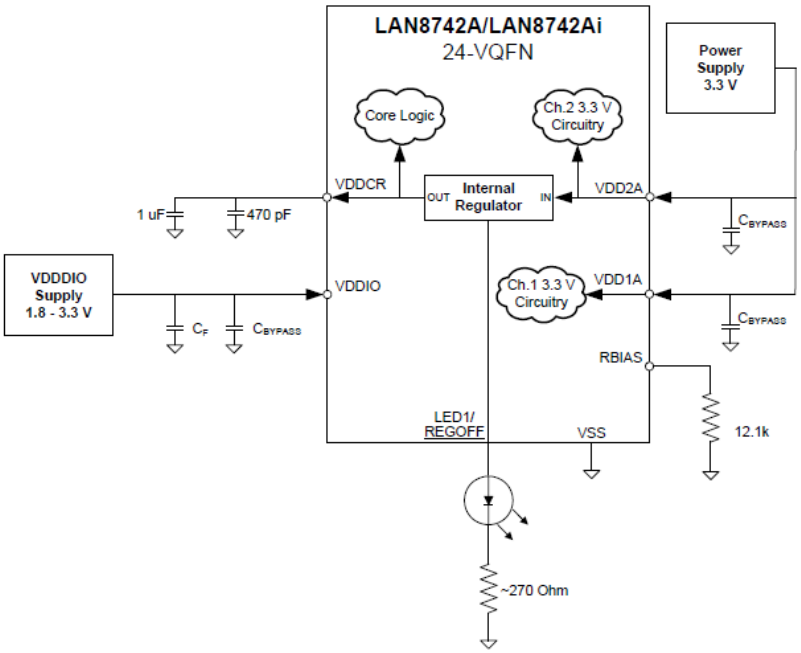

Figure 4:Power schematic when internal 1.2V regulator is used.

Datasheet does not indicate what the C_{BYPASS} value should be. 100nF capacitors are used in the evaluation kit and this will be used.

C_F is also missing a suggestion about its value. “Schematic Checklist for LAN8742” just states that the VDDIO plane should have proper bulk capacitance. There will not be a separate power rail for VDDIO and the bulk capacitance is present on the 3.3V rail. This approach is also taken on the evaluation kit.

RBIAS is setting up critical bias currents for the device.

Twisted pair interface

Following is suggested by the datasheet.

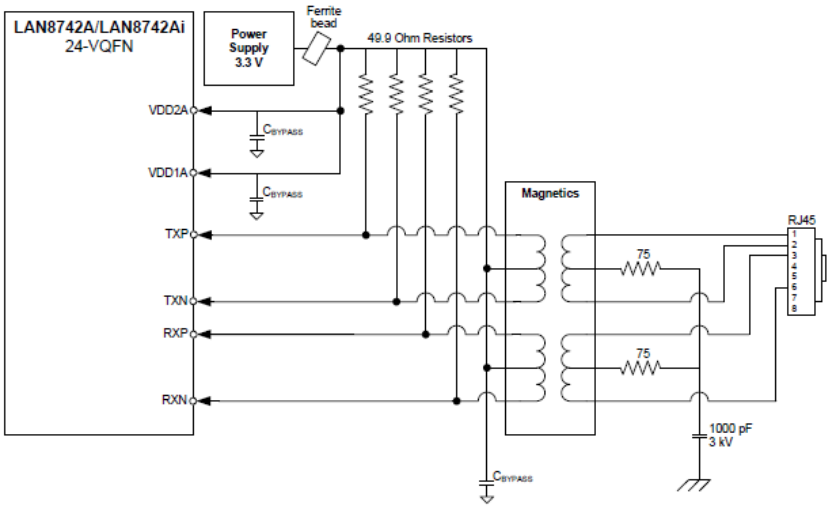

Figure 5: Schematic suggested by the datasheet for use with single power supply.

VDDA1 and VDDA2 are powered from the same rail as the 49,9Ω pull-up resistors. These are isolated from the 3.3V rail with ferrite bead and the rail will be called +3V3_ETH.

Transceiver datasheet or "Schematic Checklist for LAN8742" do not propose any values for the ferrite bead. BLM18RK601SN1D is used on MCU development kit and it fits KR-Df-01 as well. The application is identical and ferrite bead temperature range covers the temperature range of KR-Df-00.

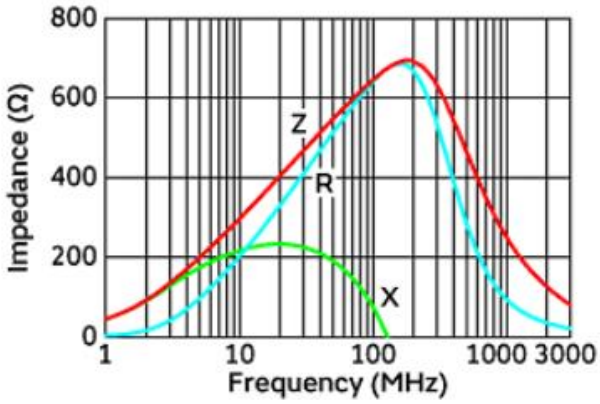

Figure 6: BLM18RK601SN1D impedance curve

Bulk capacitors are required on both sides of the ferrite bead. 10µF shall be used as on development kit. Each line on the transceiver side needs a 49.9Ω resistor connected to +3V3_ETH.

For 1:1 transformer called magnetics Pulse HX1260NL is used. On the MCU evaluation kit H1102NL was used. The HX1260NL has a wider temperature range from -40°C to 85°C. The latter also has better crosstalk between adjacent channels and common mode rejection ratio. It's connected to the transceiver as follows.

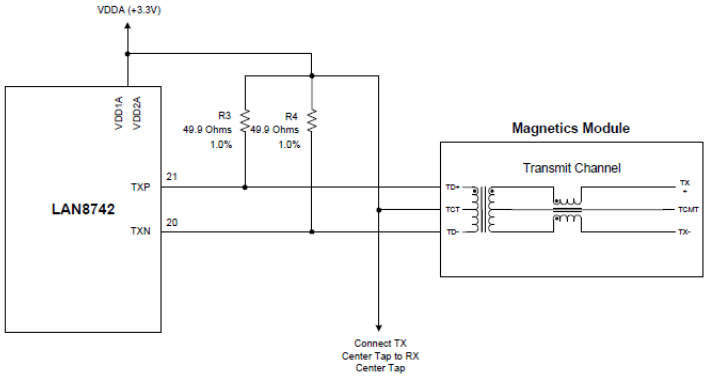

Figure 7: Connection to magnetics.

For protection against transients development kit also has a TVS diode at the transceiver side of the magnetics. Microchip Application Note AN2157 the diode junction capacitance must be below 5 pF, 1A clamp voltage below 5V and working voltage must be 3.3V

For USBLC6-4SC6 in the development kit the working voltage seems to be around 5,25V and clamping voltage for 1A 8/20 µs pulse is 12V. This is outside the specification of AN2157.

Instead D5V0P4UR6SO is selected from Krakul component library. It has the same internal diode structure, but the working voltage is 3.3V. Unfortunately, datasheet gives 8/20 µs pulse clamping voltage for only 5A. From I/O to GND the voltage for 5A is pulse is typically 6V. It's assumed for this project that for 1A the clamping voltage would be within transceiver requirements. Typical channel input is 2.1pF.

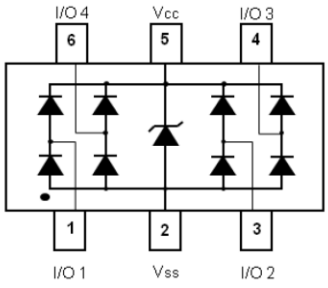

Figure 8: TVS diode internal schematic.

C_{BYPASS} shown on Figure 5 should be 22nF according to schematic checklist. However information gathered from other engineers suggests that usually 100nF capacitors are used. This is also the case on the MCU development board seen on Figure 1.

Schematic on the transceiver side of the transformer is shown below.

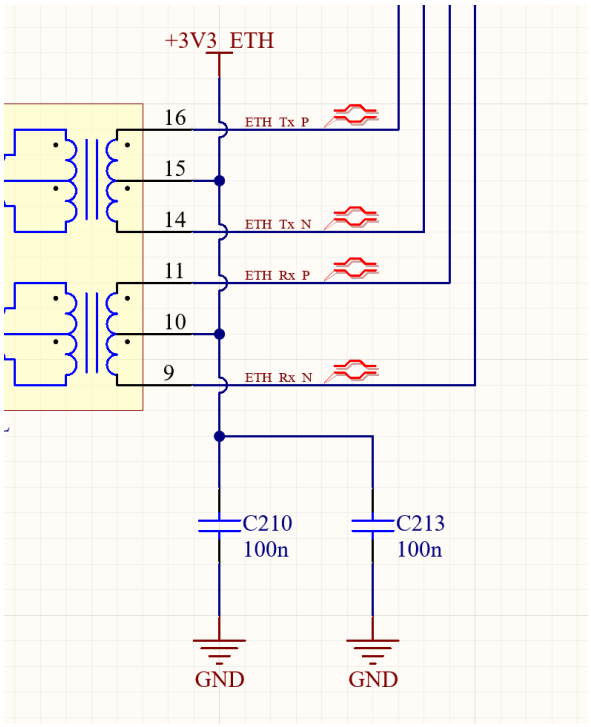

Figure 9: Twisted pair components between transformer and transceiver

On the connector side of the magnetics 3 components are required: two 75Ω resistors and 1nF capacitor. There are no special requirements for resistors, but the capacitor must be rated for 2kV.

Datasheet shows separate chassis ground for RJ45 side termination. RJ45 shield is also connected to this. On KR-Df-00 chassis ground will not be used and the RJ45 is connected to the circuit ground trough the 1nF capacitor to prevent unexpected ground loops trough the shield. The capacitor shall have 1MΩ 1206 resistor in parallel to shunt any charge that may be induced on the shield if it's unconnected on both ends.

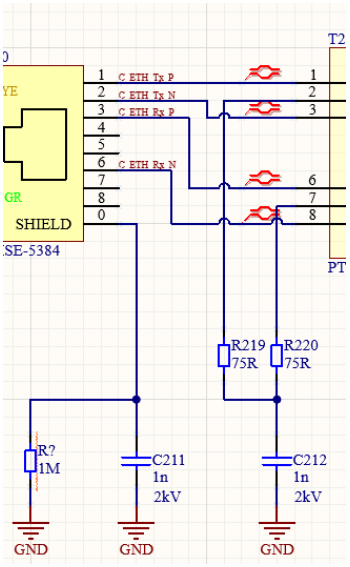

Figure 10: Circuits between transformer and connector

LED's

LED current ratings are not given in connector datasheet. The following circuit is recommended for LED1 in applications where the transceiver uses internal regulator.

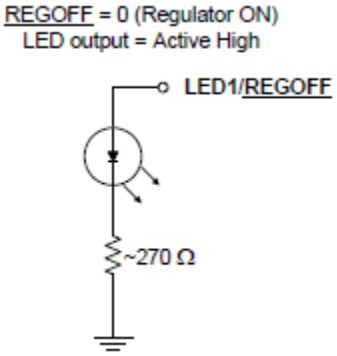

Figure 11: Circuit for LED1.

LED1 shows link activity and is connected to the Yellow LED.

LED2 shares it's pin with nINTSEL. nINTSEL selects whether transceiver generates the REF_CLK for the RMII interface. LED2 polarity depends on this selection. In KR-Df-01 the transceiver generates REF_CLK and LED2 must be pulled low.

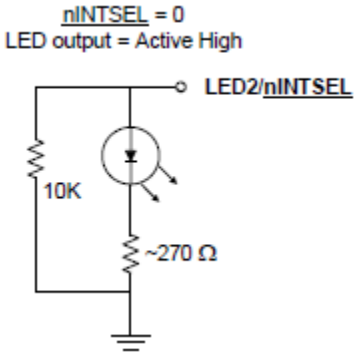

Figure 12: Circuit for LED2.

RMII

MCU development kit is used as a reference for this interface.

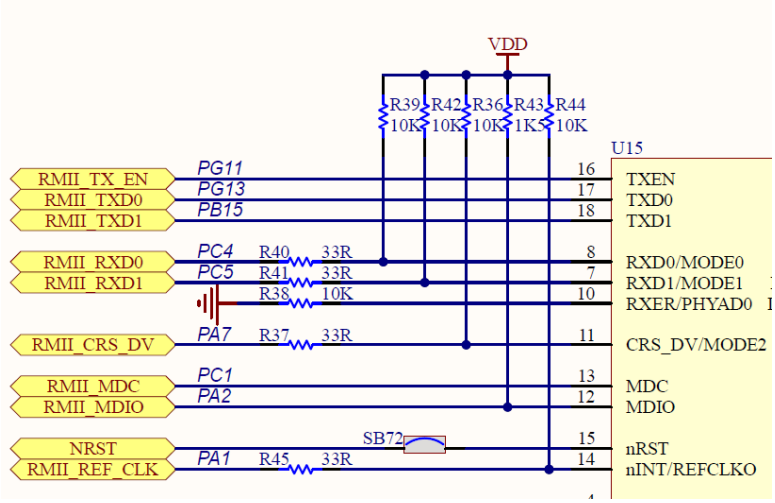

Figure 13: Schematic from development kit

9 RMII signals and one reset signal is used.

From:	Connects To:	
LAN8742 QFN	RMII MAC Device	Notes
RXD0 (pin 8)	RXD<0>	
RXD1 (pin 7)	RXD<1>	
RXD2	RXD<2>	Not Used in RMII Mode
RXD3	RXD<3>	Not Used in RMII Mode
RX_DV	RX_DV	Not Used in RMII Mode
RX_ER (pin 10)	RX_ER	This signal is optional in RMII Mode
RX_CLK	RX_CLK	Not Used in RMII Mode
TX_ER	TX_ER	Not Used in RMII Mode
TXD0 (pin 17)	TXD<0>	
TXD1 (pin 18)	TXD<1>	
TXD2	TXD<2>	Not Used in RMII Mode
TXD3	TXD<3>	Not Used in RMII Mode
TX_EN (pin 16)	TX_EN	
TX_CLK	TX_CLK	Not Used in RMII Mode
CRS_DV (pin 11)	CRS_DV	
CRS	CRS	Not Used in RMII Mode
COL	COL	Not Used in RMII Mode
MDIO (pin 12)	MDIO	
MDC (pin 13)	MDC	

Figure 14: Interconnection table from the PHY datasheet

Datasheet suggests series resistors on RX lines to match output driver impedance with PCB trace impedance to minimize ringing. The resistor values depend on the KR-Df-00 layout and there is no use of copying values from another PCB design. Datasheet suggests that 10Ω is a good value to start from.

MCU datasheet does not request a series resistors. But the same 10Ω resistors will be added for symmetry and so future tuning would be possible.

Some pull-up and pull-down resistors are needed on some dual function pins to set the transceiver up during boot. Schematic Checklist for LAN8742 requests the following pull-ups:
MDIO (pin 12) – 1,5 kΩ to VDDIO
nINT (pin 14) – Not defined. 10k is used on MCU development kit. 12.1k will be used on KR-Df-01 for it's 0402 footprint.
PHYAD0 (pin 10) has internal pull-down. Based on experience with Microchip ethernet PHY-s in Krakul external pull-down's and pull-up's improve the reliability and noise tolerance. 12,1kΩ shall be used since it's already in design in 0402 package.
Transceiver also has MODE[2:0] pins. By default these pins are pulled high by internal weak pull-up. Different configurations are described in the table below taken from the LAN8742A/LAN8742Ai datasheet.

MODE[2:0]	Mode Definitions	Default Register Bit Values	
		Register 0	Register 4
		[13,12,10,8]	[8,7,6,5]
000	10BASE-T Half Duplex. Auto-negotiation disabled.	0000	N/A
001	10BASE-T Full Duplex. Auto-negotiation disabled.	0001	N/A
010	100BASE-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.	1000	N/A
011	100BASE-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.	1001	N/A
100	100BASE-TX Half Duplex is advertised. Auto-negotiation enabled. CRS is active during Transmit & Receive.	1100	0100
101	Repeater mode. Auto-negotiation enabled. 100BASE-TX Half Duplex is advertised. CRS is active during Receive.	1100	0100
110	Power-Down mode. In this mode the transceiver will wake-up in Power-Down mode. The transceiver cannot be used when the MODE[2:0] bits are set to this mode. To exit this mode, the MODE bits in Register 18.7:5 (see Section 4.2.14, "Special Modes Register") must be configured to some other value and a soft reset must be issued.	N/A	N/A
111	All capable. Auto-negotiation enabled.	X10X	1111

In this case the “All capable. Auto-negotiation enabled” mode is desired, and all mode pins should be pulled high.

For reasons stated before, external pull-up’s will be used as well.

NRST pin of the transceiver shall have external pull down. During system startup it’s better to make sure that the Ethernet PHY remains inactive until MCU has booted up and pulled the nRST pin high.