1. Introduction

Testing temperatures
Min: -20°C
Max: 65°C
Nominal: 24°C

Testing voltages
Nominal: 24V
Maximum: 32V

2. Ethernet functional test (passed in V0 verification)

Firmware hash used for testing: 41b55d6e799b3fa55f30f365ebfebcce77e4a8eb

Ethernet was tested using a loopback configuration, where two Fuseboard UDP sockets were used to ping-pong an incrementing number over the loopback cable. UDP was chosen as it does not have any error correction. Error criteria: A socket receives a corrupt UDP packet, or the packet does not contain the valid value.

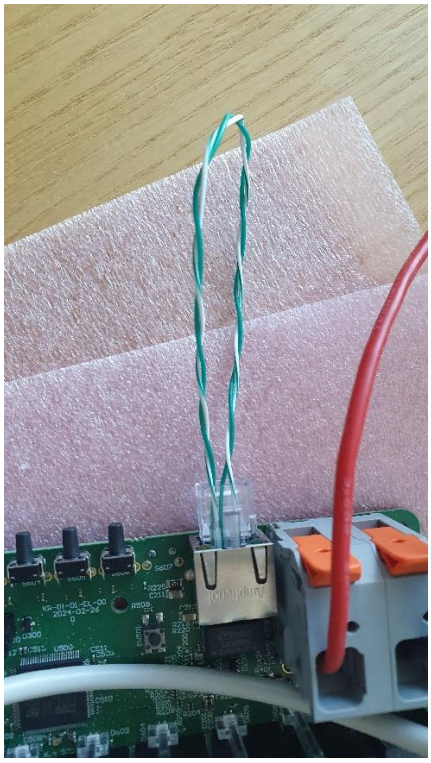

Figure 1: Loopback cable for ethernet test

Result: Pass

5,000,000 UDP packets were transmitted without errors detected.

3. RS485 interface functional test (passed in V0 verification)

Firmware hash used for testing: 2acab3907d81a91c5c4b2a2d4f8e2ccd2a1c625f

RS485 interface was tested using a PC script and USB to RS-485 dongle. A string was transmitted back and forth between the fuseboard and PC script in half-duplex mode 20,000 times (~1MiB data). Error criteria: fuseboard/PC reception timeout, or an incomplete string is received.

Result: Pass with notes

If a sufficient response delay* (between receiving a packet from fuseboard, and sending a packet to fuseboard) exists, then all data is transmitted without errors.

- 3ms delay*: ~35% of the strings received by fuseboard were incomplete;
- 5ms delay*: ~3% of the strings received by fuseboard were incomplete;
- 7ms delay*: 0% of the strings received by fuseboard were incomplete;

4. Main Input reverse polarity protection test

The main power input will be tested at -12 V, -24 V and -32 V, to validate whether polarity protection works on common battery voltages and reversed maximum tolerated input voltage.

The test was conducted using a laboratory PSU, and current draw was observed.

Test 1:
Reverse Voltage – 12V
Measured reverse current – 1mA

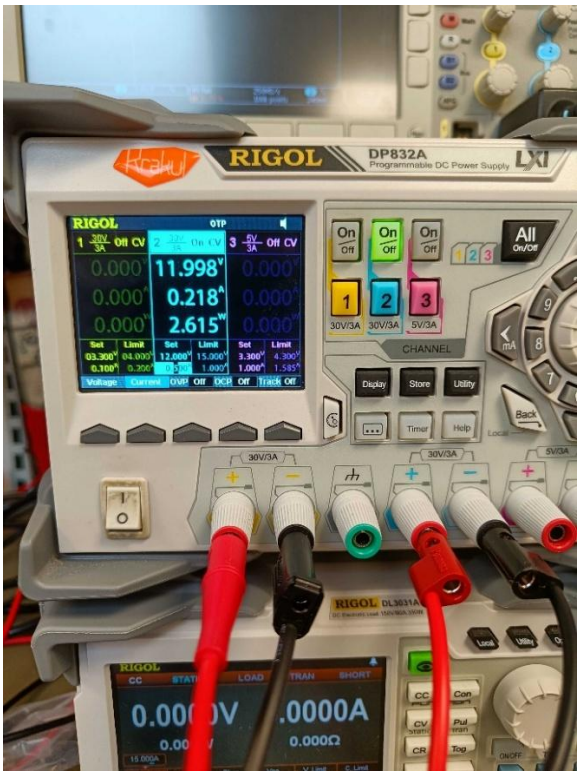

Figure 2 Correct polarity 12 V

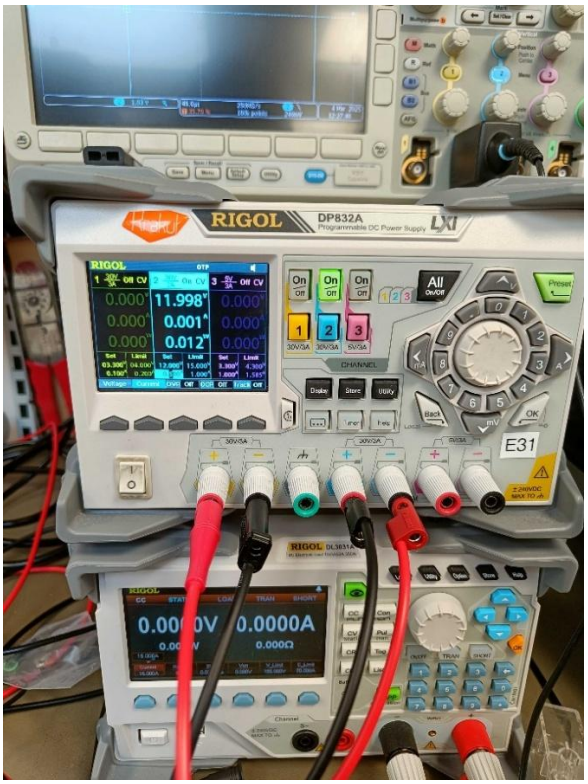

Figure 3 Reverse polarity 12 V

Test 2:
Reverse Voltage – 24 V
Measured current – 2 mA

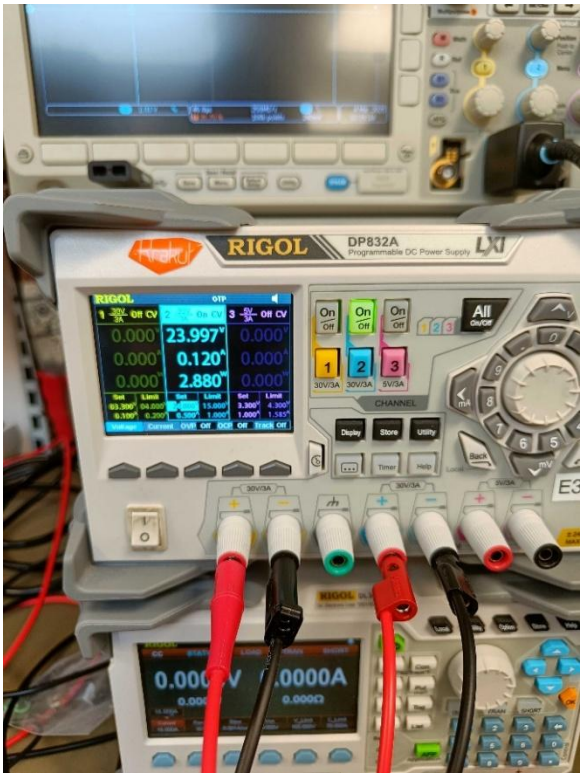

Figure 4 Correct polarity 24 V

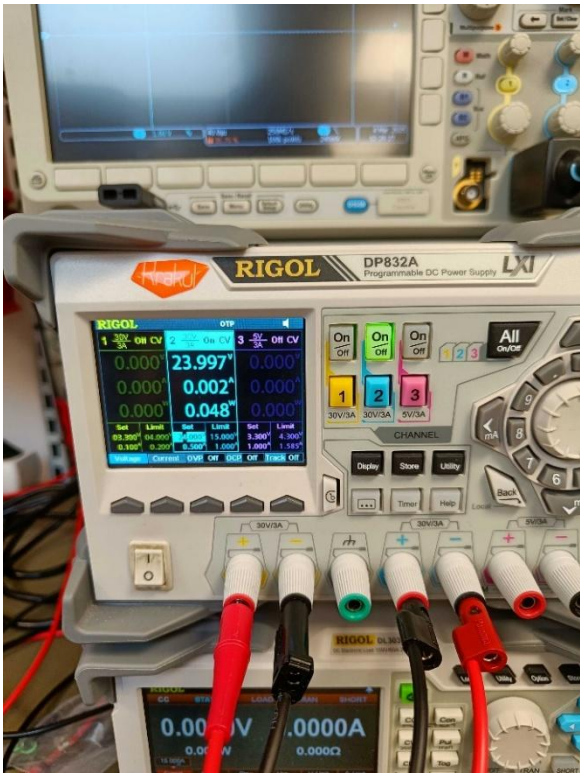

Figure 5 Reverse polarity 24 V

Test 3:
Reverse Voltage – 32 V
Measured current – 3 mA

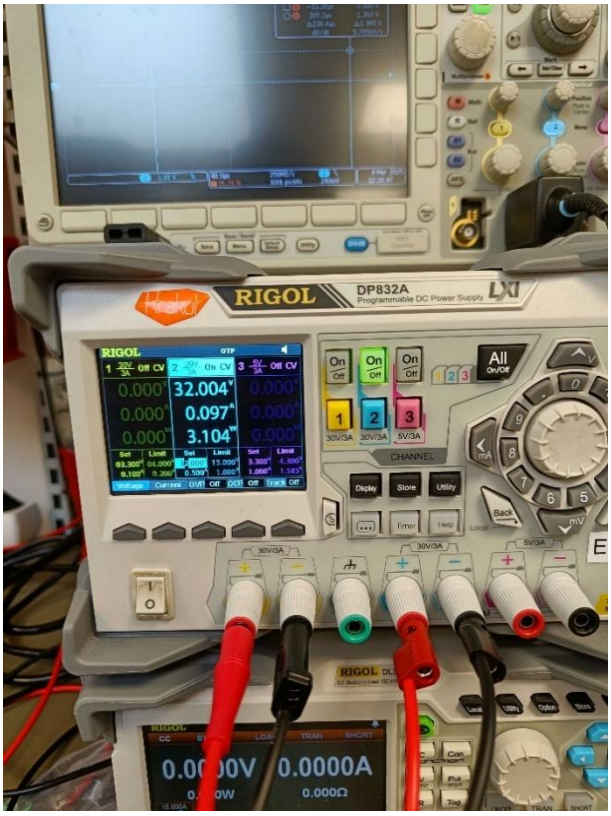

Figure 6 Correct polarity 32 V

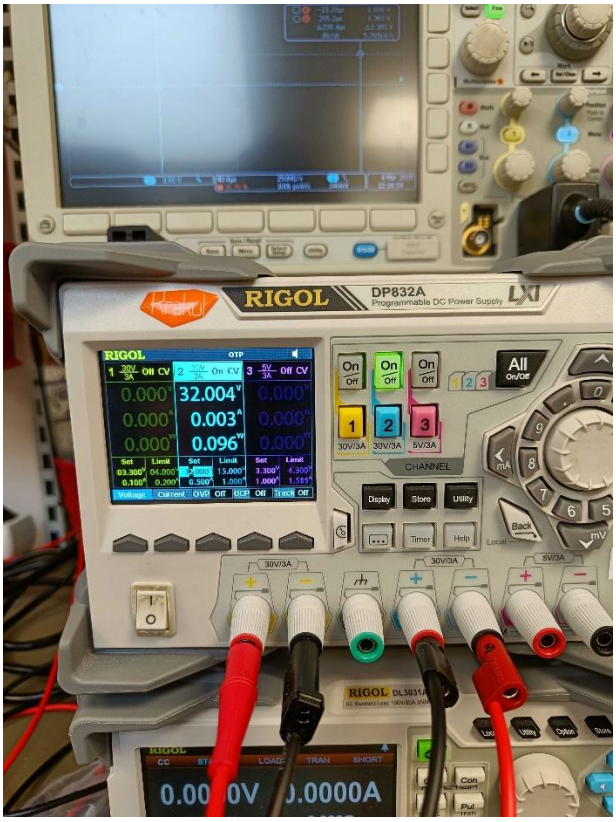

Figure 7 Reverse polarity 32 V

All voltage levels passed reverse and correct polarity testing.

After reverse polarity tests, when correct polarity input power was given, the device did not show any odd behavior and functioned as expected.

Result: **PASSED**

5. 5V SMPS (passed in V0 verification)

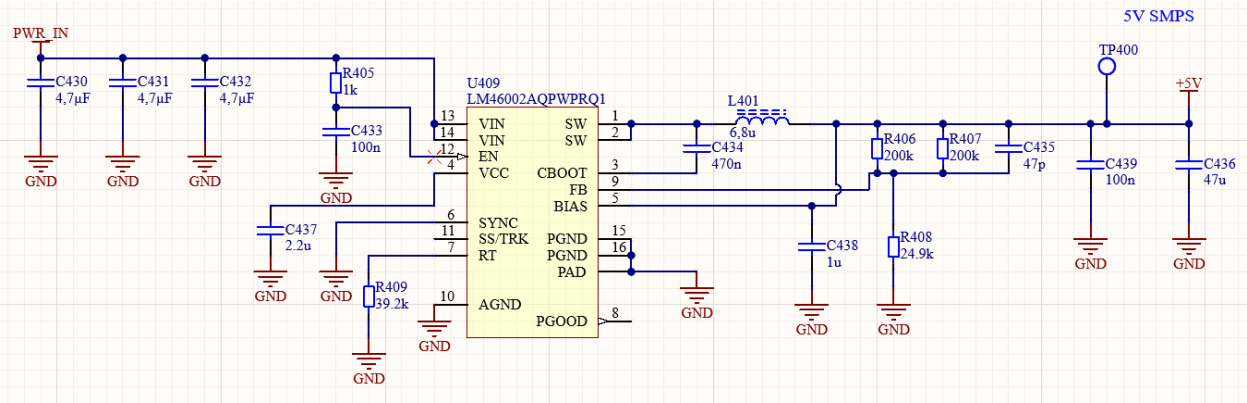

Figure 8: 5V SMPS under test

Regulator loads are removed by cutting traces on locations marked with blue lines. Electronic load is connected at the point of blue circle. Resistor R410 will not be removed. It supplies relay coils and those will not be activated.

Fuse board V0 prototype P03 was used for 5V SMPS testing.

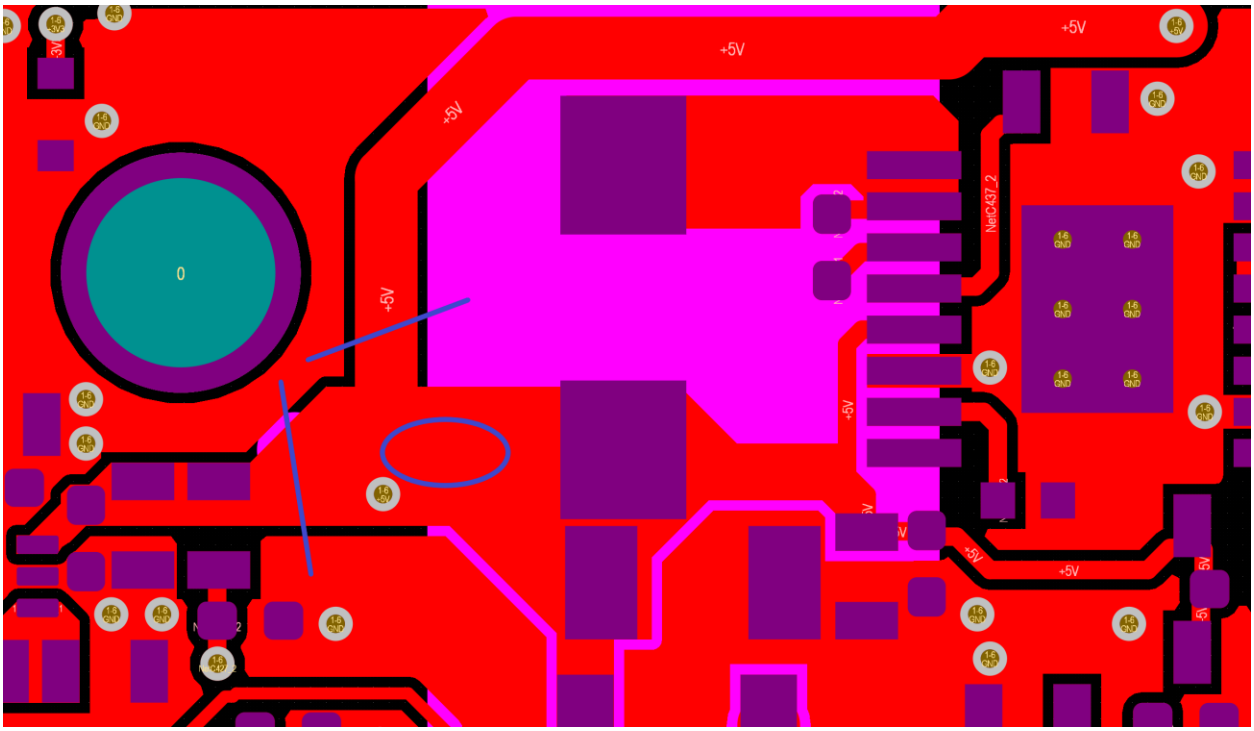

Figure 9: Modifications to PCB for 5V SMPS testing

Figure 10: 5V SMPS test setup

5V SMPS was tested on V0 prototype. The regulator is designed for 1,04A, but tested with 1,5A as well.

5.1. General reliability

Heat dissipation.
Vin = 28V.
Iload = 1,5A.
Time under load was 1,5h.
Room temperature was 24 °C.
Regulator temperature was 48.8 °C

Heat soak.
Ambient temperature was 60 °C.
Time at the ambient temperature was 16h.
Load was 1,5A.
Vin was 32A.
No difference in performance was noted after time on maximum operating temperature.

5.2. Constant load

See results in Table 1. Oscilloscope was set to 20MHz bandwidth.

Table 1: 5V SMPS static load test results

		Input voltage					
		24 V		28 V		32 V	
Temperature [°C]	Load [A]	Vout [V]	Ripple [mVp-p]	Vout [V]	Ripple [mVp-p]	Vout [V]	Ripple [mVp-p]
	0	5,138	20	5,142	23,6	5,141	24,4
	0,1	5,085	21,2	5,102	24	5,109	24,4
	0,5	5,077	26,8	5,077	26,4	5,078	23,6
	1	5,078	47,2	5,078	46,4	5,078	43,6
-20	1,5	5,078	67,2	5,077	64	5,077	62,4
	0	5,138	18	5,138	20,8	5,14	19,6
	0,1	5,08	30,04	5,099	20,8	5,107	20,8
	0,5	5,067	25,2	5,068	28,4	5,068	26,8
	1	5,066	46	5,066	45,2	5,066	44,8
24	1,5	5,064	68,4	5,064	66	5,064	69,2
	0	5,147	17,6	5,146	21,6	5,147	22
	0,1	5,088	27,6	5,104	23,6	5,114	22
	0,5	5,074	30	5,073	29,2	5,073	28,8
	1	5,076	54,8	5,075	50	5,076	55,2
60	1,5	5,078	78,4	5,078	75,6	5,081	77,6

Result: Voltage to load dependence causes output voltage change that's under 2%. This will not result in negative effects to system performance. **Test is passed**

5.3. Load step

Load was stepped from 0,25A to 1,25A and back to 0,25A. Test was performed with 28V input voltage at -20 °C, 24 °C and 60 °C.

Electronic load was used to create the load curve.

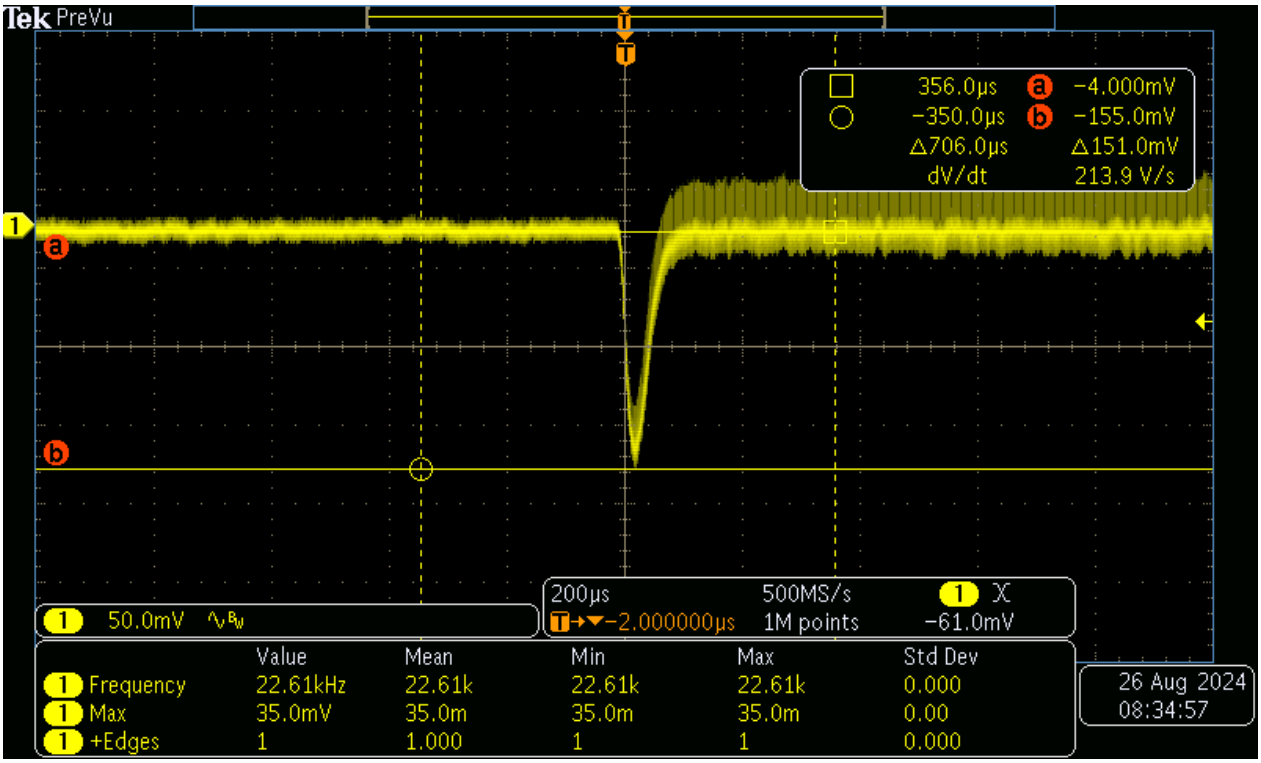

Figure 11: - 20 °C Low to high load

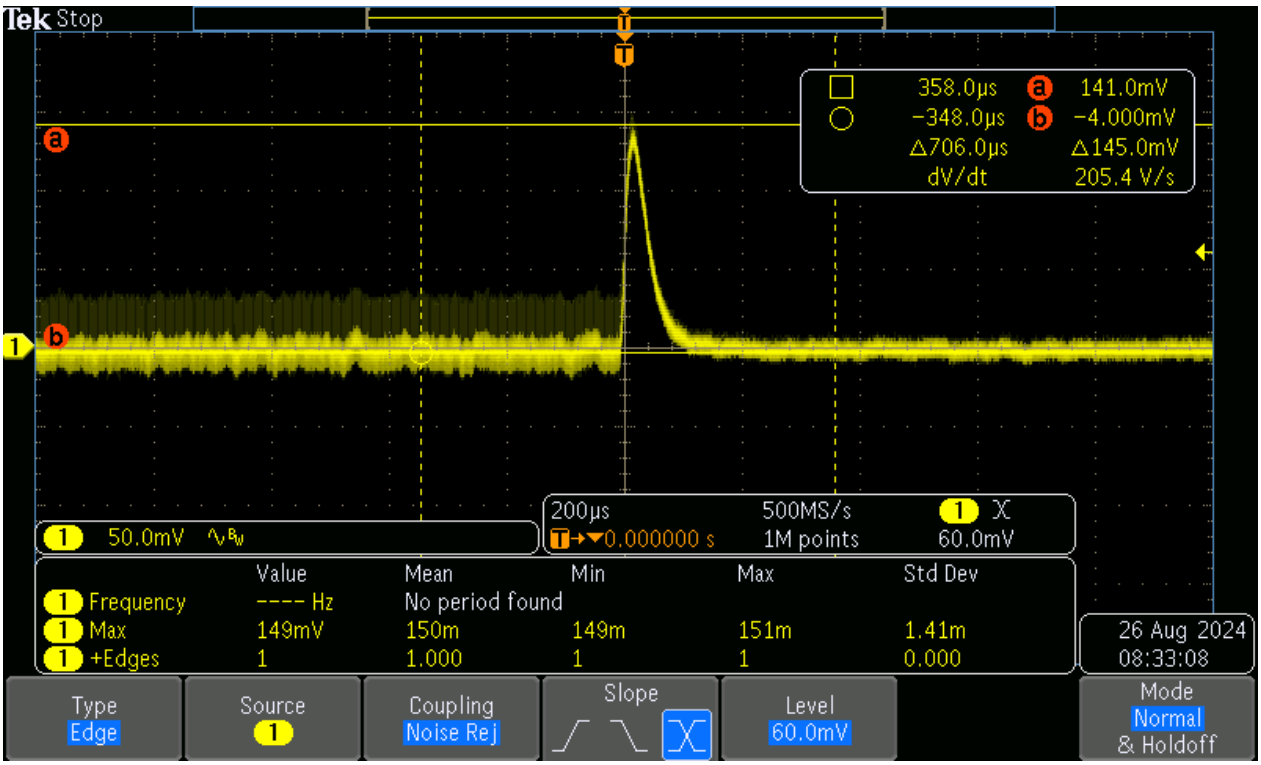

Figure 12: -20 °C High to low load

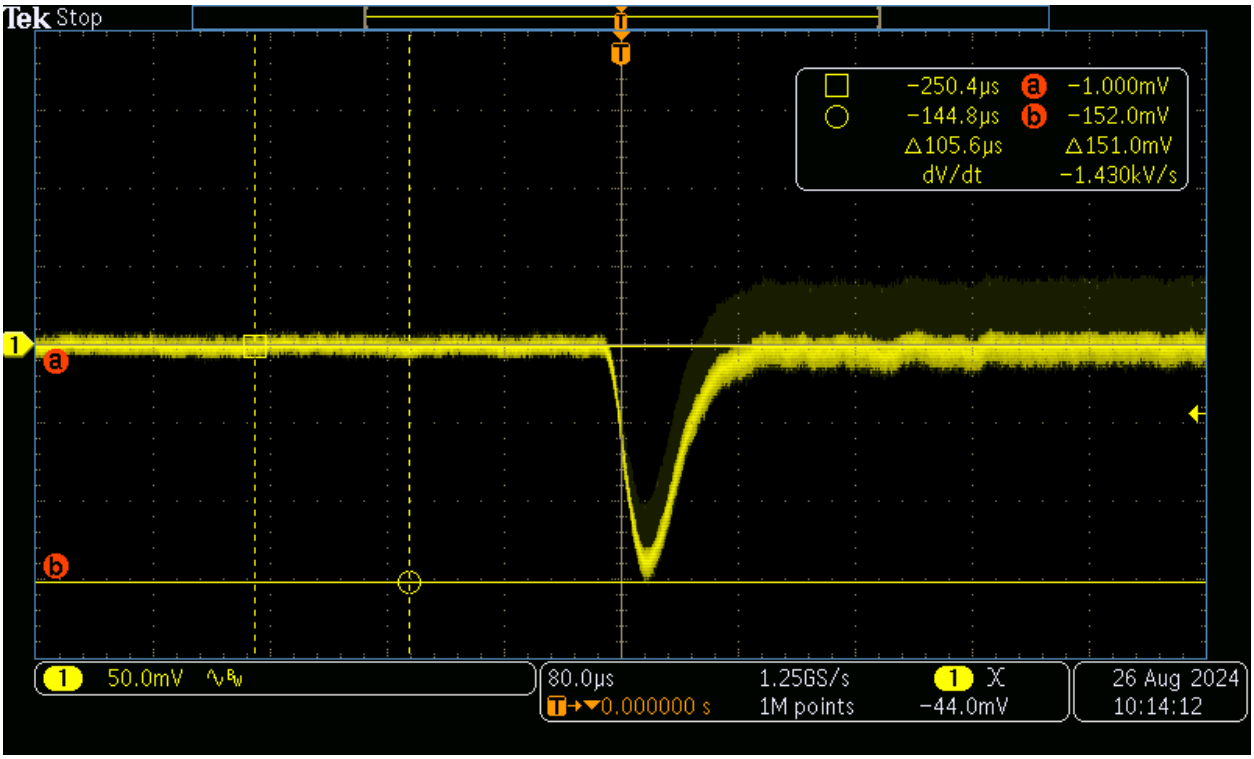

Figure 13: 24 °C Low to high load

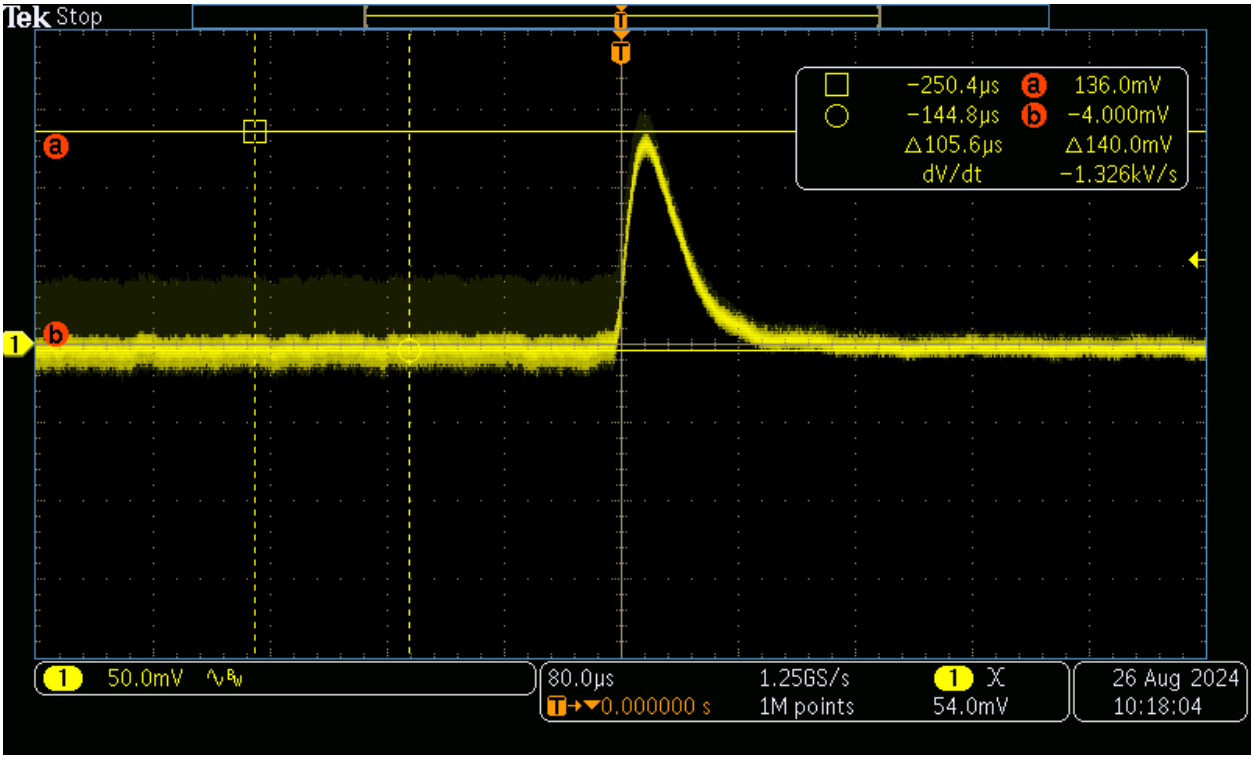

Figure 14: 24 °C High to low load

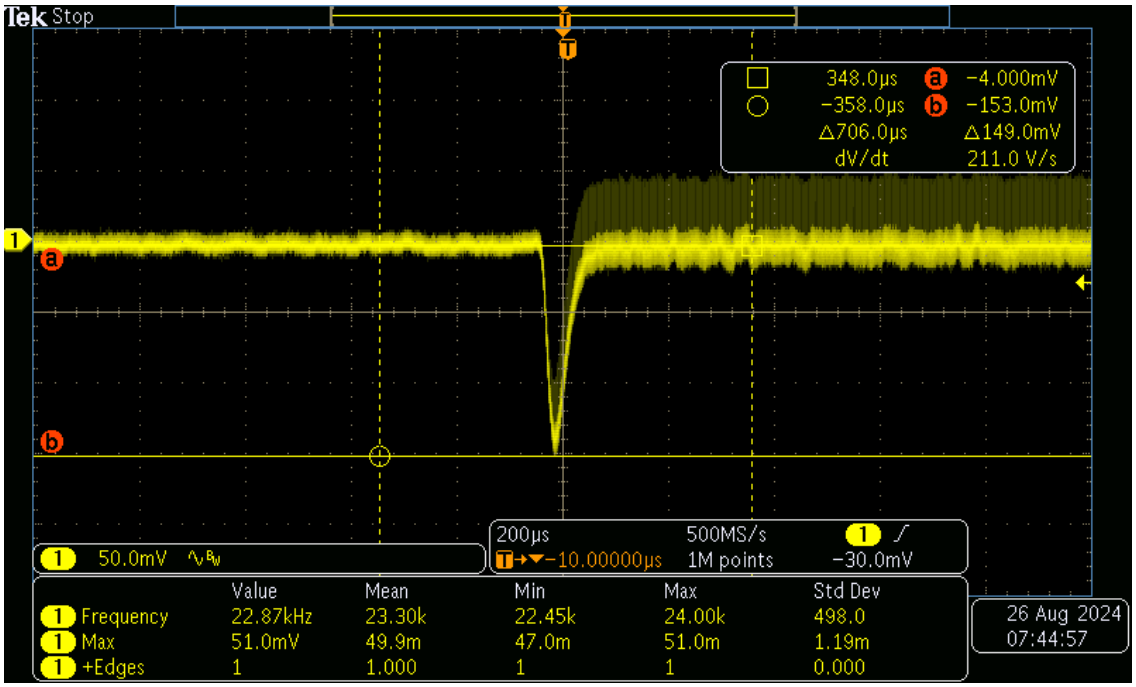

Figure 15: 60 °C Low to high load

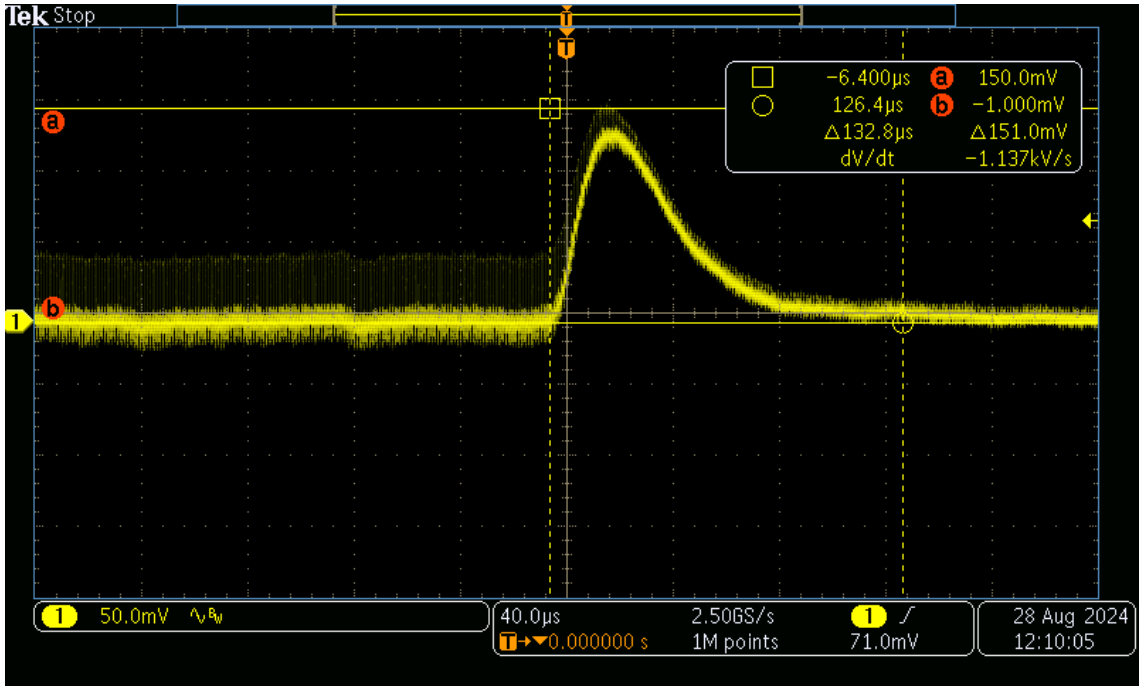

Figure 16: 60 °C High to low load

Result: Sudden change in regulator load causes a voltage deviation around 3% from nominal output voltage. This will not cause negative effects in systems supplied by this regulator. It's shown that the regulator is stable as there is no ringing while the voltage is settling. **Test is passed**

5.4. Startup under load

It was noted during tests, that if the regulator is loaded before regulation voltage is achieved it may not reach the target voltage. However once regulation voltage is achieved no problem with loading is detected. It's believed that the behavior is caused by the overload protection system reacting to large initial current. It regulates the current down to prevent damage to the regulator IC causing the regulator fall short of the target output current.

In order to make sure the system startup is not negatively effected the following test was performed. All regular system loads were re-attached and additional 10Ω (0,5A) was added to the 5V supply rail. Test was repeated at -20 °C, 24 °C and 60 °C. 3,3V power rail is also monitored.

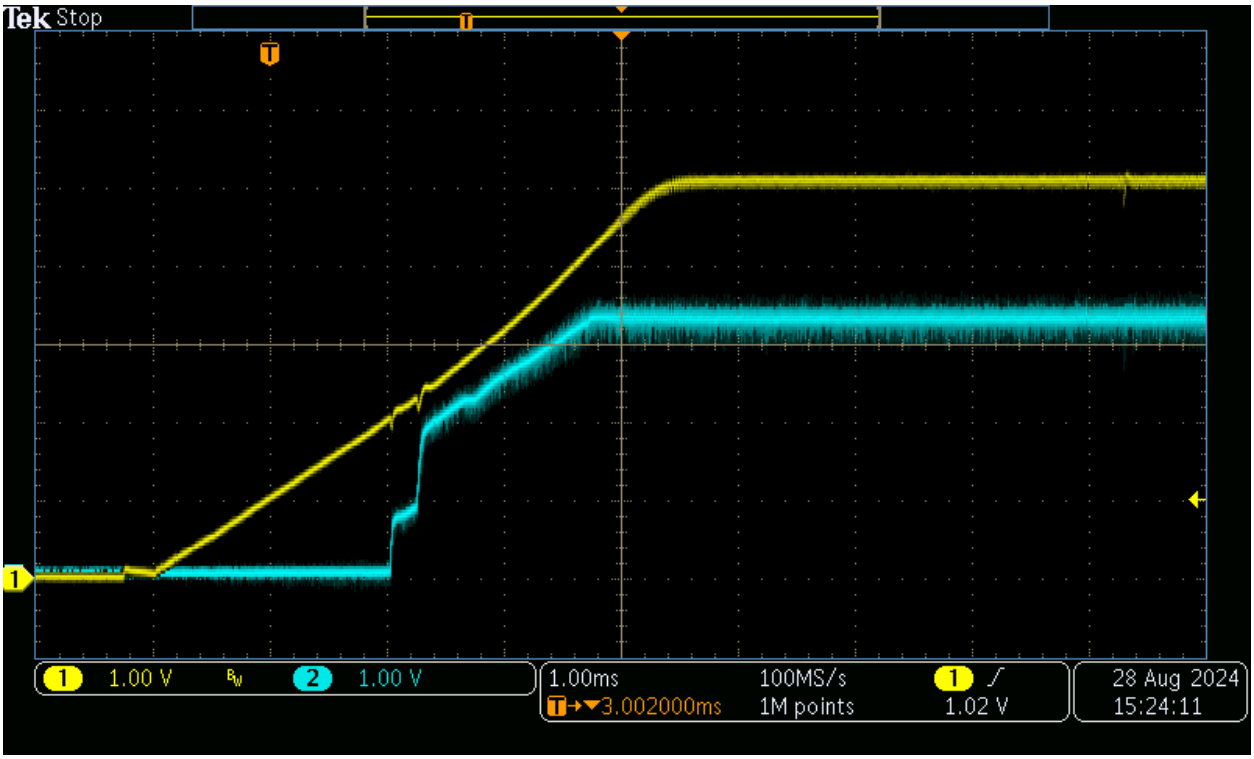

Figure 17: 5V SMPS startup while loaded. T = -20 °C

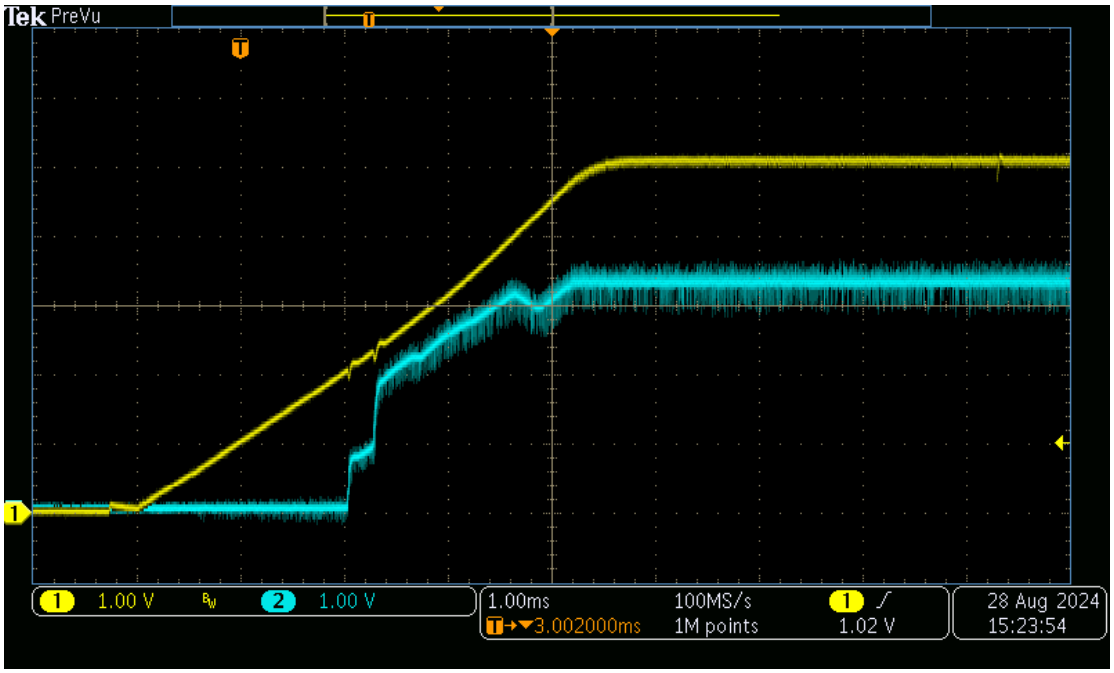

Figure 18: 5V SMPS startup while loaded. T = 24 °C

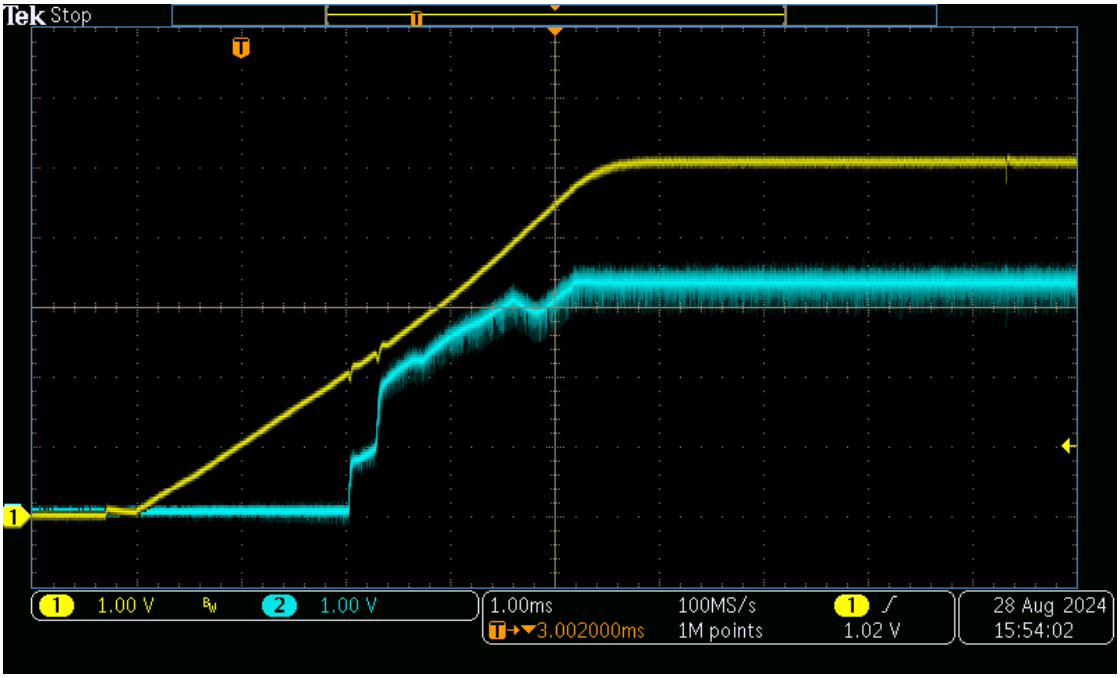

Figure 19: 5V SMPS startup while loaded. T = 60 °C

Result: It was shown, that with regular system loads the 5V regulator has no problems starting and reaching nominal output voltage. Added 10 Ω output load proves that there is enough margin, and the regulator is not close to some performance limit. **Test is passed.**

6. 3.3V SMPS

In V0 verification, Problems were detected with the regulator and these tests were skipped. They will be performed now, to validate design fixes on new revision prototype.

6.1. General reliability

Heat dissipation.
Vin = 5V (from onboard SMPS)
Iload (max) = 0.5 A
Time under load was 20 min.
Room temperature was 24 °C.
Regulator temperature was 44.5 ± 1 °C

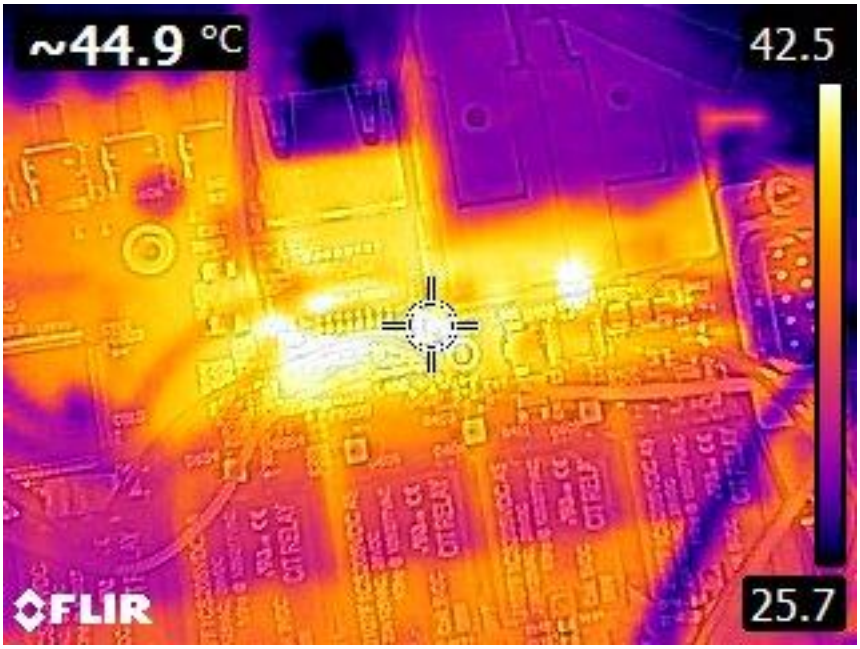

Figure 20 Hotspot at 3V3 SMPS circuit

Test is considered passed, as the temperature remained stable throughout the last 10 minutes of the test.

6.2. Constant load

See results in Table 2 3V3 SMPS static load test resultsTable 1. Oscilloscope was set to 20MHz bandwidth.

The board was held at target temperature for 15 min before gathering test data.

Table 2 3V3 SMPS static load test results

		Input voltage	
		5 V	
Temperature [°C]	Load [A]	Vout [V]	Ripple [mVp-p]
-20	0.05	3.296	72
	0.1	3.294	82
	0.2	3.287	88
	0.5	3.269	98
24	0.05	3.342	83
	0.1	3.336	82
	0.2	3.304	90
	0.5	3.275	103
60	0.05	3.319	75
	0.1	3.316	78
	0.2	3.310	90
	0.5	3.292	96

Result: Voltage to load dependence causes output voltage change that's under **2%**. This will not result in negative effects to system performance.

Test is passed.

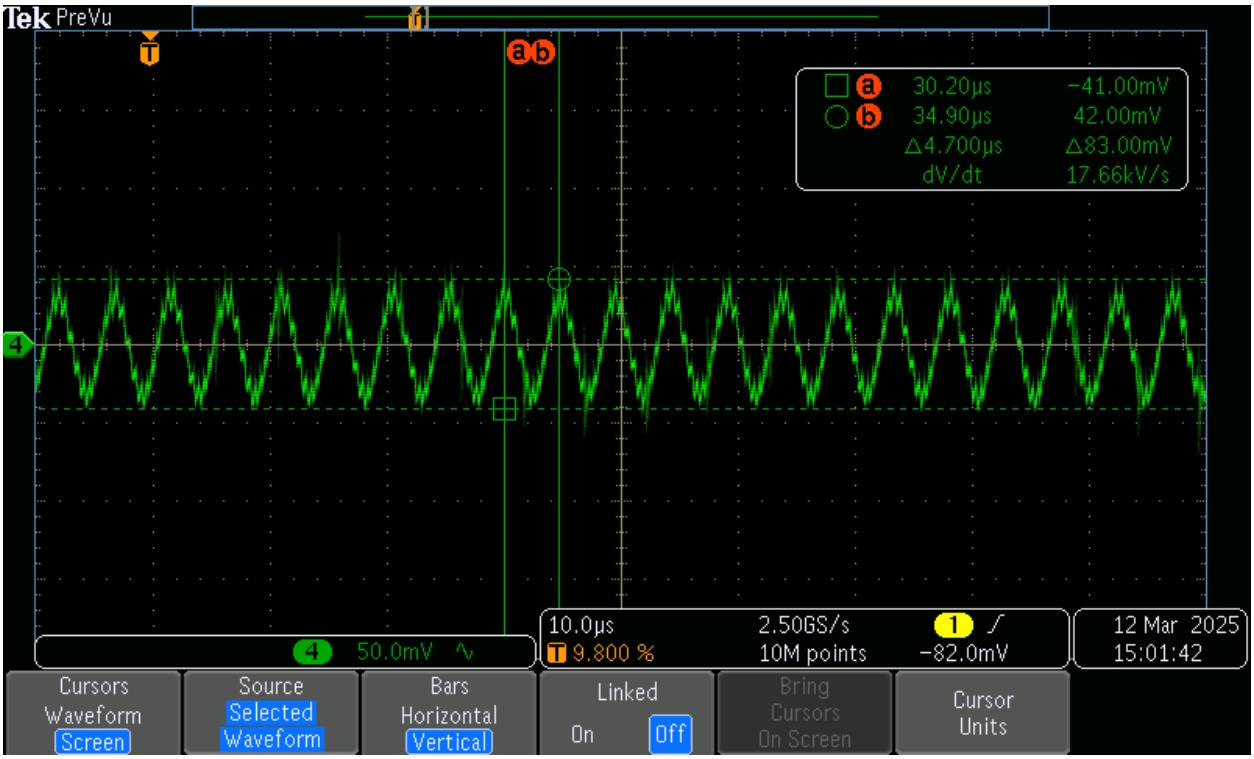

Figure 21 50mA Output ripple at 24 °C

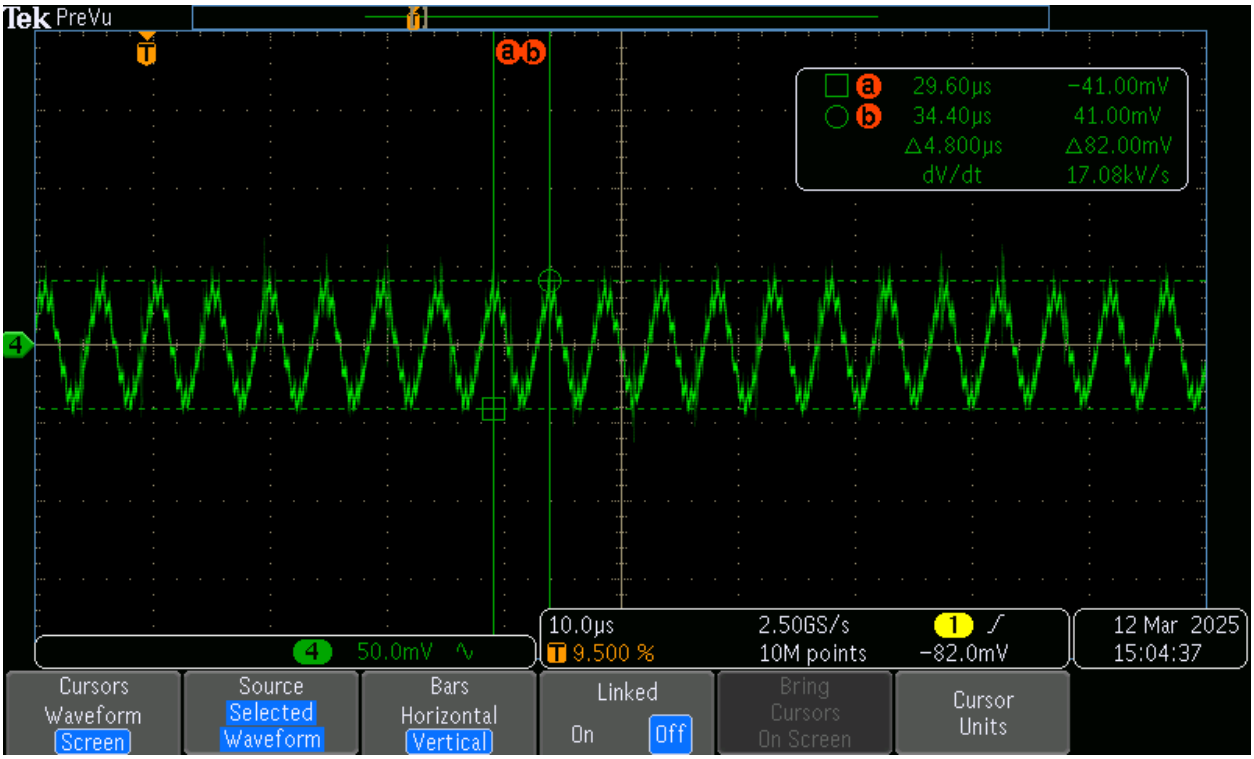

Figure 22 100mA Output ripple at 24 °C

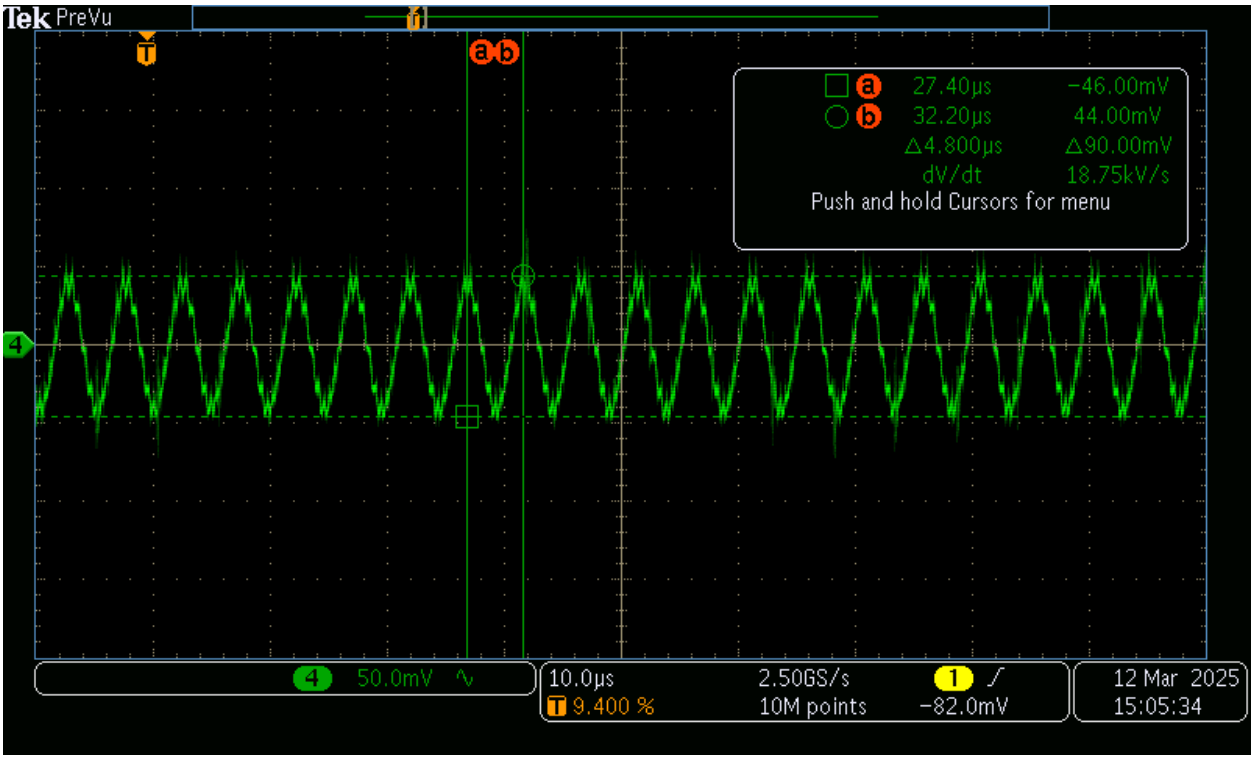

Figure 23 200mA Output ripple at 24 °C

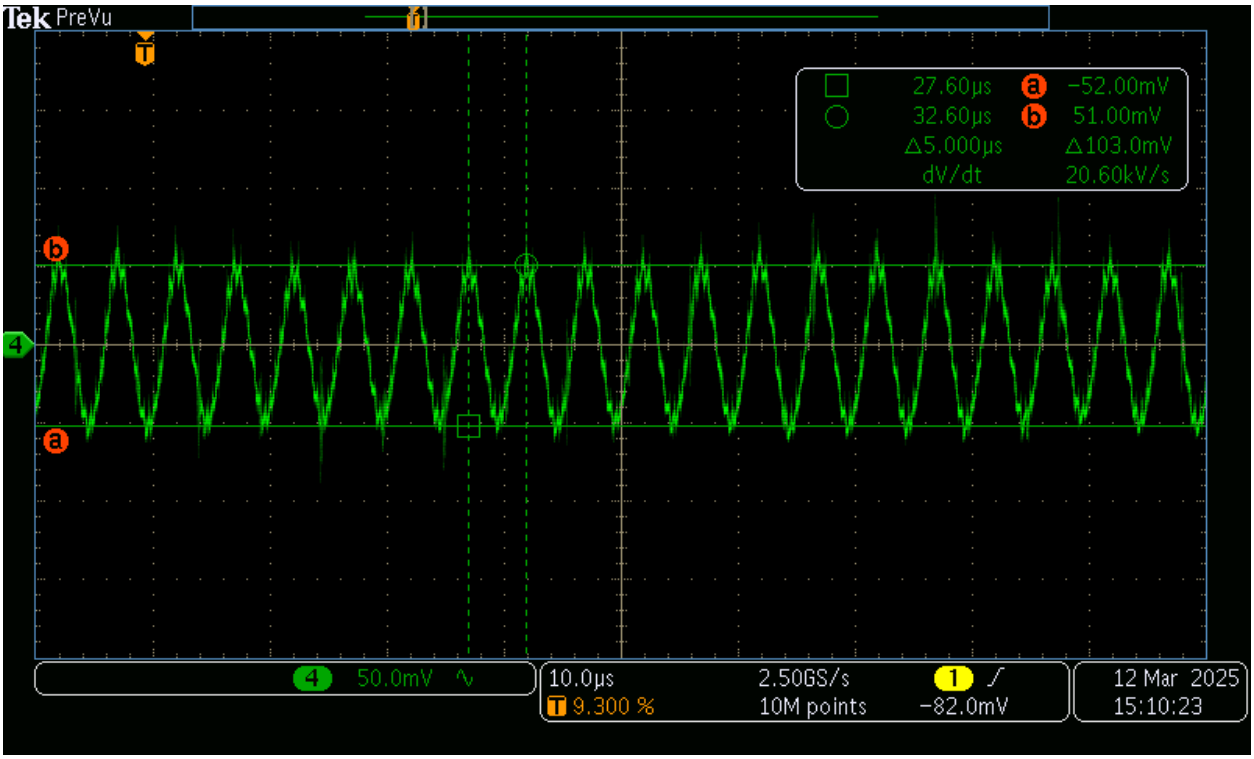

Figure 24 500mA Output ripple at 24 °C

6.3. Load step

Load was stepped from 0.1A to 0.8A and back to 0.1A.
Test was performed with 5V input voltage at **24 °C.**

Around **22mV** of load step was observed, both when going from high-low transient and vice versa. This outcome matches the waveforms in the regulator datasheet.
Electronic load was used to create the load curve.

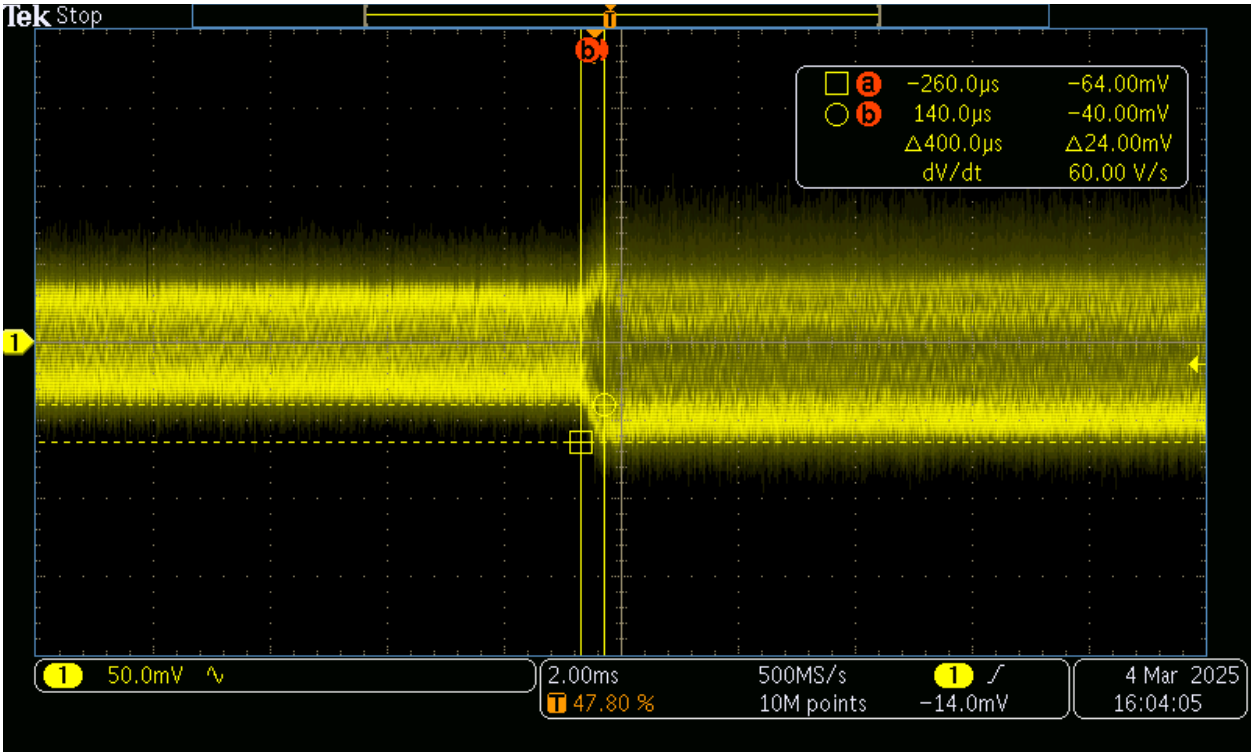

Figure 25 Load step 0.1 to 0.8 A

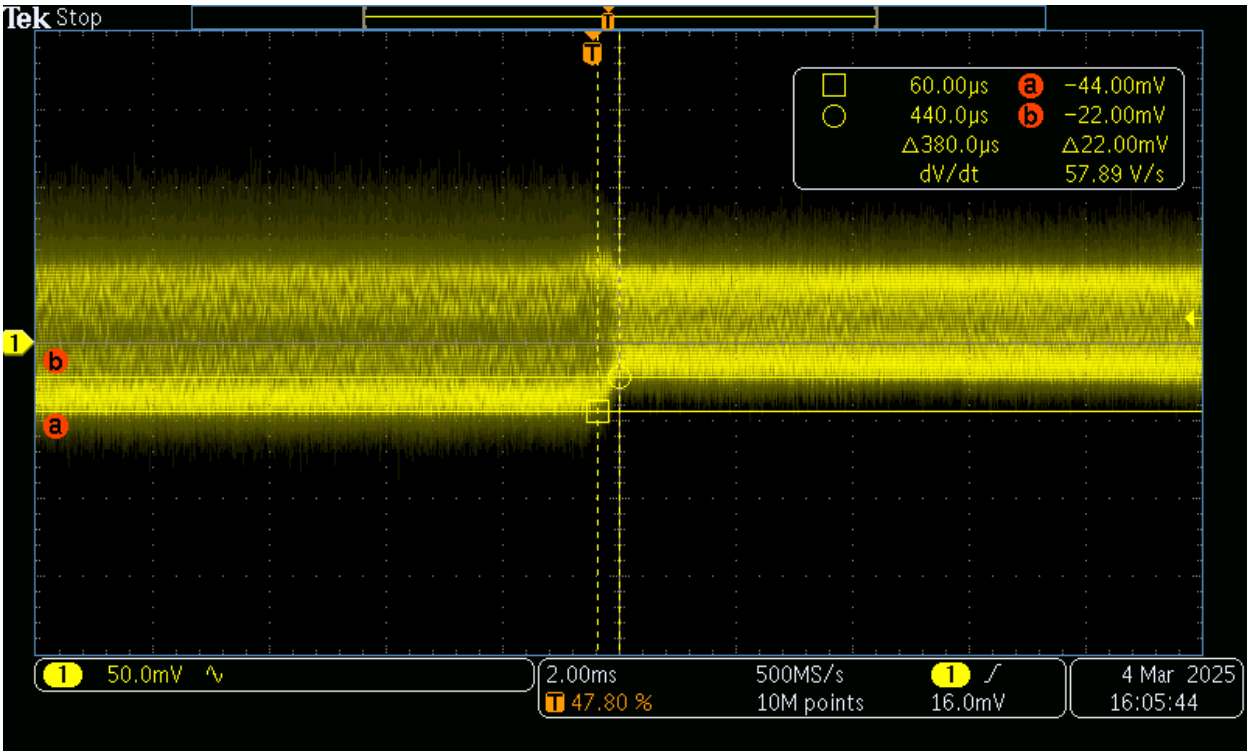

Figure 26 Load step 0.8 to 0.1 A

7. 3V3 LDO test

3V3 Analog power source LDO U410 will be loaded directly from Output Capacitor C441 terminals. The LDO will be loaded with electronic load of 100mA and 180mA (actual load on LDO is 260mA, when 8x10mA current shunt operating current is added).
The load is kept stable for 20 minutes, and LDO temperature is measured.
The loading test is conducted at ambient room temperature of 24 °C and elevated heat soak temperature 60 °C, and -20 °C.
The output voltage is observed from electronic load display and ripple is measured with an oscilloscope probe.

Test 1 (24 °C room temp):
Applied external load – 100mA
Measured input voltage – 5.067 V
Measured output voltage – 3.301 V
Measured LDO ripple voltage at output capacitor terminals – 20 mV(p-p)

Applied external load – 180mA
Measured input voltage – 5.082
Measured output voltage – 3.290 V
Measured IC temperature after 20 minutes under load – 49 ± 1 °C

Test 2 (60 °C heat soak temp):
Applied external load – 100mA
Measured output voltage – 3.297 V

Applied external load – 180mA
Measured output voltage – 3.283 V

Test 3 (-20 °C ambient temp):
Applied external load – 100 mA
Measured output voltage – 3.303 V

Applied external load – 180 mA
Measured output voltage – 3.291 V

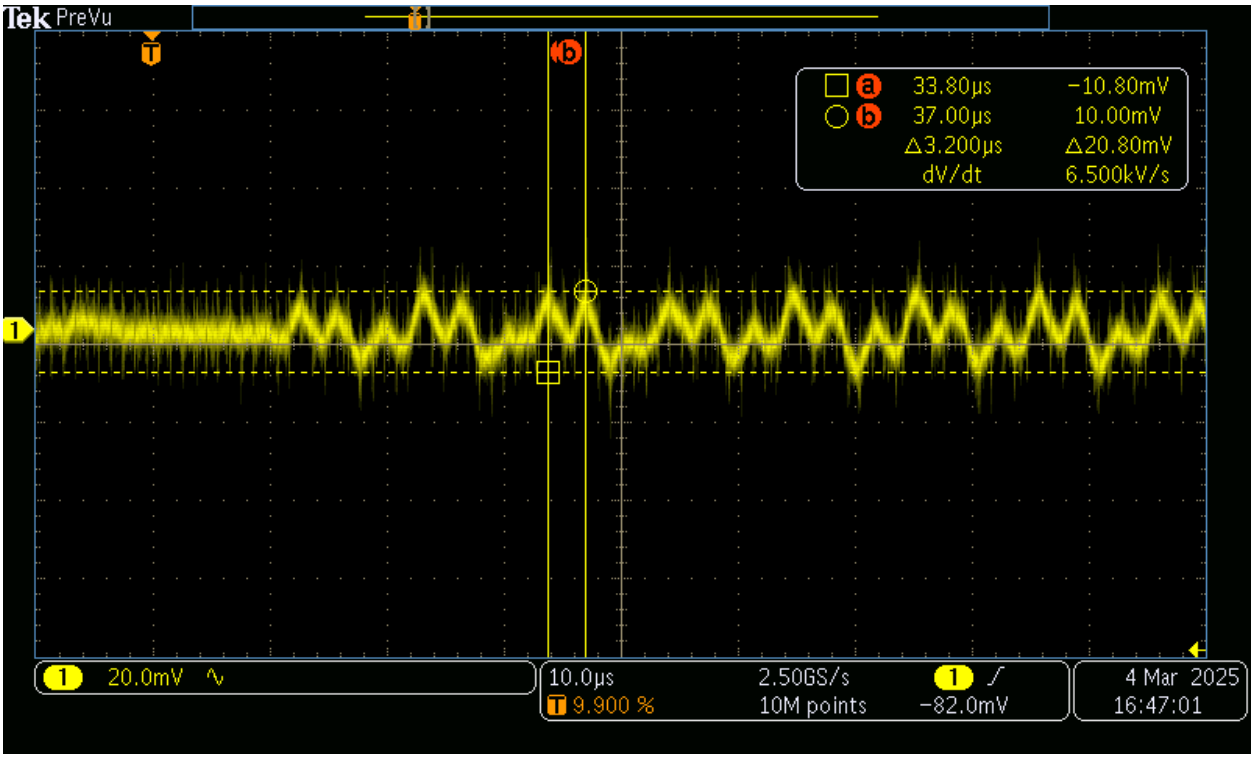

Figure 27 Ripple at LDO output capacitor terminals

8. Power output test

8.1. Output function test

Since the SW development has not reached the level where convenient tools exist to toggle MCU outputs the switching will be done manually. MCU pin will be isolated to prevent damage since the state of the pin is unknown. R106 will be lifted and attached to one PAD only. The switch will be connected to the other R106 terminal.

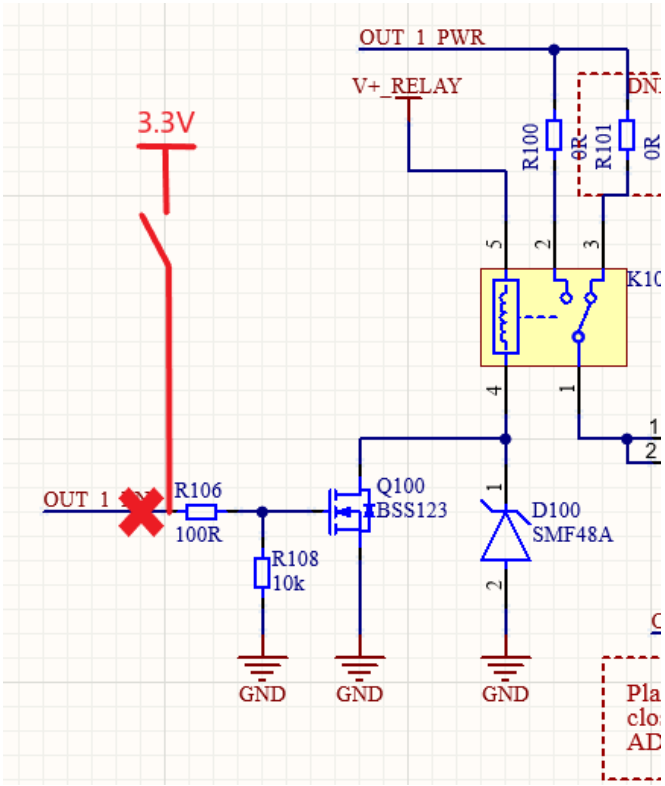

Figure 28: Output switch driver circuit

The voltage at the R106 on the switch side and the output voltage on P100 will be measured. P100 will be measured since it's the furthest from the input. Voltage drop between power output terminals Vout+ and Vout- will be measured with an oscilloscope, to monitor the voltage on relay terminals.

15A fuse will be installed in fuse holder F100.

8.1.1. Switching tests on output terminals

Waveform was measured on output terminal P100.
The tests were conducted using electronic load, oscilloscope and PSU.
Electronic load is used to load the output with 1/5/10/15A during a test, where the output is toggled at around 1Hz for 50 attempts. The test will be conducted at both room temperature 24 °C and operating temperature limits of -20 and +60 °C.

Input voltage – 24 V
1A load
Switching on - 134mV peak droop
Switching off – 508mV plateau peak

5A load
On – 320mV
Off – 1020mV

10A load
On – 320mV
Off – 1360mV

15A load
On – 490 mV
Off – 1270 mV

15A constant load 50 tests ~1Hz at room temperature.
No major deviations observed from start to finish, same waveform on terminals throughout the test.

Result: PASS.

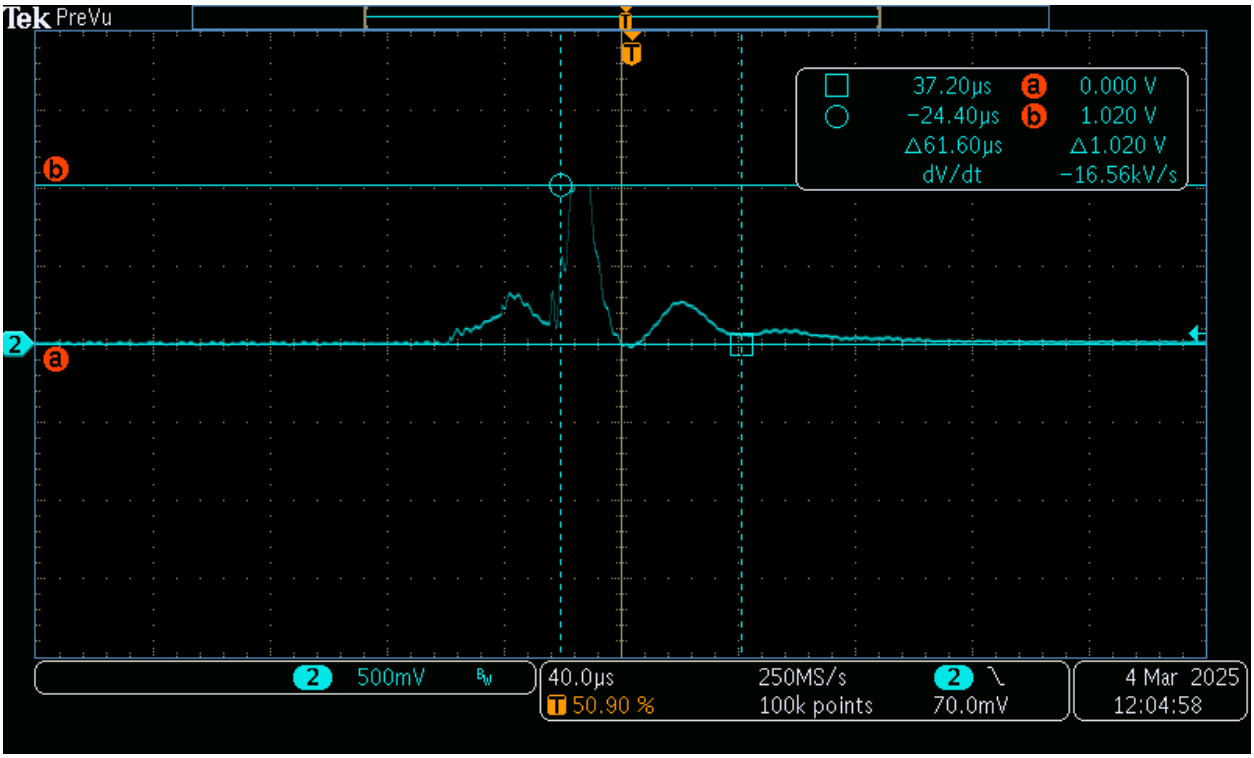

Figure 29 Waveform on switching relay ON

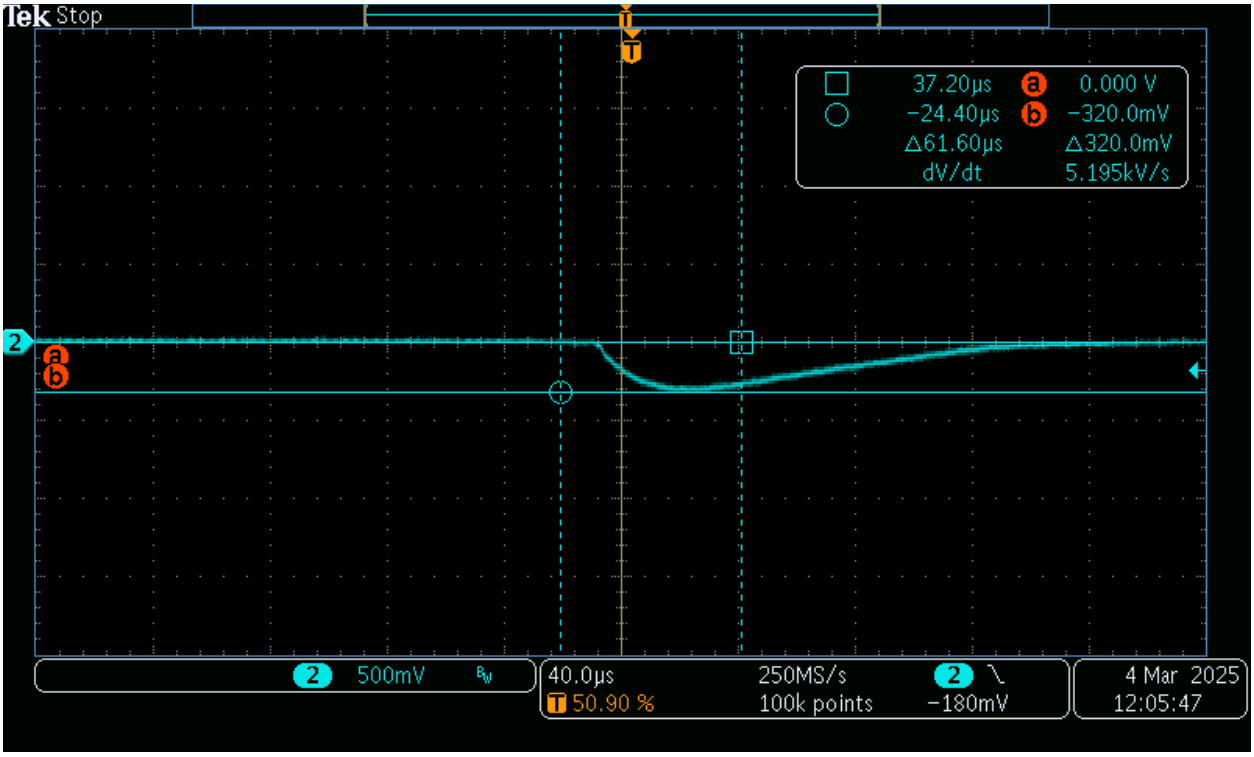

Figure 30 Waveform on switching relay ON

8.1.2. Switching tests on relay terminals

For this test, oscilloscope probes were attached to Input power(CH1, yellow) terminals, and P100(CH2, cyan) terminals.

The outputs were tested at 5/10/15A at room temperature, although the load did not change the waveform seen below.

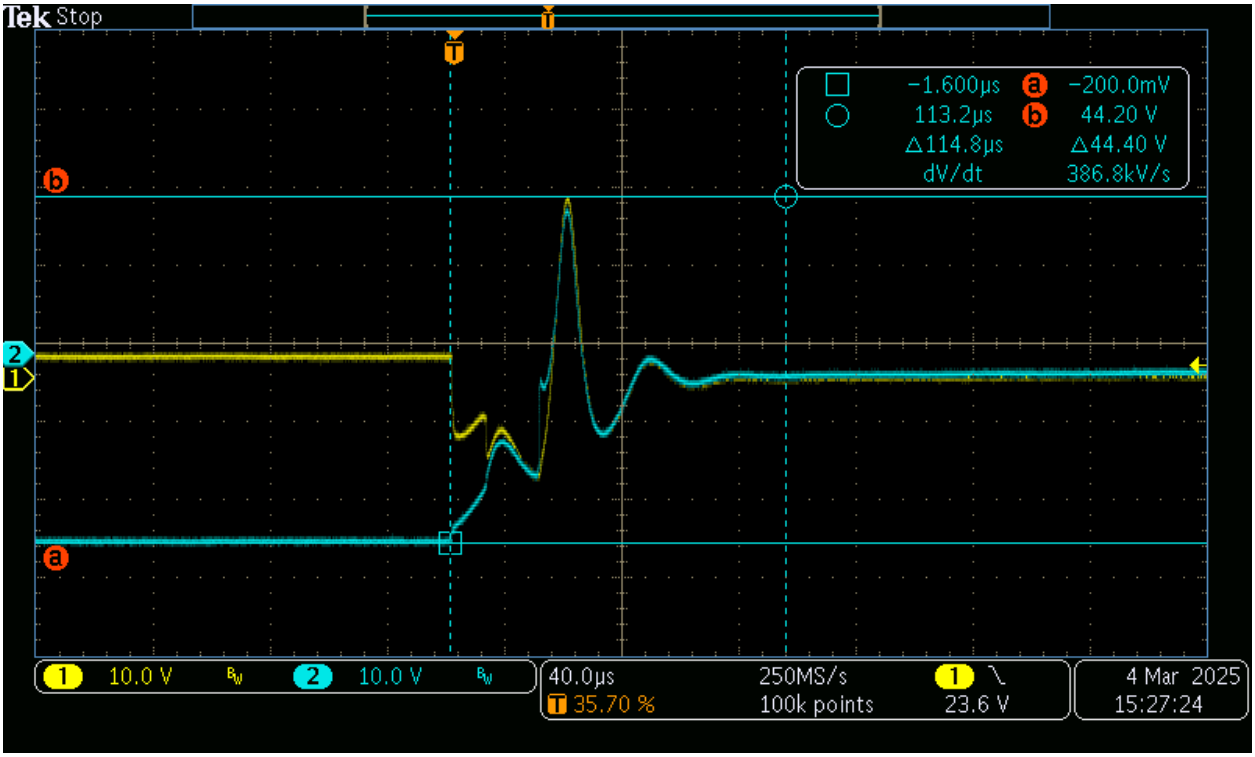

Figure 31 Waveform measured on input and output

8.2. Output feedback system test (passed in V0 verification)

Output voltage and current measurement circuits

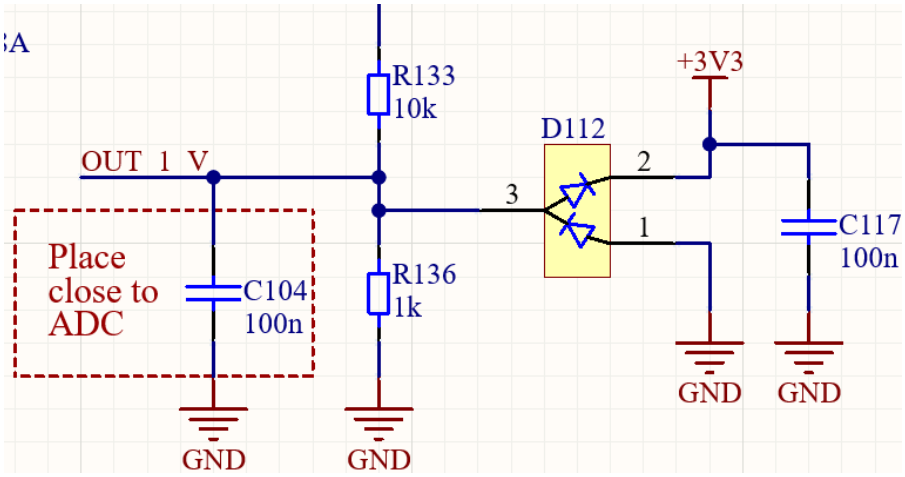

Figure 32: Output voltage measurement circuit

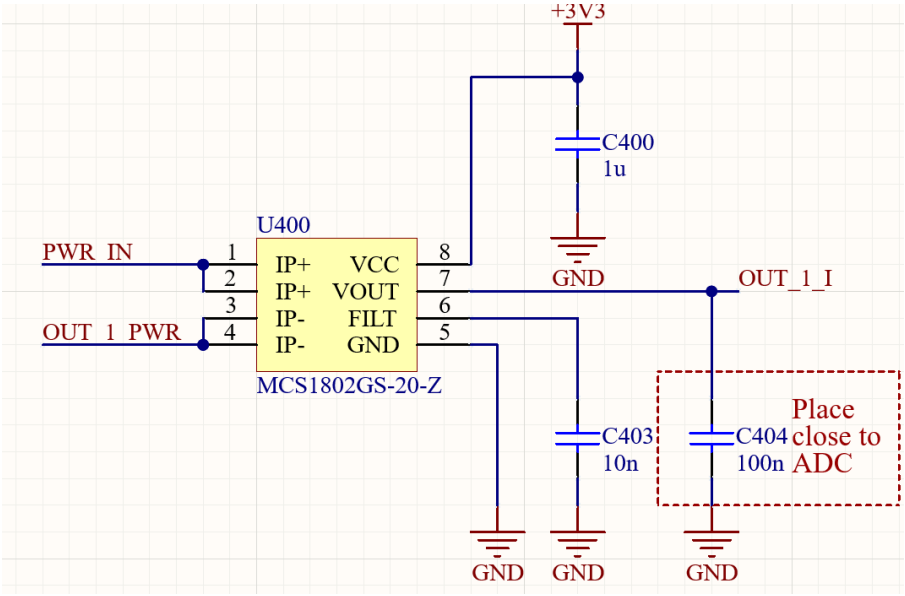

Figure 33: Output current measurement circuit

3,3 V regulator was disabled and 3,3V was supplied straight from adjustable laboratory power supply.

Output voltage was measured at ADC multiplexer input for the channel in use. Tests were performed at room temperature with unloaded output. Results are in Table 3.

Table 3: Voltage measurement circuit performance

Vin [V]	Calculated output [V]	Measured output [V]
24	2,18	2,21
28	2,55	2,58
32	2,91	2,91

Current measurement circuit output is measured at ADC multiplexer input. Tests were performed at room temperature with 28V input voltage. Results are shown in Table 4.

Table 4: Current measurement circuit performance

Iout [A]	Calculated output [V]	Measured output [V]
0	1,65	1,641
1	1,716	1,708
3	1,848	1,841
5	1,98	1,972
10	2,31	2,304
15	2,64	2,635

Result: Pass
Target voltage values and measured values show minimal deviation. The circuits perform as expected and the calculation models used to translate ADC readings to voltage values work.

8.3. Maximum load test for single output

Maximum output load will be drawn at maximum ambient temperature over 2 h period.
28V is supplied to fuse board power input. Electronic load is attached to power output. The relay will be turned on manually by supplying 3,3V to the gate resistor of the relay driving transistor as shown on Figure 28. The load current is increased to 15 A and left there for 2h. 2h is sufficient for board temperature to reach it's maximum.

Figure 34: Output load test setup

Output operation was checked before the test and again after 2h at 60 °C. Output operation is checked with 1A

Result: Passed

After 2h under maximum load under maximum temperature the 15A fuse had not blown, relay operated normally and no signs of excessive heat dissipation on PCB or connectors can be detected.

8.4. Overload test

With gradual load increase. Not implemented in SW at time of validation.

8.5. Output short circuit test

Output overcurrent and short-circuit protection. Not implemented in SW at time of validation.

8.6. Fully loaded system with added short circuit.

Draw maximum load and then add short circuit. Will input connector and busbars survive.

9. Diagnostics functions

Functions not yet implemented in SW

10. Functional tests

10.1. Buttons

Each button switches corresponding relay and appropriate LED acts accordingly.

10.2. LED’s

LED’s show on, off, and fault modes.
Check LED DATA signal shape. Oscilloscope image.