Introduction

DefSecIntel Fuse Board has serious requirements regarding current carrying capacity. The circuit has small components and copper feature size has a lower limit depending on copper thickness. Impedance controlled traces also need to be considered. This document helps manage the complexity, explain PCB technology choices and explain critical sections on the PCB design.

Würth Elektronik rules and guides will be used. Screenshots are from Basic Design Rules 2.0/04.2023.

Layer stack-up

Würth Elektronik BASIC6_ML6_1,62_35_V2.12 will be used as design basis. Nominal external copper thickness of this stack-up is 35 µm. It would be beneficial to maximize the external layer copper since this is the main interface between PCB and component traces.

Outer layers – conductor spacing

Starting foil thickness	Minimum copper thickness[1]		Nominal final thickness	Minimum conductor spacing Standard	Minimum conductor spacing Advanced	Minimum possible line width
	IPC-class 1, 2	IPC-class 3				
8,5 µm [1/4 oz.][2]	26,2 µm	31,2 µm		100 µm	75 µm	60 µm[3]
12 µm [3/8 oz.][2]	29,3 µm	34,3 µm		100 µm	80 µm	60 µm[3]
17,1 µm [1/2 oz.]	33,4 µm	38,4 µm	35 µm	120 µm	100 µm	60 µm[3]
34,3 µm [1 oz.]	47,9 µm	52,9 µm	70 µm	180 µm	160 µm	120 µm
68,6 µm [2 oz.]	78,7 µm	83,7 µm	105 µm	275 µm	225 µm	125 µm
102,9 µm [3 oz.]	108,6 µm	113,6 µm		390 µm	320 µm	150 µm

1) IPC-6012E-EN Table 3-15: External Conductior Thickness after Plating
2) Extra cost: No standard copper foil
3) Outer layers: only possible with uniform circuit layout

Figure 1: External copper thickness options for basic PCB-s

MCU LQFP package suggested footprint has 0,2mm space between solder pads. This limits the external copper thickness to 70µm nominal. IPC-class 3 should be requested for maximum final thickness.

Thicker foil is used on internal layer as well. Startin foil thickness is 68,6 µm with minimum thickness 55,7µm.

It was verified that 100Ω and 120Ω differential pairs can be constructed with these limitations. Altium layer stack impedance calculator was used.

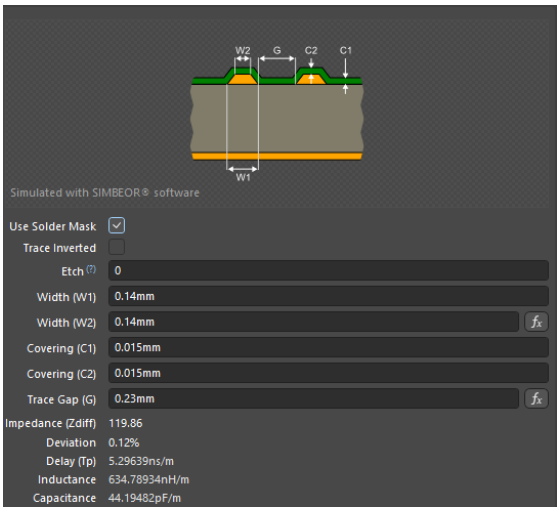


Figure 2: Transmission line for RS485

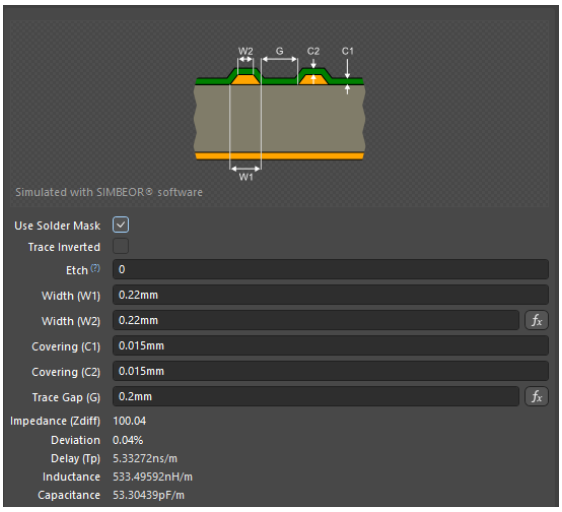


Figure 3: Transmission line for ethernet

Thinnest trace that needs to carry 15A nominal current is 1,6mm. However, this is true only on top layer. Other layers can have a wider trace.

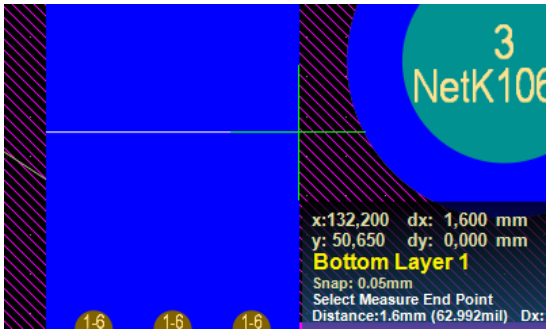


Figure 4: Thinnest line for 15A.

Multiple layers are needed to carry the current. Combining all layers the total copper thickness is shown in Table 1.

Table 1: Combined copper thickness

Layer	**Copper thickness [µm]**
Top	52,9
Inner 1	55,7
Inner 2	55,7
Inner 3	55,7
Inner 4	55,7
Bottom	52,9
Total	**328,6**

PCB Toolkit V8.05 from Saturn PCB Design, Inc is used to calculate the current capacity. 15,6 A with 40°C allowed conductor heating is the result. This is with the same trace width on all layers. In practice wider traces will be used on inner layers. It should be built so that in some areas wider inner conductor overlaps with a ground plane for better heat transfer.

This gives confidence that the PCB trances can handle the nominal current and gives reason to believe, that fault currents will be handled as well. However, behavior under fault currents must be investigated experimentally.

Layer stack is shown below.

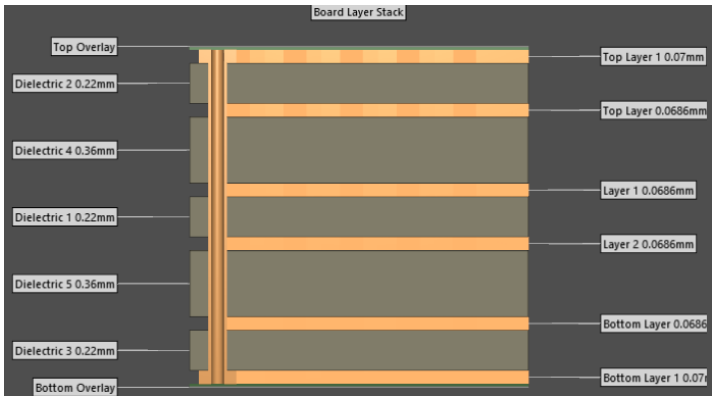


Figure 5: Layer stack

Total thickness is 1,824 mm.

Vias

Vias are basically plated through holes and the same rules apply.

Plated Through Holes						
Pad size	**Remark**	**Aspect Ratio[1]**	**Drill tool diameter**	**Finished hole diameter**	**Tolerance (Standard)**	**Copper clearance plane on inner layer without Pad**
0,60 mm	**Standard**	≤ 8:1	0,35 mm	**0,25 mm**	+0,1/-0,05 mm	≥ 0,80 mm
0,55 mm			0,30 mm	**0,20 mm**		≥ 0,75 mm
0,50 mm (Cu max. 35 µm)	Max. ca. 12 layers Max. ca. 1,80 mm PCB thickness		0,25 mm	**0,15 mm**		≥ 0,70 mm
0,45 mm (Cu max. 35 µm)	For less complex Layer stackups		0,25 mm (0,20 mm)	**0,15 mm**		≥ 0,70 mm

1) Aspect Ratio" for drill holes: Ratio of drill hole length or depth to drill hole tool diameter.
For further information, see technical delivery specification chapter 3.7.1.

Figure 6: Rules for plated through holes

Copper thickness dictates that the minimum pad size can be 0,55 mm and minimum drill tool is 0,3mm. Aspect ration can be calculated by dividing the PCB thickness 1,824 with drill too diameter. 1,824mm ÷ 0,3 mm= 6,08:1 . This is below than 8:1 required and therefore fine.

For via copper layer thicknesses Würth Elektronik Technical Delivery Specification for PCBs (October 2022) refers to IPC-6012 Table 3-4 and 3-5. From this standard it appears that plating thickness in the via for IPC-class 3 PCB is on average 25 µm. Thin areas can be 20µm. Minimum value will be used for safety.

PCB Toolkit V8.05 from Saturn PCB Design, Inc is used to calculate the via current capacity.

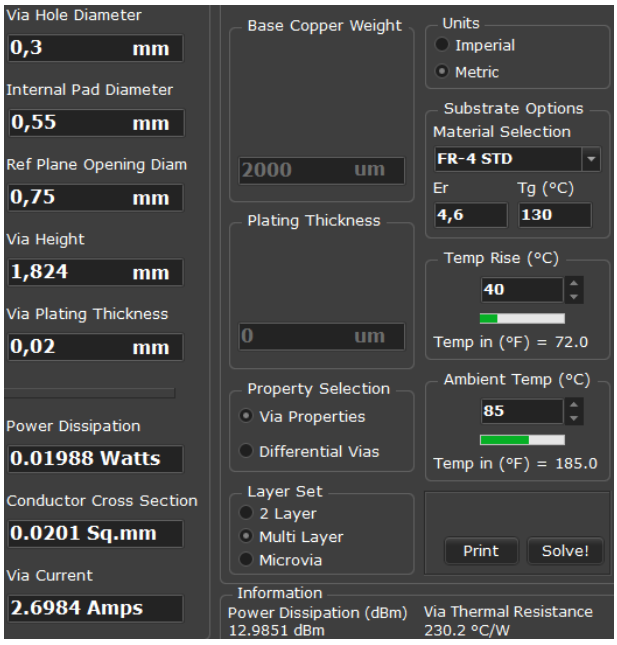


Figure 7: Via current capacity.

Again 40°C temperature rise is allowed. A minimum of 6 vias are required to connect the PCB layers sufficiently. However, since temperature induced vertical expansion is one of the main reasons for via failure overhead is desired. Where possible 7 or more vias should be used.

Traces to output terminal

For output terminals the power trace can't use all layers. The bottom layer must be reserved for copper busbar.

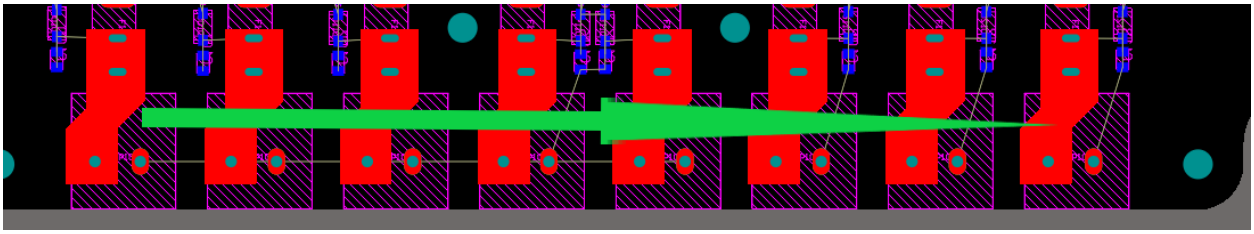


Figure 8: Return current of power outputs

Combined thickness of 5 layers is 275,7 µm. The narrowest point on the trace is 4,134 mm.

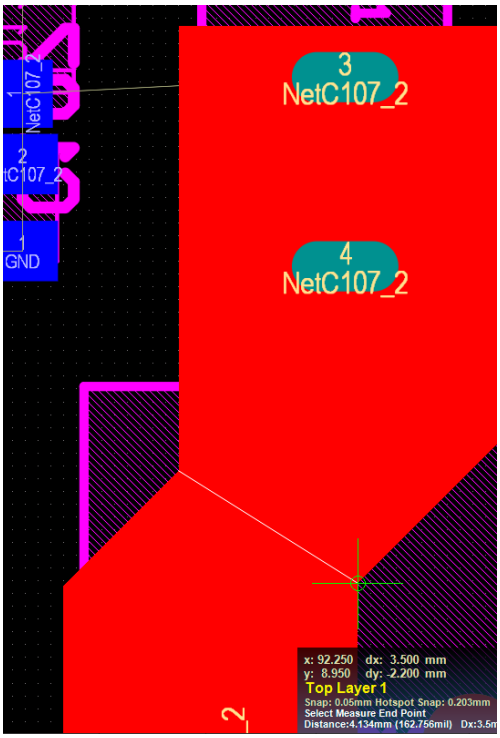
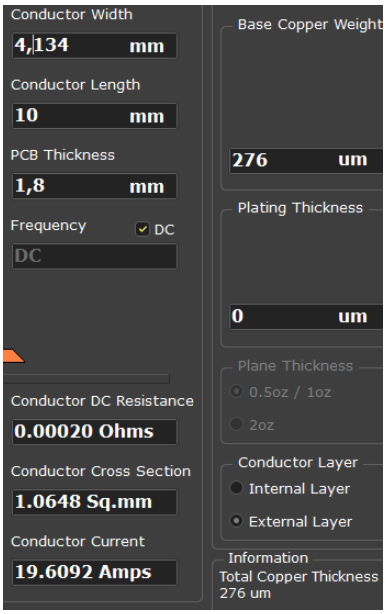


Figure 9: Output trace narrowest point

PCB Toolkit V8.05 from Saturn PCB Design, Inc was used to calculate conductor current. 19,6A is possible when maximum temperature rise allowed is 20°C.


Conductor Width
4,134 mm
Conductor Length
10 mm
PCB Thickness
1,8 mm
Frequency
DC
DC
Conductor DC Resistance
0.00020 Ohms
Conductor Cross Section
1.0648 Sq.mm
Conductor Current
19.6092 Amps
Base Copper Weight
276 um
Plating Thickness
0 um
Plane Thickness
0.5oz / 1oz
2oz
Conductor Layer
Internal Layer
External Layer
Information
Total Copper Thickness
276 um