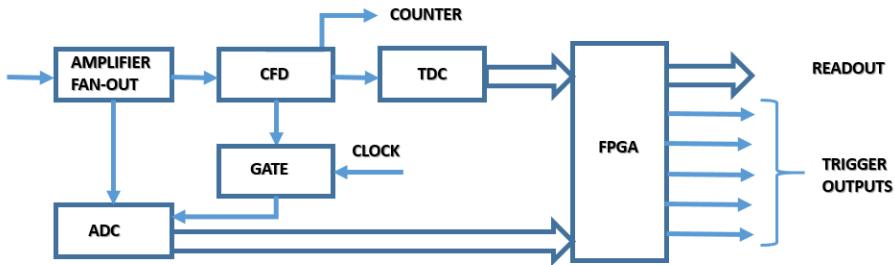


FIT Electronics

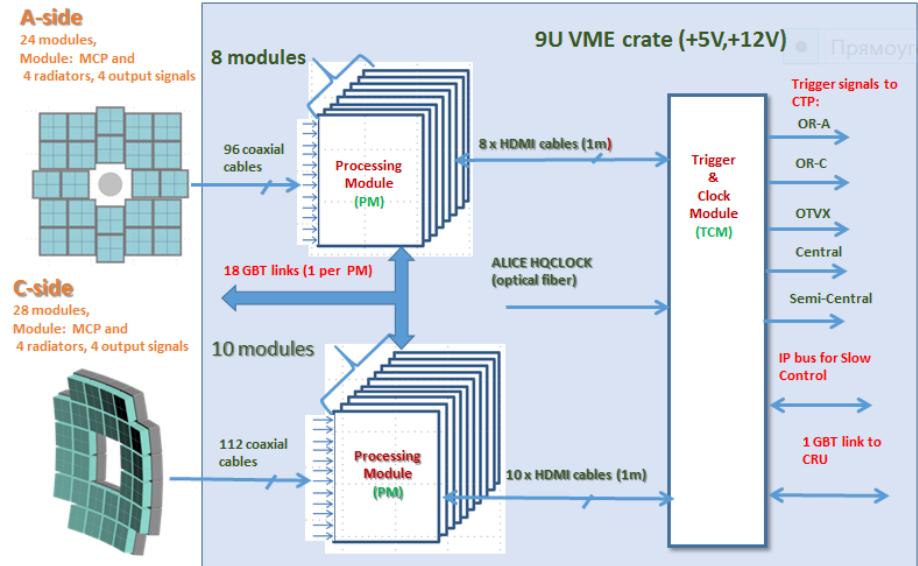
D. Serebryakov
Institute for Nuclear Research, Russian Academy
of Sciences, Moscow
on behalf of the FIT Collaboration

Production Readiness Review, December, 14, 2020

FIT electronics structure



FIT electronics uses digitized data to generate trigger signals



FT0 Example

FT0 uses Micro Channel Plates (MCP) PMTs
FV0/FDD uses Fine Mesh (FM) PMTs

Production status of the FIT electronics

1. Seven factory and one manually assembled TCMs are tested.
2. All mechanics and electronic parts for 50 PMs are purchased.
3. 35 PCBs sets for PMs are produced.
4. Shields for 50 PMs are produced.
5. Nine factory and one manually assembled PMs are tested, 7 fully calibrated.
6. All parts for remaining 14 PMs for FT0 and most parts for 12 FV0/FDD PMs are transferred to factory.
7. All CFD delay cables for FT0 modules produced.
8. Front panels design will be finally checked when first PM and TCM modules will arrive at CERN.
9. 5 9U modified Wiener crates with power supplies purchased.

Factory assembled PM module

~ 500 active components per PM

>5000 electronics parts on board

1.5 mm 6- layer impedance controlled
PCB

0.1/0.1 mm under the BGA

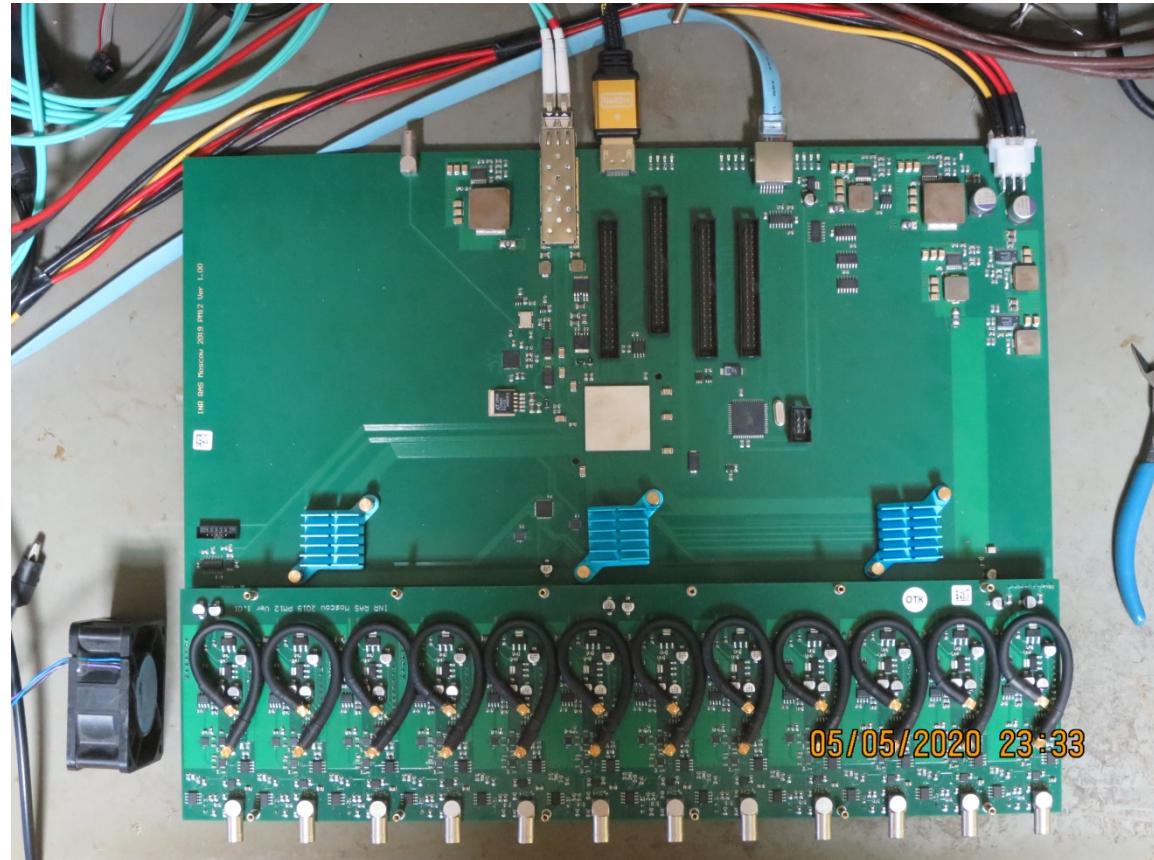
0.12/0.12 mm rest of the board

0.2 mm diff. pairs

0.48 mm/0.25 mm hole min. via

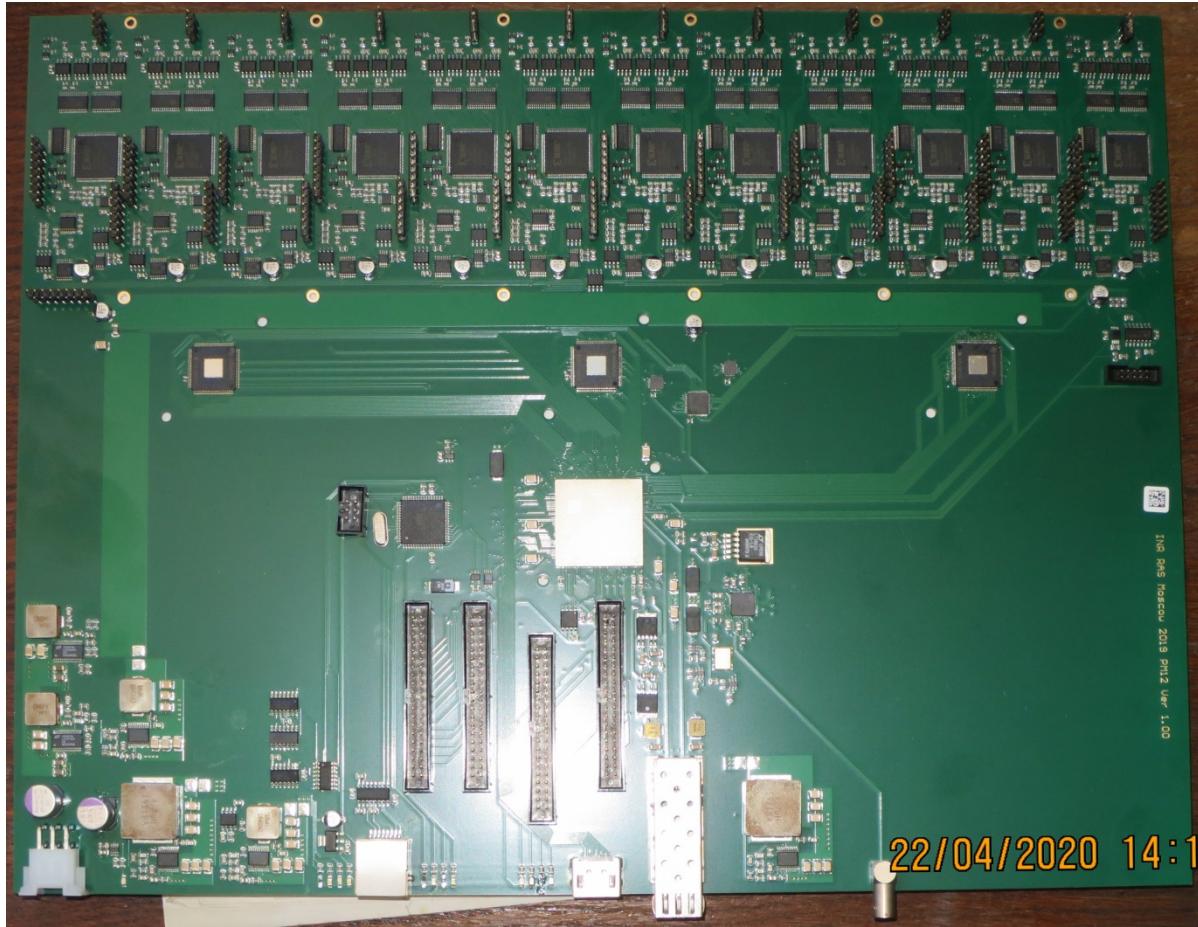
Size 362.7 x 280 mm (short 9U)

Module thickness 8 HP (40.64 mm)

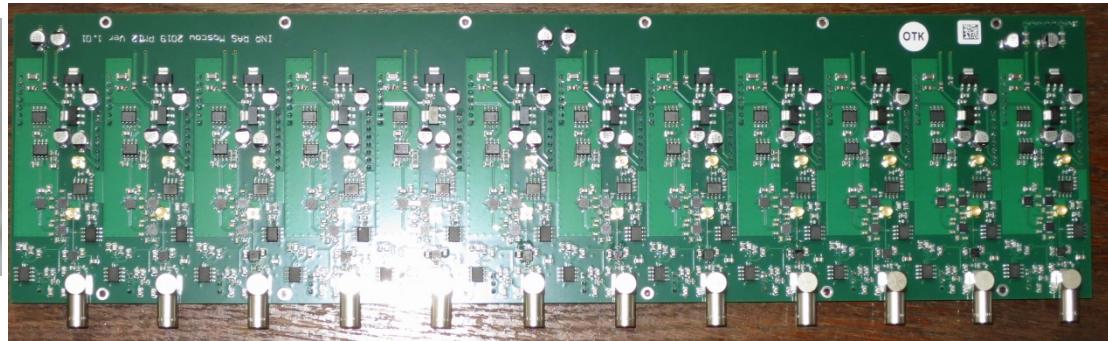


Top shielding removed, FPGA heatsink not installed

Main PCB of the PM module



Mezzanine PCB and delay cables



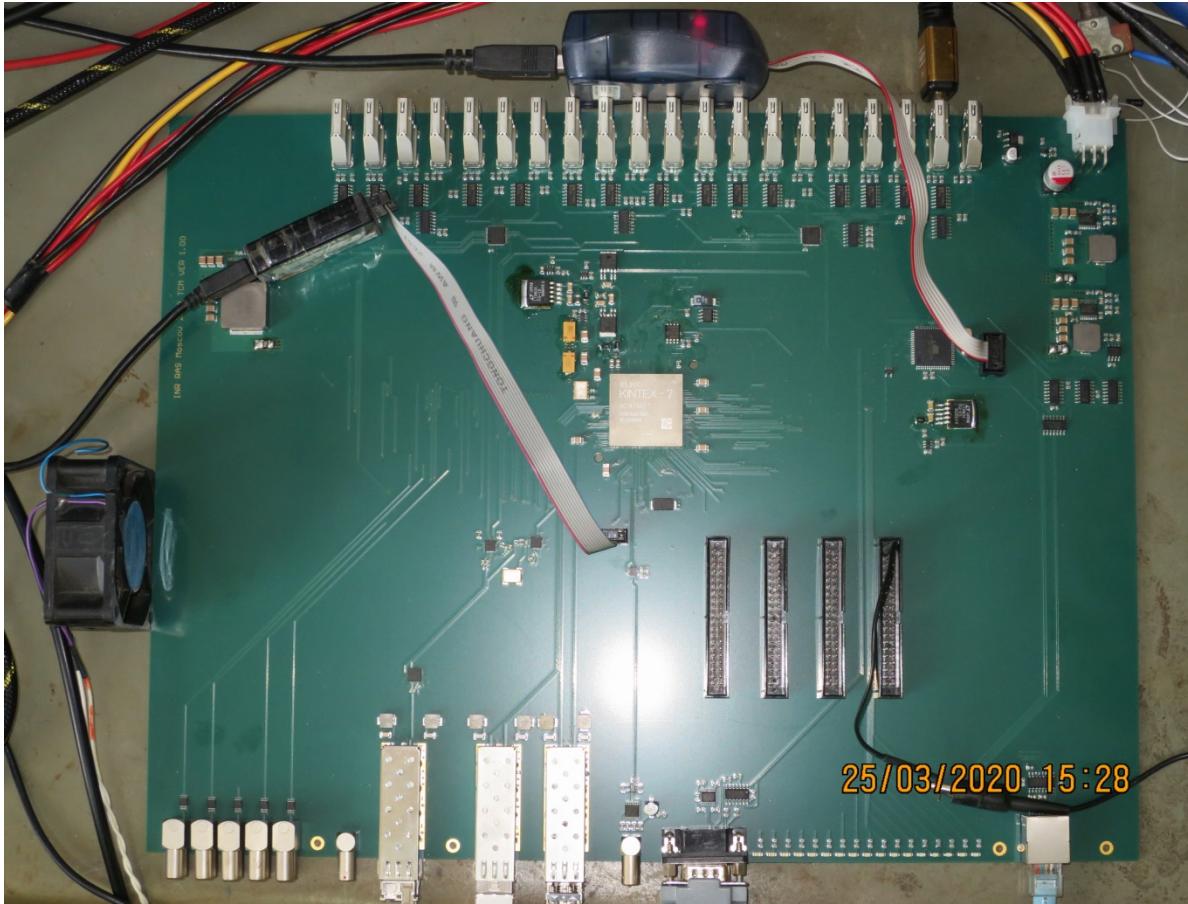
Mezzanine board has two aluminum shields from top and bottom, coated with 0,2 mm EFR10 radio absorption material.



Delay cable has 10.5 cm length for FT0 and will have ~75 cm length for FV0/FDD. It needs additional shielding, as thin 75 Ohm cables have a very simple and thin outer conductor. Additional copper braid shielding and insulation tube are placed on the cable. This eliminates the crosstalk from digital circuits, which delay cables have to cross.

With this (third) version of the mezzanine board crosstalks can be seen only when pulses with amplitudes >1 V are applied to the channel, and no signals present in the 2 neighboring channels. Then single false counts are observed in these channels. Such signal distribution can't happen in real situation.

Factory assembled TCM module



FPGA resources utilizations

DRC Violations				Timing
				Worst Negative Slack (WNS): 0.054 ns Total Negative Slack (TNS): 0 ns Number of Failing Endpoints: 0 Total Number of Endpoints: 50490 Implemented Timing Report
Utilization				Post-Synthesis Post-Implementation
				Graph Table
Resource	Utilization	Available	Utilization %	
LUT	21713	101400	21.41	
LUTRAM	66	35000	0.19	
FF	21796	202800	10.75	
BRAM	78.50	325	24.15	
DSP	3	600	0.50	
IO	275	396	69.44	
GT	2	8	25.00	
BUFG	13	32	40.63	
MMCM	4	8	50.00	
PLL	2	8	25.00	

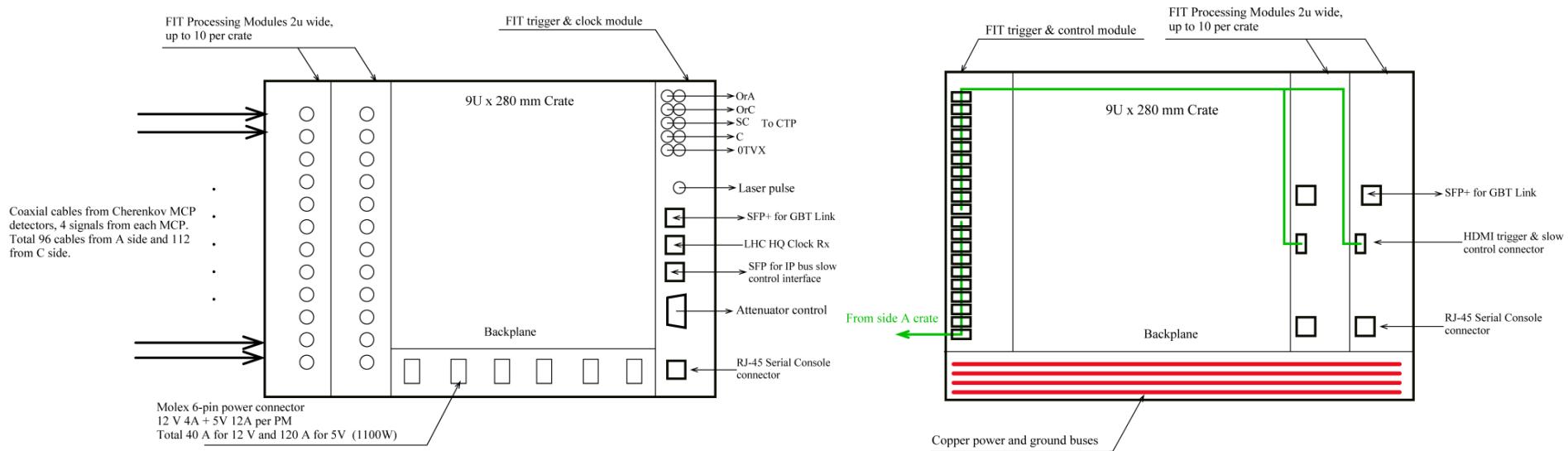
DRC Violations				Power
				Total On-Chip Power: 3.58 W Junction Temperature: 31.9 °C Thermal Margin: 68.1 °C (34.6 W) Effective 8JA: 1.9 °C/W Power supplied to off-chip devices: 0 W Confidence level: Low Implemented Power Report
Utilization				Timing
				Worst Negative Slack (WNS): 0.106 ns Total Negative Slack (TNS): 0 ns Number of Failing Endpoints: 0 Total Number of Endpoints: 42209 Implemented Timing Report
Resource	Utilization	Available	Utilization %	
LUT	14690	101400	14.49	
LUTRAM	575	35000	1.64	
FF	16359	202800	8.07	
BRAM	50	325	15.38	
DSP	12	600	2.00	
IO	278	396	70.20	
GT	1	8	12.50	
BUFG	9	32	28.13	
MMCM	4	8	50.00	
PLL	1	8	12.50	

DRC Violations				Power
				Total On-Chip Power: 2.148 W Junction Temperature: 29.1 °C Thermal Margin: 70.9 °C (36.0 W) Effective 8JA: 1.9 °C/W Power supplied to off-chip devices: 0 W Confidence level: Low Implemented Power Report
Utilization				Timing
				Worst Negative Slack (WNS): 0.106 ns Total Negative Slack (TNS): 0 ns Number of Failing Endpoints: 0 Total Number of Endpoints: 42209 Implemented Timing Report
Resource	Utilization	Available	Utilization %	
LUT	14690	101400	14.49	
LUTRAM	575	35000	1.64	
FF	16359	202800	8.07	
BRAM	50	325	15.38	
DSP	12	600	2.00	
IO	278	396	70.20	
GT	1	8	12.50	
BUFG	9	32	28.13	
MMCM	4	8	50.00	
PLL	1	8	12.50	

TCM

PM

FIT electronics crate bin



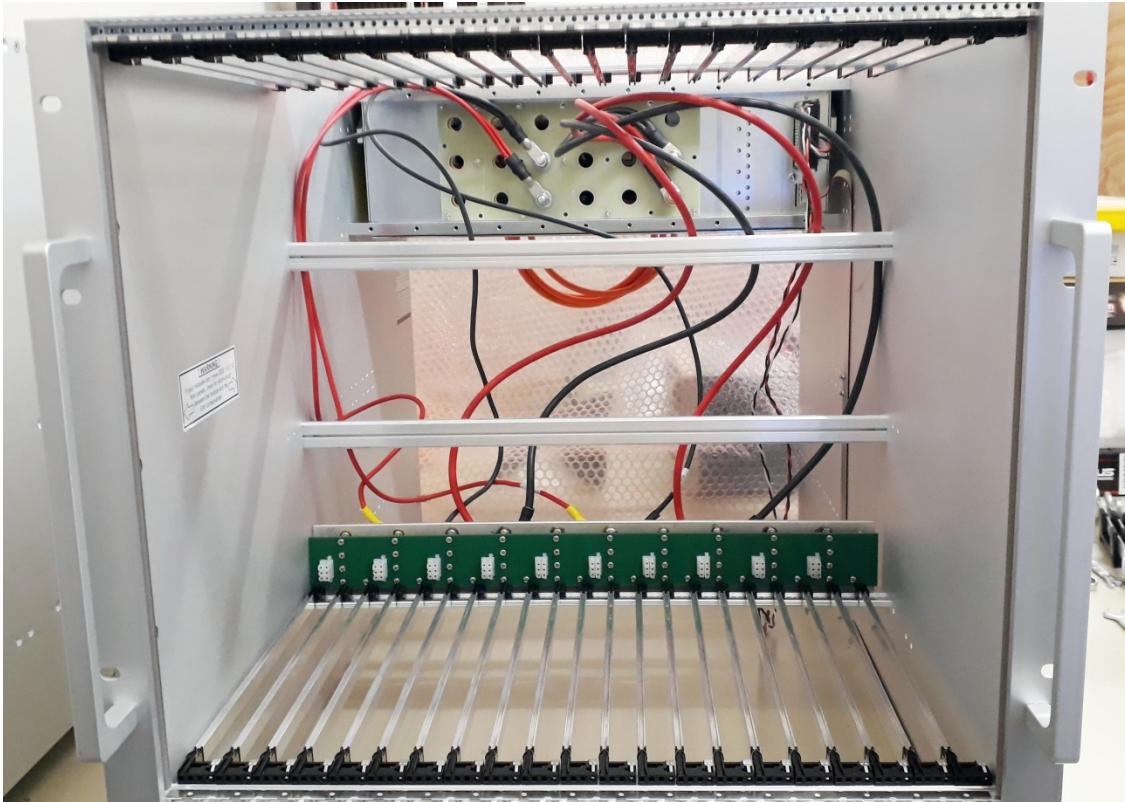
Wiener crates:

Bin 0B06.0200 11U/720mm for 21slots 9U/280mm front cards

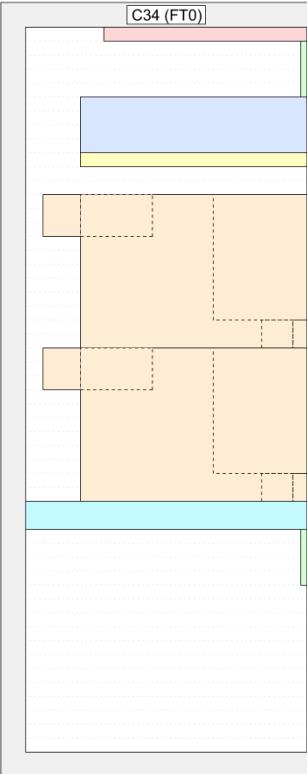
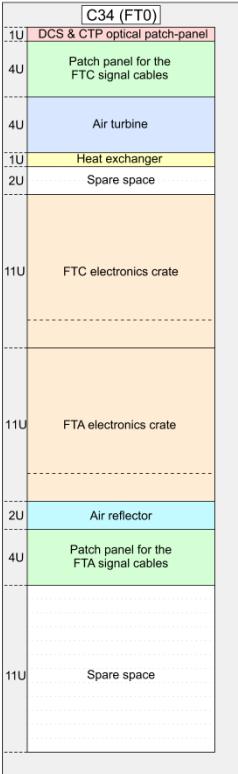
Power Supply 0P47 6U 5V/200A, 12V/40A; auto range AC input; water cooled

5 pcs. purchased and currently are at CERN

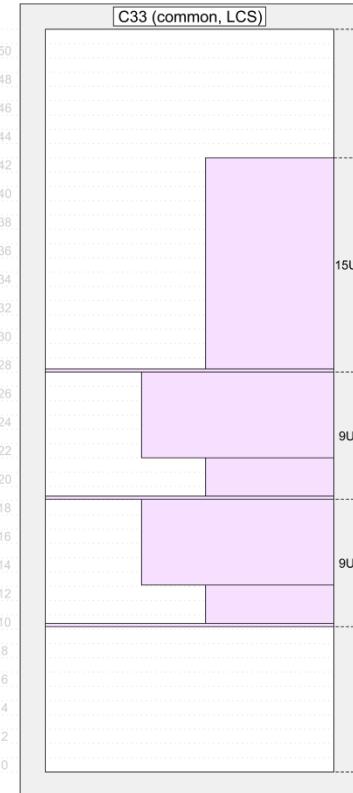
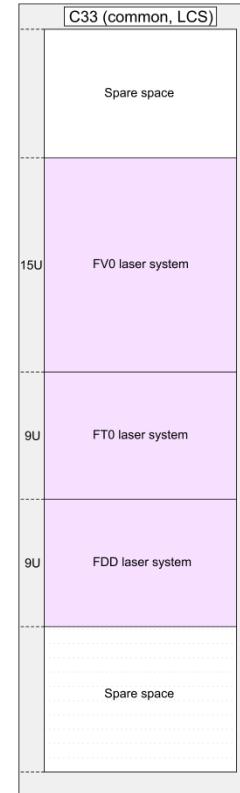
FIT electronics crate with mounted power backplane



Racks for FT0 and laser system



80 mm depth fan tray
under the front part of
the crates to improve
cooling of the PMs



Front view

Side view (from the left)

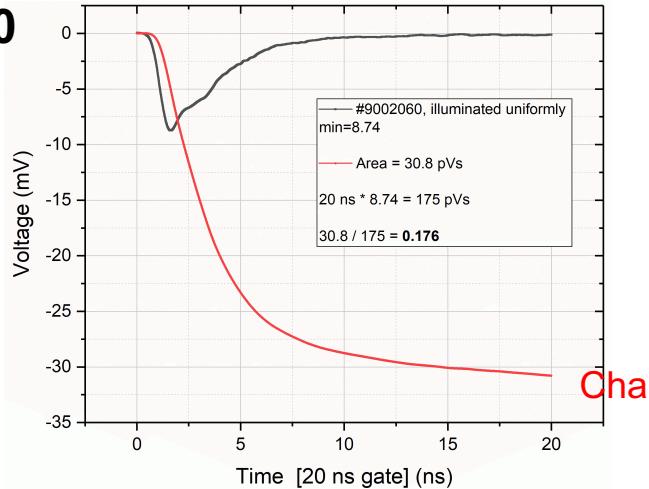
Front view

Side view (from the left)

Signal properties from detectors for FIT electronics

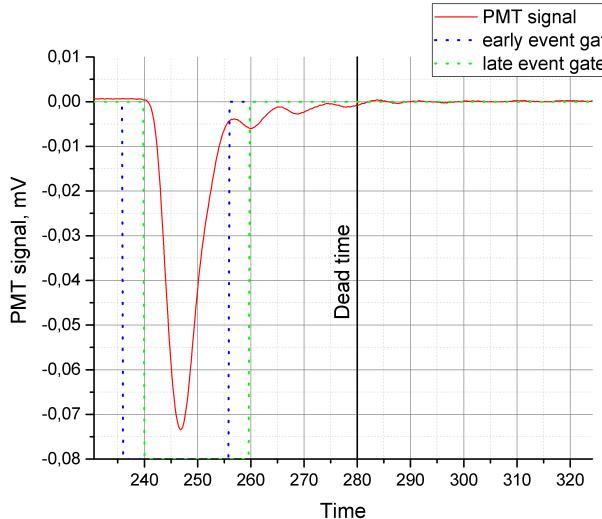
PMT gain adjusted for 1 mip pulse = 7.5 mV at the FEE inputs.

FT0



Charge

FV0
FDD?



FT0 MCP PMT signal parameters at module inputs
MCP PMT design optimized for FT0
Signal coaxial cables Ø11 mm

Pulse amplitudes 3mV – 2000 mV

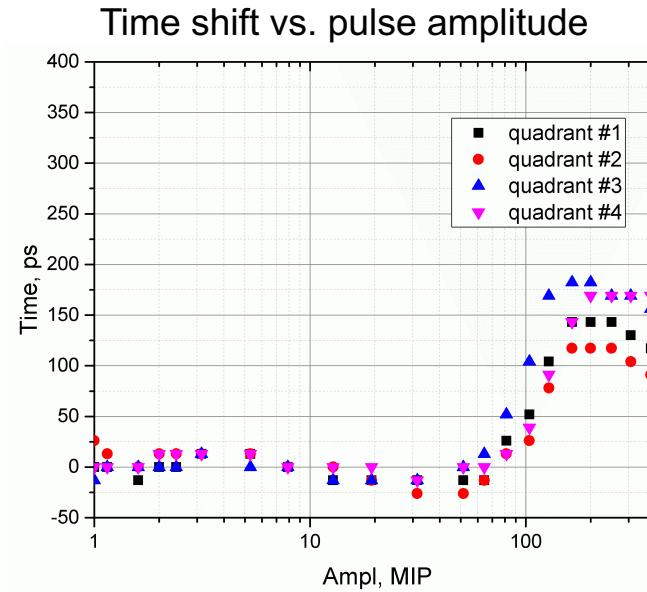
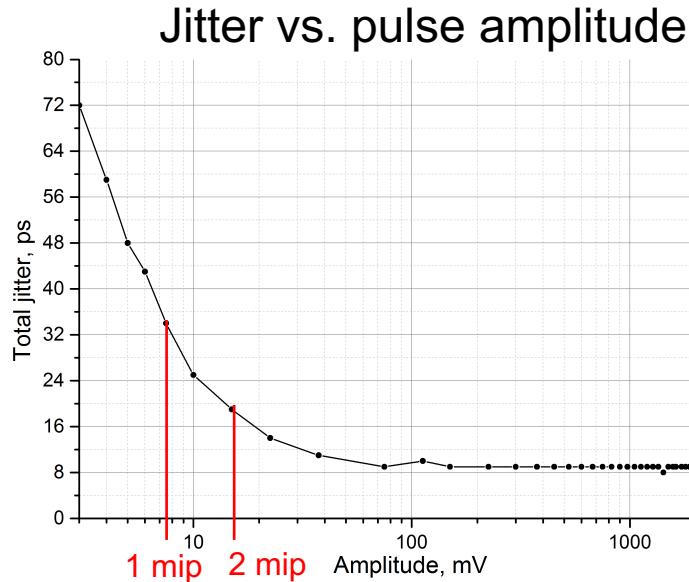
- Leading edge ~1.6 ns,
- Trailing edge ~4 ns, possible CFD dead time 14-15 ns
- Pulse charge 31 pVS/50 Ohm per 1 mip

FV0/FDD (?) Fine mesh PMT parameters at module inputs
Standard PMT voltage divider
Signal coaxial cables Ø5 mm cables

Pulse amplitudes 3mV – 5000 mV,

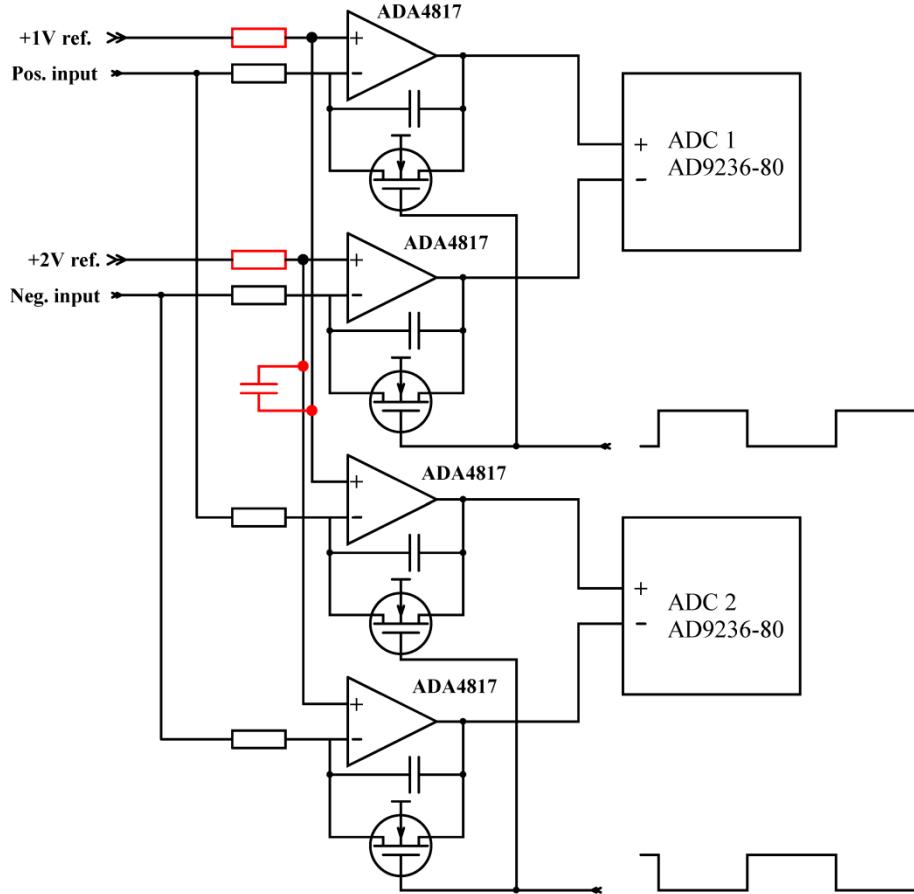
- Leading edge ~6.5 ns,
- Trailing edge ~10 ns, oscillations, possible CFD dead time ~40 ns
- Pulse charge 54 pVS/50 Ohm per 1 mip

CFD timing parameters (tested with MCP PMT, cables and laser)



Slope of the CFD delay vs. amplitude (right) for the signals below ~ 100 mV is controlled by “CFD Zero” setting. Optimal adjustment is when time for 10 mV signal is shifted $\sim 20\text{-}30$ ps later than for 100 mV signal. This adjustment is stable over temperature. For signal over 500 mV, amplifier output slew rate limitation shifts the time, maximum for 170 ps. Signals higher than ~ 750 mV will be excluded from timing triggers calculations, and will be corrected in the off-line data.

Charge measurement circuits



Fully differential analog path significantly reduces the baseline drift and noise caused by charge injection in integration capacitor through the transistors gates.

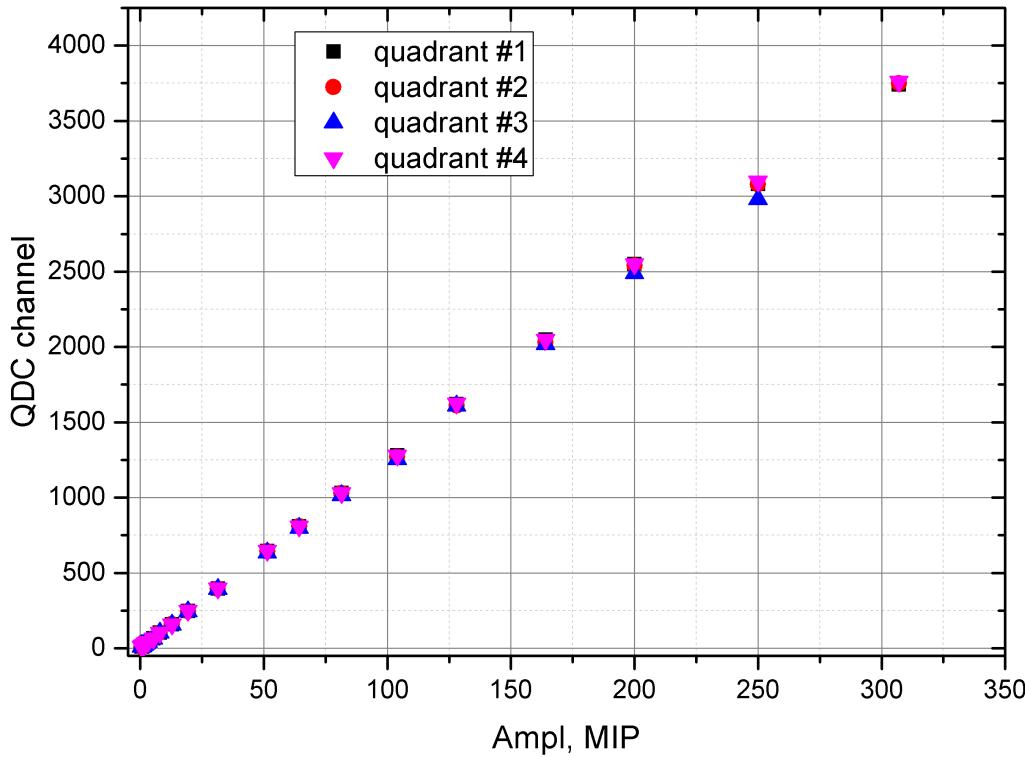
ADC works at 80 MHz to reduce data latency.
Noise is about 2 ADC LSBs.

Elements, added after the PCBs were produced, are shown in red.

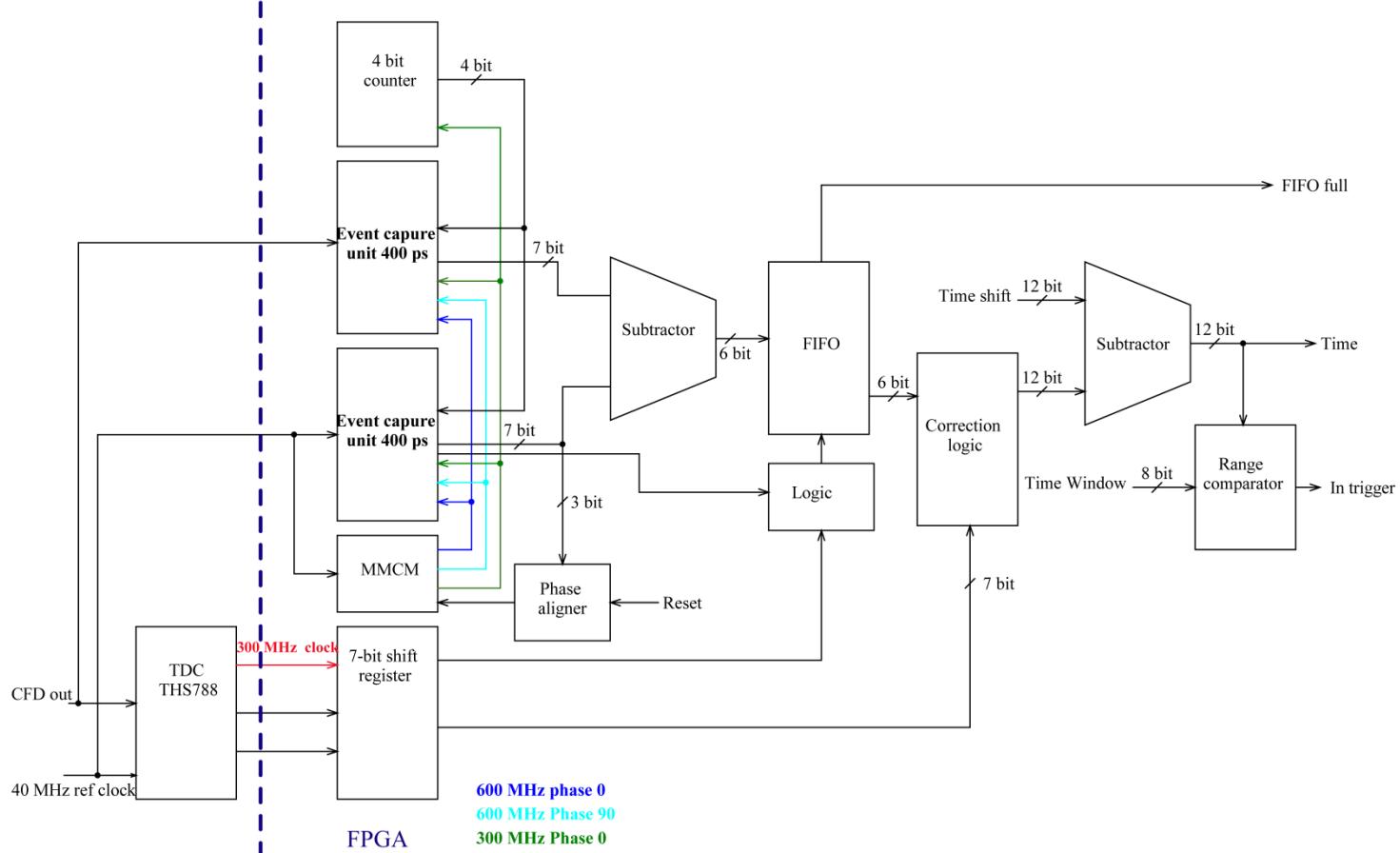
SST213 transistors has a large spread of cut-off voltage. Ones with high values are not suitable for integrators. Approximately 5% of the transistors need to be swapped. We decide not to sort them before factory assembling of the PCBs, but replace during testing, as they can easily be detected by noise level and baseline position.

Baseline is automatically measured every 25 us, checking that there were no events in the channel 3 BC before and 1 BC after the measurement. Values are averaged and subtracted from results in FPGA. Events with amplitudes below CFD threshold creates error less than 1 LSB.

Linearity of the charge measurement circuits

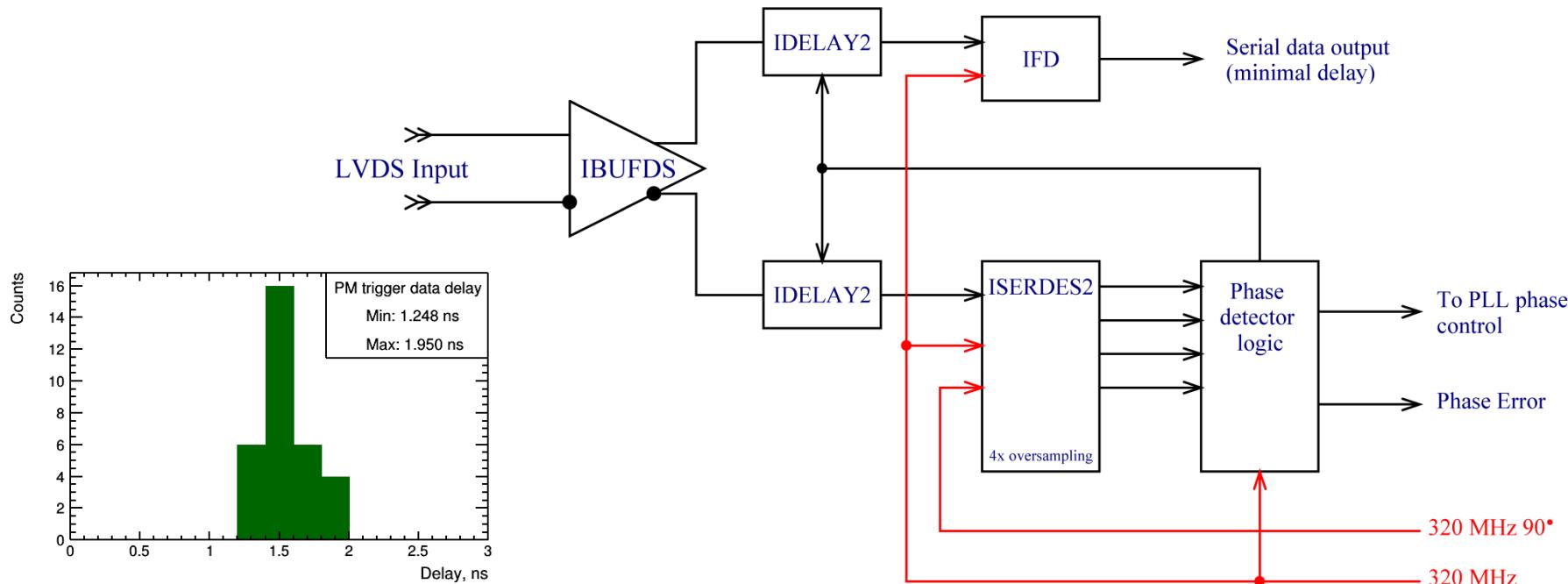


FPGA -TDC for upper 5 bits of the result



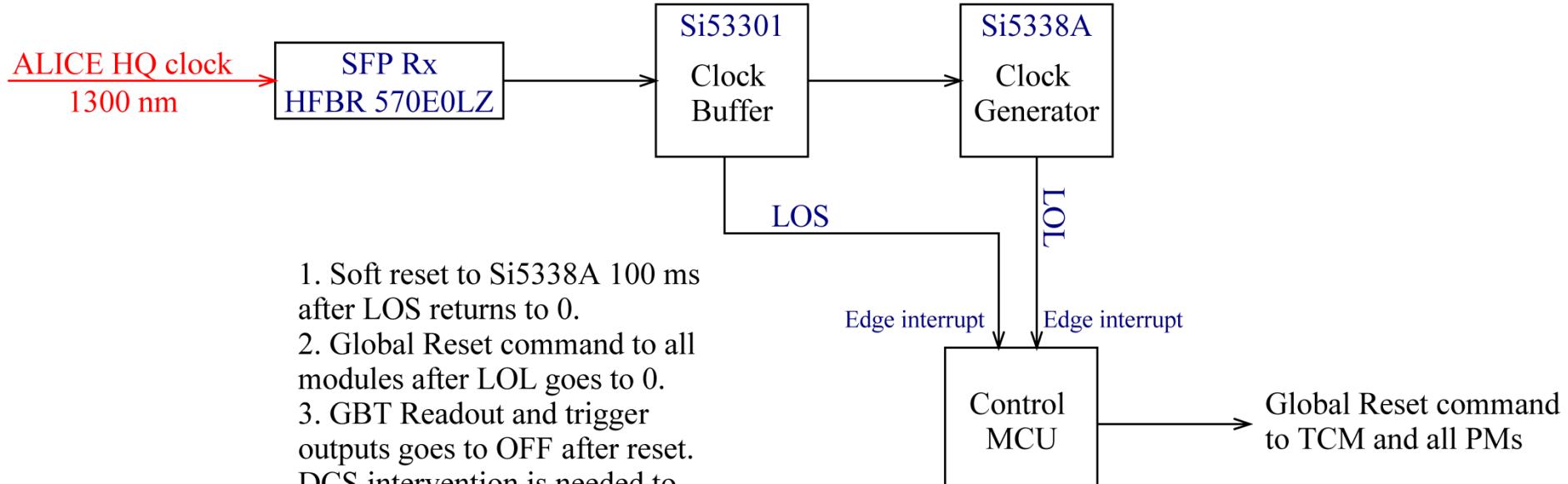
Counter, MMCM, phase aligner and Reference capture unit are common for all 4 channel of the TDC

TCM trigger data line receivers



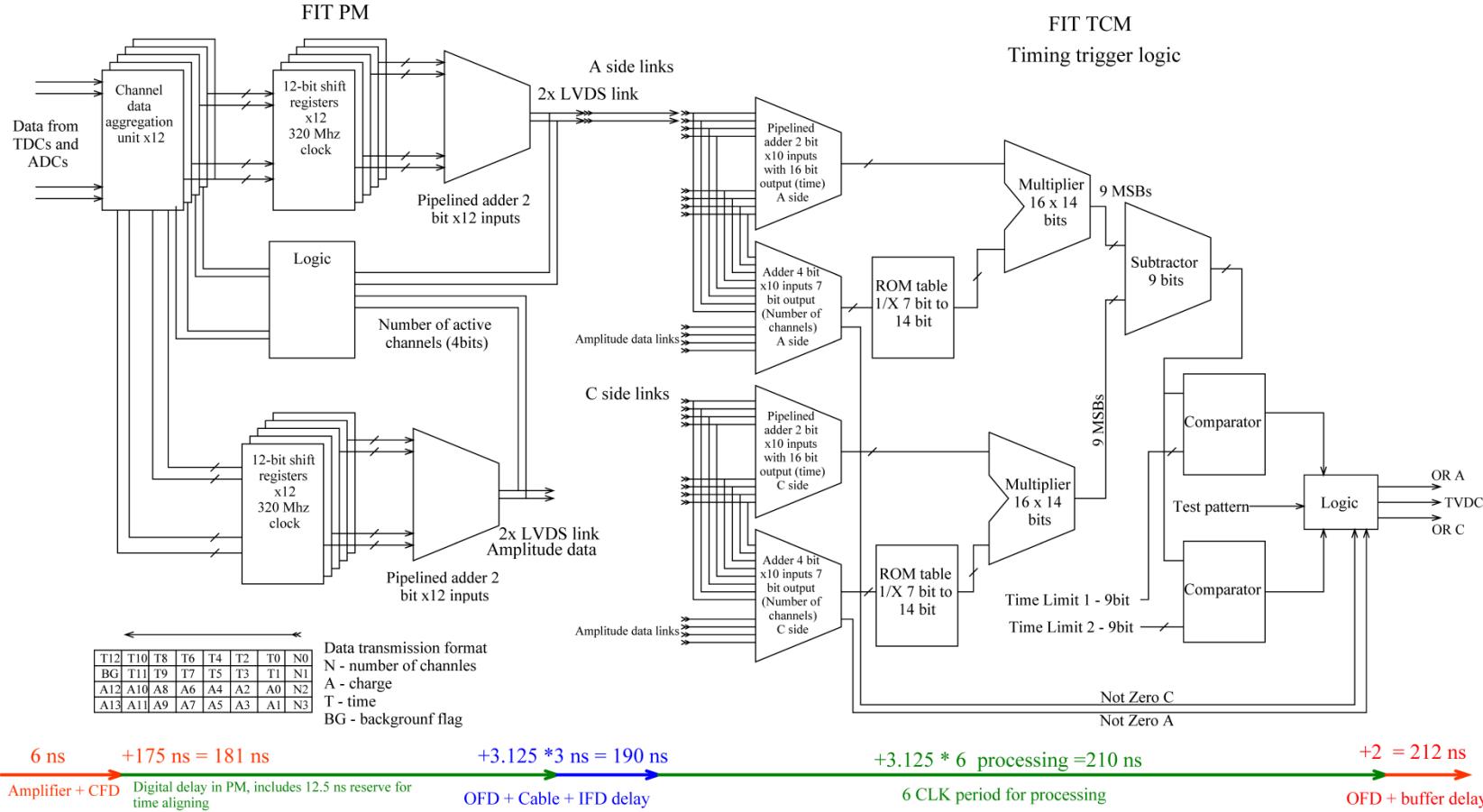
TCM has 2 groups by 10 connectors, each connector has 4 LVDS lines. All 80 lines in group must be phase aligned to master 320 MHz clock. To provide this, PLL phase control of the master clock and programmable delay in each clock line is used. The maximum adjustable range is 2.5 ns. Measured maximum delay difference between links on TCM PCB is ~1.3 ns, for different PMs - ~0.7 ns. This allows to connect any PM to any TCM input. Adding ODELAY2 elements to PMs will allow to cover any delay spread, but will increase total processing delay by 3 – 5 ns.

FIT Clock connection

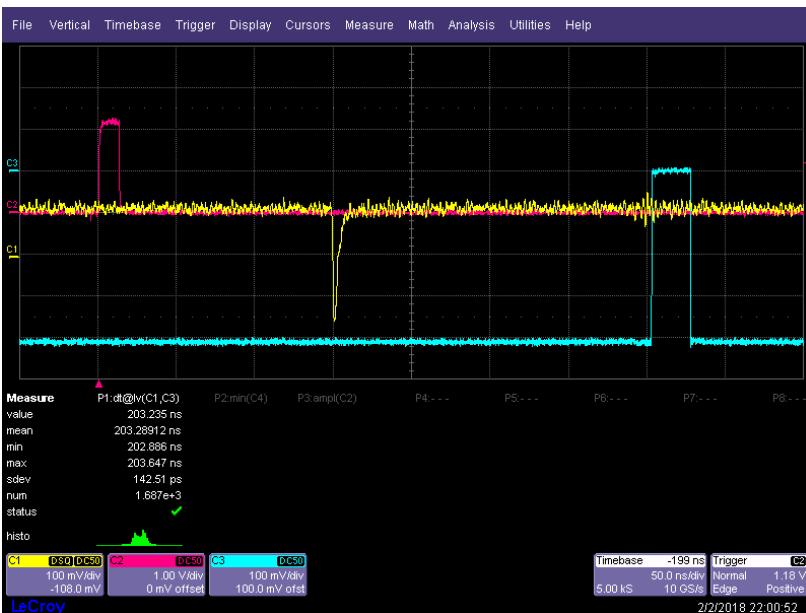


In case of the external clock loss, system automatically switches to its internal clock source. TCM's IP-bus and PM SPI slow-control subsystems is always clocked from local clock generator.

Trigger data processing in the PM and TCM for FT0

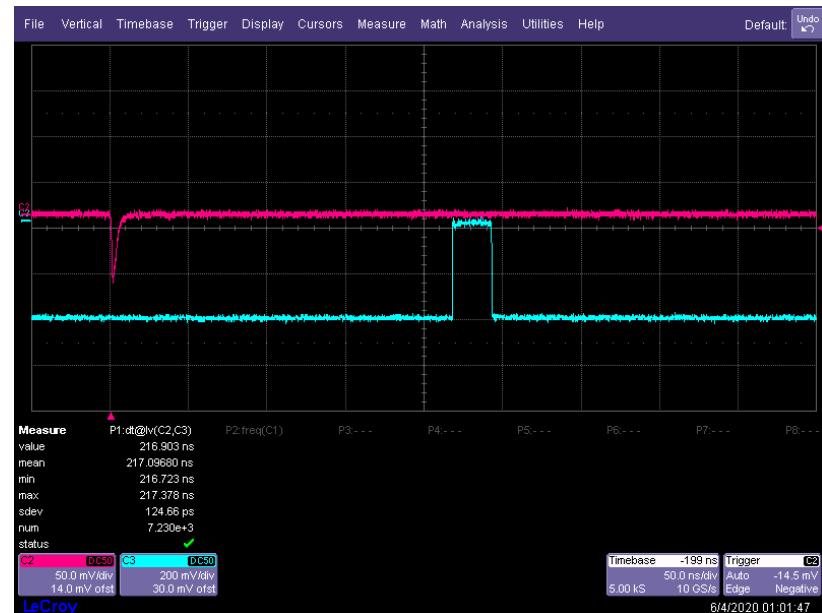


PM 4 – TCM prototypes delay and final delay tests.



Done 02.02.2018.

Purple – laser pulse, Yellow – Analog input, Blue – trigger output.
Setup had equal cable delays from PCB to scope in both channels
Trigger delay is 203.5 ns.



Done 04.06.2020.

Purple – Analog input, Blue – trigger output.
MCP cable directly connected to scope, LVDS cable has 5 ns delay. This delay must be subtracted from result.
Final trigger delay is 212 ns.

FIT FT0 LM trigger Latency

- FIT Time-of-Flight
 - A-side: 11 ns (~3,3 m between IP and FIT-A)
 - C-side: 2.6 ns (~0,8 m between IP and FIT-C).
- PMT delay
 - MCP-PMT ~1 ns,

Cabling from detector to electronics

A-side: 2.5m (2,6mm cable -4,8ns/m) +31 m (11mm cable- 4,1 ns/m) + 1 m (2,6mm cable -4,8ns/m) =143,9 ns

C-side: 5.5m (2,6mm cable -4,8ns/m) +28 m (11mm cable- 4,1 ns/m) + 1 m (2,6mm cable -4,8ns/m) =146 ns

A-Side time to electronics – 154.9 ns, C-side – 148.6 ns. Additional delay 6.2 ns to A-side cabling is needed.
(Electronics needs that side C signals comes at least 12.5 ns earlier than ones from side A).

- Cabling to CTP 29.5 ns (7 m path with 5 mm cables) + 212 ns processing time

Total $11 + 1 + 143,9 + 6,2 + 212 + 29,5 = 403,6$ ns The contingency is 21.4 ns

Legend: 5.5m – cables already placed, 31 m - preliminary

FIT FV0 LM trigger Latency

- FIT Time-of-Flight
11 ns + 6 ns (fiber delays) = 17 ns (FV0 has additional delay in optical fibers)
- PMT delay
FM-PMT ~ 10 ns + 4 ns CFD delay cable

Cabling from detector to electronics

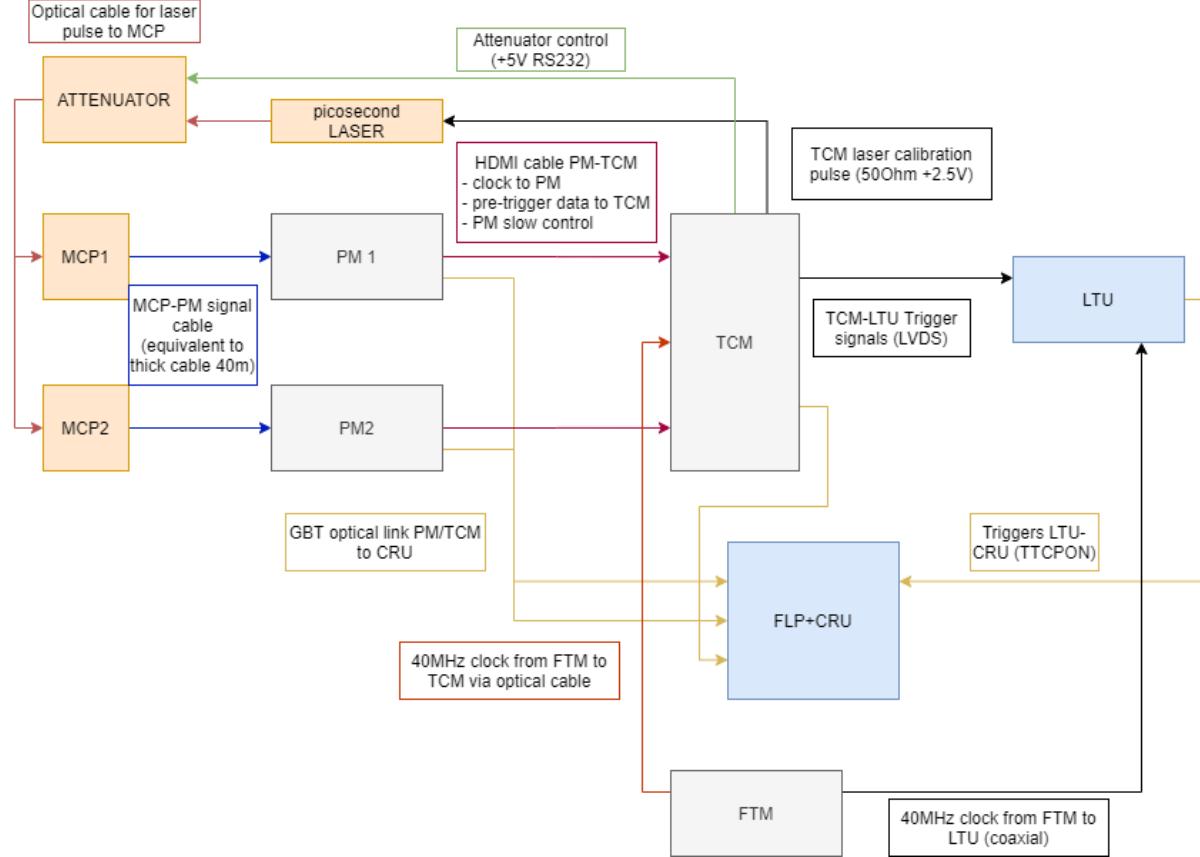
$$\underline{0,35 \text{ m}} \text{ (PMT cable } 4,8\text{ns/m)} + \underline{36,5 \text{ m}} \text{ (5mm cable- } 4,2 \text{ ns)} = 154,7 \text{ ns}$$

- Cabling to CTP 29.5 ns (7 m path with 5 mm cables) + 212 ns processing time
Total $17 + 14 + 154,7 + 212 + 29,5 = 427,2 \text{ ns}$ The contingency is -2.2 ns (With FT0 firmware)
with special FV0 firmware the delay is expected around 421 ns.

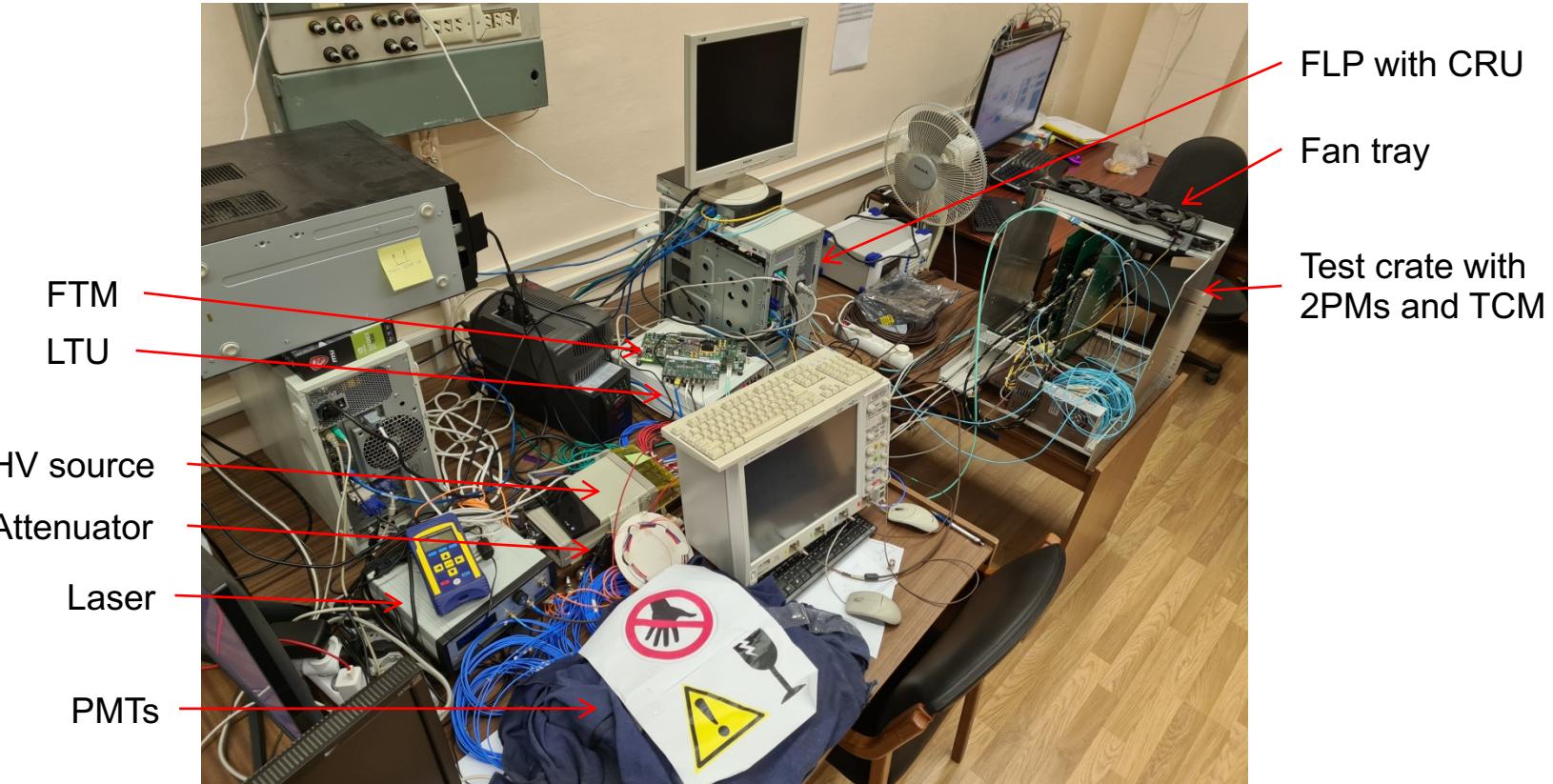
Legend: 5.5m – cables already placed, 31 m - preliminary

Test setup at INR – block diagram

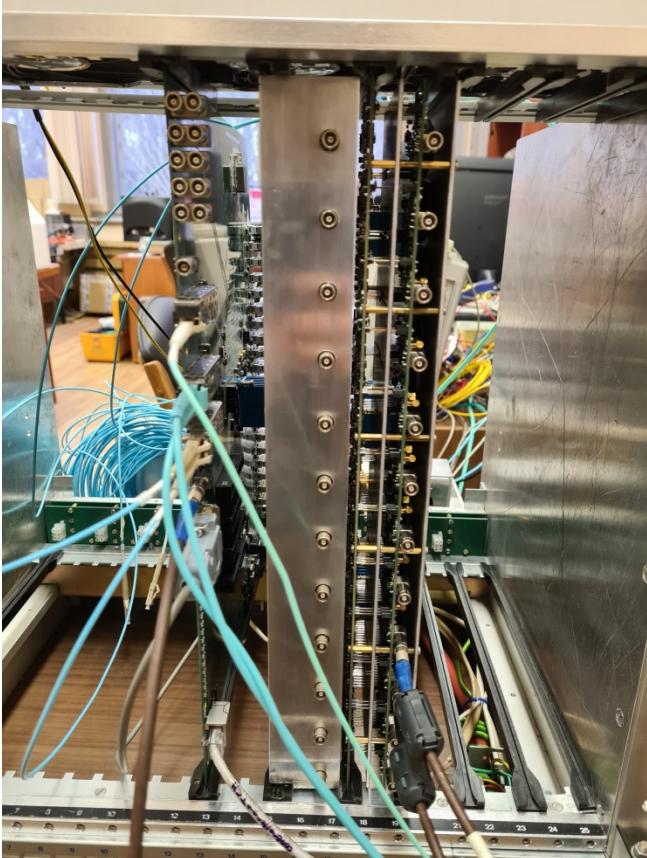
- Clock setup
 - LHC HQ clock (40MHz) is generated in FTM by Si5338
 - The clock is distributed to CRU via LTU
 - The clock is distributed to TCM via optical connection (final setup)
- Data path:
 - Attenuated laser pulse illuminate MCP
 - Analog pulse from MCP is digitized in PMs
 - Data from PMs is sent to CRU via GBT
 - Pre-trigger data is sent to TCM via HDMI
 - TCM generate trigger and send trigger data to CRU via GBT
- Trigger system
 1. LTU generate pre-pulse trigger (0x20)
 2. TCM generate laser pulse for each pre-pulse trigger
 3. Event from laser pulse digitized in PM/TCM
 4. TCM generate trigger (vertex, ORA, ORC) signal to LTU (LVDS)
 5. LTU generate physics trigger (0x10)
 6. PM/TCM receive physics trigger and select digitized event (trigger readout tested)



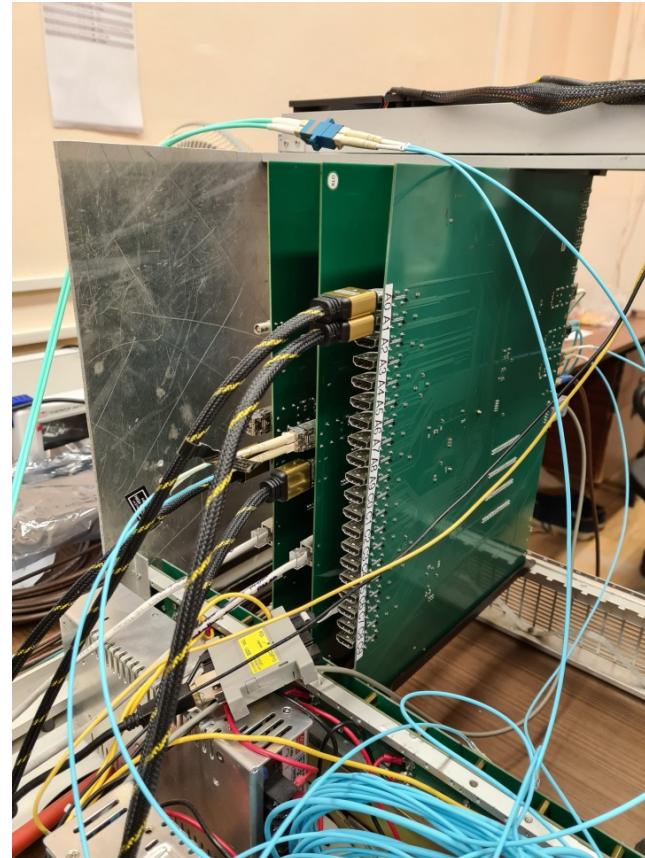
Test setup at INR



PM and TCM modules in crate



Front view



Back view

Initial tests for new boards

The first stage of testing performed on the workplace, equipped with different optical and soldering equipment to fix all possible defects except FPGA soldering (X-ray inspection of the board and FPGA performed at factory).

- Each board comes from factory with unsoldered shunts in main power rails. At first step power convertors are checked, including waveforms on the coil. After that, the shunt resistors are soldered one-by-one with testing the voltages and currents after each power rail is connected to circuitry.
- On the next step, FPGA configuration flash is programmed via JTAG and main digital tests are performed – clocks checks, GBT link, IP-bus connection and logic outputs for TCM. Each HDMI connector functionality is fully tested – trigger data transmission, slow control interface and clock.
- After that, the mezzanine board is attached to the PM and voltages on the control points are checked (~180 measurements per board). Also, the correctness of ADC clock phase control circuits in each channel are checked by scope.
- Integrator noise and offsets are checked, transistors with high threshold levels are swapped.
- On the last step, the delays cables are installed to activate the Constant Fraction Discriminators and initial threshold level settings and CFD functionality test are performed with the signal generator.
- After that, the board is mounted in the test crate and calibration procedures are performed.

The boards which were already tested (16) had from zero to three defects, which is acceptable for us. Defects are non repetitive, from missing resistor and unsoldered pin to rotated comparator with CSP case. Mounting the resistors and capacitors to fix integrator noise are also done at this workplace.

Calibration of the new boards

0. Prerequisites

- Find the laser phase and set corresponding ADC_DELAY for all channels
- set all TIME_ALIGN = 0 [0..2048] (in case of first setup)
- set all CFD_ZERO = 0 [-500..500] (in case of first setup)

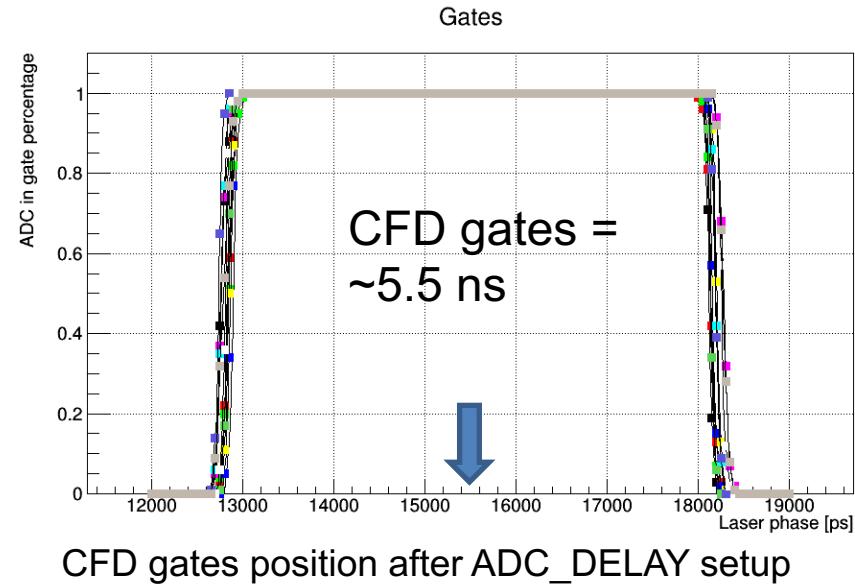
Note: calibration is done with one MCP output on channel-by-channel basis to keep test conditions equal for all channels.

1. Time measurement circuits:

- CFD level threshold calibration
- TDC calibration
- CFD zero calibration

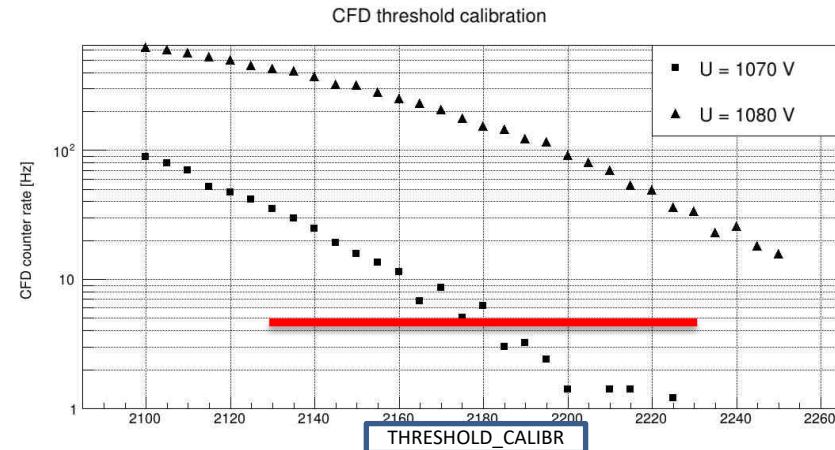
2. Charge measurement circuits:

- ADC range correction



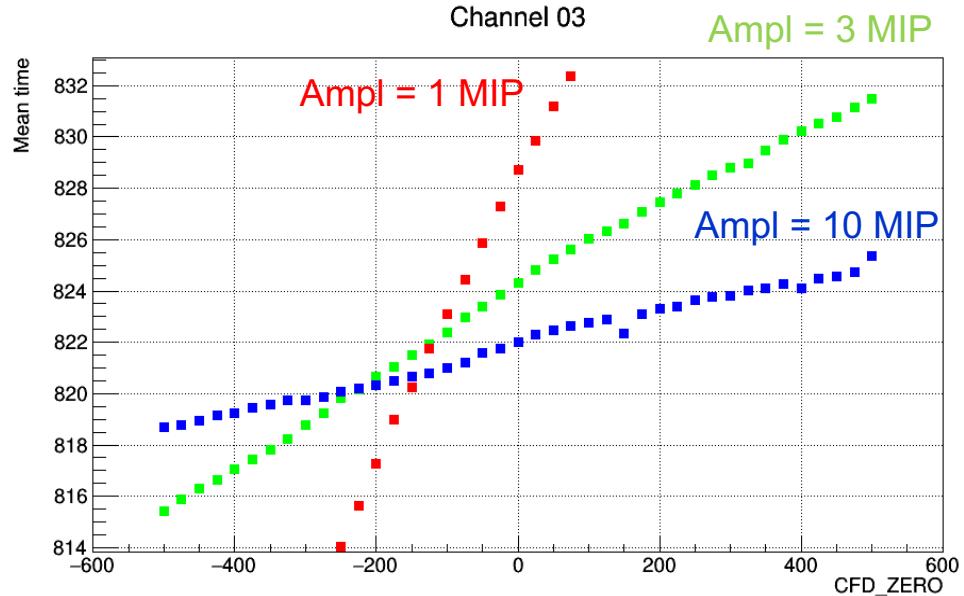
CFD threshold calibration

- Laser phase is set to be out of ADC gate, frequency = 1KHz
- Input signal amplitude is set to be equal 3mV with lower MCP gain and increased light intensity to decrease amplitude spread. Pulse amplitude is checked with scope.
- Laser rate is set to 1 kHz, CFD_THRESHOLD = 300 (3 mV).
- Calibrating threshold:
4 scans (CFD counter rate vs THRESHOLD_CALIBR):
 - Decreased HV and step =500, select point
 - Decreases HV and step =50, select point
 - Decreased HV and step =5
 - A Little higher HV, step =5, same range
 - Find point where CFD counter rate is 1-3 Hz



CFD zero calibration

- Laser phase is set to be in CFD gate.
- 3 scans performed (mean time vs CFD_ZERO [-500..500]):
 - Amplitude 1 MIP, full range scan
 - Amplitude 3 MIP, full range scan
 - Amplitude 10 MIP full range scan
- Find an area of intersection and select a point



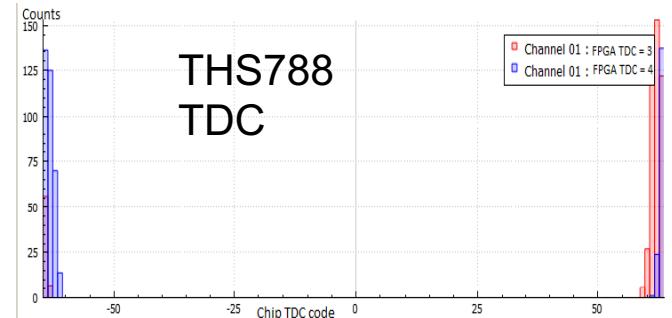
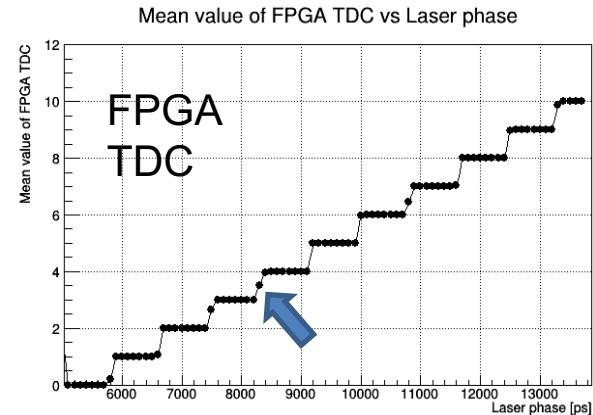
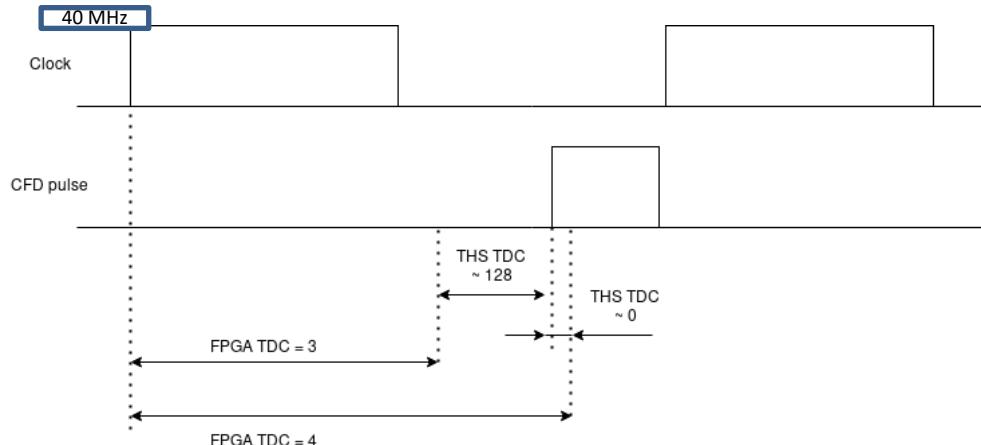
TDC calibration

Goal is to synchronize two TDCs: FPGA-based TDC ("coarse") and THS788 TDC ("fine")

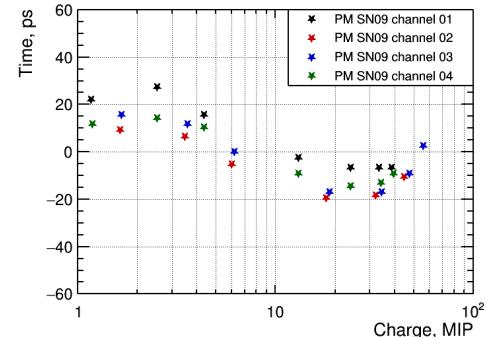
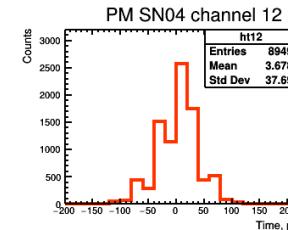
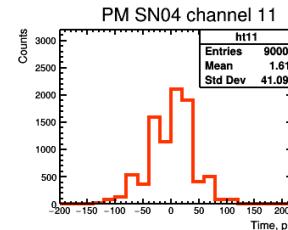
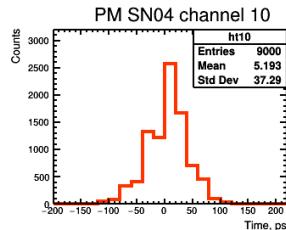
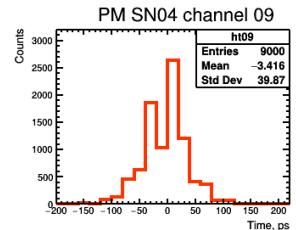
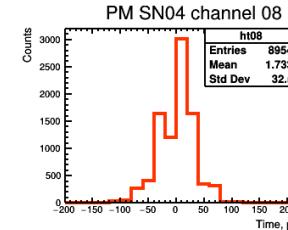
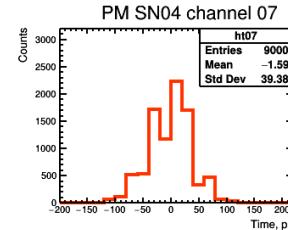
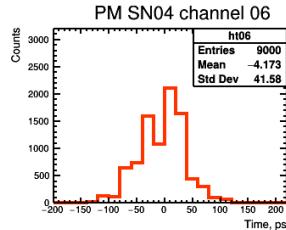
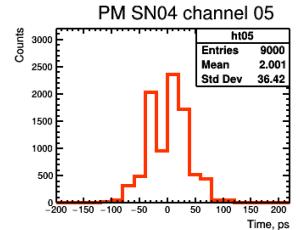
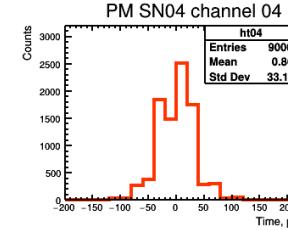
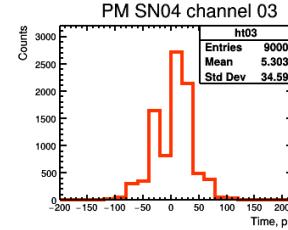
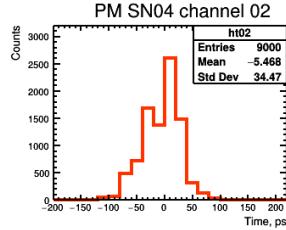
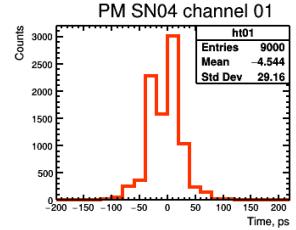
- Set the laser phase to the point, where "coarse" TDC switches between 3 and 4 by scanning laser phase.
- Find the calibration value:

7 first bit of "fine" TDC should be close to 0 or 128

Calibration value is stored in PM EEPROM, it is not accessible from DCS.

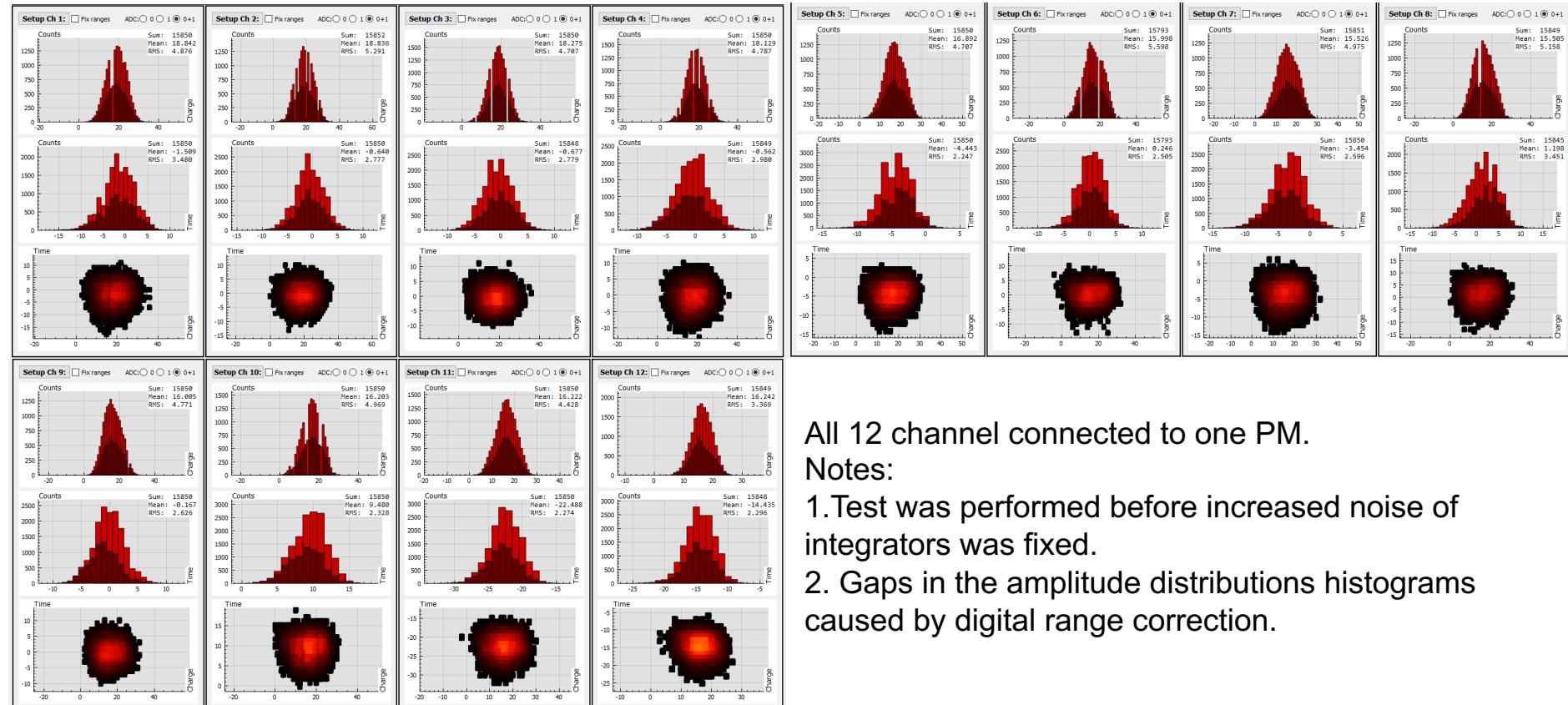


Final calibration step



On the final step, the time shift is adjusted to zero to simplify final adjustment of the board in the system. Timing accuracy for all channels and time shift vs. amplitude for selected channels are checked. Currently, all 96 tested channels are within specs (<50 ps rms at 7.5 mV pulse amplitude).

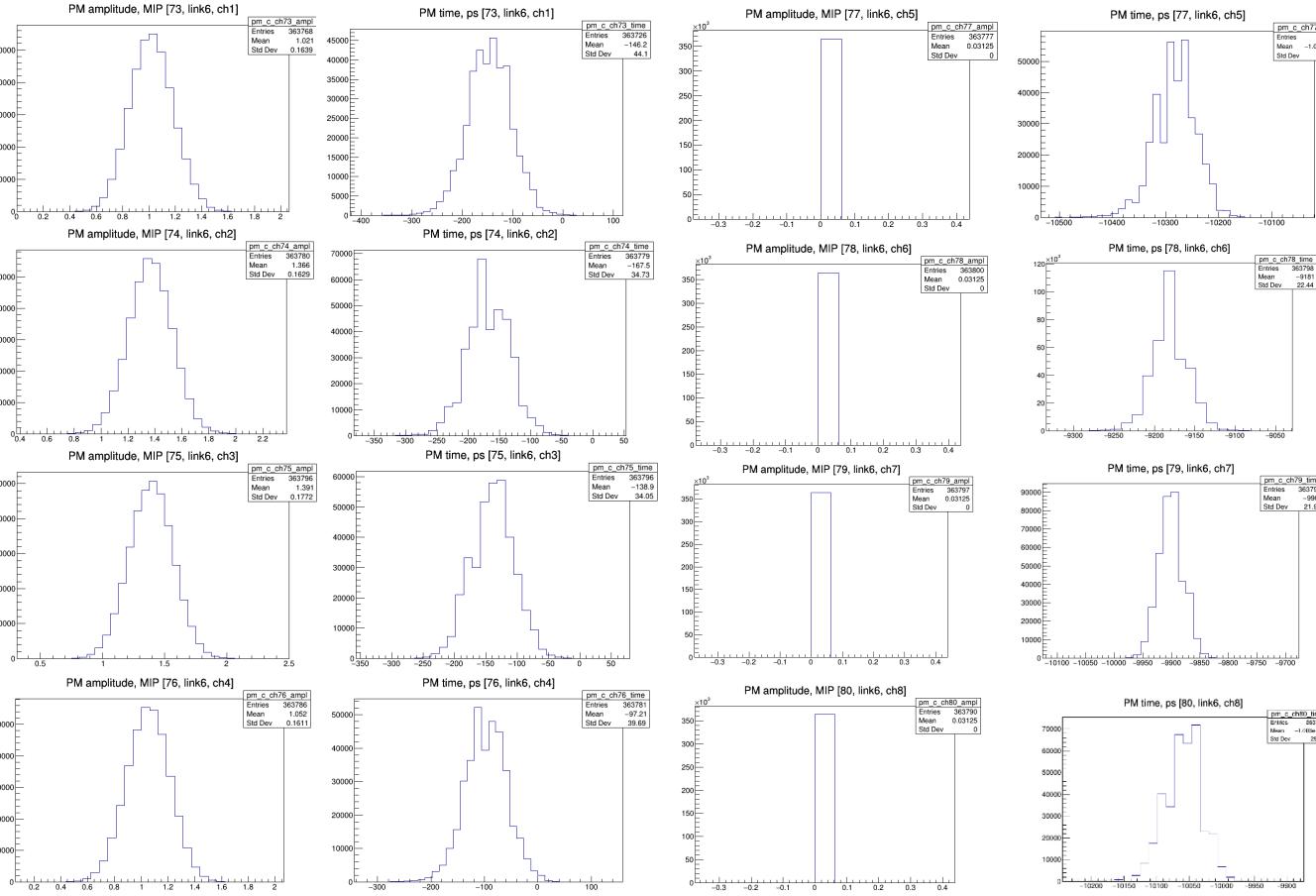
Test with FT0-A detector with 3 MCP installed



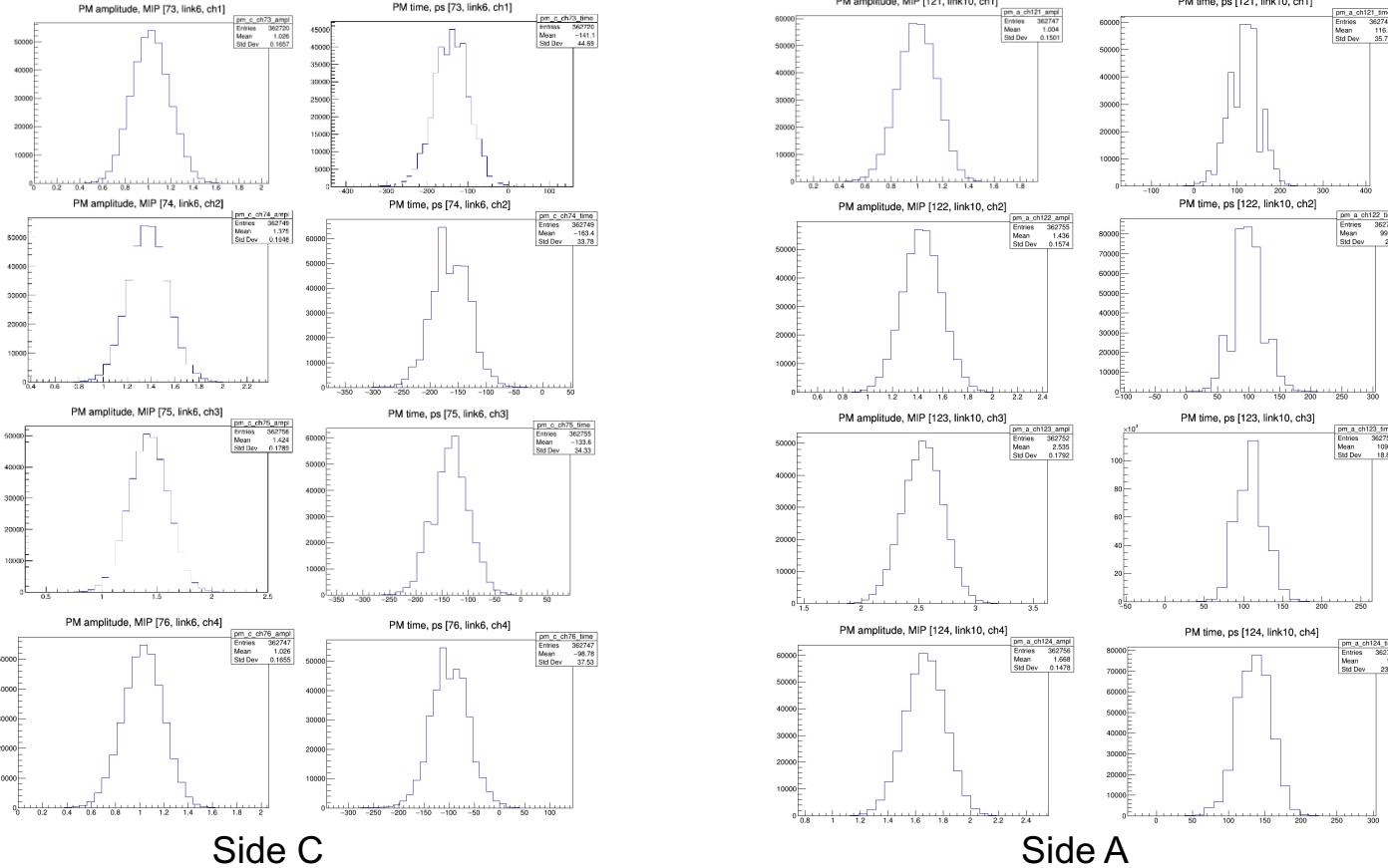
All 12 channel connected to one PM.
Notes:

1. Test was performed before increased noise of integrators was fixed.
2. Gaps in the amplitude distributions histograms caused by digital range correction.

Test with 2 MCP with time shift

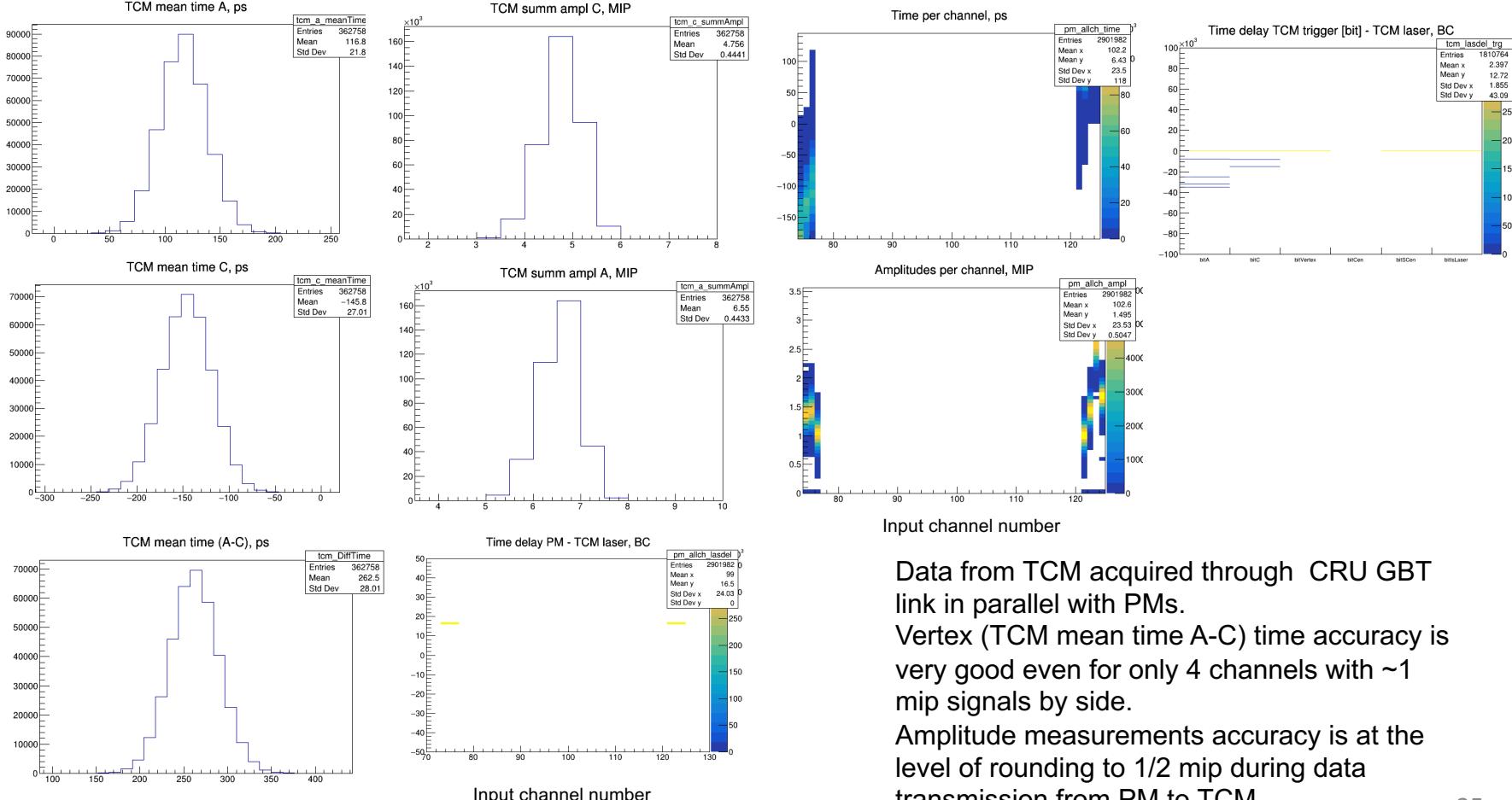


Test with full FIT electronics setup, data from PMs



Data from 2 PMs acquired through different CRU GBT links. Signal arriving time between PMs are physically shifted by ~ 15 ns, as it will be in reality. Difference reduce to 0 by subtracting the offsets in digits during processing in PMs.

Test with full FIT electronics setup, TCM data

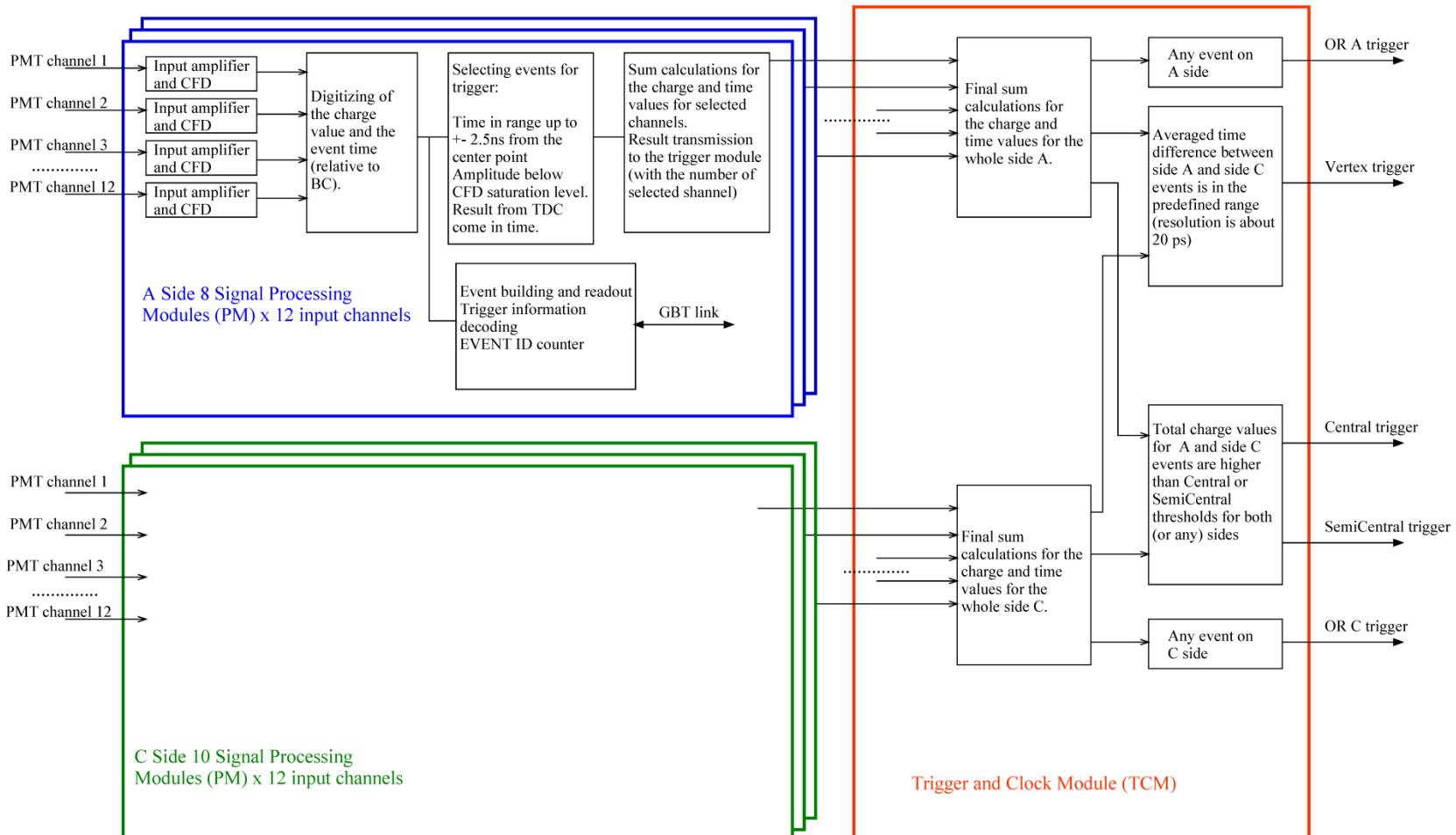


Production schedule of the FIT electronics

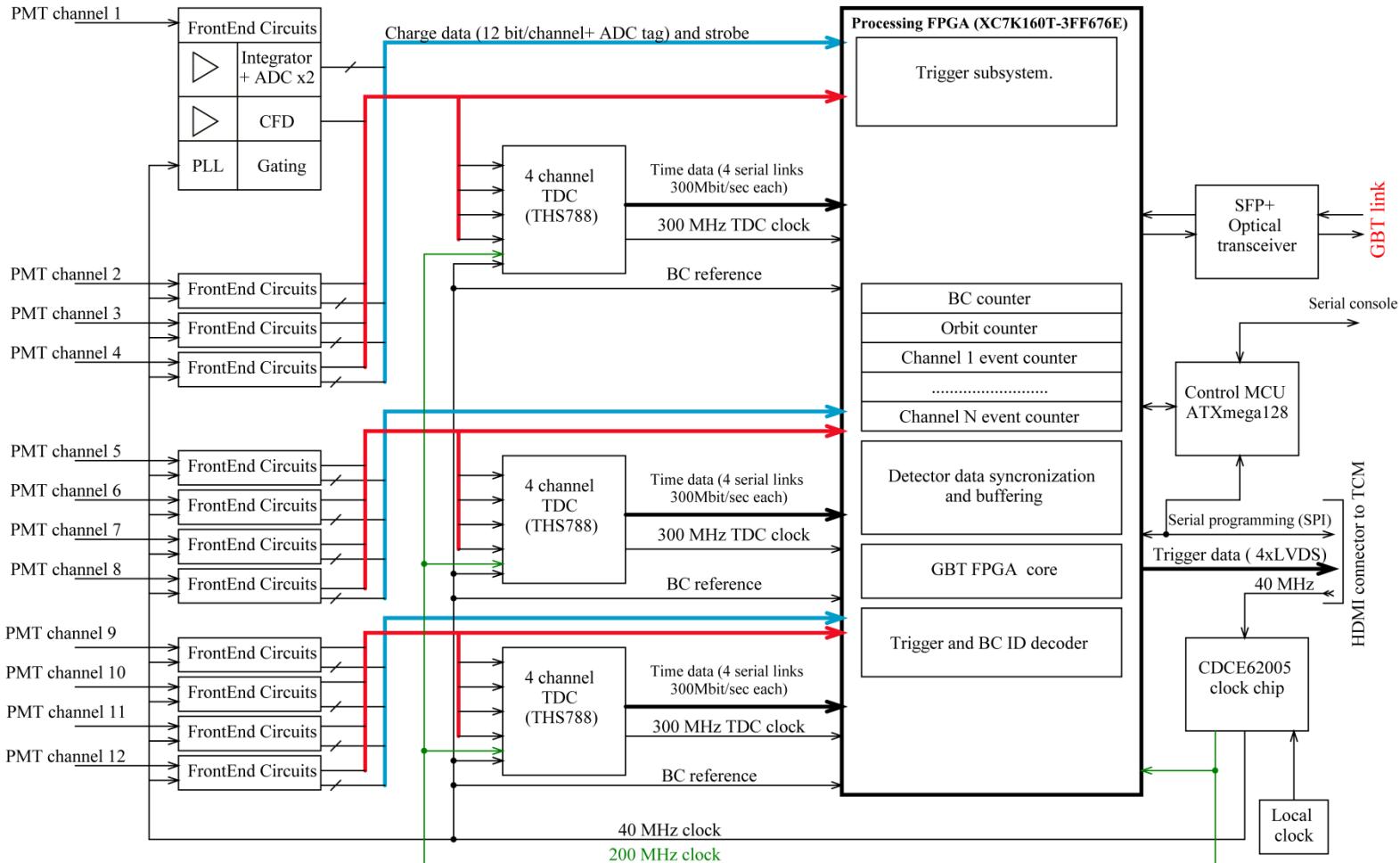
- 14 PMs for FT0 arrive to INR from factory – January, 25 – February, 5
- FT0 PM tests and calibration – February – March
- Parts for 1 FV0/FDD PM at factory – February, 8
- First PM for FV0/FDD at INR – first week of March
- Test setup for PMs at INR with FV0 PMT ready – February
- Tests of the PM for FV0/FDD, final check of the delay cables length – April
- Parts for 11 FV0/FDD PMs at factory – March
- Production of the 11 FV0/FDD PMs – April-May (after the tests of the first module are finished)
- Tests and calibration of the 11 FV0/FDD PMs – May.
- Production of the CFD delay cables for 11 FV0/FDD PMs – April - May.
- Production of the front panels for 50 PMs and 7 TCMs – February.
- One Wiener crate is ready, one will be assembled in January, 3 remaining – March – April.

Thank you for your attention

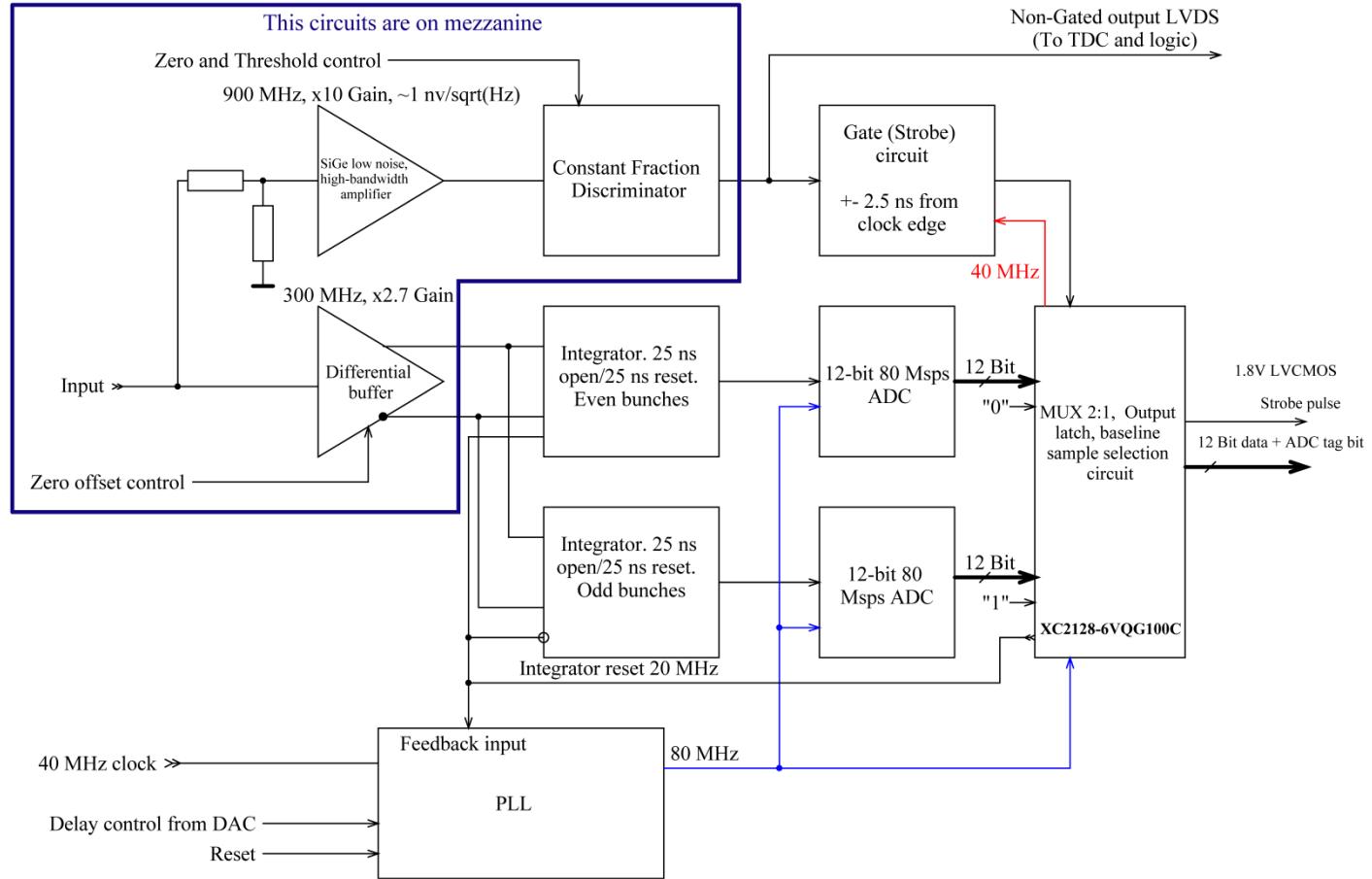
Signal processing in the FIT electronics



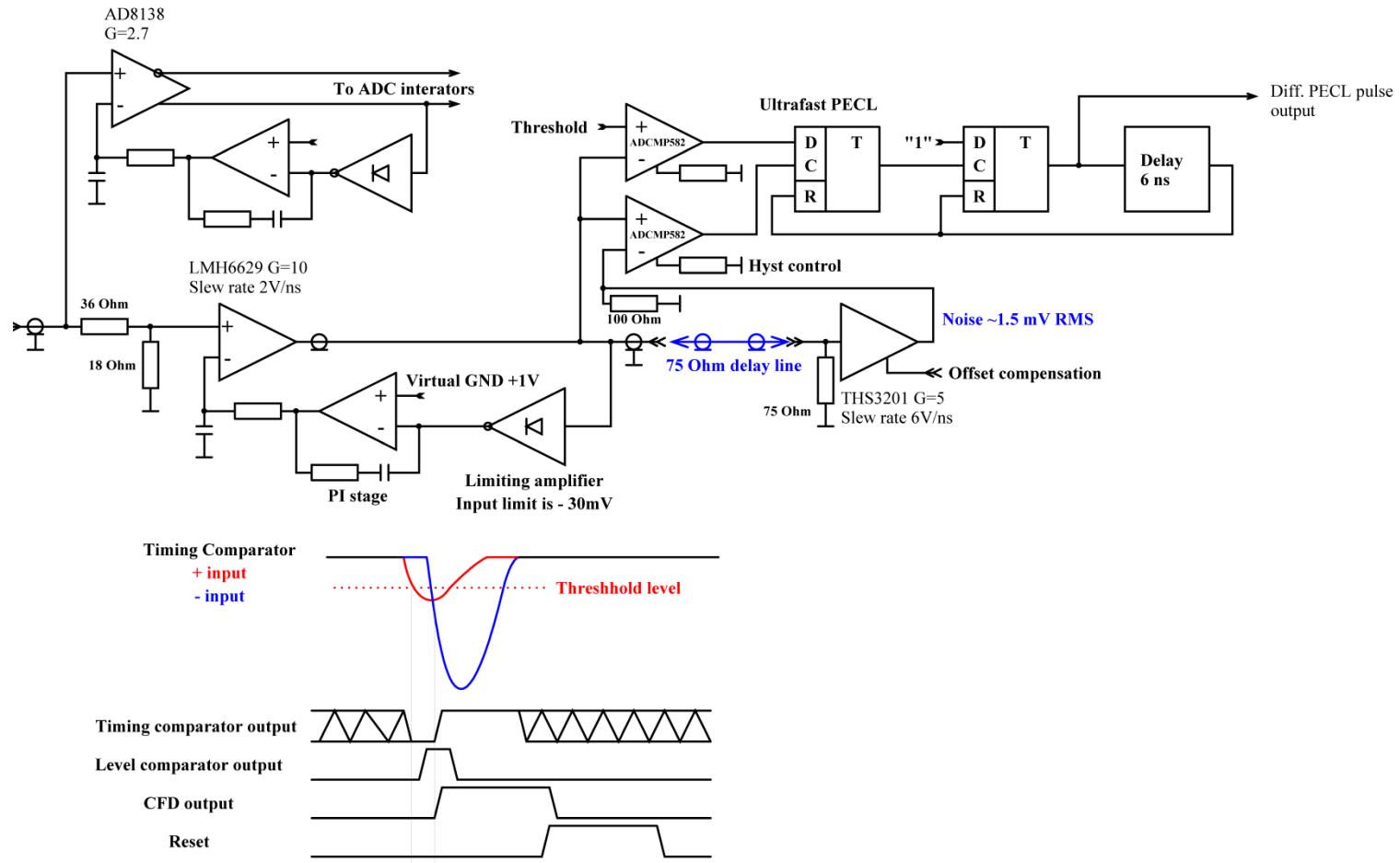
Processing module (PM) structure



Front-End Electronics for the Processing module



PM Mezzanine schematics



PM analog input parameters:

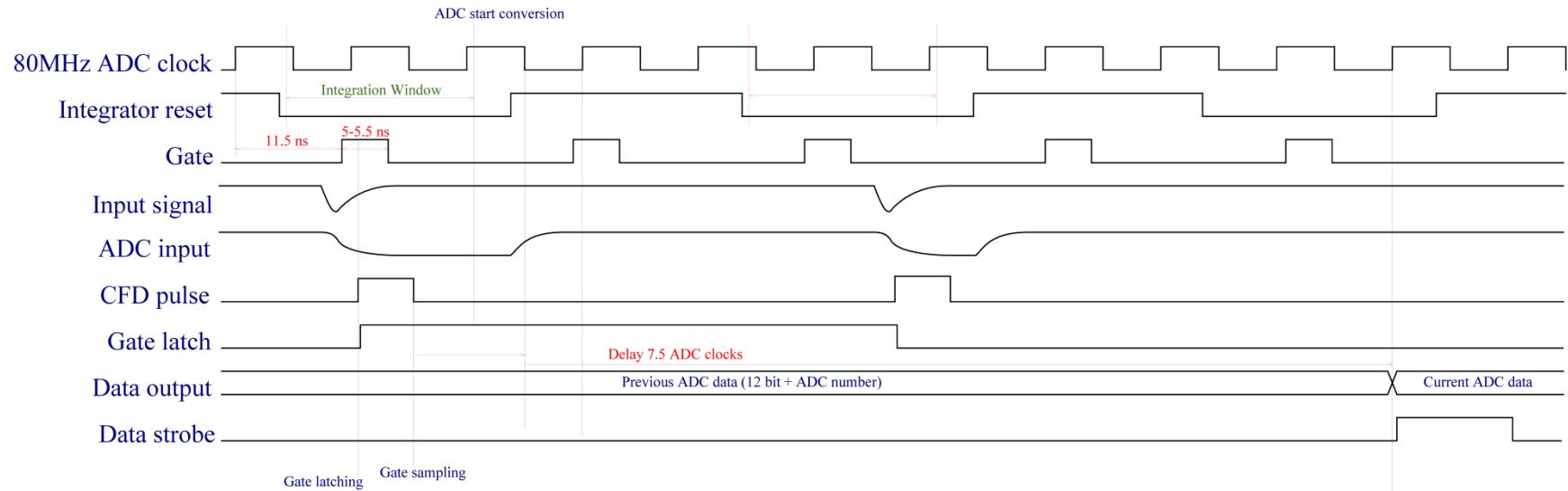
- a. Tested noise count threshold limit for the FIT prototype in ALICE during Run 2 – **3 mV**. This limit goes from noise, injected into the cables and the detector itself.
- b. Optimal threshold for Constant Fraction Discriminator (CFD) is **0.4 mip** (From T0 experience).
- c. Maximum slew rate for LMH6629 amplifier can be achieved for **G ≥10**. Maximum output pulse amplitude is **3 V**, and amplitude, at which required timing accuracy may be achieved is **25 mV**.
- d. Thermal noise limit for CFD threshold, reduced to the LMH6629 input, is **1 mV**.

Based on this we decided to use 1:3 resistive divider on the amplifier input to have maximum possible dynamic range for timing channel.

For charge measurement for FT0, we must have 250 mip dynamic range, i.e. 16 count of the ADC per mip. The gain of the AD8138 buffer for this is ~ 2.7 .

For FV0/FDD the gain must be near ~ 0.7 , as we need 500 mip dynamic range and the charge for the signal of the same amplitude is higher than for T0+.

Front-end circuits timing diagram



- The FEE has two integrators working alternately, each integrates for 25 ns, then resets for the next 25 ns. “Clean” integration window is ~20ns.
- Programmable phase shift is used to adjust the integration window position relative to the input signals, coming from the collisions at Interaction Point.
- *Signals outside the “gating” window will not generate ADC data strobe, and the data will not be transmitted to FPGA.*

TDC THS788

1200 MHz interval counter + 64 tap DLL (13.02 ps/step), independent 300 MHz serial readout for each channel



www.ti.com

THS788

SLOS616B-MARCH 2010-REVISED JUNE 2011

QUAD-CHANNEL TIME MEASUREMENT UNIT (TMU)

Check for Samples: [THS788](#)

FEATURES

- Four Event Channels + Sync Channel
- Single-Shot Accuracy: 8 ps, One Sigma
- Precision: 13 ps (LSB)
- Result Interface Range: 0 s to 7 s
- Event Input Rate: 200 MHz
- Low TC: 0.1 ps/ $^{\circ}\text{C}$
- High-Speed Serial Host-Processor Bus Interface: 50 MHz
- Programmable Serial-Result Interface Speed: 75 MHz–300 MHz
- High-Speed LVDS-Compatible Serial-Result Bus per Channel
- Programmable Serial-Result Bus Length
- Temperature Sensor
- Single 3.3-V Supply
- Power: 675 mW/Channel, 18 Bits, 300 MHz, Four Channels

APPLICATIONS

- Automatic Test Equipment
- Benchtop Time-Measurement Equipment
- Radar and Sonar
- Medical Imaging
- Mass Spectroscopy
- Nuclear/Particle Physics
- Laser Distance Measurement
- Ultrasonic Flow Measurement

TMU BLOCK DIAGRAM

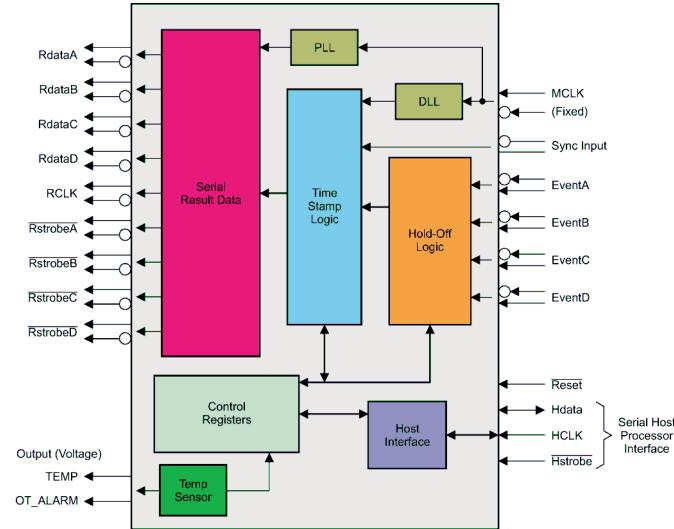


Figure 1. TMU Block Diagram

Properties of the THS788 TDC

- Excellent accuracy – as in datasheet (needs accurate clocks).
- Good phasing of the output signal – no problems with interfacing to the FPGA at 300 MHz.
- Data sync strobe can be deasserted at the arbitrary bit transmission, only leading edge is valid.
- Timing correction on reference input is done at readout time, not the capture time. This means that time must be corrected on the arbitrary reference clock edge. For our case with 1920 counts/BC period we need to read 16 bit of the result to correct the 8-11 bits of the timing value or use only lowest 7 bits (max measured time 1.666 ns).
- Maximum data transmission delay (if internal FIFO is empty) is $5 \text{ ns} + (57 + 17) * 3.333 \text{ ns} \approx 252 \text{ ns}$ for 16 bit result length and $5 \text{ ns} + (33+8) \approx 142 \text{ ns}$ for 8 bit result length (only last 7 bit can be used). Only 8 bit mode allows to be in time for trigger generation. For this mode we need to measure 4 MSB of the result independently and then merge these values into final result.
- After internal FIFO overloading can loss next event, event if FIFO is empty at that moment.

Measuring time by the FPGA.

The time measurement block in FPGA was build basing on Xilinx document xapp523 (LVDS 4x Asynchronous Oversampling Using 7 Series FPGAs and Zynq-7000 AP SoCs). It uses ISERDESE2 units in oversampling mode to sample the asynchronous inputs at 4x clock speed and IDELAY2 units to shift the positive and negative outputs of the input buffer by 1/8 clock period to double the sampling frequency (two sets of ISERDESE2 – IDELAY2 by one input).

To correctly “glue” the results from external TDC and time, measures in the FPGA, we need at least one bit, which overlaps with the result from the TDC, and maximum possible time shift between the FPGA result muss be less than $\frac{1}{4}$ of the external TDC range (<400 ps). If the latest condition is not true, one can't correctly determine the sign of correction (+1 or -1).

We can use the fact, that reference clock is synchronous to the TDC clock, if we can maintain the phase relationship between them. Than we can use 4x sampling and common BUFH for I/O and fabric clock, which significantly simplifies the design. The single problem is that if I/O clock edges is close to reference clock edges, the result will jumps by 400 ps between two values, so the total error will exceed $\frac{1}{4}$ TDC range. To avoid this, the guaranteed 200 ps real initial shift in MMCM phase is set by special phase aligner circuit after each system reset.

Event processing in the PM.

The data from the ADC has defined delay, and data from the TDC has the float one, that is dependent from the number of data in the internal FIFO.

To form the trigger in correct time there is the fast path in the PM from the FE to trigger circuits. In every bunch the logic checks if there are events in the channel and if the timing data is ready and the ADC strobe is active. Based on this, the data from the fast path is included in the trigger calculation.

For the readout path the logic waits for timing data from the TDC and stores the channel data in the FIFO buffer. Event building logic waits until all channels that has events in currently processing EVENT ID will store the data in the buffer, that build the event header, compress the data to two channels per GBT 80 bit word and stores the packet in the 80-bit readout FIFO, which buffers the data between Front-End and readout blocks.

Each channel has two 32-bit counters – one counts all events on the channel input, another – only those included in timing trigger. Counters can be buffered and simultaneously read out from the whole system by one slow-control command.

Time is measured relative to exact IP interaction time, so the resulting value is in range of +-1000.

PM can correctly process up to 32 consecutive event on each channel. After that TDC FIFO can overload and several events will have incorrect time, which will be marked in the channel data by special flag.

Pre-trigger selection

Channel will be included in timing trigger, if:

1. TDC data arrived in time (may be delayed in FIFO when two or more consecutive events occurs in one channel).
2. Event time is in predefined range.
3. ADC strobe received for this event.
4. CFD not saturated – if yes, the channel is excluded from timing trigger.

If at least one channel has event, PM sends data to TCM:

1. PM sends the number of channels in timing trigger in the first bits on PM-TCM link (4 bits parallel code) . If there are no channels in timing trigger, the PM sends 14 (0x0E) instead of number of channels.
2. The arithmetic sum of the measured times for this channels, 13 bits, signed integer format.
3. The total charge (sum) for the channels that have ADC strobe, 14 bits, signed integer format.
4. Flag bit if at least one channel has event outside ADC gate window.

If there is no trigger, PM sends 0100000 (0x40) on each of 4 lines, this allows automatically check the link and adjust receiving phase. Transmission goes on 320 MHz, locked to BC clock.

Event header data format (80 bit)

The format of elementary data packet is common for PM and TCM. It consists of the simple header and data words after it. The length of the packets may vary from 2 words to 10 words (including header word).

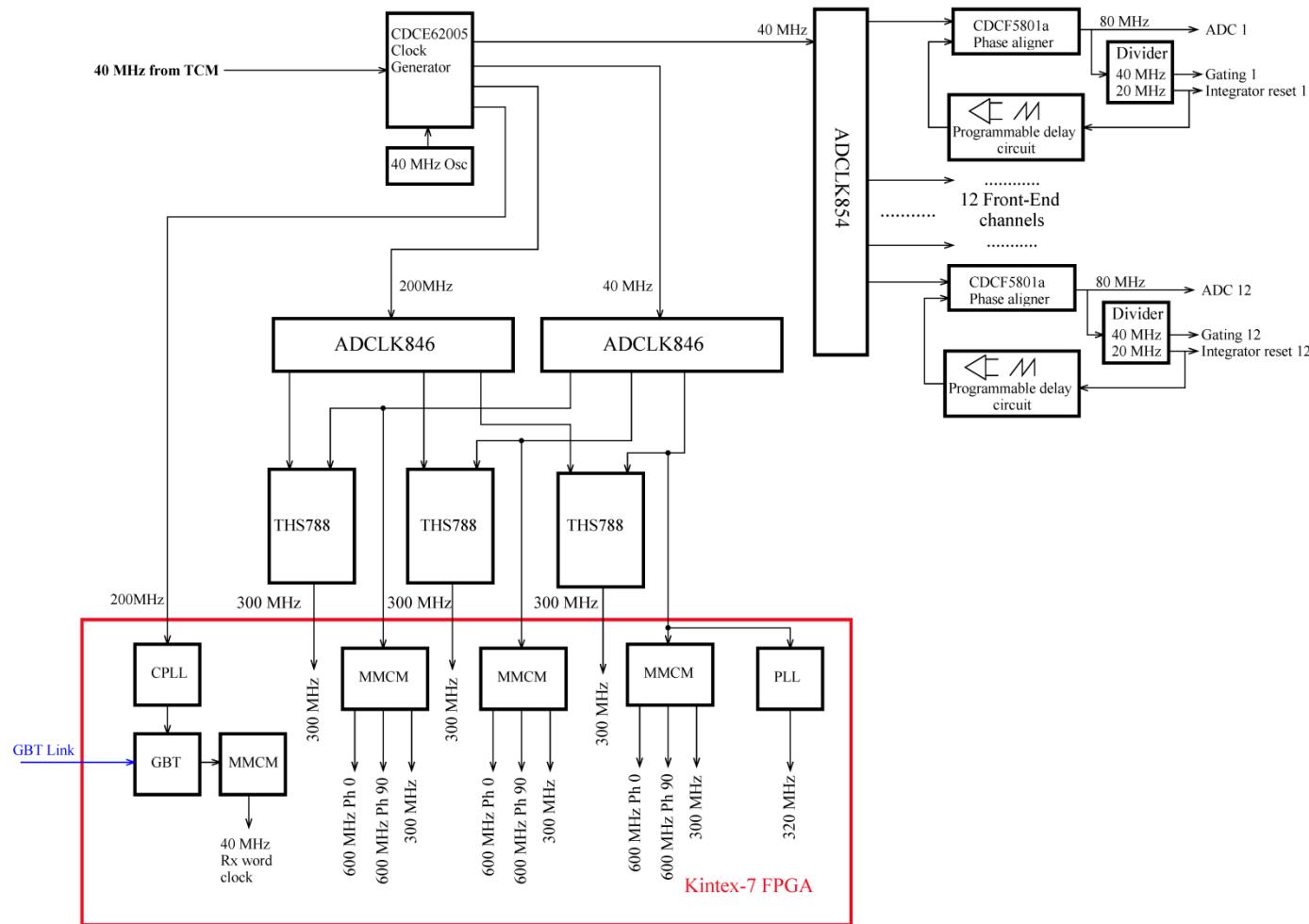
GBT RX phase field indicates current phase difference between module 40 MHz clock and GBT Rx clock, in 45 degrees step. If phase changes more than ± 1 step, the GBT Rx Phase error flag is set, indicating that possible loss of synchronization takes place.

Bits	Value
0 - 11	BC counter
12 - 43	Orbit counter
44 – 46	GBT Rx Phase
47	GBT Rx Phase error flag
48 - 70	Reserved (0)
71 – 74	Data length in GBT words after header
75 - 79	0xF Header tag

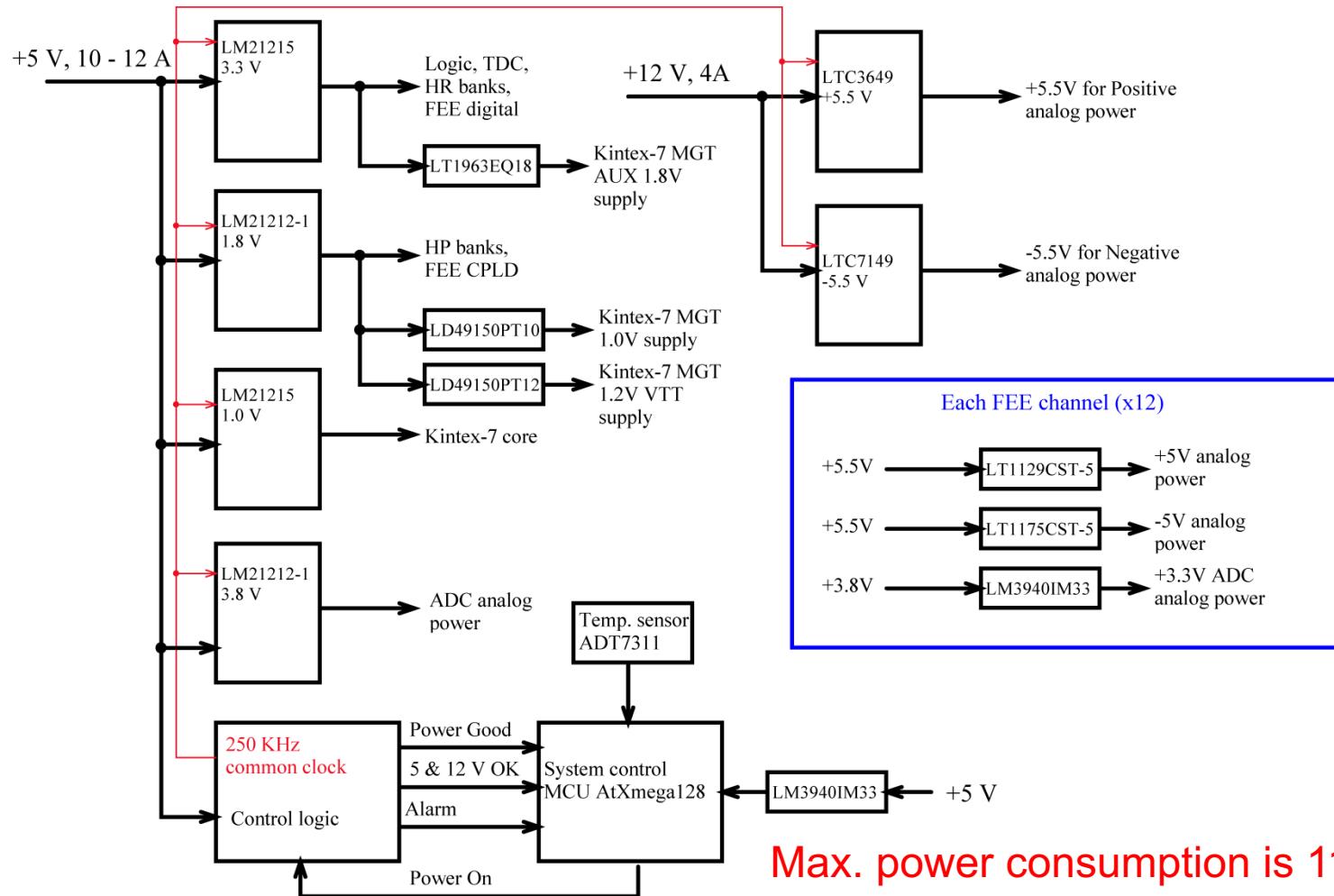
Channel data format (40 bit, $\frac{1}{2}$ GBT word)

Bits	Value
0 - 11	Time with sign bit. (Relative to IP center time value).
12 - 24	Charge with sign bit (baseline/range corrected)
25	ADC number (0/1)
26	Double event (two CFD pulses during one BC period)
27	Time information not valid
28	ADC in gate (CFD pulse time is inside ADC gate)
29	Time information too late (TDC outputs data too late to include in trigger)
30	Amplitude too high (CFD saturated, time may be incorrect)
31	Event time included in trigger calculations
32	Time information lost (TDC data did not arrive for any reason)
33 - 35	Reserved (0)
36 - 39	Channel id (1-12)

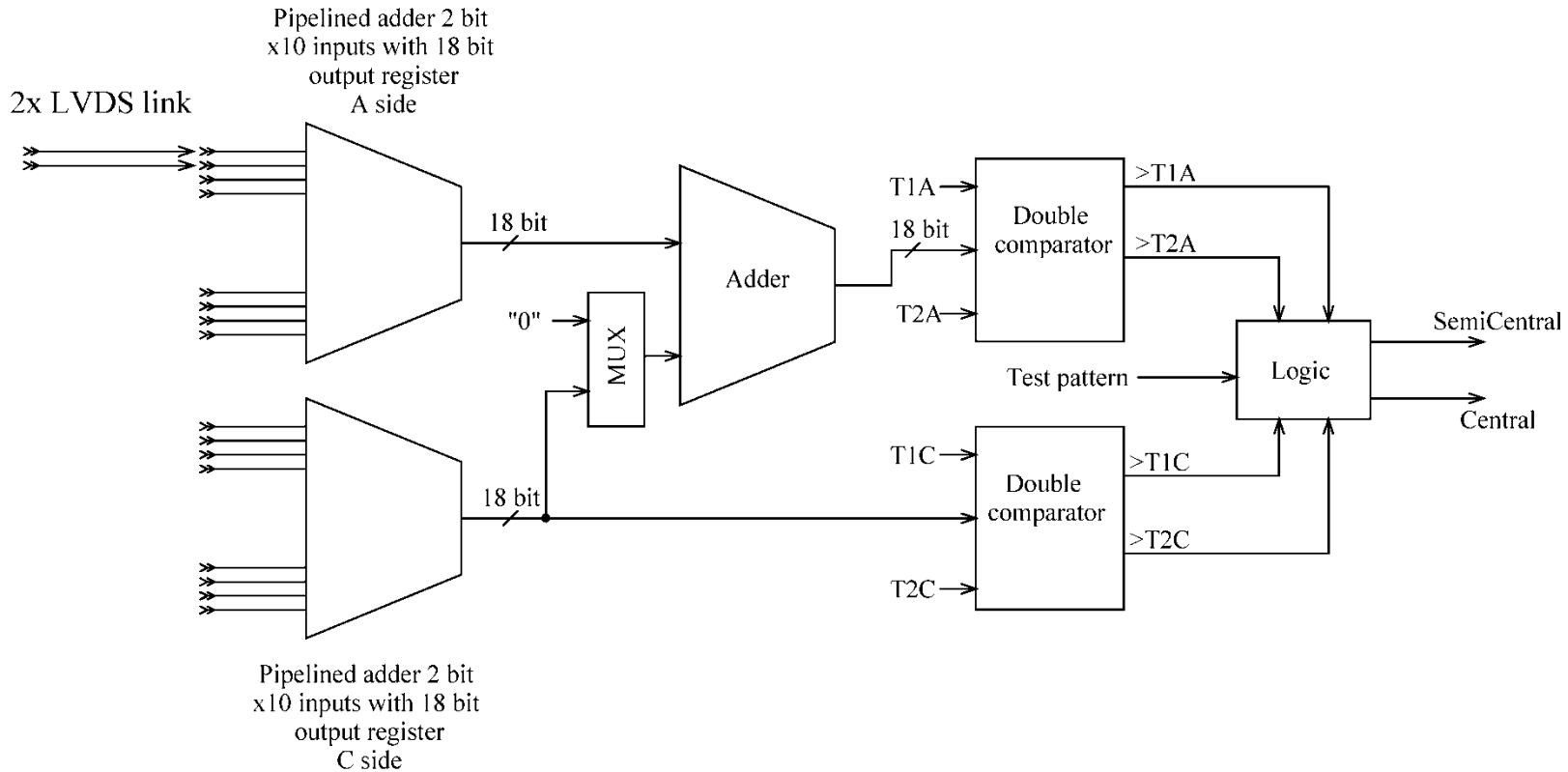
Clock subsystem of the Processing Module



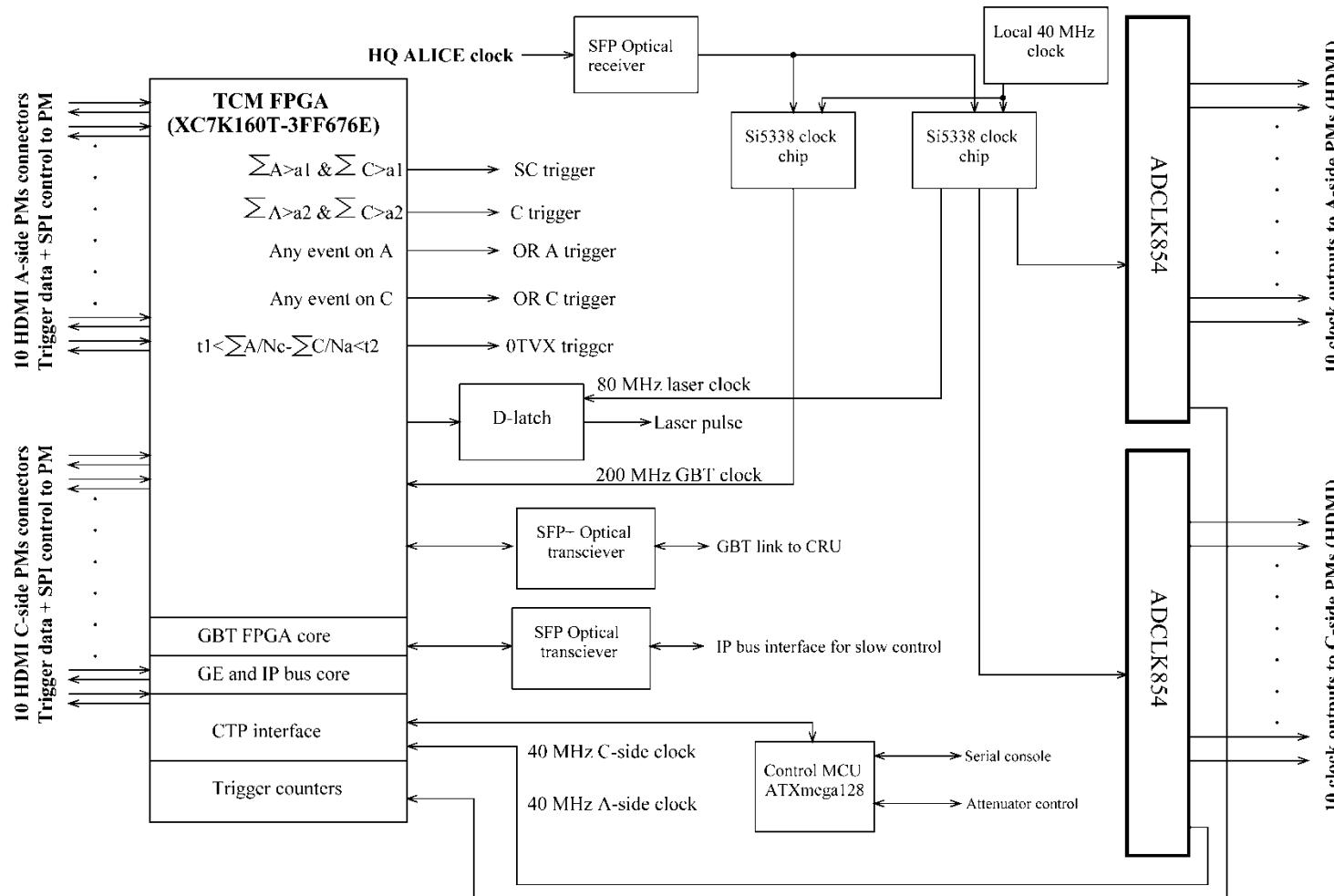
Power supply for the Processing Module



Multiplicity trigger processing in the TCM



Trigger and control module structure (FT0)



TCM data format

Bits	Value
0	OrA trigger
1	OrC trigger
2	SemiCentral trigger
3	Central trigger
4	Vertex trigger
5	Laser pulse
6 – 7	Reserved (0)
8 - 14	Number of A-side active channel
15	Reserved (0)
16 - 22	Number of C-side active channel
23	Reserved (0)
24 - 41	Total charge for A-side
42 - 59	Total charge for C-side
60 - 68	Average time for A-side
69	Reserved (0)
70 - 78	Average time for C-side
79	Reserved (0)

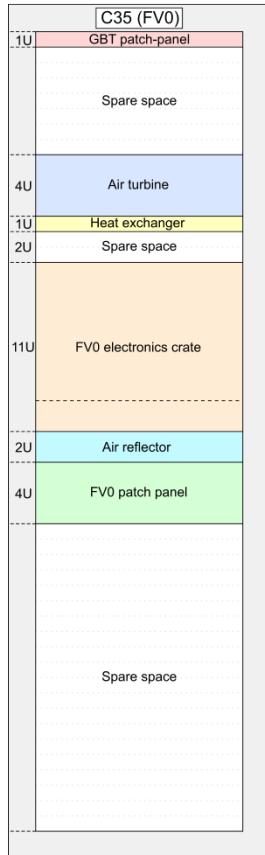
TDC extended data format (additional words)

Words	Bits	Value
1	0 - 31	A0 PM trigger data
	32 - 63	A1 PM trigger data
	63 - 79	A2 PM trigger data 0 – 15 bits
2	0 - 15	A2 PM trigger data 16 – 31 bits
	16 - 47	A3 PM trigger data
	48 - 79	A4 PM trigger data
3	0 - 31	A5 PM trigger data
	32 - 63	A6 PM trigger data
	63 - 79	A7 PM trigger data 0 – 15 bits
4	0 - 15	A7 PM trigger data 16 – 31 bits
	16 - 47	A8 PM trigger data
	48 - 79	A9 PM trigger data
5	0 - 31	C0 PM trigger data
	32 - 63	C1 PM trigger data
	63 - 79	C2 PM trigger data 0 – 15 bits
6	0 - 15	C2 PM trigger data 16 – 31 bits
	16 - 47	C3 PM trigger data
	48 - 79	C4 PM trigger data
7	0 - 31	C5 PM trigger data
	32 - 63	C6 PM trigger data
	63 - 79	C7 PM trigger data 0 – 15 bits
8	0 - 15	C7 PM trigger data 16 – 31 bits
	16 - 47	C8 PM trigger data
	48 - 79	C9 PM trigger data

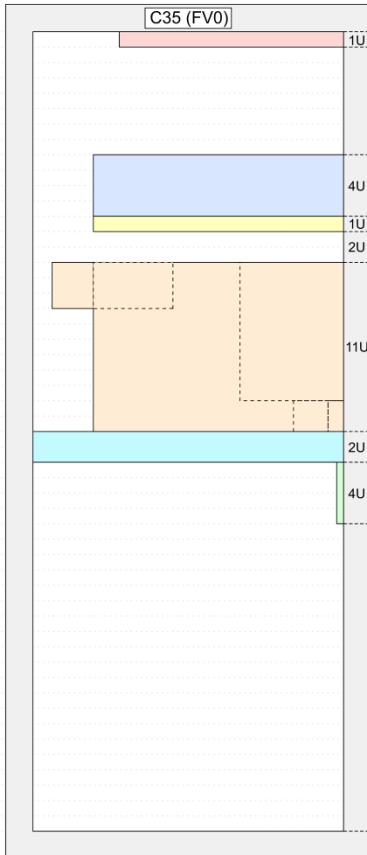
HDMI trigger data format

Bits	Value
0 - 3	Number of active channels (4 bits)
4 - 16	Time data (14 bits)
17	Background event flag
18 - 31	Charge data (14 bits)

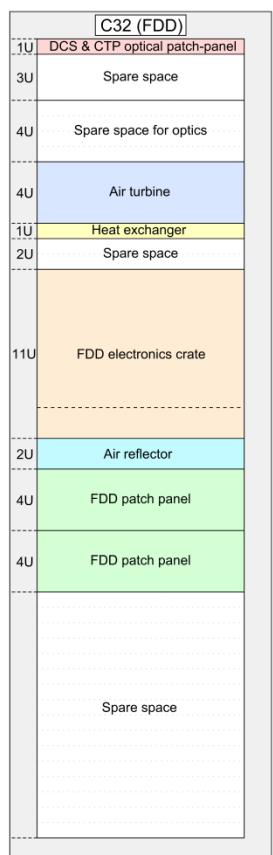
Racks for FV0 and FDD



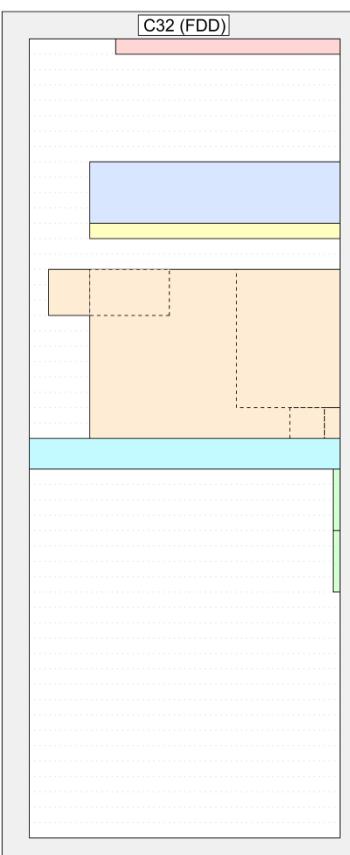
Front view



Side view (from the left)



Front view



Side view (from the left)