JMicron Technology Corporation

PCB LAYOUT GUIDE

JMS561

Document No.: LOG-16005 / Revision: 1.1 / Date: 9/23/2016

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Printed in Taiwan 2016

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Revision History

Revision	Effect Date	Description of Revision		Author
		Reference	Description of the Change	
1.0	01-07-2014	--	Initial release.	Jason
1.1	09-23-2016		Update chapter 7	Mika

This document is valid until ☐ the date dd-mm-yyyy ☒ the next revision has been effective.

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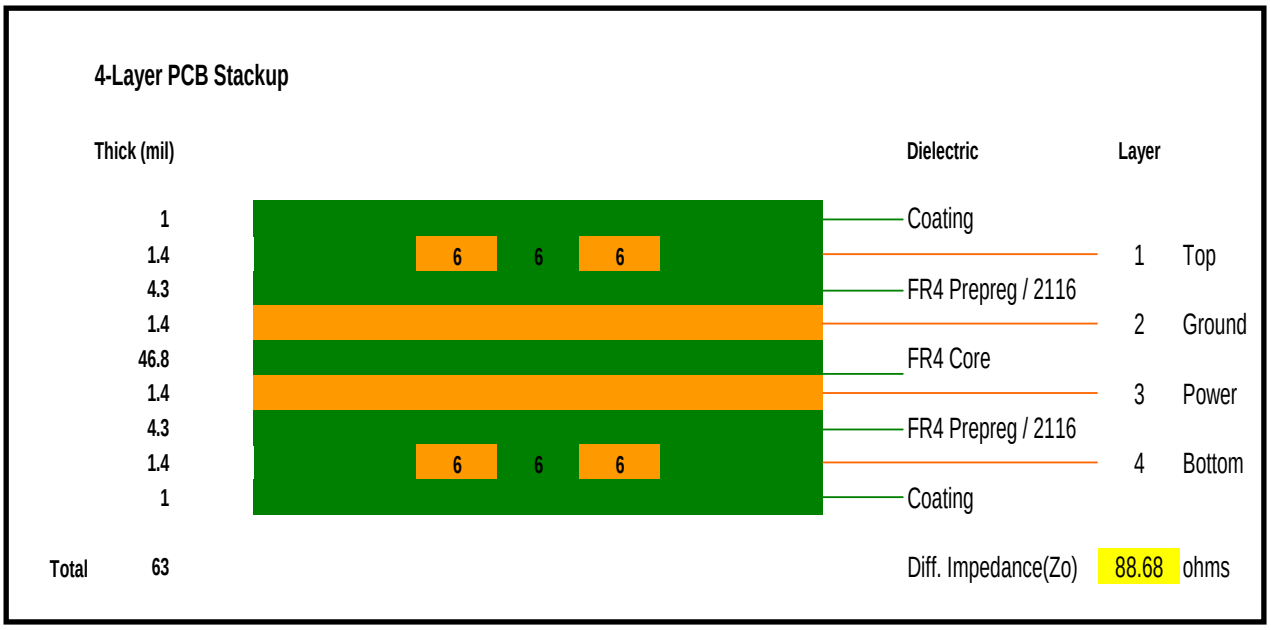
1 Overviews

1.1 Description

This layout guide includes USB3.0, SATA Gen3, USB2.0, Power plane, Crystal and Switching Regulator LC.

1.2 PCB Stack up



2 USB3.0 Layout Guide

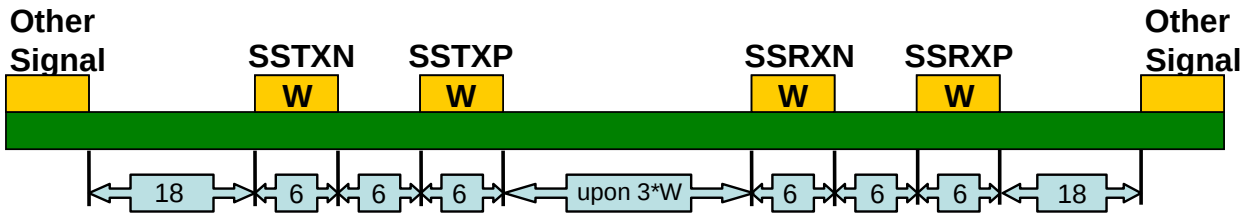
2.1 Relative Net Name & Pairs

USB3.0 has 2 differential signal pairs，detailed information is as follows:

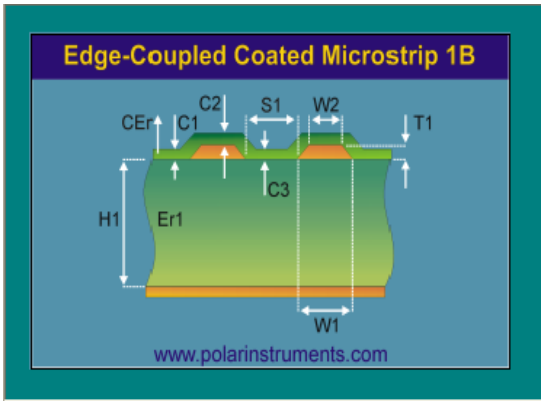
Net Name	Routing Layer	Reference Layer
SSTXP, SSTXN, SSRXN, SSRXP	1st layer	2nd layer (GND)

2.2 Net Spacing & Trace Width Rule

- USB Trace : Trace Width / Trace Separation / Pair Separation ＝ 6 / 6 / 18.0 mil]
  Target differential impedance: 89 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB3.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.

- Route all SuperSpeed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SuperSpeed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

3 SATA Gen3 Layout Guide

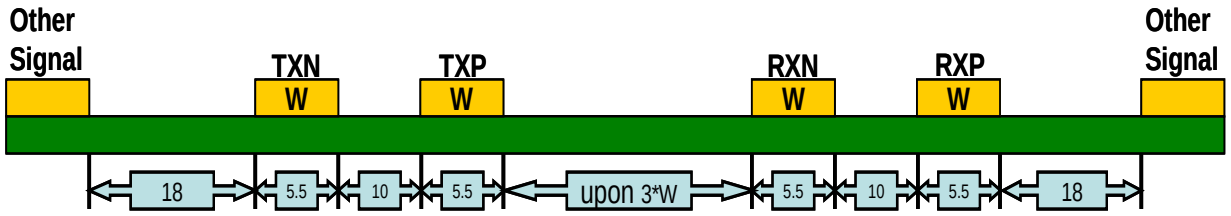
3.1 Relative Net Name & Pairs

SATA Gen3 has 2 differential signal pairs，detailed information is as follows:

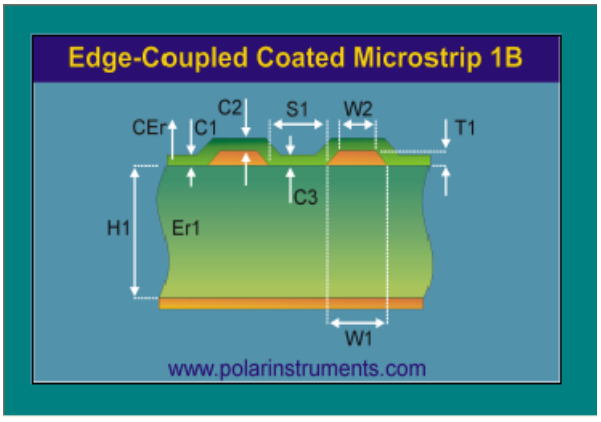
Net Name	Routing Layer	Reference Layer
TXP, TXN, RXN, RXP	1st layer	2nd layer (GND)

3.2 Net Spacing & Trace Width Rule

- SATA Trace : Trace Width / Trace Separation / Pair Separation ＝ 5.5 / 10 / 18.0 mil]
  Target differential impedance: 100 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	5.5000	+/-	0.0000	5.5000	5.5000
Upper Trace Width	W2	5.5000	+/-	0.0000	5.5000	5.5000
Trace Separation	S1	10.0000	+/-	0.0000	10.0000	10.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	100.03			100.03	100.03

- SATA Gen3 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.

- Route all SATA signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SATA traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

4 USB2.0 Layout Guide

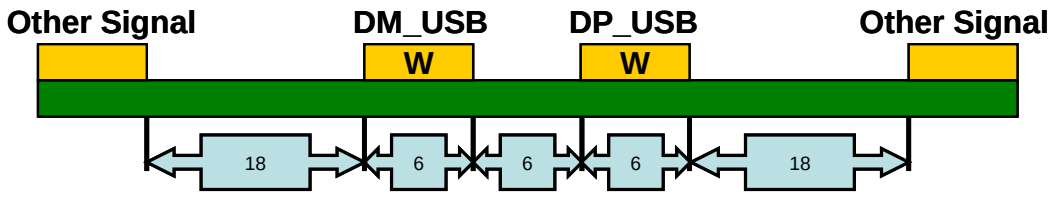
4.1 Relative Net Name & Pairs

USB2.0 has a differential signal pair，detailed information is as follows:

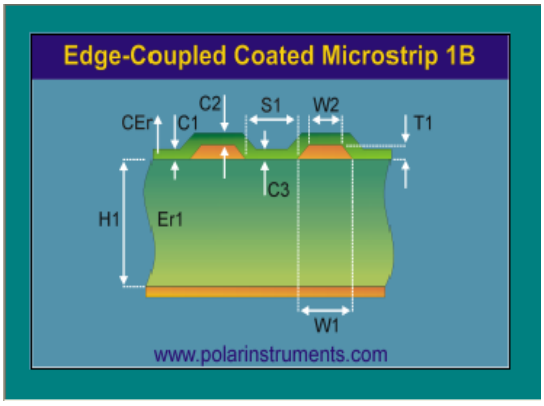
Net Name	Routing Layer	Reference Layer
DP_USB, DM_USB	1st layer	2nd layer (GND)

4.2 Net Spacing & Trace Width Rule

- USB Trace : Trace Width / Trace Separation / Pair Separation ＝ 6 / 6 / 18 mil]
  Target differential impedance: 89 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB2.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all high-speed USB signal traces over continuous planes (VCC or GND), with

no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

- Do not route high-speed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

5 Crystal Layout Guide

5.1 Relative Net Name & Pairs

The Oscillator/Crystal detailed information is as follows:

Net Name	Routing Layer	Reference Layer
XIN, XOUT	1st layer	2nd layer (GND)

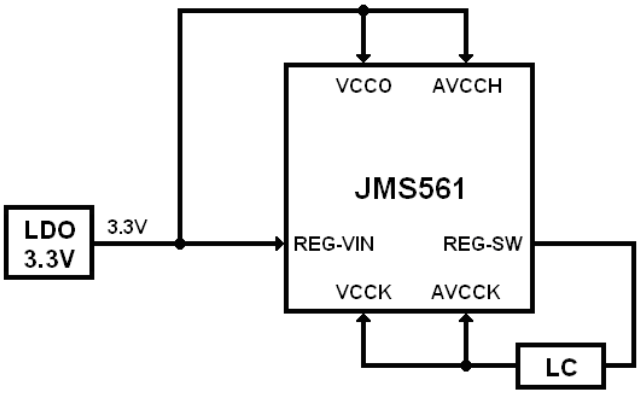
5.2 Layout Rule

- The Crystal unit should then be placed as close as possible to the XIN and XOUT pins to minimize etch lengths.
- Ensure that the ground plane under the IC and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the IC ground reference.

6 Power Layout Guide

6.1 Relative Net Name

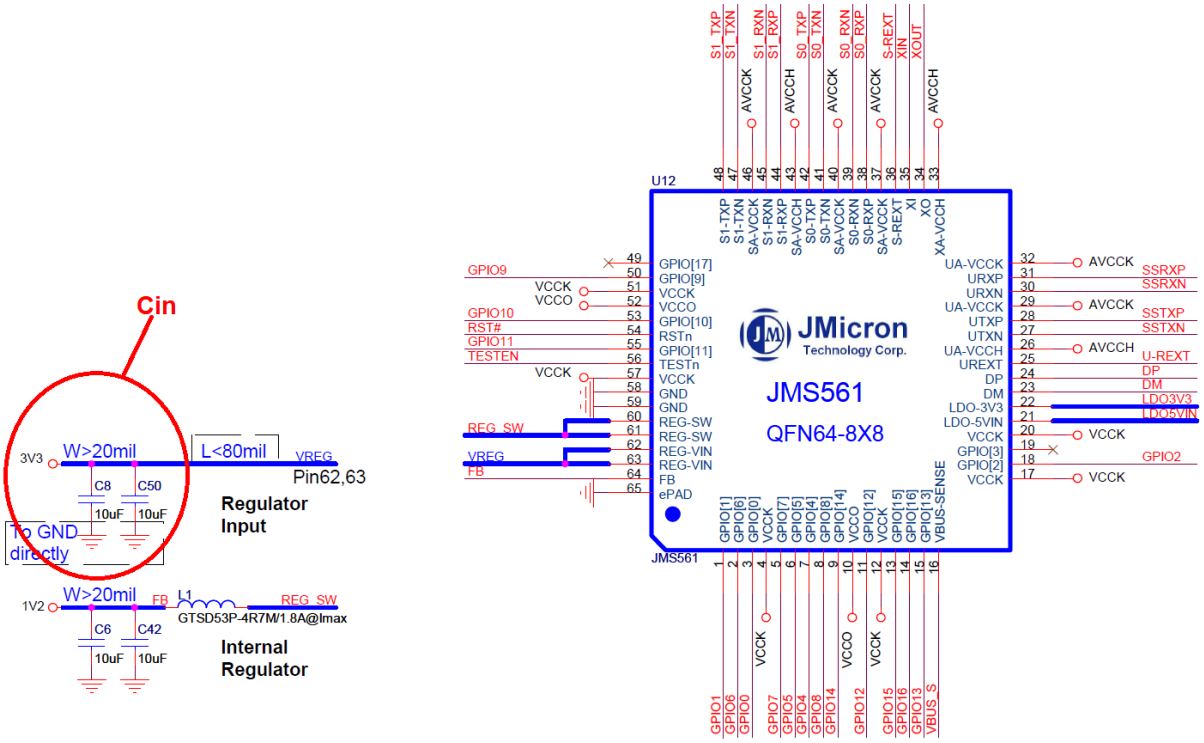
Power detailed information is as follows:



6.2 Layout Rule

- The width of 3.3V ≧ 120 mil (suggest 140mil)
- The width of VCCO , AVCCH ≧ 40 mil (suggest 50 mil)
- The width of REG_VIN , REG_SW , VCCK , AVCCK ≧ 80 mil (suggest 90 mil)

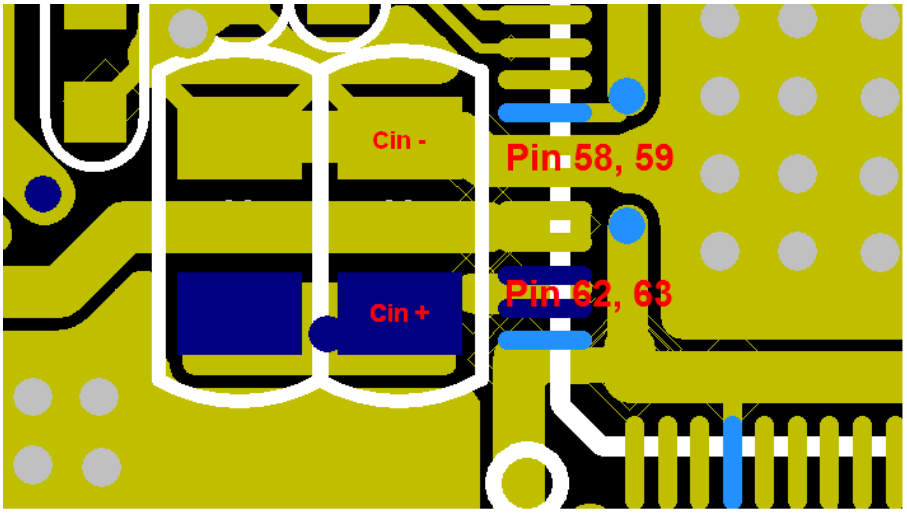
7 Switching Regulator LC Layout Guide



- C8, C50 close chip (< 100 mil)
- C6, C42, L1 keep away chip (>800 mil)
- C8, C50, C6, C42, L1 keep away SATA signal and USB signal

7.1 Cin Layout Rule

- Cin- must be as close as possible to IC.Pin 58, 59
- Cin+ must be as close as possible to IC.Pin 62, 63
- For example :



7.2 LC Layout Rule

- Away from the JMS561, USB signal and SATA signal.
- Do not insert ferrite bead in VCCK.