



## PCB LAYOUT GUIDE

### JMS561

Document No.: LOG-16005 / Revision: 1.1 / Date: 9/23/2016

#### JMicron Technology Corporation

1F, No. 13, Innovation Road 1, Science-Based Industrial Park,  
Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

Website: <http://www.jmicron.com>



Certificate No.: TW16/00614

Copyright © 2016, JMicon Technology Corp. All Rights Reserved.

Printed in Taiwan 2016

JMicron and the JMicon Logo are trademarks of JMicon Technology Corporation in Taiwan and/or other countries.

Other company, product and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use implantation or other life supports application where malfunction may result in injury or death to persons. The information contained in this document does not affect or change JMicon's product specification or warranties. Nothing in this document shall operate as an express or implied license or environments, and is presented as an illustration. The results obtained in other operating environments may vary.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will JMicon be liable for damages arising directly or indirectly from any use of the information contained in this document.

For more information on JMicon products, please visit the JMicon web site at <http://www.JMicon.com> or send e-mail to [sales@jmicon.com](mailto:sales@jmicon.com). For product application support, please send e-mail to [fae@jmicon.com](mailto:fae@jmicon.com).

JMicron Technology Corporation

1F, No.13, Innovation Road 1, Science-Based Industrial Park, Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

## Revision History

Revision	Effect Date	Description of Revision		Author
		Reference	Description of the Change	
1.0	01-07-2014	--	Initial release.	Jason
1.1	09-23-2016		Update chapter 7	Mika

This document is valid until ☐ the date [dd-mm-yyyy](#) ☒ the next revision has been effective.

## Table of Contents

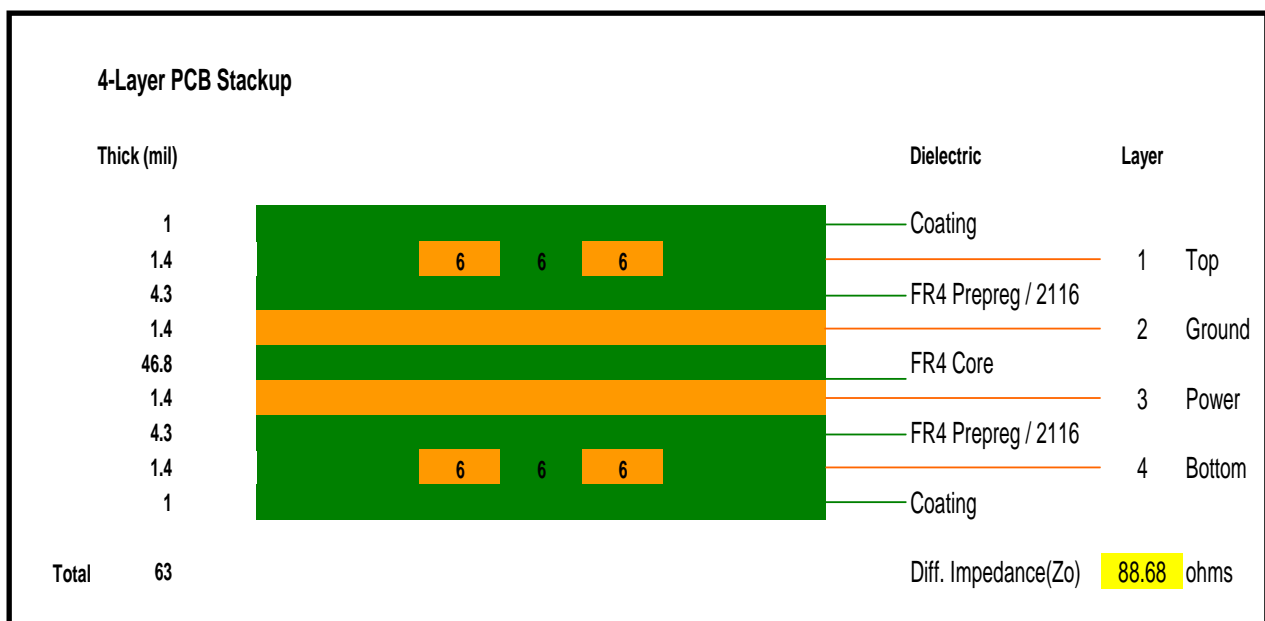
<b>Revision History</b> .....	<b>ii</b>
<b>Table of Contents</b> .....	<b>iii</b>
<b>1 Overviews</b> .....	<b>1</b>
1.1 Description .....	1
1.2 PCB Stack up .....	1
<b>2 USB3.0 Layout Guide</b> .....	<b>2</b>
2.1 Relative Net Name & Pairs .....	2
2.2 Net Spacing & Trace Width Rule.....	2
<b>3 SATA Gen3 Layout Guide</b> .....	<b>4</b>
3.1 Relative Net Name & Pairs .....	4
3.2 Net Spacing & Trace Width Rule.....	4
<b>4 USB2.0 Layout Guide</b> .....	<b>6</b>
4.1 Relative Net Name & Pairs .....	6
4.2 Net Spacing & Trace Width Rule.....	6
<b>5 Crystal Layout Guide</b> .....	<b>8</b>
5.1 Relative Net Name & Pairs .....	8
5.2 Layout Rule .....	8
<b>6 Power Layout Guide</b> .....	<b>9</b>
6.1 Relative Net Name .....	9
6.2 Layout Rule .....	9
<b>7 Switching Regulator LC Layout Guide</b> .....	<b>10</b>
7.1 Cin Layout Rule .....	10
7.2 LC Layout Rule .....	11

## 1 Overviews

### 1.1 Description

This layout guide includes USB3.0, SATA Gen3, USB2.0, Power plane, Crystal and Switching Regulator LC.

### 1.2 PCB Stack up



## 2 USB3.0 Layout Guide

### 2.1 Relative Net Name & Pairs

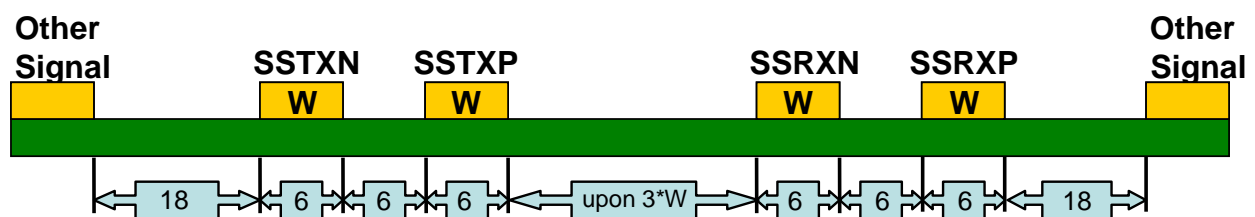
USB3.0 has 2 differential signal pairs , detailed information is as follows:

Net Name	Routing Layer	Reference Layer
SSTXP, SSTXN, SSRXN, SSRXP	1st layer	2nd layer (GND)

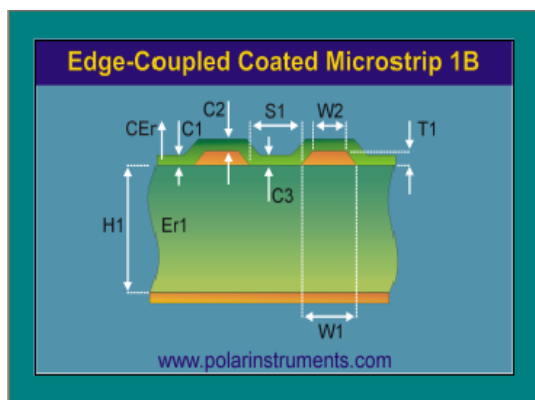
### 2.2 Net Spacing & Trace Width Rule

- USB Trace : Trace Width / Trace Separation / Pair Separation = 6 / 6 / 18.0 mil ]

Target differential impedance: 89  $\Omega$



Unit: mil



			Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000
Differential Impedance	Zdiff	88.68		88.68	88.68

- USB3.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.

- Route all SuperSpeed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SuperSpeed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

### 3 SATA Gen3 Layout Guide

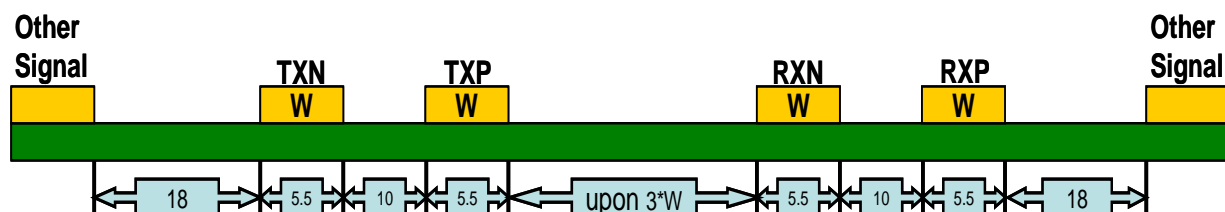
#### 3.1 Relative Net Name & Pairs

SATA Gen3 has 2 differential signal pairs , detailed information is as follows:

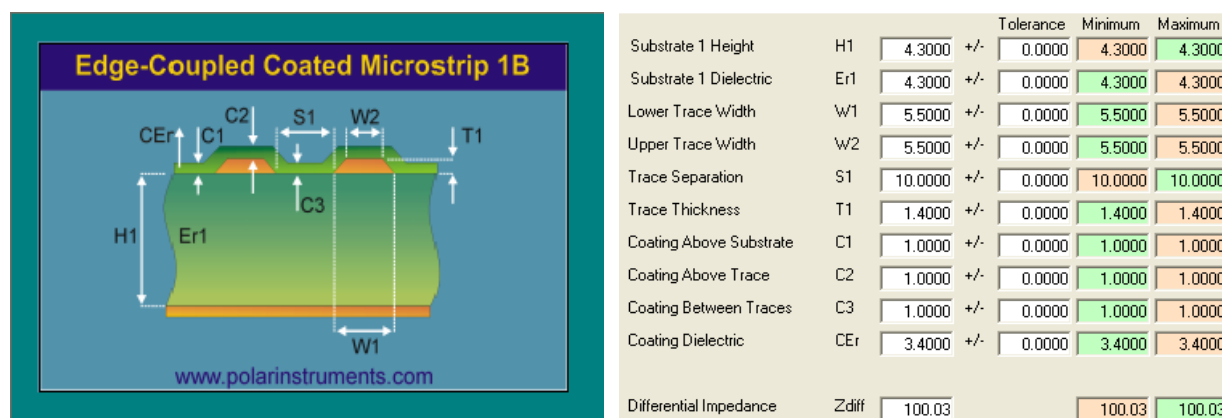
Net Name	Routing Layer	Reference Layer
TXP, TXN, RXN, RXP	1st layer	2nd layer (GND)

#### 3.2 Net Spacing & Trace Width Rule

- SATA Trace : Trace Width / Trace Separation / Pair Separation = 5.5 / 10 / 18.0 mil ]  
Target differential impedance: 100 Ω



Unit: mil



- SATA Gen3 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.



- Route all SATA signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SATA traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

## 4 USB2.0 Layout Guide

### 4.1 Relative Net Name & Pairs

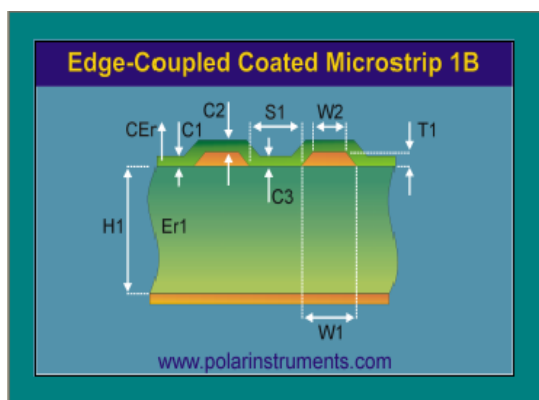
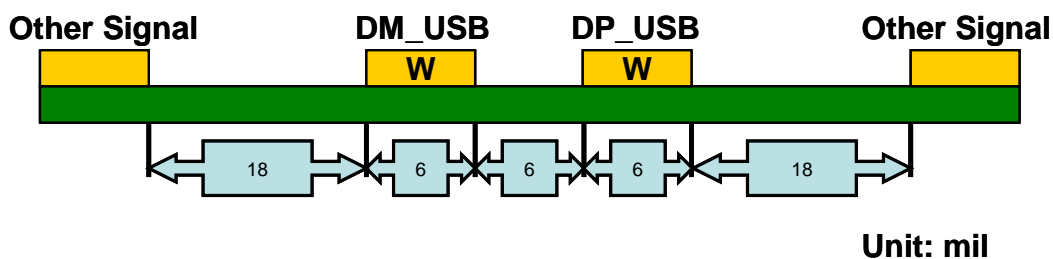
USB2.0 has a differential signal pair , detailed information is as follows:

Net Name	Routing Layer	Reference Layer
DP_USB, DM_USB	1st layer	2nd layer (GND)

### 4.2 Net Spacing & Trace Width Rule

- USB Trace : Trace Width / Trace Separation / Pair Separation = 6 / 6 / 18 mil ]

Target differential impedance: 89 Ω



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB2.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all high-speed USB signal traces over continuous planes (VCC or GND), with

- no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route high-speed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

## 5 Crystal Layout Guide

### 5.1 Relative Net Name & Pairs

The Oscillator/Crystal detailed information is as follows:

Net Name	Routing Layer	Reference Layer
XIN, XOUT	1st layer	2nd layer (GND)

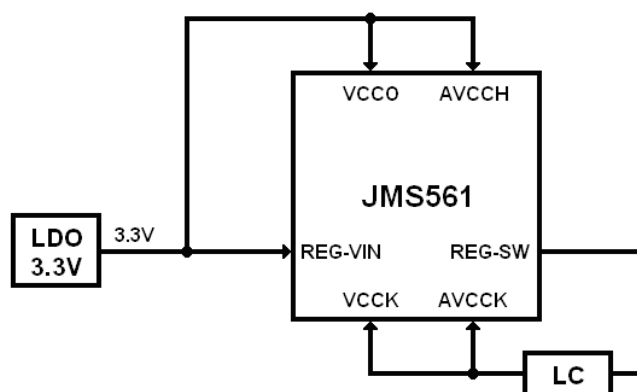
### 5.2 Layout Rule

- The Crystal unit should then be placed as close as possible to the XIN and XOUT pins to minimize etch lengths.
- Ensure that the ground plane under the IC and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the IC ground reference.

## 6 Power Layout Guide

### 6.1 Relative Net Name

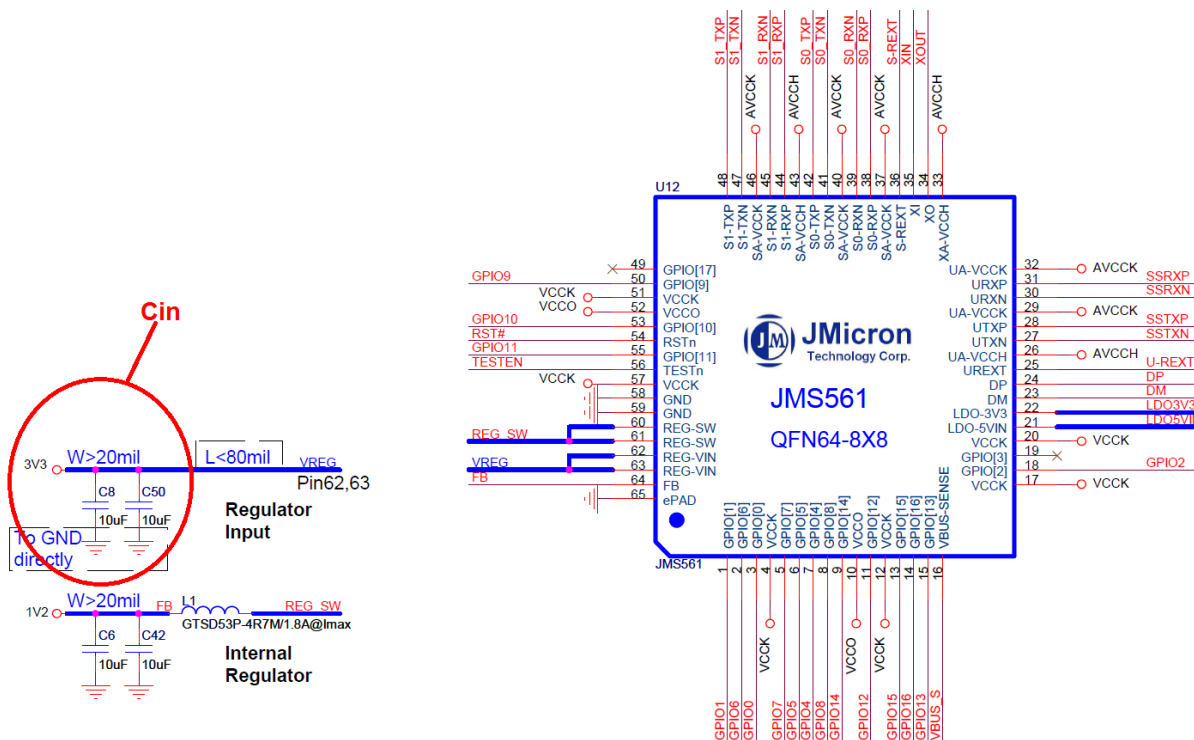
Power detailed information is as follows:



### 6.2 Layout Rule

- The width of 3.3V  $\geq$  120 mil ( suggest 140mil )
- The width of VCCO , AVCCCH  $\geq$  40 mil ( suggest 50 mil )
- The width of REG\_VIN , REG\_SW , VCCCK , AVCCCK  $\geq$  80 mil ( suggest 90 mil )

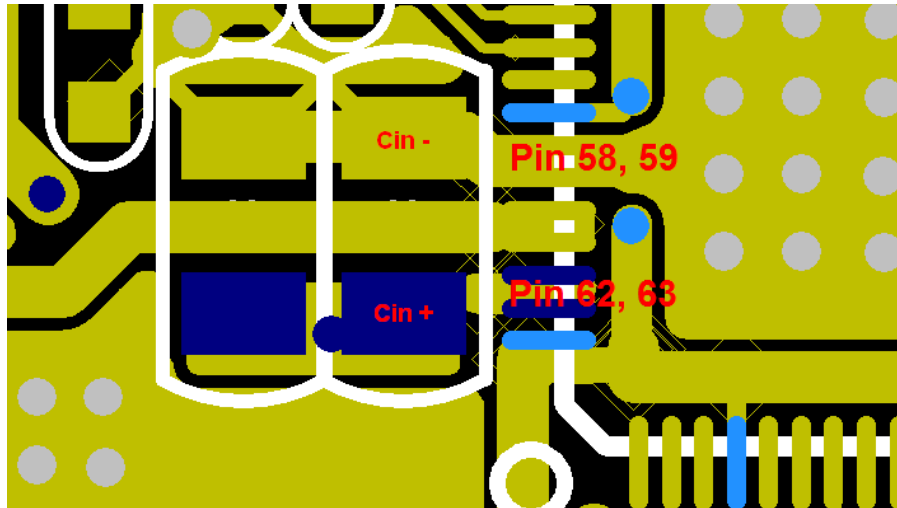
## 7 Switching Regulator LC Layout Guide



- C8, C50 close chip (< 100 mil)
- C6, C42, L1 keep away chip (>800 mil)
- C8, C50, C6, C42, L1 keep away SATA signal and USB signal

### 7.1 Cin Layout Rule

- Cin- must be as close as possible to IC.Pin 58, 59
- Cin+ must be as close as possible to IC.Pin 62, 63
- For example :



## 7.2 LC Layout Rule

- Away from the JMS561, USB signal and SATA signal.
- Do not insert ferrite bead in VCCK.

<http://www.jmicron.com>



**JMicron**

Storing the World • Bridging the Future