JMicron Technology Corporation

DATASHEET

JMS561
SuperSpeed USB To Dual SATA 6Gb/s Ports Bridge Controller

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JMicron Technology Corporation

1F, No. 13, Innovation Road 1, Science-Based Industrial Park,

Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

Website: http://www.jmicron.com

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For more information on JMicron products, please visit the JMicron web site at http://www.JMicron.com or send e-mail to sales@jmicron.com. For product application support, please send e-mail to fae@jmicron.com.

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1F, No.13, Innovation Road 1, Science-Based Industrial Park, Hsinchu, Taiwan 300, R.O.C.
Tel: 886-3-5797389
Fax: 886-3-5799566

Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
1.00	10/31/2013	--	Release revision 1.0.0	Mika Cheng
1.01	07/24/2014	--	1. Updated performance benchmark 2. Updated GPIO description 3. Updated XIN/XOUT pin voltage 4. Updated VREG-IN and FB pin voltage 5. Updated SPI support list, add “Fudan Microelectronics FM25F04A”,”Giga Device 25Q41BT”	Mika Cheng
1.02	11/03/2015	--	Removed Minimum Junction Temperature	Mika Cheng
1.03	11/15/2016	--	Removed SPI support and performance	Mika Cheng
1.04	11/30/2016	Cover	Corrected typos	Leo Tsao
1.05	10/25/2017	Figure 8	Corrected typos (part number)	Leo Tsao
1.06	08/19/2021	Figure 4 Figure 7 Figure 8	Updated New Package dimension Updated New part number Updated New Top view and Bottom view	Ming Hung Chen

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1 Introduction

JMS561 is a SuperSpeed USB 5Gb/s to dual SATA 6Gb/s bridge controller, which also supports various application configurations. It provides hardware RAID0 (striping) and RAID1 (mirror) over USB 2.0/USB 3.0/eSATA. There are flexible GPIOs for customized functions.

JMS561 complies with both USB Mass Storage Class Bulk-Only Transport (BOT) specification and USB Attached SCSI Protocol (UASP) specification. In addition to excellent system compatibilities, it also achieves high performance and low power consumption by advanced low power process.

2 Features

- Complies with Serial ATA International Organization: Serial ATA Revision 3.1
- Complies with Universal Serial Bus 3.0 Specification Revision 1.0
- Complies with USB Mass Storage Class Bulk-Only Transport (BOT) Rev. 1.0 Specification
- Complies with USB Attached SCSI Protocol (UASP) Rev. 1.0 Specification
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB 2.0/USB 3.0 power saving mode
- Supports multi LUNs for USB 2.0/USB 3.0
- Supports port multiplier for eSATA
- Supports hardware RAID0 (striping) and RAID1 (mirror) over USB 2.0/USB 3.0/eSATA
- Flexible GPIOs for customized functions
- Provides a hardware control PWM
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB3.0/eSATA
- Designed for Windows 7, Windows 8.1, Windows 10, MAC 10.9 or later versions
- 30MHz external crystal
- An embedded 3.3V to 1.2V voltage regulator
- An embedded 5.0V to 3.3V voltage regulator
- QFN 64 package

3 Block diagram

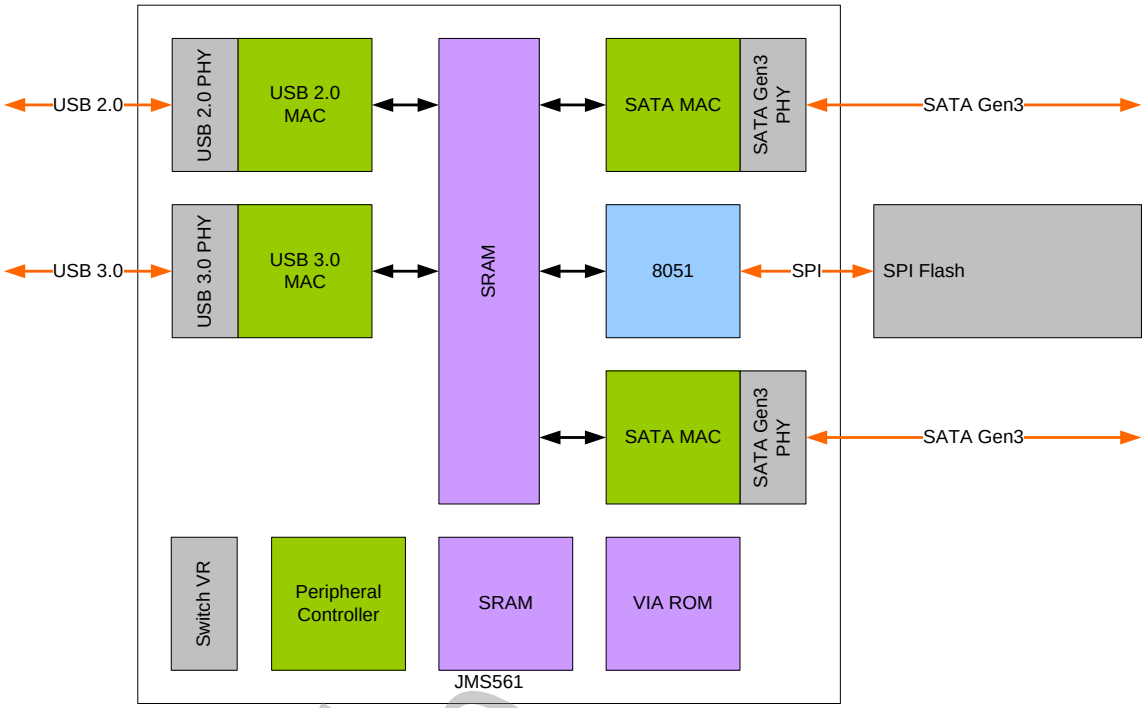


Figure 1 Block diagram

4 Application examples

4.1 USB 2.0 and USB 3.0 to two SATA 6Gb/s HDDs

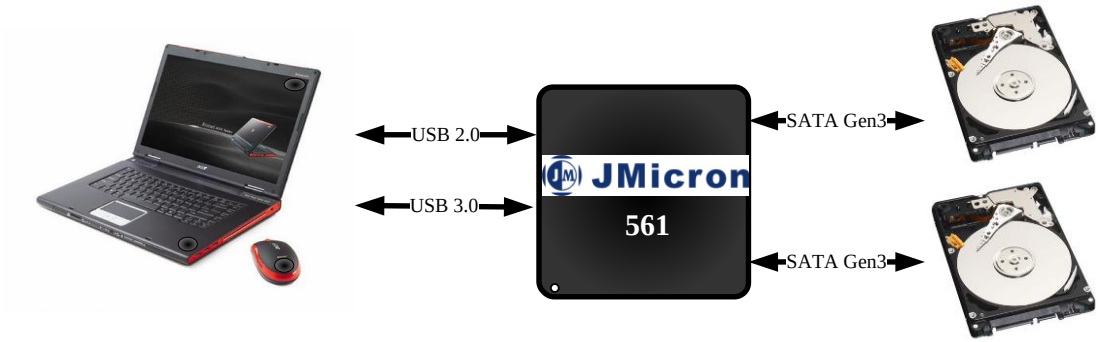


Figure 2 USB 2.0 and USB 3.0 to two SATA 6Gb/s HDDs

4.2 USB 2.0, USB 3.0 and eSATA to one SATA 6Gb/s HDDs

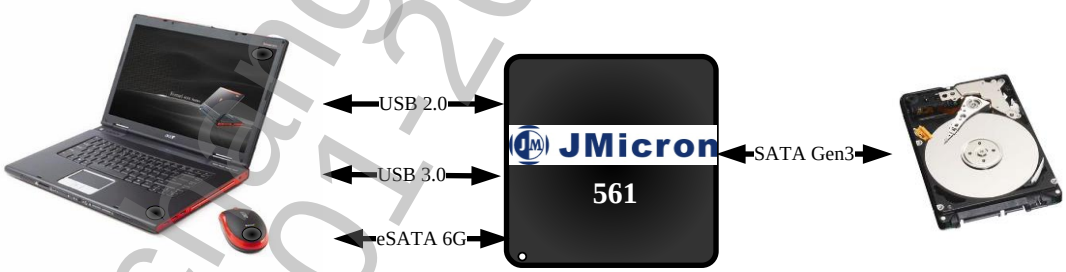
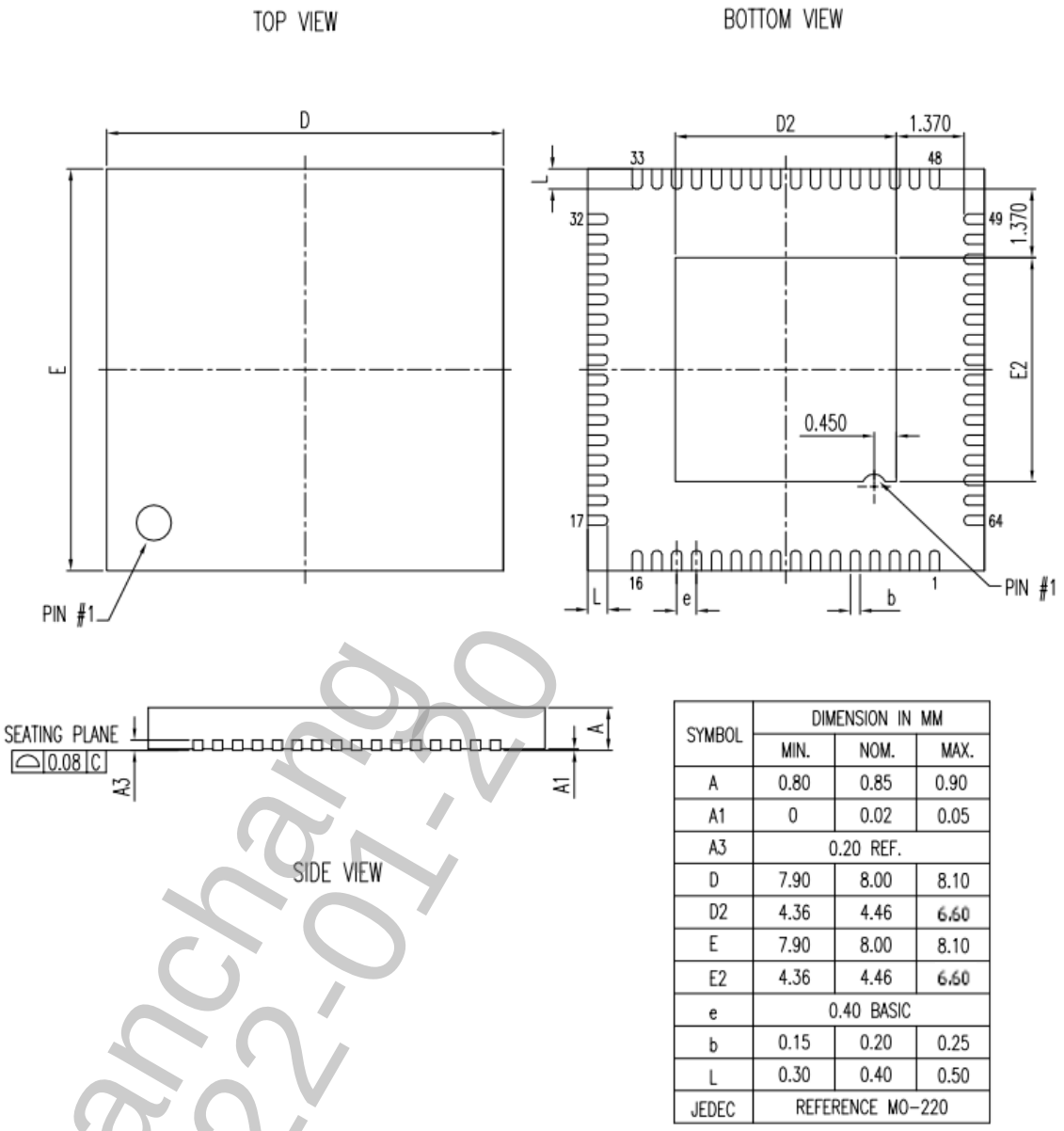


Figure 3 USB 2.0, USB 3.0 and eSATA to one SATA 6Gb/s HDDs

5 Package dimension



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3		0.20 REF.	
D	7.90	8.00	8.10
D2	4.36	4.46	4.60
E	7.90	8.00	8.10
E2	4.36	4.46	4.60
e		0.40 BASIC	
b	0.15	0.20	0.25
L	0.30	0.40	0.50
JEDEC		REFERENCE MO-220	

Figure 4 Package outline drawing of QFN64 8x8

6 Package pin-out

6.1 Pin assignment

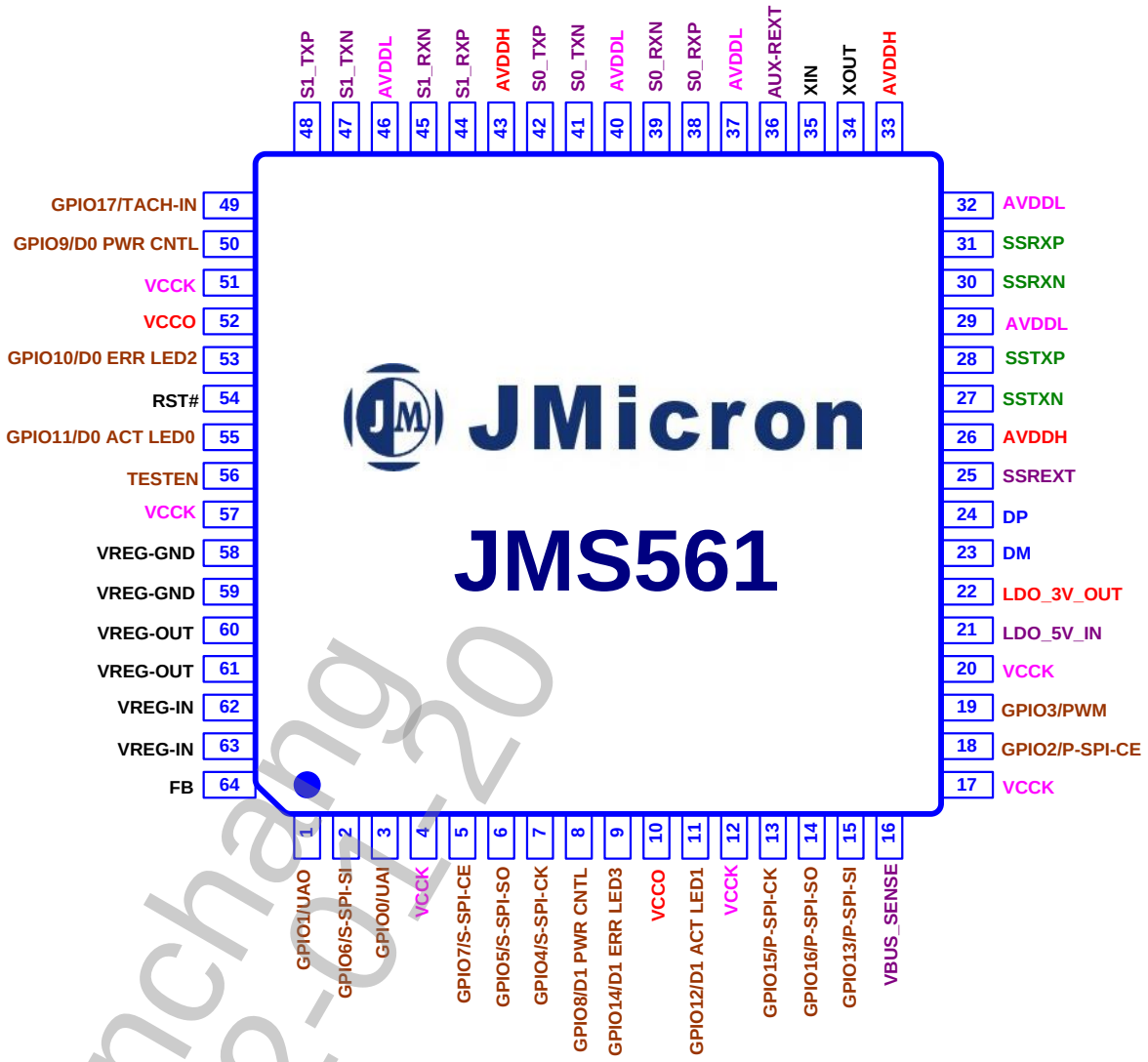


Figure 5 Pin assignment of JMS561

6.2 Pin type definition

Table 1 Pin type definition

Pin type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
L	Internal weak pull-low (Max. 164 kΩ, Typical 96 kΩ, Min. 61 kΩ)
H	Internal weak pull-high (Max. 141 kΩ, Typical 93 kΩ, Min. 66 kΩ)

6.3 Pin description

6.3.1 Serial ATA interface

Table 2 Pin description – Serial ATA interface

Signal Name	QFN 64	Type	Description
S0_RXP	38	AI	**SATA Port RX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S0_RXN	39	AI	**SATA Port RX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S0_TXP	42	AO	**SATA Port TX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S0_TXN	41	AO	**SATA Port TX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_RXP	44	AI	**SATA Port RX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_RXN	45	AI	**SATA Port RX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_TXP	48	AO	**SATA Port TX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.

Signal Name	QFN 64	Type	Description
S1_TXN	47	AO	**SATA Port TX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
REXT	36	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.

6.3.2 USB 3.0 interface

Table 3 Pin description – USB 3.1 Gen 1 interface

Signal Name	QFN 64	Type	Description
SSRXP	31	AI	**Super Speed RX+ Signal.**
SSRXN	30	AI	**Super Speed RX- Signal.**
SSTXP	28	AO	**Super Speed TX+ Signal.** A 100nF capacitor should be connected between this pin and USB connector.
SSTXN	27	AO	**Super Speed TX- Signal.** A 100nF capacitor should be connected between this pin and USB connector.
SSREXT	25	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.

6.3.3 USB 2.0 interface

Table 4 Pin description – USB 2.0 interface

Signal Name	QFN 64	Type	Description
DM	23	AIO	**USB 2.0 Bus D- Signal.**
DP	24	AIO	**USB 2.0 Bus D+ Signal.**
LDO_5V_IN	21	AI	**5V to 3.3V LDO Power Input.** This pin should be connected to the 5V input or USB connector 5V.
LDO_3V_ OUT	22	AO	**Capacitance for internal LDO of USB 2.0.** A capacitance to ground is recommended on this pin. The value should be 1uF. The output voltage range is 3.3V ±10%.
VBUS_ SENSE	16	AI	**USB 2.0/USB 3.0 Cable Power Input** This pin should be connected to USB connector 5V.

6.3.4 Crystal interface

Table 5 Pin description – Crystal interface

Signal Name	QFN 64	Type	Description
XIN	35	AI	**Crystal Input/Oscillator Input.** It is connected to a 30MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 3.3V±5%.
XOUT	34	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 3.3V±5% (input dependent).

6.3.5 Switching regulator interface

Table 6 Pin description – Switching regulator interface

Signal Name	QFN 64	Type	Description
VREG-GND	58,59	AI	**Switching Regulator Ground.**
VREG-OUT	60,61	AO	**Switch Output Pin.** An external inductor should be connected to this pin.
VREG-IN	62,63	AI	**Switching Regulator 3.3V Power Supply.**
FB	64	AI	**Feedback pin which is connected to 1V2 core voltage.**

6.3.6 Control and GPIO interface

Table 7 Pin description – Control and GPIO interface

Signal Name	QFN 64	Type	Description
RST#	54	DIS	**System Global Reset Input.** Active-low to reset the entire chip. An external RC should be connected to this pin. Please refer to the following section for detailed description.
TESTEN	56	DIS	**MP Test Mode Enable.** This pin is reserved for IC mass production testing. Please set this pin to low under normal operation.
GPIO[0]	3	DIOH	**8051 UART Output / GPIO [0].** This pin only preserves for SATA side UART function.
GPIO[1]	1	DIOH	**Buzzer Output / GPIO [1].** This pin only preserves for buzzer function.
GPIO[2]	18	DIOH	**Primary Serial Flash (CE) / GPIO [2]** This pin only preserves for SPI chip enable.
GPIO[3]	19	DIOH	**FAN OUT / GPIO [3].** This pin only preserves for FAN function.
GPIO[4]	7	DIOH	**RAID SET Button / GPIO [4]** This pin can be set hardware RAID mode by RAID mode set0 and RAID set 1 push after 3 seconds.
GPIO[5]	6	DIOH	**RAID MODE SET 0 / GPIO [5]** This pin can be set RAID mode with GPIO 7.

Signal Name	QFN 64	Type	Description
GPIO[6]	2	DIOH	**8051 UART Output / GPIO [6]** This pin only preserves for USB side UART function.
GPIO[7]	5	DIOH	**RAID MODE SET 1 / GPIO [7]** This pin can be set hardware RAID mode with GPIO 5. **PM** / **RAID 0** / **RAID 1** / **LARGE** **GPIO 5**: H / L / H / L **GPIO 7**: H / L / L / H
GPIO[8]	8	DIOH	**HDD 1 Power control / GPIO [8].** This pin only preserves for enable hard drive power.
GPIO[9]	50	DIOH	**HDD 0 Power control / GPIO [9].** This pin only preserves for enable hard drive power.
GPIO[10]	53	DIOH	**ERR & Identify LED 0 / GPIO [10].** This pin can be programmed by customized firmware.
GPIO[11]	55	DIOH	**GPIO [11].** This pin can be programmed by customized firmware.
GPIO[12]	11	DIOH	**GPIO [12].** This pin can be programmed by customized firmware.
GPIO[13]	15	DIOH	**GPIO [13]** This pin can be programmed as special function or normal GPIO function.
GPIO[14]	9	DIOH	**ERR & Identify LED 1 / GPIO [14].** This pin can be programmed by customized firmware.
GPIO[15]	13	DIOH	**GPIO [15]** This pin can be programmed as special function or normal GPIO function.
GPIO[16]	14	DIOH	**GPIO [16]** This pin can be programmed as special function or normal GPIO function.
GPIO[17]	49	DIOH	**GPIO [17].** This pin only preserves for FAN function.

6.3.7 Power supply

Table 8 Pin description – Power supply interface

Signal Name	QFN 64	Type	Description
VCCO	10,52	P	**Digital I/O Power Supply.**
VCCK	4,12,17 20,51,57	P	**Digital Core Power Supply**.
AVDDH	26,33,43	P	**Analog I/O Power Supply.**
AVDDL	29,32,37 40,46	P	**Analog Core Power Supply.**

6.4 LED indicator

If user has an application for LED function, please contact JMicron's AE before PCB layout..

6.5 GPIO initial value

All GPIOs set as input mode with pull-high resistor while in reset.

7 Clock and reset

7.1 Crystal input

Single crystal input (30MHz) is needed.

7.2 Reset input

The reset input pin is the Schmitt trigger input pin. All functions will be initialized by reset except the Analog Power-On Reset Circuit depending on the Power on-off.

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8 Electrical characteristics

8.1 Absolute maximum rating

Table 9 Absolute maximum rating

Parameter	Symbol	Condition	Min	Max	Unit
Digital I/O power supply	$VCCO_{(ABS)}$		-0.3	3.47	V
Digital core power supply	$VCCK_{(ABS)}$		-0.3	1.26	V
Analog I/O power supply	$AVDDH_{(ABS)}$		-0.3	3.47	V
Analog core power supply	$AVDDL_{(ABS)}$		-0.3	1.26	V
USB VBUS power supply	VBUS		-0.3	5.5	V
Digital I/O input voltage	$V_{I(D)}$		-0.3	3.47	V
Storage Temperature	$T_{STORAGE}$		-40	150	°C

8.2 Operating voltage and temperature

Table 10 Operating voltage and temperature

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital I/O power supply	VCCO		3.13	3.3	3.47	V
Digital core power supply	VCCK		1.14	1.2	1.26	V
Analog I/O power supply	AVDDH		3.13	3.3	3.47	V
Analog core power supply	AVDDL		1.14	1.2	1.26	V
Digital I/O input voltage	$V_{I(D)}$		0	3.3	3.47	V
Ambient operation temperature	T_A		0		70	°C
Junction Temperature	T_J				125	°C

8.3 External clock source conditions

Table 11 External clock source conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				30		MHz
Clock Duty Cycle			45	50	55	%

8.4 Power Supply DC Characteristics

The maximum and minimum values are measured at the max and min power supply levels respectively.

8.4.1 USB 2.0 to SATAx2 mode

8.4.1.1 @S0 state

Table 12 Power dissipation – USB 2.0 to SATAx2 @S0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V	VCCO and ACDDH	Operate @3.3V	40.5	48.6	56.0	mA
1.2V	VCCK and AVDDL	Operate @1.2V	325.4	328.3	332.4	mA

8.4.1.2 @S4 state

Table 13 Power dissipation – USB 2.0 to SATAx2 @S4 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V	VCCO and ACDDH	Operate @3.3V	2.0	3.0	4.0	mA
1.2V	VCCK and AVDDL	Operate @1.2V	2.0	3.0	4.0	mA

8.4.2 USB 3.0 to SATAx2 mode

8.4.2.1 U0 state (Operation)

Table 14 Power dissipation – USB 3.0 to SATAx2 U0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V	VCCO and ACDDH	Operate @3.3V	45.9	53.9	61.3	mA
1.2V	VCCK and AVDDL	Operate @1.2V	450.6	455.4	477.7	mA

8.4.2.2 U3 state (Suspend)

Table 15 Power dissipation – USB 3.0 to SATAx2 U3 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V	VCCO and ACDDH	Operate @3.3V	3.0	3.0	3.1	mA
1.2V	VCCK and AVDDL	Operate @1.2V	7.0	7.0	7.1	mA

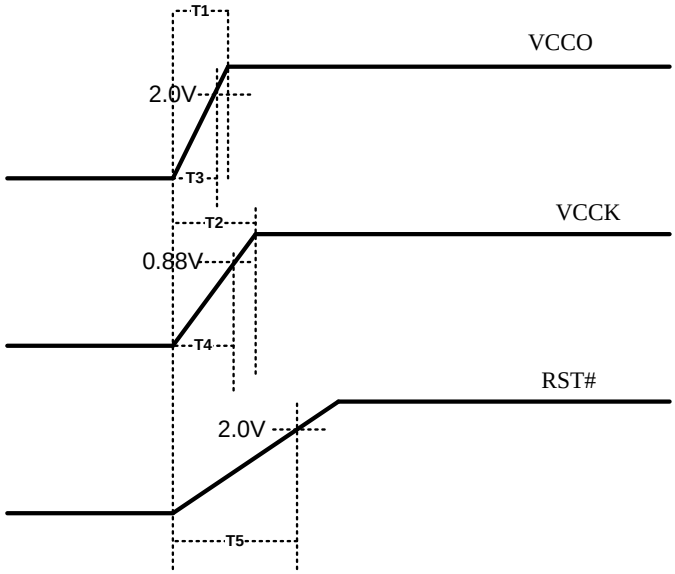
8.5 I/O DC characteristics

Table 16 I/O DC characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}				0.7	V
Input high voltage	V_{IH}		1.5			V
Output low voltage	V_{OL}				0.3	V
Output high voltage	V_{OH}		1.9			V

8.6 Power-on sequence

The Power-On sequence rules are defined in this section. Designers should follow all the rules for external power designs. Detailed explanations are listed as below.



T1: Rise time for 3.3V power rail from 0.0V to 3.3V

T2: Rise time for 1.2V power rail from 0.0V to 1.2V

T3: Rise time for 3.3V power rail from 0.0V to 2.0V

T4: Rise time for 1.2V power rail from 0.0V to 0.88V

T5: Rise time for RST# signal from 0.0V to 2.0V

The recommended power sequence and timing requirements are listed in Table 24.

Figure 6 Power-on sequence

Table 17 Power-on timing requirements

Time	Minimum	Maximum
T1	0.0 ms	10 ms
T2	0.0 ms	10. ms
T3	0.0 ms	8 ms
T4	0.0 ms	8 ms
T5	67 ms	-

The RESET timing constrain is based on the external RC reset circuits. In order to control the charge and discharge time for RC circuits, minimum and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be minimum value. In other words, the maximum value can be skipped without problems.

9 Product naming rule and order information

9.1 Format of the part number

The part number consists of the information of provider, product category, device number, package type, material type, product grade (operating temperature), mask ROM version and device version. Format of the part number is illustrated in Figure 7 below.

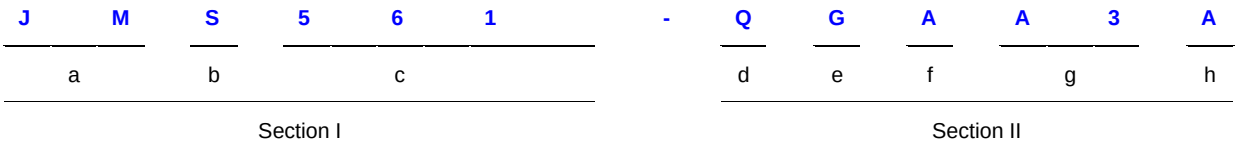


Figure 7 Format of the part number

9.2 Explanation of the part number

Table 25 explains each portion of the part number defined in Figure 7.

Table 18 Explanation of the part number

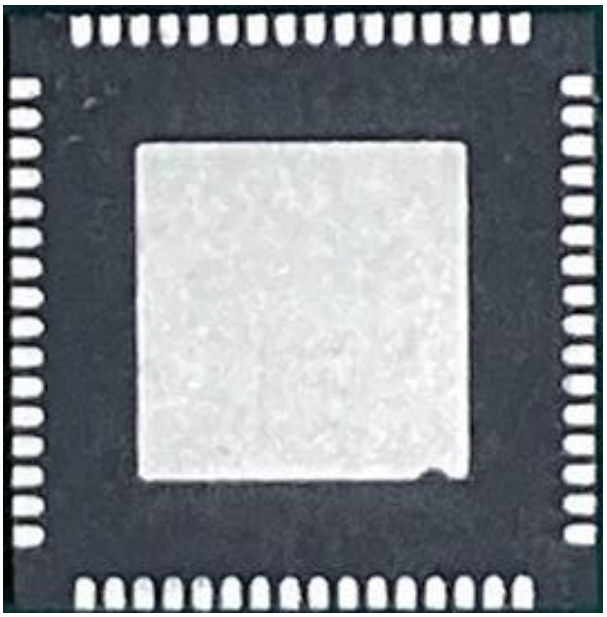
Section	Length	Purpose	Code(s)	Meaning
a	2 digits	Brand name	JM	**JM**icron
b	1 digit	Product category	S	**S**uper**S**peed USB
c	3 digits	Device number	561	Serial number assigned randomly to form the device name "**JMS561**" in conjunction with brand name and product category.
d	1 digit	Package type	Q	**Q**FN
e	1 digit	Material & grade	G	RoHS compliant **G**reen product with JEDEC MSL3 and commercial grade with the operating ambient temperature ranged from 0 to 70°C.
f	1 digit	Internal bonding type	A	Wire bonding option **A**
g	2 digit	Version of mask ROM	A3	Version **A3**
h	1 digit	Version of the IC	A	Version **A**

9.3 Top mark

Each device has its unique top mark containing information of the provider, device name, part number, manufacturing date code, lot number and pin 1 identifier. The top mark of each device is illustrated in Figure 8.

JMS561-QGAA3A – Top view

JMS561-QGAA3A – Bottom view



Top mark definition

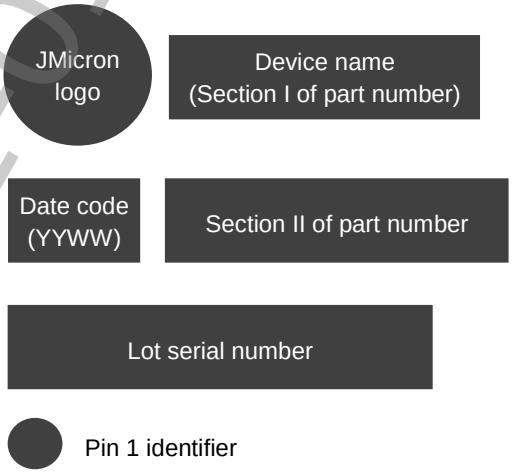


Figure 8 Illustration of device top mark