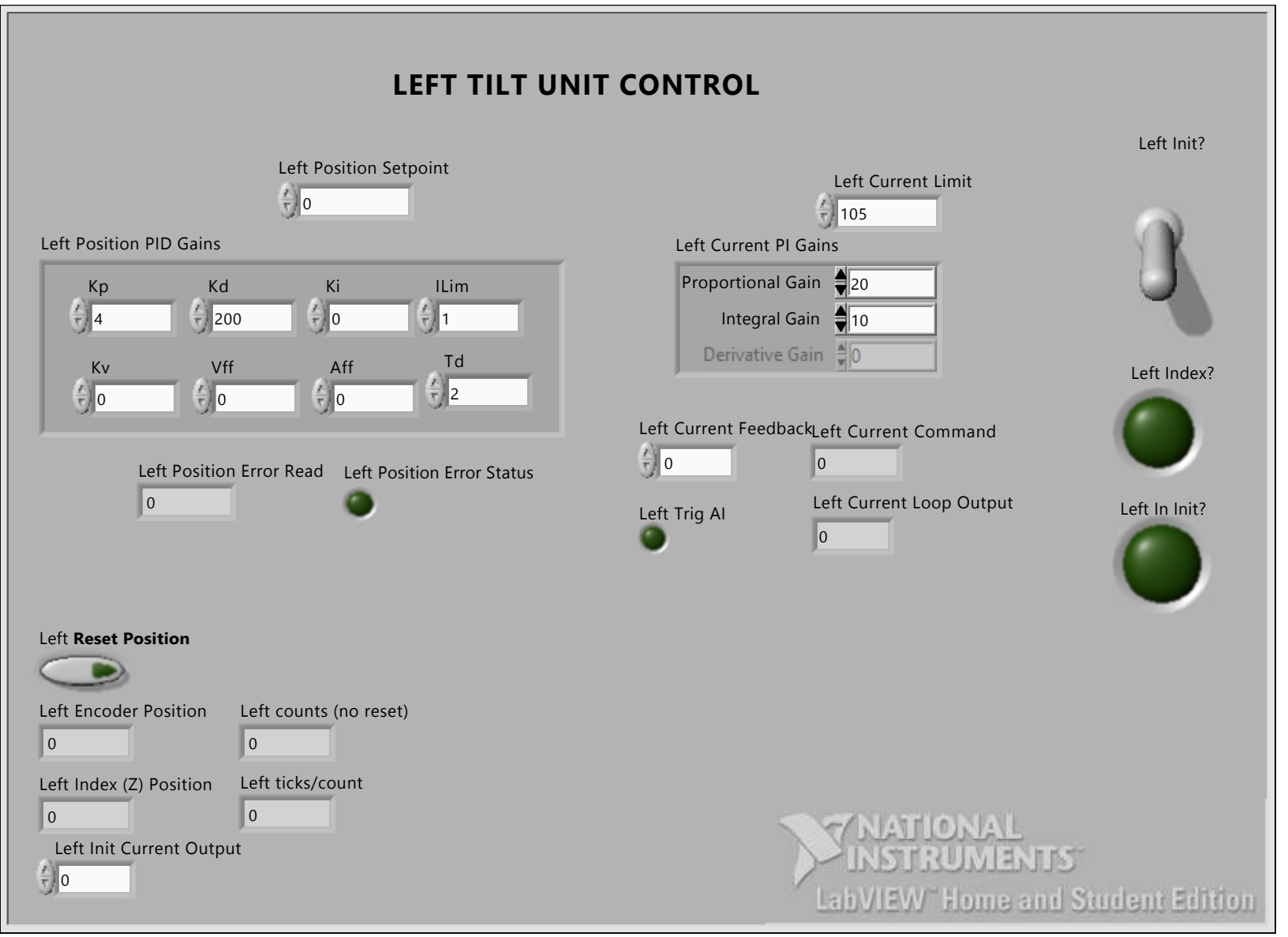
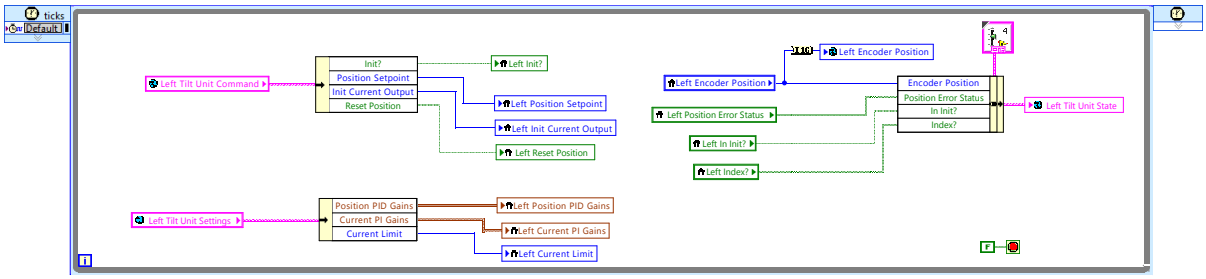
LeftTU.vi


LEFT TILT UNIT CONTROL
Left Position Setpoint
0
Left Current Limit
105
Left Init?
Left Position PID Gains
Kp
4
Kd
200
Ki
0
ILim
1
Kv
0
Vff
0
Aff
0
Td
2
Left Current PI Gains
Proportional Gain
20
Integral Gain
10
Derivative Gain
0
Left Index?
Left Current Feedback
0
Left Current Command
0
Left Position Error Read
0
Left Position Error Status
Left Trig AI
Left Current Loop Output
0
Left In Init?
Left Reset Position
Left Encoder Position
0
Left counts (no reset)
0
Left Index (Z) Position
0
Left ticks/count
0
Left Init Current Output
0
NATIONAL INSTRUMENTS
LabVIEW Home and Student Edition

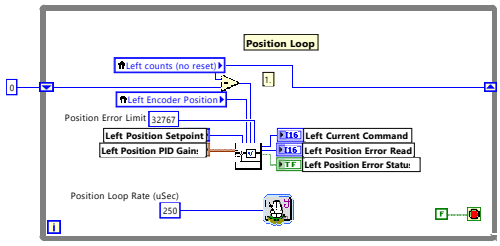
LEFT TU

This loop simply handles the information exchange between the TU subvi and the rest of hindbrain and above

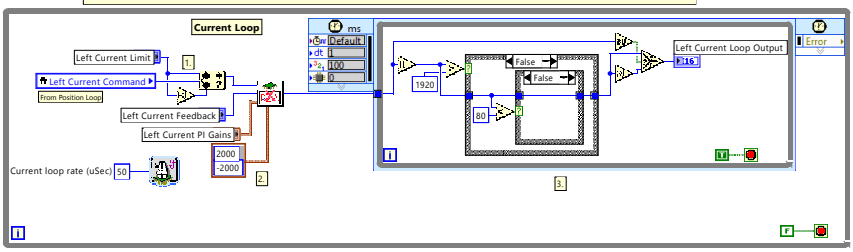


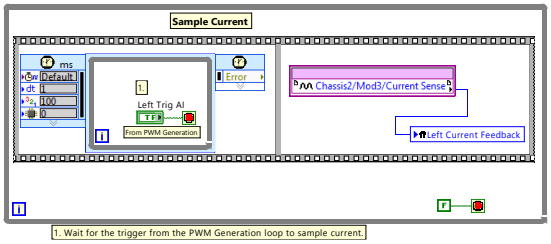
This loop is used to move to the position defined by Position Setpoint. The output, Current Command, feeds the Current Loop. The loop consists of a closed loop PID, with the feedback and velocity coming from the Encoder Loop.

1. The velocity is calculated as counts/loop by reading the subtracting the last count from the current count.

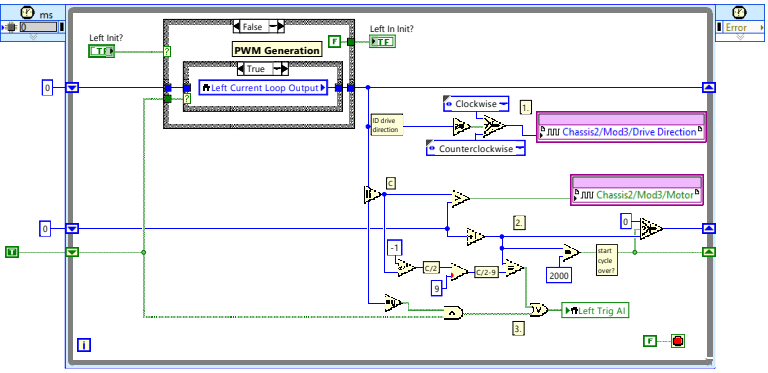


1. If the commanded current (current setpoint) is greater than the current limt, coerce the input to the PI loop to the current limit.
2. The constants of +/-2000 are used to set the output limit of the PI loop. The output is used as the duty cycle for the PWM generator. Since the PWM rate is 20kHz, which corresponds to 2000 FPGA tick counts @40MHz, the PI loop should not output anything greater than 2000. The sign of the PI loop output (PWM Duty Cycle indicator) specifies the drive direction.
3. The controller used to generate the PWM to the motor has a minimum pulse width (high or low) requirement of 2us. With 20kHz switching, which the above example shows, this results in a usable duty cycle range of 4% to 96%. However, it can generate duty cycles of 100% and 0%. If the commanded duty cycle is >96%, it is coerced to 100%, <4% is coerced to 0%.

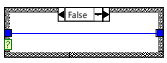


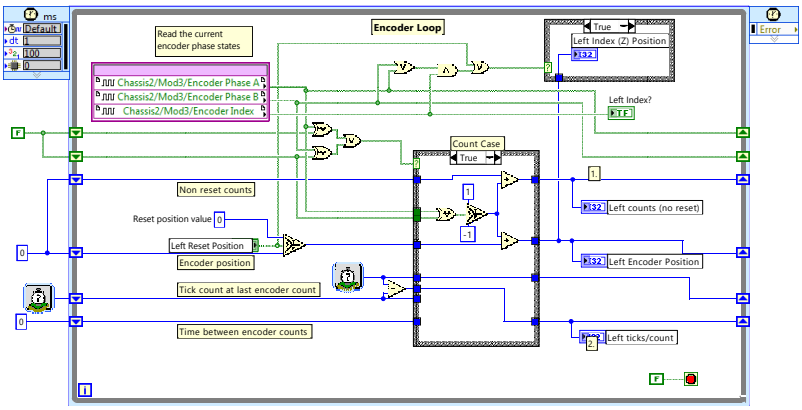


1. Wait for the trigger from the PWM Generation loop to sample current.

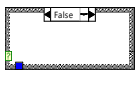


1. The sign bit of the PWM Duty Cycle specifies drive direction. A positive number is clockwise, negative is counterclockwise.
2. A counter in conjunction with a single-cycle timed loop, assuming a 40 MHz FPGA clock, is used to generate a PWM frequency of 20 kHz (2000 ticks).
3. The Trig AI is used to trigger sampling of the current. Sampling occurs at half the PWM duty cycle time (high time). Since it takes 9 ticks from the time a trigger is sent until the current is sampled, a trigger is sent 9 ticks before the desired sampling point.





1. "counts (no reset)" is used to facilitate calculation of velocity in FPGA. For example, it can be used to calculate counts/loop of a position loop without erroneous values caused by "Reset Position".
2. "ticks/count" is used in RT to calculate velocity by utilizing the accuracy of the FPGA system clock.
3. Count Case (False Case) - If no quadrature counts are detected for >0.5 seconds, "ticks/count" is set to 0 to indicate a velocity of 0. Assumes an FPGA system clock rate of 40 MHz.



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