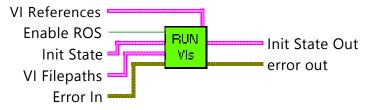
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Page 1 RUN VIs Printed on 5/8/2016 at 10:04 AM

VI References **FPGA Comms** Enable ROS **ROS Comms** Error In status code Mission Clock **⊘** ⊕ do source Cam Processes VI Filepaths Init State Out FPGA Comms Camera FPGA Ref C:\User...\FPGACommunication\MaintainFPGACommunication.vi Mission Clock Hindbrain Settings Microstrain C:\Users\jpoh\Docume...\Code\Utilities\MaintainMissionClock.vi Hindbrain Run NavComm **ROS Comms** C:\Users\jpoh\D...\Code\ROS\Midbrain\ROS_Midbrain_Network.vi **FPGA Comms** XBox Controller Cam Processes FPGA Comms Init Left TU C:\Users\jpoh\Document...\trunk\GatorLV\Code\AllImaging.vi MissionClock Right TU Ros Comms Init State FPGA Ref Camera Camera Processes **Hindbrain Settings** Microstrain error out NavComm Hindbrain Run status code FPGA Comms XBox Controller source **FPGA Comms Init** Left TU MissionClock Right TU THATHONIAL

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Page 3 RUN VIs

